

High-performance InGaN μ LEDs integrated onto flexible substrates

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Flexible optoelectronic systems, from wearable biomedical devices to conformal displays, demand light sources that combine high efficiency with mechanical compliance. Indium Gallium Nitride (InGaN) microLEDs (μ LEDs) are a leading candidate, yet two constraints have limited their adoption on flexible platforms: lateral scaling into the few-micrometer regime often incurs severe efficiency losses, and high-quality III-nitride epitaxy requires high-temperature growth on rigid substrates.

This thesis shows that the size-dependent efficiency degradation of scaled μ LEDs is largely governed by process-induced surface recombination that can be systematically suppressed. A device-centric framework is developed to decouple electrical injection, internal radiative efficiency, photon extraction, and mechanical integration, enabling the dominant loss mechanisms to be isolated and addressed in a deliberate hierarchy.

Optimized ohmic contacts to n-type Gallium Nitride (n-GaN) and p-type Gallium Nitride (p-GaN) establish a low-loss electrical baseline for interpreting size effects. Sidewall-induced Shockley–Read–Hall (SRH) recombination is identified as the primary scaling-limited loss and is quantified through a practical critical diameter, critical diameter (d_{crit}), separating bulk- and surface-dominated regimes. Combined chemical sidewall repair and polymeric encapsulation reduce the surface recombination velocity (v_s) from $\sim 3 \times 10^3 \text{ cm s}^{-1}$ to below 10 cm s^{-1} , with model extrapolation predicting a shift in d_{crit} from $43 \text{ }\mu\text{m}$ to below $0.1 \text{ }\mu\text{m}$; experimentally, no size-dependent efficiency penalty was observed over the measured diameter range of 6 to $17 \text{ }\mu\text{m}$.

With surface losses suppressed, geometry-driven extraction strategies become viable: perforated device architectures introduce internal sidewalls to enhance light extraction without a recombination penalty. Fully optimized devices are then transferred from sapphire onto polyethylene naphthalate substrates (PEN) via a photonic-assisted process while preserving reverse leakage below 100 fA and wall-plug efficiency (WPE) ($\sim 28\%$). Back-side potassium hydroxide (KOH) texturing of the exposed n-polar Gallium Nitride (GaN) raises the peak WPE of $5 \text{ }\mu\text{m}$ devices to $\sim 31\%$, with less than 5% variation under bending at an 11 mm radius of curvature (ROC).

Overall, the results show that surface and interface physics set the practical performance limits of scaled InGaN μ LEDs. The framework developed here provides guidance for engineering efficient, mechanically compliant light sources for high-resolution displays and biophotonic systems.

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I am grateful for the opportunity to intern at Apple during my PhD. During my internship, I had the privilege of interacting with nearly thirty exceptionally talented engineers every day. Keeping up with them was not always easy, to say the least. What stood out most was not only their technical depth, but also the way they approached problems. They challenged me to become a better engineer, taught me to ask better questions, and showed me the importance of never being satisfied until the root cause is understood. It was an unforgettable experience that had a lasting impact on how I think and work.

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Dedication

This thesis is dedicated to my wife, Irina, the love of my life, and to Ollie, who brings us endless joy.

Table of Contents

Examining Committee Membership	ii
Author’s Declaration	iii
Abstract	iv
Acknowledgements	v
Dedication	vii
List of Figures	xii
List of Tables	xxiv
List of Abbreviations	xxv
1 Introduction	1
1.1 Background and Motivation	1
1.2 Challenges in Scaled InGaN μ LEDs for Flexible Integration	2
1.3 Design Approach and Thesis Strategy	4
1.4 Scope and Organization of the Thesis	6

2	Ohmic Contacts on GaN	7
2.1	Fundamentals of Metal-GaN Contacts	8
2.1.1	Basic Theory of Metal-Semiconductor Contacts	8
2.1.2	GaN-Specific Considerations for Ohmic Contacts	10
2.1.3	Contact Resistivity and Measurement Concepts	12
2.1.4	Contact Resistivity Measurement Using the Circular Transmission Line Method	13
2.2	Ohmic Contacts to n-GaN	17
2.3	Ohmic Contacts to p-GaN: Opaque Contacts	19
2.4	Ohmic Contacts to p-GaN: Transparent Contacts	22
3	Minimizing interface defects and enhancing optical brightness of μLEDs through polymeric encapsulants	26
3.1	Motivation and Scope	26
3.2	Device Fabrication and Sidewall Passivation Schemes	27
3.3	Electrical and Optical Characteristics of Passivated μ LEDs	27
3.4	Surface and Bulk Recombination Analysis	32
3.5	Implications for μ LED Scaling and Device Design	47
3.6	Summary	48
4	Enhancing the light extraction efficiency of perforated Indium Gallium Nitride micro-LEDs	50
4.1	Motivation and Scope	50
4.2	Device Fabrication	50
4.3	Electrical and Optical Characteristics of perforated μ LEDs	51
4.4	FDTD Simulations	54
4.5	Summary	59

5	High Efficiency InGaN μLEDs on flexible substrates	61
5.1	Motivation and Scope	61
5.2	Device Fabrication	62
5.3	Performance on Sapphire	63
5.4	Performance on Flexible PEN	63
5.5	Performance on Flexible PEN under bending conditions	72
5.6	Summary	76
6	Conclusion and Future Work	78
6.1	Conclusion	78
6.1.1	Design Guidelines for Scaled InGaN μ LEDs	79
6.2	Future Work	82
6.3	Published Articles and Conference Papers	84
	References	86
	APPENDICES	93
A	Details of materials and methods from Chapter 3	94
A.1	microLED Fabrication	94
A.2	Device Characterization	97
A.3	Structural Characterization	98
A.4	Recombination Parameter Fitting	99
A.5	Evaluation of Light-Extraction Efficiency Effects on Sidewall Coating Comparisons	101
B	Details of materials and methods from Chapter 4	103
B.1	microLED Fabrication	103
B.2	Device Characterization	105
B.3	FDTD Simulations	107

C	Details of materials and methods from Chapter 5	109
C.1	microLED Fabrication	109
C.2	microLED Transfer	111
C.3	Device Characterization	112
C.4	Recombination Parameter Fitting	113
C.5	Spectral Measurements	113
C.6	Structural Characterization	114
C.7	FDTD Simulations	115

List of Figures

1.1	Schematic of photon propagation in a planar GaN-based LED, illustrating direct emission, total internal reflection, substrate-guided modes, and lateral waveguiding paths. Adapted from [1].	4
2.1	Schematic energy band diagrams illustrating Schottky and ohmic contact formation at a metal–n-GaN interface. The left set of diagrams shows the Schottky contact case, where the metal work function $\phi_m > \phi_n$, resulting in the formation of an energy barrier at the interface and rectifying IV behavior. The right set of diagrams shows the ohmic contact case, where $\phi_m < \phi_n$, leading to a reduced barrier for electron injection and efficient carrier transport. For each case, the band alignment is shown before contact, after thermal equilibrium is established, and under applied forward and reverse bias.	9
2.2	GaN-specific considerations relevant to ohmic contact formation. (a) Schematic band diagram of GaN illustrating the wide bandgap ($E_g \approx 3.4$ eV) and electron affinity ($\chi \approx 4.1$ eV), which contribute to large energy barriers at metal–GaN interfaces. (b) Reported SBH as a function of metal work function for n-GaN and p-GaN, adapted from Greco <i>et al.</i> , illustrating the generally lower effective barriers achievable on n-GaN compared to p-GaN.[2] (c) Schematic multilayer metal stack commonly employed for n-GaN ohmic contacts, consisting of a low-work-function contact layer, an overlayer promoting intermetallic formation, a high-melting-point diffusion barrier, and a protective cap layer. (d) Schematic illustration of the evolution of carrier transport mechanisms at the m-sc interface with increasing near-interface doping concentration, showing the transition from TE to TFE; adapted from Greco <i>et al.</i> [2]	11

2.3	(a) Top-down schematic of the c-TLM test structures and four-point measurement configuration. Concentric metal contacts (grey) with inner radius r_1 and outer radius r_2 are patterned on the semiconductor (blue), defining a gap $d = r_2 - r_1$. Structures with increasing r_2 are used to decouple lateral sheet resistance from the m-sc interface resistance. (b) Cross-sectional schematic of a c-TLM structure illustrating current flow beneath the metal contacts within the n-GaN layer. (c) Representative experimental I-V curves measured from multiple c-TLM structures with varying r_2 (or equivalently, varying d), exhibiting nonlinear behavior characteristic of a Schottky contact. (d) Representative linear I-V characteristics indicative of an ohmic contact. (e) Extracted total resistance R_{tot} plotted versus $\ln(r_2/r_1)$ for an ohmic contact. The linear dependence validates the c-TLM model and enables extraction of the sheet resistance, transfer length L_T , and specific contact resistivity ρ_c	15
2.4	Experimental c-TLM results for Cr/Al/Ni/Au (5/100/30/100 nm) ohmic contacts to n-GaN before annealing (red) and after annealing (blue). (a) Measured IV characteristics for multiple c-TLM structures with different gap spacings d , corresponding to $d = 10 \mu\text{m}$ (circles), $15 \mu\text{m}$ (triangles), $20 \mu\text{m}$ (rectangles), and $25 \mu\text{m}$ (squares). Annealed contacts exhibit significantly lower resistance, evidenced by the increased slope of the IV curves. (b) Extracted total resistance R_{tot} as a function of $\ln(r_2/r_1)$ calculated from the data in (a). The dashed red line indicates the linear extrapolation used for parameter extraction. (c) Specific contact resistivity ρ_c for annealed and non-annealed contacts. Semi-transparent solid symbols represent individual extracted values, the hollow triangle denotes the mean value, and error bars indicate the standard deviation ($N = 4$ for non-annealed and $N = 3$ for annealed).	18
2.5	Experimental results for Pd/Ni/Au (30/10/200 nm) contacts to p-GaN. (a) Extracted total resistance R_{tot} plotted versus $\ln(r_2/r_1)$ from c-TLM measurements before annealing (red) and after annealing (blue), illustrating comparable linear behavior with modest improvement after annealing. (b) JV characteristics of a $6 \mu\text{m}$ μLED measured over a -3 to 5 V sweep. Hollow semi-transparent circles denote individual data points, while triangles indicate the mean response of two devices. The inset shows a cross-sectional schematic of the μLED structure, highlighting the p-GaN and n-GaN ohmic contacts.	21

- 2.6 Experimental characterization of transparent ITO p-contacts on p-GaN. (a) IV characteristics of c-TLM structures with a fixed gap spacing of $d = 10 \mu\text{m}$ for different ITO contact stacks. ITO Type 1 (purple) corresponds to the baseline ITO process. ITO Type 2 (blue) consists of a bilayer ITO stack with a $\sim 10 \text{ nm}$ low-power (low-damage) ITO layer followed by $\sim 70 \text{ nm}$ of standard ITO. ITO Type 3 (red) is identical to Type 2, except that the initial low-power ITO layer is deposited at elevated chamber pressure. ITO Type 4 (green) is a quadlayer stack comprising an ultra-thin Ni/Au interlayer, a low-damage ITO layer, and a standard ITO overlayer. Inset: optical micrograph of patterned ITO Type 4 contacts on a sapphire-based LED epitaxial wafer, illustrating high optical transparency. (b) JV characteristics of $6 \mu\text{m}$ μLED fabricated using the optimized transparent p-contact (ITO Type 4). Hollow semi-transparent circles represent individual data points, hollow triangles denote the mean value across $N = 4$ devices, and the solid line is provided as a visual guide and does not represent a fit. Error bars indicate the standard deviation. Inset: cross-sectional schematic of the μLED structure highlighting the optimized p-contact (ITO Type 4) and n-contact. 23
- 3.1 Size- and sidewall-coating-dependent efficiency of micro light-emitting diodes. Peak wall-plug efficiency plotted as a function of micro light-emitting diode diameter for devices incorporating silicon dioxide (red diamonds) and SU-8 (blue rectangles) sidewall coatings. Symbols represent mean values, and error bars indicate one standard deviation. Semi-transparent circles denote individual device measurements used to calculate the mean values, with colors corresponding to the associated sidewall coating scheme. Dotted lines are included as visual guides and do not represent fitted models. Sample sizes were $N = 3$ devices for silicon dioxide and $N = 4$ devices for SU-8. 28

- 3.2 Sidewall-coating-dependent electrical characteristics of 6 μm micro light-emitting diodes. (a) Semi-logarithmic current–voltage characteristics for devices incorporating silicon dioxide (red diamonds) and SU-8 (blue rectangles) sidewall coatings. (b) Corresponding ideality factor extracted as a function of applied voltage for the same devices. The voltage range used for ideality factor extraction is indicated in panel (a) by the dashed box. Symbols represent mean values, and error bars indicate one standard deviation. Semi-transparent circles denote individual device measurements used to calculate the mean values, with colors corresponding to the associated sidewall coating scheme. Dotted lines are included as visual guides and do not represent fitted models. Sample sizes were $N = 3$ devices for silicon dioxide and $N = 4$ devices for SU-8. 31
- 3.3 Opto-electrical efficiency of micro light-emitting diodes with different sidewall coatings. (a) Wall-plug efficiency as a function of current density for silicon dioxide-coated micro light-emitting diodes. (b) Wall-plug efficiency as a function of current density for SU-8-coated micro light-emitting diodes. Micro light-emitting diode diameters are indicated by 6 μm (yellow diamonds), 12 μm (blue squares), and 17 μm (red triangles). Symbols represent mean values, and error bars indicate one standard deviation. Semi-transparent symbols denote individual device measurements used to calculate the mean values, with colors corresponding to the associated device diameter. Dotted lines are included as visual guides and do not represent fitted models. Sample sizes were $N = 3, 3$, and 4 devices for silicon dioxide-coated micro light-emitting diodes with diameters of 6 μm , 12 μm , and 17 μm , respectively, and $N = 4$ devices for each SU-8-coated diameter. 33
- 3.4 Normalized Shockley–Read–Hall recombination as a function of μLED size. Normalized total Shockley–Read–Hall recombination rate, expressed as A/A_0 , plotted as a function of μLED diameter d for devices with silicon dioxide (red solid line) and SU-8 (blue solid line) sidewall coatings. Values of A/A_0 are extracted from fitting the external quantum efficiency model to the experimental data, as described in Appendix A.4. The inset equation shows the size-dependent Shockley–Read–Hall recombination model, where A is the total recombination coefficient, A_0 is the bulk contribution, v_s is the surface recombination velocity, and d is the μLED diameter. The horizontal black line at $A/A_0 = 2$ indicates the condition where bulk and surface Shockley–Read–Hall recombination contributions are equal. Vertical dashed lines mark the corresponding critical diameters d_{crit} for each coating scheme. 40

- 3.5 Extracted light extraction efficiency of SU-8 encapsulated μ LEDs. Extracted light extraction efficiency (LEE) plotted as a function of μ LED diameter for SU-8 encapsulated devices. Values are obtained from fitting the EQE model to the experimental data, as described in Appendix A.4. The plotted range and fitting model are limited to $LEE \leq 60\%$ to reflect the approximately 60% reflectivity of a 30 nm Pd contact at 460 nm. Inset: Peak wall plug efficiency (p-WPE, %) plotted as a function of current density (J , $A\ cm^{-2}$), normalized by the p contact area, highlighting the high current regime where lateral current spreading beyond the p contact is reduced and size dependent light extraction differences are apparent. Symbols depicting device diameters of 6 μm (yellow diamonds), 12 μm (blue squares), and 17 μm (red triangles) represent mean values; error bars indicate the standard deviation, and semi transparent symbols denote individual device measurements. Sample sizes in the inset were $N = 4$ devices for all μ LED diameters. Dotted lines are included as visual guides to aid interpretation and do not represent fitted models. 41
- 3.6 Opto electrical efficiency of SU-8 encapsulated μ LEDs with different sidewall treatments: Peak wall plug efficiency (p-WPE,%) plotted as a function of current density (J , $A\ cm^{-2}$) for μ LEDs with diameters of 6 μm (yellow diamonds), 12 μm (blue squares), and 17 μm (red triangles) without sidewall treatment (left) and with KOH treatment (right). Symbols represent mean values; error bars indicate the standard deviation. Semi transparent symbols denote individual device measurements used to calculate the mean. Dotted lines are included as visual guides to aid interpretation and do not represent fitted models. Green arrows indicate the qualitative variation in WPE with decreasing μ LED diameter. Sample sizes were $N = 3, 4$, and 4 devices for KOH treated μ LEDs with diameters of 6, 12, and 17 μm , respectively, and $N = 4$ devices for all untreated μ LED diameters. The untreated SU-8 data shown in the left panel are identical to the SU-8 dataset presented in Figure 3.3 (right panel) and are reproduced here for direct comparison. . . 43

- 3.7 (a) Extracted light extraction efficiency plotted as a function of μ LED diameter for untreated (red solid line) and KOH treated (blue solid line) devices. Values are obtained from fitting the EQE model to the experimental data, as described in Appendix A.4. The plotted range and fitting model are limited to light extraction efficiency $\leq 60\%$ to reflect the approximately 60% reflectivity of a 30 nm Pd contact at 460 nm. Inset: Tilted scanning electron micrograph of a 6 μ m μ LED following KOH treatment and prior to SU-8 encapsulation. (b) Extracted normalized Shockley–Read–Hall recombination rate (A/A_0) plotted as a function of μ LED diameter for untreated and KOH treated devices, obtained from fitting to the recombination model. The black horizontal line at $A/A_0 = 2$ indicates the condition where bulk and surface SRH recombination contributions are equal. 44
- 3.8 (a) Semi logarithmic current–voltage characteristics for SU-8 encapsulated 6 μ m μ LEDs without sidewall treatment (green rectangles) and with KOH treatment (purple triangles). (b) Corresponding mean ideality factor plotted as a function of applied voltage for the same devices, extracted over the voltage range highlighted in panel (a). Symbols represent mean values; error bars indicate the standard deviation. Semi transparent symbols denote individual device measurements used to calculate the mean. Sample sizes were $N = 4$ devices for untreated μ LEDs and $N = 3$ devices for KOH treated μ LEDs. 45
- 3.9 Size- and sidewall-coating-dependent efficiency of μ LEDs: Peak wall plug efficiency (p-WPE, %) plotted as a function of μ LED diameter for devices with SiO₂ (green circles), SiO₂ with KOH treatment (purple stars), SU-8 (blue rectangles), and SU-8 with KOH treatment (red diamonds). Symbols represent mean values; error bars indicate the standard deviation. Semi transparent symbols denote individual device measurements used to calculate the mean, with colors matching the corresponding coating condition. Dotted lines are included as visual guides to aid interpretation and do not represent fitted models. Sample sizes were $N = 4$ devices for all conditions. Exceptions were SU-8 with KOH at 6 μ m, SiO₂ with KOH at 17 μ m, and SiO₂ at 6 μ m and 12 μ m, where $N = 3$ 46

4.1	Electrical characteristics of planar and perforated InGaN μ LEDs. (a) Semi-logarithmic current density–voltage (JV) characteristics for a 10 μ m planar circular μ LED and a perforated μ LED containing a single internal hole (1×1 array), selected to have comparable net active areas. (b) Semi-logarithmic JV characteristics for perforated μ LEDs incorporating internal hole arrays of size 1×1 , 2×2 , 3×3 , 4×4 , and 5×5 , corresponding to device side lengths ranging from approximately 10 μ m to 32 μ m. (c) Ideality factor extracted as a function of applied voltage for the perforated μ LEDs shown in panels (a) and (b), evaluated over the forward-bias voltage range indicated. Symbols represent mean values and error bars denote one standard deviation. Semi-transparent symbols indicate individual device measurements. Sample sizes were $N = 3$ devices for both planar and 1×1 perforated μ LEDs in panel (a), and $N = 3$ devices for each perforated array size in panels (b) and (c).	53
4.2	Optical efficiency characteristics of planar and perforated InGaN μ LEDs. (a) Wall-plug efficiency (WPE) plotted as a function of current density J for planar and perforated μ LEDs corresponding to the devices characterized electrically in Figure 4.1(a). Data are shown for planar circular μ LEDs and perforated μ LEDs containing a single internal hole (1×1 array). Sample sizes were $N = 3$ devices for both planar and perforated μ LEDs. (b) Peak wall-plug efficiency (p-WPE) plotted as a function of net LED active area for planar and perforated μ LEDs. For planar devices, the data points correspond (from left to right) to circular μ LED diameters of 5, 6, 7, 8, 9, 10, 20, 100, 300, and 500 μ m, with sample sizes of $N = 3, 12, 12, 12, 9, 3, 3, 3, 3$, and 3, respectively. For perforated devices, the data points correspond (from left to right) to internal hole arrays ranging from 1×1 to 5×5 , with $N = 3$ devices measured for each perforation geometry. Symbols represent mean values; error bars indicate one standard deviation; and semi-transparent symbols denote individual device measurements.	55

4.3	Finite-difference time-domain (FDTD) simulation results for planar and perforated InGaN μ LEDs. (a) Schematic of the simulated device structure and FDTD simulation domain, showing the layered InGaN/GaN LED stack embedded in an epoxy medium, the detection plane used for power collection, and the perfectly matched layer (PML) boundaries. A single electric dipole source is placed within the multiple-quantum-well (MQW) plane. (b) Spatially averaged light extraction efficiency (LEE) obtained from FDTD simulations for planar and perforated μ LEDs as a function of lateral device size (10, 15, and 20 μ m). For each device size, results are averaged over multiple in-plane dipole positions and polarizations as described in Appendix B.3. (c) Two-dimensional maps of local LEE as a function of dipole position within the MQW plane for planar and perforated μ LEDs with lateral sizes of 10, 15, and 20 μ m. Perforated devices incorporate cylindrical air holes arranged as 1×1 , 2×2 , and 3×3 arrays for the 10, 15, and 20 μ m devices, respectively. The color scale indicates the local LEE, and blue circles denote the locations of the etched holes.	56
4.4	FDTD simulation results for planar and perforated InGaN μ LEDs. (a) Simulated far-field radiation intensity distributions for planar (top) and perforated (bottom) μ LEDs, obtained using near-to-far-field projection of the electromagnetic fields recorded above the device. (b) Coarse design-of-experiments (DOE) heatmap showing normalized spatially averaged light extraction efficiency (LEE) as a function of perforation pitch and fill factor, evaluated using a single in-plane dipole positioned at the device center. The dashed region indicates the parameter space selected for refinement. (c) Refined DOE heatmap within the highlighted region of panel (b), calculated using smaller pitch and fill-factor step sizes. (d) Two-dimensional map of local LEE as a function of dipole position for the optimized perforated μ LED geometry identified from the DOE sweep. The color scale denotes local LEE, and blue circles indicate the locations of the etched air holes. Simulation setup, dipole sampling strategy, normalization procedure, far-field projection, and DOE methodology are described in Appendix B.3.	58

5.1	Optoelectronic characteristics of 10 μm -diameter μLEDs fabricated on sapphire. (a) Mean current density–voltage (J–V) characteristics over the full bias range measured. Inset shows cross-sectional schematic of the μLED . (b) Ideality factor extracted as a function of applied voltage for the μLEDs shown in panels (a), evaluated over the forward-bias voltage range indicated. (c) Wall-plug efficiency as a function of current density, with an inset showing a microscope image of a 10 μm μLED with the p-contact indicated by the blue material. Sample sizes were $N = 5$ devices for all measurements. Symbols represent mean values and error bars denote one standard deviation. Semi-transparent symbols indicate individual device measurements.	64
5.2	Schematic illustration of the μLED transfer process. (1) μLED fabrication on sapphire substrates. (2) Bonding of fully processed μLEDs to a temporary carrier containing a light absorbing layer (LAL). (3) Removal of the sapphire substrate by laser lift-off (LLO) to expose the GaN epilayer. (4) Bonding of the μLEDs onto a flexible substrate. (5) Release of the temporary carrier to complete integration onto the flexible platform.	65
5.3	Normalized GaN (002) x-ray rocking curves measured for μLED samples on the native sapphire substrate, immediately following laser lift-off (LLO), and after PATP transfer onto a silicon carrier substrate. The full-width at half-maximum (FWHM) values were extracted from each rocking curve to evaluate changes in crystal quality during the transfer process.	66
5.4	Electrical and optoelectronic characteristics of 10 μm -diameter μLEDs comparing devices on sapphire ($N = 5$) and devices transferred onto PEN ($N = 3$): (a) mean J-V characteristics in reverse- and forward-bias regimes, (b) extracted ideality factor versus LED voltage, and (c) wall plug efficiency as a function of current density.	67

5.5	Backside KOH treatment and its impact on device structure and performance. (a) Cross-sectional schematic of the μ LED device structure incorporating backside KOH-induced GaN texturing. (b) SEM image of the planar backside GaN surface following LLO and HCl-based Ga residue removal; the inset shows an optical micrograph of the same region. (c) SEM image corresponding to (b) after KOH treatment, showing the formation of a textured backside surface; the inset shows the corresponding optical micrograph. (d) Ideality factor as a function of bias for 10 μ m μ LEDs ($N = 6$); purple diamond markers indicate mean values, semi-transparent circular markers represent individual measurements, and the solid line is included to guide the eye. (e) Peak WPE for each substrate condition; green square markers indicate mean values, semi-transparent circular markers represent individual devices, and the solid line is included to guide the eye; sapphire ($N = 5$), PEN ($N = 3$), and PEN with backside KOH ($N = 6$); the inset shows WPE as a function of current density for a 5 μ m μ LED with backside KOH, exhibiting a peak WPE of 31% at 3.3 A cm ⁻² . (f) Simulated FDTD spatial LEE maps for a 10 μ m μ LED with a planar backside (top, no KOH) and a textured backside (bottom, with KOH treatment).	69
5.6	Optical and electrical characterization of flexible μ LEDs following substrate transfer and under mechanical deformation. (a) Emission energy shift (ΔE) measured after transfer from sapphire to PEN substrates for μ LEDs of different diameters. (b) Representative normalized electroluminescence spectra of a 100 μ m μ LED on sapphire and PEN substrates. (c) Schematic and photographs of the flat, tensile, and compressive bending configurations with a radius of curvature (ROC) of 11 mm. (d) Emission energy shift measured under tensile and compressive bending at an ROC of 11 mm for μ LEDs of different diameters. (e) Normalized electroluminescence spectra of an 8 μ m μ LED under flat, tensile, and compressive bending conditions. (f) Normalized WPE as a function of current density for a 5 μ m μ LED under flat, tensile, and compressive bending conditions.	74
A.1	Comparison of untreated and KOH treated μ LED mesa sidewalls. (a) 35° tilted scanning electron micrograph of a 6 μ m μ LED mesa after GaN etching and SiO ₂ strip, without sidewall treatment. (b) Corresponding 35° tilted scanning electron micrograph of a 6 μ m μ LED mesa after KOH treatment, prior to SU-8 encapsulation. The p-GaN mesa and surrounding n-GaN region are labeled in both images. Scale bars, 1 μ m.	95

A.2	Sidewall and contact geometry of a 6 μm -diameter μLED after p-contact formation. A 35° tilted SEM image showing the p-contact, the LED mesa edge, and the surrounding n-GaN region. The radial separation between the p-contact edge and the mesa sidewall ($\Delta r \approx 1.7 \mu\text{m}$) is indicated. Scale bar: 1 μm	96
A.3	Schematic illustration of the final μLED device structures. (a) Schematic of a μLED with a SiO_2 bilayer sidewall coating, showing the p-contact, mesa, GaN layers, and sapphire substrate. (b) Schematic of a LED with SU-8 sidewall encapsulation, illustrating the corresponding device geometry and contact configuration. Schematics are not drawn to scale.	97
A.4	Fully fabricated 6 μm -diameter μLED s with different sidewall coatings. (a) 45° tilted SEM image of a fully fabricated 6 μm -diameter μLED incorporating a SiO_2 bilayer sidewall coating. (b) Corresponding 45° tilted SEM image of a fully fabricated 6 μm -diameter μLED with SU-8 encapsulation. Insets show higher-magnification views of the μLED top surface for each device. Scale bars: 25 μm (main images).	98
A.5	Measured and modeled external quantum efficiency of SiO_2 passivated and SU-8 encapsulated μLED s. External quantum efficiency (EQE, %) plotted as a function of current density (J , A cm^{-2}) for SiO_2 (a) SU-8 encapsulated μLED s without KOH treatment (b) and with KOH treatment (c). Symbols indicate measured EQE data, and solid lines represent the corresponding fitted EQE curves obtained from the model. Circle, triangle, and square symbols correspond to μLED diameters of 6 μm , 12 μm , and 17 μm , respectively.	101
A.6	Opto-electrical efficiency of 6 μm μLED s with different sidewall coatings: Wall plug efficiency (WPE, %) plotted as a function of current density (J , A cm^{-2}) for 6 μm μLED s with SU-8 (blue squares), SiO_2 (red circles), and combined SiO_2 /SU-8 (yellow diamonds) sidewall coatings. Symbols represent mean values; error bars indicate the standard deviation. Semi-transparent symbols denote individual device measurements used to calculate the mean. Dotted lines are included as visual guides to aid interpretation and do not represent fitted models. Sample sizes were $N = 4$ devices for SU-8, $N = 3$ devices for SiO_2 , and $N = 3$ devices for SiO_2 /SU-8.	102

B.1	Structural comparison of planar and perforated μ LEDs: Schematic cross sections (left) illustrate the epitaxial layer stack and mesa geometry for (top) a planar μ LED and (bottom) a perforated μ LED incorporating a periodic array of etched holes extending through the active region. Corresponding top-down renderings (center) show the circular mesa used for planar devices and the square mesa with an internal hole array used for perforated devices. SEM images (right) present the fabricated structures of a 10 μ m circular planar μ LED (top) and a 15.5 μ m side-length perforated μ LED with a 2×2 array of holes (bottom), with a 5 μ m scale bar, confirming the intended mesa profiles, hole placement, and overall pattern.	105
C.1	Cross-sectional schematic of the fabricated device structure showing the layered stack comprising SU-8 overcoat, ITO p-contact, Al/Cr/Au metal pads, MQW active region within p-GaN and n-GaN, u-GaN, and the sapphire substrate.	111
C.2	(a) Schematic illustration of the mechanical deformation conditions applied to flexible devices, including flat, tensile, and compressive bending configurations, where blue represents the μ LED layers and pink represents the flexible substrate. (b) Schematic of the custom measurement jig showing the base, curved fixture (tensile configuration shown), mounted μ LED/flexible sample, probing configuration, and optical collection path (light blue cone) through an aperture to the photodiode (PD). (c) CAD schematic of the fabricated base platform. (d) CAD schematic of the compressive jig fixture with a radius of curvature of 11 mm. (e) CAD schematic of the tensile jig fixture with a radius of curvature of 11 mm. (f) Optical photograph of a μ LED on a flexible substrate assembled on the tensile 11 mm radius of curvature jig, electrically probed during operation, with the base, photodiode, and optical emission visible.	114

List of Tables

3.1	Extracted sidewall-coating-dependent recombination coefficients and calculated N_{it} and d_{crit}	38
3.2	Performance parameters for the highest performance μ LED configuration with mean p-WPE = 20.3 %.	49
4.1	Geometric parameters and surface-to-volume ($S2V$) ratios for perforated square micro light-emitting diodes compared with equivalent planar square devices and equivalent circular devices.	52
5.1	Extracted efficiency parameters from EQE model fitting for μ LEDs on sapphire and PEN substrates.	72

List of Abbreviations

N_t bulk trap density 37

N_{it} interface trap density 34, 37

R_s series resistance 29, 30, 63

R_{sh} shunt resistance 29, 30, 63

d_{crit} critical diameter iv, 26, 37–39, 43, 44, 47, 48, 78, 80

v_s surface recombination velocity iv, 32–34, 37, 38, 40, 43, 45, 47, 48, 50, 52–54, 71, 72, 77, 78, 82, 99, 100

KOH potassium hydroxide iv, 27, 36, 42–45, 47–49, 51, 67–70, 72, 75, 76, 80, 81, 94, 95, 100, 104, 110, 111

SiO₂ silicon dioxide 27, 29–32, 36, 37, 39, 40, 45, 47, 94–97, 99, 101, 104, 110

ABCCD Shockley-Read-Hall, bimolecular, Auger, and drift–leakage recombination model 32, 34, 37, 99

ALD atomic layer deposition 27, 95, 96, 101

BOE buffered oxide etch 95, 104, 110

c-TLM circular transmission line method 7, 13–18, 20, 22, 24, 25, 96, 103, 104, 109, 110

EQE external quantum efficiency 5, 28, 32, 34–37, 43, 51, 62, 71, 98–100, 105, 106, 112

FDTD finite-difference time-domain 35, 54, 55, 59, 70, 76, 107, 115

FE field emission 12, 19

FWHM full width at half maximum 54, 64, 65, 73, 75, 115

GaN Gallium Nitride iv, 2, 3, 5–8, 10, 12–14, 17, 19, 20, 27, 29, 34, 35, 42, 54, 62–65, 67, 68, 71, 73, 76, 80, 94, 95, 104, 106, 107, 110, 111, 115

I current 29

ICP inductively coupled plasma 27, 51, 62, 104, 110

IF ideality factor 28–30, 32, 40, 44, 45, 49, 51–53, 62, 63, 66, 68, 70, 76, 106

InGaN Indium Gallium Nitride iv, x, 1, 2, 13, 27, 34, 35, 40, 42, 48, 50, 54, 61, 62, 70, 72, 73, 76–82, 94, 103, 107, 109, 115

IQE internal quantum efficiency 3, 5, 7, 26, 32, 35, 36, 42, 50, 59, 62, 70, 71, 77, 79, 82

ITO indium tin oxide 22–25, 50, 62, 80, 82, 103, 104, 109, 110

IV current - voltage 8, 9, 15–17, 22, 28–30, 44, 51, 98, 105, 112

J current density 30, 31, 34, 35, 40–43, 51, 63, 67, 70, 71, 75, 98–100, 106

JV current density - voltage 21, 25, 52, 62, 63, 65, 76

LAL light absorbing layer 63, 64

LED light-emitting-diode 1–3, 19, 20, 34, 70, 73, 80, 94, 97, 98, 100, 103, 105, 109, 112

LEE light extraction efficiency 2, 3, 5–7, 21, 26, 32, 34, 35, 37, 40–43, 45, 47, 48, 50, 54–62, 67, 70–72, 76–78, 81, 83, 99–101, 107, 108, 115, 116

LLO laser lift off 63–65, 67, 68, 72, 76

m-sc metal-semiconductor 9, 10, 12–14, 16, 19

MQW multiple quantum well 3, 20, 21, 29, 33, 35, 36, 50, 54, 63, 73, 75, 107, 108, 115

n-GaN n-type Gallium Nitride iv, 7, 8, 10, 12–14, 17–20, 30, 104, 110, 115, 116

NRR non-radiative recombination 2, 3, 5, 26, 39, 47, 48, 54, 61, 71, 72, 76, 78–80, 82

OPD optical power density 48

p-GaN p-type Gallium Nitride iv, 7, 10, 12, 13, 17, 19, 20, 30, 80, 82, 96, 115

p-WPE peak wall-plug efficiency 28–32, 42, 45, 49, 63, 76

p-μLED perforated microLED 50, 104

PATP PulseForge assisted transfer process 61, 63, 65, 67, 68, 71, 72, 76

PECVD plasma-enhanced chemical vapor deposition 28, 94, 96, 104, 110

PEN polyethylene naphthalate substrates iv, 62, 63, 65–73, 75–77, 79

QCSE quantum-confined Stark effect 73

ROC radius of curvature iv, 73–77

RTA rapid thermal annealing 27, 96

S2V surface-to-volume 1, 3, 26, 47, 51–53, 59, 80

SBH Schottky barrier height 10, 17, 19, 20

SEM scanning electron microscopy 68, 95, 98, 114

SRH Shockley–Read–Hall iv, 3, 26, 29, 31, 32, 34, 36, 38, 39, 47, 48, 50, 53, 54, 59, 62, 71, 76, 78, 106

SU-8 SU-8 epoxy-based negative photoresist 27–31, 36, 37, 39–42, 47–49, 51, 62, 94–97, 99–101, 104, 110

TCO transparent conductive oxide 22

TE thermionic emission 10, 12, 19

TFE thermionic field emission 12, 19

TIR total internal reflection 3, 32, 35, 42, 47, 68, 70, 81

TLM transmission line method 13, 14

WPE wall-plug efficiency iv, 5, 7, 26, 28, 30–32, 37, 41–43, 47, 48, 51, 54, 59, 61–63, 67–72, 75–79, 98, 101, 106, 112

XRC X-Ray rocking curve 64, 115

XRD X-ray diffraction 64

μLED microLED iv, x, 1–7, 21, 22, 24, 25, 27–33, 35, 36, 38–45, 47–57, 59, 61–65, 67–73, 75–83, 94, 96–98, 100, 101, 103–113, 115, 116

Chapter 1

Introduction

1.1 Background & Motivation

Emerging types of optical systems are placing growing demands on light sources that can continue operating effectively while mechanically conforming to curved or deformable surfaces. Examples include skin-mounted or implantable biomedical devices that deliver spatially localized optical stimulation, as well as flexible and curved display platforms that demand high brightness and pixel-level control under bending or strain. In these systems, light is not used solely for illumination, but as a precisely engineered signal whose intensity, spatial distribution, and stability directly impact system performance. Enabling such functionality requires emitters that maintain high efficiency and predictable electrical behavior while operating on substrates and form factors that differ fundamentally from conventional rigid platforms.

III-nitride light-emitting-diodes (LEDs), particularly InGaN-based devices, provide a strong technological foundation for these applications. Their high radiative efficiency, material robustness, and compatibility with mature semiconductor processing have enabled widespread adoption across solid-state lighting, displays, and optical communication technologies. Continued device scaling has led to the emergence of micron-scale LEDs (μ LEDs), whose small lateral dimensions support high current densities, fast modulation speeds, and dense array integration. These attributes make μ LEDs especially attractive for applications requiring spatially resolved and dynamically controlled light emission.[3, 4]

However, reducing LED dimensions to the micrometre scale introduces performance challenges that do not arise in larger devices. As the device size decreases, surface-to-volume (S2V) ratios increase, and electrical and optical behavior becomes increasingly

sensitive to electrical contact quality, surface recombination, and optical loss mechanisms. Plasma-induced damage at etched sidewalls can introduce defect states that enhance non-radiative recombination (NRR), while photon trapping and waveguiding increase the optical path length before escape, reducing light extraction efficiency (LEE). These effects can dominate device performance in small μ LEDs if not explicitly addressed, limiting both efficiency and scalability.[5–7]

In addition to these scaling challenges, many target applications impose mechanical constraints that are incompatible with the rigid substrates typically used for high-performance III-nitride devices. Sapphire and silicon substrates provide the crystalline quality and thermal stability required for efficient InGaN μ LED growth and fabrication, yet they prevent bending and conformal integration. In contrast, flexible polymer substrates offer mechanical compliance but cannot withstand the high-temperature growth and processing conditions required to achieve high material and device quality; direct fabrication on flexible substrates therefore tends to incur substantial penalties in electrical or optical performance.[8, 9]

The central motivation of this thesis is to overcome this apparent trade-off between performance and mechanical form factor by adopting a device-centric approach: establish and optimize high-performance μ LEDs under controlled conditions, then integrate them into mechanically flexible systems using transfer-based strategies. This perspective motivates the key questions addressed throughout the thesis: how performance-limiting mechanisms evolve during scaling, how they can be mitigated through processing and design, and how integration can preserve (or enhance) optimized device characteristics.

1.2 Challenges in Scaled InGaN μ LEDs for Flexible Integration

High-performance μ LEDs based on the InGaN/GaN material system rely on high-quality epitaxial growth to achieve efficient radiative recombination, which in practice requires high-temperature processing on rigid crystalline substrates such as sapphire. Flexible substrates cannot tolerate these conditions; therefore, μ LEDs for flexible applications are typically fabricated on rigid growth substrates and only later integrated into compliant platforms via transfer-based approaches.

Beyond these material constraints, μ LEDs introduce size-dependent electrical and optical effects that are negligible in broad-area LEDs. Compared to conventional devices, their small lateral dimensions enable high current densities, fast modulation, and dense array

integration for applications requiring spatially resolved emission.[3, 4] However, continued lateral scaling also invalidates common broad-area assumptions (e.g., negligible surface effects) and shifts the dominant loss mechanisms toward contacts, perimeter recombination, and extraction.

One of the most significant challenges in scaled GaN-based LEDs is optical loss arising from the large refractive index contrast between GaN and its surrounding media. A substantial fraction of photons generated in the multiple quantum well (MQW) active region undergo total internal reflection (TIR) at the GaN–air or GaN–substrate interfaces and are subsequently guided laterally or trapped within the device structure. These photons experience extended optical path lengths, increasing the probability of re-absorption at defect sites, metal contacts, or absorbing layers before escaping the device. As a result, LEE becomes a dominant limiter of overall device efficiency, particularly at small dimensions.[1, 10]

Figure 1.1 schematically illustrates representative photon propagation paths in a planar GaN-based LED on a sapphire substrate. Photons emitted from the active region may escape directly, undergo multiple internal reflections, couple into substrate-guided modes, or propagate laterally toward the device edges. These loss channels are intrinsic to planar nitride LED geometries and are largely determined by material refractive indices and device structure rather than epitaxial quality alone. As device dimensions shrink, the relative contribution of these loss mechanisms increases, making light extraction increasingly sensitive to geometry, device layout, and integration strategy.[1]

In parallel with optical losses, electrical performance in μ LEDs becomes increasingly sensitive to surface-related effects as device dimensions are reduced. The S2V ratio increases rapidly with decreasing size, amplifying the impact of plasma-induced damage and defect states introduced during mesa definition. These defects act as NRR centers, enhancing SRH recombination and degrading internal quantum efficiency (IQE). As a result, μ LEDs often exhibit reduced efficiency at smaller dimensions unless surface recombination is explicitly mitigated through careful device design and processing.[5]

These optical and electrical effects are strongly coupled and define a central challenge in scaled GaN-based μ LEDs. While lateral size reduction can, in principle, shorten photon escape paths and enable improved extraction, these potential benefits are frequently offset by increased surface recombination and substrate-guided optical losses. Consequently, achieving high efficiency requires coordinated optimization of electrical contacts, recombination processes, and optical extraction mechanisms rather than independent treatment of each factor.[6, 7]

Taken together, these constraints show that high-efficiency μ LED operation requires

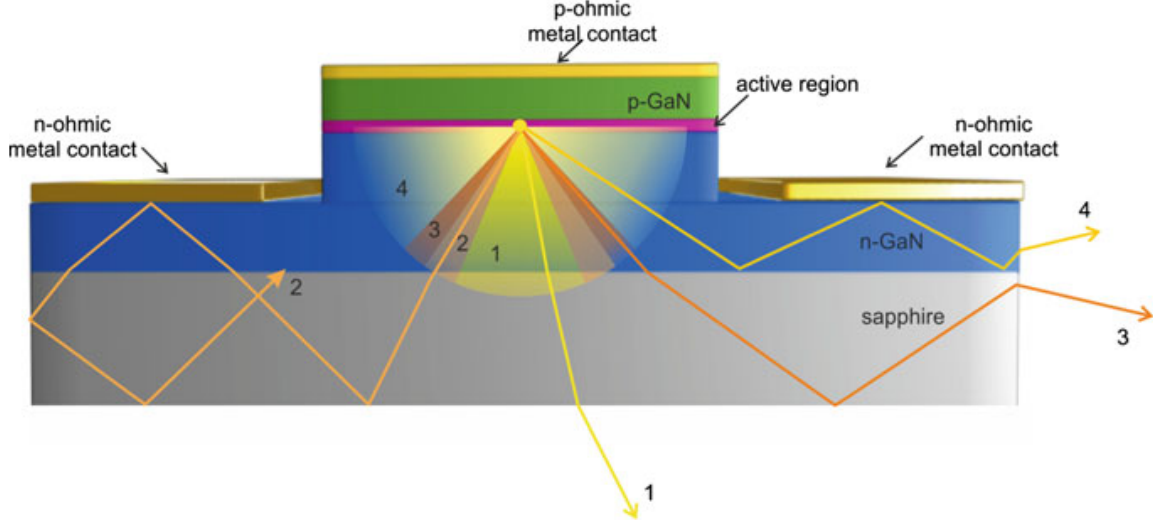


Figure 1.1: Schematic of photon propagation in a planar GaN-based LED, illustrating direct emission, total internal reflection, substrate-guided modes, and lateral waveguiding paths. Adapted from [1].

coordinated control of electrical injection, recombination losses, and optical extraction. This motivates the staged thesis strategy introduced in the next section, in which intrinsic device performance is established first and flexible integration is addressed subsequently.

1.3 Design Approach and Thesis Strategy

The preceding discussion highlights that high-performance μ LEDs are constrained by both material growth requirements and size-dependent electrical and optical loss mechanisms. To address these challenges, this thesis adopts a strategy in which performance optimization and system-level integration are treated as distinct but sequential stages. High-performance μ LEDs are first developed on rigid substrates that enable high-quality epitaxial growth and controlled processing. This provides a stable platform for systematically addressing the dominant factors limiting device efficiency before introducing mechanical flexibility through transfer-based integration.

A central premise of this thesis is that transfer-based integration is not merely a means of realizing flexible systems, but an additional stage of device optimization. Removal of

the native growth substrate exposes the GaN backside and enables optical engineering strategies that are inaccessible in conventional substrate-bound devices. Consequently, the transfer process serves a dual role: it provides the mechanical form factor required for flexible applications while creating new opportunities for performance enhancement through backside optical engineering.

Within this thesis, device performance is evaluated through the external quantum efficiency (EQE) and the WPE, which can be expressed as

$$WPE = EQE \times \eta_{elec} = IQE \times LEE \times \frac{V_p}{V_{app}} \quad (1.1)$$

where the electrical efficiency factor, $\eta_{elec} = V_p/V_{app}$, accounts for electrical losses associated with carrier injection and series resistance. Since EQE is determined by both the IQE and LEE, WPE is ultimately governed by the combined influence of electrical injection, radiative efficiency, and photon extraction. This decomposition naturally defines the optimization hierarchy adopted throughout this thesis.

This strategy consists of four primary components:

1. **Ohmic Contacts:** Establishing low-resistance, optically compatible contacts to enable efficient carrier injection and minimize electrical losses.
2. **Recombination Control:** Mitigating sidewall-induced NRR to preserve IQE during device scaling.
3. **LEE:** Optimizing device geometry and optical pathways to maximize photon extraction and EQE.
4. **Flexible Integration:** Transferring optimized devices onto compliant substrates while preserving established performance gains and enabling additional optical enhancement through transfer-enabled engineering.

Together, these stages establish a systematic framework for the realization of high-efficiency μ LEDs on flexible substrates by sequentially addressing the dominant mechanisms that limit device performance.

1.4 Scope and Organization of the Thesis

This thesis is structured according to the hierarchical design framework introduced in Section 1.3, with each stage addressing a key component of μ LED performance optimization and integration.

Chapter 2 investigates the development and optimization of ohmic contacts to GaN, establishing a reliable electrical foundation for scaled μ LED operation. Chapter 3 examines the role of sidewall passivation in mitigating surface-related non-radiative recombination and improving efficiency at small device dimensions. Chapter 4 focuses on the enhancement of LEE through geometrical design strategies, including perforated μ LED architectures that balance optical and recombination effects.

Building on these results, Chapter 5 demonstrates the integration of optimized μ LEDs onto flexible substrates using a transfer-based approach, with particular emphasis on preserving electrical and optical performance while enabling additional device-level enhancements through substrate removal and backside engineering. Together, these chapters establish a complete pathway for the realization of high-performance μ LEDs that can be systematically optimized, transferred, and integrated into flexible systems without compromising efficiency.

Chapter 2

Ohmic Contacts on GaN

GaN-based devices are widely recognized for high-power, high-frequency, and optoelectronic applications, but their performance is often limited by electrical contacts—particularly to p-GaN. Non-ideal contacts can dominate series resistance, obscure intrinsic device behavior, and limit carrier injection.

In this work, contact engineering proved to be an enabling step: early devices exhibited poor electrical characteristics that were not explained by epitaxy or other fabrication steps, and systematic optimization of both n-GaN and p-GaN contacts produced orders-of-magnitude reductions in contact resistivity and series resistance. In the WPE framework of Equation 1.1, this chapter addresses the electrical efficiency factor η_{elec} , establishing the low-loss injection baseline needed before IQE (Chapter 3) and LEE (Chapter 4) effects can be isolated.

Reliable ohmic contacts to p-GaN are especially challenging because of the low free-hole concentration and large metal–semiconductor barrier heights.[2] The problem is further constrained in transparent p-contacts, where electrical performance must be balanced against optical transmission and sputter/anneal-induced surface damage. This chapter therefore develops and validates practical ohmic contact schemes for both n-GaN and p-GaN within a shared university fabrication environment, providing the electrical foundation for the subsequent device studies.

The contact-development experiments presented in this chapter were performed on dedicated wafer runs containing circular transmission line method (c-TLM) test structures and were used to establish and optimize the contact metallization and annealing processes. The contact resistivities reported in the fabrication appendices were measured using in-line c-TLM structures fabricated on the same wafers as the corresponding μ LED devices.

Consequently, modest differences in contact resistivity and processing conditions between Chapter 2 and the appendices reflect separate fabrication runs and subsequent process refinement.

2.1 Fundamentals of Metal-GaN Contacts

2.1.1 Basic Theory of Metal-Semiconductor Contacts

When a metal is placed in contact with a semiconductor, charge transfer occurs until thermal equilibrium is reached and the Fermi levels align. This charge redistribution leads to band bending in the semiconductor near the interface and the formation of an energy barrier that governs carrier transport across the contact. Depending on the properties of this barrier, the contact may exhibit rectifying (Schottky) or non-rectifying (ohmic) behavior.

In the ideal Schottky model, the barrier height for an n-type semiconductor is given by:

$$\phi_{Bn} = (\phi_m - \chi) \quad (2.1)$$

where ϕ_m is the metal work function and χ is the semiconductor electron affinity.[11, 12] For a p-type semiconductor, the corresponding barrier height for hole injection is:

$$\phi_{Bp} = E_g - (\phi_m - \chi) \quad (2.2)$$

where E_g is the semiconductor bandgap.[11, 12]

A Schottky contact is characterized by a significant energy barrier that impedes carrier injection, resulting in nonlinear and asymmetric current - voltage (IV) characteristics. In contrast, an ohmic contact exhibits a linear IV relationship, indicating that the contact resistance is small compared to the bulk resistance of the semiconductor. Importantly, ohmic behavior does not require the complete absence of a barrier; rather, it requires that carriers can traverse the barrier efficiently under a low applied bias.

For an n-type semiconductor, it is convenient to define the semiconductor work function ϕ_n , which represents the energy difference between the vacuum level and the Fermi level of the n-type material. In GaN, ϕ_n depends on both the electron affinity χ and the position of the Fermi level relative to the conduction band, and therefore varies with doping concentration. Heavily doped n-GaN exhibits a smaller ϕ_n due to the Fermi level moving closer to the conduction band, whereas lightly doped material exhibits a larger ϕ_n .

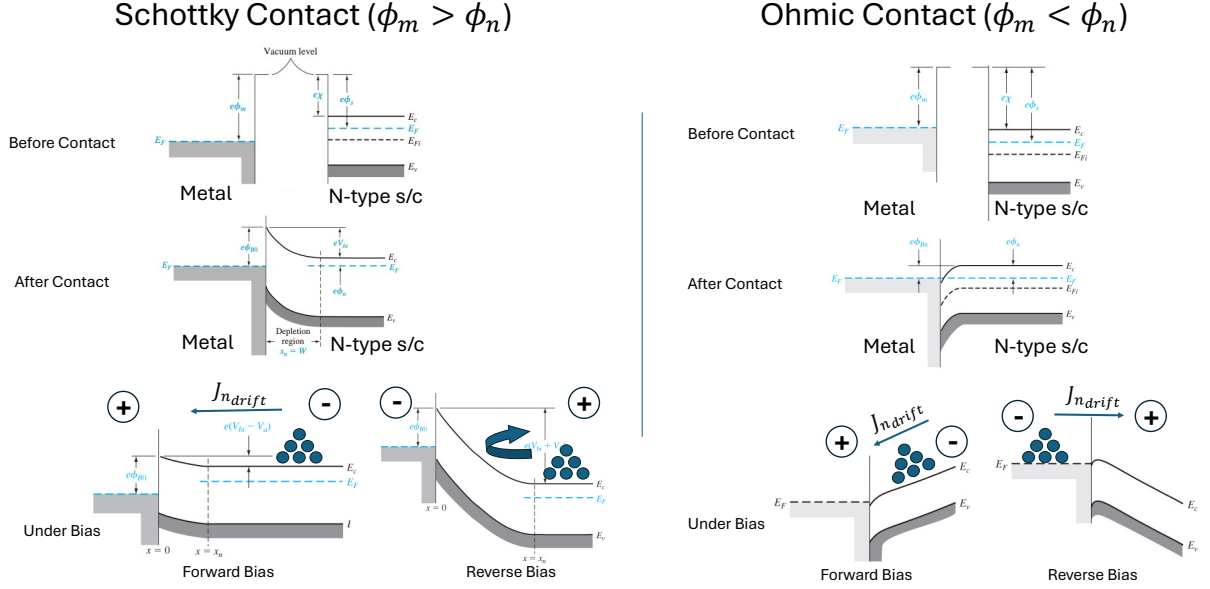


Figure 2.1: Schematic energy band diagrams illustrating Schottky and ohmic contact formation at a metal–n-GaN interface. The left set of diagrams shows the Schottky contact case, where the metal work function $\phi_m > \phi_n$, resulting in the formation of an energy barrier at the interface and rectifying IV behavior. The right set of diagrams shows the ohmic contact case, where $\phi_m < \phi_n$, leading to a reduced barrier for electron injection and efficient carrier transport. For each case, the band alignment is shown before contact, after thermal equilibrium is established, and under applied forward and reverse bias.

In the simplified picture of metal-semiconductor (m-sc) contacts, the relative magnitudes of the metal work function, ϕ_m , and ϕ_n , determine the qualitative nature of the contact. When $\phi_m > \phi_n$, electrons flow from the n-type semiconductor into the metal upon contact in order to align the Fermi levels. This charge transfer results in upward band bending in the semiconductor and the formation of an energy barrier at the m-sc interface, leading to Schottky contact behavior characterized by rectifying IV characteristics.

In contrast, when $\phi_m < \phi_n$, electrons are transferred from the metal into the semiconductor, reducing the effective barrier height for electron injection from the semiconductor into the metal. In this case, carrier transport across the interface is not strongly impeded, and the contact exhibits ohmic behavior with a linear IV relationship.

These two limiting cases are illustrated schematically in Figure 2.1, which shows the energy band alignment before contact, after thermal equilibrium is established, and under applied forward and reverse bias for metal-n-GaN interfaces. While this work-function-based model provides useful physical intuition, real metal-GaN contacts may deviate from ideal behavior due to interface states and processing-induced effects.[13] Nevertheless, the framework presented in Figure 2.1 serves as a useful starting point for understanding contact formation and motivates the experimental strategies employed in this work.

Carrier transport across a Schottky barrier is commonly described by thermionic emission (TE) theory, for which the current density is given by:

$$J = A^* T^2 e^{-\frac{q\phi_B}{kT}} \cdot \left[e^{\frac{qV}{kT}} - 1 \right] \quad (2.3)$$

where A^* is the effective Richardson constant, T is the temperature in Kelvin, and ϕ_B is the barrier height.[11] This mechanism dominates when the depletion region at the interface is sufficiently wide such that carrier tunneling is negligible.

2.1.2 GaN-Specific Considerations for Ohmic Contacts

GaN is a wide bandgap semiconductor with a bandgap of approximately $E_g \approx 3.4$ eV and an electron affinity of $\chi \approx 4.1$ eV, as illustrated schematically in Figure 2.2(a). While these properties are advantageous for high-power and optoelectronic applications, they introduce fundamental challenges for the formation of low-resistance ohmic contacts. In particular, the large bandgap leads to substantial energy barriers at metal-GaN interfaces, and many metal contacts exhibit rectifying behavior in their as-deposited state.

Figure 2.2(b), adapted from Greco *et al.*, summarizes reported Schottky barrier heights (SBHs) as a function of metal work function for both n-GaN and p-GaN.[2] Although these data are compiled from multiple literature sources and are not strictly controlled for doping concentration or growth conditions, they clearly illustrate a key asymmetry: for most practical metals, the effective SBH on n-GaN are significantly lower than those on p-GaN. This asymmetry reflects the fundamental difficulty of forming low-barrier contacts to p-type wide-bandgap semiconductors and foreshadows the markedly different contact strategies required for n-GaN and p-GaN.

In practice, ohmic contact formation to GaN relies on enabling efficient carrier transport across the m-sc interface through tunneling rather than purely TE. The width of the

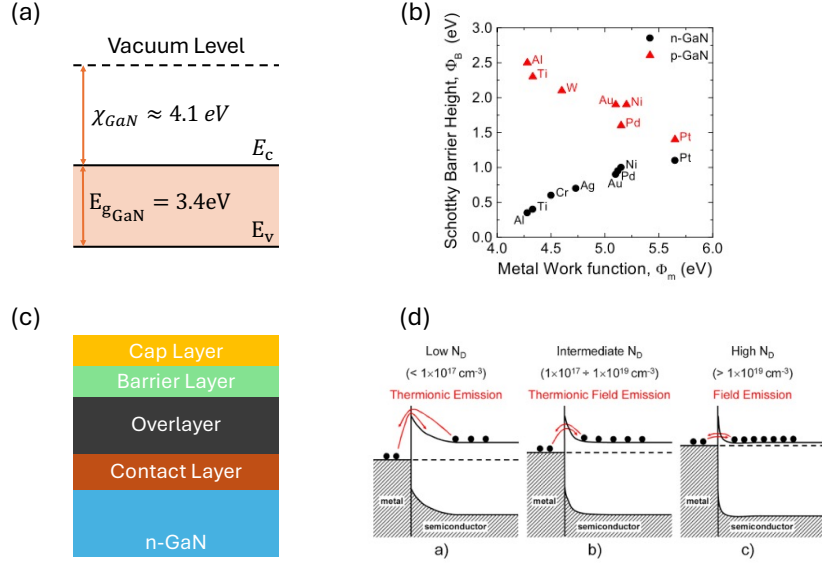


Figure 2.2: GaN-specific considerations relevant to ohmic contact formation. (a) Schematic band diagram of GaN illustrating the wide bandgap ($E_g \approx 3.4$ eV) and electron affinity ($\chi \approx 4.1$ eV), which contribute to large energy barriers at metal–GaN interfaces. (b) Reported SBH as a function of metal work function for n-GaN and p-GaN, adapted from Greco *et al.*, illustrating the generally lower effective barriers achievable on n-GaN compared to p-GaN.[2] (c) Schematic multilayer metal stack commonly employed for n-GaN ohmic contacts, consisting of a low-work-function contact layer, an overlayer promoting intermetallic formation, a high-melting-point diffusion barrier, and a protective cap layer. (d) Schematic illustration of the evolution of carrier transport mechanisms at the m-sc interface with increasing near-interface doping concentration, showing the transition from TE to TFE; adapted from Greco *et al.*.[2]

depletion region at the interface is therefore a critical parameter and is given by

$$W = \sqrt{\frac{2\varepsilon_s(\phi_B - V)}{qN}}, \quad (2.4)$$

where ε_s is the semiconductor permittivity, ϕ_B is the effective barrier height, V is the applied bias, and N is the doping concentration. Increasing the carrier concentration near the interface reduces the depletion width, thereby enhancing tunneling probability and promoting ohmic behavior.

For n-GaN, relatively high electron concentrations and low donor activation energies enable tunneling-dominated transport to be achieved using appropriate metal stacks and post-deposition annealing. A common strategy employs multilayer metal contacts, as shown schematically in Figure 2.2(c). In this architecture, the contact layer is chosen to provide a low work function and intimate electrical coupling to GaN, while an overlayer (commonly Al) promotes the formation of low work function intermetallic compounds. A high-melting-point barrier layer suppresses excessive interdiffusion during annealing, and a cap layer, typically Au, protects the stack from oxidation. Annealing plays a central role by inducing interfacial reactions, metal diffusion, and the formation of nitrogen vacancies, which act as donors in GaN.[2] These effects locally increase the effective carrier concentration near the interface and can transform an initially Schottky contact into an ohmic contact.

The evolution of carrier transport with increasing near-interface doping is illustrated schematically in Figure 2.2(d). At low doping concentrations, transport is dominated by TE over a wide barrier. As the depletion width narrows with increasing doping, thermionic field emission (TFE) becomes significant, and in the heavily doped limit, direct field emission (FE) dominates. In this regime, current transport is governed primarily by tunneling through a thin barrier rather than by the absolute barrier height.

In contrast, ohmic contacts to p-GaN remain significantly more challenging. The high activation energy of Mg acceptors results in low free-hole concentrations at room temperature, leading to wide depletion regions and reduced tunneling probability.[2] As a result, p-type GaN contacts typically exhibit higher specific contact resistivities and a strong dependence on contact material, annealing conditions, and contact geometry. Consequently, p-type contacts often dominate the overall series resistance in GaN-based devices, particularly in structures requiring lateral current spreading over small dimensions.

These challenges are further exacerbated in applications requiring optically transparent p-type contacts. In such cases, electrically favorable metal contacts must be replaced or combined with transparent conductive materials, introducing additional trade-offs between contact resistivity, optical transmission, and process-induced surface damage. These considerations motivate the separate treatment of n-GaN contacts, opaque p-GaN contacts, and transparent p-GaN contacts in the following sections.

2.1.3 Contact Resistivity and Measurement Concepts

The electrical quality of a m-sc contact is commonly quantified using the *specific contact resistivity*, ρ_c [Ωcm^2], which characterizes the resistance associated with carrier transport

across the m-sc interface, normalized by the contact area. Formally, ρ_c is defined as

$$\rho_c = \left(\frac{\partial J}{\partial V} \right)^{-1}_{V \rightarrow 0} \quad (2.5)$$

where J is the current density flowing across the interface. Low values of ρ_c are essential for minimizing voltage drops at the contacts and reducing the overall series resistance of GaN-based devices.

It is important to distinguish contact resistivity from other resistive contributions within a device. While ρ_c describes an interfacial property of the m-sc junction, the total series resistance also depends on the sheet resistance of the semiconductor layers and the lateral current spreading away from the contacts. In GaN-based devices, particularly those incorporating p-GaN, limited hole concentration and mobility can result in significant lateral voltage drops, causing the effective series resistance to be strongly influenced by contact geometry even when the intrinsic contact resistivity remains unchanged.[3] These effects are especially relevant for device structures employing thin n-GaN or p-GaN layers and for optoelectronic devices based on InGaN active regions, where efficient current injection and uniform current spreading are critical for device performance. As a result, accurate evaluation of contact properties requires measurement techniques that decouple interfacial resistance from bulk and sheet resistances within the semiconductor.

Transmission line method (TLM) structures are widely used for this purpose, as they enable the separate extraction of contact resistivity and semiconductor sheet resistance from electrical measurements. Among these techniques, the c-TLM offers advantages in terms of radial symmetry and reduced sensitivity to edge effects compared to conventional linear TLM structures. In this work, contact resistivity values for both n-GaN and p-GaN are extracted using c-TLM test structures, as described in detail in the following section.

2.1.4 Contact Resistivity Measurement Using the Circular Transmission Line Method

Accurate extraction of ohmic contact resistivity requires measurement techniques that decouple the intrinsic resistance of the m-sc interface from parasitic contributions such as semiconductor sheet resistance and probe contact resistance. Simple two-terminal measurements are insufficient for this purpose, as the measured resistance includes uncontrolled series elements that can be comparable to, or larger than, the intrinsic contact resistance being measured. This limitation is particularly severe for low specific contact resistivity (ρ_c) contacts.

TLMs is therefore widely employed for quantitative contact characterization. Among these, the c-TLM is especially well suited for planar GaN structures, as it avoids mesa isolation, minimizes edge effects, and provides a well-defined radial current flow geometry. A rigorous derivation of the c-TLM formalism is given by Schroder in *Semiconductor Material and Device Characterization*, and the same framework is adopted in this work.[14]

In the c-TLM configuration, metal is deposited on the semiconductor surface in a concentric ring geometry. An inner circular contact of radius r_1 is surrounded by an outer annular contact with an inner radius r_2 , leaving an exposed semiconductor gap of width

$$d = r_2 - r_1 \quad (2.6)$$

A top-down schematic of the c-TLM test structures used in this work is shown in Figure 2.3(a). The metal contacts are indicated in gray, while the exposed semiconductor region is shown in blue. A series of nominally identical c-TLM structures is fabricated with progressively increasing gap spacing d , corresponding to increasing outer radii r_2 , while the inner radius r_1 is held constant. The leftmost structure in Figure 2.3(a) has the smallest gap, and the gap increases toward the rightmost structure. The use of multiple c-TLM structures with systematically varied d enables the separation of the resistance associated with lateral current flow in the semiconductor from the resistance associated with vertical current injection across the m-sc interface. By parameterizing the total measured resistance as a function of a known geometric variable, the specific contact resistivity ρ_c can be extracted independently of the semiconductor sheet resistance.

In principle, the resistance between the inner and outer contacts of a c-TLM structure may be measured using a two-probe configuration. However, in this case, the measured resistance includes the contact resistance between the probe tips and the metal pads. This probe-to-metal contact resistance can be comparable to, or larger than, the intrinsic contact resistance being measured, particularly for low- ρ_c ohmic contacts, leading to significant measurement error. To eliminate this parasitic contribution, a four-point probe (Kelvin) configuration is employed. In this approach, separate probe tips are used to source current through the c-TLM contacts and to sense the voltage drop between them, ensuring that the measured voltage excludes probe contact resistance. The four-point probe configuration used in this work is illustrated schematically in Figure 2.3(a). In practice, this measurement was implemented using a Keithley 2400 source-measurement unit operated in four-wire mode in conjunction with a probe station equipped with four independent probes.

A cross-sectional schematic of a c-TLM structure fabricated on n-GaN is shown in Figure 2.3(b), with red arrows indicating the radial current flow under the applied bias. Owing to the circular symmetry of the structure, current spreads radially in the semiconductor

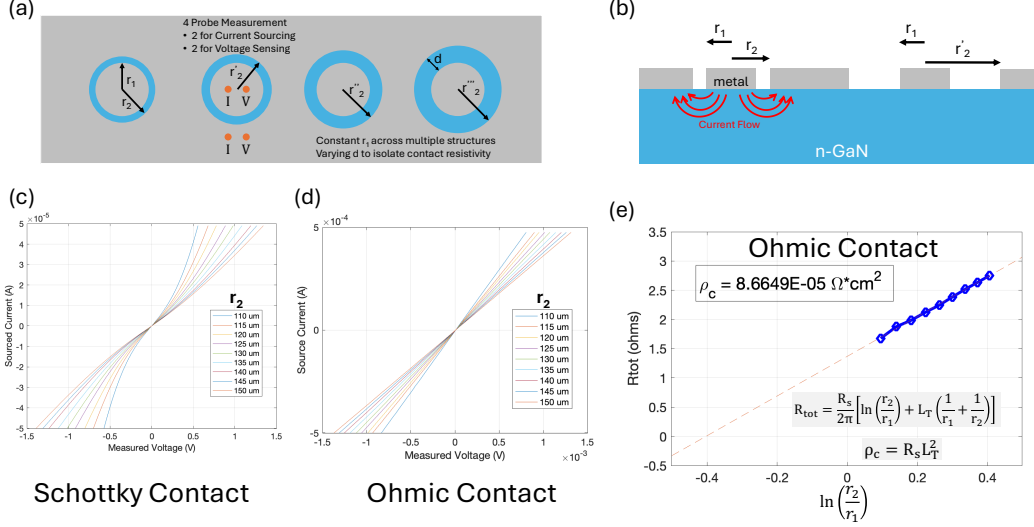


Figure 2.3: (a) Top-down schematic of the c-TLM test structures and four-point measurement configuration. Concentric metal contacts (grey) with inner radius r_1 and outer radius r_2 are patterned on the semiconductor (blue), defining a gap $d = r_2 - r_1$. Structures with increasing r_2 are used to decouple lateral sheet resistance from the m-sc interface resistance. (b) Cross-sectional schematic of a c-TLM structure illustrating current flow beneath the metal contacts within the n-GaN layer. (c) Representative experimental I-V curves measured from multiple c-TLM structures with varying r_2 (or equivalently, varying d), exhibiting nonlinear behavior characteristic of a Schottky contact. (d) Representative linear I-V characteristics indicative of an ohmic contact. (e) Extracted total resistance R_{tot} plotted versus $\ln(r_2/r_1)$ for an ohmic contact. The linear dependence validates the c-TLM model and enables extraction of the sheet resistance, transfer length L_T , and specific contact resistivity ρ_c .

and transfers vertically into the metal contacts over a characteristic length scale defined by the transfer length. For each c-TLM structure, IV measurements are first performed using the four-point probe configuration described previously. Current is sourced through the outer probes while the voltage drop between the inner probes is sensed in four-wire mode, thereby eliminating probe-to-metal contact resistance from the measurement.

An IV sweep is performed over a symmetric current range, and the resistance at each bias point is calculated using Ohm's law,

$$R = \frac{V}{I} \quad (2.7)$$

The resistance values extracted from all points along the IV sweep are then averaged to obtain the total measured resistance R_{tot} for that specific c-TLM geometry, defined by the radii r_1 and r_2 .

For an ideal ohmic contact, the IV characteristic is linear, and the resistance values extracted from individual bias points exhibit a very small standard deviation (Figure 2.3(d)). In contrast, non-ohmic or Schottky-like contacts produce nonlinear IV characteristics (Figure 2.3(c)), resulting in a larger spread in the extracted resistance values. The standard deviation of the resistance across the IV sweep therefore serves as a useful diagnostic for assessing contact linearity, although the average value is used for subsequent analysis.

This procedure is repeated for a series of c-TLM structures with increasing gap spacing $d = r_2 - r_1$, yielding a set of total resistances R_{tot} corresponding to different contact geometries. Once this experimental dataset is obtained, an analytical model is required to relate the measured resistances to the intrinsic m-sc contact properties. The total resistance R_{tot} measured between the inner and outer contacts of a c-TLM structure can be obtained by solving the two-dimensional current continuity equation in cylindrical coordinates. This analysis, described in detail by Schroder, accounts for radial current spreading in the semiconductor and vertical current injection at the m-sc interface.[14] The resulting expression involves modified Bessel functions and is given by

$$R_{\text{tot}} = \frac{R_{\text{sh}}}{2\pi} \left[\ln\left(\frac{r_2}{r_1}\right) + \frac{L_T}{r_1} \frac{I_0\left(\frac{r_1}{L_T}\right)}{I_1\left(\frac{r_1}{L_T}\right)} + \frac{L_T}{r_2} \frac{K_0\left(\frac{r_2}{L_T}\right)}{K_1\left(\frac{r_2}{L_T}\right)} \right] \quad (2.8)$$

where R_{sh} is the semiconductor sheet resistance, I_n and K_n are the modified Bessel functions of the first and second kind, respectively, and L_T is the transfer length. The transfer length can be thought of as the distance over which most of the current transfers from the semiconductor into the metal or from the metal into the semiconductor.

The specific contact resistivity ρ_c is related to the transfer length through

$$\rho_c = R_{\text{sh}} L_T^2 \quad (2.9)$$

When both contact radii satisfy

$$r_1 \gg L_T \quad \text{and} \quad r_2 \gg L_T \quad (2.10)$$

the ratios of modified Bessel functions in Eq. (2.8) approach unity. Under this condition, the total resistance simplifies to

$$R_{\text{tot}} = \frac{R_{\text{sh}}}{2\pi} \left[\ln\left(\frac{r_2}{r_1}\right) + L_T \left(\frac{1}{r_1} + \frac{1}{r_2} \right) \right] \quad (2.11)$$

In this limit, plotting R_{tot} as a function of $\ln(r_2/r_1)$ yields a linear relationship, as shown in Figure 2.3(e). The slope of this plot is proportional to the semiconductor sheet resistance, while the y-intercept provides direct access to the transfer length and, through Eq. (2.9), the specific contact resistivity. All c-TLM test structures used in this work were designed such that r_1 and r_2 were significantly larger than the extracted transfer lengths, validating the use of the simplified expression in Eq. (2.11).

2.2 Ohmic Contacts to n-GaN

Ohmic contacts to n-GaN were investigated first to establish a reliable contact process and to validate the contact resistivity extraction methodology described in Section 2.1.3 and Section 2.1.4. Compared to p-GaN, n-type GaN benefits from higher achievable doping concentrations and lower effective SBHs for several low-work-function metals, making it a suitable baseline system for contact engineering studies.

Cr-based metallization schemes were selected for this study due to their reported ability to form thermally stable ohmic contacts to n-GaN at relatively moderate annealing temperatures. As reviewed comprehensively by Greco *et al.* [2], annealed contacts to n-GaN generally rely on thermally activated interface reactions that reduce the effective barrier width and promote tunneling-dominated transport. While Ti-based systems remain the most widely studied, Greco *et al.* also report that Cr-based contacts can achieve comparable specific contact resistivities at lower annealing temperatures.

In this work, identical n-GaN epitaxial material was used for all samples. Consequently, differences in electrical behavior can be attributed directly to contact metallization and annealing. In Figure 2.4(a), red traces correspond to as-deposited contacts, while blue traces correspond to annealed contacts. The different marker styles denote the gap spacing d between adjacent electrodes in the c-TLM structures. Notably, both the as-deposited and annealed contacts exhibit linear and symmetric IV characteristics over the measured bias range, indicating ohmic behavior in both cases. However, despite this apparent ohmicity, a clear difference in electrical resistance is observed between the two conditions, with annealed contacts exhibiting substantially lower resistance across all c-TLM geometries.

Figure 2.4(b) shows the total resistance extracted from each c-TLM structure plotted as a function of $\ln(r_2/r_1)$. This representation enables the extraction of the contact parameters using the simplified c-TLM expression given by Eq. 2.11. Linear fits to the data yield the sheet resistance R_{sh} and transfer length L_T , which are subsequently used to calculate the specific contact resistivity according to Eq. 2.9. The annealed contacts show a well-defined

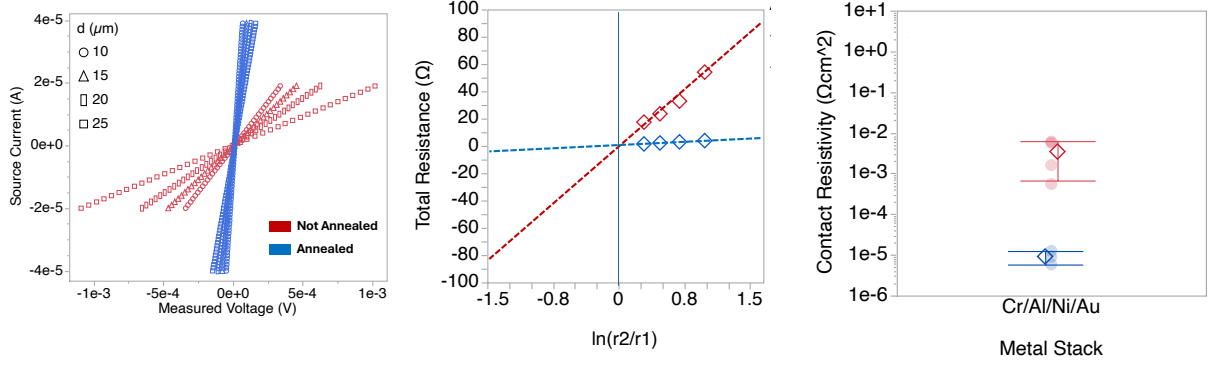


Figure 2.4: Experimental c-TLM results for Cr/Al/Ni/Au (5/100/30/100 nm) ohmic contacts to n-GaN before annealing (red) and after annealing (blue). (a) Measured IV characteristics for multiple c-TLM structures with different gap spacings d , corresponding to $d = 10 \mu\text{m}$ (circles), $15 \mu\text{m}$ (triangles), $20 \mu\text{m}$ (rectangles), and $25 \mu\text{m}$ (squares). Annealed contacts exhibit significantly lower resistance, evidenced by the increased slope of the IV curves. (b) Extracted total resistance R_{tot} as a function of $\ln(r_2/r_1)$ calculated from the data in (a). The dashed red line indicates the linear extrapolation used for parameter extraction. (c) Specific contact resistivity ρ_c for annealed and non-annealed contacts. Semi-transparent solid symbols represent individual extracted values, the hollow triangle denotes the mean value, and error bars indicate the standard deviation ($N = 4$ for non-annealed and $N = 3$ for annealed).

linear dependence with a reduced slope and intercept, consistent with lower contact and access resistance. In contrast, while the as-deposited contacts also exhibit approximately linear behavior, their significantly larger slope reflects a higher effective contact resistivity.

The extracted specific contact resistivities are summarized in Figure 2.4(c), which shows the mean ρ_c obtained from multiple independent sets of c-TLM structures. For the as-deposited Cr/Al/Ni/Au contacts, a mean specific contact resistivity of approximately $3 \times 10^{-3} \Omega \cdot \text{cm}^2$ is obtained ($N = 4$). Following annealing at 550°C for 5 min in an N_2/O_2 ambient, the mean ρ_c is reduced by nearly three orders of magnitude to approximately $9 \times 10^{-6} \Omega \cdot \text{cm}^2$ ($N = 3$). In addition to the reduction in mean contact resistivity, the annealed samples exhibit a substantially narrower distribution, as reflected by the reduced standard deviation, indicating improved process uniformity and reduced spatial variability across the wafer.

The improvement in contact performance upon annealing is consistent with previously reported behavior of Cr-based contacts to n-GaN. Prior studies have shown that thermal

annealing promotes the formation of an interfacial CrN layer at the m-sc interface. [15] The formation of CrN is accompanied by the generation of nitrogen vacancies in the near-surface region of the GaN, which act as shallow donors and locally increase the electron concentration. This results in a narrowing of the depletion region and facilitates tunneling-dominated transport across the interface, thereby reducing the effective contact resistivity. Together, these results demonstrate that effective and reproducible ohmic contacts to n-GaN can be achieved through contact engineering and annealing alone, providing a robust electrical foundation for the realization of high-performance GaN-based electronic and optoelectronic devices.

2.3 Ohmic Contacts to p-GaN: Opaque Contacts

While achieving low-resistance ohmic contacts to n-GaN is relatively well understood and technologically mature, the formation of comparable contacts to p-GaN remains one of the most persistent challenges in GaN-based optoelectronics.

Ohmic contacts to p-GaN are fundamentally limited by both material and device physics considerations. In typical GaN epitaxial structures, p-type conductivity is achieved through Mg acceptor doping with concentrations on the order of $N_A > 1 \times 10^{19} \text{ cm}^{-3}$. However, the Mg acceptor activation energy in GaN is relatively large ($E_A > 120 \text{ meV}$), resulting in a free hole concentration that is only a small fraction of the incorporated acceptor density at room temperature.[2, 16] In contrast, common n-type dopants such as Si or Ge exhibit much lower ionization energies, enabling free electron concentrations exceeding 10^{19} cm^{-3} . [2, 16] This asymmetry in dopant activation places an inherent constraint on the achievable contact resistivity for p-GaN.

From a m-sc junction perspective, the wide bandgap of GaN and the limited availability of metals with sufficiently high work functions lead to intrinsically large SBHs for hole injection into p-GaN. As summarized in Figure 2.2(b), Pd exhibits one of the lowest reported SBHs to p-GaN, motivating its selection as the contact layer in this work.[2] Nevertheless, even with optimized high-work-function metals, the combination of large SBHs and low free hole concentration restricts current transport primarily to the TE or TFE regimes, rather than pure FE, as illustrated schematically in Figure 2.2(d). According to Eq. 2.3, which describes TE across a Schottky barrier, the current density exhibits a strong temperature dependence. Consequently, during LED operation, self-heating can lead to changes in the effective contact resistivity, introducing additional variability into device performance.

The p-contact metallization employed in this work is based on a Pd/Ni/Au stack, which is structurally similar, though not identical, to the n-contact described in the previous

sections (Figure 2.2(c)). In this configuration, Pd serves as the primary contact layer to p-GaN, Ni acts as both a diffusion barrier and an adhesion layer, and Au functions as a low-resistance capping layer to ensure mechanical stability and compatibility with subsequent processing steps.

To experimentally verify that Pd/Ni/Au forms an ohmic contact to p-GaN, a c-TLM was employed. Unlike the case for n-GaN, c-TLM measurements on p-GaN present additional complications when performed directly on LED epitaxial wafers. Since the epitaxial structures used in this work were purchased rather than custom-grown, dedicated p-GaN reference layers were not available. As a result, c-TLM structures were fabricated directly on full LED stacks. When testing p-GaN c-TLM structures at voltages exceeding the LEDs turn-on voltage ($V_{\text{on}} \approx 2.7 \text{ V}$ for blue LEDs), carriers can leak into the MQWs, leading to photon emission. This parasitic injection alters the measured current distribution and effectively skews the extracted sheet resistance of the p-GaN layer. To mitigate this effect, a strict voltage compliance was enforced during c-TLM measurements, ensuring operation at or below V_{on} .

Figure 2.5(a) shows the measured total resistance R_{tot} as a function of $\ln(r_2/r_1)$ for Pd/Ni/Au (30/10/200 nm) contacts deposited on p-GaN under both as-deposited and annealed conditions. The annealing parameters were identical to those used for the n-ohmic contacts described in the previous section. As expected, the extracted ρ_c is substantially higher than that obtained for n-GaN, reflecting the combined effects of the large SBH and low free hole concentration.

For the as-deposited contacts, a mean ρ_c of approximately $6 \times 10^{-3} \Omega \cdot \text{cm}^2$ was extracted ($N = 5$), which falls within the range commonly reported for ohmic contacts to p-GaN.[2] After annealing, a modest reduction in the mean contact resistivity to $\sim 4 \times 10^{-3} \Omega \cdot \text{cm}^2$ was observed ($N = 4$). However, this change is not statistically significant, and the contact resistivity can be considered effectively unchanged by the annealing step.

In principle, thermal annealing of Pd-based contacts is expected to improve ohmic behavior through mechanisms such as Pd-Ga alloying and an associated increase in the near-surface hole concentration.[17] Detailed micro-structural studies have shown that Pd can react with GaN to form PdGa phases, potentially lowering the effective SBH and enhancing carrier transport across the interface. However, the effectiveness of this process is highly sensitive to the annealing ambient, temperature, time, and the relative thicknesses and deposition conditions of the Pd, Ni, and Au layers. The limited improvement observed here suggests that further optimization of these parameters is required to fully exploit the benefits of Pd-based contacts. Nonetheless, a contact resistivity on the order of $4 \times 10^{-3} \Omega \cdot \text{cm}^2$ is generally regarded as adequate for functional device operation, particularly when

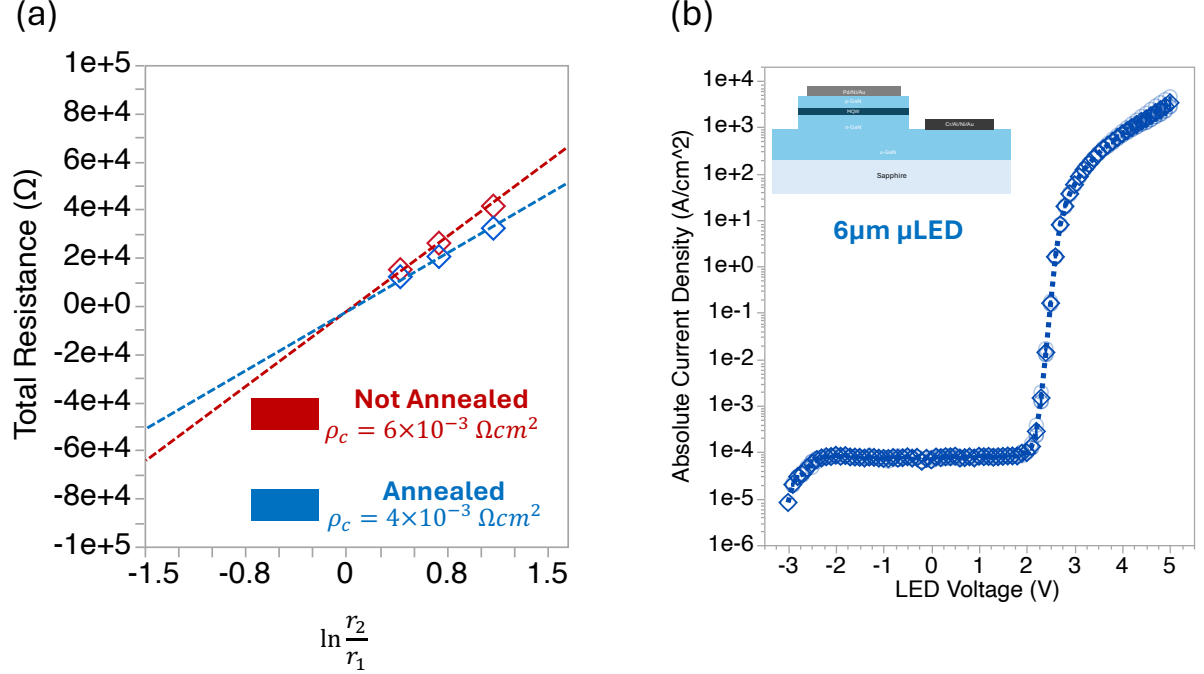


Figure 2.5: Experimental results for Pd/Ni/Au (30/10/200 nm) contacts to p-GaN. (a) Extracted total resistance R_{tot} plotted versus $\ln(r_2/r_1)$ from c-TLM measurements before annealing (red) and after annealing (blue), illustrating comparable linear behavior with modest improvement after annealing. (b) JV characteristics of a $6 \mu\text{m}$ μLED measured over a -3 to 5 V sweep. Hollow semi-transparent circles denote individual data points, while triangles indicate the mean response of two devices. The inset shows a cross-sectional schematic of the μLED structure, highlighting the p-GaN and n-GaN ohmic contacts.

combined with a low-resistance n-contact.

To assess device-level impact, Figure 2.5(b) shows the current density - voltage (JV) characteristics of a $6 \mu\text{m}$ diameter μLED fabricated without passivation using the n- and p-contacts developed here. Series resistance does not dominate until beyond turn-on ($V > 2.7$ V), and current densities approaching 1 kA/cm^2 are achieved below 5 V, indicating that the Pd/Ni/Au scheme provides a functional electrical baseline for subsequent studies.

The key limitation of Pd/Ni/Au is optical: the stack is opaque, and because the p-contact sits directly above the MQWs, absorption in the metal can significantly reduce LEE. The next subsection therefore develops transparent p-type contacts that preserve ohmic behavior while improving optical transmission.

2.4 Ohmic Contacts to p-GaN: Transparent Contacts

For high-performance optoelectronic devices such as μ LEDs, the p-side contact must provide both low electrical loss and high optical transmission at the emission wavelength. The previous section established that ohmic contacts to p-GaN can be achieved reproducibly using Pd-based metal stacks; however, these contacts are optically opaque and can therefore impose a substantial penalty on light extraction, particularly in small-area devices where the p-contact footprint occupies a significant fraction of the emitting area. This section develops a transparent p-contact scheme that targets contact resistivities comparable to the opaque baseline while maintaining high transmittance in the blue spectral range.

A widely used transparent p-contact material is indium tin oxide (ITO), a transparent conductive oxide (TCO) that can simultaneously support current spreading and high optical transmission.[2, 18, 19] Nevertheless, achieving ohmic behavior between sputtered ITO and p-GaN is not straightforward. As-deposited ITO typically forms a Schottky-like junction with p-GaN due to unfavorable band alignment, and contact improvement depends sensitively on interfacial chemistry, near-surface hole concentration, and sputter-induced surface damage. Post-deposition annealing is often required and is believed to promote interfacial modification through out-diffusion and intermixing processes that can locally enhance the effective hole concentration near the surface.[18, 19] In practice, industrially optimized ITO/p-GaN processes frequently rely on proprietary details, motivating an in-house optimization effort using the available sputtering infrastructure.

An initial baseline process was established using room-temperature RF sputter deposition (150 W RF power, 27 sccm Ar flow, 3 mTorr chamber pressure), followed by annealing at 550 °C in an O_2/N_2 ambient for 3 min to improve ITO conductivity and optical transparency. Figure 2.6(a) shows the measured IV response of a representative c-TLM structure with $d = 10 \mu\text{m}$ for multiple ITO stacks. The baseline condition (ITO Type 1, purple) exhibits strongly Schottky behavior, indicating that the annealing of the baseline film is insufficient to overcome the effective barrier at the ITO/p-GaN interface.

Sputtering-induced damage can introduce compensating defects and disorder at the p-GaN surface, directly counteracting any anneal-driven improvement in near-surface hole concentration and transport. A common industrial mitigation strategy is facing target sputtering, in which two targets face each other and the substrate is positioned outside the high-density plasma region. This geometry spatially confines the plasma between the targets and suppresses the flux of high-energy ions, fast neutrals, and secondary electrons to the substrate, reducing deposition damage.[18–20] Because facing target sputtering hardware was not available in the present work, two low-damage strategies compatible with the existing sputtering tool were evaluated.

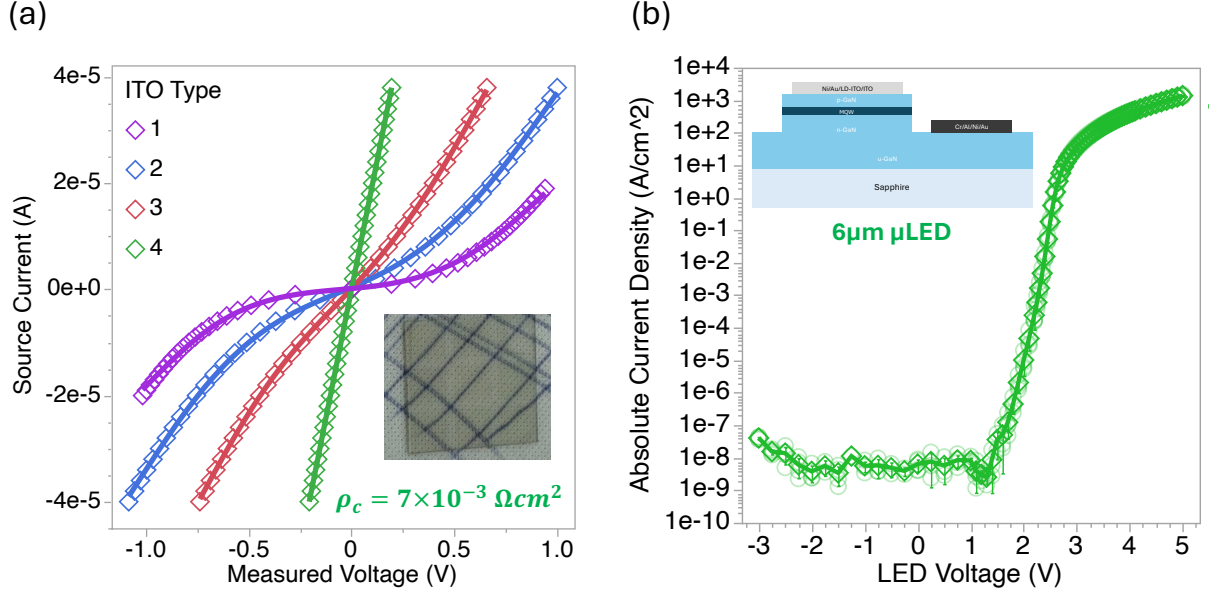


Figure 2.6: Experimental characterization of transparent ITO p-contacts on p-GaN. (a) IV characteristics of c-TLM structures with a fixed gap spacing of $d = 10 \mu\text{m}$ for different ITO contact stacks. ITO Type 1 (purple) corresponds to the baseline ITO process. ITO Type 2 (blue) consists of a bilayer ITO stack with a $\sim 10 \text{ nm}$ low-power (low-damage) ITO layer followed by $\sim 70 \text{ nm}$ of standard ITO. ITO Type 3 (red) is identical to Type 2, except that the initial low-power ITO layer is deposited at elevated chamber pressure. ITO Type 4 (green) is a quadlayer stack comprising an ultra-thin Ni/Au interlayer, a low-damage ITO layer, and a standard ITO overlayer. Inset: optical micrograph of patterned ITO Type 4 contacts on a sapphire-based LED epitaxial wafer, illustrating high optical transparency. (b) JV characteristics of $6 \mu\text{m}$ μLED fabricated using the optimized transparent p-contact (ITO Type 4). Hollow semi-transparent circles represent individual data points, hollow triangles denote the mean value across $N = 4$ devices, and the solid line is provided as a visual guide and does not represent a fit. Error bars indicate the standard deviation. Inset: cross-sectional schematic of the μLED structure highlighting the optimized p-contact (ITO Type 4) and n-contact.

First, a thin “protective” ITO interlayer ($\sim 10 \text{ nm}$) was deposited at reduced RF power (50 W) prior to depositing the remainder of the ITO using the baseline conditions. This structure (ITO Type 2, blue) yields a modest improvement relative to Type 1 but remains Schottky-like, indicating that power reduction alone does not sufficiently mitigate

the interfacial limitations. The minimum stable RF power of the tool constrained further reduction.

Second, the chamber pressure was increased during the low-power interlayer deposition to reduce the mean free path of sputtered species and decrease kinetic energy before their arrival at the substrate. Plasma diagnostics studies show that increasing pressure suppresses high-energy components of ion energy distributions and yields narrower, lower-energy incident fluxes at the substrate.[21] Guided by this principle, the pressure during the initial ~ 10 nm interlayer deposition was increased from 3 mTorr to 15 mTorr while maintaining 50 W of power. This configuration (ITO Type 3, red) further reduces the apparent resistance compared to Types 1–2 but still exhibits non-linearity in Figure 2.6(a), demonstrating that an additional mechanism is required to achieve robust ohmic behavior.

To lower the effective barrier at the p-GaN interface while maintaining transparency, an ultra-thin metallic interlayer was introduced prior to ITO deposition. A Ni/Au bilayer (20/15 Å) was deposited by e-beam evaporation at 0.1 Å/s for each metal. Ni/Au is a well-established p-GaN contact system; however, at these thicknesses, the film is not intended to provide lateral conduction and is expected to be electrically non-robust and highly resistive.[2] Instead, the purpose of the interlayer is to enable favorable interfacial modification at the p-GaN surface while preserving optical transmission. The thin Au cap additionally reduces the likelihood of oxidation during transfer from evaporation to sputtering.

Following the Ni/Au deposition, a low-damage ITO interlayer (~ 10 nm, 50 W, 15 mTorr) was deposited, followed by ~ 70 nm of ITO using the baseline condition, yielding a total thickness of ~ 80 nm. This stack (ITO Type 4, green) exhibits clearly ohmic behavior in Figure 2.6(a) with a substantially reduced resistance relative to Types 1–3. Using $N = 4$ independent c-TLM data sets, the extracted contact resistivity is $\rho_c = 7 \times 10^{-3} \Omega \cdot \text{cm}^2$, comparable in order of magnitude to the Pd-based opaque p-contacts established in the previous section. The inset optical micrograph in Figure 2.6(a) further confirms the high visual transparency of patterned ITO Type 4. UV-vis measurements show $> 88\%$ transmittance over 390–500 nm, spanning the emission range of the blue μLEDs studied here.

Figure 2.6(b) validates the Type 4 stack at the device level: 6 μm μLEDs exhibit a turn-on near 2.7 V, and series resistance does not dominate immediately beyond turn-on. Current densities approaching 1 kA/cm^2 are achieved below 5 V, indicating that introducing transparency at the p-contact does not impose a prohibitive electrical penalty. Together with the measured $> 88\%$ transmittance, these results show that Type 4 provides a practical balance between electrical performance and optical transmission for blue-emitting

μ LEDs, and it is used in Chapters 4 and 5.

With the n-GaN ohmic contact (Cr/Al/Ni/Au) and the p-GaN ohmic contact strategies (opaque Pd/Ni/Au and transparent ITO-based Type 4) established and quantitatively characterized using c-TLM and device-level JV measurements, the contact contributions to series resistance and injection non-idealities are now well constrained. This enables subsequent device studies to be interpreted with reduced ambiguity: changes in μ LED electrical and optical performance can be more confidently attributed to mechanisms unrelated to the contacts. The next chapter (Chapter 3) leverages this decoupling to examine passivation strategies aimed at suppressing sidewall recombination and improving μ LED efficiency.

Chapter 3

Minimizing interface defects and enhancing optical brightness of μ LEDs through polymeric encapsulants

3.1 Motivation & Scope

With the n- and p-type ohmic contact schemes established in Chapter 2, electrical injection losses are intentionally de-emphasized, providing a stable baseline for interpreting size-dependent behavior. With η_{elec} constrained in the WPE framework of Equation 1.1, this chapter focuses on preserving IQE during lateral scaling by suppressing sidewall-mediated SRH NRR.

As discussed in Chapter 1, reducing device dimensions increases the S2V ratio and amplifies the impact of etch-induced sidewall defects, which can dominate recombination even when bulk epitaxy and contacts are well optimized. This chapter quantifies and mitigates those perimeter-driven losses by comparing contrasting sidewall coating and repair approaches. The results motivate a two-regime picture in which larger devices are limited by bulk SRH while smaller devices are limited by surface-related recombination; a practical critical diameter, d_{crit} , is introduced to delineate this transition. Suppressing surface recombination reduces d_{crit} and enables geometric benefits (including size-dependent improvements in LEE) to be exploited in subsequent chapters.

3.2 Device Fabrication and Sidewall Passivation Schemes

Commercially available blue InGaN-based μ LED epitaxial heterostructures ($\lambda_{\text{emission}} = 445 \text{ nm}$) grown on double-side polished sapphire substrates were used in this work. Circular μ LED mesas were defined using ultraviolet photolithography and inductively coupled plasma (ICP) dry etching, resulting in mesas with a depth of approximately $1.5 \mu\text{m}$. Following mesa formation, the wafer was diced into $15 \text{ mm} \times 15 \text{ mm}$ chips. Five chips were fabricated, each incorporating a distinct sidewall passivation and surface treatment scheme to enable a systematic comparison of sidewall processing effects.

To investigate the influence of sidewall chemistry and encapsulation, devices employed either silicon dioxide (SiO_2)-based dielectric coatings or SU-8 epoxy-based negative photoresist (SU-8) polymer encapsulation, with and without post-etch KOH sidewall chemical treatment. Selected chips were subjected to a room-temperature KOH treatment following mesa etching. Rather than uniformly smoothing the complete mesa perimeter, KOH anisotropically removes plasma-damaged and crystallographically less stable GaN, allowing relatively stable nonpolar crystallographic facets to emerge. Individual facets can therefore be locally smooth, while the collection of differently oriented facets around the nominally circular mesa produces a faceted and macroscopically textured sidewall morphology. The resulting morphology is visible in the scanning electron micrographs presented in Appendix Figure A.1.

After sidewall processing, ohmic n- and p-type contacts were formed using standard lift-off metallization and rapid thermal annealing (RTA). The p-contact geometry was designed with a fixed radial offset of approximately $1.7 \mu\text{m}$ from the mesa edge, a value chosen to remain within the lateral current-spreading length typically reported for μ LEDs and thus avoid injection-limited operation.[22]

To complete the device, vias were patterned into the sidewall coating material, followed by aluminum deposition and patterning, with the aluminum serving as both probe pads and optical reflectors. Further fabrication details are provided in Appendix A, Section A.1.

3.3 Electrical and Optical Characteristics of Passivated μ LEDs

To isolate the role of sidewall processing, InGaN μ LEDs were fabricated using a common chlorine-based mesa etch and identical ohmic contacts, followed by two contrasting encapsulation strategies: a bilayer SiO_2 coating (10 nm atomic layer deposition (ALD) +

150 nm plasma-enhanced chemical vapor deposition (PECVD)) and a polymeric SU-8 3010 encapsulant.[23–26] Full fabrication details are provided in Appendix A, Section A.1.

Devices were characterized electrically (semiconductor parameter analyzer) and optically (calibrated photodiode collection through sapphire) under a light-tight Faraday-cage setup; measurement details are provided in Appendix A, Section A.2. From the measured IV characteristics and optical power, EQE and WPE were extracted using the definitions introduced in Chapter 1 (Equation 1.1). Figure 3.1 summarizes the resulting peak wall-plug efficiency (p-WPE) versus diameter for the two sidewall strategies.

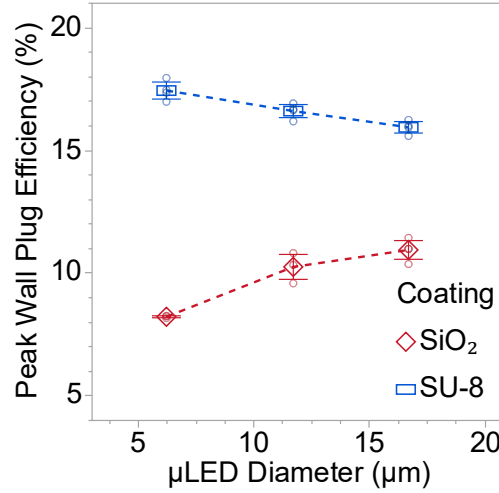


Figure 3.1: Size- and sidewall-coating-dependent efficiency of micro light-emitting diodes. Peak wall-plug efficiency plotted as a function of micro light-emitting diode diameter for devices incorporating silicon dioxide (red diamonds) and SU-8 (blue rectangles) sidewall coatings. Symbols represent mean values, and error bars indicate one standard deviation. Semi-transparent circles denote individual device measurements used to calculate the mean values, with colors corresponding to the associated sidewall coating scheme. Dotted lines are included as visual guides and do not represent fitted models. Sample sizes were $N = 3$ devices for silicon dioxide and $N = 4$ devices for SU-8.

To better understand the differences observed between the two sidewall coating schemes, the electrical characteristics of the μ LEDs were analyzed. Given that the largest optical performance discrepancy was observed in the 6 μ m devices, the electrical analysis focused on this device size. Electrical characterization involved extraction of the ideality factor

(IF) from the diode IV characteristics over an applied voltage range of 2 V to 3 V. The IF provides a diagnostic metric for assessing transport and recombination behavior that may not be readily apparent from standard linear or semi-logarithmic IV representations alone. The extraction is based on the non-ideal diode equation,

$$I = I_0 \exp \left(\frac{qV_{\text{app}}}{nkT} \right) \quad (3.1)$$

where I_0 is the dark saturation current, current (I) is the measured diode current, V_{app} is the applied voltage, n is the IF, q is the elementary charge, k is the Boltzmann constant, and $kT/q \approx 25.6$ meV at room temperature.

The IF is commonly used as a diagnostic framework for assessing recombination behavior associated with SRH processes within the device. In the ideal limit, corresponding to the absence of SRH recombination, $n = 1$. An IF of $n = 2$ is commonly associated with SRH recombination dominated by mid-gap defect states. In practical GaN-based devices, extracted IFs frequently exceed 2 due to parasitic contributions such as series resistance (R_s), shunt resistance (R_{sh}), or additional parasitic diode pathways originating from surface states or defects within the MQW plane.[3, 27] Examination of the IF as a function of applied voltage allows the device operation to be evaluated across bias regimes where different parasitic effects may influence the measured current.

Figure 3.2(a) shows the mean semi-logarithmic IV characteristics for 6 μm μLEDs incorporating SiO_2 and SU-8 sidewall coatings. The reverse-bias and low forward-bias currents measured between -3 V and 1.5 V remained within the noise floor of the measurement system, with no observable differences between the two sidewall coating schemes under reverse-bias conditions. Under forward bias, measurable current onset occurs near 1.5 V, with no discernible differences between the SiO_2 - and SU-8-coated devices in this voltage range. The slopes of the linear regions in the semi-logarithmic plots are comparable for both coating schemes, despite the differences observed in the p-WPE results shown in Figure 3.1.

Further analysis of the electrical behavior is presented in Figure 3.2(b), which shows the extracted IF as a function of applied voltage over the 2 V to 3 V range, corresponding to measured currents spanning approximately 1 pA to 10 μA for the 6 μm devices. Both sidewall coating schemes exhibit a minimum IF of approximately $n \approx 1.6$ near 2.5 V, corresponding to a current level of approximately 30 nA to 40 nA. The minimum IF corresponds to the bias regime where the measured current is least influenced by parasitic contributions. At low forward bias, elevated IFs may arise from leakage through parallel conduction paths, such as shunt resistance or parasitic diode pathways, while at higher forward bias,

series resistance becomes increasingly influential. Accurate extraction of the IF is therefore confined to the sub-turn-on regime, provided that the contact resistance remains low and the effective shunt resistance is sufficiently high.[3] In devices with substantial parasitic contributions, a well-defined ideality region may not be observable. In general, minimum IFs exceeding $n = 2$ are indicative of significant parasitic influences, including R_s , R_{sh} , or other parasitic diode components.[3, 27]

At applied voltages above approximately 2.5 V, the extracted IF increases rapidly, coinciding with a reduction in the slope of the semi-logarithmic IV characteristics with increasing V_{app} . This behavior is consistent with R_s effects associated with the p- and n-type ohmic contacts. Owing to the lower achievable doping concentrations in p-GaN relative to n-GaN, the p-contact is expected to dominate the R_s at higher current densities.[2] The higher mean forward current measured for the SiO₂-coated devices at voltages above 2.5 V is attributed to lithographic variations in the p-contact geometry. For the 6 μm mesas, deviations of up to $\pm 0.32 \mu\text{m}$ relative to the mesa diameter were observed and contribute to the measured current variations.

At applied voltages below 2.5 V, an increase in the extracted IF above the minimum value and exceeding $n = 2$ is observed, indicating the presence of parasitic current pathways under forward-bias conditions. The full IV characteristics measured from -3 V to 5 V , shown in Figure 3.2(a), indicate that this sub-threshold parasitic current is present only under forward bias. Possible contributions include carrier transport via surface-related trap states along the diode perimeter or through defect-related regions within the device structure.[3]

The SiO₂-coated 6 μm μLEDs exhibit a slightly higher IF compared to devices incorporating SU-8 encapsulation within the applied voltage range of approximately 2.0 V to 2.4 V, corresponding to measured currents between approximately 1 pA to 10 nA. The elevated IF indicates increased sub-threshold parasitic current contributions in the SiO₂-coated devices, consistent with carrier transport through surface-related trap states along the diode perimeter or defect-assisted leakage pathways.[3] These electrical observations are consistent with the WPE results, where the p-WPE of the 6 μm SU-8-encapsulated devices is approximately 1.6 times higher than that of the corresponding SiO₂-coated devices. While the electrical measurements indicate reduced parasitic contributions in the SU-8-encapsulated devices, these results alone do not fully account for the origin of the improvement observed in Figure 3.1.

To further analyze the observed efficiency trends, the WPE as a function of current density (J) was examined for μLEDs with diameters of 6 μm , 12 μm , and 17 μm , incorporating both SiO₂ and SU-8 sidewall coating schemes, as shown in Figure 3.3. The J was

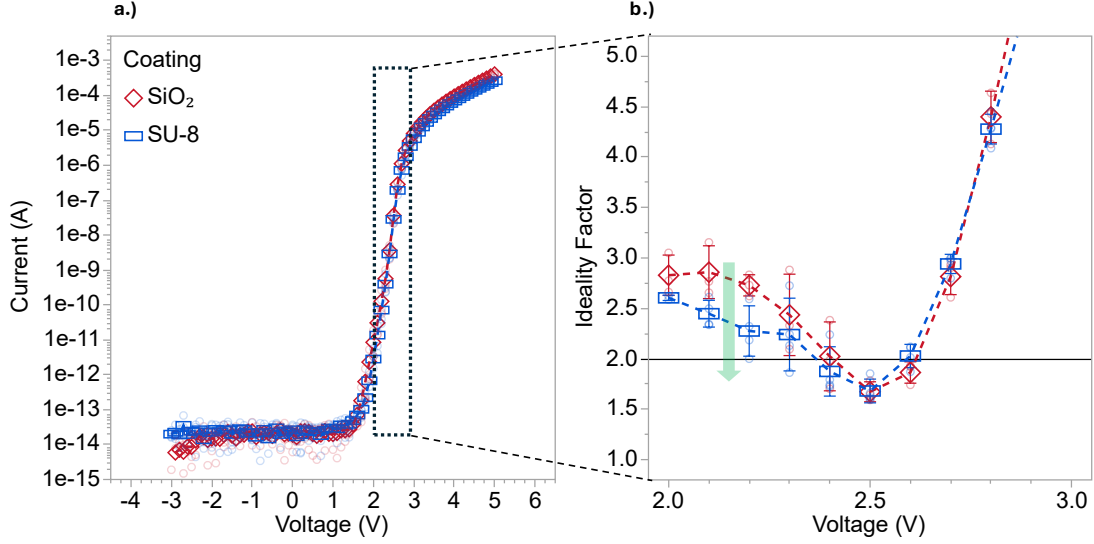


Figure 3.2: Sidewall-coating-dependent electrical characteristics of 6 μm micro light-emitting diodes. (a) Semi-logarithmic current-voltage characteristics for devices incorporating silicon dioxide (red diamonds) and SU-8 (blue rectangles) sidewall coatings. (b) Corresponding ideality factor extracted as a function of applied voltage for the same devices. The voltage range used for ideality factor extraction is indicated in panel (a) by the dashed box. Symbols represent mean values, and error bars indicate one standard deviation. Semi-transparent circles denote individual device measurements used to calculate the mean values, with colors corresponding to the associated sidewall coating scheme. Dotted lines are included as visual guides and do not represent fitted models. Sample sizes were $N = 3$ devices for silicon dioxide and $N = 4$ devices for SU-8.

calculated using the mesa area for all device sizes and sidewall coating conditions.

Across all diameters, SU-8-encapsulated μLEDs exhibit higher WPE compared to SiO₂-coated devices of identical dimensions. For the 6 μm devices, SU-8 encapsulation yields a mean p-WPE of approximately 17.4% at a J of approximately 6 A cm^{-2} , whereas the SiO₂-coated devices reach a mean p-WPE of approximately 8% at a J of approximately 16 A cm^{-2} . For both sidewall coating schemes, the J at which p-WPE occurs increases as the device diameter decreases. However, the increase in J with decreasing diameter is smaller for the SU-8-encapsulated devices. Since the sidewall coating is the only variable altered in these experiments, the reduced diameter sensitivity is consistent with a reduction in sidewall-related SRH recombination in the SU-8-coated devices.[28–30] Correspondingly, the SU-8-encapsulated μLEDs exhibit increasing p-WPE with decreasing

diameter, whereas the SiO₂-coated devices show a decreasing p-WPE as the diameter is reduced. This behavior is consistent with the higher IF values observed for the SiO₂-coated devices in the sub-threshold regime, as shown in Figure 3.2(b).

In addition to the electrical characteristics, optical contributions must also be considered. Previous studies have reported that geometric scaling can increase LEE in smaller mesas by reducing TIR and shortening optical path lengths, thereby lowering the probability of photon reabsorption.[1, 31–33] This size-dependent increase in LEE contributes directly to WPE when the v_s is sufficiently low; otherwise, non-radiative losses dominate and limit the observable benefit. To quantify the combined influence of v_s and LEE, the measured efficiency curves were analyzed using the Shockley-Read-Hall, bimolecular, Auger, and drift–leakage recombination model (ABCCD) recombination framework, as described in the following section.

3.4 Surface and Bulk Recombination Analysis

Starting with the EQE, the relationship between extraction and internal recombination is written as

$$EQE = LEE \cdot IQE \quad (3.2)$$

Here, LEE is defined previously, and the IQE is described using the ABCCD recombination framework as

$$IQE = IE \cdot \frac{Bn^2}{An + Bn^2 + C_{\text{aug}}n^3 + C_{\text{dl}}n^3 + D_{\text{dl}}n^4} \quad (3.3)$$

In this expression, IE is the carrier injection efficiency, defined as the fraction of injected carriers that reach the active region and are available for radiative recombination. In the present analysis, IE is assumed to be equal to unity. The coefficient A , with units of s^{−1}, represents the total effective SRH recombination coefficient and is expressed for a μ LED as

$$A = A_0 + A_s \quad (3.4)$$

Here, A_0 is the bulk SRH recombination coefficient with units of s^{−1}, and A_s is the surface-related SRH recombination coefficient, also with units of s^{−1}. The surface contribution is written as

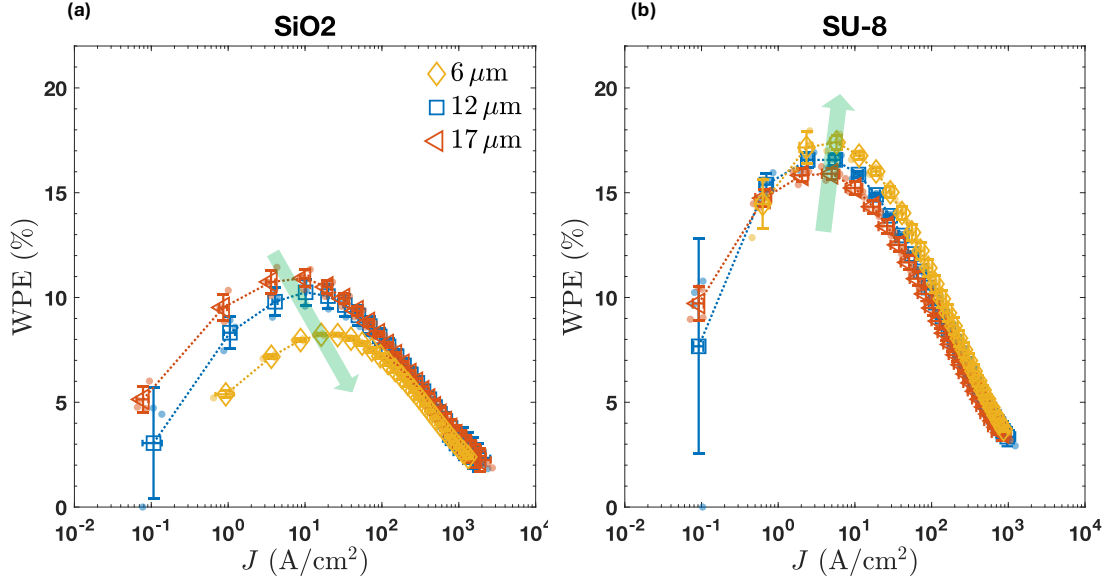


Figure 3.3: Opto-electrical efficiency of micro light-emitting diodes with different sidewall coatings. (a) Wall-plug efficiency as a function of current density for silicon dioxide-coated micro light-emitting diodes. (b) Wall-plug efficiency as a function of current density for SU-8-coated micro light-emitting diodes. Micro light-emitting diode diameters are indicated by $6\text{ }\mu\text{m}$ (yellow diamonds), $12\text{ }\mu\text{m}$ (blue squares), and $17\text{ }\mu\text{m}$ (red triangles). Symbols represent mean values, and error bars indicate one standard deviation. Semi-transparent symbols denote individual device measurements used to calculate the mean values, with colors corresponding to the associated device diameter. Dotted lines are included as visual guides and do not represent fitted models. Sample sizes were $N = 3$, 3 , and 4 devices for silicon dioxide-coated micro light-emitting diodes with diameters of $6\text{ }\mu\text{m}$, $12\text{ }\mu\text{m}$, and $17\text{ }\mu\text{m}$, respectively, and $N = 4$ devices for each SU-8-coated diameter.

$$A_s = v_s \frac{S_{\text{active}}}{V_{\text{active}}} \quad (3.5)$$

In this form, S_{active} and V_{active} denote the sidewall surface area and the volume of the MQW active region, respectively. The parameter v_s , with units of cm s^{-1} , characterizes the effective surface recombination velocity of the sidewall interface and is treated as independent of device size for a given surface chemistry and processing condition. The ratio $S_{\text{active}}/V_{\text{active}}$ represents a geometric scaling factor for surface recombination and is equivalent to perimeter-to-area-type metrics commonly used in μLED analyses.[34, 35]

For devices with circular mesa geometries and diameter d , the total SRH recombination coefficient is written as

$$A = A_0 + v_s \frac{4}{d} \quad (3.6)$$

The surface recombination velocity is related to the interface trap density interface trap density (N_{it}) through

$$v_s = \sigma_{it} v_{th} N_{it} \quad (3.7)$$

Here, σ_{it} is the capture cross-section of interface traps, with units of cm^2 , and v_{th} is the thermal velocity of carriers, with units of cm s^{-1} . [36] Similarly, the bulk SRH recombination coefficient is given by

$$A_0 = \sigma_{bulk} v_{th} N_t \quad (3.8)$$

In this expression, σ_{bulk} is the capture cross-section of bulk traps, and N_t is the bulk trap density.

For the remaining parameters in Equation 3.3, B is the bimolecular radiative recombination coefficient, typically on the order of $1 \times 10^{-10} \text{ cm}^3 \text{ s}^{-1}$ for GaN-based LEDs, while C_{aug} denotes the Auger recombination coefficient, commonly reported to be less than or equal to $1 \times 10^{-31} \text{ cm}^6 \text{ s}^{-1}$. [3]

The higher-order coefficients C_{dl} and D_{dl} account for drift-induced carrier leakage and become relevant at elevated carrier concentrations. The carrier concentration, n , varies with the applied drive current. For InGaN-based devices, values of C_{dl} are frequently reported to be much larger than C_{aug} , typically in the range of $1 \times 10^{-29} \text{ cm}^6 \text{ s}^{-1}$ to $1 \times 10^{-28} \text{ cm}^6 \text{ s}^{-1}$. [3]

To extract effective SRH recombination parameters, including v_s , the measured EQE as a function of J is fitted using the ABCCD framework. [30, 37] Accurate fitting of EQE data requires explicit consideration of LEE, which has been reported to exhibit a dependence on device size. [1, 31–33, 38] Because the present study investigates both mesa diameter and sidewall coating while other variables are held constant, a size-dependent LEE term is included to improve the consistency of the comparative analysis. The diameter dependence of LEE is described using an empirical first-order expression

$$LEE(d) = LEE_{\infty} + \alpha d^{-\beta} \quad (3.9)$$

In this formulation, LEE_∞ represents the asymptotic LEE of an infinitely large device, accounting for baseline losses associated with TIR and absorption in structures with identical epitaxial layers and metal contacts. The parameter d is the diameter of the circular μ LED. The parameters α and β quantify the extent to which LEE is influenced by device geometry, where α serves as a proportionality constant and β is a power-law exponent. Both parameters depend on the μ LED epitaxial structure and device architecture, as well as on the specific approaches employed to enhance light extraction, including surface roughening, microlenses, photonic crystals, and metasurfaces, and on photon absorption pathways associated with defects, metal layers, and reabsorption within the MQW active region.

This model is supported by prior results reported by Ryu et al., who demonstrated an increase in LEE with decreasing circular μ LEDs diameter using three-dimensional finite-difference time-domain (FDTD) simulations.[38] In that work, the size dependence of LEE was discussed in terms of the interplay between TIR and absorption in the GaN/InGaN layers and the metallic contacts. As the device dimension increases, a larger fraction of emitted photons undergoes TIR, resulting in an increased optical path length. An increased path length raises the probability of absorption within the GaN/InGaN active region, defect states, or metal layers, contributing to net optical loss. In contrast, smaller μ LEDs experience reduced TIR-induced trapping, leading to fewer absorption events and higher LEE. Agreement between the empirical relationship given by Equation 3.9 and the data reported by Ryu et al. supports the applicability of this relationship for describing the size dependence of LEE in circular μ LEDs over diameters between 2 μ m to 25 μ m.

To fit the measured EQE as a function of J , a constrained global fitting procedure was implemented using a standard MATLAB nonlinear optimization routine. The measured EQE curves were modeled according to

$$\begin{aligned} EQE(d, n) &= LEE(d) \times IQE(d, n) \\ &= [LEE_\infty + \alpha d^{-\beta}] \times IE \times \frac{Bn^2}{(A_0 + \frac{4v_s}{d})n + Bn^2 + C_{\text{aug}}n^3 + C_{\text{dl}}n^3 + D_{\text{dl}}n^4} \end{aligned} \quad (3.10)$$

In this expression, the diameter dependent LEE is represented by $LEE_\infty + \alpha d^{-\beta}$, while the diameter dependent surface recombination contribution enters independently through the $\frac{4v_s}{d}$ term. The model therefore treats optical extraction and surface recombination as distinct contributions to EQE. The Auger coefficient, C_{aug} , was omitted from the fitting expression because its reported magnitude is substantially smaller than the effective third order drift and leakage coefficient, C_{dl} , for the devices and operating range considered here. Accordingly, the fitted third order contribution is represented by C_{dl} .

For each measured value of J , the corresponding carrier concentration n was determined by numerically solving the total recombination equation

$$R(n, d) = \left(A_0 + \frac{4v_s}{d} \right) n + Bn^2 + C_{\text{dl}}n^3 + D_{\text{dl}}n^4 \quad (3.11)$$

where the total recombination rate was related to the measured current density through

$$R = \frac{JA_{\mu\text{LED}}}{qV_{\text{active}}} \quad (3.12)$$

Here, $A_{\mu\text{LED}}$ is the cross-sectional area of the μLED , V_{active} is the volume of the MQW active region, and q is the elementary charge. At each current density, the physically meaningful positive real solution for n was used to calculate the modeled IQE and EQE. The optimization routine varied the fitting parameters within physically defined bounds and minimized the total sum of squared errors between the measured and modeled EQE.

Rather than fitting each EQE curve independently, all nine curves were fitted simultaneously. These curves comprised three device diameters, 6 μm , 12 μm , and 17 μm , for each of the three sidewall coating or treatment conditions: untreated SiO_2 , untreated SU-8, and KOH-treated SU-8. The epitaxial layer dependent recombination coefficients A_0 , B , C_{dl} , and D_{dl} were shared across all devices because the devices were fabricated from the same epitaxial wafer. This constraint assumes that changing the sidewall coating or treatment modifies the semiconductor interface without changing the bulk defect concentration or the intrinsic recombination properties of the epitaxial layers.

Within each sidewall coating or treatment condition, a single value of v_s was shared across all three device diameters. This constraint reflects the treatment of v_s as an effective property of the processed sidewall interface rather than a device size dependent parameter. The influence of device size on surface recombination was instead introduced explicitly through the $\frac{4v_s}{d}$ term. Consequently, one value of v_s was required to reproduce the systematic diameter dependence of all three EQE curves associated with a given sidewall condition.

The complete measured current density range was included in the fitting procedure. At low current density, the modeled efficiency is particularly sensitive to the SRH recombination terms A_0 and v_s . At higher current density, the higher order C_{dl} and D_{dl} terms become increasingly important. Fitting the entire EQE curve therefore constrains these higher order terms using the high injection regime, rather than requiring them to be selected arbitrarily, while the use of multiple device diameters constrains v_s through its expected geometric dependence.

The principal benefit of this global fitting approach is that the extracted v_s is constrained simultaneously by the current density dependence and diameter dependence of

EQE. Because LEE and surface recombination enter the model through separate terms, and because a common v_s must reproduce measurements from multiple device diameters, the procedure reduces the likelihood that diameter dependent optical extraction or individual device variation is incorrectly attributed to changes in surface recombination. The resulting global recombination coefficients and sidewall dependent v_s values are summarized in Table 3.1. Comparisons between the measured and modeled EQE curves are provided in Appendix A.4.

The extracted parameters are constrained by the experimentally investigated diameter range of 6 μm to 17 μm . Calculations for diameters below 6 μm , including the predicted values of d_{crit} , therefore represent extrapolations of the fitted model rather than direct experimental measurements. Additional details regarding the numerical implementation and fitting constraints are retained in Appendix A.4.

The extracted coefficients, which primarily reflect the epitaxial wafer properties, are consistent with values reported in the literature.[3, 37] Using the bulk and surface recombination formulations introduced above, bulk trap density (N_t) and interface trap density N_{it} can be estimated once representative carrier capture cross-sections are assumed. Reported capture cross-sections span several orders of magnitude, from $1 \times 10^{-17} \text{ cm}^2$ to $1 \times 10^{-14} \text{ cm}^2$, depending on trap energy, charge state, and surface preparation.[39–41] For a first-order numerical estimate, a capture cross-section of $5 \times 10^{-16} \text{ cm}^2$ and a thermal velocity of $2 \times 10^7 \text{ cm s}^{-1}$ are adopted, corresponding to values near the geometric mean of the reported range and representative of room-temperature carrier thermal velocities. Using these assumptions, N_t is calculated to be approximately $2.7 \times 10^{14} \text{ cm}^{-3}$. The interface trap density N_{it} is calculated assuming identical thermal velocity and capture cross-section values for bulk and surface traps. The extracted surface recombination velocity v_s and N_{it} for each sidewall coating scheme are listed in Table 3.1. Within the ABCCD framework, the global coefficients are fixed across all devices and sidewall coating conditions, while only the surface-related recombination term varies. This term, and the associated v_s , is the sole parameter in the recombination model that depends on sidewall treatment. The MATLAB code used to implement the global fitting procedure, together with example input data, has been made publicly available through Figshare.[42]

The extracted v_s for the SU-8 encapsulation is approximately one order of magnitude lower than that obtained for the SiO_2 coating. This trend is consistent with the measured WPE as a function of device size shown in Figure 3.1 and Figure 3.3, where silicon-dioxide-coated devices exhibit a shift of the current density at peak WPE toward higher values with decreasing diameter, while SU-8-encapsulated devices show a comparatively smaller shift. The lower v_s associated with SU-8 indicates a reduced contribution of surface-related recombination relative to bulk recombination within the analyzed size

range.

Table 3.1: Extracted sidewall-coating-dependent recombination coefficients and calculated N_{it} and d_{crit} .

Extracted recombination coefficient	SiO ₂	SU-8	SU-8 with KOH
A_0 (s ⁻¹)		2.8×10^6	
B (cm ³ /s)		1.1×10^{-10}	
C_{dl} (cm ⁻⁶ /s)		1.1×10^{-29}	
D_{dl} (cm ⁹ /s)		2.8×10^{-47}	
v_s (cm s ⁻¹)	2.97×10^3	404	<10
N_{it} (cm ⁻²)	3×10^{11}	4×10^{10}	$< 1 \times 10^8$
d_{crit} (μm)	43	6	<0.1

To quantify the contribution of surface-related SRH recombination to the total SRH recombination rate, the total SRH term can be normalized by the bulk component. This normalization yields the relationship shown in Equation 3.13,

$$\frac{A}{A_0} = \frac{4v_s}{A_0 d} + 1 \quad (3.13)$$

where A is the total SRH recombination coefficient, A_0 is the bulk SRH recombination coefficient, v_s is the surface recombination velocity, and d is the μLED diameter.

Ratios approaching 1 indicate that bulk SRH recombination dominates the total SRH recombination rate, which can occur for sufficiently large device diameters or for material systems with relatively high bulk recombination compared to surface contributions. Conversely, large values of A/A_0 indicate an increased relative contribution of surface-related SRH recombination, which may arise from small μLEDs diameters or elevated v_s . This ratio defines a reference condition corresponding to equal bulk and surface SRH recombination rates, given by $A = 2A_0$, or equivalently $A/A_0 = 2$. Based on this condition, a critical diameter d_{crit} can be defined, representing the μLED diameter at which the bulk and surface SRH recombination contributions are equal. The critical diameter is given explicitly by Equation 3.14,

$$d_{crit} = \frac{4v_s}{A_0} \quad (3.14)$$

where all variables retain the definitions given above.

The value of d_{crit} depends on both v_s and A_0 . These parameters are influenced by epitaxial material quality as well as by the μLED fabrication process, including the sidewall

coating or treatment applied to mitigate sidewall defects. This dependence is illustrated in Figure 3.4, which shows the normalized SRH recombination ratio A/A_0 as a function of μ LED diameter for the two sidewall coating schemes investigated in this study. The variation reflects the differing contributions of surface and bulk SRH recombination across device sizes for SiO_2 and SU-8 sidewall coatings.

Figure 3.4 also illustrates the dependence of the normalized recombination ratio on v_s . The plotted curves are generated using the extracted fitting parameters A_0 and the sidewall-coating-dependent values of v_s , as summarized in Table 3.1. These parameters are used to extrapolate the behavior of A/A_0 to μ LED diameters both smaller and larger than the experimentally investigated range. This extrapolation defines the size regimes over which bulk or surface SRH recombination is expected to dominate and enables extraction of a characteristic d_{crit} for each sidewall coating scheme. For standard sidewall coatings such as SiO_2 , the model predicts a pronounced increase in surface-related SRH recombination at comparatively large μ LED diameters. In contrast, SU-8 encapsulation corresponds to smaller values of d_{crit} , indicating reduced sensitivity to surface recombination as device dimensions decrease.

The horizontal black line in Figure 3.4 denotes the condition $A/A_0 = 2$, corresponding to equal bulk and surface SRH recombination contributions. For silicon-dioxide-coated devices, the intersection with this condition occurs at a diameter of approximately $43\text{ }\mu\text{m}$, consistent with the extracted d_{crit} . Because the μ LED diameters investigated in this study are substantially smaller than this value, the normalized recombination ratio indicates a regime dominated by surface-related NRR for oxide-coated devices. Since all devices were fabricated from the same epitaxial heterostructure and processed using identical mesa etching conditions, differences in recombination behavior are attributed to the sidewall coating and the resulting semiconductor–dielectric interface.

The subsequent analysis of the SU-8-encapsulated diodes further suggests that NRR originating from the bulk is not a dominant contribution for the oxide-coated devices. SU-8-encapsulated diodes exhibit a d_{crit} of approximately $6\text{ }\mu\text{m}$, which is approximately seven times smaller than that extracted for the oxide-coated devices. Given the comparatively low v_s relative to the bulk SRH coefficient A_0 for the SU-8 encapsulation, size-dependent SRH recombination is not the dominant mechanism governing optical degradation in these devices. The normalized SRH recombination remains relatively constant with decreasing μ LED diameter, exhibiting minimal variation until the device size approaches d_{crit} .

For the SU-8 encapsulation, the $6\text{ }\mu\text{m}$ -diameter μ LED lies close to the predicted critical diameter. Although SU-8 is employed as an encapsulation material in this work, experimental observations suggest that it may also provide electronic passivation effects. This

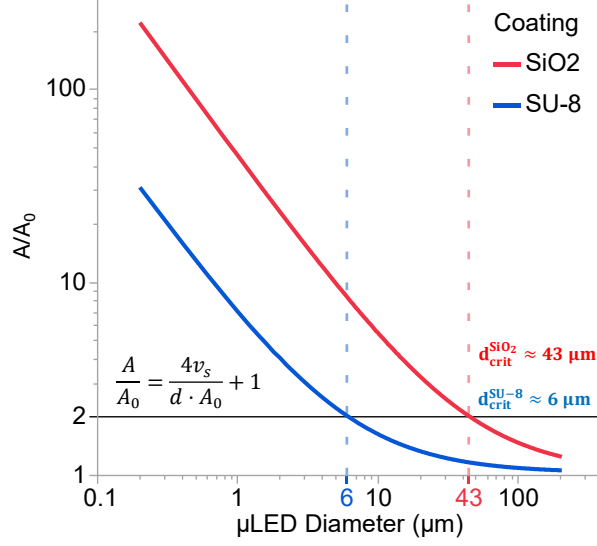


Figure 3.4: Normalized Shockley–Read–Hall recombination as a function of μ LED size. Normalized total Shockley–Read–Hall recombination rate, expressed as A/A_0 , plotted as a function of μ LED diameter d for devices with silicon dioxide (red solid line) and SU-8 (blue solid line) sidewall coatings. Values of A/A_0 are extracted from fitting the external quantum efficiency model to the experimental data, as described in Appendix A.4. The inset equation shows the size-dependent Shockley–Read–Hall recombination model, where A is the total recombination coefficient, A_0 is the bulk contribution, v_s is the surface recombination velocity, and d is the μ LED diameter. The horizontal black line at $A/A_0 = 2$ indicates the condition where bulk and surface Shockley–Read–Hall recombination contributions are equal. Vertical dashed lines mark the corresponding critical diameters d_{crit} for each coating scheme.

inference is supported by the lower extracted IF in the low-current regime, as shown in Figure 3.2, and by the reduced extracted v_s compared to SiO_2 . Additional experimental characterization is required to conclusively establish SU-8 as a passivation layer for InGaN μ LEDs.

Although surface recombination effects are minimal for SU-8 encapsulated devices, a size-dependent efficiency is still observed in Figure 3.1 for diameters below $20\,\mu\text{m}$. This behavior is consistent with a size-dependent LEE, as reported in prior studies.[1, 31–33, 38] While LEE varies with device size, our measurements show no detectable evidence of LEE changing as a function of J in the high- J regime. The extracted $\text{LEE}(d)$ values obtained

using the empirical model in Equation 3.9 increase with decreasing μ LED diameter for the SU-8-coated devices, as presented in Figure 3.5. Both Figure 3.5 and the fitted LEE model are limited to $\eta_{\text{LEE}} \leq 60\%$ to reflect the $\sim 60\%$ reflectivity of 30 nm Pd at 460 nm.

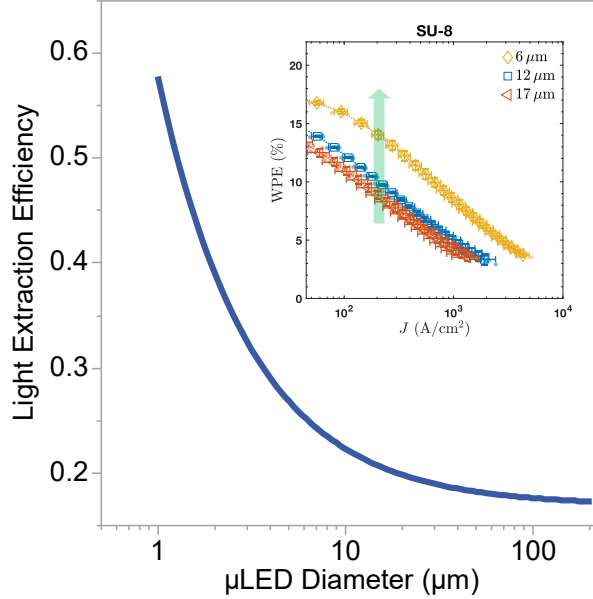


Figure 3.5: Extracted light extraction efficiency of SU-8 encapsulated μ LEDs. Extracted light extraction efficiency (LEE) plotted as a function of μ LED diameter for SU-8 encapsulated devices. Values are obtained from fitting the EQE model to the experimental data, as described in Appendix A.4. The plotted range and fitting model are limited to $\text{LEE} \leq 60\%$ to reflect the approximately 60% reflectivity of a 30 nm Pd contact at 460 nm. Inset: Peak wall plug efficiency (p-WPE, %) plotted as a function of current density (J , A cm^{-2}), normalized by the p contact area, highlighting the high current regime where lateral current spreading beyond the p contact is reduced and size dependent light extraction differences are apparent. Symbols depicting device diameters of 6 μm (yellow diamonds), 12 μm (blue squares), and 17 μm (red triangles) represent mean values; error bars indicate the standard deviation, and semi transparent symbols denote individual device measurements. Sample sizes in the inset were $N = 4$ devices for all μ LED diameters. Dotted lines are included as visual guides to aid interpretation and do not represent fitted models.

The inset of Figure 3.5 shows the WPE plotted as a function of J normalized by the p contact area. This data shows recombination is increasingly localized beneath the p contact, reducing lateral spreading toward the mesa sidewalls.[3] As a consequence, a smaller

fraction of injected carriers reaches the sidewalls and sidewall related non radiative losses become less dominant, with LEE increasing. This behavior is consistent with prior experimental and simulation studies of μ LEDs with finite p contact geometries, which show that current spreading beyond the p contact footprint diminishes at elevated J . [22] In this high- J regime, the WPE (Figure 3.5 inset) increases as the device diameter decreases, consistent with the extracted size dependent increase in LEE. Similar high current WPE enhancements with decreasing μ LED size have been reported in previous studies emphasizing light extraction effects, although those reports typically employ full mesa p contacts, whereas the present devices utilize a reduced p contact footprint. [31] Consequently, the improvement in WPE observed in SU-8 encapsulated devices (Figure 3.1) may be driven by enhancement in LEE, rather than changes in IQE.

To examine this hypothesis, a KOH sidewall etch treatment was applied in combination with the polymeric coating. The KOH wet-etch method is commonly utilized to mitigate sidewall defects induced by the dry-etching process of GaN, and μ LED devices were fabricated with and without KOH treatment prior to the SU-8 encapsulation. [39] Figure 3.6 presents the WPE as a function of J for the different μ LED diameters (6 μm , 12 μm , and 17 μm) comparing both treatment scenarios. Figure 3.3 (SU-8 encapsulated, right) and Figure 3.6 (no treatment, left) present the same image/plot. The general trend of increasing efficiency with decreasing device size is consistent between both treatment methods. However, Figure 3.6 clearly indicates that KOH-treated devices consistently exhibit higher peak WPE values across all tested diameters. The largest improvement due to KOH treatment is observed at the smallest device diameter (6 μm), achieving a peak WPE increase of approximately 15 % compared to untreated devices. No observable shift in the $J_{\text{peak-WPE}}$ was observed, suggesting negligible surface SRH recombination. The KOH treated sidewall devices had an average p-WPE of 20.3 % at an average J of 2.5 A cm^{-2} for the 6 μm blue InGaN μ LEDs.

The KOH-treated sidewall exhibits a macroscopically textured morphology comprising multiple exposed crystallographic facets. KOH etching of GaN is anisotropic and preferentially removes plasma-damaged and crystallographically less stable material, allowing relatively stable nonpolar facets to emerge. Thus, although the complete sidewall appears rough at the scale of the mesa perimeter, the individual exposed facets may remain locally smooth. For the nominally circular mesas investigated here, the collection of facets distributed around the perimeter introduces changes in local sidewall orientation that can redirect laterally propagating photons, reduce TIR-induced confinement, and enhance LEE. [28, 43]

Figure 3.7(a) shows the LEE improves for μ LED sizes below 10 μm , directly correlated to the 15 % increase in the WPE observed in Figure 3.5. Both Figure 3.7(a) and the fitting

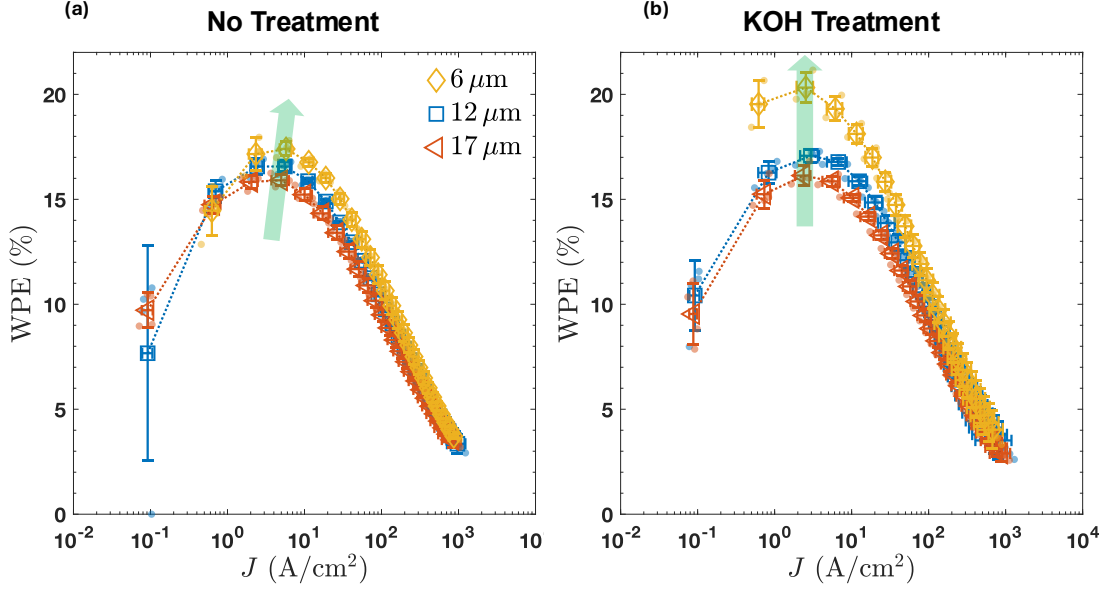


Figure 3.6: Opto electrical efficiency of SU-8 encapsulated μLED s with different sidewall treatments: Peak wall plug efficiency (p-WPE, %) plotted as a function of current density (J , A cm^{-2}) for μLED s with diameters of 6 μm (yellow diamonds), 12 μm (blue squares), and 17 μm (red triangles) without sidewall treatment (left) and with KOH treatment (right). Symbols represent mean values; error bars indicate the standard deviation. Semi-transparent symbols denote individual device measurements used to calculate the mean. Dotted lines are included as visual guides to aid interpretation and do not represent fitted models. Green arrows indicate the qualitative variation in WPE with decreasing μLED diameter. Sample sizes were $N = 3, 4$, and 4 devices for KOH treated μLED s with diameters of 6, 12, and 17 μm , respectively, and $N = 4$ devices for all untreated μLED diameters. The untreated SU-8 data shown in the left panel are identical to the SU-8 dataset presented in Figure 3.3 (right panel) and are reproduced here for direct comparison.

model have been limited to $\text{LEE} \leq 60\%$ to reflect the $\sim 60\%$ reflectivity of 30 nm Pd at 460 nm. These observations help explain the improved LEE values extracted from the fitted model and the corresponding increase in WPE shown in Figure 3.6.

The effect of KOH etching was further evaluated using the d_{crit} model by extracting the recombination coefficients from EQE versus J data (Table 3.1). The extracted v_s for the devices treated with the KOH etch was substantially reduced; the KOH-treated samples exhibit v_s values of $< 10 \text{ cm s}^{-1}$, among the lowest reported for InGaN μLED s.[5] Conse-

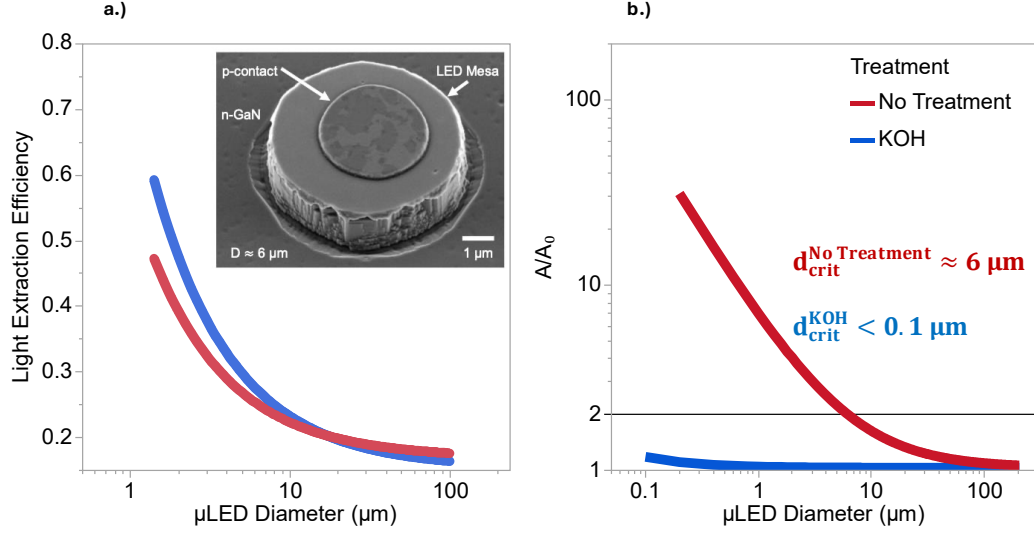


Figure 3.7: (a) Extracted light extraction efficiency plotted as a function of μ LED diameter for untreated (red solid line) and KOH treated (blue solid line) devices. Values are obtained from fitting the EQE model to the experimental data, as described in Appendix A.4. The plotted range and fitting model are limited to light extraction efficiency $\leq 60\%$ to reflect the approximately 60% reflectivity of a 30 nm Pd contact at 460 nm. Inset: Tilted scanning electron micrograph of a $6 \mu\text{m}$ μ LED following KOH treatment and prior to SU-8 encapsulation. (b) Extracted normalized Shockley–Read–Hall recombination rate (A/A_0) plotted as a function of μ LED diameter for untreated and KOH treated devices, obtained from fitting to the recombination model. The black horizontal line at $A/A_0 = 2$ indicates the condition where bulk and surface SRH recombination contributions are equal.

quently, the extracted d_{crit} for KOH-treated SU-8 encapsulated μ LEDs was predicted to be smaller than $0.1 \mu\text{m}$ (Figure 3.7(b)) compared to the non-KOH treated diodes. Under extrapolation of the fitted model, surface recombination is predicted to remain below the bulk SRH contribution down to submicrometer dimensions. This prediction has not been experimentally validated below the minimum measured diameter of $6 \mu\text{m}$. Thus, employing an effective sidewall treatment (KOH etching) combined with a suitable sidewall coating scheme (SU-8) enabled top-down etched InGaN μ LEDs to achieve high-performance operation.

Further analysis of the electrical characteristics, illustrated by the IV and IF versus voltage plots in Figure 3.8, reveals nearly identical behavior for both treatment conditions, suggesting minimal electrical differences resulting from the KOH sidewall treatment. The

minimum mean IF values for untreated and treated devices are $n = 1.68$ and $n = 1.54$, respectively. Although there is a slight decrease in minimum IF, the difference is insignificant and within the measurement error.

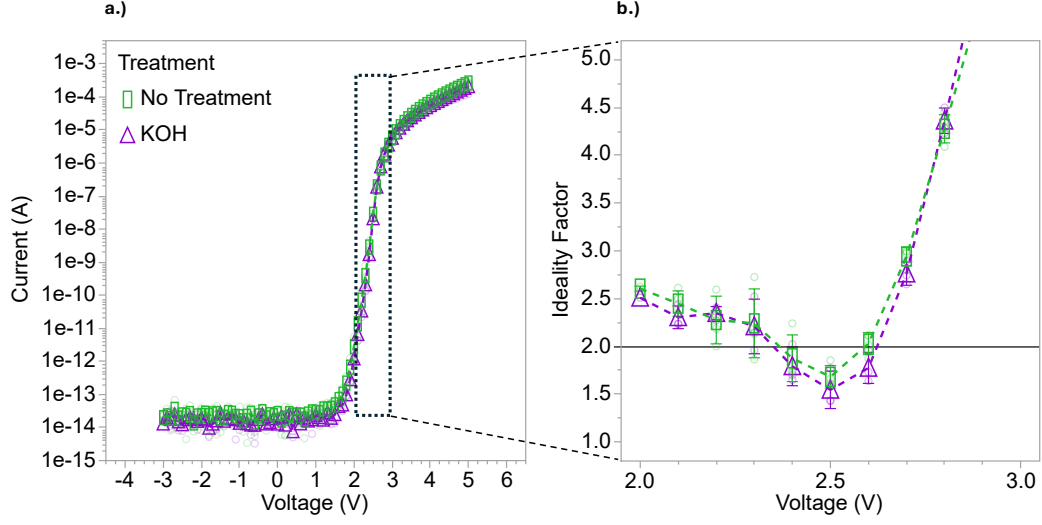


Figure 3.8: (a) Semi logarithmic current–voltage characteristics for SU-8 encapsulated $6\ \mu\text{m}$ μLEDs without sidewall treatment (green rectangles) and with KOH treatment (purple triangles). (b) Corresponding mean ideality factor plotted as a function of applied voltage for the same devices, extracted over the voltage range highlighted in panel (a). Symbols represent mean values; error bars indicate the standard deviation. Semi transparent symbols denote individual device measurements used to calculate the mean. Sample sizes were $N = 4$ devices for untreated μLEDs and $N = 3$ devices for KOH treated μLEDs .

As shown in Figure 3.6, KOH treatment enhances the efficiency of SU-8-encapsulated devices by reducing v_s and improving the LEE, particularly at smaller diameters. Devices treated with KOH and coated with SiO_2 exhibit substantially lower p-WPE compared to KOH-treated SU-8-coated devices, as evident from the size-dependent trends in Figure 3.9. While KOH treatment provides optical benefits, it is not sufficient by itself. The results, supported by the presented models, indicate that the impact of KOH is constrained by factors such as bulk epitaxial layer quality, sidewall coating selection, and sidewall etching processes.

These results demonstrate the potential effectiveness of using polymeric materials and simple etching processes for fabricating high-performance light emitters. This approach creates a feasible approach for producing large-area arrays of μLED media for high-resolution

displays, creating a pathway for display applications requiring high pixel density, low-cost, and high brightness.

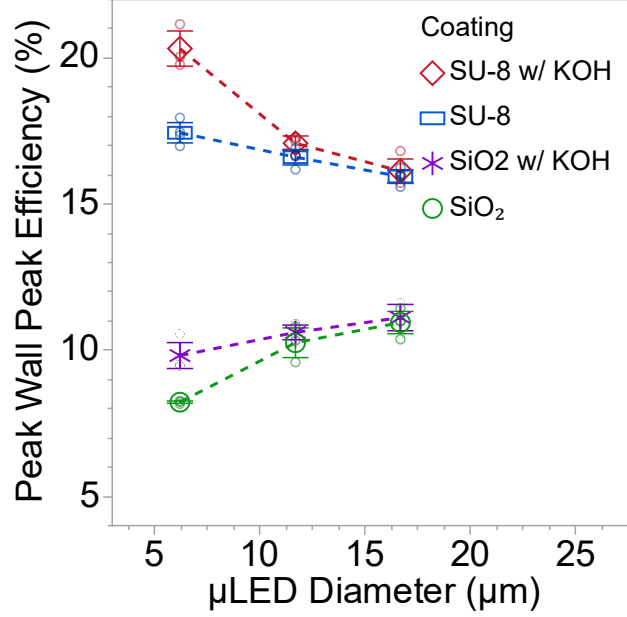


Figure 3.9: Size- and sidewall-coating-dependent efficiency of μ LEDs: Peak wall plug efficiency (p-WPE, %) plotted as a function of μ LED diameter for devices with SiO₂ (green circles), SiO₂ with KOH treatment (purple stars), SU-8 (blue rectangles), and SU-8 with KOH treatment (red diamonds). Symbols represent mean values; error bars indicate the standard deviation. Semi transparent symbols denote individual device measurements used to calculate the mean, with colors matching the corresponding coating condition. Dotted lines are included as visual guides to aid interpretation and do not represent fitted models. Sample sizes were $N = 4$ devices for all conditions. Exceptions were SU-8 with KOH at 6 μ m, SiO₂ with KOH at 17 μ m, and SiO₂ at 6 μ m and 12 μ m, where $N = 3$.

3.5 Implications for μ LED Scaling and Device Design

The results in this chapter clarify that the efficiency degradation often observed as μ LEDs are laterally scaled is not an intrinsic consequence of shrinking device dimensions; it is primarily driven by process-induced surface recombination. When surface-related NRR is suppressed, scaling can instead reveal performance gains (e.g., enhanced light extraction) without the efficiency penalties typically associated with large S2V ratios.

A key outcome is the practical critical diameter, d_{crit} , which marks the transition between bulk-dominated and surface-dominated SRH NRR. For diameters $\gtrsim d_{crit}$, bulk SRH recombination dominates and additional sidewall passivation yields diminishing returns. For diameters $\lesssim d_{crit}$, surface recombination becomes the primary loss channel, making performance highly sensitive to sidewall processing and interface quality. Reducing d_{crit} is therefore a central fabrication objective, as it defines the size regime over which scaling can proceed without sacrificing efficiency.

The extracted d_{crit} values further show that conventional dielectric sidewall coatings (e.g., SiO_2) can drive surface-dominated recombination at diameters well above those required for high-resolution displays. Although such dielectrics may be optimized, ALD-deposited alternatives (e.g., Al_2O_3 or HfO_2) generally introduce added cost and process complexity. In contrast, polymeric encapsulation with SU-8 - particularly when combined with KOH sidewall treatment - is predicted by extrapolation of the fitted model to substantially reduce v_s and shift d_{crit} into the sub-micrometer regime. This effectively decouples performance from lateral geometry over the investigated size range, indicating that sidewall engineering (not epitaxial quality alone) sets the dominant scaling limit for top-down fabricated μ LEDs. In addition, SU-8 lowers barriers to adoption by avoiding expensive capital equipment and enabling faster materials/process iteration.

From a device-design perspective, these results highlight that electrical passivation must be co-optimized with optical extraction. Diameter-dependent gains in LEE (e.g., reduced TIR and shortened optical path lengths) become apparent only once surface-related non-radiative losses are sufficiently suppressed: in high- v_s regimes, optical improvements are masked by perimeter-related SRH recombination, whereas in low- v_s regimes reductions in diameter translate directly into higher WPE.

The ability of polymeric encapsulation to lower v_s also strengthens manufacturability. Polymeric materials such as SU-8 are compatible with low-temperature processing, back-end-of-line integration, and wafer-scale fabrication; their simultaneous provision of environmental encapsulation, electrical passivation, and optical benefits challenges the conventional reliance on inorganic dielectrics and offers a route to high-yield, dense arrays with

reduced process complexity.

At the system level, minimizing d_{crit} supports robust operation across a wide range of pixel sizes, improving pixel-to-pixel uniformity and relaxing constraints on pixel pitch. The reduced dependence of efficiency on device size also enables heterogeneous pixel architectures in which emitters of different dimensions coexist on the same backplane.

Finally, the recombination framework developed here is not specific to InGaN μ LEDs. The concepts of v_s , geometry-dependent SRH recombination, and a critical dimension separating bulk- and surface-dominated regimes are broadly applicable to other III-V emitters, nanostructured light sources, and emerging nano-optoelectronic devices. As dimensions continue to shrink, physically meaningful metrics such as v_s and d_{crit} will be increasingly valuable for linking fabrication processes to performance and guiding rational design and optimization.

3.6 Summary

This study examined the optoelectronic performance of InGaN μ LEDs under a range of sidewall coating and sidewall treatment conditions. A key finding is that a simple change in the sidewall coating material produces two qualitatively different efficiency-scaling behaviors as a function of μ LED size. Detailed electrical and optical characterization, combined with model fitting, enabled extraction of the dominant recombination parameters, including the surface recombination velocity v_s and the bulk SRH recombination coefficient A_0 .

A practical reference dimension, the critical diameter d_{crit} , was introduced and defined as the point at which surface-related and bulk SRH recombination contribute equally to the total NRR. μ LEDs with diameters larger than d_{crit} are therefore relatively insensitive to sidewall defects, whereas devices with diameters approaching or below d_{crit} are strongly influenced by surface recombination. Minimizing d_{crit} consequently emerges as a central objective in μ LED fabrication, as it enables second-order size-dependent effects, such as enhancements in LEE, to be exploited without incurring efficiency penalties.

Through effective sidewall engineering using optimized polymeric encapsulation with SU-8 and chemical sidewall treatment via KOH, 6 μ m-diameter μ LEDs achieved a mean peak WPE of 20.3 % at a current density of 2.5 A cm⁻², corresponding to an optical power density (OPD) of 1.4 W cm⁻². The same fabrication approach yielded d_{crit} values below 0.1 μ m and v_s below 10 cm s⁻¹ (extrapolated from the fitted model), underscoring its effectiveness in suppressing surface-related loss mechanisms. Table 3.2 summarizes the full set

of performance parameters for the highest-performing μ LED configuration demonstrated in this work.

Table 3.2: Performance parameters for the highest performance μ LED configuration with mean p-WPE = 20.3 %.

Parameter	Value
Sample size	3
Sidewall coating	SU-8
Treatment	KOH
μ LED diameter (μm)	6
μ LED area (μm^2)	30.4
Δr (μm)	1.7
p-contact area (μm^2)	6.1
Mean p-WPE (%)	20.3
Mean light output power at mean p-WPE (μW)	0.29
Mean light output power at 5 V (μW)	36.1
Mean voltage at mean p-WPE (V)	2.68
Mean current at mean p-WPE (μA)	0.76
Mean current density at mean p-WPE (A cm^{-2})	2.5
[Extracted] Mean minimum local IF	1.53
Mean reverse-bias current within -3 V to 0 V (fA)	< 30

Chapter 4

Enhancing the light extraction efficiency of perforated InGaN μ LEDs

4.1 Motivation & Scope

Once electrical injection and surface recombination are sufficiently controlled, light extraction becomes the dominant limiter of efficiency in scaled μ LEDs. As established in Chapter 1 and experimentally supported by the low- v_s regime developed in Chapter 3, suppressing perimeter SRH losses can render IQE comparatively size-insensitive, shifting the primary bottleneck in Equation 1.1 from IQE to LEE.[1, 31–33, 44, 45]

This shift motivates optical strategies that improve extraction without reintroducing recombination penalties. Here we investigate a perforated microLED (p- μ LED) architecture in which a periodic array of etched holes is introduced through the mesa and MQW region to create internal escape interfaces and increase LEE.[46] Although perforation increases sidewall area, it becomes viable when v_s is low enough that the added interfaces do not measurably degrade IQE, allowing geometry-enabled extraction gains to dominate - particularly for larger emitters that would otherwise be limited by optical confinement.

4.2 Device Fabrication

Blue InGaN-based μ LEDs were fabricated from commercially sourced epitaxial wafers on sapphire substrates. Devices employed Ni/Au/ITO-based p-type contacts optimized for

low contact resistance, followed by a two-step hard-mask mesa etch process to define either planar mesas or perforated geometries incorporating periodic arrays of etched holes extending through the active region. A combination of ICP etching, KOH-based removal of plasma-damaged sidewall material, crystallographic sidewall faceting, and dielectric processing was used to ensure well-defined mesa profiles and controlled surface quality. Both p- and n-type contacts were thermally annealed to achieve low specific contact resistivities.

To suppress surface recombination and planarize the device topography, an SU-8 overcoat was applied and patterned to expose contact vias. The resulting device set included planar circular μ LEDs spanning diameters from 5 to 500 μm , as well as perforated square μ LEDs with internal hole arrays of varying sizes, as illustrated in Appendix Figure B.1. Perforated devices employed 3 μm -diameter holes on a 5.6 μm pitch, with total hole counts ranging from 1 to 25.

Electrical and optical characterization was performed using combined IV and photodiode-based optical measurements. Devices were probed under controlled conditions while optical emission was collected through the sapphire substrate, enabling extraction of IV, IF, EQE, and WPE characteristics. Measurements were repeated across multiple devices to ensure statistical reliability, with J consistently calculated using the defined mesa area.

Additional fabrication and measurement details are provided in Appendix B, specifically Appendix B.1 and Appendix B.2.

4.3 Electrical and Optical Characteristics of perforated μ LEDs

Figure B.1 summarizes the two device architectures investigated in this work: a conventional planar μ LED and a perforated μ LED in which a periodic array of etched holes is introduced directly through the active region. The perforated structures were fabricated in several array sizes, ranging from a single central hole to a 5×5 -hole pattern, corresponding to side lengths from approximately 10 μm to 32 μm . All perforated devices used 3 μm -diameter holes on a 5.6 μm pitch, resulting in total hole counts of 1, 4, 9, 16, and 25. As shown in Table 4.1, increasing the number of holes systematically increases the internal sidewall area. Over the geometries investigated here, the absolute $S2V$ values span from 5357 cm^{-1} for a single-hole device to 4187 cm^{-1} for the 25-hole geometry, while the $S2V$ enhancement relative to an unperforated planar square increases monotonically with hole count.

Table 4.1: Geometric parameters and surface-to-volume ($S2V$) ratios for perforated square micro light-emitting diodes compared with equivalent planar square devices and equivalent circular devices.

Side Length (μm)	No. of Holes	$S2V$ (cm^{-1})	$S2V$ of Planar Square μLED (cm^{-1})	$S2V$ Ratio (Perforated / Planar)	Equivalent Circular μLED Diameter (μm)
9.7	1	5357	4124	1.30	7.47
15.5	4	4616	2581	1.79	8.66
21.0	9	4423	1905	2.32	9.04
26.8	16	4231	1493	2.83	9.45
32.3	25	4187	1238	3.38	9.55

Columns three and four of Table 4.1 compare each perforated device to a planar square μLED of the same lateral side length but without holes, highlighting how the addition of internal hole sidewalls increases the $S2V$ ratio. Because the planar comparison device has identical outer dimensions but lacks internal sidewalls, the two structures do not have the same net active area; as the μLED size increases, the perforated geometry exhibits an increasingly larger $S2V$ ratio than its planar square counterpart. To facilitate comparison with the actual devices fabricated in this work, the final column reports the equivalent $S2V$ ratio of a circular planar μLED with the same total active area as each perforated structure. This conversion is particularly useful because we fabricated circular planar μLEDs experimentally, allowing the perforated devices to be benchmarked directly against planar structures with comparable active-area scaling.

Figure 4.1 summarizes the electrical characteristics of the perforated μLEDs and their planar counterparts. Figure 4.1(a) compares the 1×1 perforated device to a $10 \mu\text{m}$ planar circular μLED possessing a similar net active area. The two devices show comparable forward-bias behavior, diverging only in the high-current regime where the perforated μLED exhibits a slightly larger series resistance. This increase is attributed to current-spreading limitations in the p-contact, whose lateral extent was restricted by lithographic alignment tolerances. Figure 4.1(b) shows the JV behavior for perforated devices ranging from a single-hole 1×1 array to a 5×5 array ($10 \mu\text{m}$ to $32 \mu\text{m}$ side length). All perforated structures exhibit nearly identical JV characteristics, with reverse-bias leakage currents below 10 fA at -3 V , indicating that the introduction of internal hole sidewalls does not measurably increase leakage. These measurements are particularly important because the perforated architecture intentionally increases the internal sidewall area. If the devices were not operating in the low- v_s regime established in Chapter 3, the additional sidewalls would be expected to increase SRH recombination and reduce efficiency.

Figure 4.1(c) shows the extracted IF as a function of applied voltage for perforated

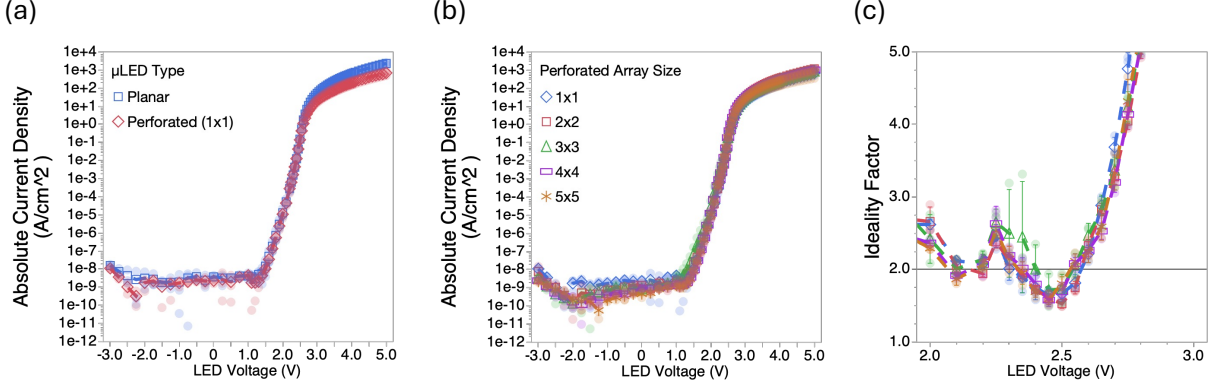


Figure 4.1: Electrical characteristics of planar and perforated InGaN μ LEDs. (a) Semi-logarithmic current density–voltage (JV) characteristics for a 10 μ m planar circular μ LED and a perforated μ LED containing a single internal hole (1×1 array), selected to have comparable net active areas. (b) Semi-logarithmic JV characteristics for perforated μ LEDs incorporating internal hole arrays of size 1×1 , 2×2 , 3×3 , 4×4 , and 5×5 , corresponding to device side lengths ranging from approximately 10 μ m to 32 μ m. (c) Ideality factor extracted as a function of applied voltage for the perforated μ LEDs shown in panels (a) and (b), evaluated over the forward-bias voltage range indicated. Symbols represent mean values and error bars denote one standard deviation. Semi-transparent symbols indicate individual device measurements. Sample sizes were $N = 3$ devices for both planar and 1×1 perforated μ LEDs in panel (a), and $N = 3$ devices for each perforated array size in panels (b) and (c).

μ LEDs containing internal hole arrays ranging from 1×1 to 5×5 . Across all perforation densities, the minimum IF remains between approximately 1.5 and 1.7, well below the $n \approx 2$ regime typically associated with dominant SRH recombination. Furthermore, no systematic increase in IF is observed as the number of perforations increases, despite the substantial increase in internal sidewall area and S2V ratio. At higher forward bias, a modest rise in IF is observed for all devices and is attributed to series-resistance effects associated with the current-spreading geometry.

Combined with the ultra-low reverse-bias leakage currents (< 10 fA at -3 V), these results indicate that the additional sidewalls introduced by the perforation process do not create significant electrically active defects. This observation confirms that the sidewalls remain well passivated and that the devices operate in a low- v_s regime where surface recombination does not significantly influence device performance.

The WPE characteristics of the devices are presented in Figure 4.2(a). The comparison between the 10 μm planar circular μLED and the perforated μLED containing a single internal hole demonstrates that both structures reach their peak WPE at nearly the same current density. The planar device peaks at approximately 5 A cm^{-2} , whereas the perforated device peaks at approximately 4 A cm^{-2} . This similarity suggests that the introduction of internal sidewalls does not significantly increase the SRH NRR. The perforated device also exhibits a slightly higher maximum WPE than the planar device, with approximate values of 29.6% for the perforated structure and 28.6% for the planar structure. This modest improvement is consistent with the expected increase in LEE produced by the additional optical escape interfaces within the perforated μLED .

Figure 4.2(b) highlights the peak-WPE trend for planar circular μLED s as a function of active area. Smaller devices achieve higher WPE values, which is a characteristic response of emitters operating in a low- v_s regime with well-passivated and minimally damaged sidewalls. The perforated devices achieve peak-WPE values that are comparable to or greater than those of planar μLED s with significantly smaller active areas. A perforated μLED with a side length of 32.3 μm and a 5×5 internal hole array reaches a WPE similar to that of a planar μLED with a diameter of 5 μm . This result shows that, once surface recombination is suppressed, the introduction of internal sidewalls enables large-area μLED s to approach the optical performance of much smaller emitters. The enhanced light-extraction pathways provided by the perforation pattern allow large devices to achieve efficiency levels that would normally only be accessible in the deeply sub-10 μm size regime.

4.4 FDTD Simulations

We evaluated the LEE of planar and perforated InGaN/GaN μLED s using Lumerical's three-dimensional finite-difference time-domain (FDTD) simulations based on the methodology of Ryu et al.[38] The modeled device stack included an Ag reflector, a p-GaN layer, a 50 nm-thick InGaN/GaN MQW region represented with an effective refractive index, and an n-GaN overlayer. To replicate typical epoxy encapsulation, the LED chip was embedded in a surrounding medium with a refractive index of 1.5. A single electric dipole emitter was placed at the center of the MQW plane and excited with a Gaussian spectrum centered at 450 nm (20 nm full width at half maximum (FWHM)). Only in-plane dipole orientations were simulated, consistent with the predominantly transverse electric emission of InGaN quantum wells.[38] For each dipole position, both X- and Y-polarized dipoles were simulated, and their results were averaged to obtain a polarization-independent LEE. A schematic of the simulated structure is shown in Figure 4.3(a). More details on the

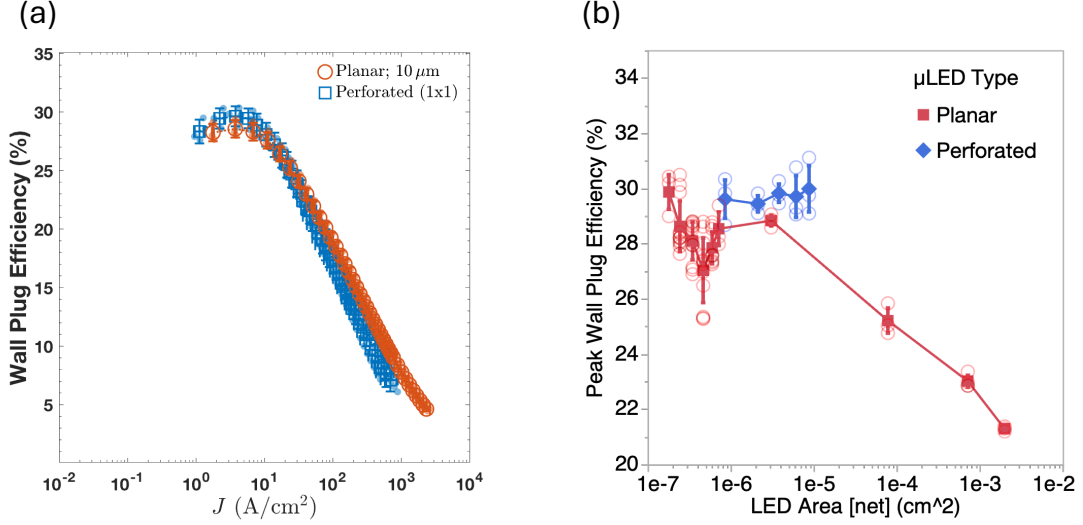


Figure 4.2: Optical efficiency characteristics of planar and perforated InGaN μ LEDs. (a) Wall-plug efficiency (WPE) plotted as a function of current density J for planar and perforated μ LEDs corresponding to the devices characterized electrically in Figure 4.1(a). Data are shown for planar circular μ LEDs and perforated μ LEDs containing a single internal hole (1×1 array). Sample sizes were $N = 3$ devices for both planar and perforated μ LEDs. (b) Peak wall-plug efficiency (p-WPE) plotted as a function of net LED active area for planar and perforated μ LEDs. For planar devices, the data points correspond (from left to right) to circular μ LED diameters of 5, 6, 7, 8, 9, 10, 20, 100, 300, and 500 μm , with sample sizes of $N = 3, 12, 12, 12, 9, 3, 3, 3, 3$, and 3, respectively. For perforated devices, the data points correspond (from left to right) to internal hole arrays ranging from 1×1 to 5×5 , with $N = 3$ devices measured for each perforation geometry. Symbols represent mean values; error bars indicate one standard deviation; and semi-transparent symbols denote individual device measurements.

FDTD methodology and simulation parameters are provided in Appendix B, specifically Appendix B.3.

Figure 4.3(b) compares the spatially averaged LEE for planar and perforated μ LEDs as a function of device size. Perforated devices consistently outperform their planar counterparts. For small μ LEDs ($10\ \mu\text{m}$), perforation yields approximately a $1.07\times$ boost in LEE. For the $20\ \mu\text{m}$ devices, the enhancement increases to $1.16\times$, demonstrating that the internal sidewalls remain effective even when the device volume increases substantially.

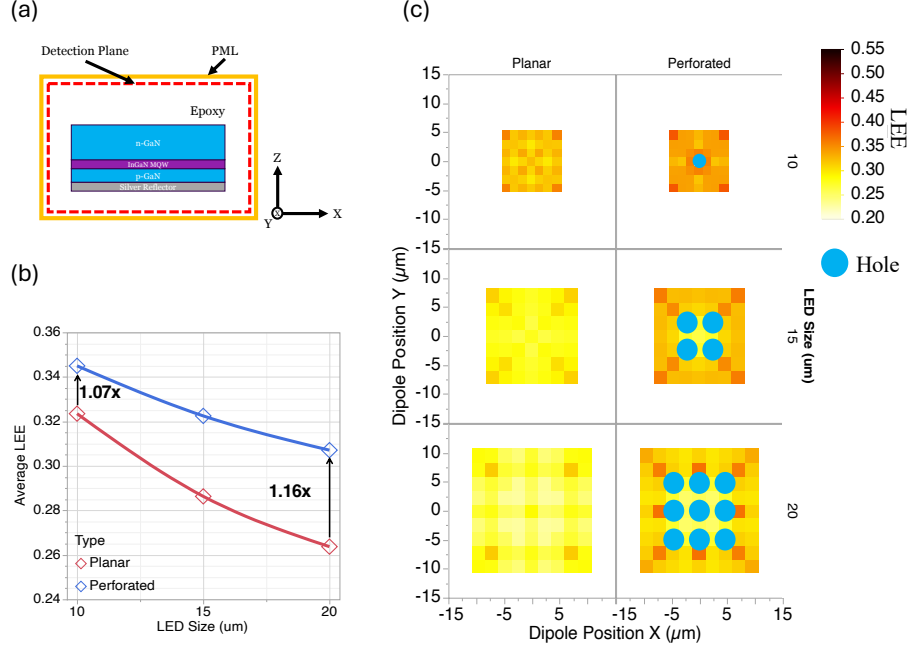


Figure 4.3: Finite-difference time-domain (FDTD) simulation results for planar and perforated InGaN μ LEDs. (a) Schematic of the simulated device structure and FDTD simulation domain, showing the layered InGaN/GaN LED stack embedded in an epoxy medium, the detection plane used for power collection, and the perfectly matched layer (PML) boundaries. A single electric dipole source is placed within the multiple-quantum-well (MQW) plane. (b) Spatially averaged light extraction efficiency (LEE) obtained from FDTD simulations for planar and perforated μ LEDs as a function of lateral device size (10, 15, and 20 μ m). For each device size, results are averaged over multiple in-plane dipole positions and polarizations as described in Appendix B.3. (c) Two-dimensional maps of local LEE as a function of dipole position within the MQW plane for planar and perforated μ LEDs with lateral sizes of 10, 15, and 20 μ m. Perforated devices incorporate cylindrical air holes arranged as 1×1 , 2×2 , and 3×3 arrays for the 10, 15, and 20 μ m devices, respectively. The color scale indicates the local LEE, and blue circles denote the locations of the etched holes.

Figure 4.3(c) shows the spatial LEE distributions across the μ LED surface for both planar and perforated devices. In planar structures, LEE is lowest near the device center and increases toward the edges due to strong lateral confinement and limited escape pathways. In contrast, perforated μ LEDs exhibit a more uniform and noticeably enhanced

LEE distribution. The introduction of internal vertical sidewalls (epoxy–hole boundaries) provides additional scattering and extraction interfaces, enabling lateral optical modes to couple more efficiently into the escape cone. Figure 4.3(c) also shows the corresponding LEE maps, indicating where perforations produce the greatest local improvement. These enhancements coincide with regions where planar devices typically accumulate the strongest guided-mode intensity, confirming that the perforations effectively break lateral confinement.

Figure 4.4(a) shows the simulated far-field emission patterns for planar and perforated μ LEDs. The far-field intensity at 450 nm was obtained using Lumerical’s three-dimensional far-field projection and incoherently summed over all dipole positions and both in-plane polarizations. The two devices exhibit similar angular distributions and symmetry, indicating that internal perforations do not strongly modify the far-field radiation profile. Perforation therefore primarily increases the extracted power (Figure 4.3(a–c)) while preserving the overall emission pattern.

Figure 4.4(b) summarizes a design-of-experiments sweep used to identify promising perforation geometries. The perforation pitch p and fill factor FF were varied over wide ranges ($0.5\,\mu\text{m}$ to $3.5\,\mu\text{m}$ and 0.3 – 0.7 , respectively), corresponding to hole diameters $D = FF \times p$ and edge-to-edge spacing $S = p - D$ (with pitch p also being the center-to-center spacing).

The heatmap displays the simulated LEE for each parameter combination, obtained using a single X-polarized dipole placed at the device center. This simplified excitation accelerates the DOE while still capturing relative performance trends across the design space. The coarse sweep narrowed the feasible parameter space to $p \approx 1.9\,\mu\text{m}$ to $2.5\,\mu\text{m}$ and $FF \approx 0.6$ – 0.8 , which was then targeted in a higher-resolution local search (Figure 4.4(c)). The refinement identified an improved geometry with $p = 2.4\,\mu\text{m}$ and $FF = 0.75$, corresponding to a hole diameter of $1.8\,\mu\text{m}$ (radius $0.9\,\mu\text{m}$) and an edge-to-edge spacing of $0.6\,\mu\text{m}$. This was implemented as a 4×4 array within a $10\,\mu\text{m}$ mesa and selected for full dipole-sweep analysis.

Figure 4.4(d) shows the LEE map for the optimized geometry, obtained from a 7×7 dipole sweep simulated over a single quadrant and extended using symmetry to yield an effective 13×13 dipole grid across the $10\,\mu\text{m}$ mesa. This optimized design exhibits a substantially more uniform and elevated extraction profile compared with both the planar LED and the initial perforated structure shown earlier in Figure 4.3(c). The initial perforated geometry in Figure 4.3(c) reflects the hole dimensions achievable experimentally given fabrication toolset constraints, whereas the optimized design in Figure 4.4(d) results from the DOE-guided refinement. The spatially averaged LEE increases to 0.45 ,

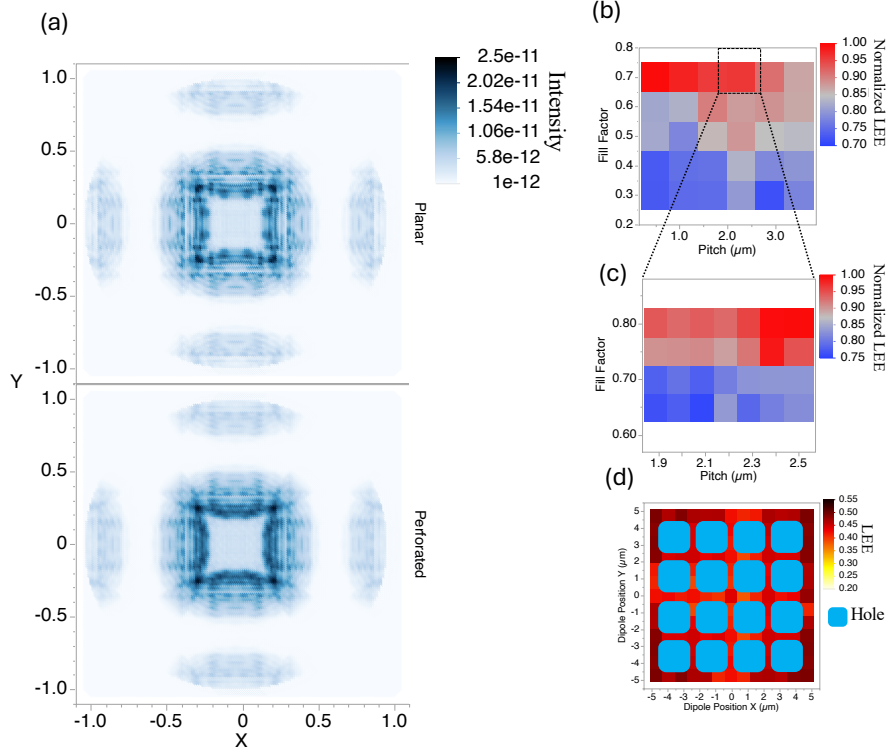


Figure 4.4: FDTD simulation results for planar and perforated InGaN μ LEDs. (a) Simulated far-field radiation intensity distributions for planar (top) and perforated (bottom) μ LEDs, obtained using near-to-far-field projection of the electromagnetic fields recorded above the device. (b) Coarse design-of-experiments (DOE) heatmap showing normalized spatially averaged light extraction efficiency (LEE) as a function of perforation pitch and fill factor, evaluated using a single in-plane dipole positioned at the device center. The dashed region indicates the parameter space selected for refinement. (c) Refined DOE heatmap within the highlighted region of panel (b), calculated using smaller pitch and fill-factor step sizes. (d) Two-dimensional map of local LEE as a function of dipole position for the optimized perforated μ LED geometry identified from the DOE sweep. The color scale denotes local LEE, and blue circles indicate the locations of the etched air holes. Simulation setup, dipole sampling strategy, normalization procedure, far-field projection, and DOE methodology are described in Appendix B.3.

corresponding to a $1.37\times$ improvement relative to the planar LED ($\text{LEE} = 0.32$) and a $1.30\times$ improvement over the original perforated geometry ($\text{LEE} = 0.35$). This suggests

that targeted DOE-based refinement of the perforation parameters may be an effective strategy for further boosting extraction efficiency in μ LEDs.

4.5 Summary

From the FDTD simulations shown in Figure 4.3 and Figure 4.4, perforation-induced internal sidewalls consistently enhance LEE across all simulated μ LEDs sizes, with larger emitters benefiting the most. Smaller devices already couple out efficiently and therefore show only an approximately $1.07\times$ improvement, whereas the simulated $20\mu\text{m}$ structure exhibits a stronger $1.16\times$ enhancement, indicating that, within the modeled parameter space, larger μ LEDs gain disproportionate advantages from the added internal extraction interfaces. A two-stage design-of-experiments procedure further refined the perforation geometry, converging on a compact $2.4\mu\text{m}$ -pitch, $0.9\mu\text{m}$ -radius, 4×4 -hole array that increases the dipole-averaged LEE to 0.45, yielding a $1.37\times$ improvement over the planar device and a $1.30\times$ gain relative to the initial fabricated perforated design. Together, these results show that carefully engineered internal sidewalls provide a scalable and effective pathway for restoring high-extraction performance in larger-area μ LEDs.

The experimental results corroborate the central trends predicted by simulation. As summarized in Table 4.1, perforated μ LEDs exhibit steadily increasing S2V ratios compared with planar square structures of the same outer dimensions, with S2V enhancements ranging from $1.30\times$ to $3.38\times$ as device size and hole count grow. Despite this substantial increase in internal sidewall area, the electrical characteristics show that all perforated devices maintain ultralow leakage currents (below 10 fA at -3 V) and forward-bias behavior closely matching planar circular μ LEDs, confirming that the additional sidewalls do not introduce measurable SRH-related recombination. Optical measurements further reveal that the perforated μ LEDs achieve peak WPE values comparable to, or slightly higher than, their circular planar counterparts, and that large perforated devices can reach WPE levels normally attainable only in planar emitters nearly an order of magnitude smaller.

Taken together, the simulation, DOE-driven optimization, and experimental validation demonstrate that once surface recombination is effectively suppressed, the strategic introduction and refinement of internal sidewalls provide a robust and scalable route for enhancing extraction in large-area μ LEDs. This approach enables large emitters to recover efficiency levels traditionally restricted to miniaturized devices, offering a practical pathway toward high-brightness, large-format μ LED architectures. In the context of the WPE framework introduced in Chapter 1, these results demonstrate that once IQE losses

associated with sidewall recombination are suppressed, deliberate introduction of internal sidewalls can be used to enhance LEE and further increase overall device efficiency.

Chapter 5

High Efficiency InGaN μ LEDs on flexible substrates

5.1 Motivation & Scope

Chapters 2–4 established a framework for the realization of high-performance InGaN μ LEDs through the systematic optimization of the primary factors governing WPE. Electrical injection losses were minimized through optimized ohmic contacts, sidewall-mediated NRR was suppressed through passivation and surface treatments, and LEE was enhanced through geometry-driven optical design. Collectively, these efforts established high-efficiency μ LEDs on rigid sapphire substrates. However, despite these advances, device performance remains constrained by the substrate itself, which not only prevents integration into mechanically compliant systems but also defines the optical environment of the device. This chapter addresses that final constraint.

Flexible integration enables new form factors (e.g., curved or wearable displays and biophotonic platforms) that require mechanically compliant, stable light sources.[4, 9, 47, 48] However, the high thermal budgets required for III-nitride growth and processing are incompatible with most polymer substrates, making direct fabrication on flexible platforms challenging. Transfer-based integration therefore decouples high-temperature device fabrication from the final form factor and, through substrate removal, can also enable additional backside optical engineering.[9]

In this work, we demonstrate a scalable photonic double-transfer technique, referred to as the PulseForge assisted transfer process (PATP), for the integration of InGaN μ LEDs

onto flexible PEN.[49, 50] This approach enables the transfer of fully fabricated and optimized devices while preserving their electrical and optical characteristics. Following an initial transfer to a glass carrier, backside surface texturing is introduced to enhance LEE, after which the optimized μ LEDs are transferred onto flexible substrates. Electrical, optical, and mechanical properties are systematically evaluated throughout the process to distinguish changes in IQE from improvements in LEE. The resulting devices exhibit high efficiency, robust mechanical performance, and enhanced optical extraction, demonstrating that transfer-based integration can function as both an enabling technology for flexible systems and a final stage of device optimization.

5.2 Device Fabrication

InGaN μ LEDs were fabricated on double-side-polished sapphire substrates and characterized on sapphire and after transfer to the final substrate. A transparent p-type ITO contact was first deposited and patterned prior to mesa definition. Lateral μ LED mesas were then formed using standard photolithography and chlorine-based ICP-RIE etching, followed by a second, deeper mesa etch. After completion of both mesa etches, n-type ohmic contacts were deposited. Device sidewalls were passivated and the surface was planarized using an SU-8 overcoat.[24–26, 51] Circular μ LEDs with diameters ranging from $5\mu\text{m}$ to $100\mu\text{m}$ were fabricated. Full fabrication details are provided in Appendix C.1.

The optoelectronic performance of the fabricated μ LEDs was evaluated using simultaneous electrical probing (semiconductor parameter analyzer) and photodiode-based optical power collection in a light-tight Faraday-cage setup (see Appendix C.3 for experimental details). From the measured JV characteristics and optical power, EQE and WPE were extracted using the definitions introduced in Chapter 1 (Equation 1.1). To gain insight into the electrical transport and recombination mechanisms, the diode IF was extracted from the forward-bias JV characteristics. The IF was obtained by fitting the data in the 2–3V range using the non-ideal diode equation

$$J = J_0 e^{\frac{qV_{\text{app}}}{nkT}} \quad (5.1)$$

where J_0 is the saturation current density, n is the IF, and $kT/q \approx 25.6\text{meV}$ at room temperature. The IF provides sensitivity to recombination mechanisms that are not readily apparent from linear or semi-logarithmic JV plots alone. In an ideal diode dominated by radiative recombination, $n = 1$, whereas $n = 2$ indicates SRH recombination via mid-gap defect states. In practical GaN-based μ LEDs, values of $n > 2$ are commonly observed due

to parasitic effects such as R_s , R_{sh} , or additional parasitic conduction paths associated with surface states or defects in the MQW active region. Consequently, meaningful IF extraction is typically confined to the sub-turn-on regime, where these parasitic contributions are minimized.

5.3 Performance on Sapphire

Figure 5.1 summarizes the optoelectronic characteristics of $10\mu\text{m}$ -diameter μLEDs fabricated on sapphire, based on measurements from $N = 5$ devices. Figure 5.1(a) shows the mean JV characteristics over the full bias range. The reverse-bias leakage current remains below 100fA at -3V , indicating high diode isolation and low parasitic leakage. Under forward bias, measurable current onset occurs near 1.5V , with minimal device-to-device variation.

The extracted IF as a function of applied voltage is shown in Figure 5.1(b). A clear minimum IF of 1.54 is observed in the sub-turn-on regime, reflecting a bias region where carrier transport is least affected by parasitic resistive or leakage pathways. At lower forward biases, elevated IF values are attributed to parallel leakage or parasitic conduction paths, while at higher biases the IF increases sharply as R_s begins to dominate, reducing the slope of the semi-logarithmic JV curve. Figure 5.1(c) presents the WPE as a function of J . The $10\mu\text{m}$ μLEDs exhibit a mean p-WPE of 28.3% at a current density (J_{peak}) of 3.7Acm^{-2} . The combination of low reverse leakage, low minimum IF, and high peak WPE demonstrates strong electrical integrity and efficient power conversion for μLEDs fabricated on sapphire in this study.

5.4 Performance on Flexible PEN

Having established the strong electrical integrity and high efficiency of μLEDs fabricated on sapphire, these devices were subsequently used as the starting point for integration onto flexible substrates. The transfer strategy, schematically illustrated in Figure 5.2, decouples device fabrication from final substrate integration, enabling intermediate optical optimization while preserving electrical performance. In brief, fully processed μLED chips are first bonded to a glass carrier that contains a light absorbing layer (LAL), followed by laser lift off (LLO) of the sapphire growth substrate to expose the GaN epilayer. After optional backside surface treatment, the optimized devices are transferred onto flexible PEN substrates using the PATP. This multi-step approach enables scalable, wafer-scale

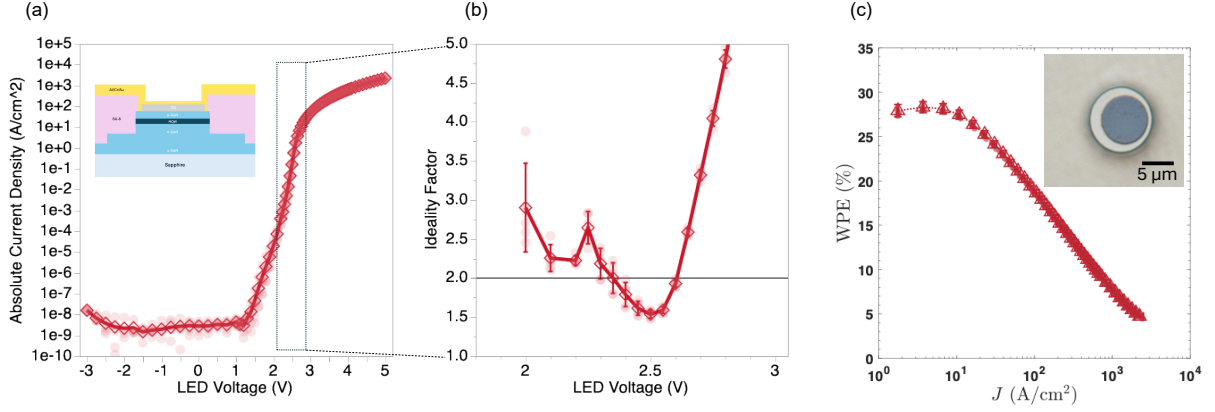


Figure 5.1: Optoelectronic characteristics of 10 μm -diameter μLEDs fabricated on sapphire. (a) Mean current density–voltage (J – V) characteristics over the full bias range measured. Inset shows cross-sectional schematic of the μLED . (b) Ideality factor extracted as a function of applied voltage for the μLEDs shown in panels (a), evaluated over the forward-bias voltage range indicated. (c) Wall-plug efficiency as a function of current density, with an inset showing a microscope image of a 10 μm μLED with the p-contact indicated by the blue material. Sample sizes were $N = 5$ devices for all measurements. Symbols represent mean values and error bars denote one standard deviation. Semi-transparent symbols indicate individual device measurements.

integration of high-performance μLEDs onto flexible platforms; full experimental details are provided in Appendix C.2.

To evaluate the impact of the transfer process on the crystalline quality of the μLED GaN epilayer, structural characterization was performed at key stages of the transfer sequence using X-ray diffraction (XRD) and X-Ray rocking curves (XRCs). The crystalline quality was assessed through changes in the FWHM of the GaN diffraction peaks. Measurements were first conducted on the as-fabricated μLEDs on sapphire, followed by characterization after LLO, where the released GaN film remained bonded to the glass carrier through the LAL. A final set of measurements was obtained after the second bonding step and PulseForge-assisted transfer. To isolate the effects of the transfer process and eliminate additional variables associated with flexible substrates, these measurements were performed on samples transferred onto a rigid silicon substrate. The resulting XRCs and extracted FWHM values are summarized in Figure 5.3.

Figure 5.3 shows the normalized GaN (002) XRCs measured on the as-grown sapphire wafer, following LLO, and after PulseForge-assisted transfer onto silicon. The extracted

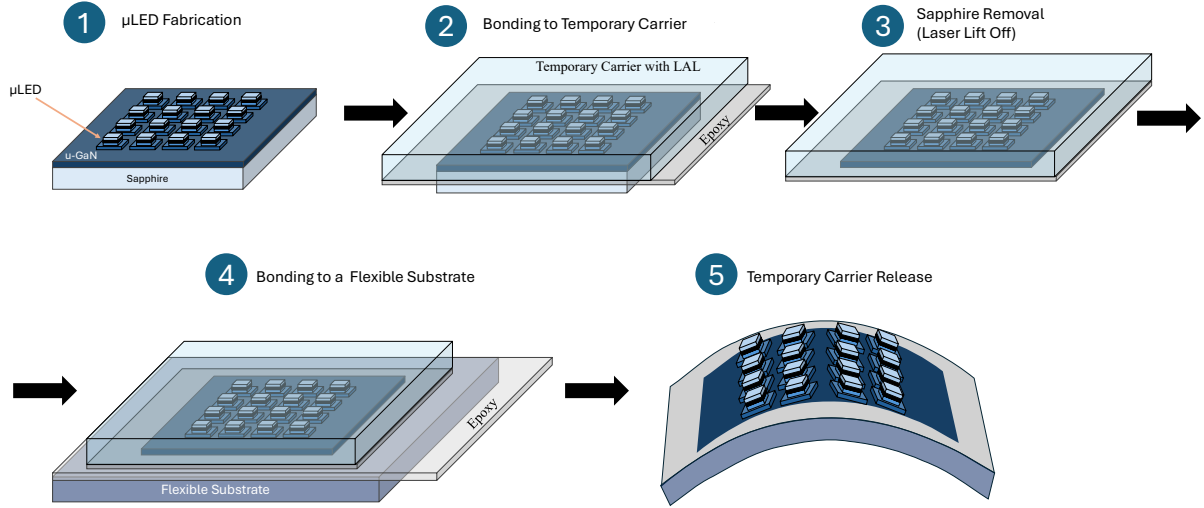


Figure 5.2: Schematic illustration of the μ LED transfer process. (1) μ LED fabrication on sapphire substrates. (2) Bonding of fully processed μ LEDs to a temporary carrier containing a light absorbing layer (LAL). (3) Removal of the sapphire substrate by laser lift-off (LLO) to expose the GaN epilayer. (4) Bonding of the μ LEDs onto a flexible substrate. (5) Release of the temporary carrier to complete integration onto the flexible platform.

FWHM increases from 0.0854° for the as-grown sample to 0.1016° following LLO, while remaining nearly unchanged after transfer to silicon (0.1008°). The observed broadening therefore originates primarily from the LLO process, likely due to strain relaxation within the GaN epilayer following removal of the sapphire substrate. In contrast, the subsequent transfer process does not introduce measurable additional degradation in crystalline quality, indicating that the structural integrity of the epilayer is largely preserved during transfer.

Figure 5.4 summarizes the electrical and optoelectronic characteristics of $10\text{ }\mu\text{m}$ -diameter μ LEDs following transfer, comparing devices on sapphire ($N = 5$) to devices transferred onto flexible PEN substrates ($N = 3$). Figure 5.4(a) shows the mean JV characteristics. Under reverse bias, both substrates exhibit leakage currents below 100 fA at -3 V (near the measurement noise floor). The modest increase in apparent reverse-bias leakage observed for some PEN devices could reflect process-induced degradation from the post-PATP epoxy removal (O_2/CF_4 plasma etch; Appendix C.2), but it is also consistent with measurement noise and day-to-day environmental variation; repeated measurements show comparable leakage across both substrates, indicating preserved diode isolation after transfer.

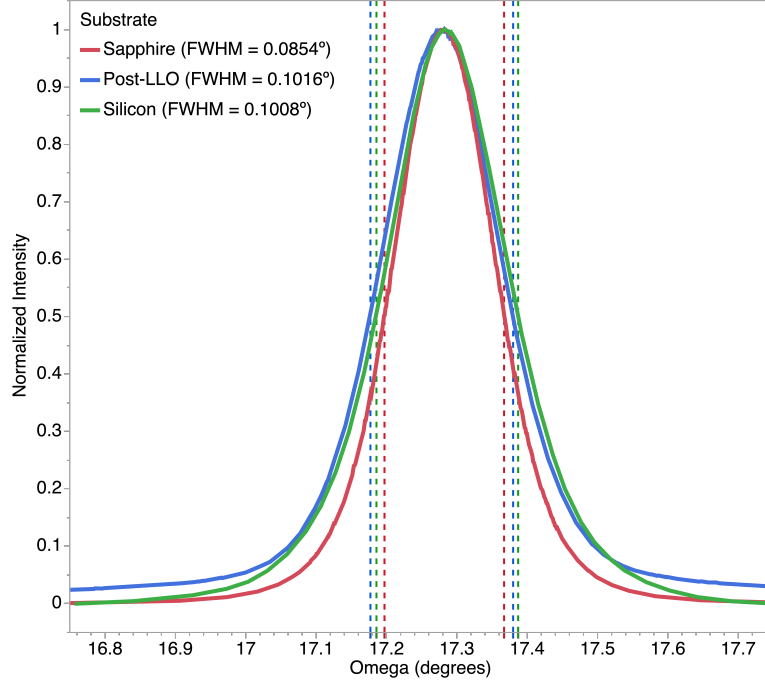


Figure 5.3: Normalized GaN (002) x-ray rocking curves measured for μ LED samples on the native sapphire substrate, immediately following laser lift-off (LLO), and after PATP transfer onto a silicon carrier substrate. The full-width at half-maximum (FWHM) values were extracted from each rocking curve to evaluate changes in crystal quality during the transfer process.

In forward bias, PEN-based devices closely match sapphire controls in turn-on and high-current slope, with no evidence of added series resistance or contact degradation. As discussed below, the extracted IF (Figure 5.4(b)) likewise remains unchanged, supporting the conclusion that any reverse-leakage increase is minor and not substrate-dependent.

The extracted IF as a function of applied voltage is shown in Figure 5.4(b). Both sapphire and PEN devices exhibit nearly identical IF trends across the bias range, including a well-defined minimum in the sub-turn-on regime. The PEN devices show a mean minimum IF of 1.43, compared to 1.54 for sapphire-based devices; however, this difference lies within the standard deviation of the measurements and is therefore not statistically significant. In addition, PEN devices exhibit slightly lower IF for $V_{\text{LED}} < 2.5$ V, suggesting that the observed reverse-bias leakage increase is dominated by measurement artifacts and/or only minor plasma-induced damage.

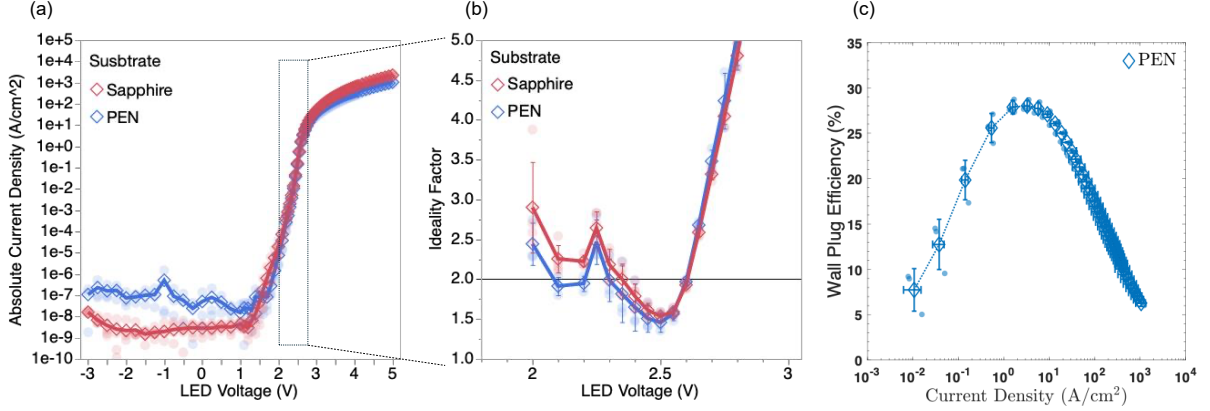


Figure 5.4: Electrical and optoelectronic characteristics of 10 μm -diameter μLEDs comparing devices on sapphire ($N = 5$) and devices transferred onto PEN ($N = 3$): (a) mean J-V characteristics in reverse- and forward-bias regimes, (b) extracted ideality factor versus LED voltage, and (c) wall plug efficiency as a function of current density.

Optoelectronic performance is summarized in Figure 5.4(c), which shows the WPE vs J for 10 μm μLEDs on PEN. A mean peak WPE of 28.0 % is achieved at a J_{peak} of 3.3 A cm^{-2} , closely matching the peak efficiency observed for devices on sapphire (Figure 5.1(c)). The small difference in peak efficiency falls within experimental uncertainty and is not deemed statistically significant. Overall, the electrical and optoelectronic results demonstrate that transfer onto flexible PEN substrates preserves the intrinsic device performance, confirming that the transfer process does not adversely affect the electrical and optical properties of the high performance μLEDs .

In conventional sapphire-based μLED architectures, a bottom-emitting configuration is already advantageous, as photons emitted toward the top surface can be redirected downward using reflective contacts, enabling light extraction primarily through the transparent sapphire substrate. The PATP preserves this favorable emission geometry while enabling transfer onto a final transparent substrate of choice, here a flexible PEN film. The PATP flow incorporates a double-transfer sequence with an intermediate rigid carrier, during which the n-polar GaN backside is exposed following LLO. This intermediate handling step provides direct access to the GaN backside for additional processing prior to final transfer. Importantly, the use of a rigid glass carrier during this stage allows for backside treatments or layer integrations that may be impractical on a flexible substrate. In this work, the exposed n-polar GaN surface is subjected to a KOH-based wet etch to introduce controlled surface roughening, providing a pathway to enhance LEE by reducing total

internal reflection (TIR) and promoting optical scattering. As with the electrical results discussed above, any optical benefits enabled by this approach arise from transfer-enabled backside engineering rather than from the flexible substrate itself.

Figure 5.5 summarizes the structural, electrical, and optoelectronic implications of transfer-enabled backside processing enabled by the PATP. A cross-sectional schematic of the final device configuration on a flexible substrate is shown in Figure 5.5(a), illustrating a bottom-emitting μ LED architecture in which light is extracted through the transparent PEN substrate. Consistent with conventional sapphire-based designs, this emission geometry allows photons initially emitted toward the top surface to be redirected downward using reflective contacts, while additionally enabling optical engineering of the GaN backside following transfer.

A key feature of the PATP flow is the intermediate rigid-carrier step introduced after LLO, during which the n-polar GaN backside is exposed and mechanically supported by a glass carrier. This configuration provides direct access to the GaN backside for post-growth processing prior to final transfer onto the flexible substrate. Figure 5.5(b) and Figure 5.5(c) present scanning electron microscopy (SEM) images of the GaN backside following LLO and hydrochloric-acid-based Ga residue removal, without and with subsequent KOH treatment, respectively. The untreated backside (Figure 5.5(b)) remains relatively planar and serves as a reference, while the KOH-treated surface (Figure 5.5(c)) exhibits pronounced nanoscale roughening, consistent with the known anisotropic etching behavior of n-polar GaN.[52, 53] The inset optical micrograph in Figure 5.5(b) and Figure 5.5(c), acquired through the backside GaN, further highlights the optical roughness of the planar reference compared to the textured devices.

To assess whether backside chemical processing impacts device integrity, the electrical characteristics of μ LEDs subjected to backside KOH treatment were evaluated after completing the full PATP flow. Figure 5.5(d) shows the IF as a function of voltage for 10 μ m μ LEDs on PEN with backside KOH treatment ($N = 6$). The mean minimum IF is approximately 1.5, closely matching that of μ LEDs on sapphire and PEN without KOH treatment (Figure 5.4(b)). The observed differences lie within the standard deviation of the measurements and are therefore not statistically significant, indicating that backside KOH processing does not measurably alter the dominant recombination mechanisms or degrade electrical performance. This result further supports that the PATP flow, including backside chemical treatment, preserves the intrinsic electrical properties of the devices.

In contrast, a clear improvement is observed in the optoelectronic efficiency. Figure 5.5(e) compares the peak WPE of 10 μ m μ LEDs across different substrates and backside treatments. Devices on sapphire and PEN without backside texturing exhibit nearly

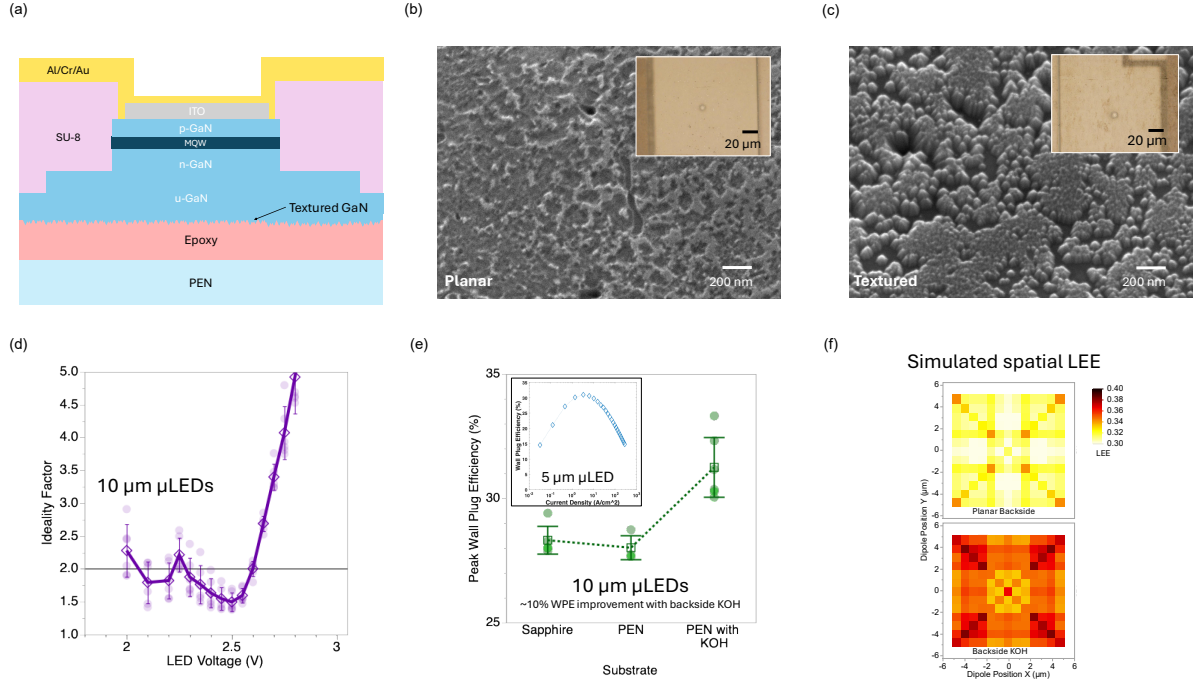


Figure 5.5: Backside KOH treatment and its impact on device structure and performance. (a) Cross-sectional schematic of the μ LED device structure incorporating backside KOH-induced GaN texturing. (b) SEM image of the planar backside GaN surface following LLO and HCl-based Ga residue removal; the inset shows an optical micrograph of the same region. (c) SEM image corresponding to (b) after KOH treatment, showing the formation of a textured backside surface; the inset shows the corresponding optical micrograph. (d) Ideality factor as a function of bias for 10 μ m μ LEDs ($N = 6$); purple diamond markers indicate mean values, semi-transparent circular markers represent individual measurements, and the solid line is included to guide the eye. (e) Peak WPE for each substrate condition; green square markers indicate mean values, semi-transparent circular markers represent individual devices, and the solid line is included to guide the eye; sapphire ($N = 5$), PEN ($N = 3$), and PEN with backside KOH ($N = 6$); the inset shows WPE as a function of current density for a 5 μ m μ LED with backside KOH, exhibiting a peak WPE of 31% at 3.3 A cm^{-2} . (f) Simulated FDTD spatial LEE maps for a 10 μ m μ LED with a planar backside (top, no KOH) and a textured backside (bottom, with KOH treatment).

identical peak WPE values of approximately 28%, consistent with the electrical and optoelectronic equivalence discussed previously. However, μ LEDs on PEN with KOH-textured

back surfaces show a higher peak WPE of $\sim 31.2\%$, corresponding to an improvement of roughly 10% relative to the planar reference devices. The inset of Figure 5.5(e) shows the WPE versus J for a $5\text{ }\mu\text{m}$ μLED on PEN with backside KOH treatment, which reaches a peak WPE of $\sim 31\%$ at a J_{peak} of 3.3 A cm^{-2} , demonstrating that the efficiency enhancement persists at smaller device dimensions. This peak efficiency is competitive with leading reports of flexible InGaN μLEDs . [4, 9, 47, 48, 54–56]

Importantly, the absence of any measurable change in IF (Figure 5.5(d)) suggests that the IQE remains largely unchanged by the backside KOH treatment. The observed increase in WPE therefore cannot be attributed to modified electrical injection or recombination dynamics. Instead, the improvement is most consistently explained by enhanced LEE, arising from backside surface roughening that reduces total internal reflection (TIR) and redistributes guided optical modes into escape cones. [1, 57] To further substantiate this interpretation, the role of backside texturing on LEE is examined using two complementary approaches: (FDTD) optical simulations (Figure 5.5(f)) and size-dependent efficiency modeling based on recombination-parameter extraction, as discussed in the following.

Three-dimensional FDTD simulations were performed to evaluate how backside surface roughening influences optical extraction in $10\text{ }\mu\text{m}$ μLEDs , with full simulation details provided in Appendix C.7. In these simulations, spontaneous emission was modeled using spectrally weighted dipole sources distributed across the active region, and the extracted optical power was normalized to the analytically computed dipole injection power to obtain the LEE.

Figure 5.5(f) presents a spatial map of the LEE across the $10\text{ }\mu\text{m}$ LED active area. Each pixel in the heatmap corresponds to the LEE at a given dipole position and represents the average of the two in-plane dipole polarizations, namely x - and y -polarized emission. The planar reference exhibits a spatially averaged LEE of approximately 0.31 across all simulated source locations, whereas the backside-roughened configuration shows a higher spatially averaged value of approximately 0.35. This increase is observed consistently across the device area, indicating that backside roughening enhances optical extraction broadly rather than at isolated locations.

The simulated enhancement in LEE occurs without any accompanying change in electrical characteristics or recombination behavior, as evidenced by the unchanged IF following backside processing (Figure 5.5(d)). This supports the conclusion that the experimentally observed increase in WPE after backside roughening (Figure 5.5(e)) originates from improved optical outcoupling rather than changes in IQE. Further verification of the enhanced LEE is obtained through size-dependent efficiency fitting based on recombination-parameter extraction, which is discussed directly below.

To further validate that the observed efficiency enhancement after backside processing originates from increased LEE rather than changes in recombination dynamics, we fitted a diameter-dependent EQE model (Equation 5.2) to the 10 μm μLED experimental data using a nonlinear optimization loop implemented in custom MATLAB code, enabling extraction of efficiency-related parameters such as v_s and size-independent LEE terms. Further details of the fitting procedure, model implementation, and its application to GaN μLEDs efficiency analysis are provided in our previously published work and are therefore not repeated here.[45, 50, 51] The MATLAB code used to implement the global fitting procedure, together with example input data, has been made publicly available through Figshare.[42]

$$\begin{aligned} EQE(d, n) &= LEE(d) \times IQE(d, n) \\ &= [LEE_\infty + \alpha d^{-\beta}] \times \text{IE} \times \frac{Bn^2}{(A_0 + \frac{4v_s}{d})n + Bn^2 + C_{\text{aug}}n^3 + C_{\text{dl}}n^3 + D_{\text{dl}}n^4} \end{aligned} \quad (5.2)$$

In this formulation, a size dependent LEE is modeled where LEE_∞ represents the baseline extraction efficiency for an infinitely large device, and α and β describe the geometric influence on optical outcoupling. IQE is expressed through the product of injection efficiency (IE) and a recombination-based model that includes SRH, radiative, Auger, and carrier overflow processes, characterized by the coefficients A_0 for SRH recombination, B for radiative recombination, C_{aug} for Auger recombination, and C_{dl} and D_{dl} for carrier overflow and leakage effects. The v_s enters only through the SRH term and is independent of LEE, ensuring that optical extraction and recombination dynamics are treated as separate parameters. This separation allows accurate interpretation of efficiency improvements after transfer, where changes in EQE or WPE can be attributed primarily to enhanced LEE rather than variations in SRH-related NRR.[45, 50, 51]

Fitting results from Equation 5.2 reveal opposing trends in the extracted optical and recombination parameters when comparing μLEDs on sapphire and PEN substrates (Table 5.1). Upon transfer from sapphire to PEN, the fitted LEE_∞ increases from 0.29 to 0.34, which would be expected to enhance EQE and WPE through improved optical outcoupling. At the same time, the extracted v_s increases from approximately 50 cm s^{-1} to 96 cm s^{-1} , which would tend to reduce efficiency by increasing NRR losses; this increase in v_s may in part reflect mild process-induced degradation during the post-PATP epoxy removal (O_2/CF_4 plasma etch; Appendix C.2). These opposing effects are therefore expected to partially counterbalance one another. We speculate that this compensation provides a plausible explanation for the nearly identical WPE versus J characteristics observed earlier

for sapphire and PEN devices (Figure 5.5(e)), where no statistically significant difference in peak efficiency was measured.

Importantly, despite the increase observed upon transfer, the extracted v_s remains below 100 cm s^{-1} for all substrate conditions, which is notably low compared to values typically reported for InGaN-based μLEDs .^[5] This suggests that sidewall-mediated NRR is not a dominant loss mechanism in these devices and helps explain the overall high efficiency maintained after transfer.

A different trend is observed when comparing PEN devices with and without backside KOH treatment. In this case, the extracted v_s remains essentially unchanged, while LEE_∞ increases substantially from 0.34 to 0.42. The absence of a corresponding change in recombination parameters indicates that the enhanced WPE observed after backside KOH processing arises predominantly from improved optical extraction rather than from modifications to carrier recombination dynamics. This conclusion is consistent with the unchanged electrical characteristics and further supports an optical origin for the efficiency enhancement enabled by backside surface texturing.

Table 5.1: Extracted efficiency parameters from EQE model fitting for μLEDs on sapphire and PEN substrates.

Substrate	v_s (cm s^{-1})	LEE_∞
Sapphire	50	0.29
PEN	96	0.34
PEN with backside KOH	98	0.42

Having established both the preservation of intrinsic μLED performance after transfer and the additional performance gains enabled by PATP-accessible backside processing, we next examine the influence of mechanical deformation.

5.5 Performance on Flexible PEN under bending conditions

Before introducing bending-induced strain, it is beneficial to first quantify any spectral changes associated solely with the transfer process itself, as these may provide insight into strain relaxation occurring during LLO and PATP. Figure 5.6(a) shows the emission energy shift, ΔE , defined as the difference in peak electroluminescence energy measured on PEN relative to sapphire, as a function of device diameter for $8 \mu\text{m}$, $10 \mu\text{m}$, $20 \mu\text{m}$ and $100 \mu\text{m}$

μ LEDs. Additional details on the spectral measurements can be found in Appendix C.5. All PEN measurements were performed under flat, unbent conditions. Across all device sizes, the magnitude of the emission energy shift remains below 12 meV (<2 nm), with a consistent shift toward lower photon energies, corresponding to a small red shift of the emission wavelength.

Such a red shift is commonly associated with partial relaxation of the biaxial compressive strain in InGaN/GaN MQW structures. Strain is intrinsic to III-nitride heteroepitaxy due to lattice mismatch and modifies the electronic band energies through deformation potentials, which couple strain to the band structure and lead to shifts in the optical transition energy.[58, 59] Relaxation of this compressive strain is therefore expected to reduce the bandgap, and can lead to a red shift of the emission energy, consistent with prior reports of substrate lift-off in InGaN/GaN blue LEDs, where a shift of ~ 11 meV was observed following strain relaxation and redistribution.[60] At the same time, strain relaxation reduces the piezoelectric polarization field and the associated quantum-confined Stark effect (QCSE), which would be expected to blue-shift the emission; the small net red shift observed here therefore suggests that deformation-potential-induced bandgap reduction likely dominates under partial relaxation.[39, 60]

In μ LEDs, strain relaxation at mesa edges is known to increase as device size decreases, leading to a reduction in QCSE and size-dependent changes in emission energy.[39] However, no systematic dependence of the emission energy shift on device diameter is observed here over the range of 8 μ m to 100 μ m, with all devices exhibiting a similar red shift below 12 meV. Because of this, the observed behavior is more consistent with a global modification of the strain state following substrate removal, rather than lateral edge-driven relaxation effects. This may also indicate that QCSE reduction plays a limited role in the present structures, either due to the relatively low indium content of the blue-emitting MQWs, which leads to smaller piezoelectric fields, or due to geometric factors such as the double-mesa architecture, which could partially isolate the active region from size-dependent strain relaxation.[39, 59]

Figure 5.6(b) presents representative normalized electroluminescence spectra for a 100 μ m μ LED measured on sapphire and after transfer to PEN sourced at a current of 0.5 mA. The spectra exhibit nearly identical FWHM, with the small red shift on PEN clearly observable, further indicating that the transfer process does not introduce additional inhomogeneous broadening or spectral distortion.

Figure 5.6(c) illustrates the mechanical bending configurations used to evaluate strain-induced effects, including flat, tensile, and compressive conditions. For both tensile and compressive bending, the PEN substrate was bent to a ROC of 11 mm using custom jigs

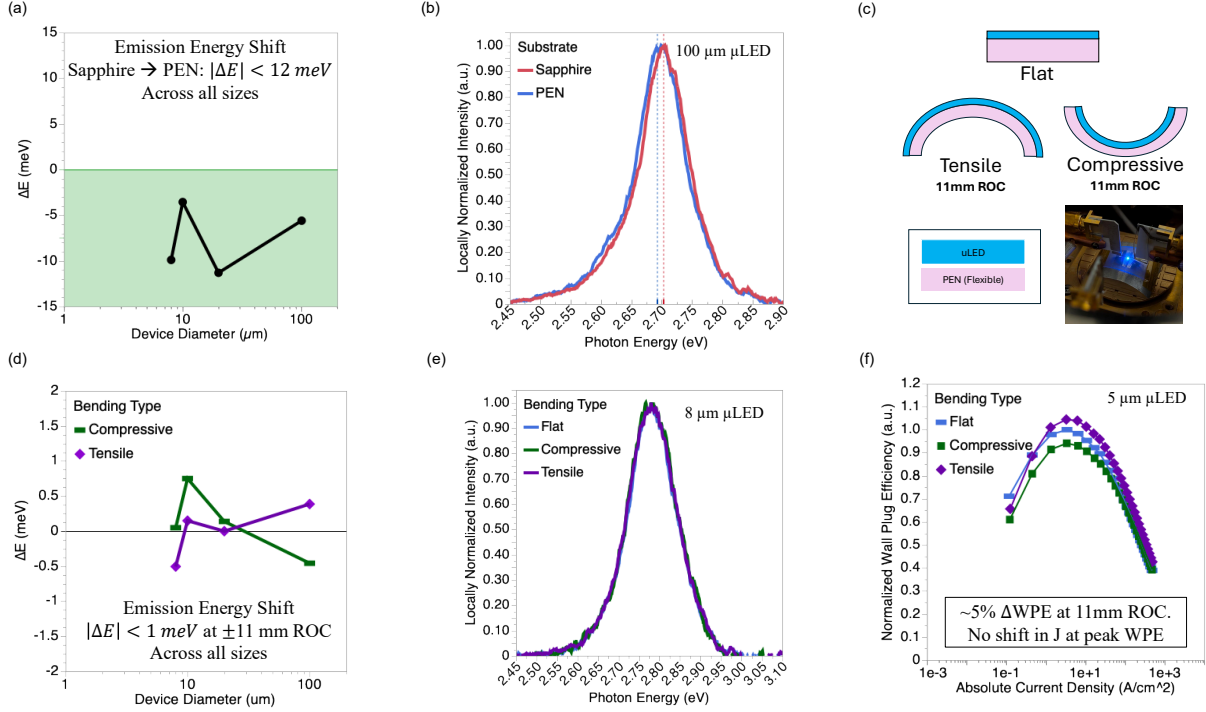


Figure 5.6: Optical and electrical characterization of flexible μ LEDs following substrate transfer and under mechanical deformation. (a) Emission energy shift (ΔE) measured after transfer from sapphires to PEN substrates for μ LEDs of different diameters. (b) Representative normalized electroluminescence spectra of a 100 μm μ LED on sapphires and PEN substrates. (c) Schematic and photographs of the flat, tensile, and compressive bending configurations with a radius of curvature (ROC) of 11 mm. (d) Emission energy shift measured under tensile and compressive bending at an ROC of 11 mm for μ LEDs of different diameters. (e) Normalized electroluminescence spectra of an 8 μm μ LED under flat, tensile, and compressive bending conditions. (f) Normalized WPE as a function of current density for a 5 μm μ LED under flat, tensile, and compressive bending conditions.

and secured with Kapton tape. This relatively demanding ROC is more severe than typical operating conditions in many flexible and wearable optoelectronic applications, where mechanical requirements depend on device thickness, form factor, anatomical placement, and whether deformation is static or cyclic. Flexible biosensors and wearable optical devices are designed to conform to soft, curved, dynamically deforming biological surfaces while maintaining mechanical reliability and signal stability; because bending strain scales inversely with radius, smaller radii impose more stringent demands on the device stack.[61]

The chosen ROC therefore offers a stringent yet practically relevant test of mechanical robustness. An optical photograph of a representative 100 μm μLED on PEN mounted on the bending jig and electrically probed under electroluminescent operation is also shown in Figure 5.6(c). Further details of the mechanical testing setup and in situ optoelectronic measurements under bending are provided in Appendix C.3

To evaluate whether mechanical bending induces additional strain in the MQW region that could alter the optical response, the emission energy shift was also measured under controlled bending conditions. Figure 5.6(d) summarizes the change in ΔE extracted under compressive and tensile bending and referenced to the flat condition, as a function of device diameter (8 μm , 10 μm , 20 μm and 100 μm). The bending configurations correspond to the same tensile and compressive conditions described previously, with a ROC of 11 mm.

Across all device sizes and for both bending polarities, the magnitude of the emission energy shift remains below 1 meV. This indicates that mechanical bending to a relatively small ROC does not measurably perturb the emission spectrum of the μLED s. The absence of a systematic shift with device size further suggests that, for this specific double-mesa μLED structure, bending-induced strain does not significantly modify the band structure or polarization fields within the MQW region.

Figure 5.6(e) shows representative normalized electroluminescence spectra for an 8 μm μLED on PEN measured under flat, compressive, and tensile bending conditions sourced at a current of 0.5 mA. The peak position and FWHM are essentially identical across all three cases, confirming that mechanical deformation does not introduce detectable spectral broadening or energy shifts. Together with the results in Figure 5.6(a) and Figure 5.6(d), these data indicate that while a small red shift is observed upon transfer from sapphire to PEN, subsequent bending of the flexible substrate has a negligible effect on the optical emission characteristics.

To assess whether mechanical bending influences overall optoelectronic efficiency, the WPE was measured under flat, compressive, and tensile conditions using a custom-designed bending jig. The jig incorporates an aperture beneath the device to allow bottom-emitted light to reach a calibrated photodiode positioned below the substrate. Separate jigs were fabricated for each bending condition, with care taken to maintain an identical distance between the μLED and the photodiode in all cases. Additional details of the optical collection geometry and measurement procedure are provided in Appendix C.3

Figure 5.6(f) shows the normalized WPE as a function of absolute J for a 5 μm μLED on PEN with backside KOH texturing under flat, compressive, and tensile bending at a ROC of 11 mm. The WPE is normalized to the peak value measured in the flat condition. For both tensile and compressive bending, the relative peak WPE deviates from the flat

case by less than approximately 5%. While small variations may arise from unavoidable experimental factors such as device centering relative to the jig aperture, no significant degradation or enhancement of WPE is observed under bending. Furthermore, the J_{peak} remains unchanged, indicating that bending does not measurably affect recombination dynamics, including SRH NRR.

Overall, these results demonstrate that high-efficiency μ LEDs with lateral dimensions down to 5 μm can be integrated onto flexible PEN substrates while remaining largely insensitive to mechanical bending, even at a relatively aggressive ROC of 11 mm. For the double-mesa μ LED architecture studied here, both optical emission properties and optoelectronic efficiency are preserved under tensile and compressive deformation, underscoring the mechanical robustness of the transfer-enabled flexible μ LED platform.

5.6 Summary

This chapter has demonstrated a robust and scalable pathway for integrating high-efficiency InGaN μ LEDs onto flexible substrates while preserving, and in some cases enhancing, their optoelectronic performance. A PATP approach was employed to decouple high-temperature device fabrication from the final flexible form factor, enabling fully optimized μ LEDs to be transferred from sapphire onto flexible PEN substrates without compromising electrical integrity or efficiency.

Detailed electrical and optoelectronic characterization confirmed that the transfer process preserves intrinsic device behavior. μ LEDs on PEN exhibited reverse leakage currents below 100 fA, near-identical forward JV characteristics, and statistically indistinguishable minimum IFs compared with devices on sapphire. Correspondingly, p-WPEs of approximately 28 % were maintained after transfer, indicating that neither parasitic resistance nor NRR pathways are introduced by the transfer and bonding sequence. A key advantage of the PATP flow is the intermediate rigid-carrier step following LLO, which provides direct access to the exposed n-polar GaN backside for post-fabrication optical engineering. Exploiting this capability, controlled backside roughening using a KOH-based wet etch was introduced to enhance light extraction. Devices incorporating backside texturing exhibited a clear improvement in p-WPE, reaching values of ~ 31 % for 5 μm μ LED, corresponding to an enhancement of roughly 10% relative to planar reference devices. Electrical measurements confirmed unchanged IFs after KOH treatment, indicating that the efficiency improvement originates from enhanced LEE rather than modified recombination dynamics. This conclusion was further supported by FDTD simulations and size-dependent efficiency

modeling, which showed a substantial increase in the extracted LEE_{∞} with negligible change in the v_s .

The mechanical robustness of the flexible μ LEDs platform was evaluated under tensile and compressive bending at a ROC of 11 mm. A small red shift in emission energy was observed upon transfer from sapphire to PEN, consistent with partial strain relaxation following substrate removal. However, subsequent mechanical bending induced no measurable changes in emission energy and spectral linewidth. Across device diameters down to 5 μ m, variations in WPE under bending remained within experimental uncertainty, demonstrating that both optical and electrical performance are largely insensitive to mechanical deformation under demanding bending conditions.

Overall, this work establishes that high-performance InGaN μ LEDs can be reliably integrated onto flexible substrates using a scalable transfer strategy that preserves intrinsic efficiency while enabling additional optical optimization through transfer-enabled back-side processing. The demonstrated combination of high efficiency, mechanical resilience, and compatibility with wafer-scale fabrication provides a compelling foundation for next-generation flexible display technologies and emerging biophotonic systems that require bright, efficient, and mechanically compliant light sources. In the framework of Equation 1.1, transfer preserved η_{elec} and IQE while raising LEE, completing the optimization hierarchy on a mechanically compliant platform.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis examined the physical and technological limits governing the efficiency and scalability of laterally scaled InGaN μ LEDs as device dimensions approach the few-micrometer regime. A central conclusion is that the efficiency degradation often observed at small sizes is not an intrinsic consequence of miniaturization; it primarily arises from process-induced NRR pathways that dominate when surface and interface quality are not sufficiently controlled.

Within the WPE decomposition of Equation 1.1, Chapters 2–4 sequentially address electrical injection (η_{elec}), recombination losses, and photon extraction through contact engineering, suppression of surface-related SRH recombination, and enhancement of LEE. Chapter 5 then removes the remaining substrate constraint via transfer-based integration, preserving the preceding gains while enabling additional backside optical engineering.

Experimentally, robust ohmic contacts (including a practical transparent p-contact) provided a low-loss electrical baseline, allowing size-dependent behavior to be interpreted in terms of intrinsic recombination and optical effects. The dominant size-dependent loss mechanism was identified as surface-related SRH recombination, parameterized by the surface recombination velocity v_s ; introducing a practical critical diameter, d_{crit} , provided a transferable metric for benchmarking when devices transition from bulk- to perimeter-limited operation. By combining chemical sidewall repair with polymeric encapsulation, model extrapolation showed that v_s was suppressed such that d_{crit} shifted below the targeted device dimensions, enabling geometry-driven extraction strategies (including perforated architectures) to increase LEE without incurring a recombination penalty.

Finally, photonic-assisted transfer enabled high-efficiency μ LEDs to be integrated onto flexible PEN while preserving electrical and recombination behavior and improving WPE via backside engineering, with minimal sensitivity to bending. Overall, the results show that scaled μ LEDs performance is governed primarily by surface and interface physics rather than geometry alone, and that coordinated control of contacts, surfaces, optics, and integration enables scaling and form factors that would otherwise be prohibitive.

6.1.1 Design Guidelines for Scaled InGaN μ LEDs

Although this thesis focuses on InGaN μ LEDs, the governing principles at small dimensions are broadly applicable. The guidelines below summarize a step-by-step framework for laterally scaled optoelectronic devices: treat epitaxy, contacts, surface recombination control, optical extraction, and integration as a deliberate hierarchy to reach a regime where performance is limited primarily by intrinsic material properties rather than by geometry- or process-induced losses.

1. Epitaxy

The most critical determinant of scaled device performance is the intrinsic quality of the epitaxial material and the resulting IQE. No degree of contact optimization, surface passivation, or optical engineering can compensate for a low radiative recombination efficiency in the active region. As device dimensions shrink, any residual NRR channels in the bulk are increasingly amplified.

In this work, the epitaxial structure was commercially sourced and therefore fixed; nevertheless, the results underscore that future improvements in scaled μ LED performance will increasingly rely on epitaxial-level innovations. Emerging approaches such as strain engineering, polarization-field management, advanced techniques including V-pit engineering or novel heterostructure concepts provide promising routes toward higher IQE and improved carrier confinement. These strategies are broadly applicable across high-performance optoelectronic material systems.

2. Electrical contacts

For any high-performance optoelectronic device, electrical contacts must enable efficient carrier injection without introducing parasitic electrical resistance, optical absorption, or process-induced damage. As device dimensions shrink and operating current densities increase, contact-related losses can become performance-limiting even when the active material itself exhibits high IQE. Consequently, contact quality

must be treated as a first-order design consideration across material systems and device platforms.

In wide-bandgap semiconductors, and particularly in III–nitride devices, p-type contacts remain a central challenge due to limited dopant activation, low hole mobility, and the competing requirements of transparency and low resistivity. In many cases, achieving optimal contact performance necessitates co-design of the contact scheme with the epitaxial structure itself. Approaches such as tunnel junctions, which replace conventional p-type injection with n-type layers, exemplify this strategy and have become increasingly prevalent in GaN-based optoelectronics, including deep-UV LEDs where p-GaN limitations are especially severe.

In this thesis, a conventional GaN μ LED architecture employing p-GaN was used, combined with a carefully optimized, in-house ITO transparent contact. While this approach does not represent an ideal solution to p-type injection in GaN, it enabled reliable ohmic behavior, high-current-density operation, and substantial efficiency improvements within the constraints of a commercially sourced epitaxial structure. In contrast, n-type contacts were readily achieved and did not constitute a limiting factor, consistent with broader experience across III–V optoelectronic material systems.

3. Surface recombination

After epitaxy and contacts, surface-mediated NRR becomes the dominant limitation in laterally scaled devices. As the S2V ratio increases, the surface recombination velocity, v_s , governs the balance between radiative and non-radiative processes and ultimately determines whether efficiency can be maintained at small dimensions.

This behavior can be captured through the concept of a critical diameter, d_{crit} , which marks the transition between bulk-dominated and surface-dominated recombination. Designing devices such that d_{crit} lies well below the intended lateral dimensions ensures that recombination remains bulk-limited and that efficiency is robust against further scaling. In this sense, d_{crit} serves as a physically meaningful process benchmarking metric, complementary to absolute efficiency values.

In this work, surface recombination was suppressed through a combination of chemical sidewall treatment and polymeric passivation. Chemical repair steps, such as KOH-based wet etching, mitigate plasma-induced damage and restore well-defined surface terminations, while polymeric encapsulants provide low-trap-density interfaces that stabilize the surface electrically. Although demonstrated here for InGaN μ LEDs, this general approach to surface recombination control is applicable to scaled optoelectronic devices across material systems.

4. Light extraction

Only after surface recombination has been sufficiently suppressed does it become meaningful to pursue optical optimization. When v_s is high, improvements in LEE are masked by non-radiative losses, and the full impact of optical engineering cannot be realized. This statement pertains to *device-level* optical design; additional gains are often achievable at the package/system level (e.g., index-matched encapsulants, epoxy selection, and optical coupling from sapphire into the external medium). As such, light extraction can be treated as a secondary design step that follows electrical and surface optimization.

In this thesis, LEE was enhanced through multiple approaches. Backside KOH texturing reduced TIR and increased optical scattering, leading to improved extraction without measurably changing the dominant recombination behavior. In addition, perforated device architectures were employed to introduce additional emitting surfaces, enabling geometry-driven extraction enhancements that become viable only once surface recombination is adequately controlled.

These results highlight a clear hierarchy: electrical and recombination losses must be minimized before geometry-driven optical gains can be fully exploited in scaled devices.

5. Integration and form factor

With intrinsic device performance established through control of epitaxy, contacts, surface recombination, and light extraction, devices can then be integrated onto substrates and platforms selected for their intended application rather than their compatibility with high-temperature processing.

In this work, a transfer-based integration strategy enabled high-efficiency μ LEDs fabricated on rigid substrates to be integrated onto flexible polymer substrates without degrading electrical or optical performance. Importantly, the transfer process also enabled additional backside optical engineering prior to final integration. More broadly, such approaches allow high-performance optoelectronic devices to be deployed across diverse form factors - including rigid, flexible, and mechanically compliant platforms - without sacrificing efficiency.

This final step underscores a general principle: when intrinsic performance is preserved, integration becomes a system-level design choice enabling the same device architecture to serve a wide range of applications.

Overall, these steps define a general design framework for scaled high-performance optoelectronic devices. While demonstrated here using InGaN μ LEDs, the hierarchy of

epitaxial quality, contact engineering, surface recombination control, optical optimization, and platform integration is broadly applicable across material systems and device technologies.

6.2 Future Work

This thesis has demonstrated that high-efficiency InGaN μ LEDs can be laterally scaled, optically engineered, and integrated onto flexible substrates while preserving intrinsic electrical and optical performance. Importantly, many of the fabrication and integration steps employed here were not fully optimized, indicating that the results presented represent a robust baseline rather than a fundamental performance limit. Several clear and complementary directions for future work therefore emerge.

A primary opportunity lies in further optimization of the epitaxial structure. In this work, commercially available epitaxy was used, limiting direct control over material quality, carrier confinement, and recombination dynamics. Access to optimized or custom-grown epitaxy would enable targeted reductions in NRR and carrier overflow, particularly under high-current-density operation. Approaches such as strain engineering, improved quantum well design, and V-pit engineering offer promising routes to enhancing IQE and mitigating efficiency droop, especially in laterally scaled devices where carrier confinement becomes increasingly critical.

Electrical contact optimization represents a second avenue for improvement. While the in-house ITO-based transparent contact employed here enabled reliable ohmic behavior and high-current operation, further gains are possible through improved contact transparency, reduced optical absorption, and lower contact resistivity. Advanced transparent conductors or refined ITO deposition and annealing strategies could reduce optical losses while maintaining electrical performance. More fundamentally, co-design of contacts and epitaxy - such as through tunnel-junction-based architectures - could eliminate p-GaN-related limitations altogether, improving current spreading and injection efficiency across a broader operating range.

Further development of surface passivation strategies is also warranted. Although polymeric encapsulation proved effective at suppressing v_s , future work could focus on optimizing polymer formulations and deposition methods to achieve fully conformal coverage of μ LED sidewalls and surface topography. Achieving uniform, pinhole-free passivation while maintaining low interface trap densities would not only further suppress surface recombination, but also enable subsequent processing steps that are currently limited by surface exposure.

One such opportunity enabled by improved passivation is the integration of conformal reflective layers. With robust electrical passivation in place, conformal reflectors deposited on or around the μ LED mesas could be used to redirect laterally guided optical modes downward, reducing waveguiding losses and further enhancing LEE. When combined with backside texturing and perforated device architectures, such reflectors could enable hierarchical optical optimization strategies that substantially increase extraction efficiency without compromising recombination dynamics.

Beyond optical optimization, future work should address efficiency droop and thermal effects at high current densities. While improvements in epitaxy, carrier confinement, and contact design can mitigate droop by reducing carrier overflow and injection imbalance, thermal management becomes increasingly important as optical power density increases. This challenge is particularly pronounced for flexible substrates, which typically exhibit poor thermal conductivity. Integration strategies incorporating thermally conductive layers, heat-spreading films, or hybrid substrates could provide effective heat dissipation while preserving mechanical compliance. Such approaches would be especially valuable for sustained high-brightness operation in micro-display and biophotonic applications.

An additional and critical area for future investigation is the long-term reliability of flexible μ LEDs under mechanical and electrical stress. While this work demonstrated that device performance is largely insensitive to static bending, systematic studies of cyclic bending over large numbers of mechanical cycles are required to assess fatigue, delamination, and degradation mechanisms in flexible device stacks. In parallel, long-term operational stability under continuous or high-duty-cycle electrical operation must be evaluated, particularly under elevated current densities where self-heating and thermomechanical stress may accelerate degradation. Understanding the coupled effects of mechanical deformation, thermal loading, and prolonged electrical stress will be essential for translating high-performance flexible μ LEDs into practical, reliable systems.

Finally, the transfer-based integration strategies developed in this thesis provide a foundation for exploring a broader range of form factors and system-level architectures. Extending these techniques to heterogeneous integration with electronic backplanes, stretchable substrates, or thermally engineered platforms could enable new device classes that combine high efficiency, mechanical adaptability, thermal robustness, and long-term reliability.

Collectively, these directions highlight that the platform established in this work is not only compatible with, but well suited for, continued materials, device, and system-level optimization. By combining improved epitaxy, advanced contact schemes, enhanced passivation, hierarchical optical engineering, thermal management, and reliability studies, future iterations of scaled μ LEDs can push beyond current performance while expanding

the range of viable applications and form factors.

6.3 Published Articles and Conference Papers

Portions of the research presented in this thesis have been published in peer-reviewed journals and conference proceedings, as listed below. Additional manuscripts building on the results of this thesis are currently in preparation.

Journal Articles

- **P. Gavirneni** and W. S. Wong, “Perforated InGaN μ LED Architectures for Enhanced Light Extraction and Efficiency Scaling,” manuscript in preparation for journal submission.
- **P. Gavirneni** *et al.*, “Flexible High-Efficiency μ LED Devices Enabled by Transfer Printing and Backside Optical Engineering,” manuscript in preparation for journal submission.
- **P. Gavirneni** and W. S. Wong, “Minimizing interface defects and enhancing optical brightness of μ LEDs through polymeric encapsulants,” *Nature Communications Engineering*, 2026. DOI: 10.1038/s44172-026-00661-0
- S. Ranjan; C. H. Lee; **P. Gavirneni**; W. S. Wong, and M. Sachdev, “Design of Low-Power DFFs With Unipolar Thin-Film Transistor,” *IEEE Journal of Flexible Electronics*, 2026. DOI: 10.1109/JFLEX.2026.3658025
- M. Asad, R. Wang, Y.-H. Ra, **P. Gavirneni**, Z. Mi, and W. S. Wong, “Optically invariant InGaN nanowire light-emitting diodes on flexible substrates under mechanical manipulation,” *npj Flexible Electronics*, 2019. DOI: 10.1038/s41528-019-0059-z

Conference Proceedings

- **P. Gavirneni** and W. S. Wong, “Design, fabrication, and effect of polymeric passivation layers to suppress sidewall recombination in high efficiency GaN μ LEDs,” *Proceedings Volume 13913, Light-Emitting Devices, Materials, and Applications XXX; 1391303* (2026). DOI: 10.1117/12.3075097

- **P. Gavirneni** and W. S. Wong, “Optical enhancement of mechanically flexible μ LEDs enabled by photonic transfer,” *Proceedings Volume 13915, Advances in Display Technologies XVI; 1391504* (2026) DOI: 10.1117/12.3077729
- **P. Gavirneni et al.**, “Optical and Electrical Characteristics of Heterogeneously Integrated Blue microLEDs for High-Resolution Displays,” **INVITED**. *International Display Workshops (IDW)*, Japan, 2025. Proceedings forthcoming.
- **P. Gavirneni**, R. T. Rashid, C.-H. Lee, W. S. Wong, and K. Schroder, “High-Efficiency MicroLED Displays Enabled Through PulseForge Assisted Die Transfer,” *SID Symposium Digest of Technical Papers*, 2023. DOI: 10.1002/sdtp.16674
- A. Pil-Ali, S. Adnani, **P. Gavirneni**, S. Shin, B. Sadeghimakki, M. Poudineh, W. S. Wong, and K. S. Karim, “Self-aligned fabrication of high aspect-ratio, high-resolution μ LED structures,” *Proc. SPIE*, 2022. DOI: 10.1117/12.2613059
- **P. Gavirneni**, J. Coggan, W. Chang, C. Rennick, and E. Veintimilla, “Development and Assessment of a Training Module on Intellectual Property Literacy,” *Proceedings of the Canadian Engineering Education Association (CEEAA)*, 2022. DOI: 10.24908/pceea.vi.15859

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APPENDICES

Appendix A

Details of materials and methods from Chapter 3

A.1 μ LED Fabrication

Commercially available blue InGaN-based LED epitaxial heterostructures ($\lambda_{\text{emission}} = 445 \text{ nm}$) grown on double-sided polished planar (unpatterned) sapphire substrates were obtained from SemiLEDs Corporation. The substrates were initially cleaned using a piranha solution prior to processing.

A 600 nm-thick PECVD-deposited SiO_2 film was used as an etch mask for subsequent GaN mesa definition. Ultraviolet photolithography was employed to define the μ LED mesa areas. The SiO_2 etch mask was patterned and followed by a GaN dry etch performed using an Oxford Instruments ICP380 system with a Cl_2/BCl_3 plasma chemistry. The resulting mesa etch depth was 1.5 μm . Following the mesa etch, the wafer was diced into smaller chips with dimensions of 15 mm $\times$ 15 mm. In total, five chips were fabricated, each incorporating a distinct sidewall passivation configuration as listed below:

- Chip #1: SiO_2 bilayer without KOH treatment
- Chip #2: SiO_2 bilayer with KOH treatment
- Chip #3: SU-8 without KOH treatment
- Chip #4: SU-8 with KOH treatment

- Chip #5: SiO₂ (ALD) / SU-8 bilayer without KOH treatment

Samples incorporating both SiO₂/SU-8 bilayer encapsulants (Chip #5) were fabricated for comparison. Following dicing, Chip #2 and Chip #4 were subjected to a KOH treatment at room temperature. All chips subsequently underwent removal of the SiO₂ etch mask using a 10:1 buffered oxide etch (BOE) solution. Figure A.1 presents SEM images acquired after SiO₂ mask removal for devices with and without KOH treatment. KOH etching of GaN is crystallographically anisotropic. The treatment preferentially removes plasma-damaged and crystallographically less stable material from the dry-etched sidewall, allowing relatively stable nonpolar GaN facets to emerge. For the nominally circular mesas used here, several facets form around the perimeter. Consequently, the treated sidewall appears macroscopically textured in the SEM image even though the individual crystallographic facets are expected to be locally smoother than the original plasma-etched surface. The SEM images confirm the change from an approximately continuous dry-etched perimeter to a faceted morphology, but they do not provide sufficient spatial resolution to establish atomic-scale surface roughness.

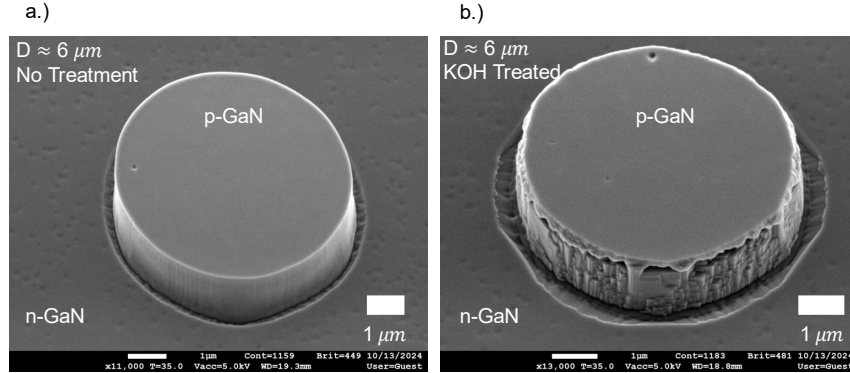


Figure A.1: Comparison of untreated and KOH treated μ LED mesa sidewalls. (a) 35° tilted scanning electron micrograph of a 6 μ m μ LED mesa after GaN etching and SiO₂ strip, without sidewall treatment. (b) Corresponding 35° tilted scanning electron micrograph of a 6 μ m μ LED mesa after KOH treatment, prior to SU-8 encapsulation. The p-GaN mesa and surrounding n-GaN region are labeled in both images. Scale bars, 1 μ m.

The n-type contact was deposited using an Angstrom Engineering electron-beam evaporator. The n-contact metallization stack consisted of Cr/Al/Ni/Au with thicknesses of 5 nm/100 nm/30 nm/100 nm, respectively, and was defined using a metal lift-off process. Prior to metal deposition, the exposed GaN surface was treated with a 1:1 hydrochloric acid solution. The p-type contact consisted of a Pd/Ni/Au metallization stack

(30 nm/10 nm/200 nm) and was deposited using an identical lift-off procedure. The p-contact radius was defined to be consistently approximately $1.7\text{ }\mu\text{m}$ smaller than the corresponding μLED mesa radius, resulting in a fixed radial offset $\Delta r \approx 1.7\text{ }\mu\text{m}$.

Both n- and p-contacts were annealed simultaneously using RTA at $550\text{ }^\circ\text{C}$ for 5 min in ambient air. The resulting contact resistivities were measured using the c-TLM technique, as described in detail in Chapter 2. The mean contact resistivities extracted for the p-contact and n-contact were $4 \times 10^{-3}\text{ }\Omega\cdot\text{cm}^2$ and $9 \times 10^{-6}\text{ }\Omega\cdot\text{cm}^2$, respectively. The extracted p-contact resistivity lies within the range commonly reported for effective p-GaN ohmic contacts under similar device dimensions and operating conditions. [2]

Prior experimental and simulation studies have shown that lateral current spreading in μLED s typically extends approximately $1\text{ }\mu\text{m}$ to $2\text{ }\mu\text{m}$ beyond the p-contact edge.[22] The p-contact-to-mesa separation employed in this work ($\Delta r = 1.7\text{ }\mu\text{m}$) lies within this range and is not expected to limit charge injection into the p-layer for the device geometries investigated.

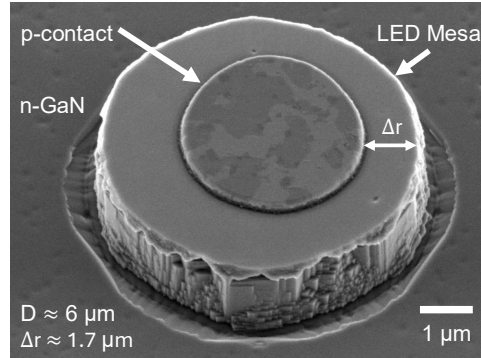


Figure A.2: Sidewall and contact geometry of a $6\text{ }\mu\text{m}$ -diameter μLED after p-contact formation. A 35° tilted SEM image showing the p-contact, the LED mesa edge, and the surrounding n-GaN region. The radial separation between the p-contact edge and the mesa sidewall ($\Delta r \approx 1.7\text{ }\mu\text{m}$) is indicated. Scale bar: $1\text{ }\mu\text{m}$.

A SiO_2 bilayer consisting of 10 nm deposited by ALD followed by 150 nm deposited by PECVD was applied to Chips #1, #2, and #5 using an Oxford PlasmaLab 100 PECVD/ALD cluster tool. SU-8 3010 was spin-coated and patterned onto Chips #3, #4, and #5.

A conformal 500 nm-thick aluminum layer was sputtered and patterned on all chips to define the metal interconnects. These metal traces served both as probe pads and as a

reflector to redirect emitted light downward through the sapphire substrate. For SU-8-encapsulated devices, the via step height was approximately $6\text{ }\mu\text{m}$, corresponding to a via aspect ratio below 2, which provided adequate electrical access to the p-contact.

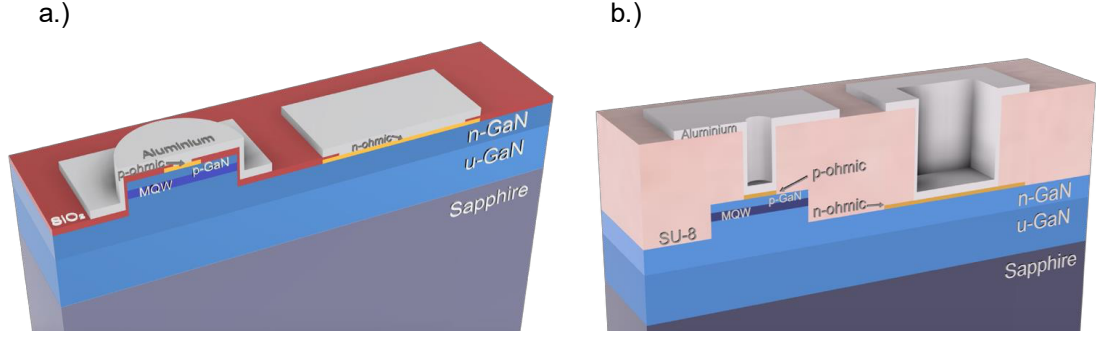


Figure A.3: Schematic illustration of the final μLED device structures. (a) Schematic of a μLED with a SiO_2 bilayer sidewall coating, showing the p-contact, mesa, GaN layers, and sapphire substrate. (b) Schematic of a LED with SU-8 sidewall encapsulation, illustrating the corresponding device geometry and contact configuration. Schematics are not drawn to scale.

Two key differences exist between the sidewall coating approaches. First, the SiO_2 bilayer was deposited under high-vacuum conditions, whereas the SU-8 encapsulant was applied via spin coating under ambient cleanroom conditions. Second, the SiO_2 bilayer permits conformal aluminum metallization along the μLED sidewalls, with the metal separated from the semiconductor only by the SiO_2 bilayer. In contrast, the SU-8 encapsulation planarizes the device surface and spatially decouples the aluminum metal from the μLED sidewalls.

A.2 Device Characterization

Devices were characterized through combined optical and electrical measurement techniques. For characterization, each LED device on a sapphire substrate was positioned atop a silicon photodiode detector (Thorlabs FDS1010) with a known responsivity curve, capturing emitted light through the sapphire substrate. Electrical connections were established by probing the μLED within a blackout Faraday cage to eliminate external interference. Both the photodiode and the μLED s were connected to a Keithley 4200A Semiconductor Characterization System Parameter Analyzer, capable of measuring currents down to

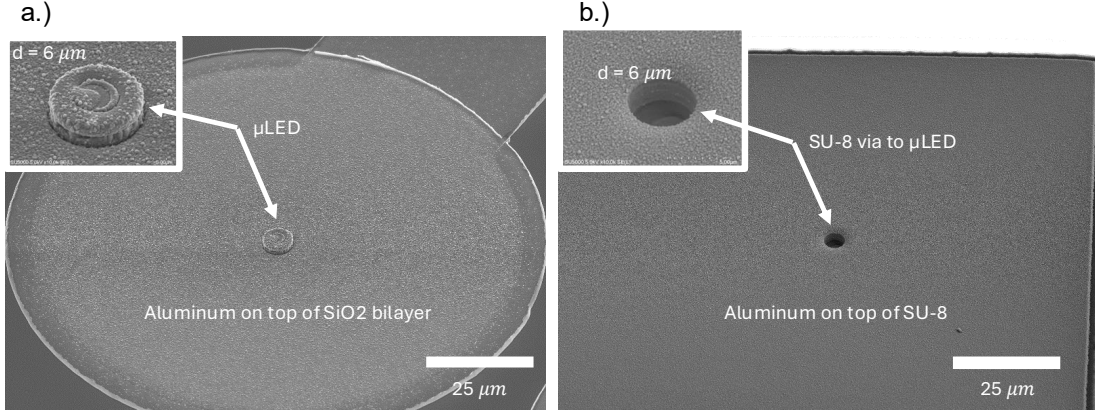


Figure A.4: Fully fabricated 6 μm -diameter μLED s with different sidewall coatings. **(a)** 45° tilted SEM image of a fully fabricated 6 μm -diameter μLED incorporating a SiO₂ bilayer sidewall coating. **(b)** Corresponding 45° tilted SEM image of a fully fabricated 6 μm -diameter μLED with SU-8 encapsulation. Insets show higher-magnification views of the μLED top surface for each device. Scale bars: 25 μm (main images).

femto-ampere levels. The measurement involved performing a current–voltage (IV) sweep of the diode while simultaneously recording the LED’s optical intensity through the photodiode’s photocurrent. The electrical measurements were performed across a minimum of three devices to extract device parameters; the error bars represent the extracted standard deviation of the measurements. The μLED IV and photodiode current were used to calculate the EQE and the WPE for optical characterization. For the WPE measurements, errors for a given J were determined at a fixed applied voltage. The μLED J was consistently calculated using the mesa area for all sizes and sidewall coating schemes.

A.3 Structural Characterization

The SEM images were taken using both a JSM-7200F JEOL and a SU5000 Hitachi microscope system. Both systems were equipped with a variable angle stage allowing for measurements at 35° tilt. An accelerating voltage of 5 kV was used for imaging.

A.4 Recombination Parameter Fitting

A fitting procedure, using a standard MATLAB built-in nonlinear optimization loop, employed the physical ABCCD model to determine a single set of global epitaxial-layer parameters (A_0 , B , C_{dl} , D_{dl}) to be shared across all devices, regardless of size, sidewall coating, or treatment. This approach enabled global fitting over a wider current density (J) range, where the optimizer fits the entire EQE– J curve rather than the low- J region only. While surface recombination dominates at low J , higher-order terms (C_{dl} and D_{dl}) become significant at high injection. Constraining these terms through full-range fitting ensures that the low- J shoulder is primarily determined by v_s , avoiding arbitrary parameter choices. To capture the overall behavior, the optimizer simultaneously fits all EQE curves, covering three sidewall coating/treatment configurations (SiO₂ untreated, SU-8 untreated, and SU-8 treated), each with three device diameters. In total, nine EQE curves were fitted concurrently using the global and local parameter constraints described. Within each sidewall coating/treatment set, the surface recombination velocity v_s was treated as a material-dependent parameter and applied across all device sizes. Convergence occurs when a single v_s reproduces all EQE– J curves for a given configuration, constraining the solution. This combined strategy, full-range global fitting and multi-geometry enforcement of v_s , ensures a physically meaningful extraction despite detection-limited sampling at low current densities.

To fit the EQE dependence on the measured current density (EQE vs J data), the MATLAB optimization loop was run to minimize the sum of squared errors (SSE) between measured and modeled EQE. In this fitting procedure, the measured EQE curves were modeled using,

$$EQE(d, n) = LEE(d) \times IQE(d, n) \quad (\text{A.1})$$

$$= [LEE_{\infty} + \alpha d^{-\beta}] \times \frac{Bn^2}{\left(A_0 + \frac{4v_s}{d}\right)n + Bn^2 + C_{dl}n^3 + D_{dl}n^4} \quad (\text{A.2})$$

In this expression, the light-extraction efficiency (LEE) and the surface recombination velocity (v_s) are treated as separate, independent parameters: LEE(d) accounts for device size-dependent optical extraction, while v_s enters only through the surface recombination rate term. Treating LEE and v_s as separate model terms, together with simultaneous fitting across multiple device diameters, reduces the likelihood that diameter-dependent optical extraction is incorrectly attributed to surface recombination. The model first takes an initial estimate at the coefficients and then solves the following total recombination equation for the carrier density (n) by numerically finding the zeros of the polynomial at

each J value for a specific device,

$$R(n, d) = \left(A_0 + \frac{4vs}{d} \right) n + Bn^2 + C_{dl}n^3 + D_{dl}n^4 \quad (\text{A.3})$$

R is the total recombination rate and is related to J through,

$$R = \frac{J \cdot A_{\mu\text{LED}}}{q \cdot V_{\text{active}}} \quad (\text{A.4})$$

$A_{\mu\text{LED}}$ is the cross-sectional area, and V_{active} is the volume of the active region. Once the carrier density is numerically solved for each J , EQE is calculated using the current parameter estimates, and the SSE is then evaluated. Additionally, global boundary conditions were enforced so that all dies from the same epitaxial wafer share the same LED epilayer-dependent coefficients (A_0 , B , C_{dl} , D_{dl}), since these values do not change with μLED size or sidewall quality. In parallel, μLED s with identical sidewall coating and sidewall quality (i.e. identical process treatments) were bounded with the same v_s , reflecting v_s is not dependent on the μLED size. These boundary conditions imply that A_0 is assumed to remain constant across all sidewall coating schemes. This assumption is based on the premise that sidewall coating primarily affects the interface between the LED and the sidewall coating layer, without altering bulk defect concentrations. Consequently, the model considers only changes in sidewall surface defect densities and the associated v_s when evaluating the impact of sidewall coating.

The MATLAB optimization loop varies the values of the parameters (bounded by physical limits) until the SSE is minimized to provide best-fit values that are represented by both the recombination behavior (A_0 , v_s , B , C , D terms) and size-dependent light extraction (LEE(d)).

Figure A.5 presents the measured EQE curves for SU-8-encapsulated μLED s, with and without KOH treatment, across three device diameters (6 μm , 12 μm , and 17 μm). Data points represent experimental measurements, while the solid lines correspond to EQE curves generated by the model used to extract recombination and light extraction parameters.

The MATLAB code used to implement the global fitting procedure, together with example input data, has been made publicly available through Figshare.[42]

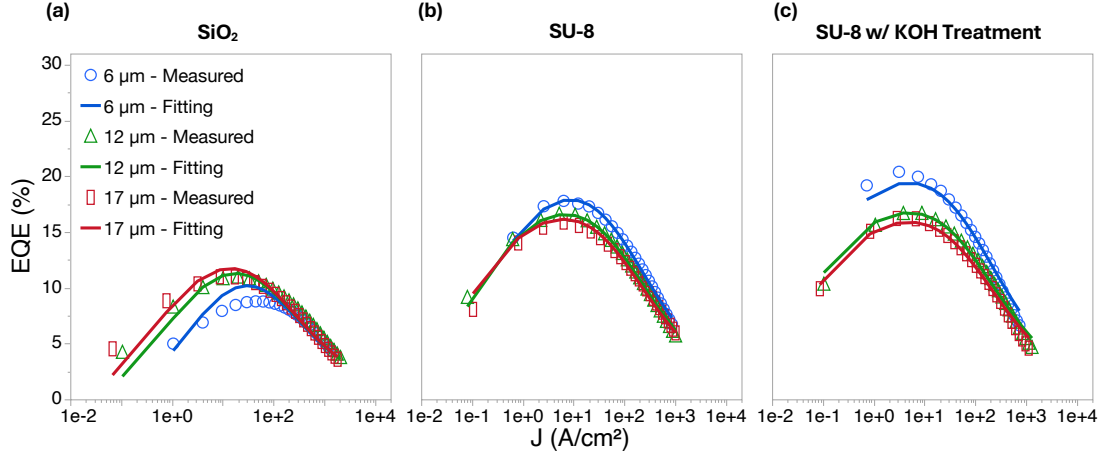


Figure A.5: Measured and modeled external quantum efficiency of SiO₂ passivated and SU-8 encapsulated μ LEDs. External quantum efficiency (EQE, %) plotted as a function of current density (J , A cm⁻²) for SiO₂ (a) SU-8 encapsulated μ LEDs without KOH treatment (b) and with KOH treatment (c). Symbols indicate measured EQE data, and solid lines represent the corresponding fitted EQE curves obtained from the model. Circle, triangle, and square symbols correspond to μ LED diameters of 6 μ m, 12 μ m, and 17 μ m, respectively.

A.5 Evaluation of Light-Extraction Efficiency Effects on Sidewall Coating Comparisons

Differences in WPE between SiO₂ and SU-8-encapsulated μ LEDs could potentially be influenced by variations in LEE, as changes in surface coatings may alter optical behavior. To examine this effect, device structures were fabricated with sidewalls incorporating a 10 nm ALD SiO₂ layer followed by SU-8 3010 coating and patterning. The SiO₂/SU-8-coated devices share a comparable structure with SU-8-only encapsulated devices and are expected to exhibit similar optical characteristics.

Figure A.6 shows WPE versus current density for 6 μ m μ LEDs across three sidewall coating schemes: SiO₂, SU-8, and SiO₂/SU-8. The peak WPE current density for SiO₂ and SiO₂/SU-8-coated devices is nearly identical, indicating similar nonradiative recombination behavior. In contrast, SU-8-only encapsulated devices achieve peak WPE at a current density approximately five times lower, suggesting more effective suppression of nonradiative recombination. Across the entire operating range, SU-8-encapsulated devices consistently exhibit higher WPE than SiO₂-based structures.

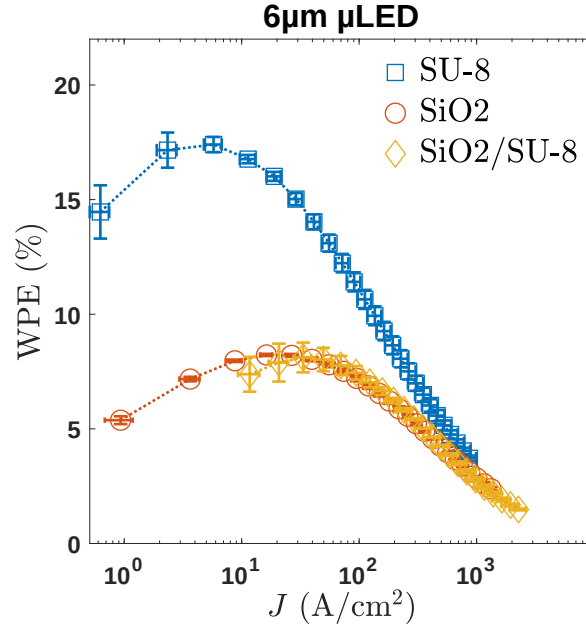


Figure A.6: Opto-electrical efficiency of 6 μm μLEDs with different sidewall coatings: Wall plug efficiency (WPE,%) plotted as a function of current density (J , A cm^{-2}) for 6 μm μLEDs with SU-8 (blue squares), SiO2 (red circles), and combined SiO2/SU-8 (yellow diamonds) sidewall coatings. Symbols represent mean values; error bars indicate the standard deviation. Semi-transparent symbols denote individual device measurements used to calculate the mean. Dotted lines are included as visual guides to aid interpretation and do not represent fitted models. Sample sizes were $N = 4$ devices for SU-8, $N = 3$ devices for SiO2, and $N = 3$ devices for SiO2/SU-8.

Appendix B

Details of materials and methods from Chapter 4

B.1 μ LED Fabrication

Commercially available blue InGaN-based LED epitaxial heterostructures ($\lambda_{\text{emission}} = 445 \text{ nm}$) grown on a 4" double-sided polished planar (unpatterned) sapphire substrates were obtained from SemiLEDs Corporation. The wafer was initially cleaned using a piranha solution prior to processing the p-contact. The p-type contact consisted of a Ni/Au/low-damage ITO/ITO stack (2/1.5/10/70 nm), corresponding to ITO type 4 as described in Section 2.4. Ni/Au layers were deposited by an Angstrom Engineering electron-beam evaporator at a rate of $0.1 \text{ \AA/s}$, followed by ITO deposition by a AJA sputter tool. Prior to deposition, the wafer was treated in a 1:1 HCl solution for 10 min. After patterning, the p-contact was defined using a dual wet-etch process comprising a 10:1 HCl etch for the ITO bilayer and a diluted Transene TFA gold etchant for Au. The p-contact radius was consistently defined to be approximately $1.7 \mu\text{m}$ smaller than the corresponding μ LED mesa radius. The contact stack was annealed at 550°C for 2 min in an N_2/O_2 ambient. C-TLM measurements were performed at six locations across the wafer yielded a specific contact resistivity of $\rho_c = 3 \times 10^{-3} \Omega \cdot \text{cm}^2$.

Unless otherwise specified, the contact resistivities reported in this appendix were measured using in-line c-TLM structures fabricated on the same wafer as the μ LED devices. These values therefore represent the specific Chapter 4 device fabrication run. The annealing time was reduced from the 5 min used during the dedicated contact-development

experiments in Chapter 2 to 2 min because the shorter treatment was found to be sufficient for obtaining low-resistivity ohmic contacts.

Mesa definition employed a two-step hard-mask process. A 600 nm PECVD SiO₂ hard mask was deposited and lithographically patterned, followed by ICP-RIE etching using a Cl₂/BCl₃ plasma to a depth of 1.5 μm , reaching the n-GaN layer. Post-etch KOH treatment at room temperature was used to remove plasma-damaged and crystallographically less stable GaN from the mesa sidewalls and promote the formation of relatively stable, locally smooth nonpolar facets.[28, 43] Because the mesas were not bounded by a single crystallographic plane, the resulting perimeter was macroscopically faceted rather than geometrically smooth. A second 600 nm SiO₂ hard mask and ICP etch defined a deeper surrounding mesa with a total etch depth of 3.5 μm , leaving approximately 1 μm of u-GaN in the field. Residual SiO₂ was removed using BOE, and all exposed GaN surfaces were cleaned in a 1:1 HCl solution prior to metallization.

The n-type contact (Cr/Al/Ni/Au, 5/100/30/100 nm) was deposited by electron-beam evaporation, patterned by metal-lift-off, and annealed. The contact stack was annealed at 550 °C for 2 min in an N₂/O₂ ambient. C-TLM measurements were performed across the wafer yielded a specific contact resistivity of $\rho_c \approx 5 \times 10^{-6} \Omega \cdot \text{cm}^2$. P-type c-TLMs measurements on the ITO stack were repeated after n-contact annealing, and the subsequent annealing step led to a negligible change in ρ_c .

The wafer was diced into $25 \times 25 \text{ mm}^2$ chips. To suppress surface recombination and planarize the topology, a SU-8 overcoat was applied, patterned to open contact vias, briefly cleaned by O₂ plasma, and cured at 200 °C for 20 min. The device set comprised planar circular μLEDs with diameters ranging from 5 to 500 μm , as well as perforated square μLEDs incorporating periodic arrays of internal holes. Fabrication constraints limited the minimum perforation geometry to 3 μm -diameter holes on a 5.6 μm pitch. Finally, probing pads were formed using an Al/Cr/Au (500/30/100 nm) metal stack deposited by metal-lift-off. Figure B.1 summarizes the two device architectures investigated in this work: a conventional planar μLED and a p- μLED in which a periodic array of etched holes is introduced directly through the active region. The perforated structures were fabricated in several array sizes, ranging from a single central hole to a 5 $\times$ 5-hole pattern, corresponding to side lengths from approximately 10 μm to 32 μm . All perforated devices used 3 μm -diameter holes on a 5.6 μm pitch, resulting in total hole counts of 1, 4, 9, 16, and 25.

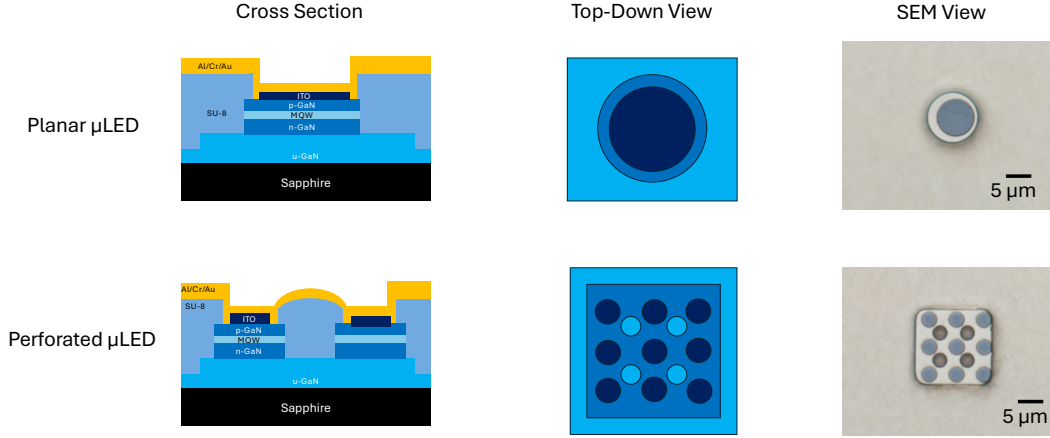


Figure B.1: Structural comparison of planar and perforated μ LEDs: Schematic cross sections (left) illustrate the epitaxial layer stack and mesa geometry for (top) a planar μ LED and (bottom) a perforated μ LED incorporating a periodic array of etched holes extending through the active region. Corresponding top-down renderings (center) show the circular mesa used for planar devices and the square mesa with an internal hole array used for perforated devices. SEM images (right) present the fabricated structures of a $10\text{ }\mu\text{m}$ circular planar μ LED (top) and a $15.5\text{ }\mu\text{m}$ side-length perforated μ LED with a 2×2 array of holes (bottom), with a $5\text{ }\mu\text{m}$ scale bar, confirming the intended mesa profiles, hole placement, and overall pattern.

B.2 Device Characterization

Devices were characterized through combined optical and electrical measurement techniques. For characterization, each LED device on a sapphire substrate was positioned atop a silicon photodiode detector (Thorlabs FDS1010) with a known responsivity curve, capturing emitted light through the sapphire substrate. Electrical connections were established by probing the μ LED within a blackout Faraday cage to eliminate external interference. Both the photodiode and the μ LEDs were connected to a Keithley 4200A Semiconductor Characterization System Parameter Analyzer, capable of measuring currents down to femto-ampere levels. The measurement involved performing a IV sweep of the diode while simultaneously recording the LED's optical intensity through the photodiode's photocurrent. The electrical measurements were performed across a minimum of three devices to extract device parameters; the error bars represent the extracted standard deviation of the measurements. The μ LED IV and photodiode current were used to calculate the EQE and

the WPE for optical characterization. For the WPE measurements, errors for a given J were determined at a fixed applied voltage. The μ LED J was consistently calculated using the mesa area for all sizes and sidewall coating schemes.

The current–voltage characteristics were analyzed to extract the IF within the 2 V–3 V regime using the non-ideal diode equation

$$I = I_0 \exp\left(\frac{qV_{\text{app}}}{nkT}\right) \quad (\text{B.1})$$

The IF provides insight into the dominant recombination mechanisms. Values near $n = 1$ correspond to ideal radiative recombination, whereas $n = 2$ indicates SRH-dominated recombination linked to mid-gap defect states. In practice, GaN-based emitters can exhibit effective IFs exceeding 2 due to parasitic series resistance, leakage pathways, or defect-mediated lateral current channels within the quantum well plane.[3, 27] Examining the IF evolution with voltage therefore helps distinguish regimes dominated by SRH recombination, parasitic conduction, or resistive artifacts, enabling a more complete interpretation of size-dependent and geometry-dependent variations in device behavior. Simultaneous measurement of diode current and photodiode photocurrent enabled extraction of EQE and WPE using the thesis-wide definitions introduced in Chapter 1 (Equation 1.1). For completeness, the extracted forms are

$$EQE = \frac{P/h\nu}{I/q} \quad (\text{B.2})$$

and

$$WPE = EQE \left(\frac{V_p}{V_{\text{app}}} \right) \quad (\text{B.3})$$

where P is the collected optical power, I is the injected current, and $V_p = h\nu/q$ is the photon voltage. The ratio V_p/V_{app} accounts for ohmic losses and is particularly relevant in assessing the influence of increased sidewall area and modified current spreading in planar and perforated devices. In all cases, current density was calculated using the full mesa area to ensure a consistent comparison across device sizes and architectures.

B.3 FDTD Simulations

We evaluated the optical extraction characteristics of planar and perforated InGaN/GaN μ LEDs using three-dimensional finite-difference time-domain (FDTD) simulations in Lumerical, following the dipole-based methodology of Ryu *et al.*[38]. The simulated device stack comprised an Ag bottom reflector, a 100 nm p-GaN layer, a 50 nm-thick InGaN/GaN MQW active region represented using an effective refractive index, and a 3 μ m n-GaN overlayer. The LED mesa was embedded in a homogeneous surrounding medium with refractive index $n = 1.5$ to approximate epoxy encapsulation. Perfectly matched layers were applied on all simulation boundaries.

Spontaneous emission was modeled using an electric dipole source placed at the center of the MQW plane and excited with a Gaussian spectrum centered at 450 nm with a 20 nm full width at half maximum. Only in-plane dipole orientations were considered, consistent with the predominantly transverse-electric emission of InGaN quantum wells.[38] For each dipole position, both X- and Y-polarized dipoles were simulated and averaged to obtain polarization-independent results. A schematic of the simulated structure is shown in Fig. 4.3(a).

To capture spatial variations in extraction, dipole sources were distributed over symmetry-reduced grids: 4×4 for the 10 μ m and 15 μ m devices, and 5×5 for the 20 μ m devices. Because spontaneous emission is incoherent and the device geometry is symmetric, these sampled points can be mapped to the full device area via quadrant reflection without introducing interference artifacts. This symmetry-expanded sampling yields effective dipole arrays of 7×7 (10 μ m, 15 μ m) and 9×9 (20 μ m) points. Any dipole locations that mapped into air-hole regions were excluded.

The perforated μ LEDs contained cylindrical air holes of radius 1.35 μ m on a 5.6 μ m pitch, arranged as 1×1 (10 μ m), 2×2 (15 μ m), and 3×3 (20 μ m) arrays to match the experimentally fabricated devices. The air holes extended vertically through the full epitaxial stack, from the p-GaN/reflector interface to the top of the n-GaN layer.

The LEE was calculated using Lumerical's analytic dipole power normalization, which compares the total outward radiated power collected by a closed monitoring surface surrounding the LED to the analytically computed dipole injection power. As a consistency check, a secondary numerical normalization based on a small enclosing flux box surrounding the dipole was also evaluated and yielded comparable trends.

In addition to total extraction efficiency, the far-field radiation characteristics of selected planar and perforated μ LEDs were evaluated. Near-field electromagnetic fields were recorded on a planar monitor above the device and transformed to the angular far field

using Lumerical’s built-in near-to-far-field projection. Far-field intensity distributions were extracted at the peak emission wavelength of 450 nm. For each dipole position and polarization, two-dimensional angular intensity maps were obtained and subsequently symmetry-unfolded and incoherently summed over all dipole positions and both in-plane polarizations to reconstruct the full-device far-field radiation pattern. One-dimensional angular cuts were also extracted along the central emission plane for comparison with Lambertian emission profiles.

To explore the influence of perforation geometry on optical extraction, a parametric design-of-experiments (DOE) study was performed on 10 μm μLEDs by sweeping the hole pitch and fill factor. In these simulations, a single in-plane dipole was fixed at the center of the MQW region to reduce computational cost while preserving the dominant extraction trends. For each geometry, the maximum even-numbered hole array that could be accommodated within the LED mesa was automatically generated, ensuring that no air hole coincided with the dipole location. The LEE, Purcell factor, and directional power components were calculated using the same spectrally averaged normalization procedure as in the spatially averaged simulations. While these DOE simulations do not capture spatial variations in emission, they serve to identify robust trends and optimal regions in the geometric design space, which were subsequently examined using the more comprehensive spatial and far-field simulation frameworks described above.

Appendix C

Details of materials and methods from Chapter 5

C.1 μ LED Fabrication

Commercially available blue InGaN-based LED epitaxial heterostructures with an emission wavelength of approximately $\lambda_{\text{emission}} = 445 \text{ nm}$, grown on 4" double-side-polished planar (unpatterned) sapphire substrates, were obtained from SemiLEDs Corporation. The wafers were initially cleaned in piranha solution prior to device processing.

Transparent p-type contacts were formed using a Ni/Au/low-damage ITO/ITO stack (2/1.5/10/70 nm), corresponding to ITO type 4 as described in Section 2.4. Prior to metal deposition, the wafer was treated in a 1:1 HCl solution for 10 min to remove native oxides. The Ni/Au layers were deposited by electron-beam evaporation (Angstrom Engineering) at a rate of $0.1 \text{ \AA/s}$, followed by sputter deposition of the ITO bilayer using an AJA system. The p-contacts were patterned lithographically and defined using a dual wet-etch process comprising a 10:1 HCl etch for the ITO bilayer and a diluted Transene TFA gold etchant for Au. The p-contact radius was consistently defined to be approximately $1.7 \mu\text{m}$ smaller than the corresponding μLED mesa radius. The contact stack was annealed at 550°C for 2 min in an N_2/O_2 ambient. c-TLM measurements performed at six locations across the wafer yielded a specific contact resistivity of $\rho_c = 3 \times 10^{-3} \Omega \cdot \text{cm}^2$.

Unless otherwise specified, the contact resistivities reported in this appendix were measured using in-line c-TLM structures fabricated on the same wafer as the μLED devices. These values therefore represent the specific Chapter 5 device fabrication run. The annealing time was reduced from the 5 min used during the dedicated contact-development

experiments in Chapter 2 to 2 min because the shorter treatment was found to be sufficient for obtaining low-resistivity ohmic contacts.

Mesa definition employed a two-step SiO₂ hard-mask process. A 600 nm-thick PECVD SiO₂ layer was deposited and patterned by standard photolithography, followed by ICP reactive-ion etching (ICP-RIE) using a Cl₂/BCl₃ plasma (Oxford Instruments PlasmaPro 100 Cobra). The first etch step reached a depth of approximately 1.5 μm , terminating in the n-GaN layer. Post-etch treatment in KOH at room temperature was used to remove plasma-damaged and crystallographically less stable GaN from the mesa sidewalls and promote the formation of relatively stable, locally smooth nonpolar facets.[28, 43] The overall mesa perimeter consequently remained macroscopically faceted rather than geometrically smooth. A second 600 nm SiO₂ hard mask and ICP etch defined a deeper surrounding mesa with a total etch depth of approximately 3.5 μm , leaving roughly 1 μm of unintentionally doped GaN (u-GaN) in the field region. Residual SiO₂ was removed using BOE, and all exposed GaN surfaces were rinsed in a 1:1 HCl solution prior to metallization.

N-type contacts consisting of Cr/Al/Ni/Au (5/100/30/100 nm) were deposited by electron-beam evaporation, patterned by metal lift-off, and annealed at 550 °C for 2 min in an N₂/O₂ ambient to form ohmic contacts. C-TLM measurements performed across the wafer yielded a specific contact resistivity of $\rho_c \approx 5 \times 10^{-6} \Omega \cdot \text{cm}^2$. P-type c-TLM measurements on the ITO contact stack were repeated following n-contact annealing, with the subsequent anneal resulting in a negligible change in ρ_c .

The processed wafer was diced into 25 $\times$ 25 mm² chips. To suppress surface recombination and planarize the device topography, an SU-8 overcoat was deposited and lithographically patterned to open vias to the p- and n-contacts. A brief O₂ plasma treatment was used to ensure complete via opening, followed by curing at 200 °C for 20 min. The device set comprised planar circular μLEDs with diameters ranging from 5 to 500 μm . Following SU-8 processing, probing pads were defined using an Al/Cr/Au (500/30/100 nm) metal stack deposited by lift-off.

The final device structure is depicted in Figure C.1 as a cross-sectional schematic. For preliminary transfer and handling experiments, simpler test structures were fabricated on the same epitaxial material. These devices consisted of single-mesa μLEDs with SiO₂ passivation and basic Cr/Au p- and n-contacts, omitting SU-8 planarization and multi-level mesa definition, and were used solely to evaluate transfer feasibility rather than final device performance.

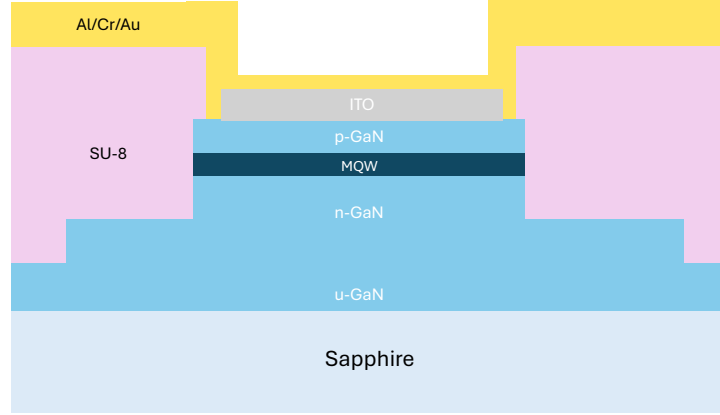


Figure C.1: Cross-sectional schematic of the fabricated device structure showing the layered stack comprising SU-8 overcoat, ITO p-contact, Al/Cr/Au metal pads, MQW active region within p-GaN and n-GaN, u-GaN, and the sapphire substrate.

C.2 μ LED Transfer

Processed μ LEDs chips were diced into smaller chips with typical dimensions ranging from $5\text{ mm} \times 5\text{ mm}$ to $10\text{ mm} \times 10\text{ mm}$. Initial bonding was performed using a semiconductor-grade two-part epoxy (EPO-TEK® 301-2FL, Epoxy Technology Inc.). The diced μ LED samples were bonded to a glass carrier substrate coated with a light-absorbing layer (LAL) using the epoxy. The bonded stack was cured on a hotplate at 80°C for 3 hours.

Following carrier bonding, the double-side-polished sapphire substrate used for GaN epitaxial growth was removed using laser lift-off.[8] A KrF excimer laser operating at 248 nm (MLASE), integrated into a ProMaster laser system (Optec, Belgium), was employed for this process. A laser fluence of approximately 400 mJ cm^{-2} was rastered across the bonded device area to induce localized decomposition of GaN at the GaN–sapphire interface. Ultraviolet laser irradiation induces decomposition of GaN at the GaN–sapphire interface into metallic gallium and nitrogen gas, enabling separation of the sapphire growth substrate.

After sapphire removal, the backside of the GaN epilayer was exposed. Residual gallium metal was removed using a 1:1 hydrochloric acid solution for 1 minute. To further treat the exposed GaN surface, a KOH treatment was optionally performed at this stage. Samples were immersed in a 22% KOH solution for 15 minutes at room temperature, followed by thorough rinsing with DI water.

Final bonding to the target substrate was carried out using the same EPO-TEK® 301-2FL epoxy and curing procedure. For flexible devices, the LEDs were ultimately transferred onto a 125 μm thick polyethylene naphthalate (PEN) substrate. The final transfer was achieved using a photonic assisted transfer process (PATP). PATP employs sub-millisecond pulsed broadband light from a high-instantaneous-power flashlamp tool (PulseForge® PD300SA, PulseForge Inc., USA) to selectively heat the adhesive interface between the LED stack and the carrier substrate. Each optical pulse had a duration of approximately 300 μs and delivered peak radiant intensities of up to 45 kW cm^{-2} over a broadband spectrum spanning 200 nm to 1100 nm.

The illuminated area exceeded 100 cm^2 , and large-area processing up to 60 $\text{cm} \times 60 \text{ cm}$ was enabled through rastering with a motorized stage synchronized to the flash sequence. This wafer-scale transfer approach provides high throughput and is compatible with scalable manufacturing. A detailed description of the PATP process and associated tooling has been reported previously by Schroder et al.[62] Following final transfer and removal of the glass and LAL substrate using the PATP process, the epoxy originating from the initial carrier bonding step was etched away in a reactive ion etching system using an O_2/CF_4 plasma until the underlying device layers and metallic contact pads of the individual μLEDs were exposed.

C.3 Device Characterization

Devices were characterized through combined optical and electrical measurement techniques. For characterization, each LED device on a sapphire substrate was positioned atop a silicon photodiode detector (Thorlabs FDS1010) with a known responsivity curve, capturing emitted light through the sapphire substrate. For flexible samples, the polymer substrate supporting the transferred μLEDs was likewise placed directly on the photodiode during absolute efficiency measurements, ensuring identical optical collection conditions. Electrical connections were established by probing the μLEDs inside a blackout

Faraday cage to eliminate external electrical and optical interference. Both the photodiode and the μLEDs were connected to a Keithley 4200A Semiconductor Characterization System parameter analyzer, capable of measuring currents down to the femtoampere level. The measurement involved performing an IV sweep of the diode while simultaneously recording the μLED optical output via the photodiode photocurrent, which was reverse biased to ensure linear response. The measured μLED current voltage characteristics and photodiode photocurrent were used to calculate the EQE and WPE. The μLED current

density was consistently calculated using the lithographically defined mesa area for all device sizes and sidewall passivation schemes.

Bending dependent optical measurements were performed using custom machined mechanical jigs designed to impose controlled concave and convex curvature (Figure C.2). The jig system consisted of a common base housing the photodiode, with interchangeable curved fixtures machined to a radius of curvature of 11 mm. In all bending configurations, the μ LED was located at the apex of the curvature, and the distance between the emitting surface and the photodiode active area was fixed at 6 mm. Flexible samples were secured to the curved fixtures using Kapton tape to ensure conformal contact and prevent mechanical slippage during bending. For efficiency measurements under bending, the emitted light passed through a precision-machined aperture in the jig, ensuring a fixed optical path before being collected by the photodiode. To ensure consistent optical collection geometry, all bending measurements, including the nominally flat reference case, were performed using the same jig assembly rather than direct placement on the photodiode.

C.4 Recombination Parameter Fitting

The recombination parameter fitting procedure using in Chapter 5 is similar to the procedure used in Chapter 3. More details on this can be found in Appendix A.4. The MATLAB code used to implement the global fitting procedure, together with example input data, has been made publicly available through Figshare.[42]

C.5 Spectral Measurements

Spectral measurements were performed using a Lake Shore TTPX probe station equipped with a Keithley 2400 source meter unit and an Ocean Optics spectrometer. The μ LEDs were electrically driven using the Keithley 2400, and the emitted optical spectrum was collected using an Ocean Optics FLAME T UV VIS ES spectrometer with a spectral range of 200 nm to 850 nm, coupled via a 600 μ m core polarization resistant optical fiber.

A CC 3 UV S cosine corrector incorporating Spectralon diffusing material was attached to the fiber and positioned in close proximity to the μ LED emission surface. This configuration minimized angular sensitivity and ensured consistent spectral collection across devices and measurement conditions. All spectral data were acquired under identical electrical bias and optical alignment conditions.

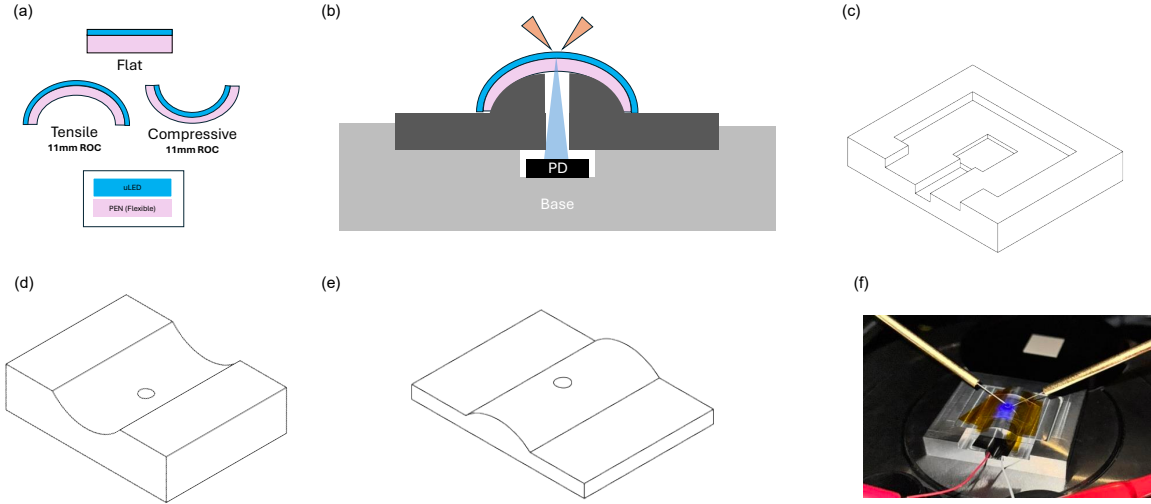


Figure C.2: (a) Schematic illustration of the mechanical deformation conditions applied to flexible devices, including flat, tensile, and compressive bending configurations, where blue represents the μ LED layers and pink represents the flexible substrate. (b) Schematic of the custom measurement jig showing the base, curved fixture (tensile configuration shown), mounted μ LED/flexible sample, probing configuration, and optical collection path (light blue cone) through an aperture to the photodiode (PD). (c) CAD schematic of the fabricated base platform. (d) CAD schematic of the compressive jig fixture with a radius of curvature of 11 mm. (e) CAD schematic of the tensile jig fixture with a radius of curvature of 11 mm. (f) Optical photograph of a μ LED on a flexible substrate assembled on the tensile 11 mm radius of curvature jig, electrically probed during operation, with the base, photodiode, and optical emission visible.

The measured emission spectra were used for relative comparison only. Accordingly, each spectrum was normalized to its peak intensity to allow comparison of spectral shape, peak wavelength, and linewidth across different devices and operating conditions.

C.6 Structural Characterization

The SEM images were taken using both a JSM-7200F JEOL and a SU5000 Hitachi microscope system. Both systems were equipped with a variable angle stage allowing for measurements at 35° tilt. An accelerating voltage of 5 kV was used for imaging.

Structural characterization was performed using a Bruker D8 Discover X-ray diffractometer equipped with a Dectris Eiger detector. Samples were mounted on a removable stage and centered using the integrated optical microscope to ensure measurements were acquired from the desired device region. Prior to data acquisition, the diffractometer was aligned by maximizing the incident beam intensity, adjusting the sample height (z -position) to center the sample within the beam, and optimizing the ω and 2θ positions corresponding to the target reflection.

GaN (002) XRC measurements were performed on samples at three stages of the transfer process: on the native sapphire substrate, immediately following laser lift-off (LLO), and after PATP transfer onto a rigid silicon carrier substrate. Rocking curves were acquired by scanning ω over a range of approximately 5° using a step size of 0.0005° and an integration time of 5 s per step. Following acquisition, background subtraction was performed using the Bruker analysis software, and the resulting data were used to extract the FWHM of each XRC peak.

C.7 FDTD Simulations

Three-dimensional FDTD simulations were performed using Lumerical FDTD Solutions to evaluate the LEE of planar and backside-roughened GaN/InGaN μ LEDs. The simulation methodology follows a full-chip, source-averaged approach that accounts for spatial, spectral, and polarization averaging of spontaneous emission.

The modeled device geometry corresponds to a $10\,\mu\text{m} \times 10\,\mu\text{m}$ square μ LED and comprises, from bottom to top, an Ag reflector ($0.5\,\mu\text{m}$), a p-GaN layer ($0.1\,\mu\text{m}$), a 50 nm InGaN/GaN MQW active region represented using an effective refractive index, and an n-GaN overlayer with a total thickness of approximately $3\,\mu\text{m}$. The μ LED chip is embedded in a surrounding medium with refractive index $n = 1.5$ to emulate typical encapsulation conditions. Perfectly matched layer (PML) boundary conditions are applied on all simulation boundaries to ensure an open electromagnetic domain.

Optical emission is modeled using a point electric dipole source placed at the center of the MQW region and excited with a Gaussian spectrum centered at 450 nm with a 20 nm FWHM. Only in-plane dipole orientations are considered, consistent with the predominantly transverse-electric polarized emission of InGaN quantum wells. For each spatial location, both X- and Y-polarized dipoles are simulated and averaged to obtain polarization-independent results.

To capture spatial variations in optical extraction, dipole sources are distributed over

a 7×7 grid within a symmetry-reduced quadrant of the active area. Owing to the incoherent nature of spontaneous emission and the geometric symmetry of the device, each simulated source position represents multiple equivalent locations within the full μ LED. When mapped across the complete device area, this sampling corresponds to an effective 13×13 grid, resulting in 169 spatial source locations. Accounting for the two orthogonal in-plane dipole polarizations, a total of 338 dipole simulations is represented for each device configuration.

LEE is defined as the ratio of the total optical power extracted through monitoring planes enclosing the device (top, bottom, and side surfaces positioned near the PML boundaries) to the analytically computed dipole injection power. The extracted optical power is spectrally weighted according to the source emission profile prior to normalization. The final LEE values reported in this work correspond to averages over all spatial source locations and both in-plane polarizations, providing a representative device-level metric. While the simulated geometry does not replicate every fabrication detail of the experimental devices, it captures the dominant optical interfaces and emission pathways governing photon escape; as such, it is well suited for relative comparisons of light extraction behavior between planar and backside-roughened configurations.

For the backside-roughened configuration, the exposed n-GaN surface was modeled using a statistically defined roughness layer implemented through a Lumerical structure group. The roughened region was represented as a three-dimensional, Gaussian-correlated height distribution applied to the top 100 nm of the n-GaN layer. The surface morphology was parameterized by a root-mean-square roughness amplitude of 5 nm and lateral correlation lengths of 90 nm in both in-plane directions. The rough surface profile was generated on a lateral grid with a spatial resolution of 20 nm, ensuring adequate sampling of the correlation length while maintaining numerical stability. A fixed random seed (seed = 12345) was used to generate the surface profile, enabling reproducibility of the simulated morphology.

The roughened region retained the optical properties of n-GaN and was positioned directly above a flat n-GaN base layer with a thickness of 2.85 μ m, yielding a total n-GaN thickness of approximately 2.95 μ m. To accurately resolve sub-wavelength field variations associated with the nanoscale roughness, a local mesh override was applied across the roughened region with lateral mesh steps of 20 nm and a vertical mesh step of 2 nm. This statistical roughness model does not attempt to replicate the exact etched topography of the fabricated devices; rather, it provides a controlled and physically representative means of introducing backside surface disorder to evaluate its impact on optical mode redistribution and light extraction behavior.