Image Sensor Pixel Integration for Large Area Imaging

by

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Abstract

This thesis examines the various issues underlying integration of Mo/a-Si:H image sensor with inverted-staggered thin film transistor (TFT) for large area digital x-ray imaging applications.

The thin film transistor process has been modified to include a highly doped (n^+) microcrystalline silicon (μc-Si:H) film as the contact layer in the source and drain regions. The deposition temperature of the n^+ μc-Si:H film is varied from 200°C to 400°C to observe the crystalline and amorphous phase formations in these films. The results show that the films deposited at low temperatures are more crystalline in nature than their high temperature counterparts.

A comparison of the performance of aluminium (Al)-gated thin film transistors is presented in which the process parameters are varied in terms of the sputter deposition temperature, process pressure, and power. Gate films deposited at 30°C/5mTorr/300W yield TFT characteristics with low leakage current (~ 10 fA at low V_{DS}), an ON/OFF ratio better than 10^8, and a mobility of 1.1 cm^2/Vs. In contrast, films deposited at 150°C/10mTorr/400W, yield a significant degradation in leakage current (~ 1 pA) and mobility (0.77 cm^2/Vs). The degradation stems from the high surface roughness of the a-SiN:H gate insulator, and hence the TFT channel.

Two different pixel integration processes for direct x-ray detection are studied. In one process, the Schottky diode is stacked on top of the TFT. In the other process, the two devices did not overlap. The two processes are compared in terms of mask count and pixel performance. Fully-overlapped and partially-overlapped pixel structures provide high fill factor, but suffer from the stresses due to multi-layers. In addition, the TFT leakage current of a fully-overlapped pixel is very high (~10^{-7} A), due to parasitic capacitance. The partially-overlapped structure also suffers from high stress, however,

the leakage current is considerably lower and comparable to that of a discrete TFT. The stress is not as severe in the non-overlapping structures. Also, the leakage current is of the order of 100fA.

The high intrinsic film stress associated with the stacked pixel structures has been further investigated. It is shown that the high compressive stress of Mo film ($\sim 10^9$ Pa) can be reduced to $\sim 10^7$ Pa by varying the deposition process parameters without seriously undermining the physical and electrical properties of the films.

A small-scale (4 rows x 5 columns) teat array has been designed and characterized. The results show that several technical challenges need to first be solved before extending the design to a larger array for x-ray image generation. The most outstanding challenge is to improve the uniformity of the Schottky diode interface.

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Chapter 1

Introduction

1.1 Background History of Amorphous Silicon

Hydrogenated amorphous silicon has become the material of choice in semiconductor technology, particularly in solar cells construction and active matrix display industries [1, 2, 3, 4, 5, 6, 7, 8]. The most outstanding attribute of amorphous silicon technology is its large area capability [7, 8]. Although the material contains defects that are associated with "no long-range order" crystalline structure [1, 2, 3], it still possesses all the requisite properties for semiconductors, such as doping, photoconductivity, and junction formation [4, 5, 6].

In the 1960s, when the physicists first turned their attention to the differences between the electronic states of amorphous and crystalline semiconductors, they found that evaporated or sputtered pure silicon had a very large defect density [1]. At the time, it seemed impossible to use amorphous silicon as a semiconducting material. It was not until the late 1960s when amorphous silicon was deposited from silane plasma for the first time by Dr. Chittick's group [2], and later on by Dr. Spear's group in the early 1970s, that the plasma deposited material had greatly improved semiconducting

properties [3]. It was then discovered in the mid 1970s that the improved properties were the result of hydrogen incorporation, which removed the electronic states in the band gap by binding hydrogen atoms to the dangle bond defects, thus eliminating the trapping and recombination centers [4]. Also in the mid 1970s, physicists discovered that amorphous silicon could be doped. The addition of phosphine or diborane to the silane plasma lead to n-doped or p-doped amorphous silicon films, respectively [5, 6]. The ability to control the location of the Fermi level in the band gap, along with the good photoconductivity of amorphous silicon, led to solar cell application in the late 1970s [7]. After the first thin film transistor was deposited in 1978 with a silicon nitride film from silane and ammonia gas mixture in the plasma chamber, display and imaging industries started to develop active TFT matrix arrays [8]. Since then, the rapid development of the active matrix liquid crystal display for laptop computer screens has allowed for advanced two-dimensional imaging arrays. One of the recent advanced imaging applications is the imaging of x-rays which will ultimately replace current conventional x-ray film.

1.2 Motivations

The main objective of this work is to investigate the production feasibility of a large-area flat panel x-ray imaging array with hydrogenated amorphous silicon technology. The x-ray imaging array can replace the conventional screen films used for radiography (ex. chest x-ray and mammography).

The main advantages of digital radiology include the following:

(i) Fast turn around time. In a simple case of biopsy, doctors will no longer have to wait for several iterations of the 20-minute long film development cycle just to see if the end of the needle has reached the desired area in the body [9].

(ii) Improved image visualization. For example, the contrast between images is enhanced, which allows for more accurate diagnoses [10].

(iii) Assistance in finding subtle abnormalities [11, 12].

(iv) Easy electronic storage and retrieval.

(v) Remote viewing. With the advances in internet and wireless communications, doctors can view the image from remote places. It also facilitates tele-conferencing.

1.3 Advantages of a-Si:H technology

Hydrogenated amorphous silicon offers a suitable platform for medical x-ray imaging over other process technologies, such as CCD or CMOS technologies. The most outstanding advantages of a-Si:H are:

(i) the capacity to inexpensively deposit films of uniform thickness over a large area [13, 14];

(ii) resistance to radiation damage [15];

(iii) optical band gap of 1.7eV;

(iv) low temperature deposition capability with plasma-enhanced chemical vapor deposition (PECVD) technique;

(v) little constraint on substrate material; and

(vi) low leakage current of a-Si:H devices due to low conductivity.

The low device leakage current will be discussed in greater detail in the main body of this thesis. The main driving force of the a-Si:H flat panel array is the active matrix liquid crystal display (AMLCD) industry. In each pixel of the array in this application, there is a thin film transistor (TFT) whose function is to locally switch the pixel on and off, hence the term "active." The light-emitting device in the flat display panel can be replaced with any type of photo sensors – in this project, x-ray sensors – to convert the active matrix display array to an x-ray imaging array.

1.4 X-ray Detection Schemes

1.4.1 Indirect Detection Scheme

One method to detect x-rays using a-Si:H technology is to convert the radiation into visible light in an intermediate (phosphor) layer, then detect the visible light with a-Si:H photosensors (Fig. 1.1). Since 1985, there have been a number of reports on the fabrication and testing of x-ray imaging arrays, most of which rely on the indirect detection mechanism [15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25]. One of the research groups working on this scheme is *dpiX, LLC* in Palo Alto, CA. *dpiX* manufactures a-Si:H image sensor arrays with pixel sizes from 127μm to 392μm and image formats from 20cm x 25cm to 30cm x 40cm in area. These arrays are supplied with a coating of cesium iodide, used as an x-ray scintillating layer. The commercially available array is then assembled into a complete imaging system. Following this, gate driver and readout amplifier circuit boards are connected to the array. Moreover, the electronics on the array is designed for radiographic imaging in which the frame time is greater than 3 seconds [25]. This array is reported to have a noise level of approximately 0.3fC and the maximum signal of 3 pC [26], which allows a potential dynamic rage of ~10000. High

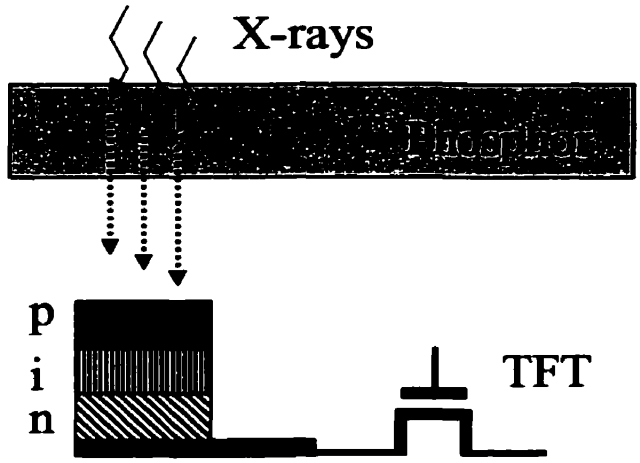


Figure 1.1: Indirect x-ray detection method, based on combination of a phosphor layer and an a-Si:H image sensor.

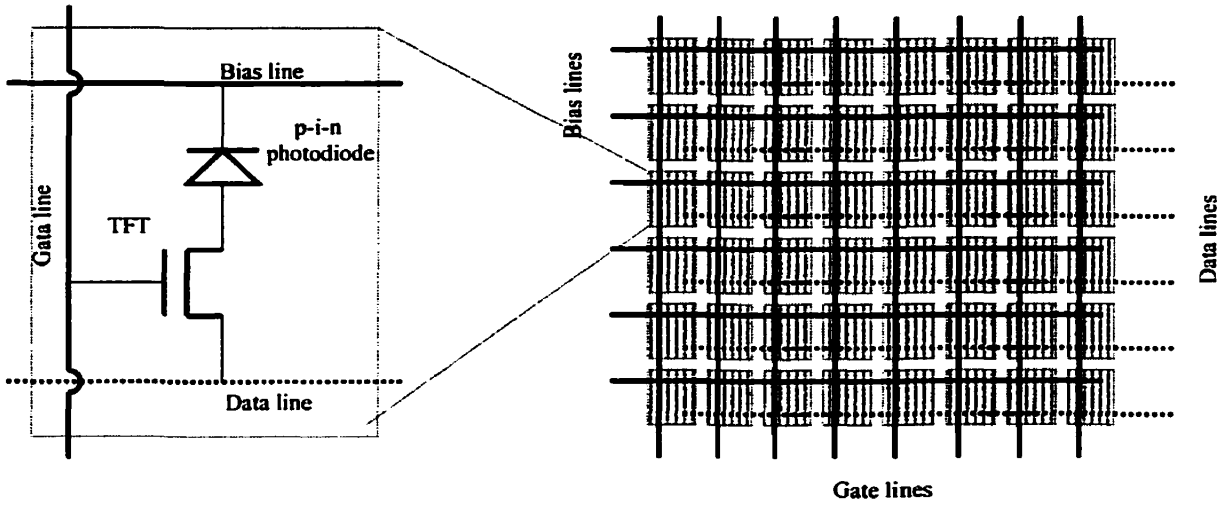


Figure 1.2: Pixel circuit schematic diagram of indirect x-ray detection array. Each pixel contains a p-i-n photodiode to capture the visible light emitted from the phosphor layer and a TFT to make the array gate-addressable.

dynamic range and low noise are essential figures of merits for large area imaging electronics [26]. Figure 1.2 illustrates the pixel schematics of this indirect detection method along with a simplified drawing of the array layout.

The medical imaging is performed either in radiographic mode or fluoroscopic mode. In the radiographic mode, the imager captures a single image in response to a brief x-ray exposure. The requirements for radiographic imagers are a large-area, a high resolution and a high dynamic range [26]. In the fluoroscopic mode, the imager has to capture a continuous real-time sequence of x-ray images at a rate of at least 15 frames per second [26]. The most outstanding requirement for fluoroscopic arrays is speed, which is largely dependent on the performance of the TFTs in the array [13]. The requirement for high speed switching, meaning fast data transfer, will be discussed in details in section 2.1.

The efficiency of indirect x-ray detection is determined by a number of factors, e.g., the efficiency of conversion of x-ray photons to visible light, the efficiency of the photodetectors in converting the visible light to a useful electrical signal, and fill factor [14, 18, 19, 25]. This scheme has been reported to yield good results at relatively high x-ray energies. However, at low energies, the detection efficiency is not as high [25]. This technological difficulty does not appear to be an issue in the direct detection scheme. This idea will be further explained in the following section.

1.4.2 Direct Detection Scheme

Alternatively, a direct detection scheme can also be employed (Fig.1.3). This scheme requires thick (300 ~ 500μm) vapor-deposited amorphous selenium (a-Se) layers [27, 28, 29]. In this method, x-ray photons are absorbed in the a-Se layer, where their radiation energies are transferred to the generation of electron-hole (e-h) pairs.

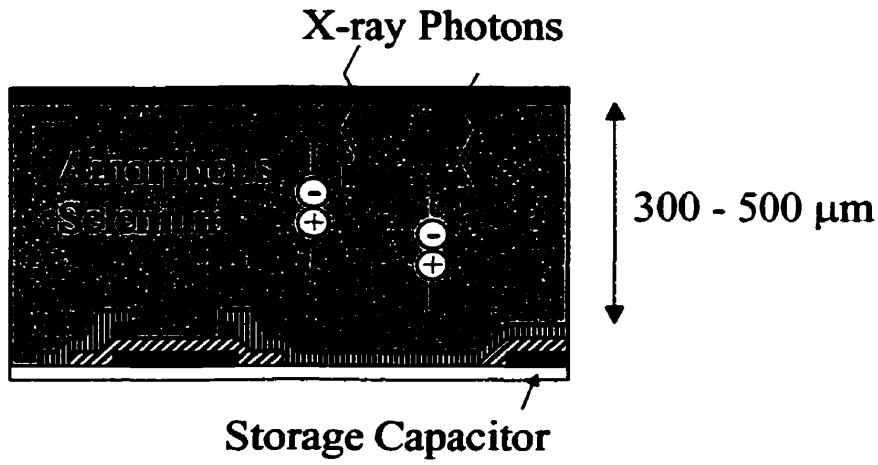


Figure 1.3: Direct x-ray detection method using a thick vapor-deposited amorphous selenium layer.

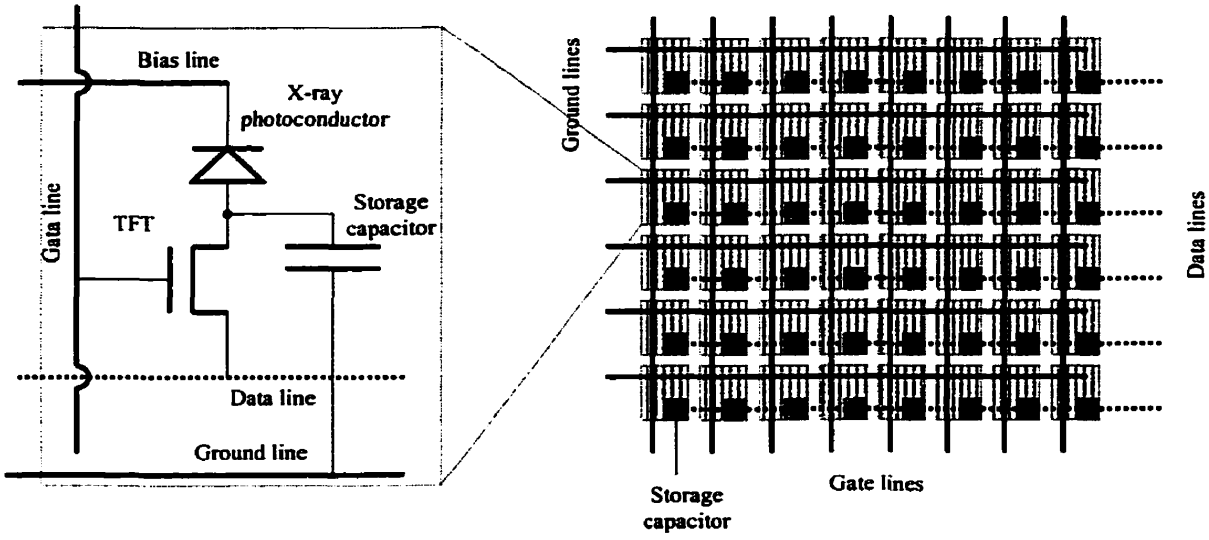


Figure 1.4: Pixel circuit schematic diagram of direct x-ray detection array. Each pixel contains a storage capacitor to keep the charge generated by x-rays. The selenium layer is continuous over the entire detection area. The bias line is not shown in the simplified array layout.

Subsequently, the e-h pairs are separated by an applied electric field and collected to form the signal. Our collaborator, Dr. J Rowlands' group at Sunnybrook Hospital of the University of Toronto, has successfully produced x-ray images using a-Se as the x-ray photoconductor [11, 27, 28]. The design of a direct detection array is very similar to that of the indirect array. It consists of a two-dimensional array of TFTs (Fig. 1.4). The major difference here is that, in this design, an additional storage capacitor is required. A storage capacitor is made by overlapping the pixel electrode with either adjacent gate line or a separate ground line. Radiation detection is accomplished with a uniform layer of x-ray sensitive photoconductor deposited on the active matrix (see Fig. 1.3). The top surface is a continuous high voltage bias electrode which is used to apply an electric field across the photoconductor. When electron-hole pairs are created by the x-ray photons, they are then separated by this applied electric field. The storage capacitor collects the charge generated and holds it until the gate of the TFT is turned on.

The direct detection method offers advantages in resolution and efficiency [27, 28]. Moreover, they do not depend on scintillation layers. However, despite the potentially high resolution of these image sensors, the thick selenium layer introduces difficulties in the collection of the generated charges [28]. A strong electric field is required to separate the e-h pairs, which is achieved by applying a high bias voltage (4 ~ 10kV). Furthermore, charge trapping in the a-Se layer can lead to an image lag, which reduces the frame rate of the imaging array [27].

1.4.3 Detection Scheme of This Study

In 1997, α-sidic group has developed the design, fabrication, and characterization of a direct-conversion x-ray detector based on Molybdenum (Mo)/a-Si:H Schottky diode for low-energy x-rays [30, 31]. In this diode, the interaction of x-ray photons with Mo leads

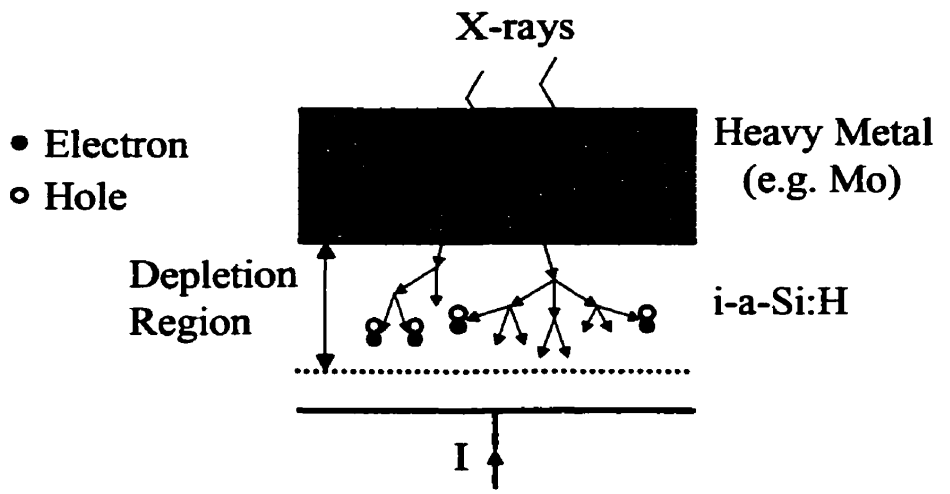


Figure 1.5: X-ray detection scheme based on Mo/a-Si:H Schottky diode.

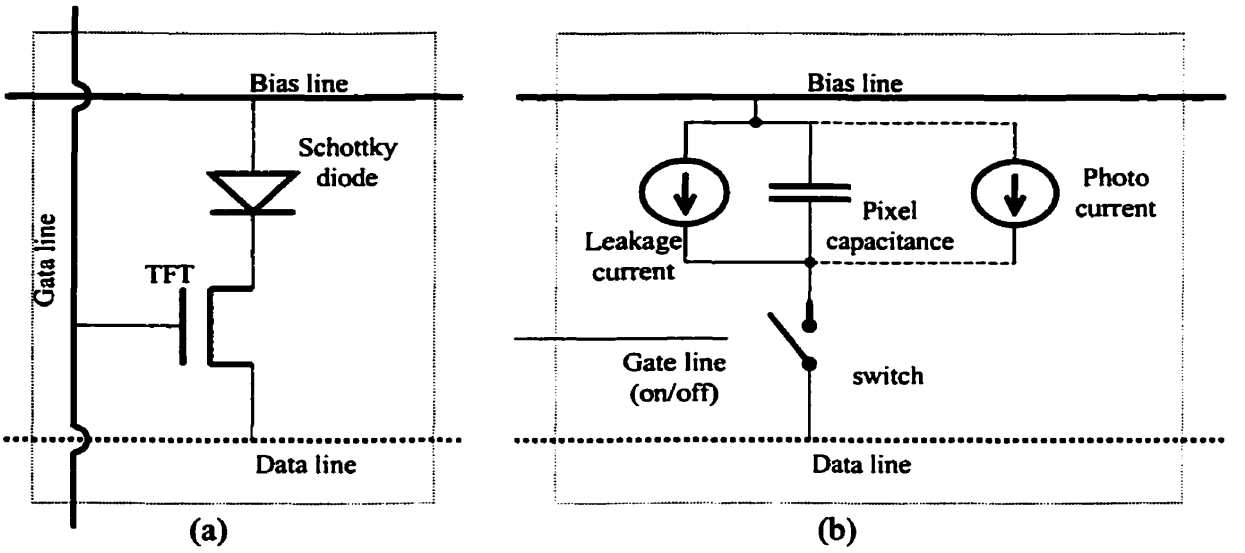


Figure 1.6: Direct detection x-ray imaging pixel based on a-Si:H/Mo Schottky diode as a detector. (a) Circuit schematic diagram. (b) Equivalent circuit diagram

to injection of high energy electrons, by virtue of the photoelectric effect, into a reverse-biased a-Si:H depletion layer, where electron (avalanche) multiplication yields a gain (Fig 1.5). The e-h pairs are then separated by the electric field inside the depletion region of the reverse-biased Schottky diode, thereby producing the output signal. The array layout is essentially identical to that of indirect detection array shown in Fig. 1.2.

The pixel operation can be described with the equivalent circuit diagram shown in Fig. 1.6b). The TFT is represented by a switch that is controlled by the gate signal. The Schottky diode can be represented by a capacitor to model the internal pixel capacitance and a current source to model the leakage current of the diode. With the gate signal at "off" and the bias line at a negative voltage, for example –4V, the internal pixel capacitance is not fully charged and the other side of the capacitor is at a voltage level higher than –4V, for example –1.5V. Without x-rays only a small charge is transferred to data line when the gate is turned on. If incidence x-ray photons are present while the gate is turned off, the x-ray can be modeled by an additional current source parallel to the pixel capacitor and the leakage current source. For simplicity, assume that there is a high dose of x-ray, which fully charges the internal pixel capacitance. There is now a strong conductance between the two sides of the capacitor. The opposite side to the bias line of the capacitor is close to –4V. When the gate is turned on, assuming that this charge is retained despite the leakage current of the TFT, a large charge is transferred to the data line. The difference, according to data line, is the dynamic range of the pixel.

At low bias operation (< 4V), the detector yields a sensitivity of approximately 10^8 electrons over x-ray energies in the range of 40 ~ 100 kVp [30, 31]. The fabrication process of this diode is fully compatible with that of an a-Si:H TFT, which is intended to be used as a switch for charge readout.

The performance of this detection method depends on the quality of the Schottky interface. The silicon/metal interfaces in p-i-n photodiode form ohmic

contacts, since the silicon is heavily doped near the interfaces. A Schottky barrier junction includes an abrupt termination of the semiconductor crystal. The silicon surface contains interface states due to incomplete covalent bonds, which can lead to trapped charges at the metal-semiconductor interfaces. This property of the Schottky diode will be further discussed in Chapter 3 as a discrete device and in Chapter 6 as in a fixed pattern noise within an array.

1.4.4 Comparisons of Different Detection Schemes

The three different x-ray detection schemes that were discussed in the previous sections have their own advantages and disadvantages [9 – 31]. The ultimate objective for the design of an detection scheme is to optimize the performance of the detector in terms of its ability to capture and digitize the information content of the incident x-rays. Thus, it is important that the different detection schemes be compared for their performance, cost and complexity in fabrication processes. It is not feasible to compare these detection schemes in terms of quantitative figures since no x-ray images have yet been successfully captured with a-Si:H/Mo Schottky diodes. But based on the information from the published literatures, and the results produced from our laboratory, the different detection schemes can be compared qualitatively (Table 1.1).

1.5 Thin Film Deposition

The devices made in this work are composed of thin films. There are a number of ways that thin films can be deposited. Major deposition techniques are categorized in Table 1.2. Of all these available deposition techniques, an engineer should be able to determine which methods to use based on the following considerations.

Detection scheme	Indirect detection scheme using a scintillating layer to convert the x-ray photons to visible light then process the visible light with p-i-n photodiode.	Direct detection scheme employing a thick (~500nm) a-Se layer as detector. The a-Se layer is deposited by evaporation over the entire array.	Direct detection scheme with a-Si:H/Mo Schottky diode as the x-ray detector. The diode is reverse biased by a small voltage.
Signal gain and charge collection	Since the x-ray photons are converted to visible light, p-i-n diodes do not exhibit a large gain. The efficiency of the p-i-n photodiode is ~75% [16]. At a reverse bias of –8V, the charge collection efficiency is nearly 1 [14].	Although energetic electron created by x-ray photons generate a gain ($g(E) = E/W$, E is the x-ray energy and W is the energy required to generate a electron in a-Se.) [28], due to the poor charge collection, not all electrons get stored [27].	According to [30, 31] the gain is ~1000 over the x-ray source voltage range of 40kVp – 100kVp. The charge collection efficiency should be close to that of the p-i-n diode. The effect of the leakage current will be discussed in Chapter 3.
Image spreading	The p-i-n diodes array does not spread the image. However, the conversion of x-rays emits visible light in	Even with the continuous a-Se layer, due to the large bias applied across it, the generated	Image spreading is not a concern in this design.

	all directions [13]. Anisotropic phosphors are becoming available.	electron-hole pairs travel vertically [11, 27, 28].	
Smallest pixel size	The smallest pixel size is largely limited by the anisotropy of the phosphor layer as well as its conversion efficiency [13]. The smallest pixel size is ~ 100μm^2.	Since the a-Se layer is continuous, pixel size is determined by the size of the TFTs. For mammography, the pixel can be as small as ~50μm^2. [27, 28]	The smallest pixel size is determined by the leakage current of the diodes. In Chapter 3, a diode as small as 26μm^2 will be observed.
Fill Factor	With isotropic light emission, a fill factor >50% does not improve the image quality [14].	Because the a-Se layer is covering the entire array, fill factor is 100% [9, 10].	In this design, fill factor is determined by the size of the TFT and line width. In Chapter 6, the arrays have ~45% fill factor. It can be as high as ~80% with vertical channel TFTs.
Additive noise	Along with any reduction in signal-to-noise performance generated by blurring and sampling stages, additional noise arises	The electronics to process an image are the same as in the indirect detection. The electronic noise per pixel is	Once the full imaging system is developed, the electronics associated with the detector will be the same as the other two.

	from the electronics such as amplifier noise. The electronic noise per pixel is approximately 1000 electrons [13].	approximately 1000 electrons [27]. There is an additional shot noise caused by thermal excitation of charge carriers in a-Se layer.	

Table 1.1: Comparisons of the difference x-ray detection scheme.

	Mechanism: Physical → Chemical		
Medium: Plasma	Sputtering	Reactive Sputtering	Plasma-assisted chemical vapor deposition
Vapor	Evaporation	Reactive evaporation	Chemical vapor deposition
Liquid	Spinning or preying	Particle plating	Plating anodization
Solid	Diffusion	Ion implantation	Case-hardening

Table 1.2: Various thin film deposition techniques [32].

(i) The appropriate deposition rate for the required thickness, purity and production rate.

(ii) The effects on substrate in terms of heat, ion bombardment, etc.

(iii) Reliability and lifetime requirements.

(iv) Affordability.

The family of silicon films can be easily deposited by the CVD process whereas the metals films can be deposited by the PVD process. Both processes allow for the films to be deposited at a low temperature, <400°C, which is the temperature that the substrate glass, Corning 1737, starts to soften. The CVD process is well-known [32] for its conformal coverage of the substrate profile (Fig. 1.7a). This is a very useful property of CVD process when wet etch processes are used and the protection layer is a thin insulating layer, such as silicon nitride. However, the PVD process covers only the top surfaces. Vertical profiles do not get covered by films deposited by the PVD process, which can lead to uncovered and exposed surface (Fig. 1.7b). The effect of this step coverage will be shown in Chapter 3 as a part of the Schottky diode device performance.

(a) (b)

Figure 1.7: Surface coverage of tin film processes (a) CVD process. (b) PVD process.

1.5.1 Plasma Enhanced Chemical Vapor Deposition

For the thin film device fabrication, two plasma enhanced chemical vapor deposition (PECDV) chambers are available, namely PlasmaTherm VII (Fig. 1.8) and Oxford

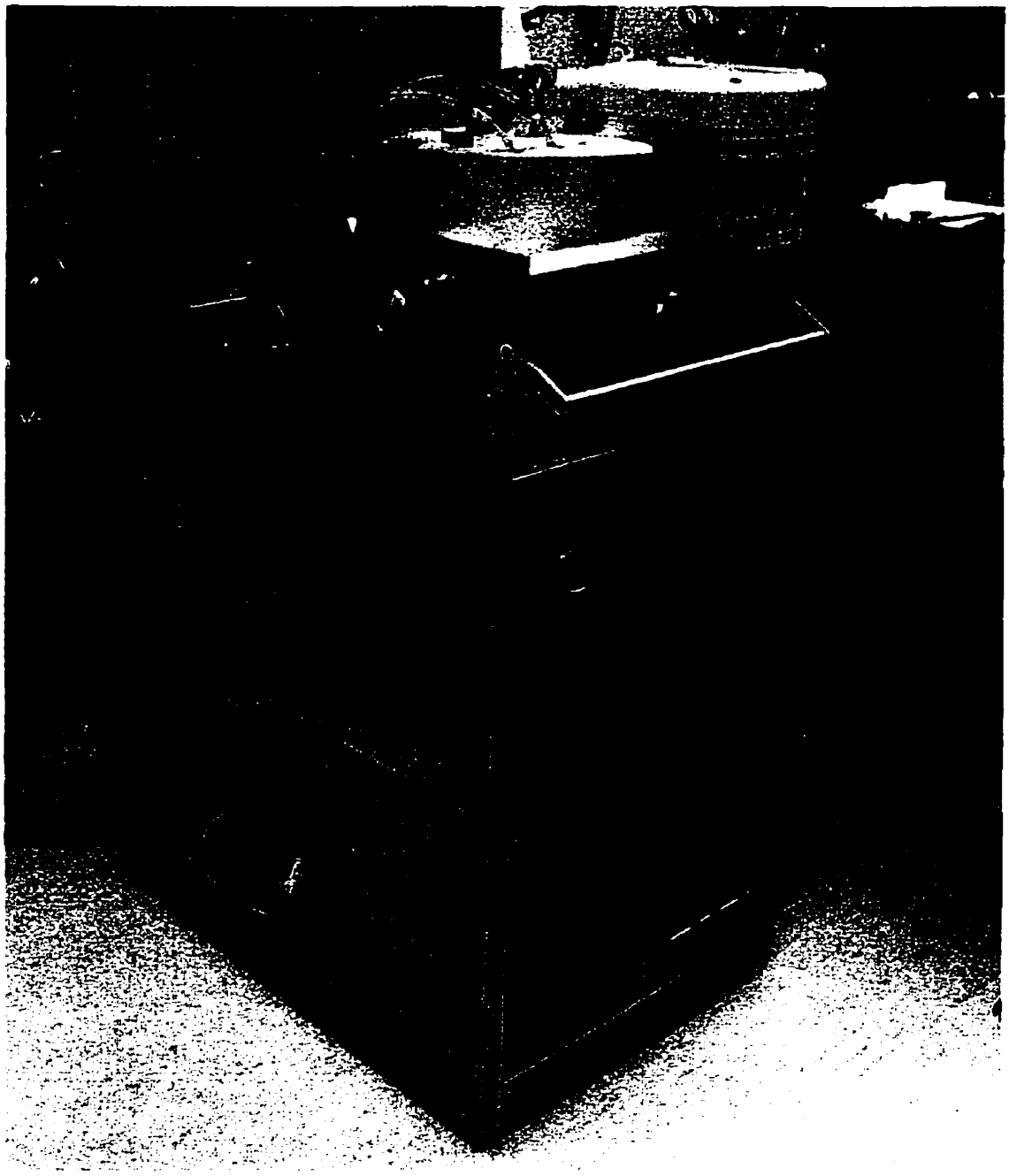


Figure 1.8: PlasmaTherm VII parallel plates PECVD system for thin film depositions.

PECVD systems. Both systems have a parallel plate reactor chamber. The advantage of PECVD system over low pressure CVD (LPCVD) system is that the deposition temperature can be lowered due to the RF power being applied to the parallel plates, which help dissociate the source gas molecules (Fig 1.9). The PlasmaTherm VII system is used for depositions of intrinsic amorphous silicon layer, n^+ doped amorphous silicon layer, and silicon nitride layer. This chamber is used for the tri-layer deposition of TFT (Chapter 2) and active layer in the Schottky diode (Chapter 3). The Oxford PECVD system is mainly used for n^+ doped microcrystalline silicon layer (Chapyer 2), which serves as the contact layer in TFTs. Chemical vapor deposition is the reaction or decomposition of gases flowing over a heated substrate, leaving behind a solid film as a reaction product. When the source gas, for example, silane, enters the PECVD chamber and the RF power is applied on the parallel plates, the source gas molecules dissociate

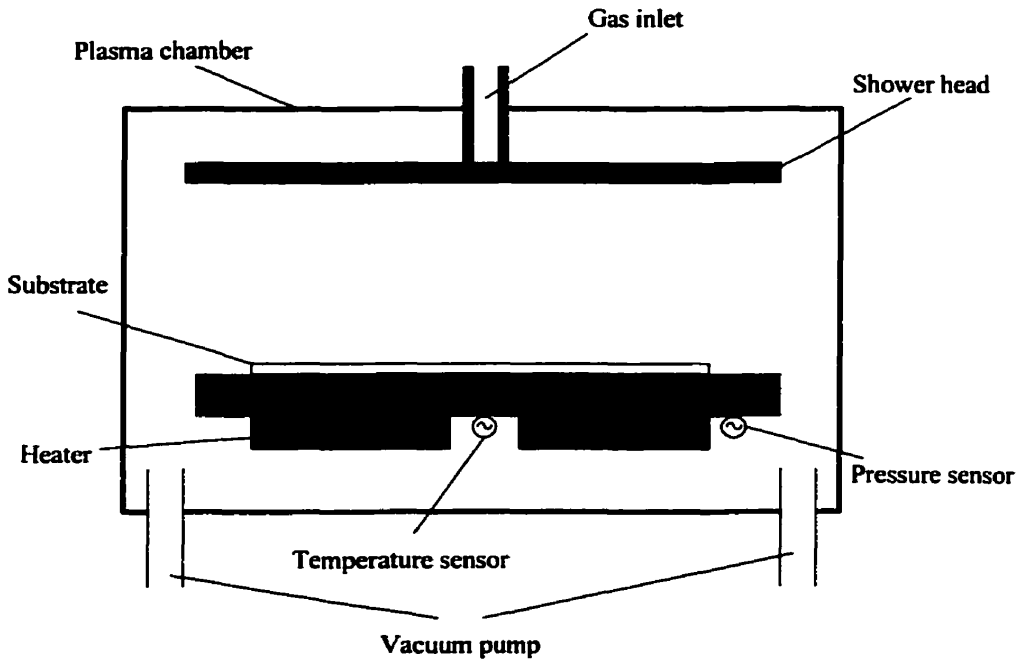


Figure 1.9: A simplified cross section view of the PECVD chamber. Only the most vital components are shown.

into silane radicals such as SiH_3, SiH_2 and SiH. Unfortunately, the exact plasma chemical balance equations are still not discovered. But the products of such plasma reactions are thin films which compose thin film devices that are being used everyday. Chapter 2 will examine the CVD plasma deposition process for microcrystalline silicon films in an attempt to explain why crystallization happens at low deposition temperature with hydrogen dilution in the plasma chamber.

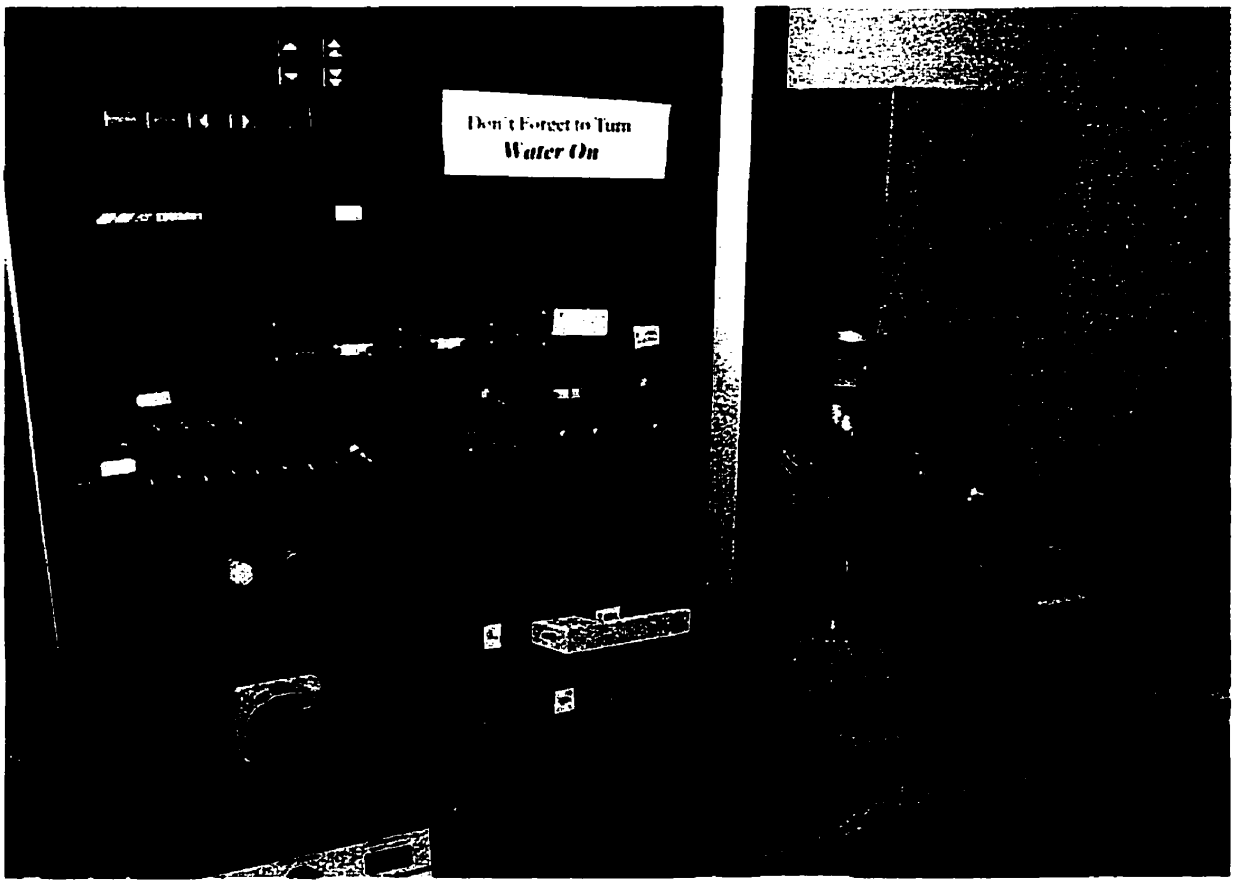


Figure 1.10: Edwards magnetron DC/RF sputtering system thin metal film depositions.

1.5.2 Sputter Deposition

Edwards magnetron sputtering system (Fig. 1.10) used for this work has three target guns so that a combination of metal layers can be deposited in one vacuum pump-down This system has both DC and RF power supplies. For highly conductive metal such as aluminum, the DC power supply is used. For metals not as conductive as aluminum, such as molybdenum, the RF power supply is used. Unlike the PECVD process, the process gas atoms do not get deposited in the film. However, the sputtering gas molecules do have a chance to get trapped in the film. They do not bind to the metal Atoms, simply fill in the voids created during the deposition. Edwards system uses argon as the sputter gas [32]. Figure 1.11 shows a rotating substrate holder in the PVD chamber. The purpose of the rotating substrate is to improve the uniformity of film

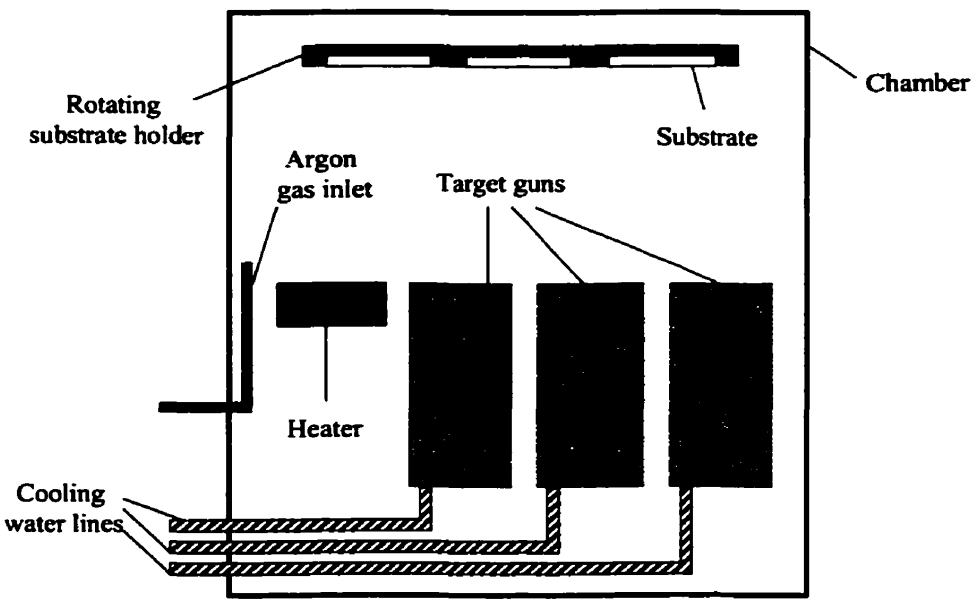


Figure 1.11: A simplified cross sectional view of the Edward sputtering system. Only the most vital components are shown.

thickness. Unlike the PECVD system, whose uniformity difference is within 5%, the PVD system has a uniformity of 10%, or even 15% when the DC power supply is used.

Sputtering is the process of removing surface atoms by ion bombardment. Sputtering processes can be used to deposit films or even to clean or etch surfaces [32]. When positive ions are generated by an ion source such as a glow discharge, they bombard a negative cathode, the target material. The momentum of the ion is transferred to the surface atoms of the target, some of which acquire sufficient energy to leave the surface. Then, these atoms from the target material travel by diffusion to reach the surface of the substrate. Chapter 5 of this thesis will discuss that the quality of films deposited by the PVD sputtering process depends on how much energy the sputtering atoms carry by the time they reach the substrate surface.

1.5.3 Film Deposition in Vacuum

Understanding the film deposition mechanisms in vacuum is very difficult. This thesis does not focus on the film deposition. However, the devices fabricated for this work are made of thin films, deposited by the CVD and PVD systems. Therefore, this thesis does contain discussions of vacuum environment, such as the analysis of microcrystalline growth in chapter 2 and the sputtering kinetics in Chapter 5. In this section, some of the terms that are discussed in the main body of this thesis are introduced.

The international standard unit of pressure is the pascal, Pa, which is defined as a Newton per meter^2, N/m^2. This unit is used to describe the film stresses in Chapter 5. But this unit is seldom used when describing the vacuum chamber pressure. For thin film deposition processes, the vacuum pressure is the torr, Torr, or millitorr, mTorr. One torr is the pressure exerted by the weight of a one millimeter high column of mercury. One pascal is 7.5 mTorr.

In a vacuum, the density of molecules (or atoms) is very low compared to that of the ambient environment at atmospheric pressure. Thus, the molecules travel long distances before they collide with another molecule. The mean free path, λ, of a particle in a vacuum is the average distance that it travels before it collides with another molecule. The mean free path depends on how close together the molecules are and how big a collision target they make. How far the particles are from another depends on the degree of vacuum. The mean free path is expressed as [32]

$$\lambda = kT/\sigma P \qquad \{1.1\}$$

where P is the pressure, σ is the collision cross section, k is the Boltzmann's constant and T is the temperature. The effect of a change in mean free path of the atoms in the sputtering system on the properties of the film being deposited will be presented in Chapter 5.

Both CVD and PVD chambers have to be brought to ambient atmospheric environment for the loading and unloading of wafers. Then, the chambers are pumped down to the base vacuum level of $\sim 10^{-6}$ Torr. Very often, this vacuum level is considered to be "clean" and free of foreign gas molecules. For a given temperature, the density, n, of atoms or molecules in a vacuum is directly proportional to pressure. The relationship is [32]

$$n = 9.67 \times 10^{18}\, P/T \text{ molecules/cm}^3. \qquad \{1.2\}$$

When a vacuum chamber is open and pumped down to 10^{-6} Torr, there are still 10 billion gas molecules in the chamber. It is, therefore, wise not to completely ignore the chance of contamination in the film growth. Furthermore, the rate at which these molecules bombard the surfaces in a vacuum, called bombardment flux, Γ, is given by [32]

$$\Gamma = n\sqrt{(kT/2\Pi M)} = 3.15 \times 10^{22}\, P/\sqrt{(MT)} \text{ particles/cm}^2\text{/second} \qquad \{1.3\}$$

where M is the atomic or molecular weight of the particle. At 10^{-6} Torr, Γ is $\sim 10^{15}$ particles/cm^2/second. From Eqs. 1.14 and 1.15, the time it takes to form a mono-layer of the surface of the wafer at 10^{-6} Torr is only ~ 1 sec. As it will be mentioned later in this thesis, HF dip process is used in device fabrications in order to remove the native oxide at the surface before the wafers are loaded into the plasma chambers. But at atmospheric pressure, it takes only 1 μsec to form a mono-layer on the surface after the HF dip process. The purpose of this HF dip is really to clean the surface rather than to remove the native oxide, unless the native oxide is really thick. The effect of this mono-layer formation on the surface will be discussed in Chapter 2 and Chapter 3 for TFT and Schottky diode device performances, respectively.

1.6 Overview of the Thesis

This thesis describes the technological difficulties that were encountered in integrating this direct detection x-ray sensor with a TFT (as a switch) to make an imaging pixel. Chapter 2 discusses the advancements made in the TFT process and device performance. Chapter 3 presents the leakage current behavior of the Schottky diode. Chapter 4 explores the fabrication process integration of the two devices. Here, two very different processes are compared in terms of the process complexity and the pixel performance. Chapter 5 focuses on the intrinsic film stress that can cause catastrophic damage to deposited films. Chapter 6 discusses the designs of x-ray imaging arrays, followed by conclusions. Although the arrays fabricated in this work are on a very small scale (2mm die), they can be used as templates for larger scale arrays (2" to 6" arrays). Other mask designs are presented in the Appendices along with fabrication specifics.

Chapter 2

Thin Film Transistors (TFTs)

Thin film transistors are most widely used as the switching element in large-area electronics applications. In imaging applications, achieving low leakage current of the transistor is crucial [26]. Each pixel should retain the charge collected by the sensor for as long as possible. This can be achieved only when the leakage current of the transistor is small. For faster switching speed, the transistors should have fast rising current in the sub-threshold region [13, 26]. And as the area of the display/imaging arrays becomes larger (>~17"), the gate delay due to RC constant can become a limiting factor [8, 22, 26]. Thus, the transistor should employ low resistivity gate metal in order to reduce the RC constant. This chapter deals with the advancements achieved in TFT performance with respect to the above mentioned.

2.1 TFT Operation

In flat panel display applications, polycrystalline silicon TFTs are often used as the switching devices due to their high device mobility, which leads to higher maximum drive current to the light emitting device and higher frame rates. In imaging

applications, due to the low device leakage current requirement, amorphous silicon TFTs are used. The TFTs used for this study are based on the inverted-staggered-structure which is widely used in a-Si:H large area displays and imaging systems [9 – 29]. A simplified cross-sectional view of the TFT is shown in Fig. 2.1. This TFT operates in the n-channel accumulation mode when a positive bias is applied, i.e., when the TFT is on. The electric field from the gate metal attracts electrons in the intrinsic amorphous silicon layer to form a thin n-channel at the gate dielectric interface. When a positive bias is applied to the drain with the respect to the source, the electrons can flow from source to drain. This TFT operation follows the usual semiconductor relations for MOSFET transistors. The challenge for a-Si:H TFT is achieving low on-resistance, R_{ON}. For large area imaging applications, the frame rate can be 15 ~ 70 frames/s [13, 14, 21]. A simple calculation can be done assuming that the frame rate is 30 frames/s and there are 2000 gate lines in the large area imaging array. In this case, each line must be read in 15 μs. Allowing 5 μs for gate switching, the actual time left for the TFT to transfer the charge from the sensor to the data line is only 10μs. Again, assuming that the transfer of charge takes 5 time constants (RC) and the pixel capacitance is ~1pF [33], the on-resistance of the TFT is

$$R_{ON} \leq 2\ M\Omega \qquad \{2.1\}$$

In the imaging applications, the TFT operates in the linear regime for which the on-resistance, the ratio of source drain voltage and current, is [34]

$$R_{ON} = V_{DS} / I_{DS} = [C_G \cdot \mu_{FE}(V_G - V_T)W/L]^{-1}\ , \qquad \{2.2\}$$

where C_G is the gate capacitance, μ_{FE} is the field effect mobility, V_G is the gate bias, V_T is the threshold voltage, W is the width of the TFT, and L is the TFT channel length. For a thin film transistor with the gate dielectric thickness of 250nm and a field effect

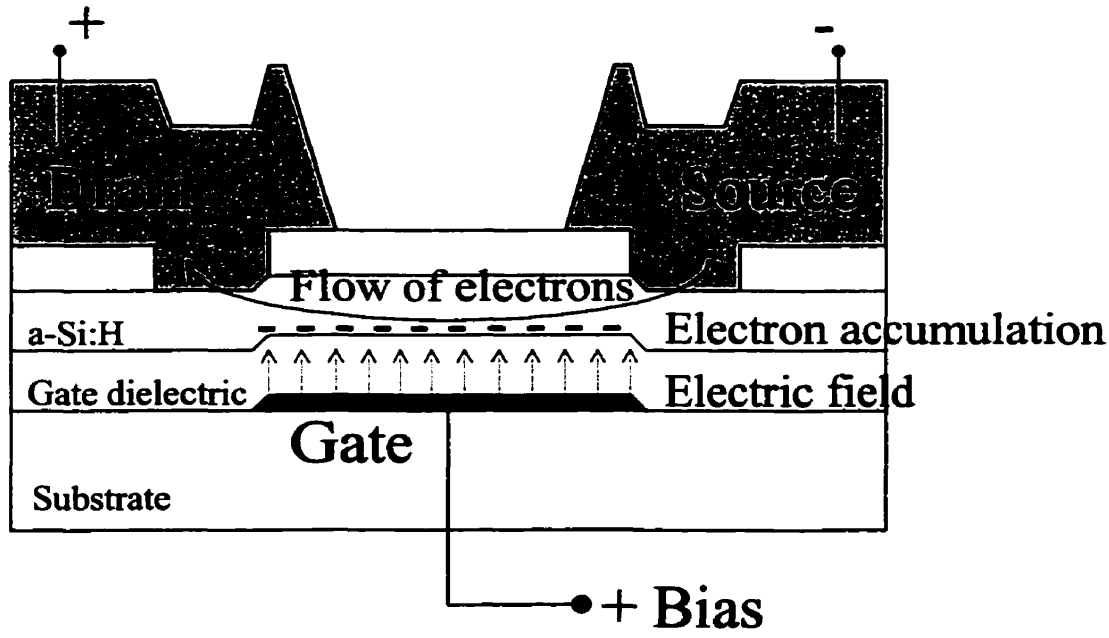


Figure 2.1: Inverted-staggered a-Si:H TFT. When the gate positively biased, an electron channel is induced at the gate dielectric/intrinsic silicon interface providing a conduction path from drain to source.

mobility of ~1 cm^2/Vs, the gate capacitance is ~5 x $10^{-8}F/cm^2$ [35]. Then, the equation for on-resistance can be simplified to

$$R_{ON} = 25[(V_G - V_T)W/L]^{-1}\ M\Omega. \qquad \{2.3\}$$

For a TFT with $V_G - V_T = 5V$, the requirement suggested in Eq. 2.1 can be achieved if the aspect ratio of the transistor W/L is greater than 2.5. In Chapter 6 (see Fig. 6.2), the channel of the TFTs in the array is 50μm wide and 20μm long, which results in W/L ratio of 2.5. The upper limit of this ratio is strongly governed by another array design requirement, namely, fill factor. The trade-off of these two design criteria will be revisited in Chapter 4 where the pixel designs will be discussed. In this chapter,

however, since the TFT is presented as a single discrete device, the aspect ratio is kept at 10 (W = 200μm / L = 20μm).

The requirement for low on-resistance of the channel is really for the fluoroscopy application. For radiographic application, the TFT is required to hold the charge on the pixel for the radiographic frame time which can be as long as one second or even longer. If only 1% of the data loss is allowed on a pixel whose pixel capacitance is 1pF, and the frame time is 1 second, the required *RC* constant of the TFT when turned off is

$$R_{OFF}C > 100 \text{ second}, \qquad \{2.4\}$$

which means that

$$R_{OFF} > 10^{14}\ \Omega. \qquad \{2.5\}$$

This is why low TFT leakage current is important for radiographic application. In the following section of this chapter, the TFT device performance will be compared in terms of the leakage current. A TFT leakage current of 100 fA or higher is not suitable for x-ray imaging applications.

The current-voltage characteristics of a-Si:H TFTs are effectively the same as those of a crystalline silicon MOS transistors except for a fact that the magnitude of the current level of a-Si:H TFTs are much lower. The accumulated charge at the gate dielectric interface can be expressed using the MOS transistor equation [36]

$$Q(x) = C_G[V_G - VT - V(x)], \qquad \{2.6\}$$

where $V(x)$ is the additional voltage along the channel at distance x that is formed by the applied bias V_{DS}. The drain current I_D can be expressed as

$$I_D(x) = W \bullet Q(x) \bullet \mu_{FE} \bullet E(x), \qquad \{2.7\}$$

where $E(x)$ is the electric field between drain and source. Substituting Eq. 2.6 into Eq. 2.7 leads to

$$I_D(x) = W \bullet \mu_{FE} \bullet C_G[V_G - V_T - V(x)]dV(x)/dx. \quad \{2.8\}$$

Integrating Eq. 2.8 along the channel results in

$$I_D(x) = \mu_{FE} \bullet C_G[(V_G - V_T)V_D - V_D^2] \bullet W/L. \quad \{2.9\}$$

Just as in the MOS transistors case, the drain current of a-Si:H TFTs saturates after a certain bias point at V_{DS}. When $\Delta I_D/\Delta V_{DS} = 0$, the drain saturation current can be expressed as

$$I_{D_Saturation} = 1/2 \bullet \mu_{FE} \bullet C_G(V_G - V_T)^2 \bullet W/L. \quad \{2.10\}$$

Equations 2.6 ~ 2.10 are essentially the same as the MOSFET model equations. These equations will be revisited in the following sections of this chapter where measured a-Si:H TFT device characteristics are presented.

2.2 TFT Fabrication

A fully wet etch process has been used in the fabrication. The fabrication sequence is shown in Fig. 2.2. Corning 7059 glass wafers are used as the substrate material. First, the gate metal is deposited by the PVD method. The gate metal thickness is between 90nm and 150nm. Usually, molybdenum (Mo) and chromium (Cr) are used as gate metal. For low resistivity gate metallization, aluminum (Al) gate metallization was developed, which will be discussed in section 2.3. After the gate is patterned with mask one, gate dielectric, active layer (intrinsic a-Si:H), and top dielectric layer are deposited in a single vacuum deposition process to preserve the interface quality. For this study of direct detection x-ray imaging, the dielectric layer used in TFT is silicon nitride film

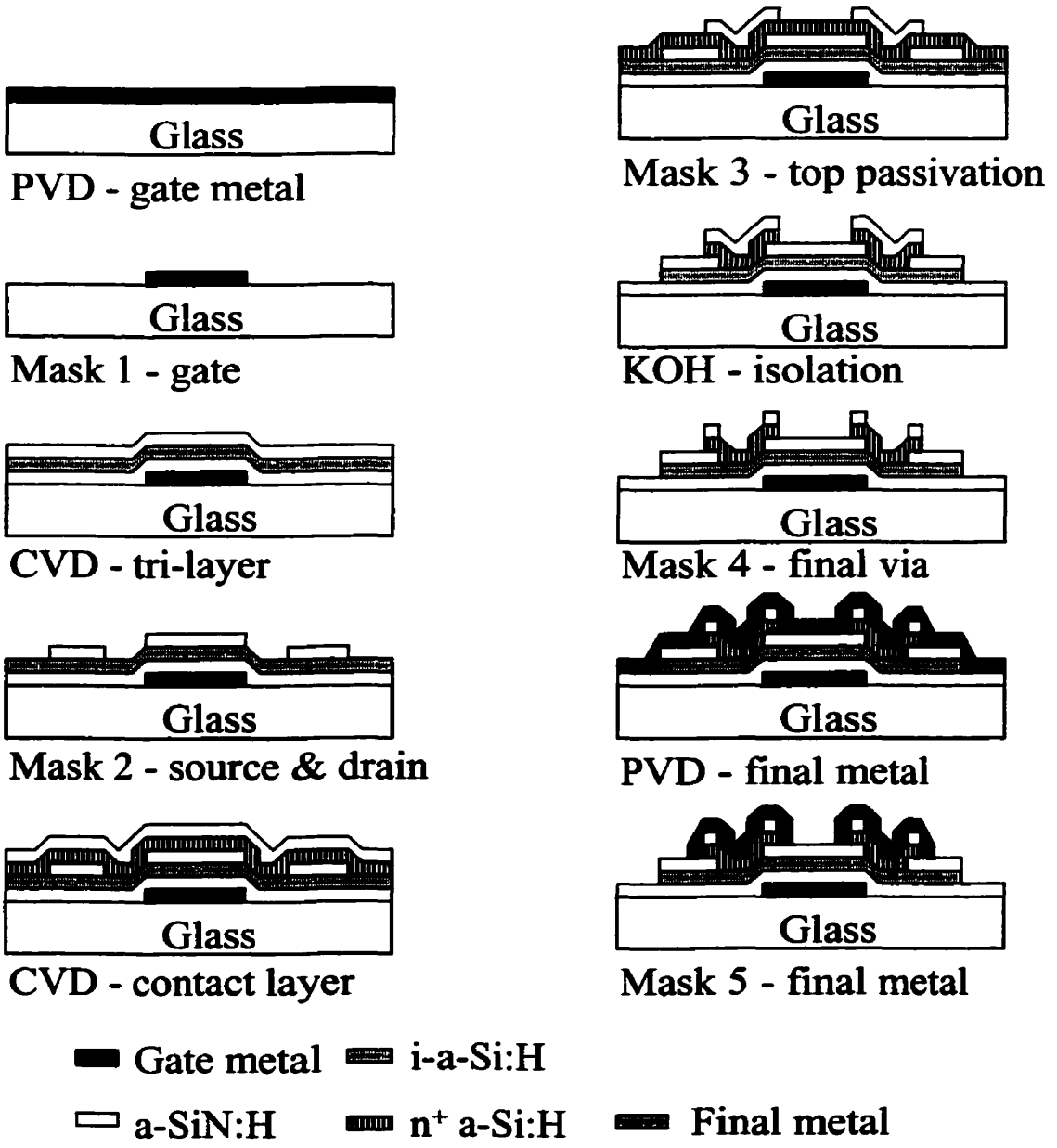


Figure 2.2: Fabrication sequence of thin film transistor in inverted-staggered-structure deposited on Corning 7059 glass substrate.

(a-SiN:H). In this tri-layer deposition, the a-SiN:H layer thickness is 250nm and the intrinsic a-Si:H thickness is 50nm. The thickness of the i-a-Si:H layer is optimized for the lowest leakage current [37]. The top silicon nitride layer is patterned with mask two, which defines the source and the drain regions of the TFT. Then, another CVD process is carried out to deposit the contact layer (50nm) covered by the top passivation layer (250nm). The contact layer is deposited to form ohmic contact between the active layer and the final metal. A low-temperature (200°C), low-resistivity n^+ μc-Si:H film process is developed to serve as this contact layer as opposed to n^+ a-Si:H film. The details are discussed in section 2.2. After the top passivation layer is patterned with mask 3, the entire wafer is dipped in KOH solution for wet etching of the contact layer and the active layer. Etching the contact layer separates the source and the drain of TFTs. Etching of the active layer isolates one device from another. In this step, the mechanical integrity of the top passivation silicon nitride film is crucial. If the top passivation layer is porous (rich in pinholes), the KOH solution will attack the silicon films underneath the passivation layer. When the devices are isolated from one another, they are ready for the last PVD deposition of the final metal. Mask four opens via's on the top passivation layer such that the final metal can be deposited on the contact layer film. The final metal is then patterned with mask five, which completes the fabrication of the inverted staggered-structured TFTs. The most critical alignment steps are mask two and three. These steps are, respectively, the major determinants in a device performance and yield.

2.3 Low Temperature, Low-Resistivity Highly Doped Microcrystalline Silicon (n^+ μc-Si:H)

2.3.1 Motivation for Studying n^+ μc-Si:H

Hydrogenated microcrystalline silicon (μc-Si:H) has been of current technological interest for device applications because of its high electrical conductivity, high doping efficiency and low optical absorption, compared to a-Si:H. Heavily phosphorous-doped μc-Si:H films are being widely used as an ohmic contact layer of TFTs to lower the contact resistance in the drain and source regions, thereby improving the sub-threshold characteristics of the TFTs. Doped or undoped μc-Si:H can be viewed as a material comprised of crystalline grains and amorphous grain boundaries.

It is well known that the deposition temperature affects the surface migration process, which is one of the key characteristics in the film formation. The dependence of the μc-Si film formation on the deposition temperature has already been discussed by several research groups. However, the growth mechanism of the film is not yet fully understood and is still considered controversial. Arai et al. have reported that the crystallization does not occur at low deposition temperatures, because of the poor migration of deposition precursors and the absence of ordered sites [38]. He has shown the formation of micro-crystallinity on the growing surface by heating the source gas (SiH_4) in the plasma enhanced chemical vapor deposition (PECVD) process to promote the diffusivity of the deposition precursors. Conde et al. have reported that the microcrystalline films, which were obtained by the hot-wire deposition method at high hydrogen dilution, are independent of the deposition temperature [39]. Matsuda [40] and Kanicki et al. [41] have reported that the degree of crystallinity of the films increased with the deposition temperature varied from 100°C to 500°C.

The study of the n^+ μc-Si:H was done in order to explore the feasibility of using this material as the contact layer in a-Si:H TFTs. Since the fabrication process of the μc-Si:H should be compatible with that of a-Si:H, particular attention was paid to the effect of the deposition temperature on the structural properties of the n^+ μc-Si:H, to gain an

insight into the structural transition from the amorphous to the crystalline phases. The n^+ μc-Si films have been deposited by PECVD on glass substrates (Corning 7059) at different deposition temperatures from 200°C to 400°C. The deposition conditions are summarized in Table 2.1. The films were characterized by grazing incidence x-ray

Deposition Parameter	Value
FR(1 % PH_3 / SiH_4)	10 sccm
FR(H_2)	1000 sccm
Pressure	1 Torr
Power Density	40 mW/cm^2
Deposition rate	2 nm/min

Table 2.1: Deposition conditions of n^+ μc-Si:H films used in this study (FR indicates the flow rate of each gas).

diffraction (GIXD), Raman scattering spectroscopy, and Fourier transform infra red (FTIR) spectroscopy measurement techniques.

2.3.2 Crystallinity Shown by GIXD

GIXD measurements were performed with a Nicollet-12 diffractometer (Cu radiation, 30 KV, 20 mA). The average crystallite size was determined from (hkl) lines according to the Scherrer formula [42]. The preferred orientation was determined from the relative line intensities.

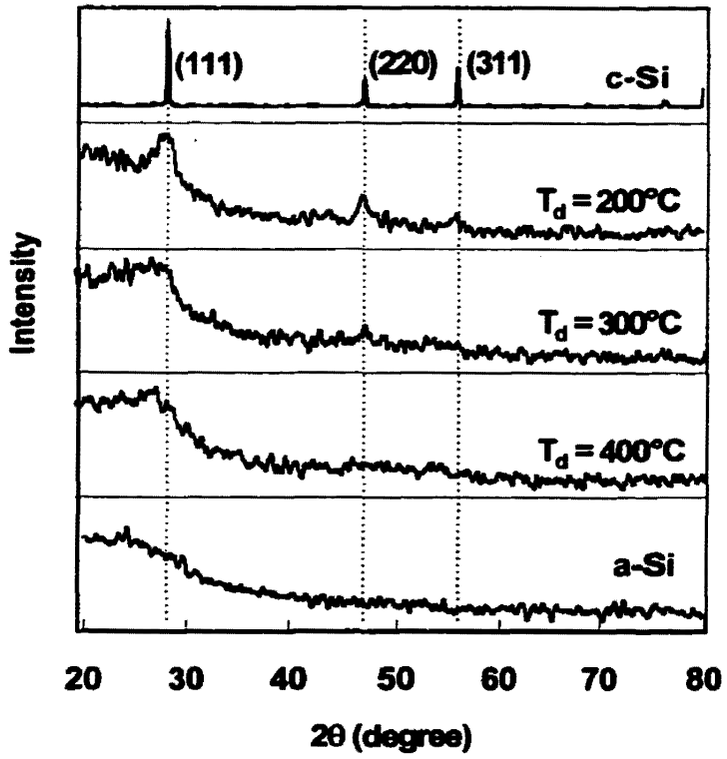


Figure 2.3: X-ray diffraction patterns for n^+ μC-Si:H films deposited at 200°C, 300°C and 400°C.

Figure 2.3 shows the x-ray diffraction patterns of the n^+ μc-Si films deposited at 200°C, 300°C and 400°C, along with those of crystalline silicon (c-Si) and n^+ a-Si test samples. The film deposited at 200°C appears to have (111), (220), and (311) preferred orientations, as in the c-Si sample. The mean grain size, which was estimated from the full width at half maximum of the peak (111) using the Scherrer formula, was found to be approximately 4nm. This indicates that the micro-grains in the network are perfect crystals. The absence of these peaks and the existence of a broad shoulder at $2\theta = 25°$ in the films deposited at 400°C, as in the a-Si sample, indicate the evidence of the

amorphous state of the material. It was observed that the films deposited at T_d = 300°C represent an intermediate behavior, i.e., a transition from the crystalline to the amorphous phase. The fraction of the crystallinity was observed to be 60 %, 30 % and 10 % in the films deposited at 200°C, 300°C and 400°C, respectively. This observation contradicts the results reported in the literatures [40, 41] in which it was shown that the higher deposition temperature facilitates the (220) and the (311) peaks. The behavior in the samples was further confirmed by Raman and FTIR measurements.

2.3.3 Crystallinity Shown by Raman Spectroscopy

Raman scattering spectroscopy measurements were performed with a micro Raman spectrometer using 632.8 cm^{-1} line of a He-Ne laser (Melles - Griot). The laser light was focused on the sample through an Olympus BH-2 microscope. The scattered light was detected by a CCD, which was attached to the output slit of a Renishaw Raman 1000 spectrograph. The crystalline volume fraction and the crystallite grain size were determined based on this data, using the method proposed by He et al. [43].

Figure 2.4 shows the Raman spectra of films deposited at 200°C, 300°C and 400°C. The enhancement of the peak and the narrowing of the spectrum at 521 cm^{-1} of the film deposited at 200°C represent the crystalline phase, whereas the decrease of the peak intensity at 521 cm^{-1} and the increase of the broad shoulder at 483 cm^{-1} of the film deposited at 400°C indicate the amorphous phase. The crystalline volume fractions were estimated to be 70 %, 35 % and 20 % in the films deposited at 200°C, 300°C, and 400°C, respectively. The grain size of the crystallites was reduced from 4.5 nm (200°C) to 2.5 nm (400°C).

These observations also showed that the relative ratio of the crystalline phase to the amorphous phase decreased with the increasing deposition temperature. The samples were further tested by Fourier transform infrared spectroscopy.

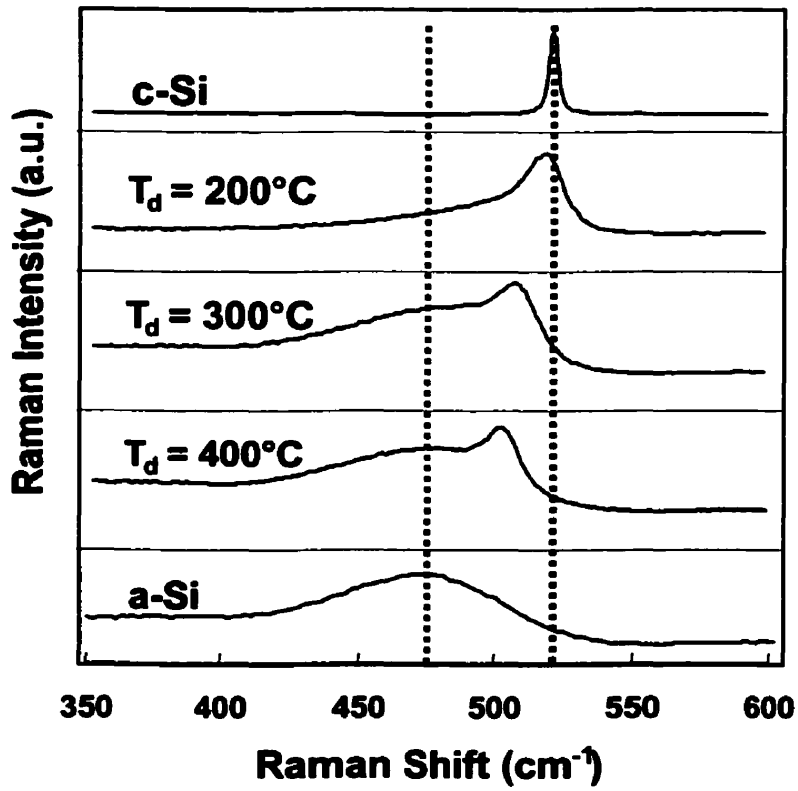


Figure 2.4: Raman spectra for n^+ μc-Si:H films deposited at 200°C, 300°C and 400°C.

2.3.4 Hydrogen Content (FTIR)

Samples were also deposited on c-Si wafers for IR studies to estimate the hydrogen concentration in the films. These measurements were performed in absorbance mode with a resolution of 4 cm^{-1} using a Bomem IR spectrometer.

The FTIR spectra showed peaks in our samples at 630 cm^{-1}, 2010 cm^{-1}, and 2400 cm^{-1} (Fig. 2.5). The prominent peak at 630 cm^{-1} corresponded to the Si-H wagging

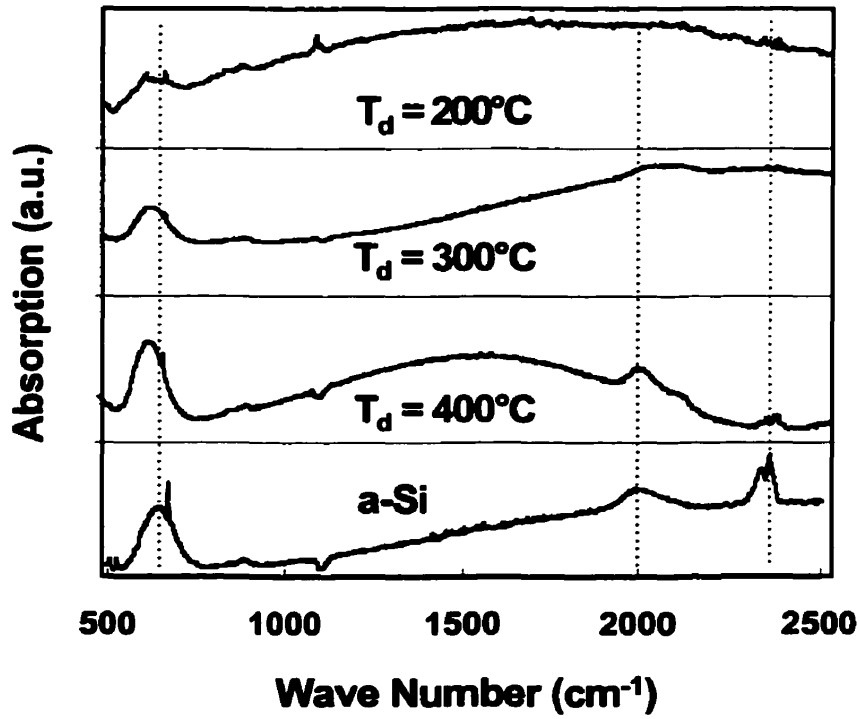


Figure 2.5: Infrared spectra for n^+ μc-Si:H films deposited at 200°C, 300°C and 400°C.

mode. As the deposition temperature decreaseed from 400°C to 200°C, the intensity of this peak was reduced, which implied that the hydrogen content decreased. The slight shift of this peak towards lower frequencies indicated a change in the hydrogen bonding. The bonded H concentration, estimated using an oscillator strength of 1.6 x 10^{19} cm^{-2}, as given by Shanks et al., was 10^{21} cm^{-3} in the sample deposited at 200°C [44]. It increased to 4.5 x 10^{21} cm^{-3} in the sample deposited at 400°C. The observed peaked at higher frequencies arose from SiH and SiH_2 stretching vibrations.

2.3.5 Resistivity

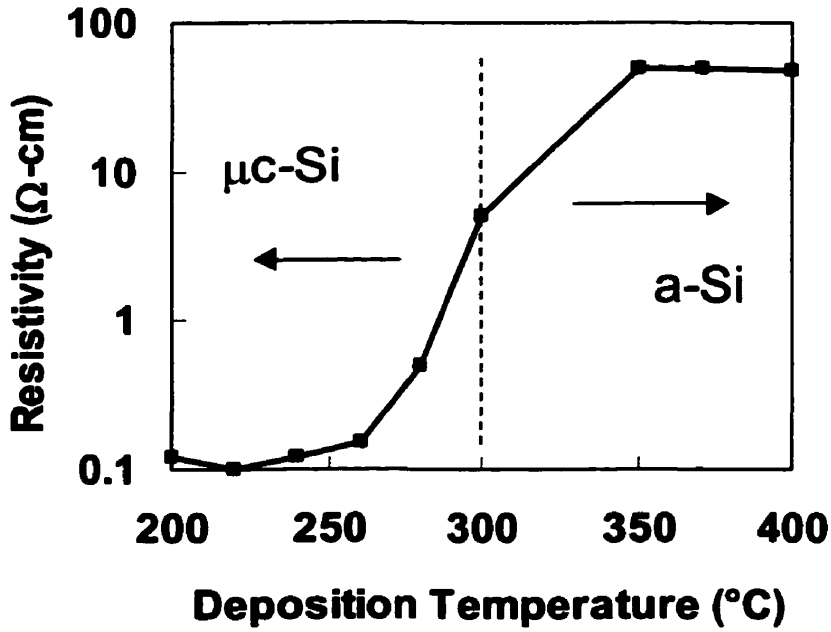


Figure 2.6: Resistivity of n^+ μc-Si:H films as a function of the deposition temperature.

As a further confirmation of above results, the resistivity of n^+ μc-Si:H as a function of the deposition temperature is shown in Fig. 2.6. Here, the value of the resistivity is 0.1 Ω-cm for low-temperature ($T_d \leq 240°C$) deposited films, and it increases to a value of 70 Ω-cm for films deposited at high temperatures ($T_d \geq 340°C$), which is close to that of n^+ a-Si:H [45]. This shows that our n^+ μc-Si:H films deposited at low temperatures have a higher conductivity of 10 $\Omega^{-1}cm^{-1}$, which is essential for high performance a-Si:H TFTs.

2.3.6 Optical Band Gap

The optical band gap (E_{op}) was measured with Oriel optics instruments. They are a grating monochrometer (model 77200), DC regulated power supply (model 68735), quartz halogen lamp, photodiode head (model 71925), and photodiode (model 71803).

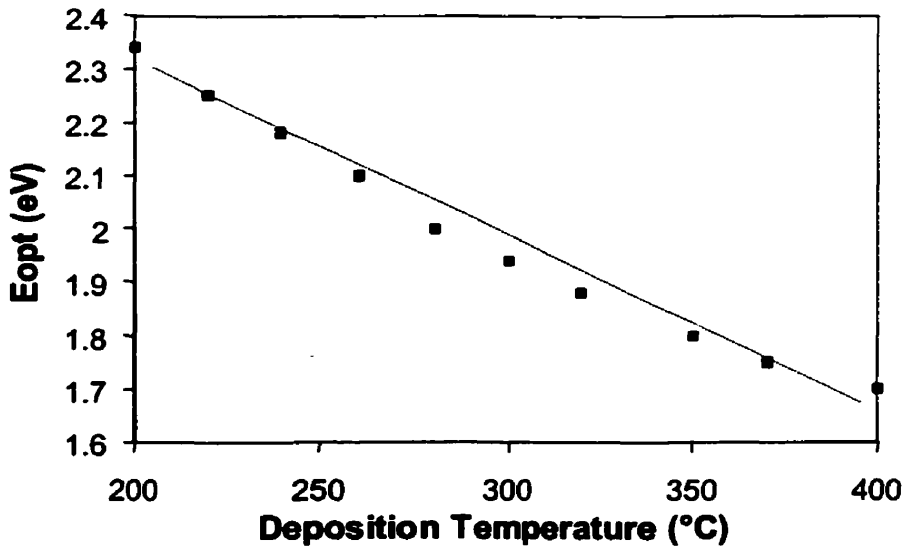


Figure 2.7: Optical band gap of n^+ μc-Si:H films as a function of the deposition temperature.

The optical energy gap as a function of deposition temperature is shown in Figure 2.7. It shows that the E_{op} is higher (2.3eV) in films deposited at low temperature and decreases to a value of 1.75eV, which is a characteristic of a-Si:H films deposited at higher temperatures. It has been reported that the optical band gap of μc-Si material is 2.3eV [45]. The measured E_{op} values match exactly with the reported values in the films deposited at low temperatures. These data show that the films deposited at low

temperatures are more in crystalline phase, whereas the films deposited at high temperatures are in amorphous phase.

2.2.7 Crystallization at Low Temperature

Although μc-Si:H films have been investigated for several years, the growth mechanism, transport, and optical properties are still not fully understood. In most studies, it is generally agreed that the hydrogen dilution is necessary for the crystallization of silicon network during the growth [38 – 49]. But it is still not clear how the excess hydrogen concentration in the plasma leads to crystallization of silicon atoms. Several possible roles of hydrogen dilution during the growth of μc-Si:H have been proposed.

1. The excess hydrogen atoms on the growing surface enhance the diffusion of the absorbed radicals (SiH, SiH_2, and SiH_3) [46].
2. The hydrogen radicals act as etchant of Si and promote chemical equilibrium between the deposition and the etching of the growing surface [47].
3. hydrogen atoms soak into several layers below the top surface and promote the network propagation reaction [48].

It has also been proposed that the crystallization occurs due to the elevated thermal energy of the arriving radials at the growing surface [41]. According to this theory, at an elevated temperature, the radicals at the surface possess enough thermal energy to move around until a favored (lowest) energy site is found, which leads to unstrained crystalline network of silicon atoms. This proposed explanation contradicts the

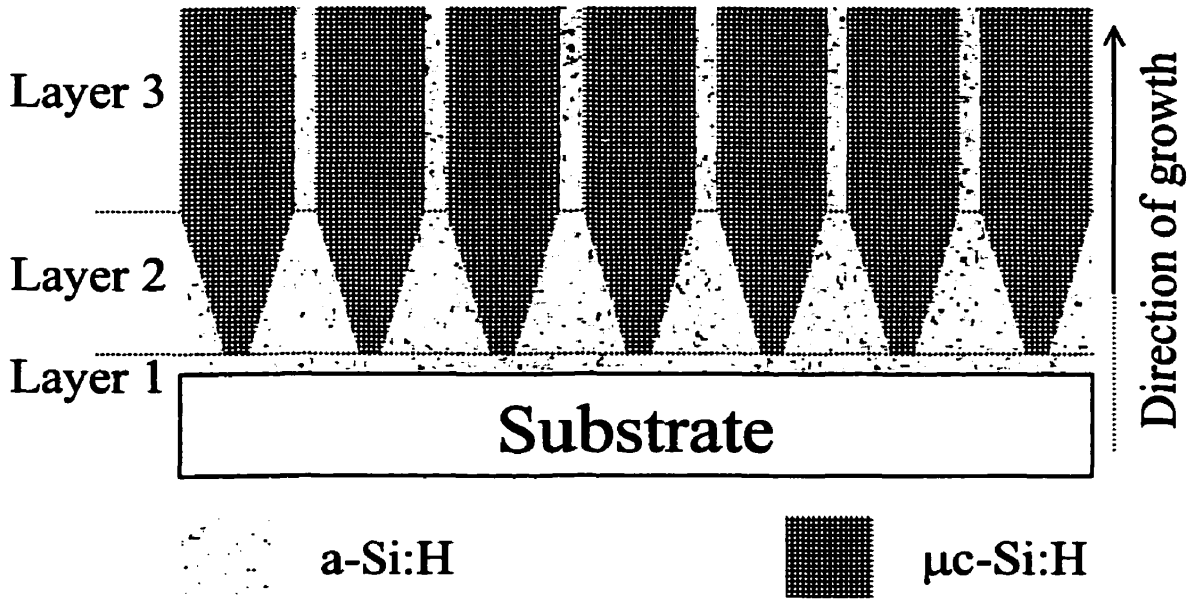


Figure 2.8: The three layer model of microcrystalline film growth.

observations made at our laboratory (see Figs 2.2 ~ 2.7). Furthermore, this theory does not clearly explain why crystallization occurs only with hydrogen dilution and why hydrogen content in the film is reduced with high hydrogen dilution.

The growth process of μc-Si:H films is often represented by the three layer model (Fig. 2.8) [49]. During the initial nucleation stage of the growth process, the film is mostly amorphous. But as the film grows thicker (~150Å), microcrystallites start to form. At this stage, the film is made of crystalline grains with amorphous grain boundaries. The incoming radicals (SiH, SiH_2, and SiH_3) at the growing surface can be attached to silicon atoms from either amorphous or crystalline parts. When the film grows to be even thicker (>1000Å), the growing surface is largely crystalline. This growth model theory appears to be valid for films grown at our laboratory [50]. In the transmission electron microscopy (TEM) patterns of 1800Å and 600Å thick n^+ μc-Si:H

films, patterns with sharper rings are obtained for the thicker film [50]. This indicates a better structural quality for the 1800Å thick film compared to 600Å thick film. Based on above observations, a preliminary growth model for μc-Si:H deposition process can be extracted.

It is well known that the hydrogen dilution – unlike other dilution gases (such as He or Ar) – slows down the growth rate [38 – 49]. This is due to the etching property of hydrogen radicals in the plasma. Even without the hydrogen dilution, the plasma contains hydrogen radicals created by the dissociation of the source gases (i.e. SiH_4 and PH_3). Therefore, at the growing surface of a-Si:H film, both etching and deposition occur. The total rate of film growth, R, can be expressed as

$$R = D - E \qquad \{2.11\}$$

where D is the rate of deposition and E is the rate of etching.
The rate of deposition can be divided into two parts

$$D = c_1 D + a_1 D \qquad \{2.12\}$$

$$c_1 + a_1 = 1 \qquad \{2.13\}$$

where c_1 and a_1 are unitless coefficients for depositions which leads to crystalline and amorphous bonds between silicon atoms, respectively. Similarly, the rate of etching can be written as

$$E = c_2 E + a_2 E \qquad \{2.14\}$$

$$c_2 + a_2 = 1 \qquad \{2.15\}$$

where c_2 and a_2 are coefficients for fractions of etched crystalline bonds and amorphous bonds, respectively. Without the hydrogen dilution, the deposited film is amorphous, which can be achieved under any of the following three conditions.

(1) $c_1 D < a_1 D,\ c_2 E \approx a_2 E,$ {2.16}

(2) $c_1 D < a_1 D,\ c_2 E > a_2 E,$ or {2.17}

$$(3) \qquad c_1 D \approx a_1 D,\ c_2 E > a_2 E. \qquad \{2.18\}$$

Above coefficients can only be determined experimentally, but reasonable assumptions (based on the existing data from the experiments in the previous sections) can simplify the case. With the hydrogen dilution, the total deposition rate is reduced to ~25% (see Table C.1). This can be easily explained by the increased rate of etching process due to the extra hydrogen radicals in the plasma. The total rate of film growth with hydrogen dilution, R', is then

$$R' = D - E - E' \qquad \{2.19\}$$

where E' represented the additional etching rate. The total deposition rate with hydrogen dilution is still a positive quantity (see Table C.1). Thus,

$$D > E + E' \qquad \{2.20\}$$

and since $R' \approx 0.25R$,

$$E' > E \qquad \{2.21\}$$

which leads to

$$D > E' > E. \qquad \{2.22\}$$

The exact chemical balance equations in the plasma are still not discovered. Equations 2.20 – 2.22 are only qualitative observations based on the experimental data. But the rough approximation stated in Eq. 2.22 suggests that the dominant term in Eq. 2.11 is D. Then, among the three conditions from Eqs. 2.16 – 2.18, the most likely case is Eqs. 2.16 and 2.17. In other words, without the hydrogen dilution, the grown silicon film is amorphous in nature mainly because most incoming radicals form amorphous bonds at the surface at deposition temperature of 260°C (see Table C.1). But no information can yet be extracted about the coefficients for etching (i.e. c_2 and a_2).

With hydrogen dilution, the film grows to contain microcrystalline grains. The additional etch rate, E', in Eq. 2.19 can be broken down to

$$E' = c_3E' + a_3E' \qquad \{2.23\}$$

$$c_3 + a_3 = 1 \qquad \{2.24\}$$

where c_3 and a_3 are coefficients for fractions of etched crystalline bonds and amorphous bonds, respectively. Using above two equations and Eqs. 2.12 – 2.15, Eq. 2.19 can be rewritten as

$$R' = c_1D + a_1D - c_2E - a_2E - c_3E' - a_3E'. \qquad \{2.25\}$$

Again, the exact plasma chemical balance equations are not known. But since the additional hydrogen atoms are mixed with the hydrogen radicals from the source gases in the gaseous state in the plasma chamber,

$$c_2 \approx c_3,\ a_2 \approx a_3. \qquad \{2.26\}$$

Then Eq. 2.25 becomes

$$R' = c_1D + a_1D - c_2(E + E') - a_2(E + E'). \qquad \{2.27\}$$

Let

$$E'' = E + E'. \qquad \{2.28\}$$

Eq. 2.27 can be simplified to

$$R' = c_1D + a_1D - c_2E'' - a_2E''. \qquad \{2.29\}$$

In Eq. 2.29, microcrystalline film can be deposited if and only if the following conditions are satisfied.

$$(c_1 + a_1)D > (c_2 - a_2)E'' \text{ and} \qquad \{2.30\}$$

$$(c_1D - c_2E'') > (a_1D - a_2E''). \qquad \{2.31\}$$

The condition stated in Eq. 2.30 ensures that the film is deposited, not etched. This equation is essentially reinforcing the condition set in Eq. 2.20. If the inequality is reversed, the result would lead to plasma-etching. In fact, this plasma-etching process is carried out in industries (with pure H_2 as etching gas) where the surface requires cleaning. This will be mentioned again in Chapter 3 of this thesis. The condition stated in Eq. 2.31 ensures that the effective net deposition rate of crystalline silicon bonds is greater than that of amorphous bonds.

The condition in Eq. 2.30 is always satisfied at all deposition temperatures, T_{Dep}. However, the condition in Eq. 2.31 is violated as the deposition temperature increases to 400°C as seen in Figs. 2.2 – 2.7. There are three possible ways for Eq. 2.31 to be satisfied:

$$(1) \quad c_1D > a_1D,\ c_2E'' \approx a_2E'', \qquad \{2.32\}$$

$$(2) \quad c_1D > a_1D,\ c_2E'' < a_2E'', \text{ or} \qquad \{2.33\}$$

$$(3) \quad c_1D \approx a_1D,\ c_2E'' < a_2E''. \qquad \{2.34\}$$

Unfortunately, all coefficients in Eq. 2.31 can be temperature dependent. Thus, all four terms in Eq.2.31 can be a function of deposition temperature. It is, therefore, not easy to determine how the inequality is satisfied at 200°C but violated at 400°C. But further analyses can be carried out by observing each term in Eq. 2.31 individually.

The a_2E'' term represents the rate of amorphous silicon bonds being etched. Consider a silicon atom with a strained amorphous silicon bond to the surface. For simplicity, assume that all other three valence electrons are bonded with hydrogen atoms. If there is a free valence electron in the silicon atom, the incoming hydrogen atom is more likely to bond to that electron. The mechanism of hydrogen etching is illustrated in Fig. 2.9a). Similarly, the hydrogen etching process of a stable silicon-silicon bond is illustrated in Fig. 2.9b). The plasma chamber is highly diluted with the

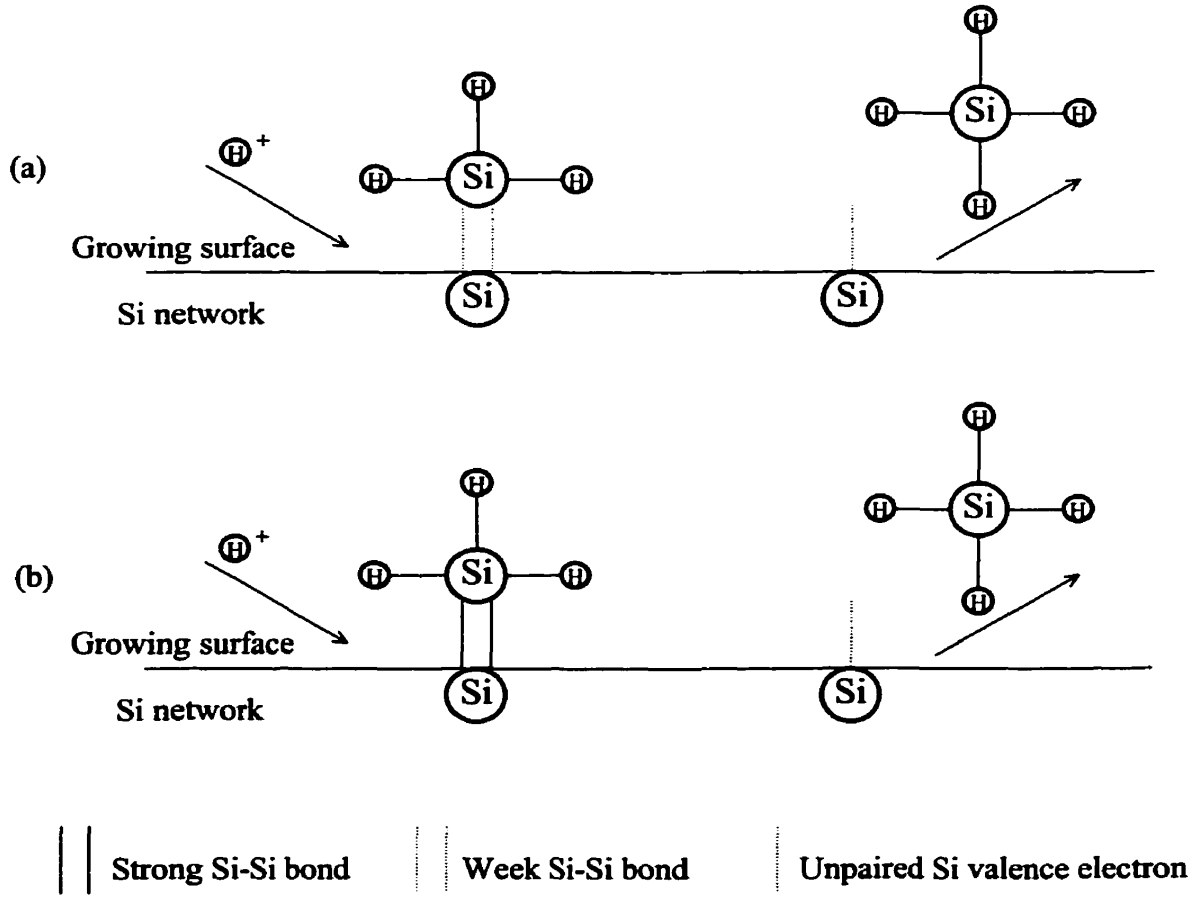


Figure 2.9: The etching mechanisms of hydrogen atoms in the microcrystalline growth process. (a) Etching of unstable and strained Si-Si bond. (b) Etching of a stable and strong Si-Si bond.

hydrogen gas (100:1). It is, therefore, apparent that not all hydrogen atoms arriving at the surface etch a silicon atom. Only a small fraction of hydrogen atoms that arrive at the growing surface have enough energy to break the silicon bonds. This would explain why the film still gets deposited, not etched, even at such high hydrogen dilution ratio.

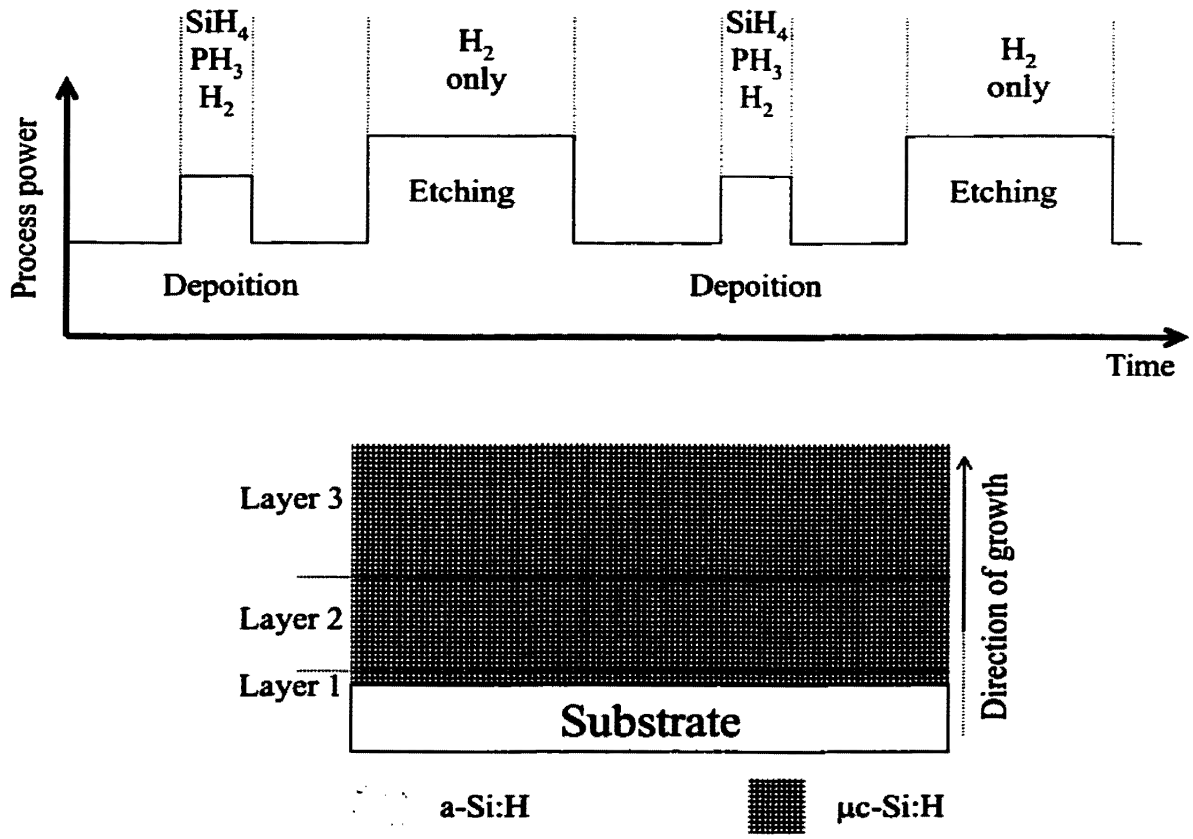


Figure 2.10: Layer-by-layer deposition of microcrystalline films. The process is repeated between deposition cycle and etching cycle. The result is a microcrystalline film from the very initial layer.

It is also reasonable to assume that the energy required to etch a strained week amorphous Si-Si bond is lower than the energy needed to break a stable strong Si-Si covalent bond. This assumption appears to be valid in the layer-by-layer deposition experiment in which a few mono-layers of Si are deposited followed by subsequent pure hydrogen plasma treatment at the surface [47]. By repeating this deposition-etching cycles, a completely microcrystalline silicon film can be deposited (Fig. 2.10).

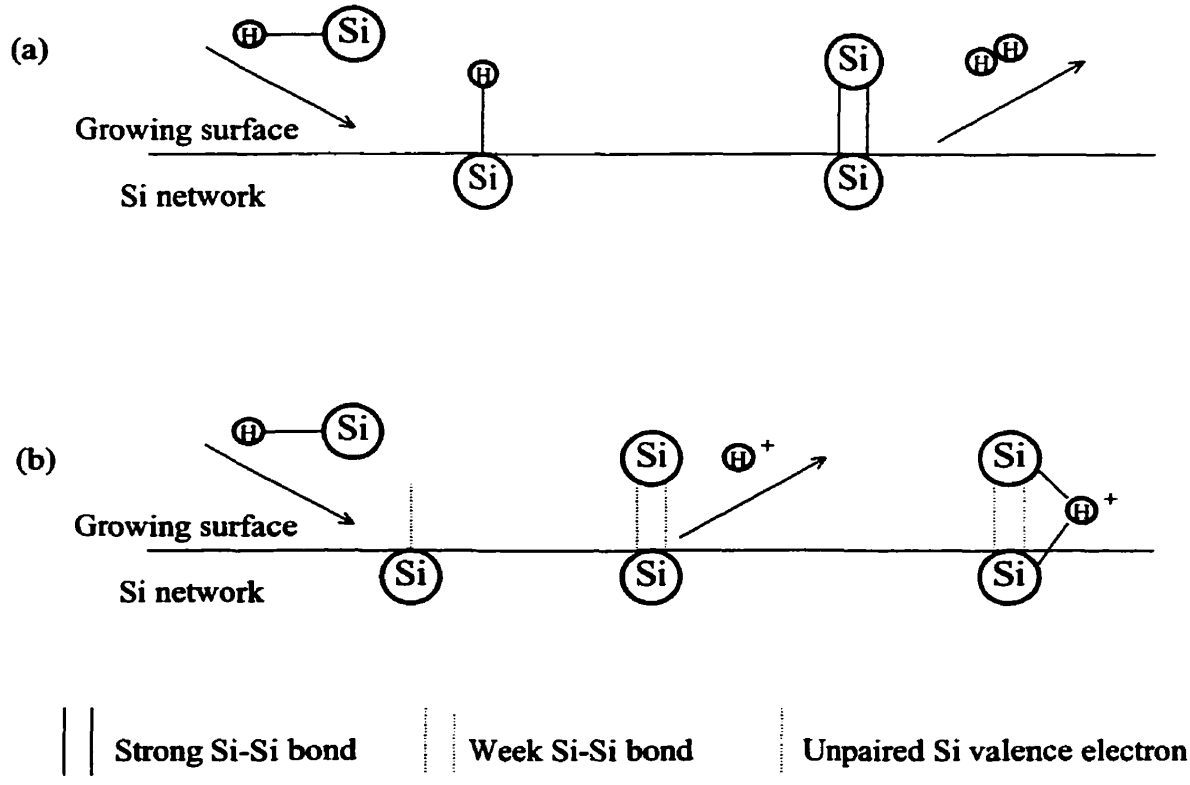


Figure 2.11: The deposition mechanisms in the growth of microcrystalline silicon films. (a) An inception of a silane radical which leads to a strong and stable Si-Si bond. (b) An inception of a silane radical which leads to an unstable and strained Si-Si bond.

The deposition mechanisms of silicon atoms are illustrated in Fig. 2.11. It is believed that the most useful radical for deposition is SiH_3 [34]. However, all silane radicals can contribute to deposition. For simplicity, in Fig. 2.11, all incoming radicals are represented by Si-H. These incoming radicals have a tendency to bond with a silicon atom at the growing surface, allowing the hydrogen atoms to form a stable H_2 molecule and leaving a strong stable Si-Si bond at the surface (see Fig. 2.11a). But when most of

the hydrogen atoms have evaporated from the growing surface due to the high deposition temperature, the hydrogen atom of the incoming radical has to depart from the weak strained Si-Si bond as an ion or it gets incorporated in the Si network causing the film to be amorphous. This also explains why at higher deposition temperature the hydrogen content in the film is higher as seen in Fig. 2.5.

Based on above analyses, the following conclusions can be extracted:

1. The hydrogen dilution etches more amorphous Si bonds than crystalline bonds. $a_2 > c_2$
2. Even with the hydrogen dilution, the deposition rate is higher than the etch rate. $D > E' > E$
3. At low deposition temperatures (~200°C), the hydrogen atoms form a hydrogen molecule leaving a strong Si-Si bond at the surface. At high deposition temperatures (~400°C), most hydrogen atoms evaporate from the growing surface which can cause the unpaired hydrogen atoms to be incorporated in the film. $a_1 \propto T_{Dep}$, and $c_1 \propto 1/T_{Dep}$
4. Microcrystallization happens if and only if $(c_1 + a_1)D > (c_2 - a_2)E''$ and $(c_1D - c_2E'') > (a_1D - a_2E'')$ are satisfied.

The conclusions stated above are based on the qualitative observations from the experiments. In order to model the coefficients, a_1, a_2, c_1 and c_2, many more experiments need to be carried out. But the statements above should be able to provide a concrete foundation for further investigation of the microcrystalline film growth.

2.3.8 TFT Performance Improvement

The n^+ μc-Si:H film deposited at low temperature was used to reduce contact resistance in the source and drain regions of the TFTs. The conductivity of n^+ μc-Si:H film is

higher than that of n^+ a-Si:H film due to a higher degree of crystallinity and a higher doping efficiency (see Fig. 2.6). The improvement of the TFT performance was verified by depositing TFTs with different contact layers in the source and drain regions and comparing the electrical properties. Figure 2.12 shows the transfer characteristics of the TFTs deposited with 200°C n^+ μc-Si:H, 260°C n^+ μc-Si:H and 260°C n^+ a-Si:H films as contact layers. The electrical experiments were conducted in a shielded metal box using Keithley source measure units (SMUs model 236) whose resolution is 10fA. For each group, four samples were tested. The scatter in the measurements among the group was less then 5%. The thickness of the contact layers in all of these TFTs was 50nm.

Compared to the TFT with 260°C n^+ a-Si:H film, the TFT with 200°C n^+ μc-Si:H shows suppressed leakage current in the low gate bias region. This effect is explained by reduced degree of diffusion of the phosphorous atoms at lower temperature [37]. However, there can be a second explanation for the lowered leakage current in the TFTs with low temperature n^+ μc-Si:H films. Section 2.3.7 already mentioned that the hydrogen in the PECVD plasma have a tendency to etch the film at the surface. Section 1.5.3 also mentioned that the surface of the silicon layer is almost instantly covered by gas molecules from the ambient atmosphere before the wafers are loaded in the vacuum chamber. The use of hydrogen dilution to grow microcrystalline films has a side effect of cleaning this undesirable layers at the surface by the means of plasma cleaning. The gas molecules that are attached to the surface get etched off by the hydrogen plasma, which removes the defect states at the surface. The subsequent film deposition on such a clean surface results in superior interface quality, leading to a low device leakage current.

When the gate is in the positive bias region, the TFT with 200°C n^+ μc-Si:H film showed improved sub-threshold slope due to reduced contact resistance in the source and the drain regions of the TFT. From the measurement data, the sub-threshold slope

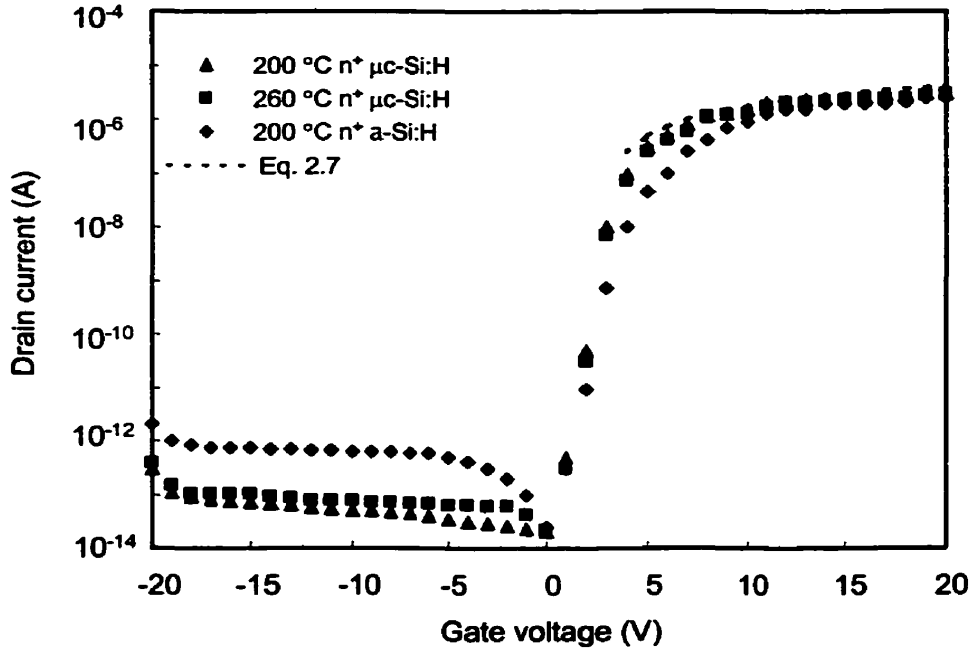


Figure 2.12: Transfer characteristics of TFTs fabricated with 200°C n^+ μc-Si:H, 260°C n^+ μc-Si:H and 260°C n^+ a-Si:H films as contact layers

of the TFT with 260°C n^+ a-Si:H film was extracted to be 0.58V/dec, whereas that of the TFT with 200°C n^+ μc- Si:H film was 0.47V/dec. Between the TFTs deposited with 200°C n^+ μc-Si:H and 260°C n^+ μc-Si:H films, the difference in device characteristics was almost negligible. In fact, the sub-threshold slope of the TFT with 260°C n^+ μc-Si:H film was also 0.47V/dec. This corresponded to the resistivity values of n^+ μc-Si:H as a function of the deposition temperature shown in Fig. 2.6.

The dotted line in Fig. 2.12 represents the simulated values from Eq. 2.9. This curve appears to be in a reasonably good agreement with the measured TFT on-current characteristics. The small discrepancy could be due to the fact that the field effect mobility of the transistor is not as high as it was assumed to be in section 2.1.

According to the measured current-voltage characteristics, the TFT with 200°C n^+ μc-Si:H film as contact layer appears to have ~0.9 cm^2/Vs.

In conclusion, the n^+ μc-Si:H film deposited at a low temperature (~200°C) has a higher degree of crystallinity than that of films deposited at a higher temperature (~400°C). And the TFT fabricated with this low temperature μc-Si:H film shows improved device characteristics.

2.4 Aluminum Gate Metallization

2.4.1 TFT Gate Metals (Mo, Cr, Cu or Al)

While the demand for displays and image sensor arrays with larger area and higher pixel integration is increasing, there remain several fundamental scaling issues associated with gate (and hence, interconnect) metallization of inverted-staggered hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) in the active matrix [8, 14, 16]. Presently, high refractory metals such as molybdenum (Mo) and chromium (Cr) are employed. Although these are stable materials, their high resistivity results in RC gate delays that impose constraints on the array size [8, 22, 26]. High conductivity metals such as copper (Cu) and aluminum (Al) are highly desirable, but their use is generally constrained by process considerations. Copper typically suffers from poor adhesion to glass and reacts with silicon and other PECVD films. These problems are typically overcome, although at the cost of increased process complexity, by depositing the Cu on indium tin oxide (ITO) coated glass for increased adhesion [51] or through self-passivation of the copper surface with Cu_2O_3 to avoid reactions during the PECVD process [52].

2.4.2 Motivation for Studying Aluminum Gate TFT

Although its resistivity is higher than that of Cu, Al adheres to glass substrates much better [53, 54]. More importantly, Al constitutes a mature process technology that is routinely used in VLSI. However, Al can suffer from the problems with hillock generation induced by subsequent process steps that are relatively high in temperature [53, 54]. In TFT fabrication, these include plasma-enhanced chemical vapor deposition (PECVD) of amorphous silicon nitride (a-SiN:H) dielectric and a-Si:H active layers. The presence of hillocks, which will be observed in the TFT samples considered in this section, increase the leakage current and reduce the field effect mobility. Furthermore, it can potentially lead to short-circuits between TFT terminals and interconnects. Although hillock formation can be minimized by passivating or capping the Al surface with a mechanically hard metal layer [53], using relatively low resistivity Al alloys [54, 55, 56], or anodizing the Al at room temperature prior to deposition of the PECVD films [57, 58], these solutions require additional processing steps associated with lithography, deposition, and annealing, thus adding to process complexity and cost.

It is well known that hillock formation depends on the film's microstructure and its thermal processing conditions [53 – 58]. The microstructure, to a large extent, can be controlled through careful selection of parameters associated with the sputter deposition process, and thus warrants a systematic characterization. This constitutes the focus of this work. Here, the sputtering deposition conditions for the Al gate metal are varied in terms of deposition temperature, process pressure, and DC power, and the performance of corresponding TFTs are compared in terms of leakage current and field effect mobility.

2.4.3 Surface SEM

To investigate surface morphology, Al films of thickness 150nm were deposited on Corning 7059 glass substrates by DC magnetron sputtering under different deposition conditions (Table 2.2). All of the films were subsequently annealed at 260°C for 12 hours to maintain consistency with the PECVD processes pertinent to TFT fabrication. Fig. 2.13 shows SEM micrographs of the Al surface for deposition temperatures of 150°C, 100°C and 30°C (room temperature), respectively. Here, the process pressure and the power were fixed at 10mTorr and 400W, respectively.

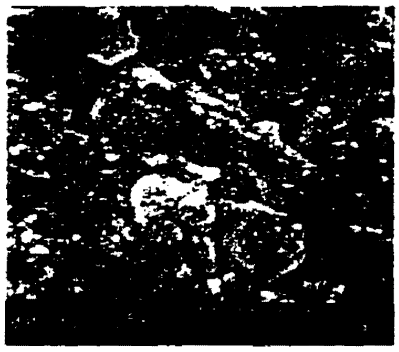
	Substrate temperature (°C)	Process pressure (mTorr)	DC Power (W)
Al	30, 100, and 150	5, 10, and 20	200, 300, and 400

Table 2.2: Deposition parameters of Al films deposited as the gate metallization.

With films deposited at 150°C, one can observe the characteristic appearance of tapered grains with domed tops, which are separated by voided boundaries [59]. This appearance is not as dramatic with films deposited at 100°C, although no significant reduction in void density is observed. However, films deposited at 30°C show a far smoother surface, as well as a significant reduction in the grain size. More importantly, it is observed that the boundaries are densely packed with no visible voids.

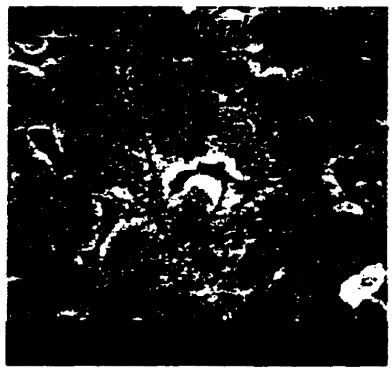
To investigate the likelihood of hillock formation in these films, another set of films was deposited at different process pressures. Fig. 2.14 shows the SEM micrographs of Al films deposited at process pressures of 5mTorr, 10mTorr, and 20mTorr, with the deposition power fixed at 400W. Here, a decrease in grain size with

(a)



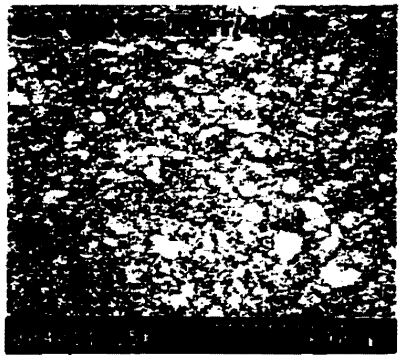
$\rho = 2.8\mu\Omega$-cm

(b)



$\rho = 2.9\mu\Omega$-cm

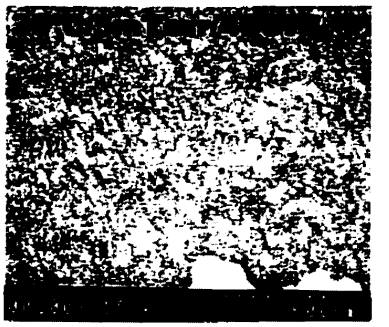
(c)



$\rho = 3.8\mu\Omega$-cm

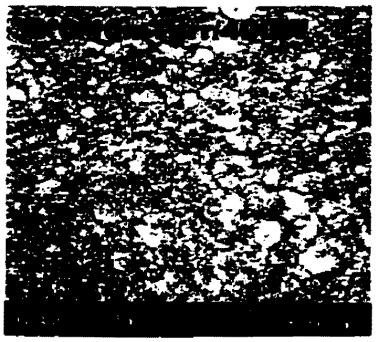
Figure 2.13: SEM micrographs of the Al films deposited at (a) 150°C, (b) 100°C, and (c) 30°C, and subject to thermal annealing at 260°C for 12 hours. The process pressure and power were fixed at 10mTorr and 400W, respectively.

(a)



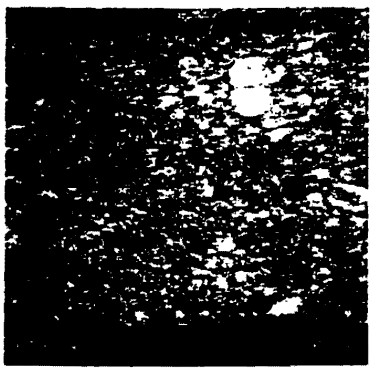
$\rho = 3.8\mu\Omega$-cm

(b)



$\rho = 3.8\mu\Omega$-cm

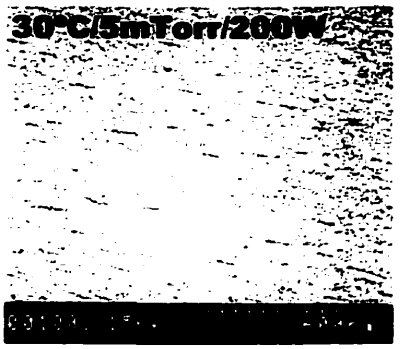
(c)



$\rho = 3.2\mu\Omega$-cm

Figure 2.14: SEM micrographs of the Al films deposited at (a) 5mTorr, (b) 10mTorr, and (c) 20mTorr, and subject to thermal annealing at 260°C for 12 hours. The deposition temperature and power were fixed at 30°C and 400W, respectively.

(a)

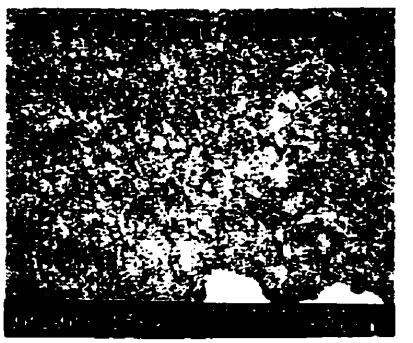


$\rho = 3.2\mu\Omega$-cm

(b)

$\rho = 4.0\mu\Omega$-cm

(c)



$\rho = 4.1\mu\Omega$-cm

Figure 2.15: SEM micrographs of the Al films deposited at (a) 200 W, (b) 300 W, and (c) 400 W, and subject to thermal annealing at 260°C for 12 hours. The process pressure and temperature were fixed at 5mTorr and 30°C, respectively.

decreasing process pressure is observed. In particular, films deposited at 5mTorr show a dense array of arbitrarily defined grain sizes with densely packed boundaries.

Maintaining the same process temperature, films under different sputtering power - but at a low process pressure (5mTorr) - were deposited in order to observe possible changes in film morphology. Fig. 2.15 shows SEM micrographs of Al films deposited at 200W, 300W and 400W, respectively, with the deposition temperature and the process pressure fixed at 30°C and 5mTorr. Here, it is observed that the surface of films deposited at 300W were smooth and free from the pinholes or voids, as compared to the samples deposited at 200W or 400W.

Figs. 2.13, 2.14 and 2.15 show that the conductivity of the film is higher when its grain size is larger. This is due to the fact that inside the grains the Al atoms form a crystalline structure. When the grain size is small, as seen in Figs. 2.15a) and 2.15b), the Al film is mostly amorphous, which leads to lower conductivity. The variation in conductivity of Al films in Figs 2.13 through 2.15 is similar to that of microcrystalline silicon in section 2.2.7. The only difference is the growth mechanism of the Al film and μc-Si:H film. For μc-Si:H films, crystallization happens due to the etching property of the hydrogen dilution. In Al deposition, the crystallization is highly dependent on the kinetic energy of the incoming atom at the growing surface. The kinetics of the PVD deposition process was briefly discussed in Chapter 1. It will be considered again when the deposition conditions of Mo films are discussed in Chapter 5.

2.4.4 Intrinsic Film Stress

All films, regardless of the deposition process method, possess intrinsic thin film stress. The film stress is discussed in Chapter 5 in more detail. Al metal is a very flexible metal, and thus, it does not have severe film stresses. The Al gate films deposited in this work showed small film stress in magnitudes ranging from 5.69MPa to

98MPa (Table 2.3). The film stress was measured using Ionic Systems Stressgauge (Fig. 5.8). The experimental setup is described in section 5.3. For these experiments, the Al films were deposited on two different wafers for each deposition condition. A total of seven readings were taken for each wafer. Among all the readings, the measurement scatter was less than 2%. The values in Table 2.3 are the average of all the readings. In all cases, the intrinsic stress in Al films became more tensile (or less compressive) after annealing at 260°C for 12 hours. The compressive stress, caused by ion bombardment during the deposition, is believed to be relaxed during the annealing period, which may lead to a rougher surface profile. This is discussed in the following section. The film stress measurement technique is discussed in Chapter 5 of this thesis along with the intrinsic film stress data of other films.

2.4.5 Surface Roughness

Based on the findings from the preliminary SEM surface morphologies, three Al films from Table 2.3 were re-fabricated so that further investigation of the degree of surface roughness in Al gate metals could take place. The surface atomic force microscope (AFM) images were obtained by non-contact mode on these films. To observe the hillock formation, the AFM imaging was done on the samples before and after the annealing at 260°C. In all results, both area arithmetic (Ra) and root mean square (RMS) roughness values are given. The scan area was 7μm x 7μm. There were 512 lines per image. The vertical resolution was 5Å.

Each of the samples was presented in two different styles, namely top view and 3-D view. The top view was useful for studying the shape of the surface features whereas the 3-D view was helpful for understanding the height information (surface roughness).

Deposition temperature (°C)	Deposition pressure (mTorr)	Deposition power (Watts)	Film stress before annealing (MPa)	Film stress after annealing (MPa)
150	10	400	-49.7	+5.69
100	10	400	-47.5	+5.00
30	10	400	-47.1	+10.5
30	5	400	-98.6	+14.7
30	20	400	-40.2	+33.6
30	5	200	-39.0	+57.6
30	5	300	-47.0	+22.5

Table 2.3: Intrinsic stress of Al films deposited at various deposition conditions, before and after annealing. (-: compressive, +: tensile)

Shown in Figs. 2.16 a) and b) are the AFM images of the Al gate film deposited at the process temperature of 150°C, with a pressure of 10mTorr, and a DC sputtering power of 400W. As it can be expected from the SEM image in Fig 2.13a), the surface was very rough and the RMS value was 76.9nm, which was higher than the thickness of the active channel layer (50nm). The 3-D image displays very large grain features. The surface roughness information of the same film after annealing at 260°C for 12 hours is shown in Figs. 2.16 c) and d). As it was predicted from the intrinsic film stress data in section 2.3.4, after the annealing, the surface became rougher (RMS: 82.8nm). In Table 2.3, the film stress of 49.7MPa compressive became 5.69MPa tensile after annealing.

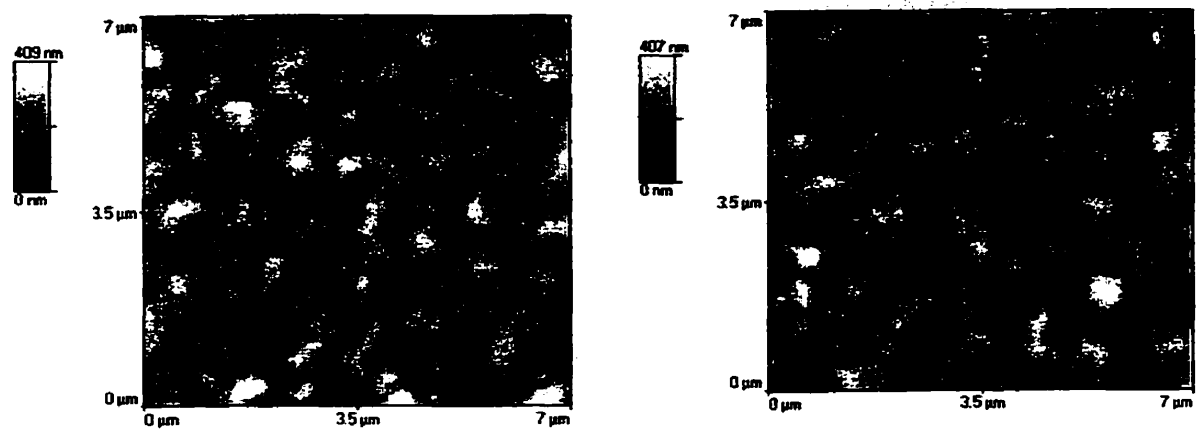
As it was already shown in Fig 2.13, the deposition temperature has a strong effect on the surface roughness. Fig. 2.14 demonstrates that the deposition pressure also plays an important role. Shown in Fig. 2.17 are the AFM images of the Al gate film in Fig 2.14a) (deposition temperature: 30°C, pressure: 5mTorr, and DC sputtering power: 400W) before and after the annealing. One observation was that the grains on the surfaces were much smaller in size. Just as in Fig 2.16, the degree of roughness increased slightly after annealing from the RMS value of 4.8nm to 5.4nm.

The AFM images of the best film from Fig. 2.15 (deposition temperature: 30°C, pressure: 5mTorr, and DC sputtering power: 300W) are shown in Fig. 2.18. Before annealing, the surface roughness was RMS = 2.6nm. However, after annealing, the RMS increased to 3.6nm as a result of hillock formation.

To investigate the impact of gate surface morphology on TFT performance, TFTs were deposited on these Al gate films. The following sections will discuss the effect of surface roughness on the device performance.

2.4.6 Gate/Gate Dielectric Interface (Cross-Section SEM)

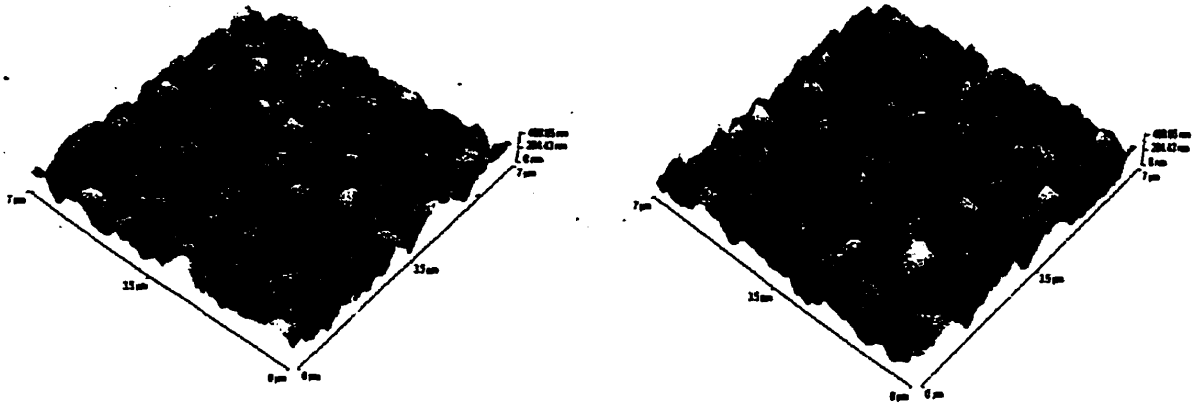
TFTs with Al gate metallization were fabricated and characterized for their current-voltage and transfer characteristics. In this section, before the completion of the TFT fabrication, the gate metal and gate insulator interface must be discussed. For comparisons, the two extreme ends of Al gate metallization spectrum will be presented. Figure 2.19 shows SEM cross sections of the gate/insulator interface of TFTs fabricated at the deposition conditions of 150°C, 10mTorr and 400W. The Al gate film in this figure is also presented in Fig. 2.13a) and Fig. 2.16. Here, the degree of roughness seems to agree with that presented in earlier figures. As one can clearly see, the gate dielectric layer (a-SiN:H) deposited by CVD process, follows the surface profile of the



(a) (c)

Before annealing
Ra: 62.5nm
RMS: 76.9nm

After Annealing
Ra: 68.4nm
RMS: 82.8nm



(b) (d)

Figure 2.16: AFM images of Al gate film deposited at 150°C, 10mTorr, and 400W - before annealing a) top view, b) 3-D view and after annealing at 260°C c) top view, d) 3-D view.

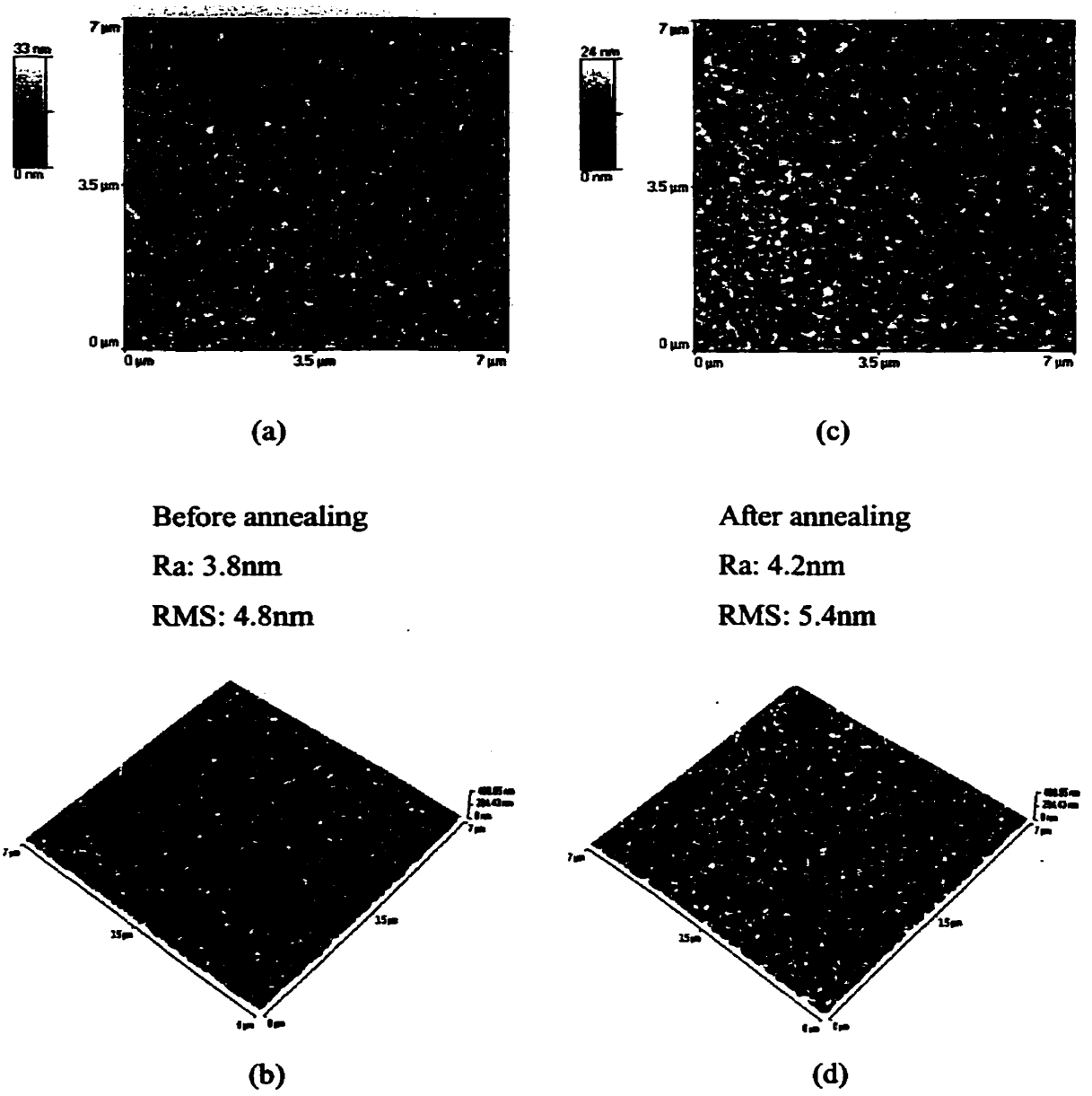


Figure 2.17: AFM images of Al gate film deposited at 30°C, 5mTorr, and 400W - before annealing a) top view, b) 3-D view and after annealing at 260°C c) top view, d) 3-D view.

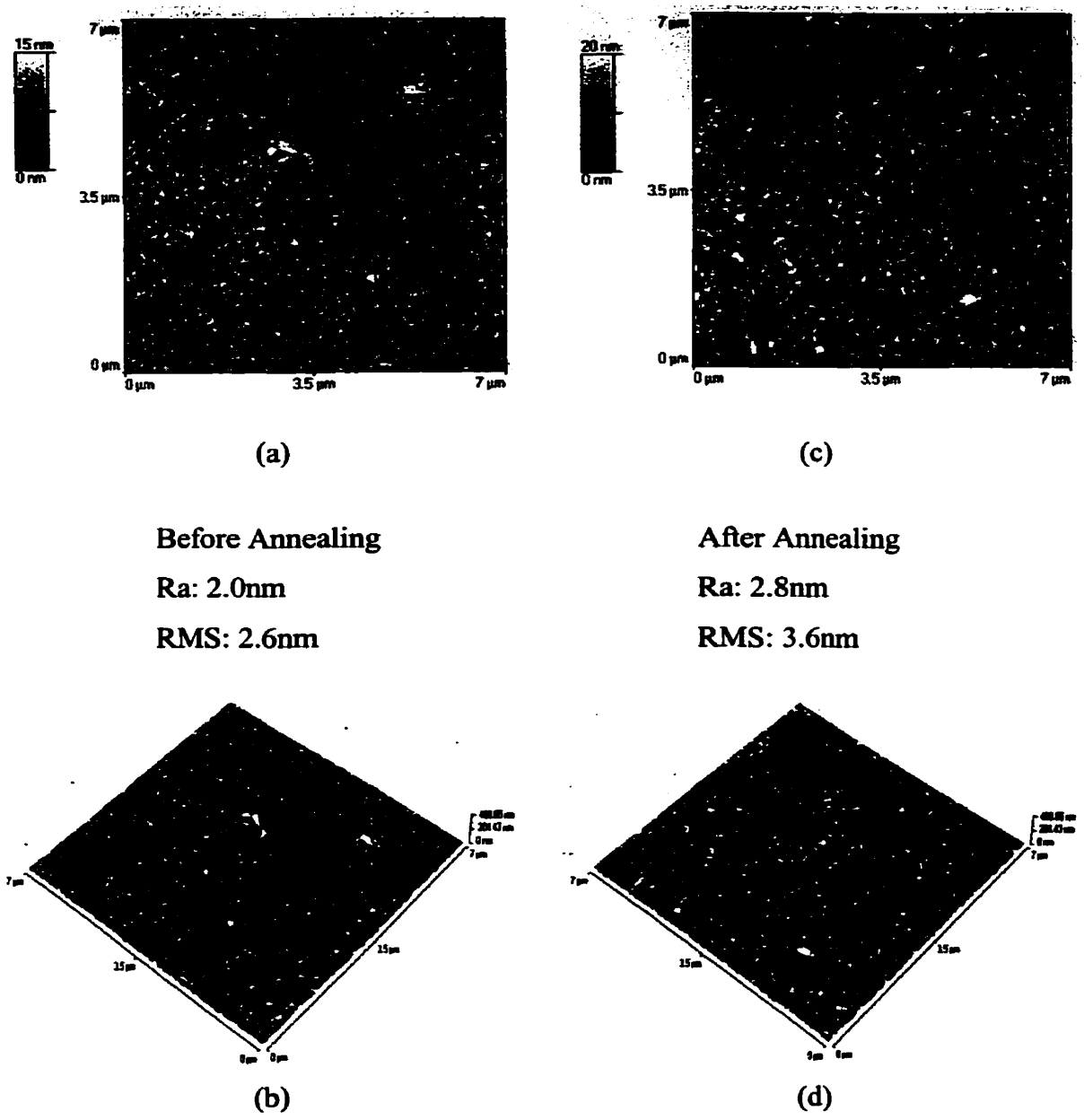


Figure 2.18: AFM images of Al gate film deposited at 30°C, 5mTorr, and 300W - before annealing a) top view, b) 3-D view and after annealing at 260°C c) top view, d) 3-D view.

gate metal. The active channel layer will be deposited on top of this rough gate nitride surface.

Figure 2.20 shows the cross-section SEM of the Al gate film at the other end of the spectrum of surface roughness deposited at 30°C, 5mTorr and 300W. Again, the degree of roughness shown in this figure is comparable to those seen earlier in Fig. 2.15b) and Fig. 2.18. The interface between the Al gate metal and the gate dielectric is sharp and smooth, allowing the gate dielectric to have a very smooth surface.

Further TFT fabrication steps were carried out in order to compare the device performance. In section 2.4.7, the TFTs with gate films in Figs. 2.19 and 2.20 will compare the device leakage current, the shift in the threshold voltage, and the mobility.

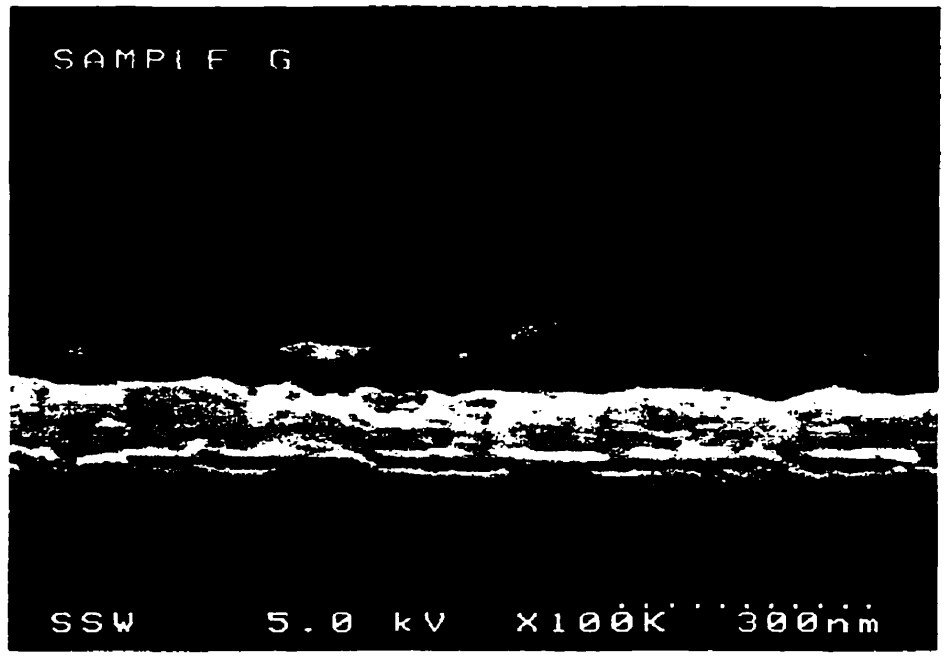


Figure 2.19: Cross-section SEM image of Al gate and gate dielectric interface. Al gate metal was deposited at 150°C, 10mTorr and 400W.

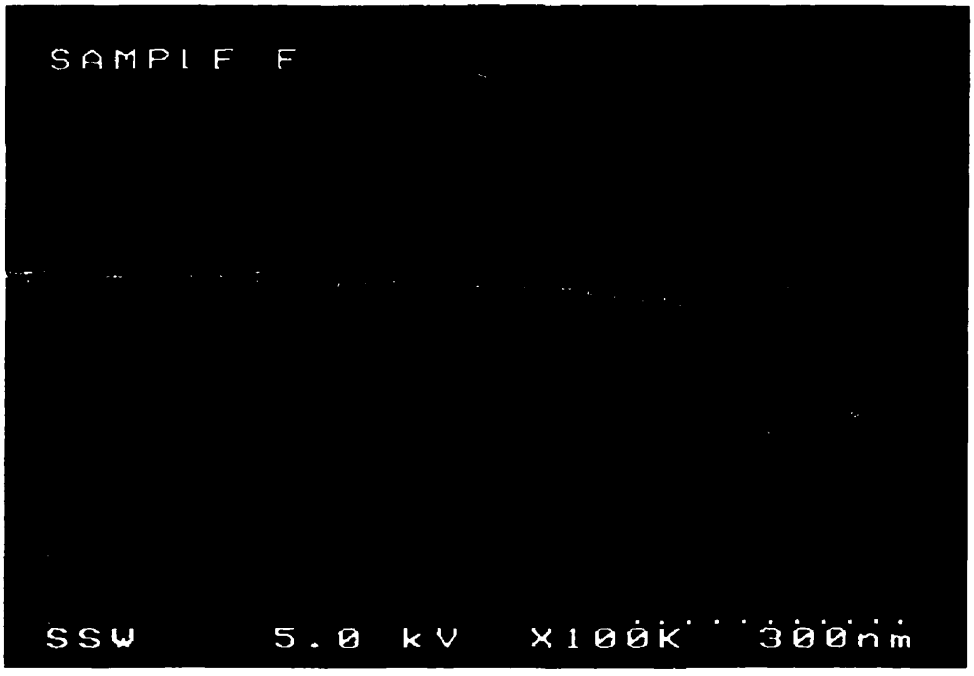


Figure 2.20: Cross-section SEM image of Al gate and gate dielectric interface. Al gate metal was deposited at 30°C, 5mTorr and 300W.

2.4.7 TFT Performance Comparisons

As shown in Fig. 2.21, a TFT with Al gate metal deposited at 150°C/10mTorr/400W, yielded a significant degradation in leakage current (~1pA) and mobility (0.77cm^2/Vs). The reasons for the degradation are clear, based on observations of the cross-section SEM (see Fig. 2.19). Here, one can observe a high surface roughness of the a-SiN:H gate insulator, and hence the TFT channel, which is caused by hillock formation on the Al gate. Note also that the corresponding shift in threshold voltage is large. The stability behaviour ($\sqrt{I_{DS}}$ vs. V_{GS}) for different time durations of electrical stress is shown in Fig. 2.22. The square root of the transistor saturation current, $\sqrt{I_{DS}}$, (see Eq. 2.8) as a

function of applied V_{GS}, when $V_{GS} = V_{DS}$, can be used to extrapolate the threshold voltage of the TFT. This serves as a measure for the metastable shift in threshold voltage with extended bias durations. After one-hour bias stress of +25 V applied to the gate, the shift in threshold voltage is $\Delta V_T \sim 5$ V. For this Al gate film, four devices were sampled. The scatter in the measurement was within 10%.

In contrast, the transistors with gate metallization deposited at 30°C/5mTorr/300W (from Fig. 2.20) show a low leakage current (~10fA at low V_{DS}), an ON/OFF current ratio better than 10^8, and a mobility of 1.0 cm^2/Vs (see Fig. 2.23). These values are comparable to those reported for TFTs with anodized Al gate [57]. In these transistors, the shift in threshold voltage is $\Delta V_T \sim 2.3$ V.

The large shift in threshold voltage in Fig. 2.22 can be attributed to the metastability in the active a-Si:H layer induced by large (and perhaps even singular) localized electric fields stemming from surface non-uniformity in the channel. The same reasons hold true for the high leakage current in Fig. 2.21. Large localized electric fields in the active region, stemming either from surface non-uniformities or applied bias (large V_{DG}), lead to an electric field dependent Frenkel-Poole type carrier generation in the active region [60]. Thus, the leakage current increases with increasing interface roughness as well as high reverse gate voltages. The field effect mobility in these transistors, retrieved from the associated transfer characteristics, clearly shows the impact of surface roughness on mobility degradation. For this Al gate film, eight devices were sampled. The scatter in the measurement was within 5%.

In conclusion, Al films can be used to replace the Mo films as the gate metal of the TFTs. To minimize the surface roughness stemming from the Hillock formation, all deposition parameters have to be fine-tuned. In this work, it was demonstrated that a smooth (RMS = 3.6nm) Al gate film can be achieved by carefully selecting the deposition temperature, the pressure and the sputtering power. For the sputtering system

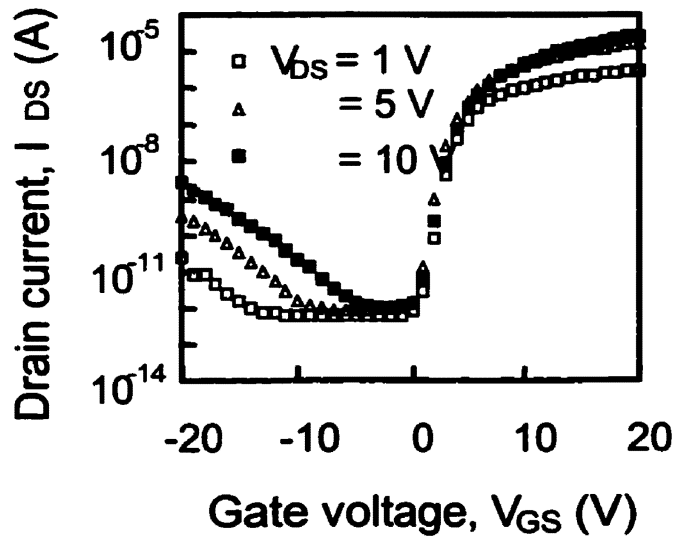


Figure 2.21: Transfer characteristics of a TFT fabricated with Al gate metal in Fig. 2.19.

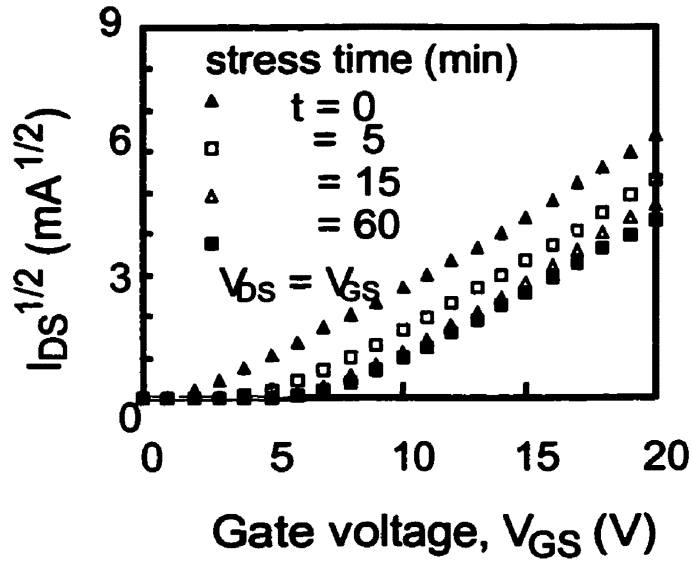


Figure 2.22: Shift in threshold voltage of a TFT fabricated with Al gate metal in Fig. 2.19.

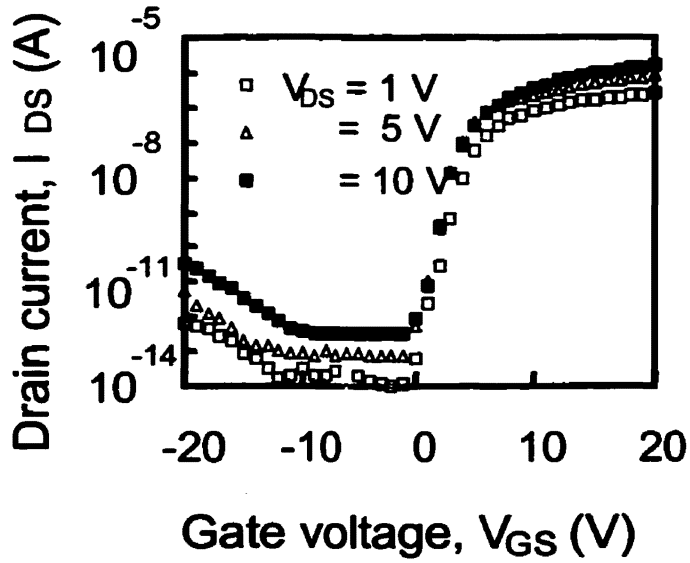


Figure 2.23: Transfer characteristics of a TFT fabricated with Al gate metal in Fig. 2.20.

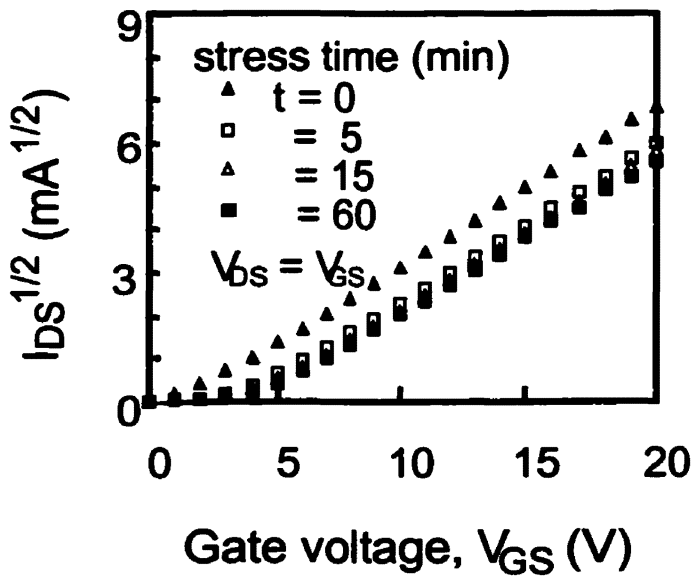


Figure 2.24: Shift in threshold voltage of a TFT fabricated with Al gate metal in Fig. 2.20.

that was used for this work, the deposition parameters are: temperature = 30°C, process pressure = 5mTorr, and DC sputtering power = 300W.

Another notable observation made from this work is the variation in the Al film resistivity. Al films are most often used as the final metal for integrated circuits. In this case, the surface roughness is not as important. The final metallization is used as the interconnects between different nodes in the integrated circuits. For this purpose, low resistivity is highly desirable. Again, the deposition parameters of Al films should be chosen so that the grain sizes are large, and hence, the film resistivity is low. For the PVD chamber used for this work, this condition is best achieved ($\rho = 2.8\mu\Omega$-cm). when the deposition temperature is 150°C, process pressure = 10mTorr, and DC sputtering power = 400W.

Chapter 3

Leakage Current of Mo/a-Si:H Schottky Diodes

The x-ray detection mechanism in this project is based on the photoelectric effect of x-ray photons with the heavy metal. The x-ray generated charge is stored in the internal pixel capacitance. Thus, it is important that the leakage current of the Schottky diode is small so that the collected charge is not dissipated until it is transferred to the data line by the TFT. Schottky interfaces are well known for inconsistency. This work was started in order to investigate the Schottky diode leakage current behavior.

3.1 Large Variation in Schottky Interface I-V Characteristics

As expected, the Schottky diodes deposited for this work showed a large variation in the I-V characteristics. Shown in Fig. 3.1 is one of the mask designs created just for this work. All devices in this mask are Schottky diodes. The dimensions of all devices are

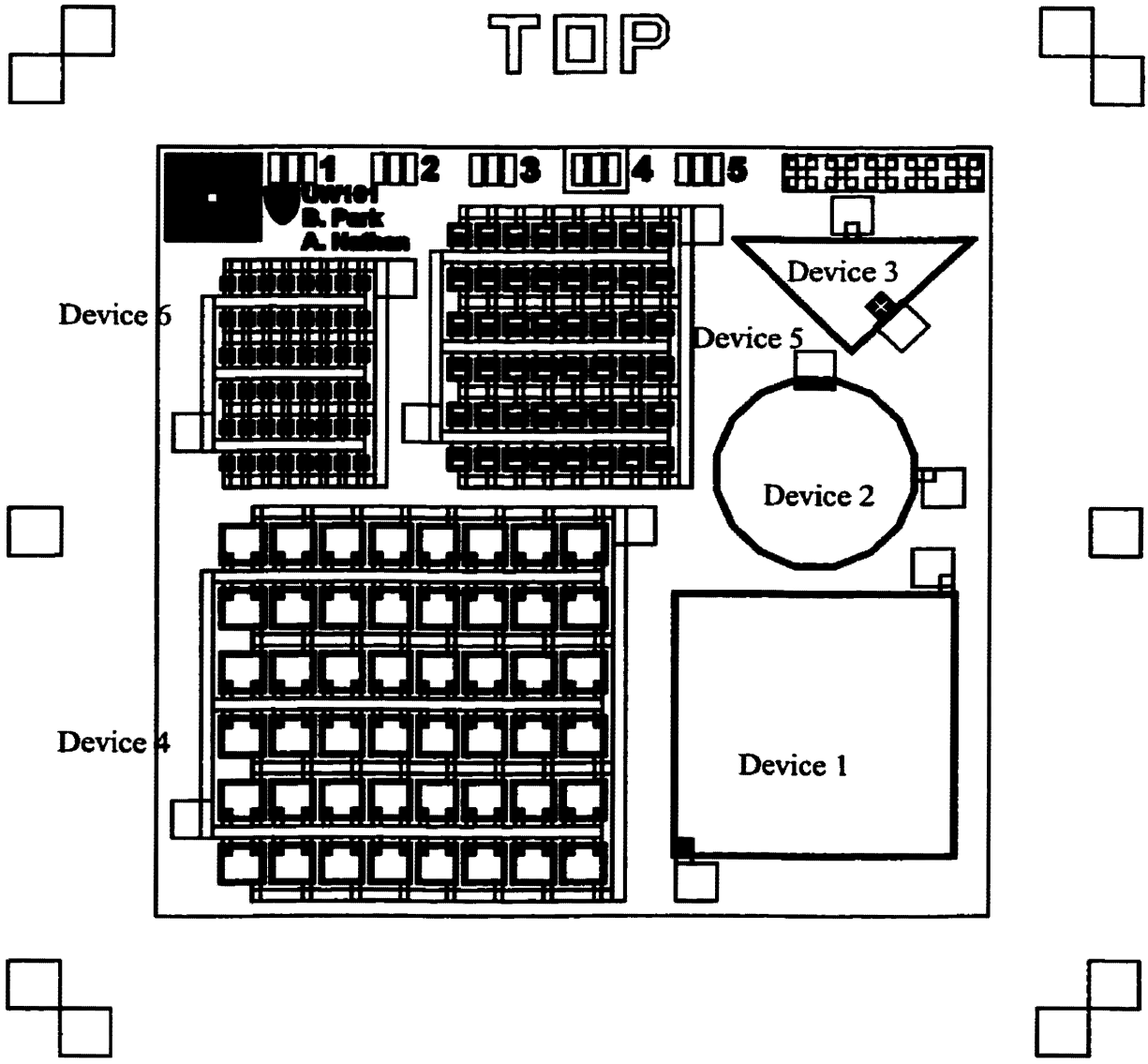


Figure 3.1: A mask layout for Schottky diode leakage current studies.

Device 1	700μm x 700μm
Device 2	Radius = 250μm
Device 3	Width = 600μm Height = 300μm
Device 4	100μm x 100μm x 48 (number of diodes)
Device 5	50μm x 50μm x 48 (number of diodes)
Device 6	26μm x 26μm x 48 (number of diodes)

Table 3.1: Dimensions of the devices in the mask layout shown in Figure 3.1.

listed in Table 3.1. In the devices 4 to 6, 48 Schottky diodes of the same geometries were connected in parallel. After the I-V characteristics were recoded by Keithley SMUs, the curve was divided by the number of devices. This had to be done because measuring the leakage current of very small devices can be difficult with the SMUs' measurement resolution of 10fA.

The current density of a number of devices of type 1 is shown in Fig 3.2. As one can notice very easily, there is a large variation in the leakage currents of the Schottky diodes (among only seven samples). These diodes are all from the same wafer. The magnitude of the difference in the leakage current from one device to another can be as large as one order. Also, the slope of the leakage current as a function of the reverse bias can be very different from one device to another. The rest of the devices (2 to 6) show roughly the same variations. It is, therefore, unscientific to compare the

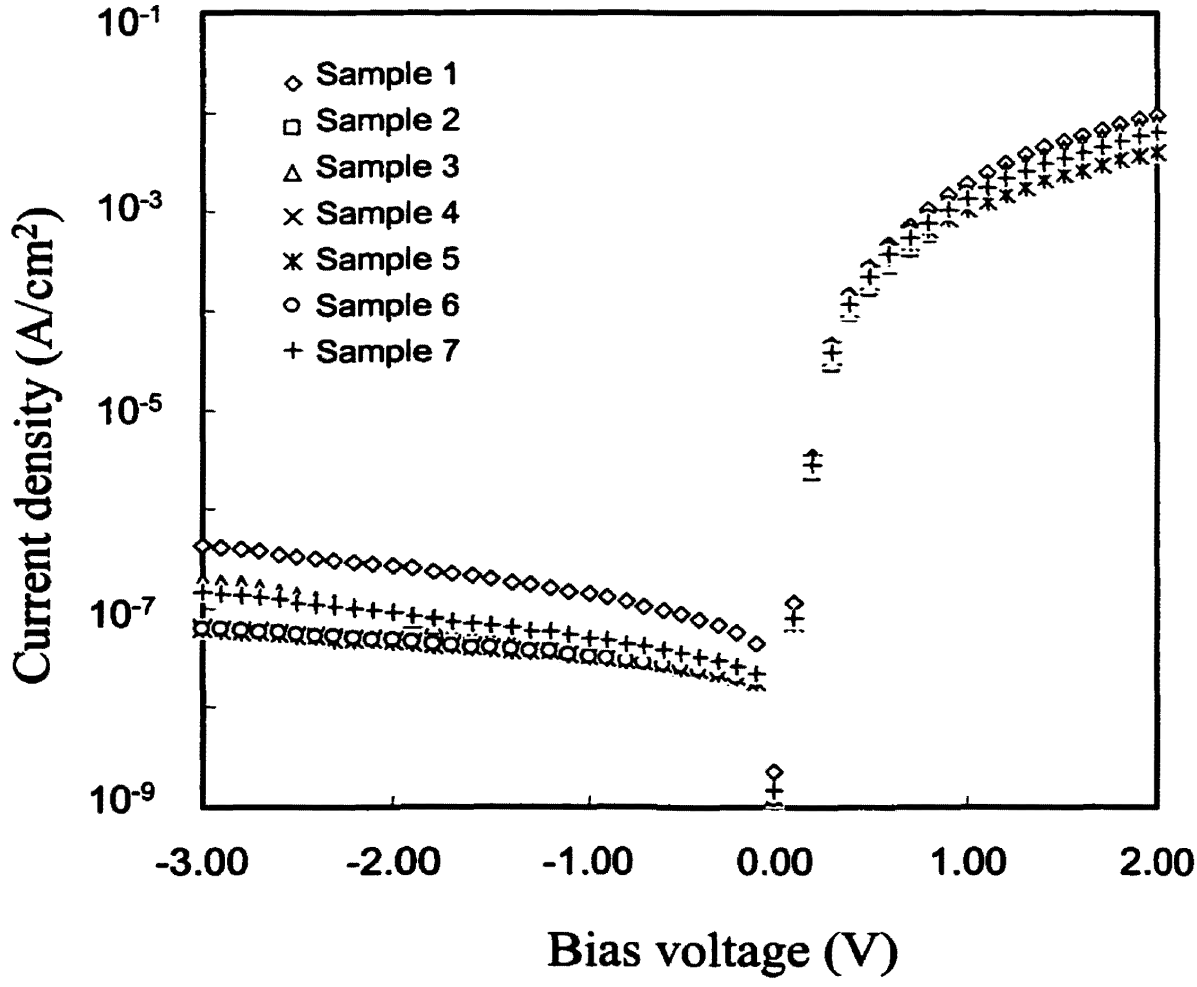


Figure 3.2: Current density of device 1 (Schottky diode) in Fig. 3.1.

characteristic of just one device to those of another to extract conclusions. From this point on, all leakage current will be an average of many devices. Due to the wide variation of the Schottky interface, minor details are not to be rigorously discussed. Only the outstanding deviation from the norm will be addressed.

3.2 Modified Schottky Diode Fabrication Process

The old Mo/a-Si:H Schottky diode fabrication was a 4-mask process. This process was modified to be a 5-mask process. In the old process, the silicon layers underneath the top metal bond pad were not etched out by KOH solution (see Fig 3.3). In terms of fabrication process complexity, this old process was easier to fabricate. However, this process has the following issues. After opening via (contact windows) with mask 4, the wire bonding has to be done on 500nm think Mo (top electrode) and 100nm thin Cr (bottom electrode). Both are heavy metals, which makes it difficult for the bonding wire to strike and make a firm contact on. Also, when characterizing for leakage current, the extra Schottky interface under the bonding pad will also contribute some current. To rectify these issues, a new 5-mask fabrication sequence was developed (see Fig 3.4). In this new fabrication process, mask 2 patterns only the detection area, not the top metal bonding pad. After the protection nitride was patterned on the top metal, the wafer was dipped into KOH solution. This wet etching step removes the silicon layers from the entire wafer except for the areas directly under the protection nitride. Then, mask 4 opens contact to the top metal, and finally mask 5 patterns the final metal, Al. This process allowed the wire bonding to be done on Al film, not on heavy metals. The detection area was then exactly what was defined by mask 2. Mask 5 for patterning final metal was not really an extra mask when this process was integrated with the TFT process for fabricating pixels. In pixel fabrication, as it will be shown in Chapter 4, the final metal for both TFTs and Schottky diodes can be deposited at the same time.

In an attempt to compare the device performances of the two fabrication processes, these two different structures were deposited such that there are many Schottky diodes connected in parallel. The mask designs for this work are in Appendix A (See Figs. A.3 and A.4). For the old process, 35 diodes were connected in parallel.

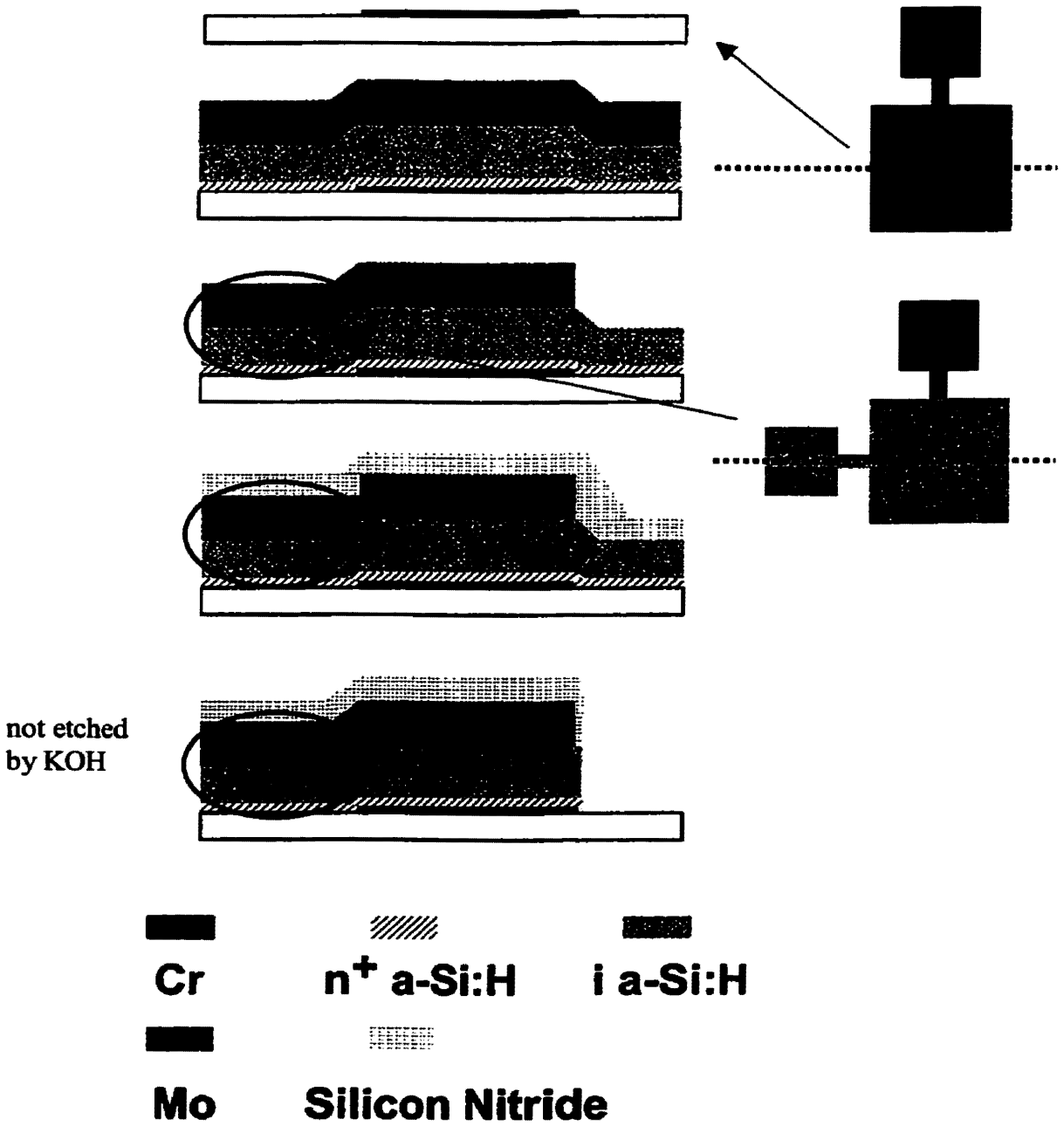


Figure 3.3: Old fabrication sequence of mo/a-Si:H Schottky diodes, adapted from [33].

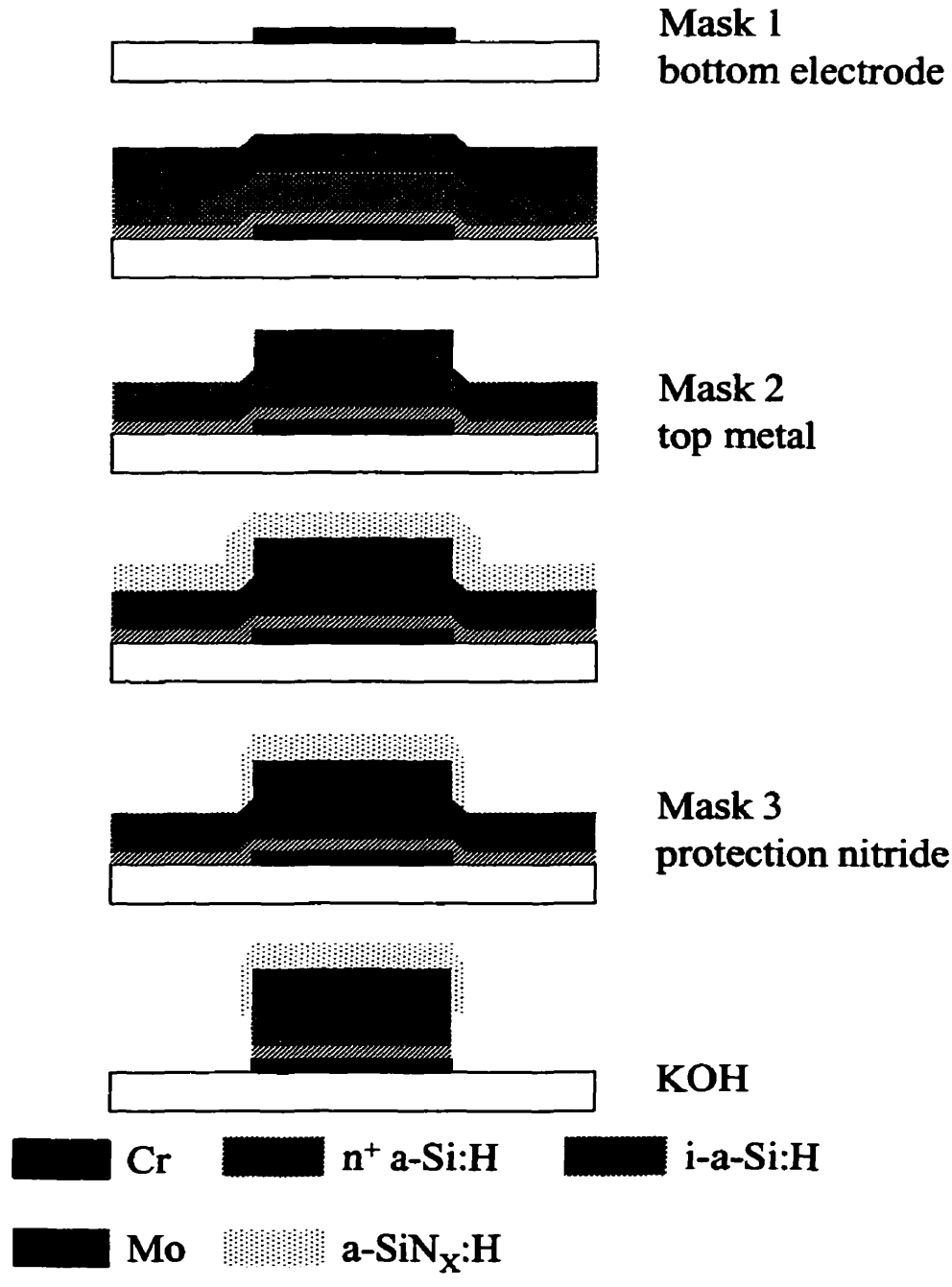


Figure 3.4: New 5-mask Mo/a-Si:H Schottky diode fabrication sequence.

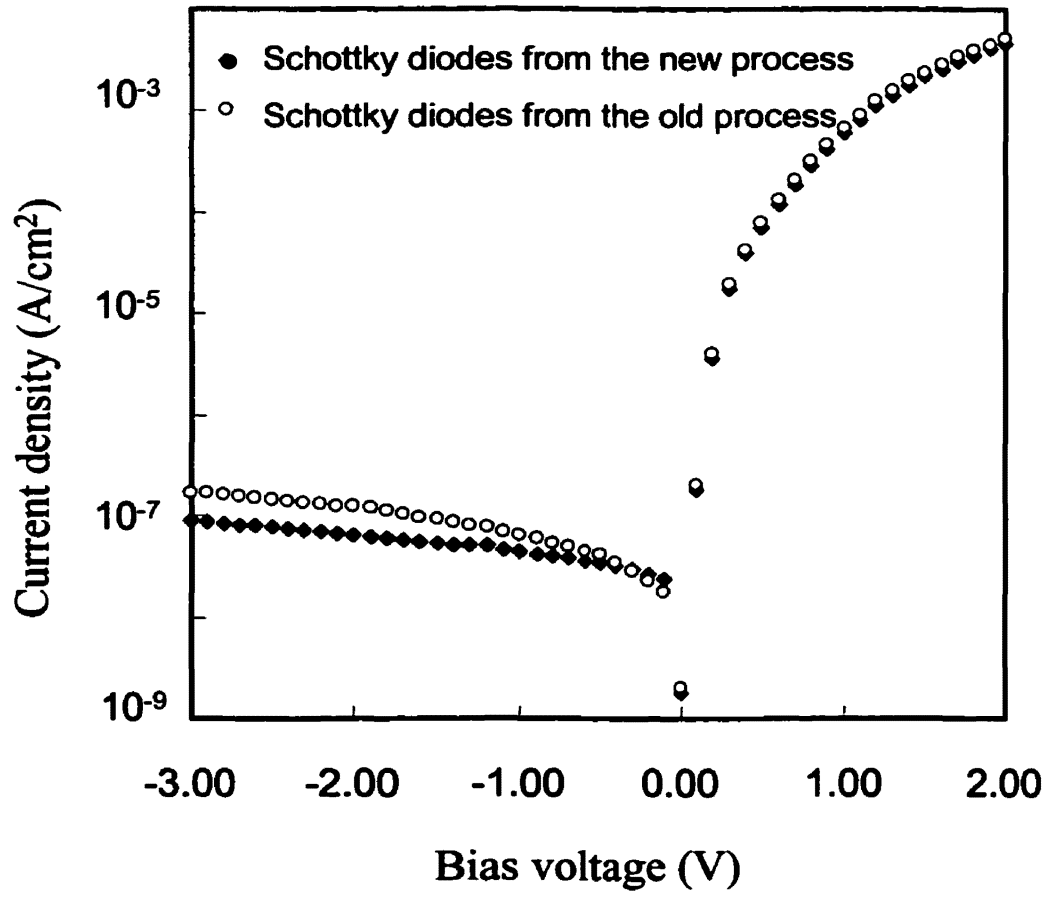


Figure 3.5: Comparison of the current density of Schottky diodes, fabricated with the old 4-mask process and the modified 5-mask process.

The area of the diodes was 200μm x 200μm. But, as mentioned before, there was an extra Schottky interface area in this design. The extra area preserved for wire bonding was 80μm x 80μm (see Fig. A.4). There was also an area of 40μm x 40μm which was used to connect the bonding pad to the detection area. The total extra Schottky interface area was then 8000μm^2. This area was not included in the calculation for current

density. Compared to the performance of the diodes of the new process, whose Schottky interface area was exactly 200μm x 200μm, it showed slightly higher leakage current (Fig. 3.5). In the new Schottky diode process, 48 diodes were connected in parallel (see Fig A.3). In both processes, since many diodes were connected in parallel, and the yield at the university laboratory was not very high, finding a working die was not easy. The curves in fig. 3.5 were the averages of 8 different dies of the old and the new processes, each containing 35 and 48 diodes in one die, respectively.

3.3 Scaling the Device Size

The average value of many Schottky diodes fabricated with the new process showed lowered leakage current, compared to that of diodes from the old process (Fig. 3.5). However, due to the wide variation in leakage current of the Schottky interface, as seen Fig. 3.2, it was not adequate to draw conclusions from just one experiment.

To better understand the leakage current behavior of Schottky diodes, another measurement was made. The leakage currents of devices 4, 5 and 6 in Fig. 3.1 were measured and compared with that of the diode in Fig. 3.5. All diodes used in this measurement were fabricated with the new modified process. Figure 3.6 shows the I-V characteristics of these diodes with different sizes. Finding working devices whose dimensions were smaller than 100μm x 100μm was even more difficult due to the low yield. In this measurement, for the devices smaller than 100μm x 100μm, only 4 different dies were averaged.

The 100μm x 100μm Schottky diode was showing very similar behavior to that of the 200μm x 200μm Schottky diode. As the device size became smaller, a deviation from the norm was observed. In the case of the 50μm x 50μm diode, the leakage current started to increase drastically from roughly –1V bias voltage. This effect was more

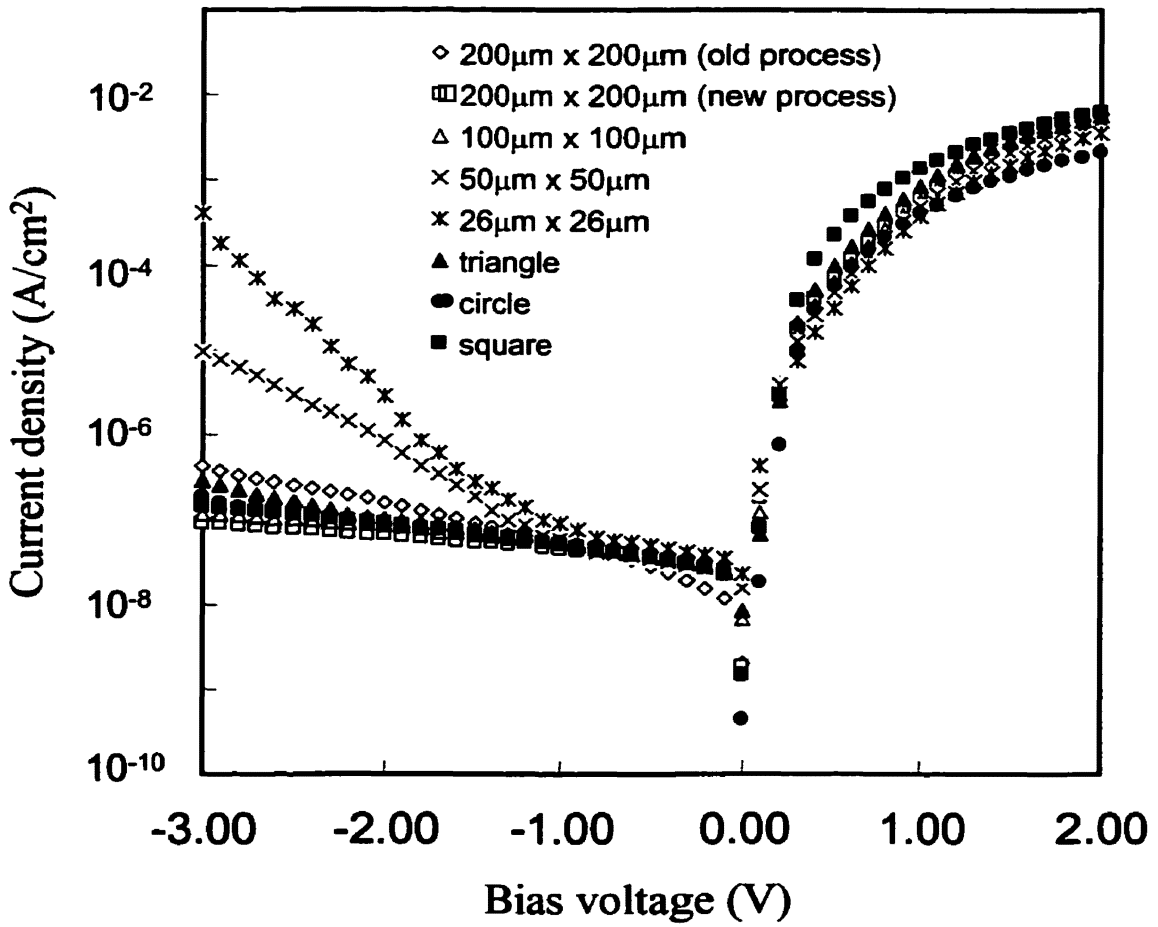


Figure 3.6: Leakage current density of the Schottky diodes with different dimensions.

prominent for the diode whose dimensions were 26μm x 26μm. This dramatic increase in the leakage current was too large to be considered part of the usual variation in the Schottky diodes. Also, the inverse correlation between the size of the diode and the increase in the leakage current suggested that it was unlikely to be just a simple experimental error. The strong dependence of this leakage current to the reverse bias

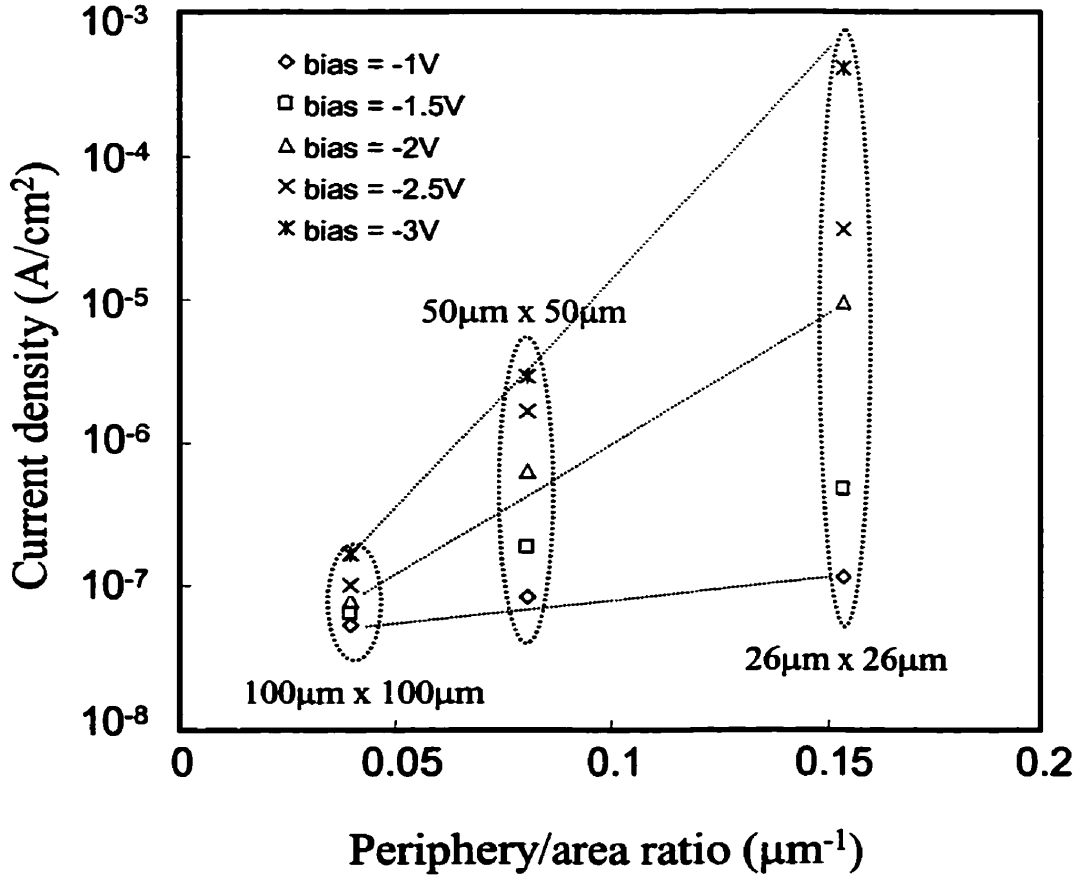


Figure 3.7: Leakage current density as a function of periphery/area ratio (μm^{-1}).

voltage indicated that the devices had tunneling characteristics. All diodes were fabricated in the same fabrication process. All films were deposited in the same CVD and PVD processes. They should have the same Schottky barrier height. Then, the only difference in these diodes was the periphery to area ratio. Shown in Fig. 3.7 is a plot of the leakage current density as a function of periphery/area ratio. Five points (-1V ~ -3V) from the reverse bias range are presented. When plotted against the logarithmic scale of the current density, the periphery to area ratio appears to have a relationship which

follows a straight line. Extrapolating from the straight lines in Fig. 3.7, one conclusion is that the leakage current density generated by the Schottky interface only (assuming that the interface is ideal) is approximately $\sim 10^{-7}$ A/cm^2. Again, the step dependence of the leakage current to the reverse bias voltage suggests that for small devices with high periphery/area ratio the dominant conduction mechanism is tunneling. The transport mechanism will be discussed further in the following section.

This rapid increase in leakage current as a function of reverse bias voltage does not occur in large devices. Also shown in Figure 3.6 are the current density curves of devices 1, 2 and 3 from Fig. 3.1. The curves in this figure are the averages of eight devices of the same kind. Table 3.2 lists the area, the periphery and the periphery/area ratio of all the diodes in Figs. 3.6.

Shape	dimensions	Area (μm^2)	Periphery (μm)	Ratio, periphery/area (μm^{-1})
Square	700μm x 700μm	490,000	2,800	0.00571
Circle	Radius = 250μm	196,250	1,570	0.008
Triangle	Base = 600μm, height = 300μm	90,000	1,448	0.016
Square	200μm x 200μm	40,000	800	0.02
Square	100μm x 100μm	10,000	400	0.04
Square	50μm x 50μm	2,500	200	0.08
Square	26μm x 26μm	676	104	0.154

Table 3.2: The periphery to area ratio of the Schottky diodes in Figs. 3.6 and 3.7.

3.4 Transport Mechanisms across Mo/a-Si:H Schottky Barrier

A Schottky barrier junction includes an abrupt termination of the semiconductor crystal. The silicon surface contains interface states due to incomplete covalent bonds, which can lead to trapped charges at the metal-semiconductor interfaces (Fig. 3.8). In addition to these interface states, the boundary between the metal and the silicon is not atomically sharp. There are a few monomolecular layers at the interface that are neither metal nor silicon. Furthermore, because the wafer is brought out from a vacuum chamber to the atmosphere after silicon layers are deposited, ~20Å thick native oxide forms on the surface. Electrons will have to tunnel through this thin layer, which affects

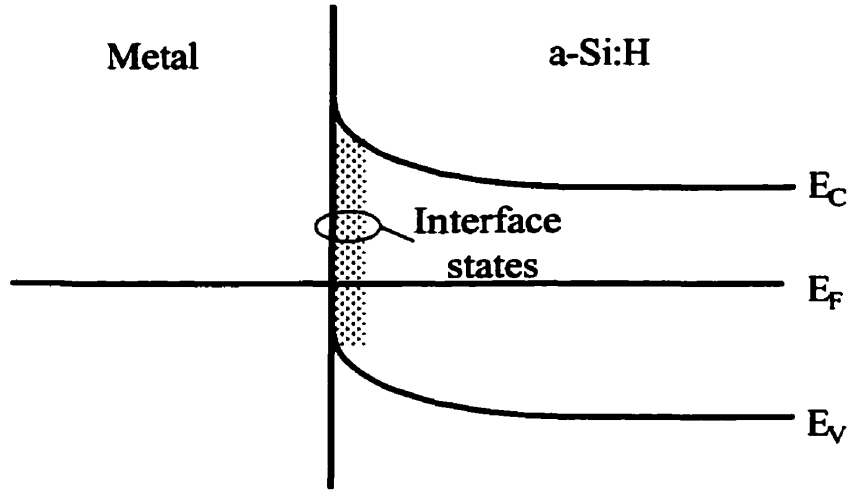


Figure 3.8: Energy band diagram of Schottky interface. The interface states at the Schottky barrier are caused by abrupt termination of the silicon bonds. This is an intrinsic property of the Schottky interface.

The barrier to current transport through the junction. Thus, the Schottky interface exhibits poor reproducibility compared to the p-i-n interfaces. This property of the Schottky diode will be further discussed in Chapter 3 as a discrete device and in Chapter 6 as in a fixed pattern noise within an array.

Despite the disadvantage of poor reproducibility of the Schottky interface, using Schottky diodes in pixels to detect x-rays has an advantage over using the p-i-n diodes. When an energetic electron is generated by absorption of an x-ray photon and ejected to the depletion layer of silicon, there can be a large gain due to the high energy of the electron. The energy of electron, E_e, is

$$E_e = E_{hv} - E_b \qquad \{3.1\}$$

where E_{hv} is the energy of photon and E_b is the electron binding energy. Since $E_{hv} >> E_b$,

$$E_e \approx E_{hv}. \qquad \{3.2\}$$

This ejected energetic electrons cause electron multiplications in the depletion region. The thickness of the Mo layer should be chosen as the best compromise between the absorption of the x-ray photons and the ejection of the energetic energy. The thicker the Mo layer, the higher the absorption of x-ray photons but lower the ejection of energetic electrons and vice versa. For the x-ray range of 40kVp to 100kVp, Mo thickness of 500nm-600nm was observed to yield the best results [30, 31]. The number of absorbed photons, N_{ab}, is

$$N_{ab} = N_i - N_{na} \qquad \{3.3\}$$

where N_i is the number of incident photons and N_{na} is the number of unabsorbed (passing through) photons [61]. Eq. 3.3 can be rewritten as

$$N_{ab}/N_i = 1 - N_{na}/N_i. \qquad \{3.4\}$$

The gain, G, due to the electron multiplication is

$$G = N_{me}/N_{ab} \qquad \{3.5\}$$

where N_{me} is the number of measured electrons. According to [30, 31], the Schottky diode exhibits a multiplication of ~1000 (number of measured electrons to the number of absorbed photons) over the x-ray source voltage range of 40kVp ~ 100kVp. The extrinsic quantum yield, η, is defined as

$$\eta = N_{me}/N_i \qquad \{3.6\}$$

and at 40kVP, the extrinsic quantum yield was measured to be ~300 [30, 31]. Then,

$$\eta = N_{me}/N_i = 300 = N_{me}/N_{ab} \cdot N_{ab}/N_i = 1000(1 - N_{na}/N_i) \qquad \{3.7\}$$

or,

$$0.3 = 1 - N_{na}/N_i \qquad \{3.8\}$$

which means

$$N_{na}/N_i = 0.7 \qquad \{3.9\}$$

In other words, at x-ray energy of 40kVp, only 30% of the incident photons are absorbed. The same calculation can be repeated for x-ray source voltage of 100kVp with the extrinsic quantum yield of 60.

$$0.06 = 1 - N_{na}/N_i \qquad \{3.10\}$$

At higher x-ray source voltage, more x-ray photons penetrate the Mo layer, thus the extrinsic quantum yield is lower. But the observed electrons have more energy, which leads to higher electron multiplication. If the molybdenum can be replaced with even heavier metal, such as tungsten, whose atomic weight and density are higher than that of Mo, the absorption of incident photons would increase. However, the work function of tungsten is 4.5 Φ/eV which is lower than the work function of molybdenum, 4.6 Φ/eV [62]. According to the diode equation

$$I = I_0(e^{qV/kT} - 1) \qquad \{3.11\}$$

and

$$I_0 \propto e^{-q\Phi/kT} \qquad \{3.12\}$$

a small decrease in the work function will lead to an exponential increase in the diode current. Either palladium or platinum would be a good candidate for the Schottky metal since they both have a high density and a high work function. However, the drawback is that these materials are expensive and hard to process in fabrication.

The electrical transport mechanisms across the Schottky barrier are illustrated in Fig. 3.9. Electron excitation over the Schottky barrier is referred to as thermionic emission, whose current density, J_O, can be expressed as [34];

$$J_O = A^* T^2 \exp(-e\Phi_B / kT) \qquad \{3.13\}$$

where A^* is the Richardson's constant (120A/cm^{2}K^2 for free electrons in vacuum) and

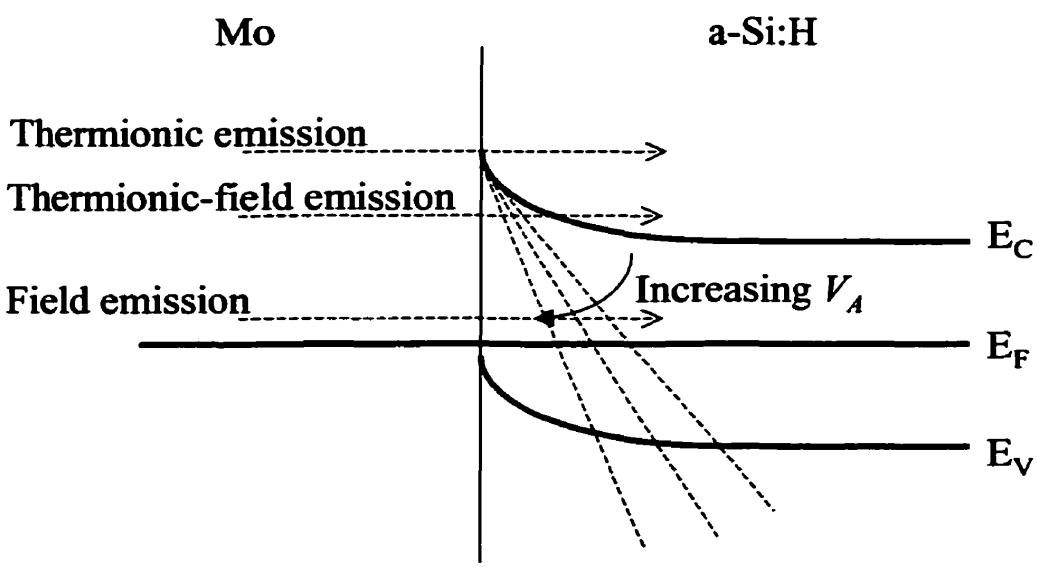


Figure 3.9: Transport mechanisms across Mo/a-Si:H Schottky barrier.

Φ_B is the Schottky barrier height. Electrons may also tunnel through the barrier by thermionic-field emission and field emission mechanisms. In large Schottky diodes with low periphery/area ratio, the dominant transport mechanism appears to be the thermionic emission with the current density, $J(V_A)$, due to the applied bias, V_A, expressed as [34];

$$J(V_A) = J_O[\exp(eV_A / kT) - 1]. \qquad \{3.14\}$$

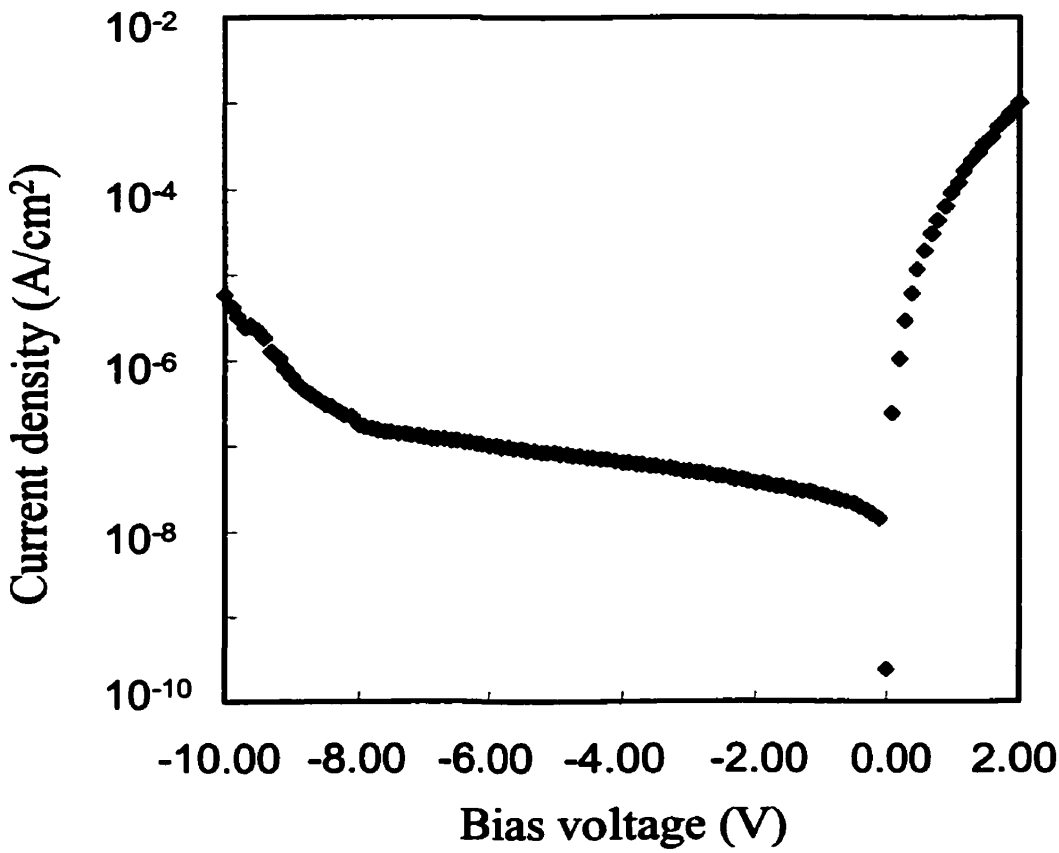


Figure 3.10: Leakage current density of a 700μm x 700μm Schottky diode under high reverse bias.

For Φ_B = 0.77eV [63]and T = 290K, Eq 3.2 saturates to a current density value of 2.89×10^{-7}A/cm^2 at a reverse bias voltage of V_A = -3V. This estimated value from the equation is compatible to what was observed in Fig. 3.6. Therefore, the dominant transport mechanism of large diodes appears to be thermionic emission. This appears to be true until a very large reverse bias is applied. Shown in Fig. 3.10 is the current density of a 700μm x 700μm Schottky diode with high reverse bias voltage. Only one device was tested for this experiment. The tunneling behavior of the leakage current is observed only with the reverse bias V_A > |8V|. This is not the case for small diodes in Figure 3.6. Even with relatively low reverse bias V_A ~ |1V|, the tunneling behavior was observed for devices whose dimensions are 50μm x 50μm and 26μm x 26μm (see Fig. 3.7). This is believed to be caused by the high defect state density on the unpassivated side walls of the diodes. As the periphery/area ratio increases, the number of defect sites increases. This increases the probability of tunneling, which leads to higher leakage

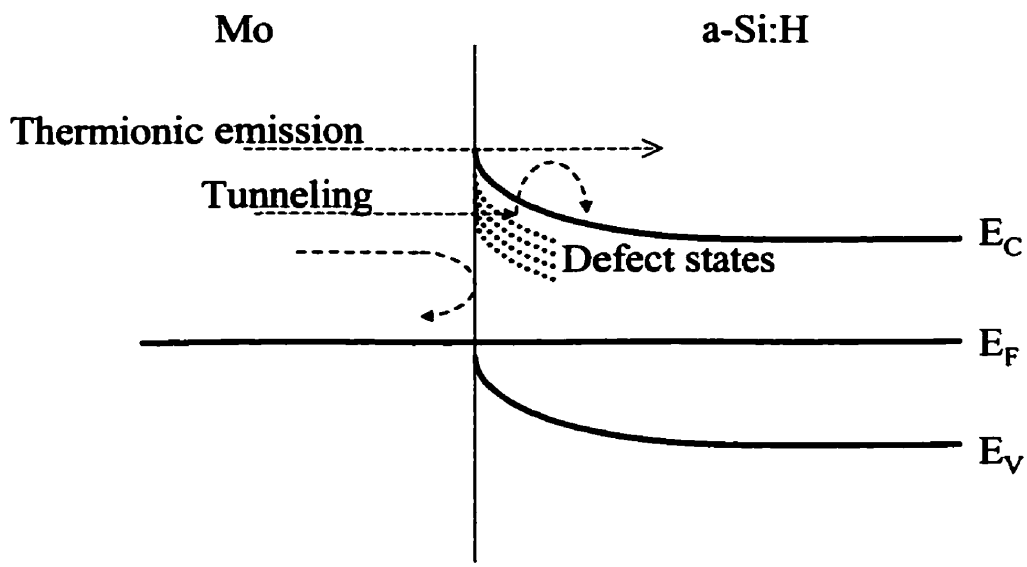


Figure 3.11: Effect of defect states in the band gap on the leakage current conduction in Schottky diodes.

current (see Fig. 3.11). This tunneling behavior appears to be the dominant transport mechanism in the small devices even at low reverse bias voltages.

The following conclusions can be made after these experiments. Firstly, the variation in the Schottky interface is very large. One order difference in the magnitude of the leakage current results in one detector being able to retain the collected charge ten times longer than another detector. In a large-area imaging array, in which many lines are read sequentially, this can be a problem. The reproducibility of the Schottky interface must be improved. Secondly, in an application which requires small imaging pixels, the side walls have to be passivated. With the current full wet-etch process, passivating the side walls are very easy. A new fabrication process for m-i-s structure is proposed in the Appendix A (Figs. A.1 and A.2). This process allows the side walls to be passivated with a silicon nitride layer. The only technical difficulty in this process is the development of the hydrogen plasma treatment on the silicon and nitride interface [64].

Chapter 4

X-Ray Pixel Integration

This chapter presents the engineering aspects of this project. Given the two devices, Mo/a-Si:H Schottky diode and TFT, the objective is to come up with designs to integrate the two different processes. There are requirements to be considered as well as problems associated with the fabrication steps. The approaches to these problems and suggested solutions will be presented.

4.1 Pixel Design Considerations

4.1.1 Pixel Size: Dimensions

There are number of design requirements to consider when designing an x-ray imaging pixel for large-area arrays. The geometrical dimensional requirements have been reported by Dr. J. Rowlands' group, our collaborator, at Sunnybrook Hospital in Toronto, Ontario [11, 27, 28]. Table 4.1 shows these requirements for different x-ray imaging modalities.

	Chest radiography	Mammography	Fluoroscopy
Array size (cm)	35 x 43	18 x 24	25 x 25
Pixel size (μm)	200 x 200	50 x 50	250 x 250
Number of pixels	1750 x 2150	3600 x 4800	1000 x 1000
Image readout time (sec)	< 5	< 5	0.033
X-ray spectrum (kVp)	120	30	70
Mean exposure to image array (mR)	0.3	12	0.001
Exposure range (mR)	0.003 - 3	0.6 - 240	0.0001 – 0.01

Table 4.1: Design requirements for large area x-ray imaging arrays for different imaging modalities, adopted from [11].

Among the three x-ray imaging modalities, chest lithography appears to have been the least stringent. As an initial attempt to fabricate a successfully working x-ray pixel, the size was chosen to be 200μm x 200μm.

4.1.2 Fill Factor

Another design requirement to consider in x-ray imaging is the high (sensor) fill factor which is defined as the active area expressed as a fraction of the physical detector area. In most of the conventional designs, the sensor can only occupy the area between data lines and the TFT. The maximum pixel size, which was discussed in the previous

section, varies with different x-ray imaging modalities (as it was shown in Table 4.1). For fluoroscopy and chest radiography, the maximum pixel size may be as large as 250μm x 250μm. But for mammography, the maximum pixel size should be around 50μm x 50μm [16]. Since the sizes of the TFT and data lines are fixed, as the maximum pixel size (detector + TFT + data line) decreases, the fill factor decreases. In attempt to overcome this problem, architectures employing a continuous sensor film were implemented [65]. Because the sensor layer is continuous, this implementation allowed for a 100% fill factor. However, due to the conducting doped layers in the p-i-n sensor, cross-talk between adjacent pixels was reported to be an issue.

4.2 Pixel Fabrication Processes

4.2.1 Stacked Pixels

In an attempt to achieve high fill factor, the Schottky diode was stacked on top of the TFT. Figure 4.1 shows a pixel structure in which the TFT is fully overlapped with the diode. In Fig. 4.2, the overlap is partial. Only the source region of the TFT is overlapped with the Schottky diode. These stacked pixel structures require eleven masks and thirteen lithographic steps. The first five masks are used for TFT fabrication as it was shown in Fig. 2.1. The design and the fabrication of this TFT, made in the inverted staggered structure, had been optimized for low leakage current ($\sim 10^{-14}$ A) [37]. The TFT process was immediately followed by the fabrication of the Mo/a-Si:H Schottky diode. Figure 4.3 describes the pixel fabrication process. Prior to deposition of the Schottky diode, the entire TFT area was passivated by 250nm thick a-SiN:H. Then, Schottky diode fabrication started with a thin n^+ a-Si:H layer (20nm) on top of the Mo

(a)

(b)

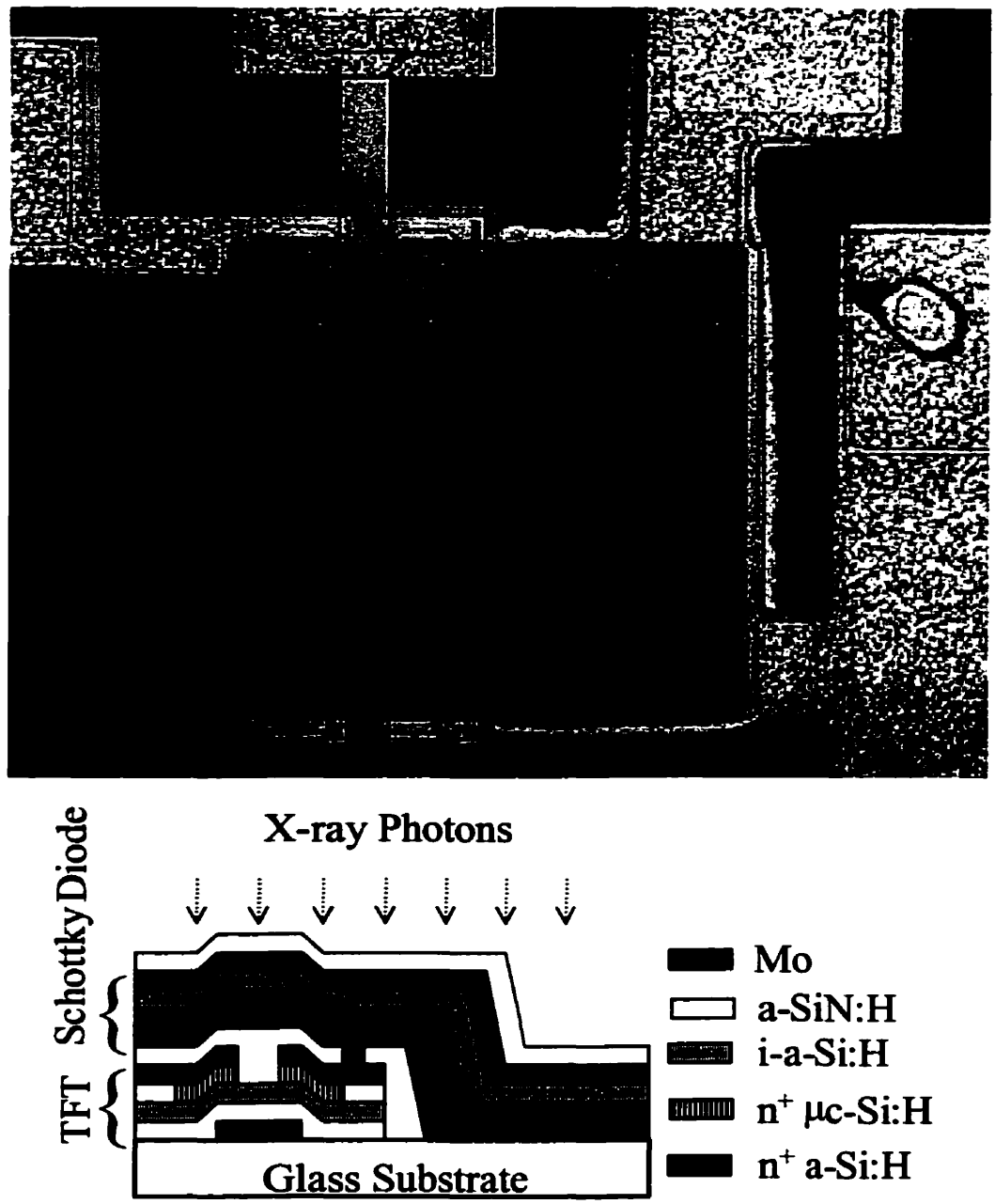
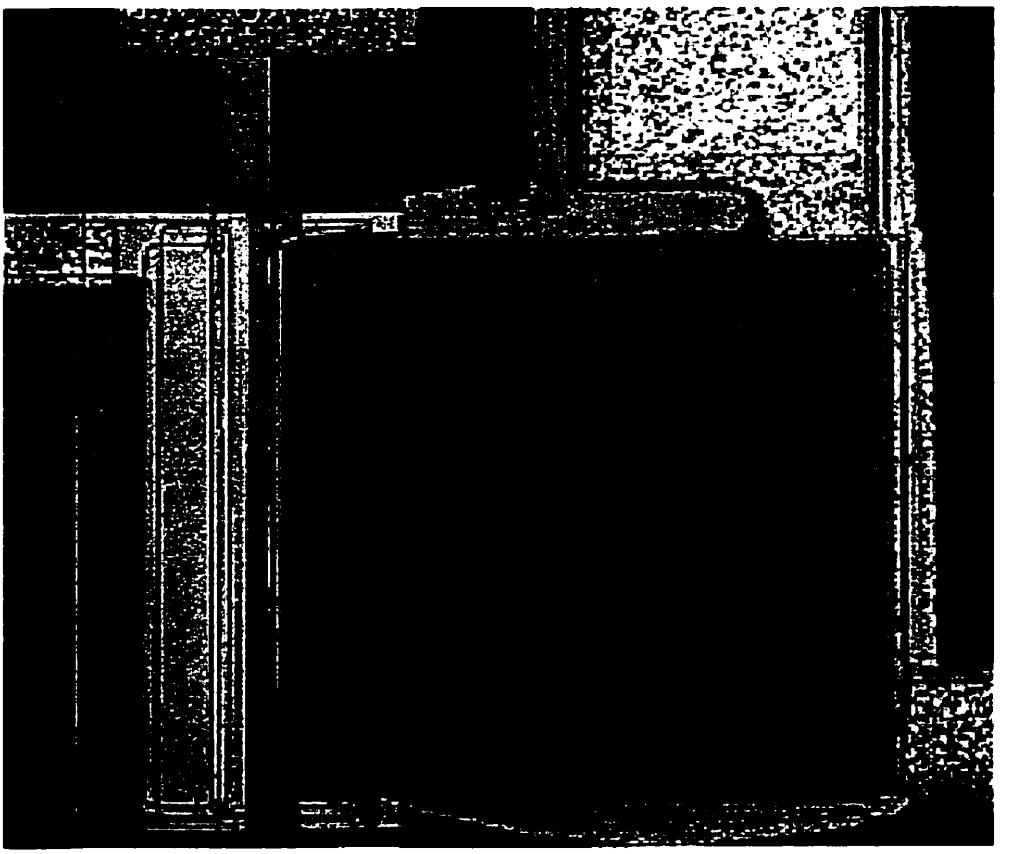


Figure 4.1: Fully overlapped x-ray pixel; a) top view, b) cross-sectional view.

(a)



(b)

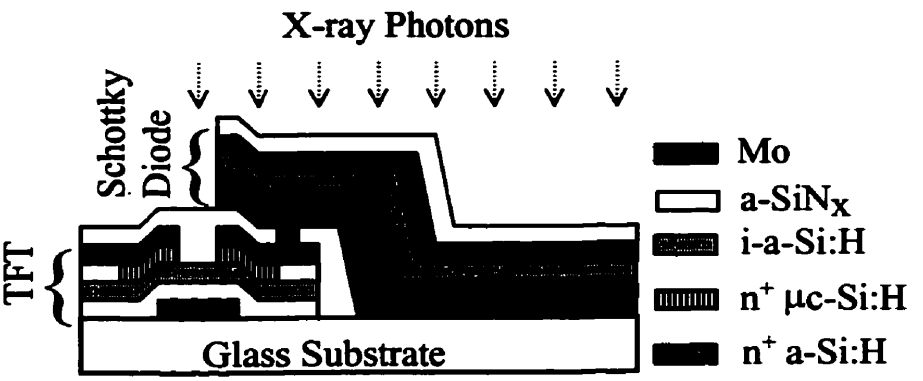


Figure 4.2: Partially overlapped x-ray pixel; a) top view, b) cross-sectional view.

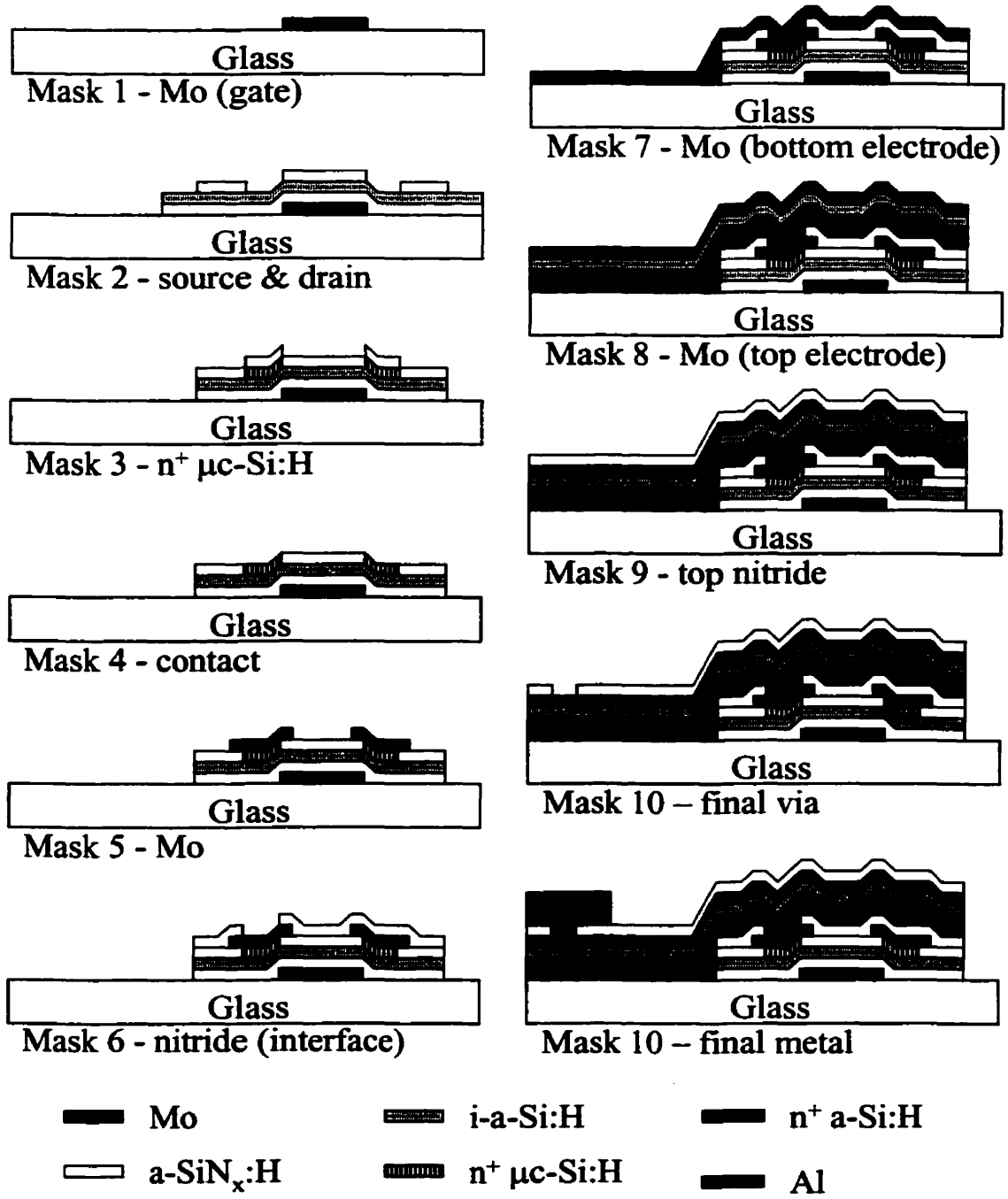


Figure 4.3: Process sequence of stacked x-ray pixel.

to give a good ohmic contact to the a-Si:H. The a-Si:H (1μm) and Mo metal (500nm) layers were then deposited in succession. In this process, a-SiN:H film was employed as the passivation layer on top of this Mo film to serve as etch-stops in the patterning of the a-Si:H layer. Mask 10 was used to open contacts on the nitride layer so that mask 11 could be used to pattern the final metal (Al). Tables C.1 and C.2 list the deposition conditions for each layer. The size of the Schottky diode in these structures was 200μm x 200μm, and the TFT channel is 200μm wide and 20μm long.

4.2.2 Non-Overlapping Pixels

Although the stacked pixel designs can provide high fill factor when designing for an array, due to the high intrinsic stress in the multiple-layered structure, the films peel off. This problem will be addressed again in section 4.3.3. To avoid the high mechanical stress associated with stacked layers, another pixel structure was studied, in which the two devices do not overlap (Fig. 4.4). In this non-overlapping structure, which is the standard pixel architecture reported in imaging arrays, the TFT occupied a small portion of the detector area to preserve the high fill factor. The channel of the TFT in the non-overlapping pixel structure was reduced to be 20μm wide and 10μm long. In this pixel fabrication process, the Schottky diode was deposited before the TFT. Since the devices were not stacked on top of each other, some of the fabrication processes could be carried out in parallel. Shown in Fig. 4.5 is the fabrication procedure of the non-overlapping x-ray pixel. The fabrication of the pixel started with chromium (Cr) patterned with mask 1 on a plain Corning 7059 glass wafer. Mask 1 defined not only the bottom electrode of the diode but also the gate of the TFT. Then, the Cr deposition was followed by the diode process. Highly doped amorphous silicon (n^+ a-Si:H) and intrinsic amorphous (i-a-Si:H) silicon were deposited in a single vacuum process to

(a)

(b)

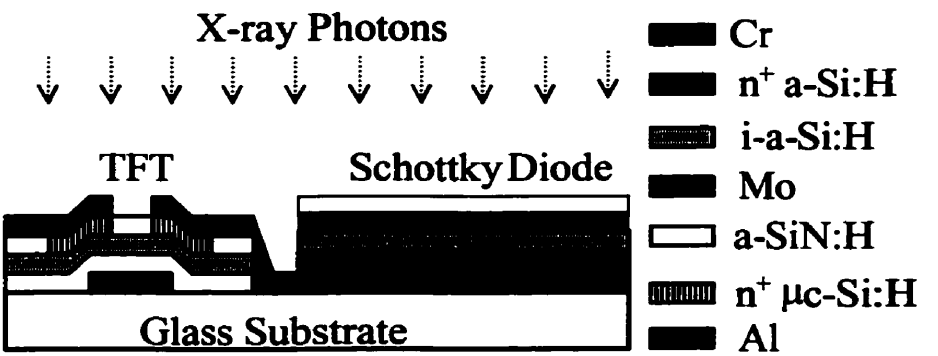


Figure 4.4: Non-overlapping x-ray pixel; a) top view, b) cross-sectional view.

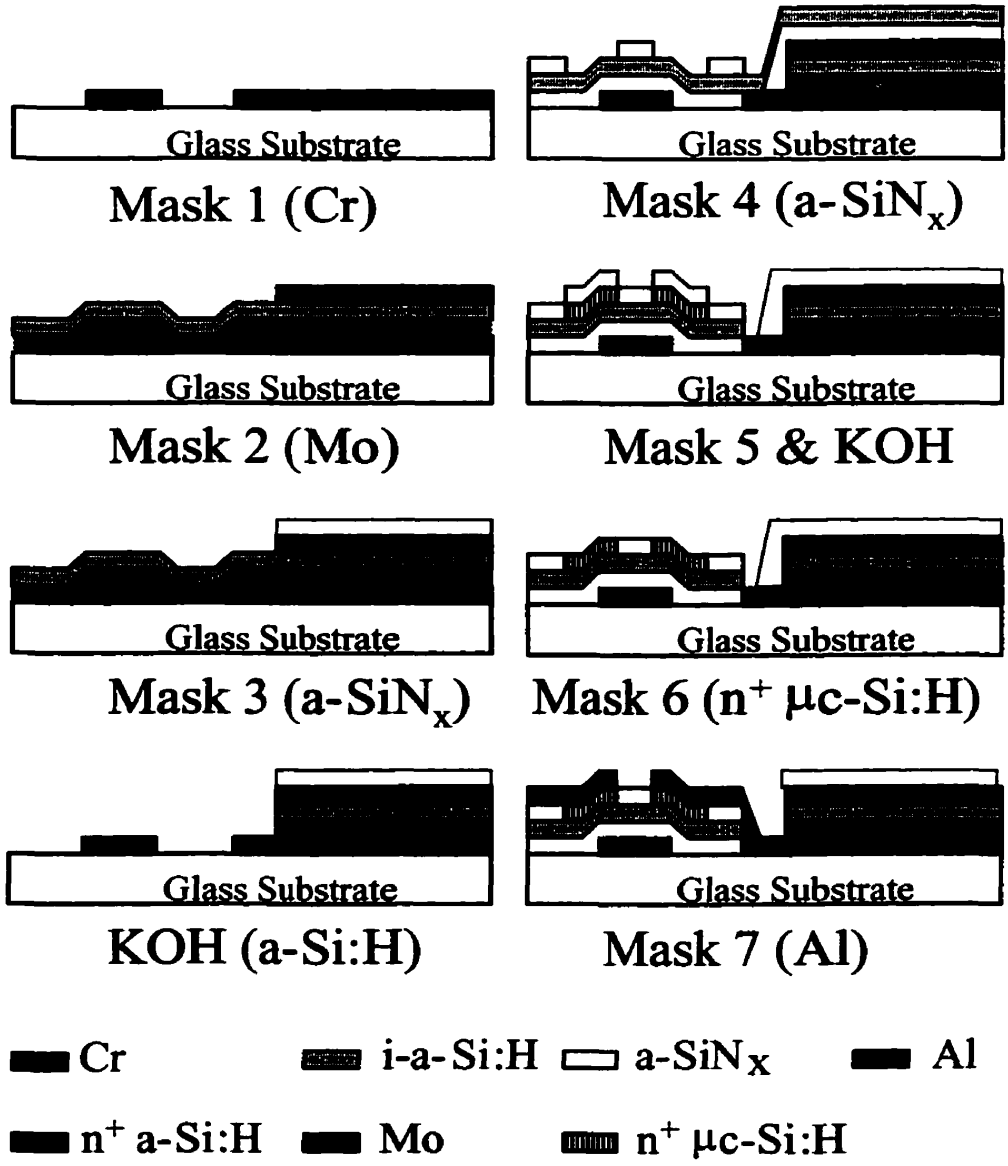


Figure 4.5: Process steps of non-overlapping x-ray pixel.

minimize the degradation of interface quality. The n^+ a-Si:H layer was deposited to provide an ohmic contact with the bottom electrode of the diode. Immediately following the i-a-Si:H deposition, a thick molybdenum layer was deposited and patterned with mask 2, which essentially defined the active area of the detector. Mask 3 patterned a N-rich amorphous silicon nitride (a-SiN_x:H) that served as the protection layer in KOH etching [31]. The KOH etching step removed both doped and undoped a-Si:H layers leaving Mo and a-Si:H layers underneath the nitride. The Schottky diode deposition was completed after this step and followed by the TFT deposition. The gate nitride, i-a-Si:H, and the top nitride were deposited in one continuous vacuum step. The top nitride was patterned with mask 4 to define the source and drain regions of the TFT. Then, low temperature (200°C) and low resistivity highly doped microcrystalline layer (n^+ μc-Si:H) was deposited in the source and drain regions to provide an ohmic contact with the final metal [66]. Mask 5 patterned the nitride layer that protects the n^+ μc-Si:H and i-a-Si:H layers, which were then removed by KOH etchant. Mask 6 opened the contact windows to the microcrystalline layer for the final metal. After mask 7 was used to pattern the final metal, the pixel deposition process was completed.

4.3 Process Considerations

4.3.1 Mask Count and Process Steps

There are a few significant differences between the stacked pixel process and conventional non-overlapping process. The most obvious difference is the mask count. In the non-overlapping pixel process, in which the two devices are deposited next to each other, the entire fabrication sequence takes only seven masks. In contrast, the stacked pixel process requires a total of eleven masks since the two devices have to be deposited one at a time. The extra four masks lead to longer fabrication time and higher

cost. Also, the stacked pixel process requires 13 lithography steps, whereas the conventional non-overlapping pixel process requires only 9 lithography steps.

4.3.2 Other Fabrication Issues

In the non-overlapping processes, the TFT is deposited after the Schottky diode is deposited. The contact layer of the TFT in this process can use the low temperature (200°C) n^+ μc-Si:H for best TFT performance. In the stacked pixel process, the TFT is deposited before the Schottky diode, thus it has to be taken to the 260°C deposition temperature of the subsequent PECVD films. In this case, the contact layer of the TFT is 260°C n^+ μc-Si:H film. Although Fig. 2.5 and Fig. 2.8 show only a small difference between the two films, in large area arrays where there are hundreds and thousands of pixels attached to one data line, a small improvement in leakage current may become significant.

Another fabrication issue to consider is the yield. The Schottky diode can have more margin of alignment error than the TFT. In TFT process, the alignment of the source/drain to the gate is very critical. Masks 2 and 3 have only 1-2μm margin of alignment error. In the non-overlapping process, the Schottky diode is patterned with strong KOH solution before the TFT is deposited (see Table D.1). The TFT is then patterned with a highly diluted KOH solution. However, in the partially overlapped pixel of the stacked process, the gate area of the TFT has to withstand the strong KOH solution whose purpose is to pattern the thick intrinsic a-Si:H film in the Schottky diode. If the TFT is misaligned, it will not survive the strong KOH solution. Thus, the yield of the partially overlapped process can be influenced by this lithography step.

In the non-overlapping pixel process, Cr can be used to replace Mo for lower resistivity. This cannot be done in the stacked pixel process. In the earlier work on the

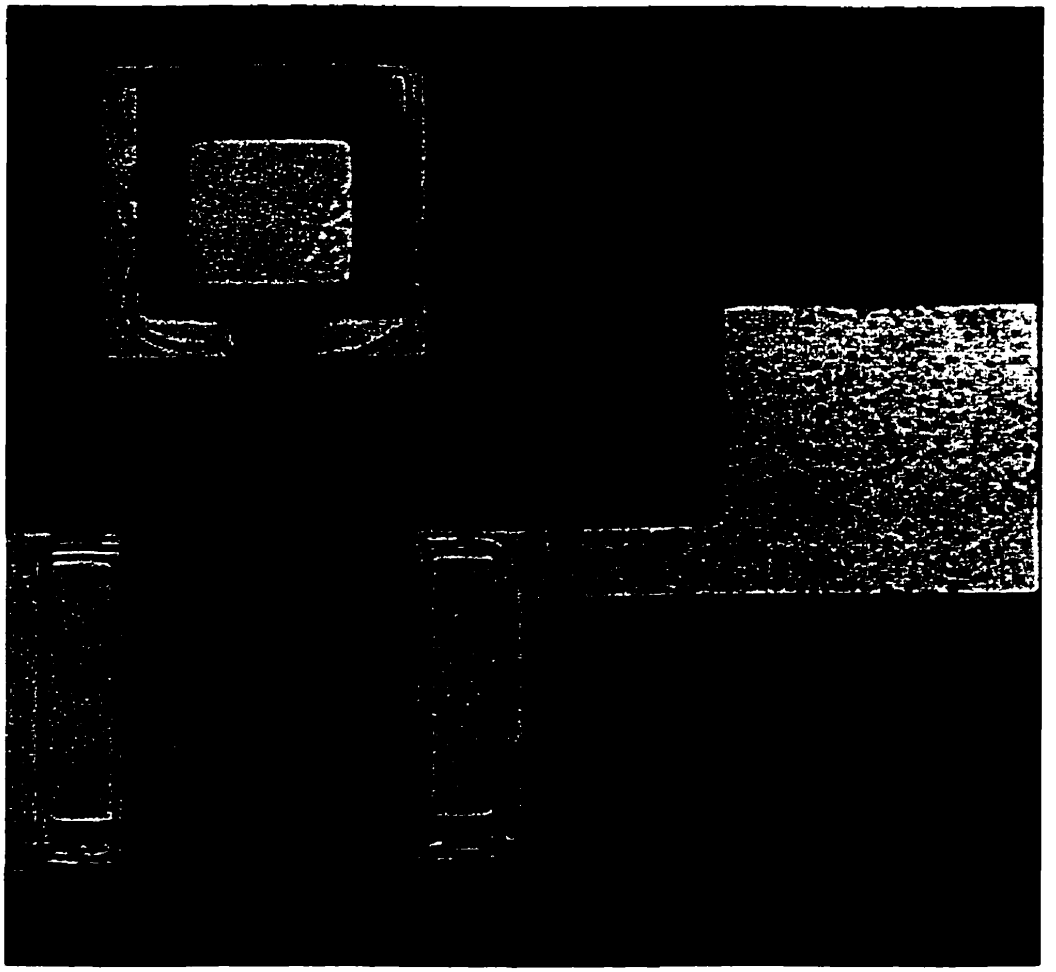


Figure 4.6: Top view of damaged thin layers, i-a-Si:H, n^+ μc-Si:H and a-SiN:H, due to Cr etching.

Schottky diode, Cr has been used as the bottom metal [31]. But in this fabrication process, it was observed that the Cr etchant, mixture of ceric ammonium nitrate and acetic acid (see Table D.1), attacks the a-SiN:H and a-Si:H-layers (Fig.4.6) [67]. Thus, Cr had to be replaced with Mo as the contact metal for both the Schottky and the TFT.

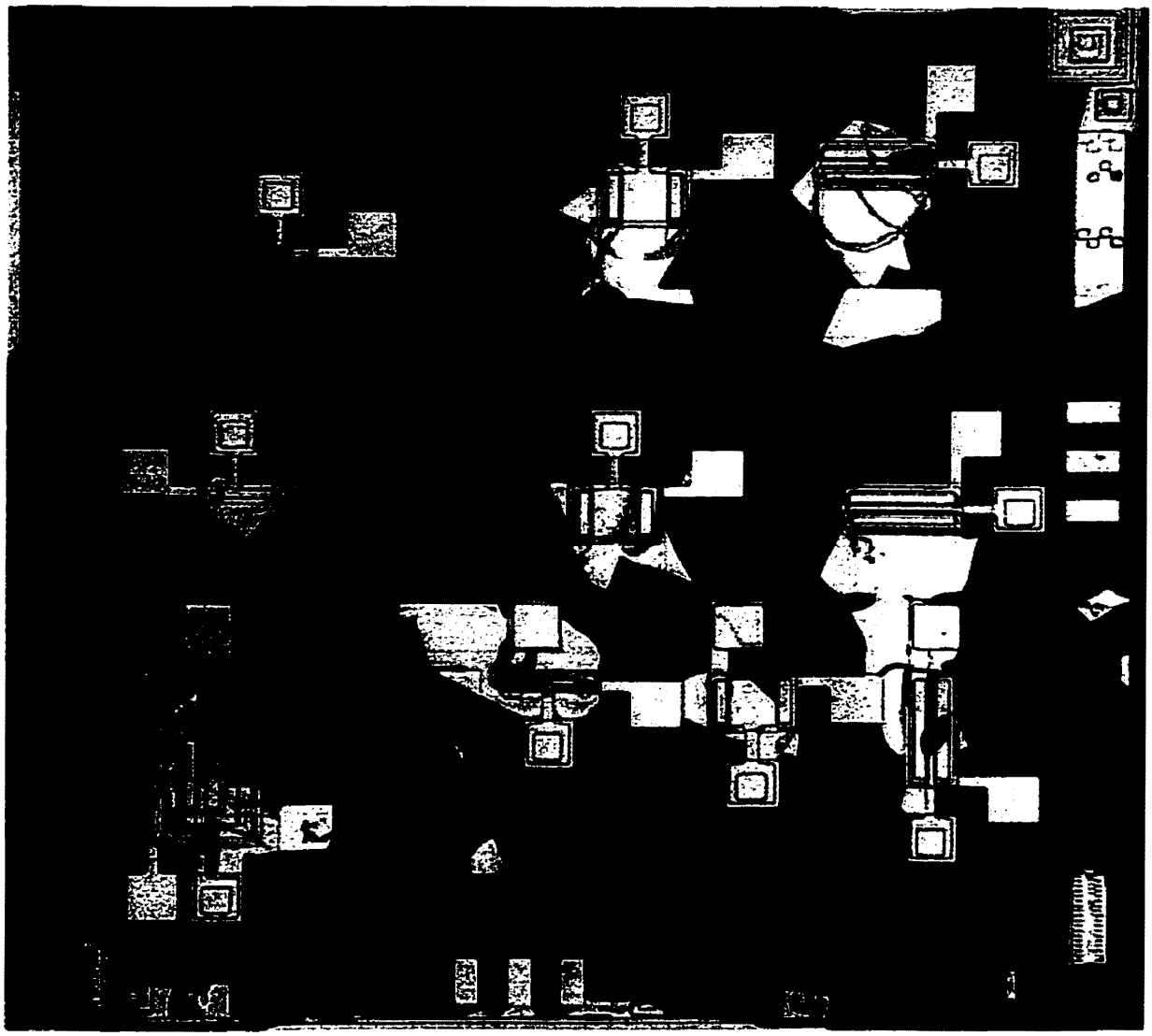


Figure 4.7: Top view of damaged thin film layers due to stresses associated with Mo, a-SiN:H and i-a-Si:H layers.

4.3.3 Intrinsic Film Stress

Although the stacked pixel structures can potentially provide high fill factor, they give rise to high mechanical stress in the films due to the multi-layer structure. It was observed that the interfaces of these layers could not withstand the shear stress between films, causing the films to peel off. Previously, it was reported that the optimal thickness of the Mo layer in the Schottky diode is 500 nm [31]. However, when a 500nm thick Mo layer was deposited on the stacked pixel structure, the layers underneath (i-a-Si:H and a-SiN:H) could not withstand the shear stress, which resulted in the films peeling off (Fig 4.7). Subsequently, film stress had to be reduced to preserve the mechanical integrity of the pixels without undermining the film quality. This work is presented in chapter 5.

4.4 Performance Considerations

4.4.1 Leakage Current

One of the key pixel performance issues is the leakage current of the TFT. The TFT leakage current has to be small in order to preserve the charges generated by x-rays during the OFF state. In the partially overlapped pixel, the TFT leakage current was as small as that of a discrete TFT (~10^{-13}A) (Fig 4.8). However, the leakage current in the fully overlapped configuration was too severe to be employed as a pixel for large area imaging arrays. For each different pixel configuration, at least five devices were sampled. The scatter in the measurement was less than 5%. The high leakage current may be caused by the parasitic back channel, formed at the a-Si:H/a-SiN:H interface [68]. In the fully overlapped pixel structure, the electric field generated by the gate metal was pinned by the 0V of the bottom metal of the Schottky diode (Fig 4.9). Then,

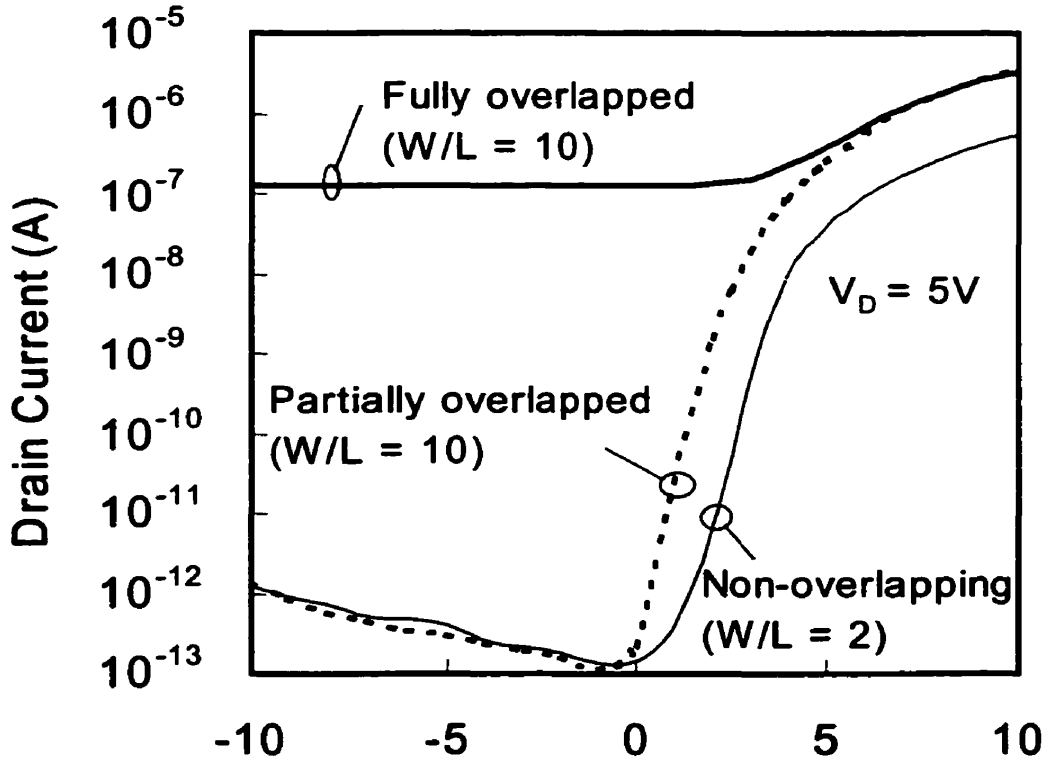


Figure 4.8: Leakage currents of TFTs in the different pixel structures.

when the TFT was reverse biased, the electrons in the a-Si:H layer experienced an electric field, forming a steady parasitic back channel at the a-Si:H/a-SiN:H interface, hence providing a high conducting path from drain to source.

The leakage current of the non-overlapping TFT was approximately the same (~10^{-13}A) as that of the TFT in the partially overlapped structure despite the smaller W/L ratio. This observation was analogous to previous studies of TFT leakage currents with varying W/L ratios [67]. Fig. 4.10 displays the ON-currents of the small TFT with various V_G's. Since the TFT was small (W/L=2), the current was small, and so was the transconductance.

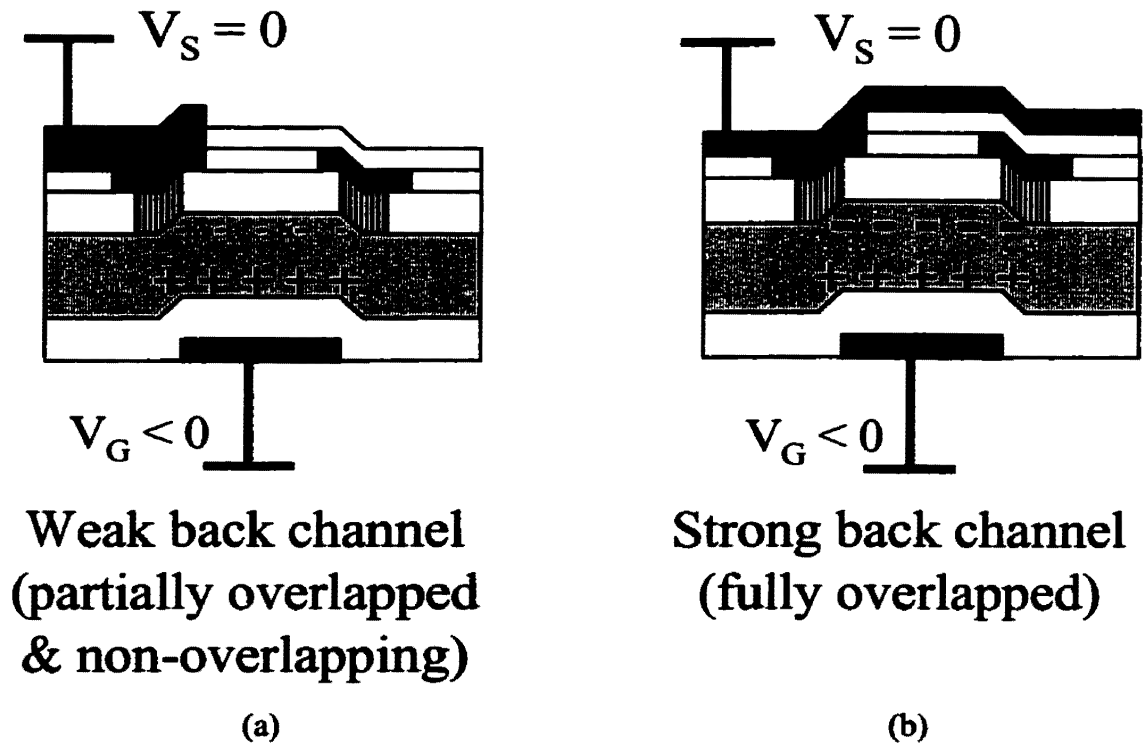


Figure 4.9: Formation of parasitic back channel a) in the partially overlapped pixel and non-overlapping pixel, and b) in fully overlapped pixel with a metal ($V_S = 0V$) covering the gate area.

4.4.2 X-Ray Response

The partially overlapped pixel and the non-overlapping x-ray pixel were exposed to x-rays for 50ms at various x-ray source voltages in the range of 30-120 kVp, generated by a Mercury Modular x-ray machine with a molybdenum target at 16 degrees. The test

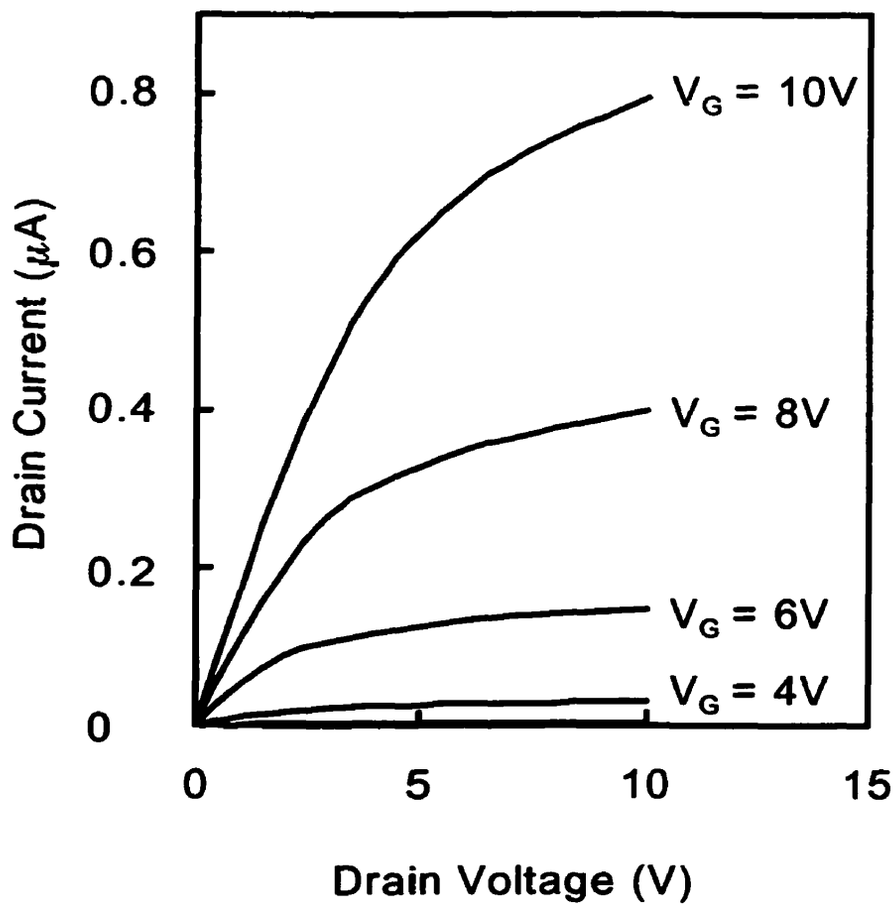


Figure 4.10: Switching behavior of the non-overlapping TFT (W=20μm/L=10μm).

instrument setting for the x-ray sensitivity measurement is shown in Fig. 4.11. The x-ray radiation was measured with an RTI Solidose 300 Digital Dosimeter whose dose range was from 0.5μR to 23,000R. The corresponding x-ray dose for this source voltage range

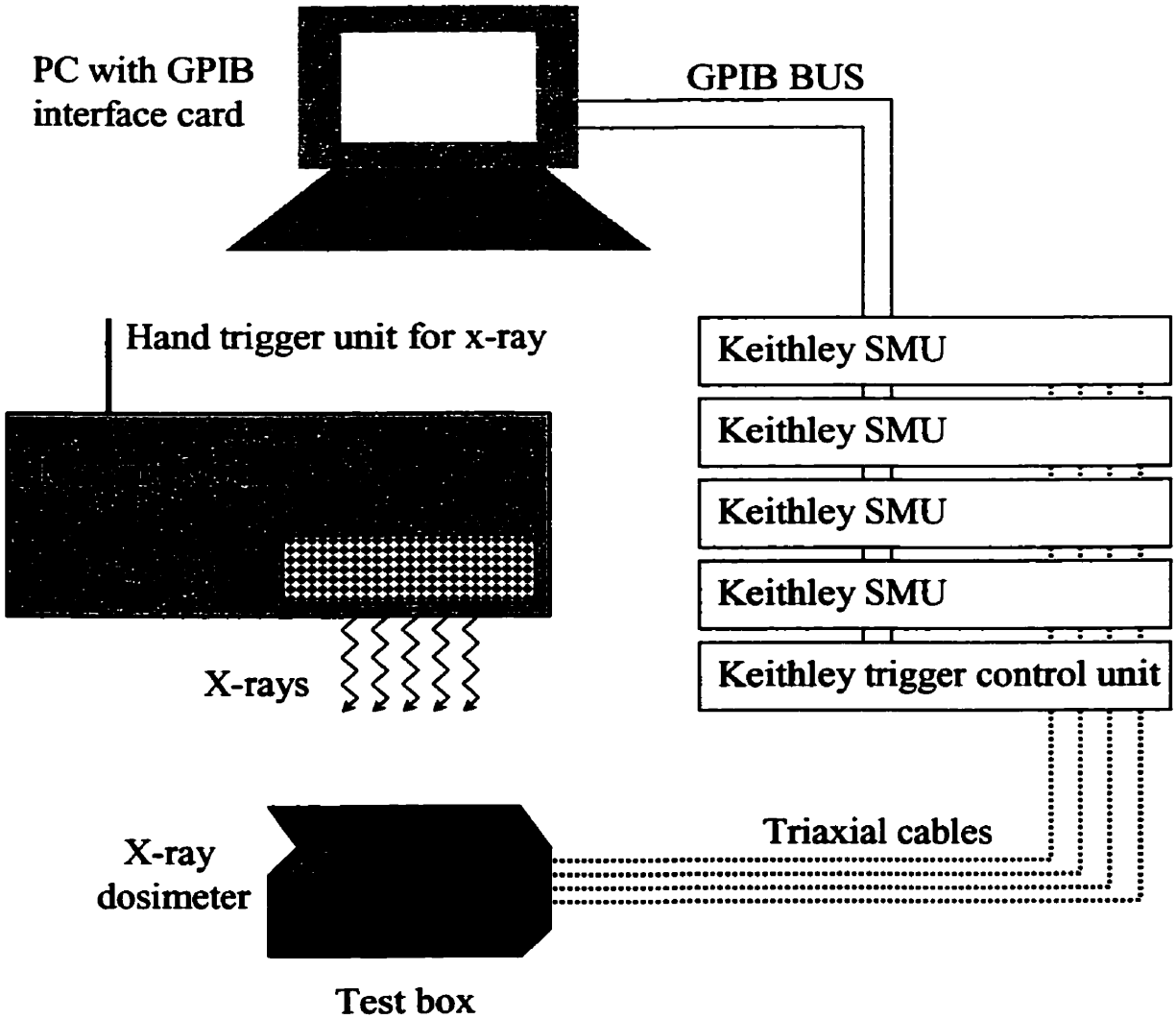


Figure 4.11: X-ray sensitivity measurement setup.

is plotted in Fig. 4.12. The biasing of the pixel and the measurement of current were carried out with Keithley 236 Source-Measure Units, remotely controlled by a computer via HPIB. The Schottky diode was reverse biased with a low voltage. The pixel

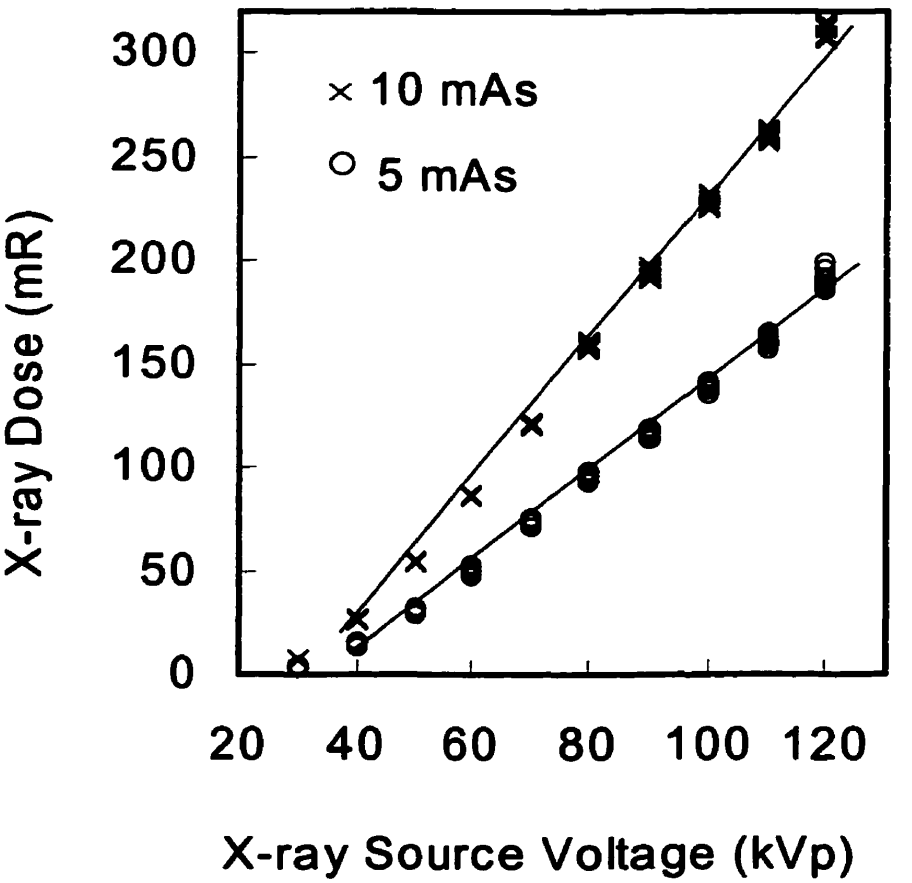


Figure 4.12: X-ray dose vs. source voltage.

operation was described in section 1.4.3. While the gate of the TFT was pulsed at 1Hz to reset the voltage at the source of TFT, the current generated by x-rays was detected through the drain by the Keithley Source-Measure Unit for a sampling period of 16.67 ms. The timing diagram is shown in Fig. 4.13. There is an unknown length of delay

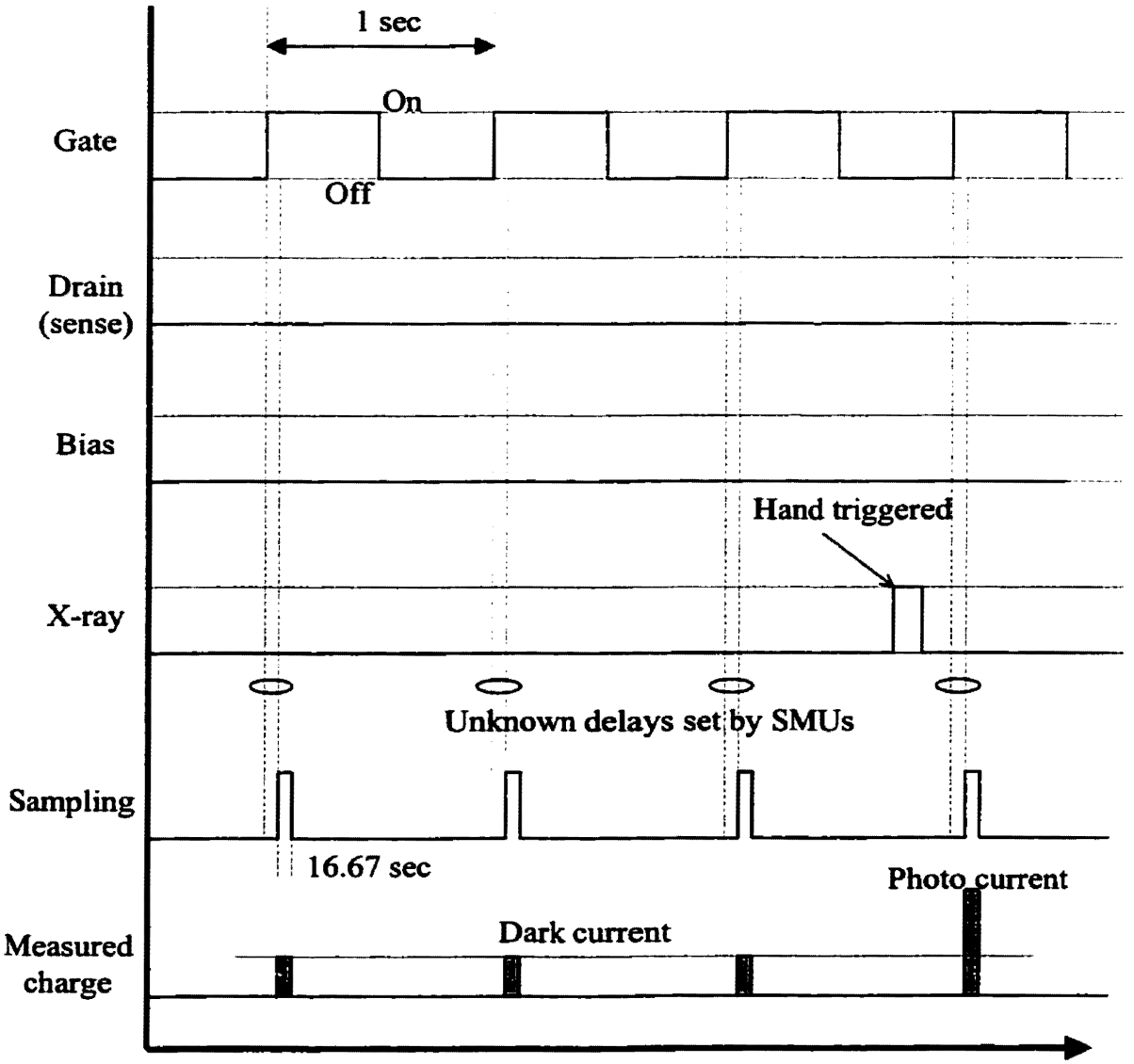


Figure 4.13: Timing diagram of x-ray sensitivity measurement.

between the controlling computer and the SMUs. When SMU #1 turns the gate signal on and sends the confirmation to the PC, the PC sends a signal to SMU #2 to start

sampling the current at the drain of the TFT. This is communicated via the GPIB bus which has a speed that is considerably slow. Even in the SMU #2, there is an internal delay between when it received the signal "start sampling" and when it actually starts to sample. For this reason, the gate has to be kept at a low on voltage to slow down the data transfer to the data line. The number of measured electrons ranged from

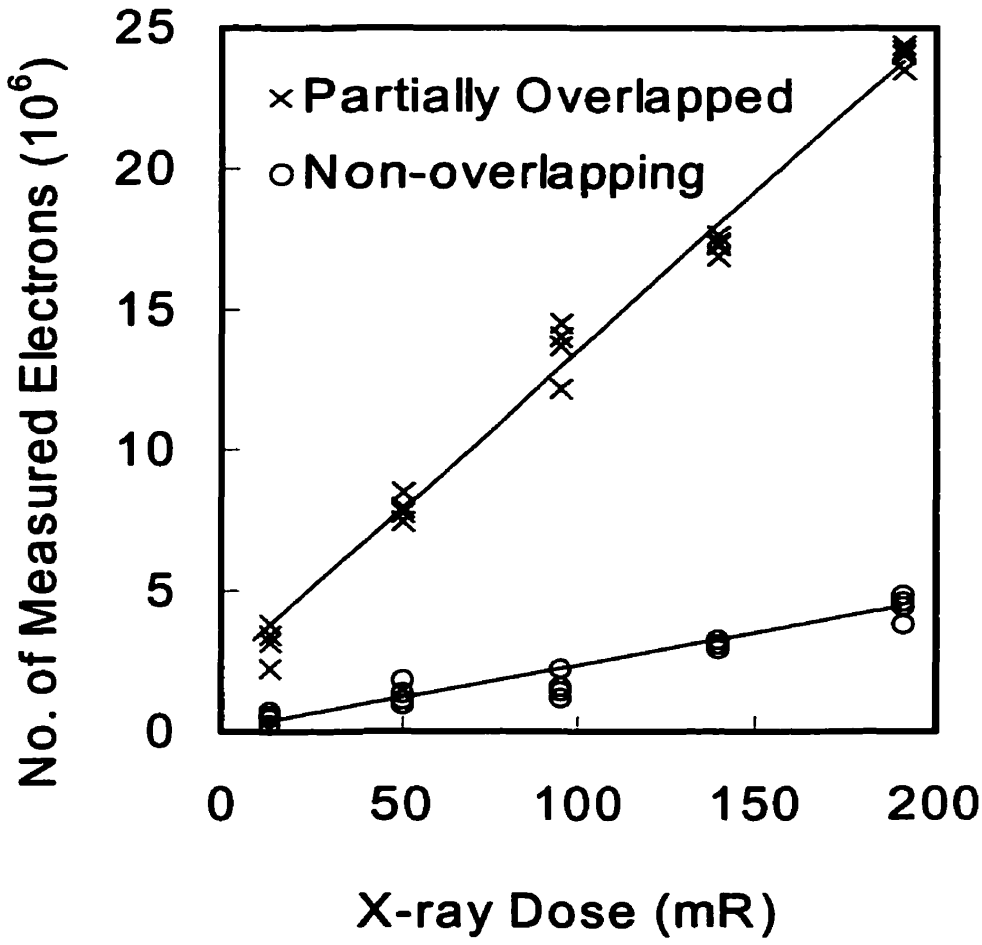


Figure 4.14: Number of measured electrons vs. x-ray dose.

3 to 20 million for the partially overlapped pixel (Fig. 4.14). However, in the non-overlapping pixel structure, because the TFT was small, the charges generated by x-rays could not be as easily transferred to the dataline as in the partially overlapped structure with a large TFT under the same bias conditions. This resulted in reduced charge transfer rate and, thus, a reduced number of total measured electrons. As shown in Fig. 4.14, with the same bias conditions as the partially overlapped pixel, the ratio of the measured electron was approximately 1/5, which is also the ratio of the sizes of the two different transistors.

In conclusion, there were trade-offs in choosing different pixel structures and, thus, an engineering decision had to be made. Fully overlapped and partially overlapped pixel structures provided high fill factor, but suffered from the stresses due to the multi-layered configuration. In addition, the TFT leakage current of a fully overlapped pixel was too high ($\sim 10^{-7}$ A) to be used in a large area imaging array. It also had a high parasitic capacitance between the bottom electrode of the diode and the drain of the TFT. The partially overlapped structure also suffered from high stress, but, the leakage current was comparable to that of a discrete TFT.

The stress was not as severe in the non-overlapping structures. Also, the leakage current was small. However, due to the small width of the TFT, the charges generated by x-rays could not be transferred as fast as in the stacked structures under the same bias conditions.

The choice of pixel design had to be compromised between performance and process complexity. Partially overlapped pixels require a high mask count, but produce more detected electrons. The non-lapping pixel did not produce as many electrons as the partially overlapped pixel under the same bias conditions. However, it was less expensive to fabricate and did not have as high a stress level.

Chapter 5

Thin Film Stress

As mentioned in section 4.3.3, when thin films are stacked on top of each other, the mechanical film stress may lead to catastrophic damage to the entire structure. This chapter is dedicated to minimizing this effect by studying and reducing the film stress. It covers from the basic fundamentals to the experimental data as well as analyses.

5.1 Motivation for Studying Mechanical Film Stress

Whether or not film stress causes problems in the application at hand depends on the circumstances and on the level of the stress. A small level of compressive stress can actually strengthen brittle films, reducing the chances of the film being put under sufficient tensile stress to cause fracturing. Corrosion resistance is also improved by avoiding tensile stress in metal films by keeping the corrosion activation energy high. It is also observed that the stress of a small magnitude improves the properties of epitaxial structures in electronic applications. However, high stresses usually lead to problems. The stress limit is the point of catastrophic failure, which is illustrated in the cross section in Figs 5.1 and 5.2. Tensile stress failure is characterized by cracking, which

appears as a mosaic pattern when viewed from the top. The cracked film may then peel off the substrate (Fig. 5.1). On the other hand, compressive stress failure is characterized by de-adherence and buckling, which from the top appears to be domes or bubbles (Fig 5.2). The studies of stresses in thin films of a-Si:H devices were conducted to analyze the causes of film stress and to characterize the stress in films, so that high stress can be avoided in multi-layer structure devices as seen in Fig. 4.1.

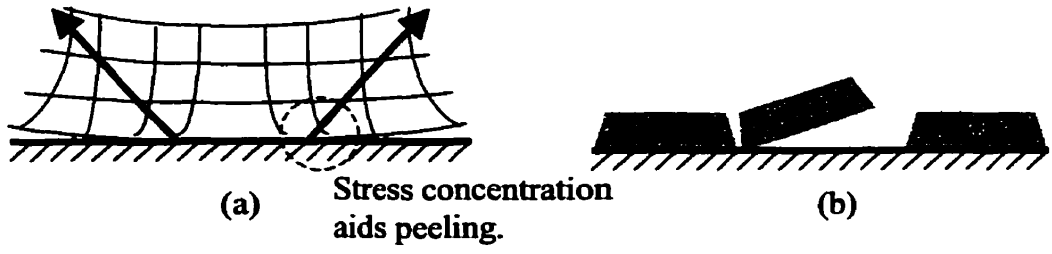


Figure 5.1: a) Qualitative cross-sectional portrait of a thin film with tensile stress. b) Catastrophic peeling-off failure from tensile film stress.

Figure 5.2: a) Qualitative cross-sectional portrait of a thin film with tensile stress. b) Catastrophic buckling failure from tensile film stress.

5.2 Breakdown of Film Stress

Interest in the mechanical stresses in thin films started as early as 1877 [69]. During the intervening years, many stress determinations had been made in thin films produced by various means, and theories had been offered to explain the results obtained. Reviews of this work have already been given with regard to stress in continuous films, and also, more specifically, to the stresses that are present in the initial stages of growth when the film consists of completely separate islands [70, 71, 72, 73].

Nearly all films, by whatever means they are produced, are found to be in a state of internal stress. The stress may be compressive or tensile, with extreme cases illustrated in Figs. 5.1 and 5.2. In general, for normal deposition temperatures (50 °C to a few hundred °C), the stress in metal films is typically 10^7 to 10^9 Pa and tensile. The refractory metals (e.g. Mo) have higher stress, whereas soft (ductile) metals (e.g. Cu, Ag, Au, and Al) have lower stress. Dielectric films can have either compressive or tensile stress depending on the stochiometry [74]. N-rich silicon nitride films are in tensile state, but the increase in the hydrogen content can change it to compressive state [75].

5.2.1 Total Stress, σ_{total}

The total stress in a thin film, σ, can be expressed as;

$$\sigma = Y\varepsilon_{external} + Y\varepsilon_{thermal} + Y\varepsilon_{intrinsic} \qquad \{5.1\}$$

where, Y: Young's modulus of the substrate,

$\varepsilon_{external}$: external strain (strain exerted from an external source),

$\varepsilon_{thermal}$: thermal strain (strain due to the mismatch in the thermal expansion coefficients), and

$\varepsilon_{intrinsic}$: intrinsic strain (strain that is internal in the film).

The total stress must be kept below the interface tolerance. In most cases, the intrinsic stress is the predominant component in Eq. 5.1. However, in this section, all three components of the total stress will be discussed.

5.2.2 External Stress, $\sigma_{external}$

In most thin film applications, external stress does not exist. However, if the devices are deposited on substrates that are flexible (e.g. polymer substrate or metal foil substrate), then external strain can be applied to the devices [76]. In the next sections, the mathematical analysis of the external stress will be carried out by starting with the basic fundamentals (i.e. Hooke's Law) of strain and stress.

Hooke's Law & Modulus of Elasticity, Y

The basic physical behavior of solids is described by the stress-strain curve (Fig. 5.3). The force applied per unit of cross-sectional area is the stress, σ, tensile being positive and compressive negative. Tensile stress along one direction, for example, x, causes the material to stretch along that direction by a fractional amount called the strain, ε_x;

$$\varepsilon_x = \Delta x / x. \qquad \{5.2\}$$

For brittle materials such as silicon and silicon nitride, this relationship is linear up to the yield point. And the material is said to be elastic. The yield point is usually defined to be where the deviation from linearity reaches 0.2%. The slope in the elastic region is a measure of material stiffness and is called the elastic modulus or Young's modulus, Y. Thus,

$$\sigma_x = Y\varepsilon_x \qquad \text{or} \qquad \varepsilon_x = \frac{\sigma_x}{Y}. \qquad \{5.3\}$$

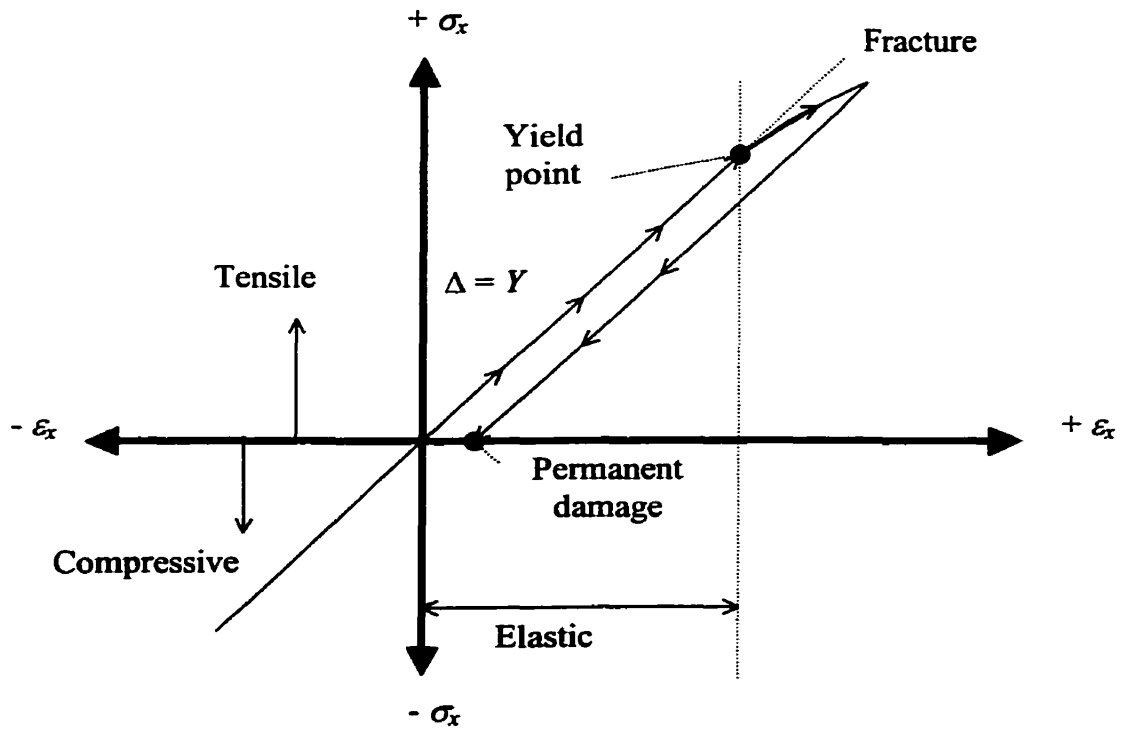


Figure 5.3: Characteristics of the stress-strain relationship.

This is Hooke's law in one dimension (and it is similar to the equation of a spring);

$$F = kx. \qquad \{5.4\}$$

where, k is the spring constant. The material in this analysis is assumed to be homogeneous and isotropic, i.e. Y_x, Y_y, and Y_z are the same.

Poisson's Ratio, ν

Uniaxial tensile stress along x direction in a freestanding sample of material causes stretching along the x direction, also shrinking along the unconstrained y and z

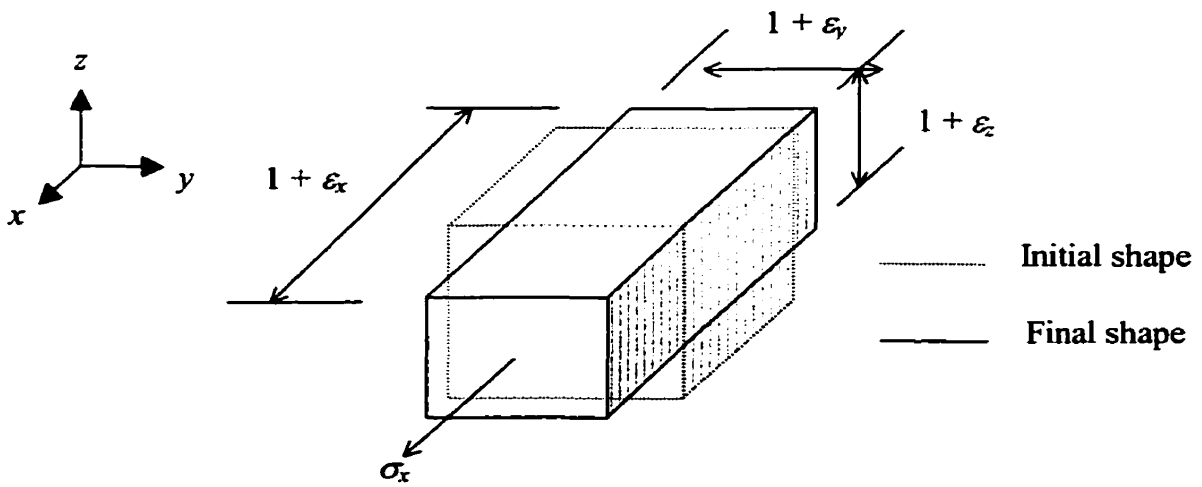


Figure 5.4: Strain resulting from uniaxial stress applied to a cube.

directions, as shown in Fig. 5.4. This means that ε_y and ε_z are negative. These three strains are related by Poisson's ratio, ν;

$$\nu = -\varepsilon_y / \varepsilon_x = -\varepsilon_z / \varepsilon_x . \qquad \{5.5\}$$

If there is no volume increase upon stressing, $\varepsilon_x + \varepsilon_y + \varepsilon_z = 0$, and thus, $\nu = ½$.

Biaxial Modulus of Elasticity, *Y'*

Thin films are mainly under biaxial stress because they are being pulled on by the substrate in two dimensions (Fig. 5.5). This changes the stress-strain relationship from that of Eq. 5.2. That is, σ_x causes stretching along x, which is σ_x/Y, but at the same time, σ_y causes a shrinkage along x direction, which is $-\nu\ \sigma_y/Y$. Thus, the net strain is the sum of the two, as illustrated by the following equations:

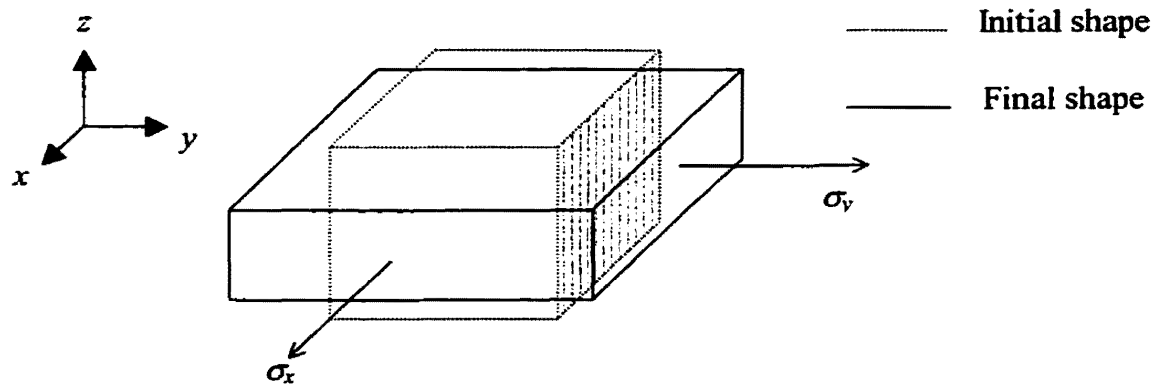


Figure 5.5: Strain resulting from biaxial stress applied to a cube.

$$\varepsilon_x = \frac{\sigma_x}{Y} - \nu\frac{\sigma_y}{Y} \text{ and} \qquad \{5.6\}$$

$$\varepsilon_y = \frac{\sigma_y}{Y} - \nu\frac{\sigma_x}{Y} \qquad \{5.7\}$$

Assuming that $\sigma_x = \sigma_y = \sigma_{x,y}$ where, $\sigma_{x,y}$ is the biaxial stress,

$$\varepsilon_x = \frac{(1-\nu)}{Y}\sigma_{x,y} = \varepsilon_y = \varepsilon_{x,y}. \qquad \{5.8\}$$

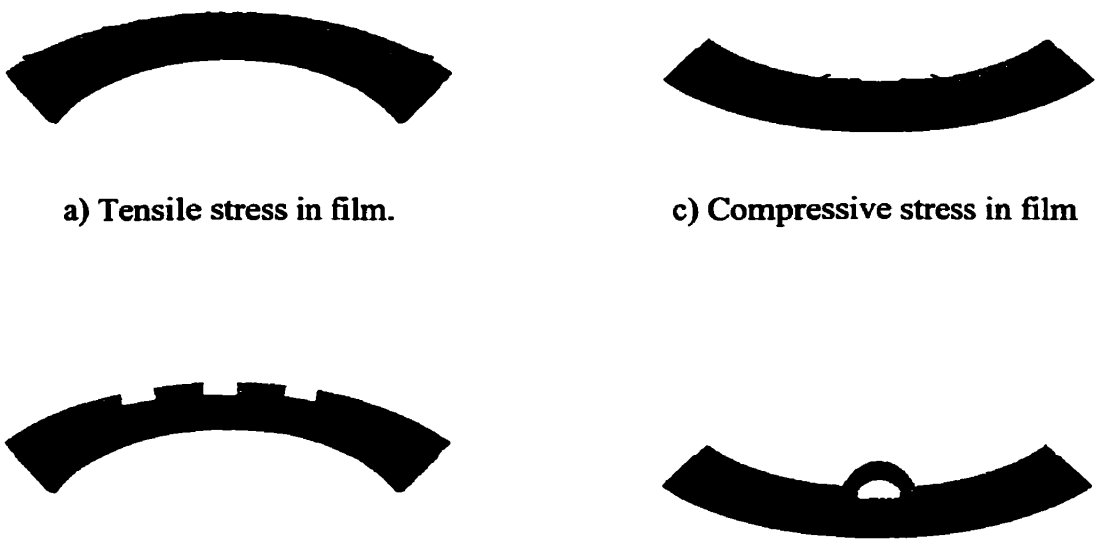
Here, $\varepsilon_{x,y}$ is the biaxial strain. From Eq. 5.7;

$$\varepsilon_x = \varepsilon_y = \varepsilon_{x,y} = \frac{(1-\nu)}{Y}\sigma_{x,y} = \frac{\sigma_{x,y}}{Y'} \qquad \{5.9\}$$

where, Y' is the biaxial modulus of elasticity.

External Stress Due To Folding

When thin film devices are deposited on foldable substrates, they can be bent, as shown in Fig. 5.6. When flat panel display technology can be implemented on polymer substrates, the display screen may be conveniently folded for compact portability. When the thin film is bent concavely, it experiences tensile stress (Fig. 5.6a). If this tension is higher than the interface tolerance, which depends on the type interfacial layer and adhesion as discussed in the previous sections, the film cracks or peels off (Fig. 5.6b). On the other hand, if the film is bent convexly, a compressive stress is experienced on the film (Fig. 5.6c). If the compression is higher than the interface tolerance, the film loses adhesion and buckles up (Fig. 5.6d).



a) Tensile stress in film.

c) Compressive stress in film

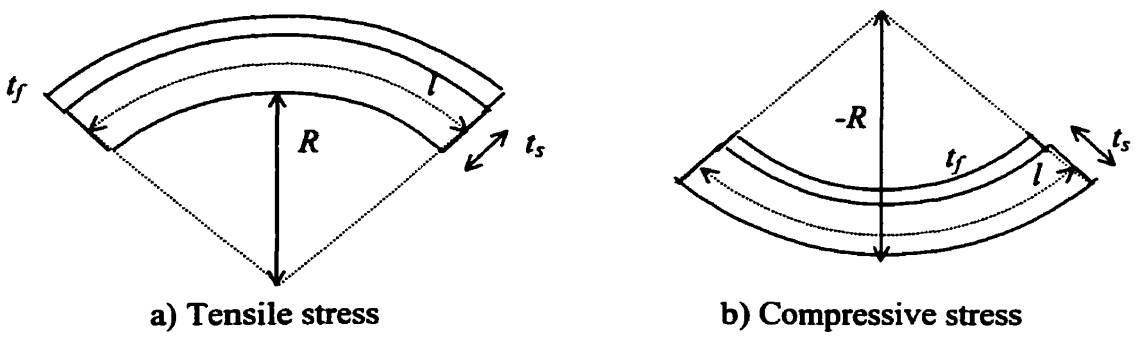
b) Film cracks due to high tension.

d) Film buckles due to high compression.

Figure 5.6: Stresses in thin film when an external force is applied.

In an attempt to quantify the external stress, the following analysis was conducted. Figure 5.7 is drawn to help describe the analysis. The assumptions made in this analysis are listed below:

1. The thickness of the substrate, t_s, is small compared to the length of the substrate, l. ($t_s << l$);
2. The thickness of the film, t_f, is much smaller than the thickness of the substrate, t_s. ($t_f << t_s$);
3. The film is isotropic, i.e. it has the same modulus of elasticity in all directions. ($Y_x = Y_y = Y_z = Y$).



a) Tensile stress b) Compressive stress

Figure 5.7: Simplified portraits of substrate bending effects.

When the substrate is bent as in Fig. 5.7, the radius of curvature, R, can easily be measured by an optical apparatus. Then, the length of the film after bending is:

$$l+\Delta l = 2\pi\left(R+t_s+t_f\right)\times\frac{(l-\Delta l)}{2\pi R} \quad \text{or,} \quad l+\Delta l = 2\pi\left(-R+t_s+t_f\right)\times\frac{(l+\Delta l)}{2\pi(-R)}. \quad \{5.10\}$$

Since $t_f << t_s$, Eq. 5.10 can be simplified to

$$l+\Delta l = \left(R+t_s\right)\times\frac{(l-\Delta l)}{R} \quad \text{or,} \quad l+\Delta l = \left(-R+t_s\right)\times\frac{(l+\Delta l)}{(-R)}. \quad \{5.11\}$$

Also, since $t_s << l$, Eq. 5.11 can be further simplified to

$$l+\Delta l = \left(R+t_s\right)\times\frac{l}{R} \quad \text{or,} \quad l+\Delta l = \left(-R+t_s\right)\times\frac{l}{(-R)}. \quad \{5.12\}$$

Then, the change in the film length, Δl, due to the stress is

$$\Delta l = \frac{l}{R}\left(R+t_s\right)-l \quad \text{or,} \quad \Delta l = \frac{l}{(-R)}\left(-R+t_s\right)-l. \quad \{5.13\}$$

Eq. 5.13 can be rewritten as

$$\Delta l = l\left(\frac{R+t_s}{R}-1\right) \quad \text{or,} \quad \Delta l = l\left(\frac{R-t_s}{R}-1\right), \quad \{5.14\}$$

and

$$\Delta l = l\left(\frac{R+t_s}{R}-\frac{R}{R}\right) = l\left(\frac{t_s}{R}\right) \quad \text{or,} \quad \Delta l = l\left(\frac{R-t_s}{R}-\frac{R}{R}\right) = l\left(\frac{-t_s}{R}\right). \quad \{5.15\}$$

Then, the strain due to the stress is

$$\varepsilon = \frac{\Delta l}{l} = \left(\frac{t_s}{R}\right) \quad \text{or,} \quad \varepsilon = \frac{\Delta l}{l} = \left(\frac{-t_s}{R}\right). \quad \{5.16\}$$

Applying Eq. 5.3, the stress due to bending is

$$\sigma_{\text{external}} = Y\varepsilon = Y\left(\frac{t_s}{R}\right) \qquad \text{or,} \qquad \sigma_{\text{external}} = Y\varepsilon = -Y\left(\frac{t_s}{R}\right) \qquad \{5.17\}$$

Eq. 5.16 shows that the strain in the thin film due to the external stress is directly proportional to the thickness of the substrate. This seems to be in agreement with the observations made by others [76]. From Eq. 5.17 one can observe that the strain is inversely proportional to the radius of curvature. This is rather obvious since the radius, R, is small when the substrate is severely bent.

5.2.3 Thermal Stress, $\sigma_{thermal}$

The thermal stress is created by a mismatch of the thermal expansion coefficients of the film and the substrate when the film is deposited at its deposition temperature, T_d, and cooled down to the temperature of measurement. The change in temperature is denoted by ΔT. Then, the thermal stress can be expressed by

$$\sigma_{\text{thermal}} = Y \cdot (\alpha_f + \alpha_s) \cdot \Delta T \qquad \{5.18\}$$

where, α_f and α_s are the thermal expansion coefficients for film and substrate, respectively. Y is the uniaxial Young's modulus for the film. But, as mentioned in the last section, thermal stress is biaxial. Therefore, Eq. 5.18 should be

$$\sigma_{\text{thermal}} = \frac{Y}{(1-\nu)} \cdot (\alpha_f + \alpha_s) \cdot \Delta T = Y'(\alpha_f + \alpha_s) \cdot \Delta T \qquad \{5.19\}$$

The calculated thermal stress of thin films used in this work for TFT and Schottky diode fabrication is listed in Table B.1 in Appendix B. The modulus of elasticity and Poisson's ratios can be found in [34, 74, 75, 77, 78, 79, 80, 81, 82, 83, 84]. The calculated values in this table are only 2-10 % of the measured stresses in thin films. This implies that, with $\sigma_{external} = 0$, i.e. when the substrate is not bent, the biggest contribution to the total stress in thin films is the intrinsic stress.

5.2.4 Intrinsic Stress, $\sigma_{intrinsic}$

The last, yet the largest (and the most difficult to understand) contribution to the total stress is the intrinsic stress, which reflects film structure, in many ways not well understood at present; there are no equations like Eq 5.17 and Eq. 5.19 that describe the internal stress. Since the intrinsic stress appears to mirror the film structure, film interface and level of adhesion, it is expected to be related to thickness, condensation rate, deposition temperature, ambient pressure, and type of the substrate. The wide variety of inconsistent experiment data on intrinsic stress published in numerous papers is certainly due to the difficulty of obtaining the same deposition parameters [72, 85]. However, these reported values of intrinsic stress can be used in qualitative comparisons with the intrinsic stress of the films measured in the lab. Again, the values in these tables should be considered representative rather than precise. In some cases, Poison's ratio is neglected and in others only total stress is listed for lack of more detailed information. Despite the diversity of results in the literature, it is possible make some general observations:

1. There is no linear relationship between the thickness of thin films and their intrinsic stress.
2. Most metal films have tensile stress with a magnitude of 10^8 - 10^9 Pa.

3. Intrinsic stress varies with different substrates.

5.3 Stress Measurement Setup

There are largely two ways to measure the deformation of the substrate due to the stress. One method is to use a thin cantilevered beam as a substrate and calculating the radius of curvature of the beam and hence the stress, from the deflection of the free end. The other is to observe the displacement of the centre of a circular disk. Stress may also be measured by x-ray or electron diffraction techniques. The position of the diffracted line gives the interplanar spacing of the set of lattice planes corresponding to the line, and the strain in the crystallites forming the film may be deduced from this. Alternatively, the stress may be deduced from the shape of the diffracted beam by apportioning the line broadening to components resulting from small particle size and from strain.

It should be noted that x-ray and electron diffraction techniques will give the strain and, hence, the stress in a crystallite lattice. This is not necessarily the same as that measured by substrate bending since the stress at the grain boundaries may not be the same as that in the crystallites. For amorphous and poly- or microcrystalline films, the disk bow measurement technique gives a better understanding of how the film stress is spread all over the wafer.

5.3.1 Wafer Bow Measurements

The intrinsic stress in thin films is measured with the Ionic Systems Stressgauge (Fig. 5.8). This instrument optically measures the stress-induced bow (deflection) in the substrate (Fig. 5.9). The sensitivity of the instrument is 0.03μm and the measurement range is from 10^6 to 10^{13} Pa. The deflection readings are taken before and after the film

Figure 5.8: Ionic Systems Stressgauge.

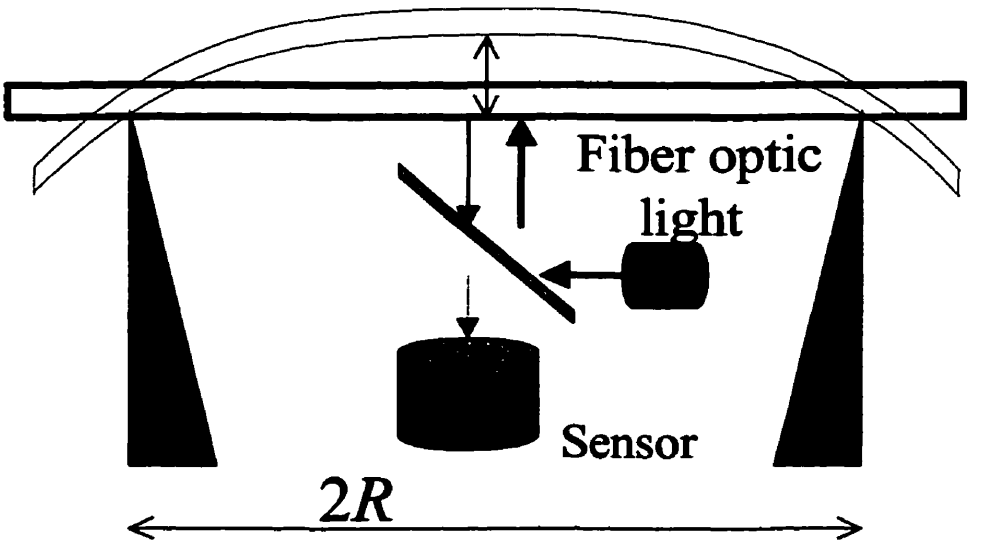


Figure 5.9: Apparatus for observing the bow deflection caused by stress.

deposition. Since the film thickness is much smaller than that of the substrate (glass wafer), the stress (σ) induced by the deposited thin film can be approximated as [86]

$$\sigma = \frac{d}{R^2} \frac{E_s}{3(1-\nu)} \frac{T_s^2}{T_f} \qquad \{5.20\}$$

where, d: displacement due to the bow,
R: knife edge radius of the instrument,
E_s: Young's modulus for the substrate,
ν: Poisson's ratio for the substrate,
T_s: substrate thickness, and
T_f: film thickness.

The scatter in data is less than 2%. The glass substrate used in this study is Corning 7059 with Young's modulus of 67.8 GPa, Poisson's ratio of 0.28 and thickness of 508μm ± 5μm. All measurements were conducted assuming that:

1. the wafers are linearly elastic;
2. the wafers are homogeneous ($\nu = \nu_x = \nu_y = \nu_z$);
3. the wafers are isotropic ($Y = Y_x = Y_y = Y_z$);
4. the thickness of the wafer is uniform;
5. the deposited film is thin compared to the wafer thickness; and
6. the deflection is small compared to the wafer thickness.

5.3.2 Shadow Masks

The Ionic Systems Stressgauge uses fiber optic sensor to measure the light intensity coming back from the unpolished back side of the silicon wafer. The films being studied in this work are deposited on glass substrates. Since glass wafers are transparent, when placed on the stressgauge, they do not produce any readings. In an attempt to overcome this problem, shadow masks had to be prepared such that a metal film could be deposited only at the center on the back side of a glass wafer to reflect the fiber optic light (Fig. 5.10). These shadow masks were placed just below the wafers in the wafer holder of the PVD system (Fig 5.11). Then, the choice of metal to reflect the light along with its thickness had to be carefully chosen.

Figure 5.10: Shadow masks for depositing Mo film only at the center of the glass wafers.

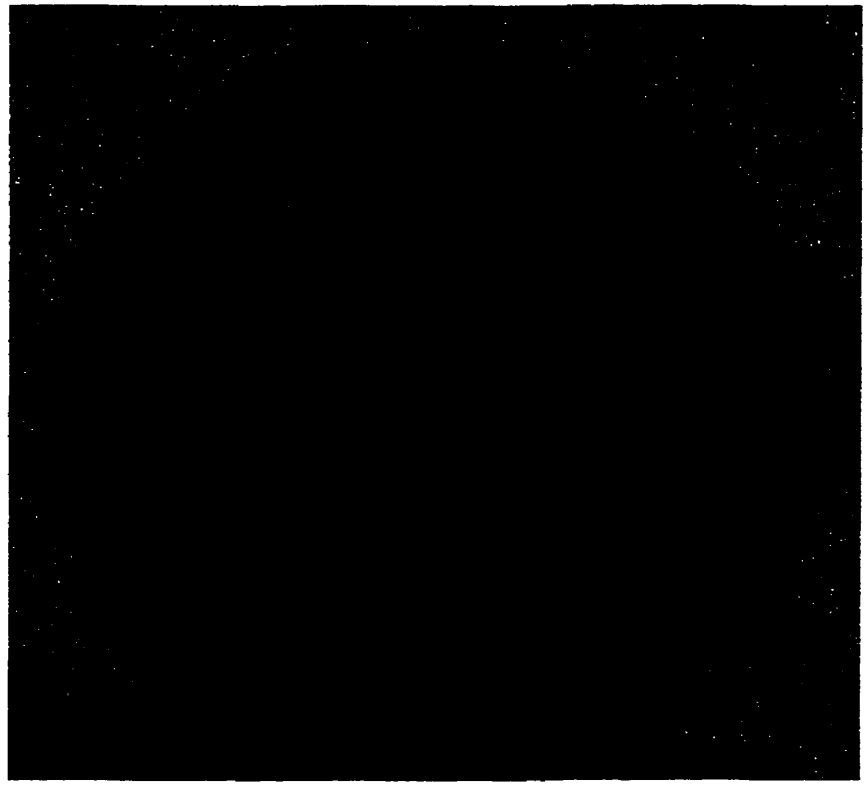


Figure 5.11: Wafer (3") holder of Edwards sputtering system (PVD).

At first, thin Al film was deposited. Al film, being a reflective metal, reflected too much light. The fiber optic sensor was fully saturated regardless of the light intensity adjustment. Then, a refractory metal, Mo, was deposited. This Mo film must be thick enough to stop light from passing through, but thin enough so that it did not change the shape of the wafer with its stress. With repeated experiments, a Mo film thickness of 350nm was determined to be a good compromise. The readings for the stress measurements were taken from glass wafers with this Mo film at the center on the back side before and after the film under study was deposited on the front side.

5.4 Stress Measurement Results

5.4.1 Intrinsic Film Stress on Glass Substrate

The intrinsic stresses of thin films deposited on glass substrates are listed in Table 5.1. These results were produced by depositing the same film on four different wafers in the same run, taking at least seven measurements (with the maximum and minimum values ignored), and averaging all readings. The scatter in data was within 5%. The stress of the Mo film, which was studied in depth to minimize its intrinsic stress, will be presented in section 5.4.3.

All silicon-based films are in compressive stress. The a-SiN:H film can be in either compressive or tensile stress. The nitrogen-rich silicon nitride film for high device stability [87] was found to be a tensile stress.

	Thickness (nm)	Stress (GPa)	State
i-a-Si:H	1000	0.116	compressive
n^+ a-Si:H	750	0.305	compressive
n^+ μc-Si:H	200	1.47	compressive
a-SiN:H	250	0.222	tensile
Al	1000	0.049	compressive
Cr	500	0.575	tensile

Table 5.1: Measured intrinsic stress of thin films deposited on Corning 7059 glass substrate.

5.4.2 Intrinsic Film Stress in Thin Film Transistors

In the fabrication of TFT, a-SiN:H (gate dielectric, 250nm), i-a-Si:H (active layer, 50nm) and a-SiN:H (top dielectric, 250nm) layers are deposited in one continuous vacuum process cycle to preserve the interface quality. When deposited on glass substrates, the magnitude of the tensile stress in nitrogen-rich a-SiN:H is 0.222 GPa. This value is comparable in magnitude to that observed earlier by other authors [74, 75]. When the same silicon nitride film is deposited on i-a-Si:H as the top dielectric, it is measured to be in a tensile stress with 56.9 MPa in magnitude. After the tri-layer deposition needed for the TFT, the compressive stress of very thin i-a-Si:H, sandwiched by the tensile gate and top dielectric layers, diminishes, and the total stress of all three layers is measured to be a tensile stress of 62.0 MPa in magnitude.

5.4.3 Intrinsic Film Stress in Mo/a-Si:H Schottky diodes

Unfortunately, the canceling out of film stresses is not achieved when fabricating Schottky diodes. The Mo layer (500nm), deposited on a thick (1μm) i-a-Si:H layer to form the Schottky barrier, can be either in compressive or tensile stress depending on the deposition pressure and the RF power. Shown in Figure 5.12 is the measured intrinsic stress of a 500nm thick Mo layer deposited on i-a-Si:H. From this graph, one can observe that the Mo layer, deposited at 200W, has stresses that are smaller in magnitude (either compressive or tensile) compared to that deposited at 400W. However, Figure 5.13 shows that the film density of a Mo layer deposited at 200W is quite low compared to films deposited at higher RF power. For retrieval of film density, the film mass is measured with a Micro Gram-Atic Balance whose measurement limit is 5μg. The effect of high RF power and low deposition pressure will be discussed in more detail later in this section. Since the x-ray detection principle of the Schottky diode is

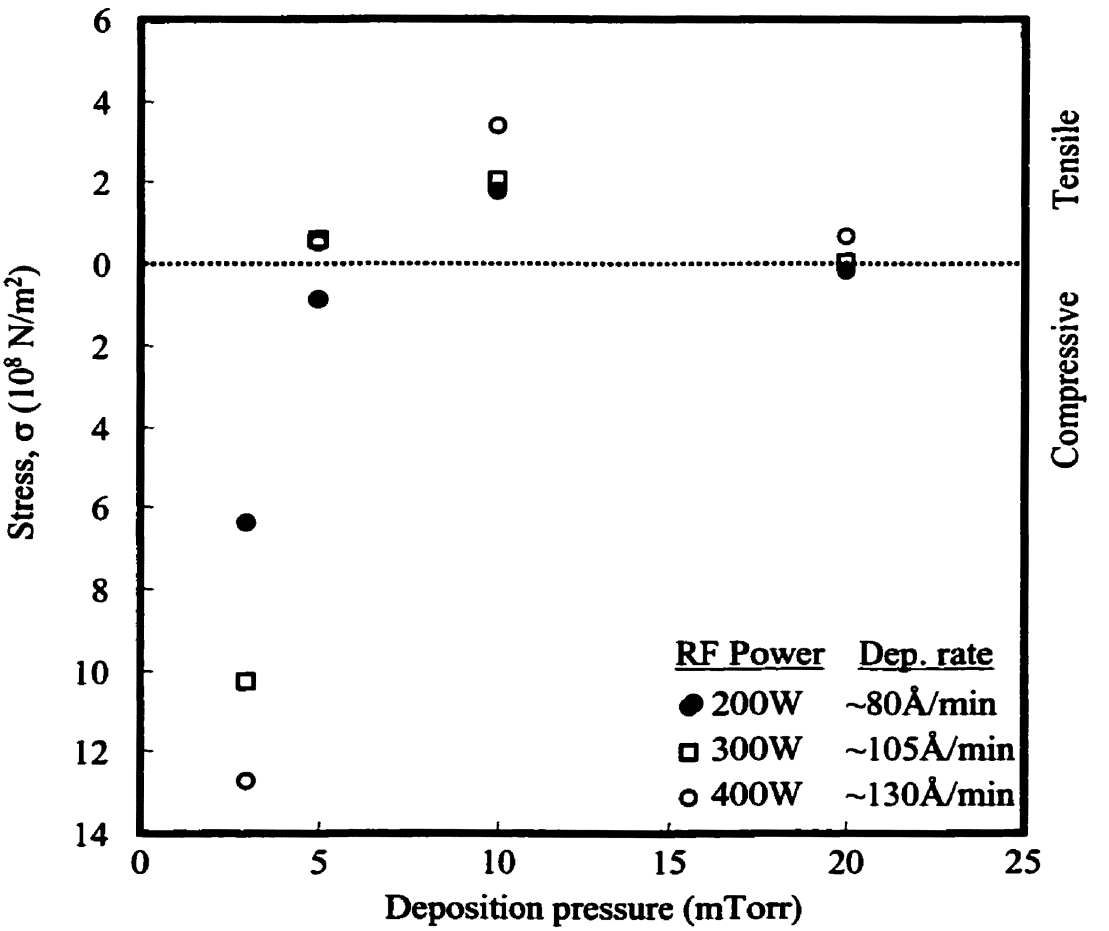


Figure 5.12: Measured stress, σ, of 500nm Mo film deposited at 25°C on i-a-Si:H.

based on the photoelectric interaction of the x-ray photons with Mo atoms, a lower density leads to a lower x-ray absorption efficiency. Therefore, it is necessary that the Mo layer for the Schottky interface is deposited at high RF power and low process pressure. However, Mo films deposited at 3mTorr peel off the i-a-Si:H due to high

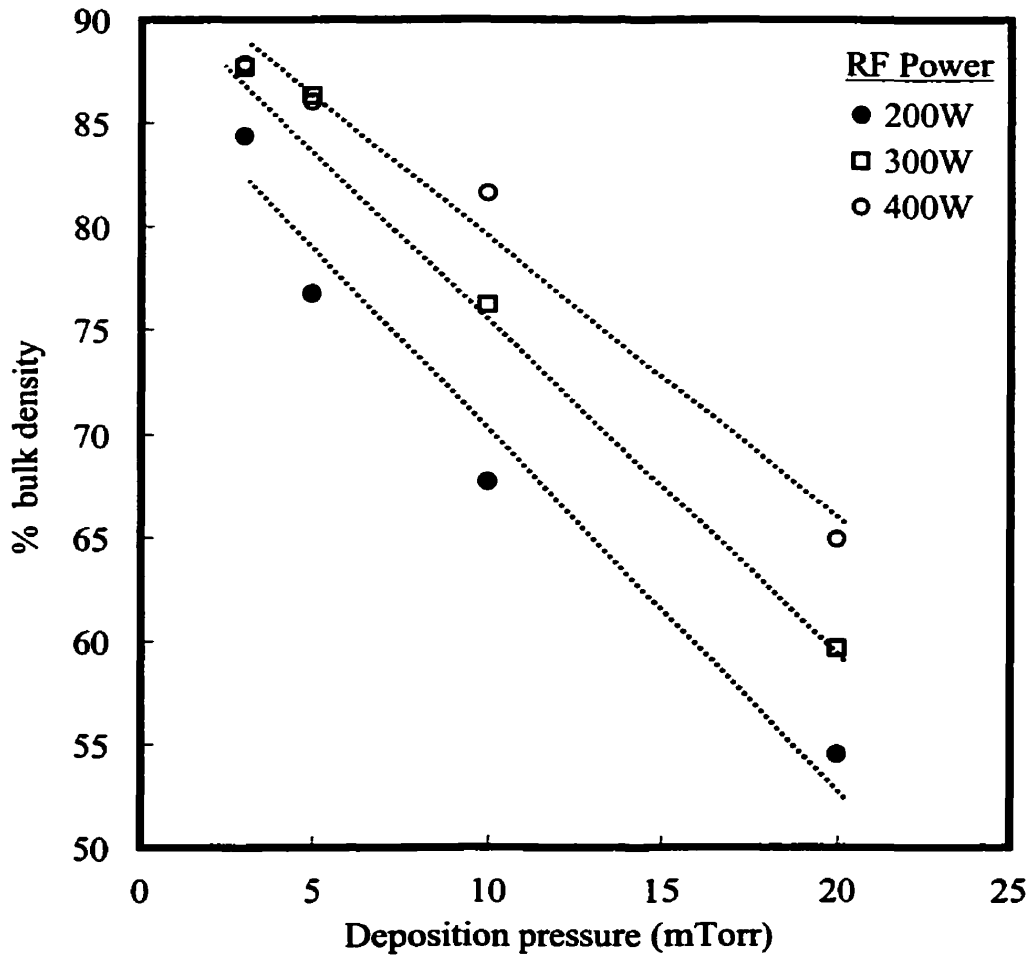


Figure 5.13: Mo film density (deposited at 25°C) relative to bulk.

compressive stress, regardless of the RF power. Without significantly undermining the film density (only 2-3% loss) (Fig. 5.13), Mo can be deposited at 5mTorr, which drastically reduces the stress as shown in Figure 5.12.

Mo layers are also deposited on glass as the gate metal of the TFT (see Fig. 4.3). Figure 5.14 shows the measured stress of 500nm Mo film deposited at 25°C on corning

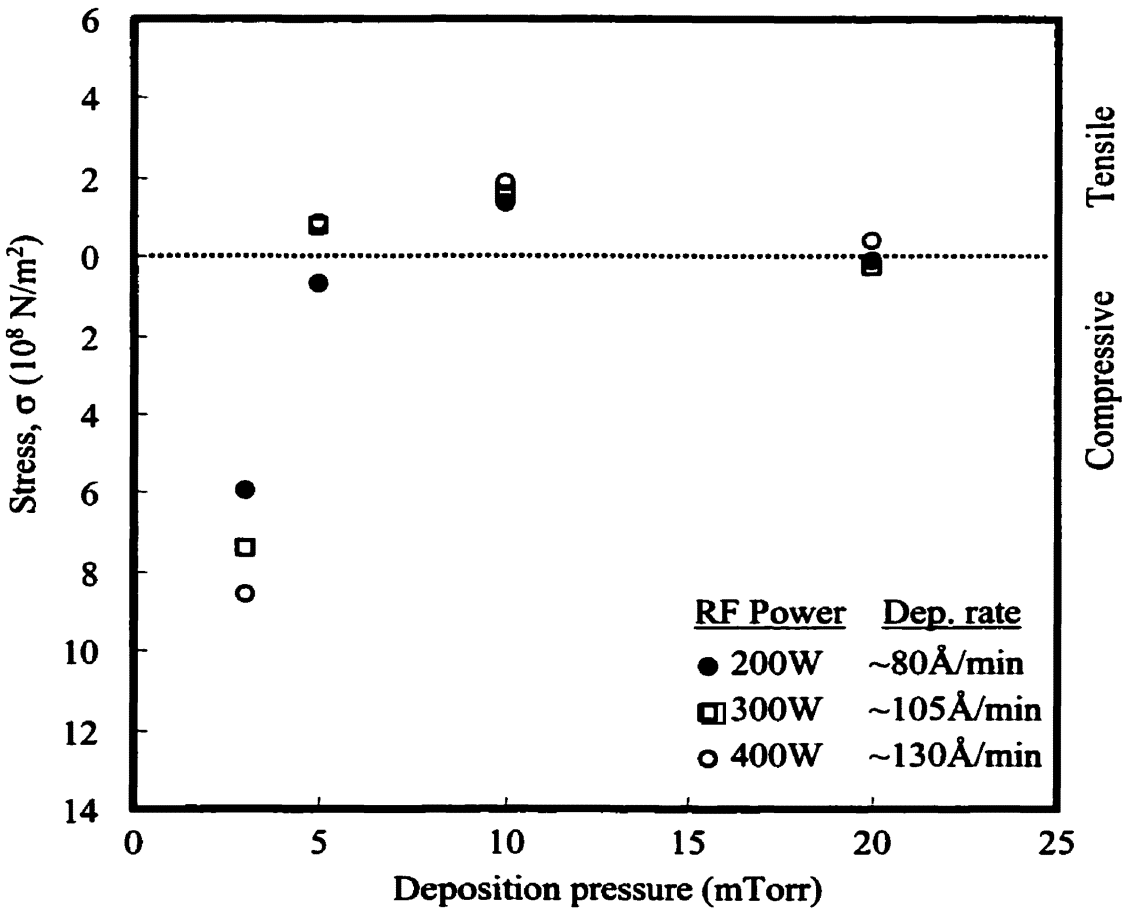


Figure 5.14: Measured stress, σ, of 500nm Mo film deposited at 25°C on glass substrates.

7059 glass. The shape of the curves is the same as that in Fig. 5.12. However, the magnitude of stress is slightly smaller. One of the requirements for the gate metal of the TFT is a low resistivity. Figure 5.15 shows the resistivity values of the Mo layer deposited on glass substrate. For the lowest resistivity, the Mo film should be deposited at 3mTorr. However, the compressive stress of Mo film deposited on glass at this

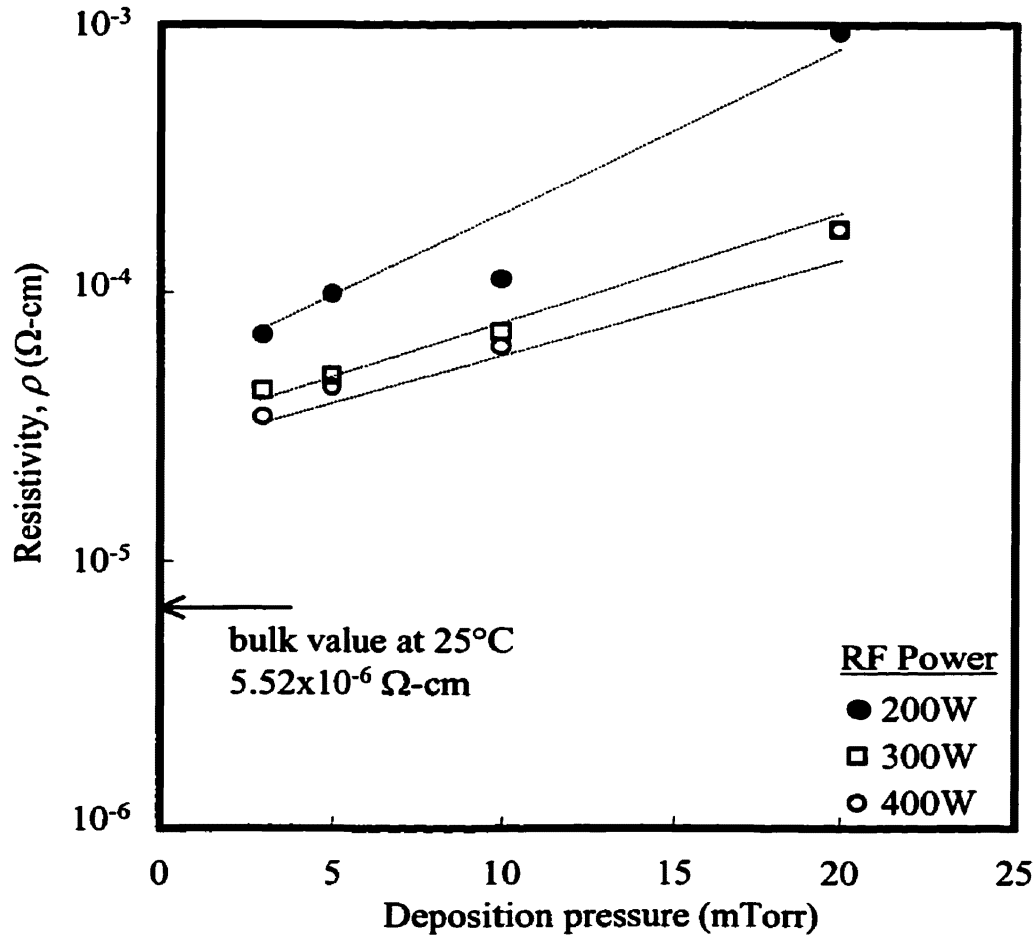


Figure 5.15: Resistivity of Mo film deposited at 25°C on glass substrates.

process pressure ranges from 0.598 GPa to 0.861 GPa. This high intrinsic stress, although it does not cause the films to peel off the glass substrate, can still undermine the mechanical integrity in view of subsequent deposition of high stress films. Therefore, it is recommended that the gate Mo be deposited at 5mTorr. For a lower resistivity gate metal, the use of Al instead of Mo is presented in section 2.3

5.5 Compressive or Tensile Intrinsic Stress of Mo Films

There are many models to explain why the intrinsic stress is formed when a film is deposited by a certain deposition method [76, 88 - 110]. The complexities of these explanations range from as simple as the thermal effect model [88] to as complicated as the lattice-misfit on the surface [102]. Most of these explanations can be applied to one specific film deposition mechanism. But none of them can adequately explain all cases. An investigation was conducted to explain why the intrinsic stress in a Mo film, deposited by magnetron RF sputtering, can be either compressive or tensile depending on the process pressure [111]. The following sections present possible causes of the Mo film stress that is presented in Figs. 5.12 and 5.14.

5.5.1 At Low Deposition Pressure

In figures 5.12 & 5.14, it is observed that the compressive intrinsic stress of the Mo films deposited at 3mTorr is very high. At low deposition pressures, there are not many collisions leading to a long mean free path of the sputtered species. Also, the rate of sputtered species arriving on the growing surface is high. At low pressure, because of the large concentration of species arriving at the growing surface coupled with a long mean free path, voids in the film are unlikely to be present as it is shown in the cross section SEM image of the film in Fig. 5.16. Also, at a high power, the surface is bombarded with ions [80], which results in a high density, smooth film (Fig. 5.17), whose intrinsic stress is compressive and increases with power. The higher film stresses of films deposited on i-a-Si:H, compared to those deposited on glass, may be related to the initial nucleation processes at the substrate surface. The deposition mechanism is illustrated in fig. 5.18.

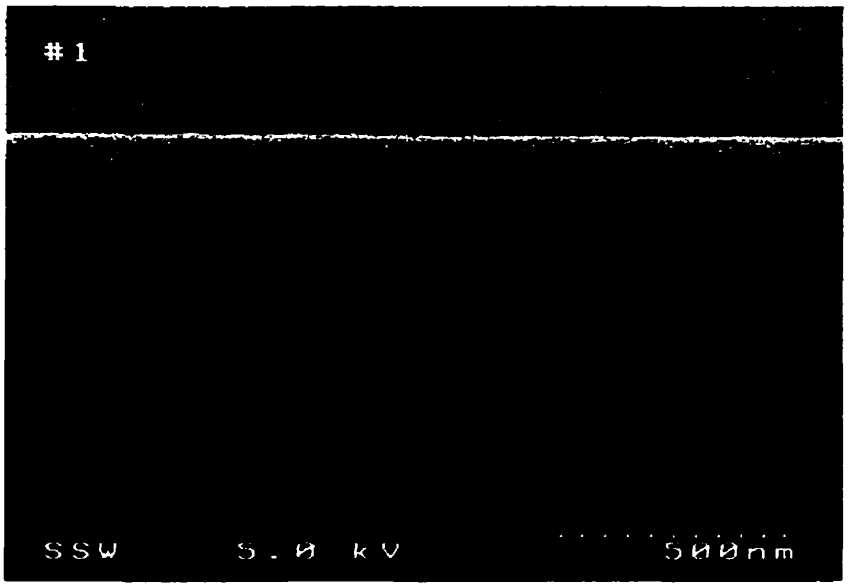


Figure 5.16: SEM cross section image of 500nm thick Mo film deposited at 3mTorr and 400Watts.

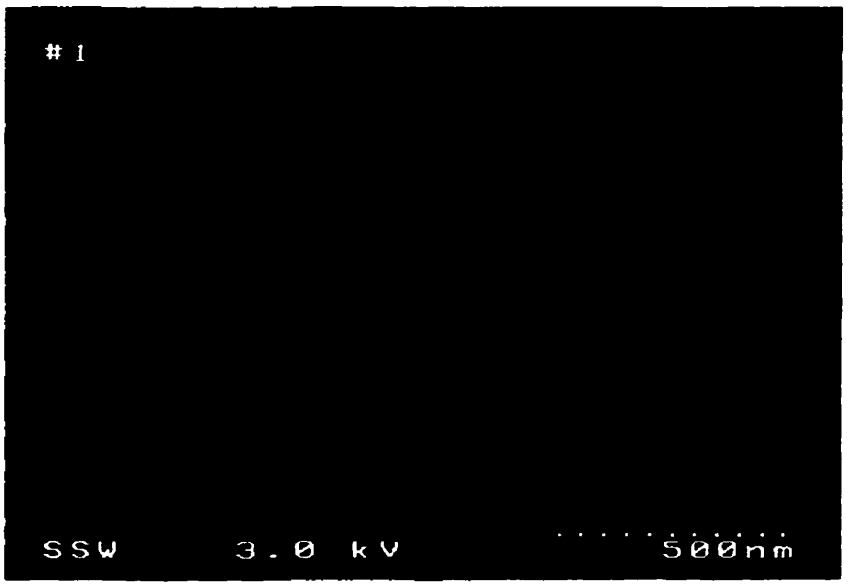


Figure 5.17: SEM surface morphology image of 500nm thick Mo film deposited at 3mTorr and 400Watts.

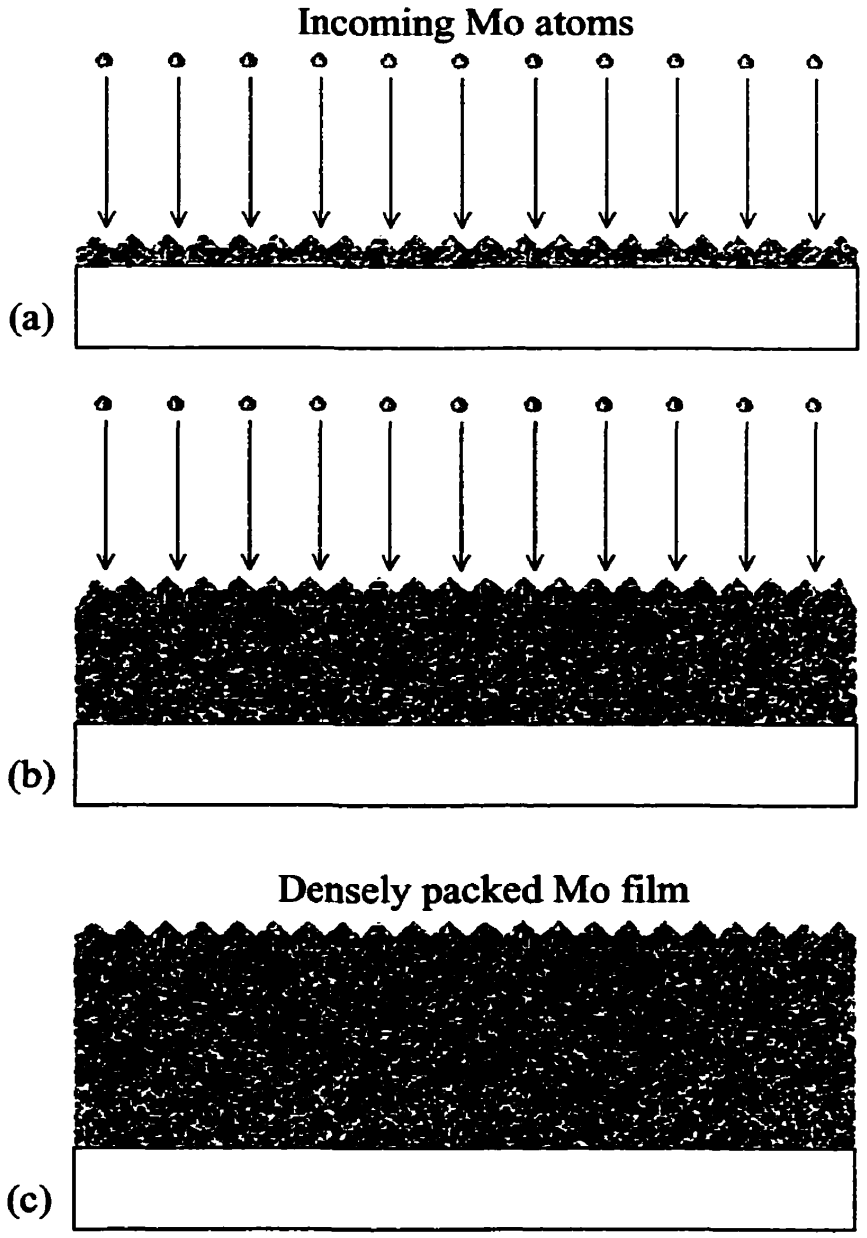


Figure 5.18: Mo deposition at low pressure. (a) Initial nucleation. (b) Incoming Mo atoms have high energy (high mean free path) and bombard on the surface. (c) The results is a densely packed Mo film.

5.5.2 At High Deposition Pressure

The Mo films deposited at high process pressure (20mTorr) have very small intrinsic stress. At high deposition pressures, there are a high number of collisions leading to a short mean free path of the sputtered species. Also, the rate of sputtered species arriving on the growing surface is low. After the initial nucleation at the substrate surface, the deposited film starts to grow in columnar pillars separated by voids (Fig. 5.19) [112], which serve as stress relief zones. The cross section of this film is shown in Figure 5.20. This type of film growth leads to low density (see Fig. 5.13), high surface roughness (i.e., poor reflectivity) as shown in Fig. 5.21 and high resistivity (see Fig. 5.15) films.

5.5.3 At Medium Deposition Pressure

At medium pressures (5-10mTorr), compared to high deposition pressure in section 5.5.2, there are fewer collisions resulting in an increased mean free path and higher rate of species arriving at the growing surface. Some of the species may go beyond the growing surface to get deposited around the columnar pillars, resulting in sealed voids (see Fig. 5.22). Figures 5.23 and 5.24 are the cross section of Mo films deposited at 5mTorr and 10mTorr, respectively. These sealed voids maintain the deposition pressure (5-10mTorr) even after they are brought to atmospheric pressure, causing the sealing boundaries to move inward. It is believed that the tensile film stresses observed at these intermediate pressures are caused by the contraction of the sealed voids. The higher tensile stress at higher RF power could be a result of higher density of sealed voids per unit volume. Because of these sealed voids, the densities of these films are not as high as that of film deposited at 3mTorr. Figures 5.25 and 5.26 are the surface SEM images of MO films deposited at 5mTorr and 10mTorr, respectively. From these figures, one observation is that the surfaces of these films are smoother than those observed in Fig. 5.21.

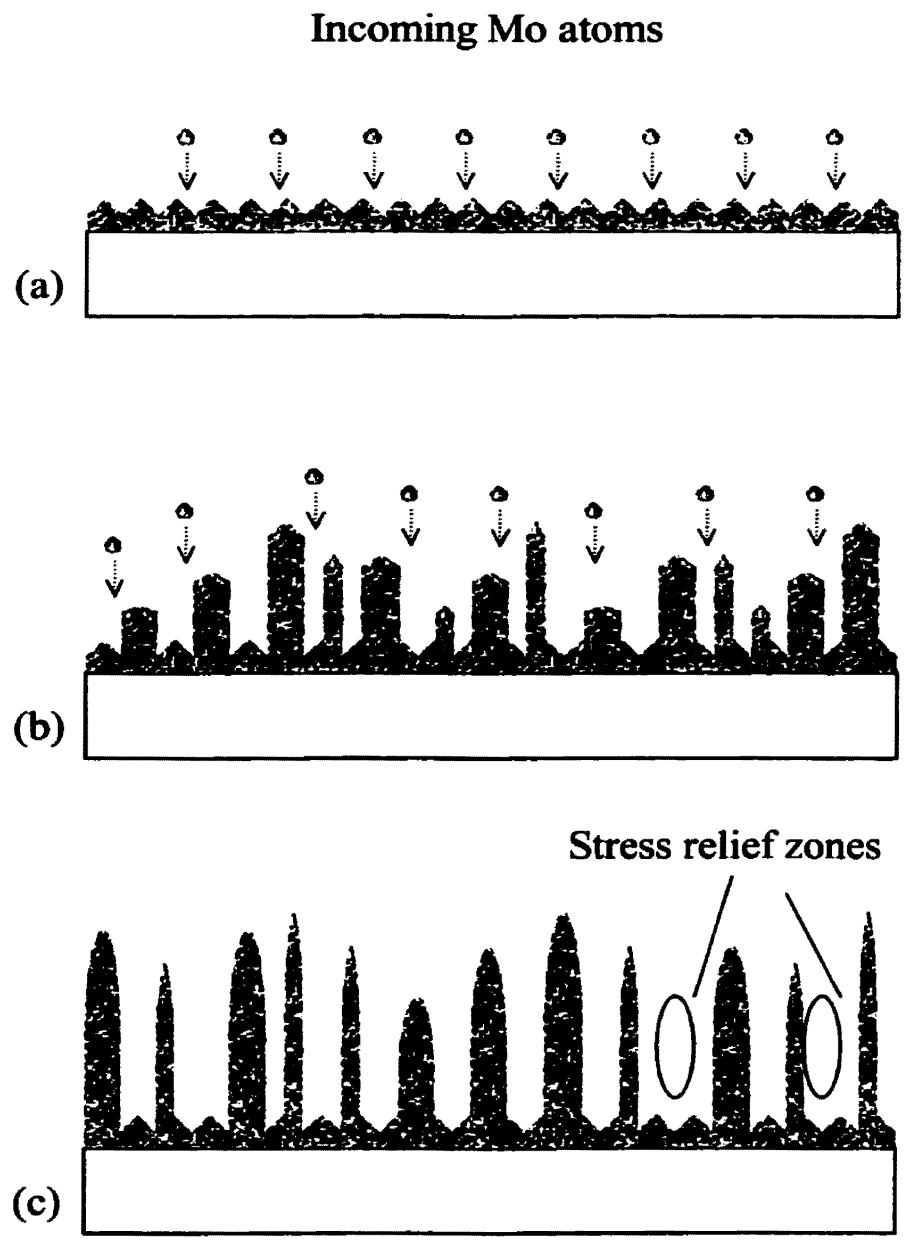


Figure 5.19: Mo deposition at high pressure. (a) Initial nucleation. (b) Incoming Mo atoms have small energy (short mean free path) and get deposited on top of the pillars. (c) The results is a porous Mo film.

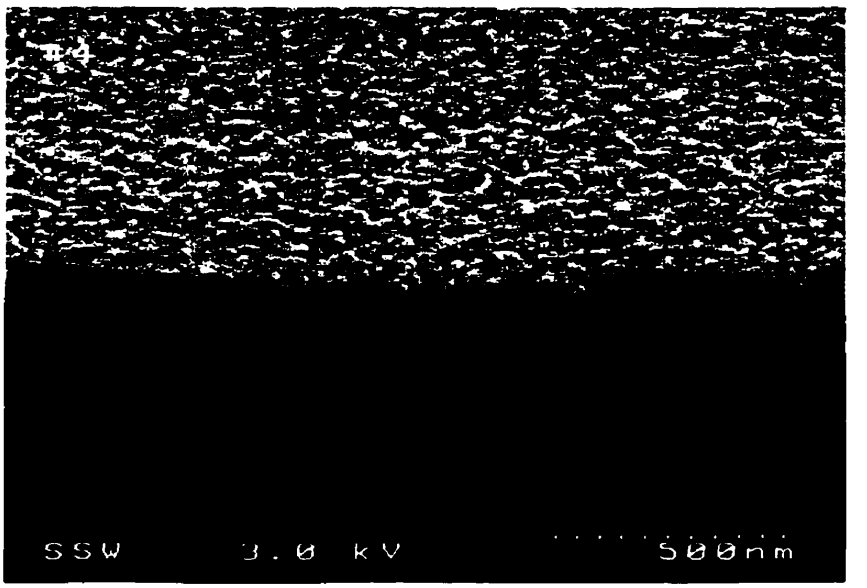


Figure 5.20: SEM cross section image of 500nm thick Mo film deposited at 20mTorr and 400Watts.

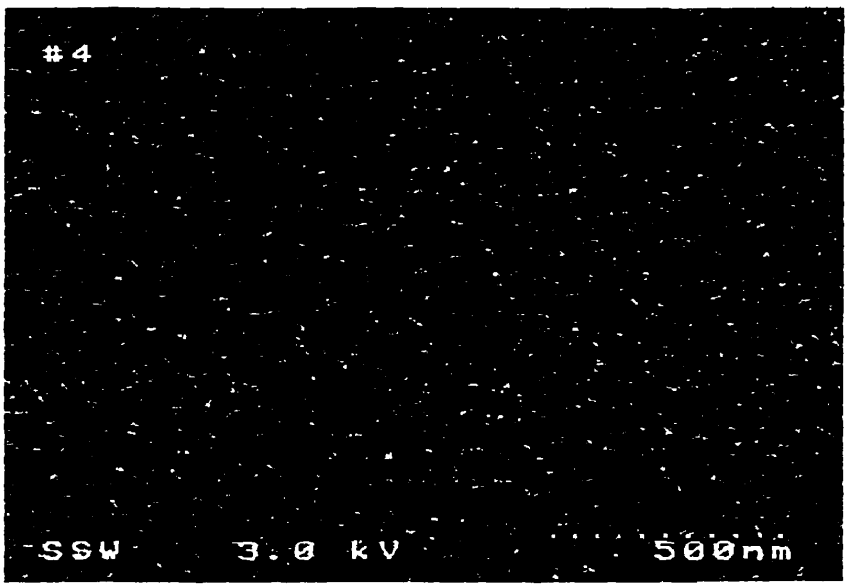


Figure 5.21: SEM surface morphology image of 500nm thick Mo film deposited at 20mTorr and 400Watts.

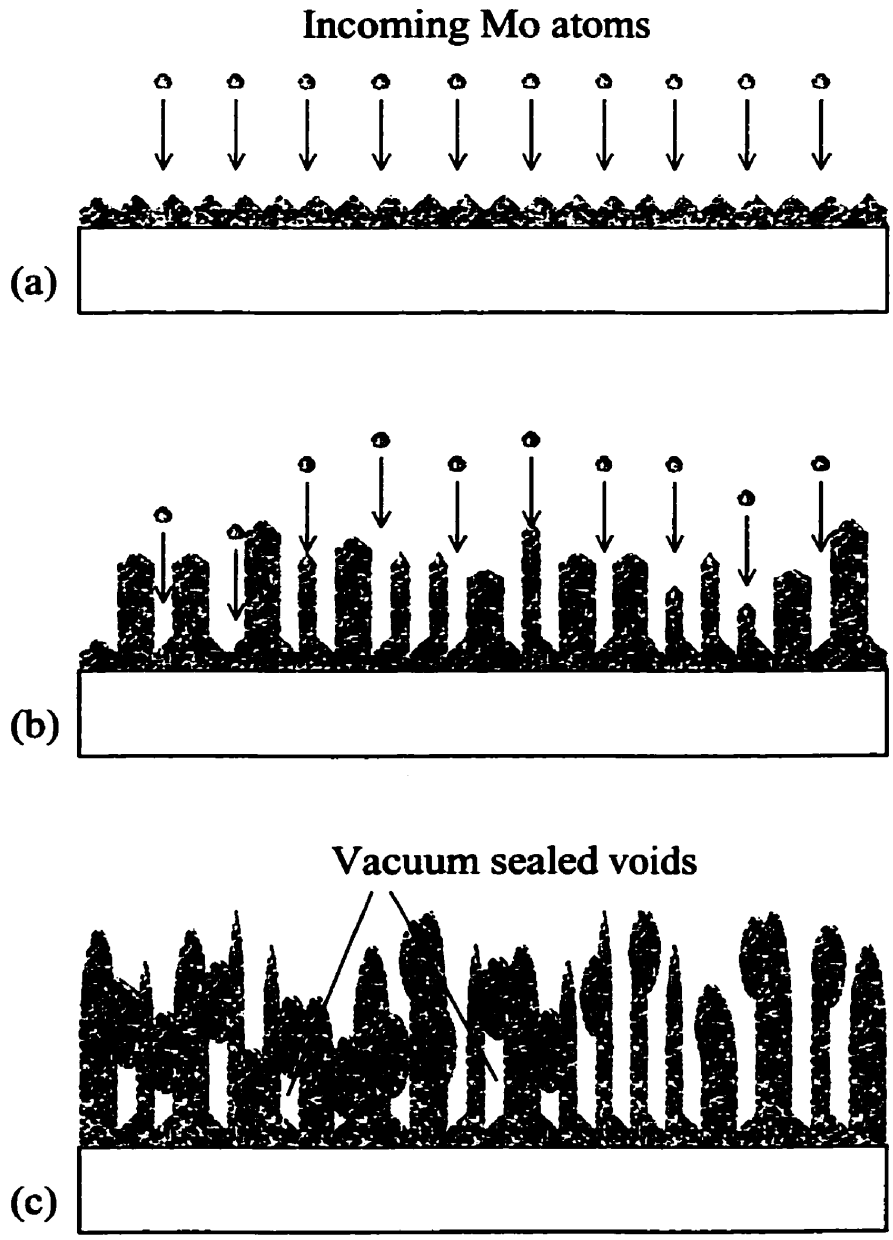


Figure 5.22: Mo deposition at medium pressure. (a) Initial nucleation. (b) Incoming Mo atoms just enough energy to travel below the surface and get deposited around the pillars. (c) The results is a film with vacuum sealed voids.

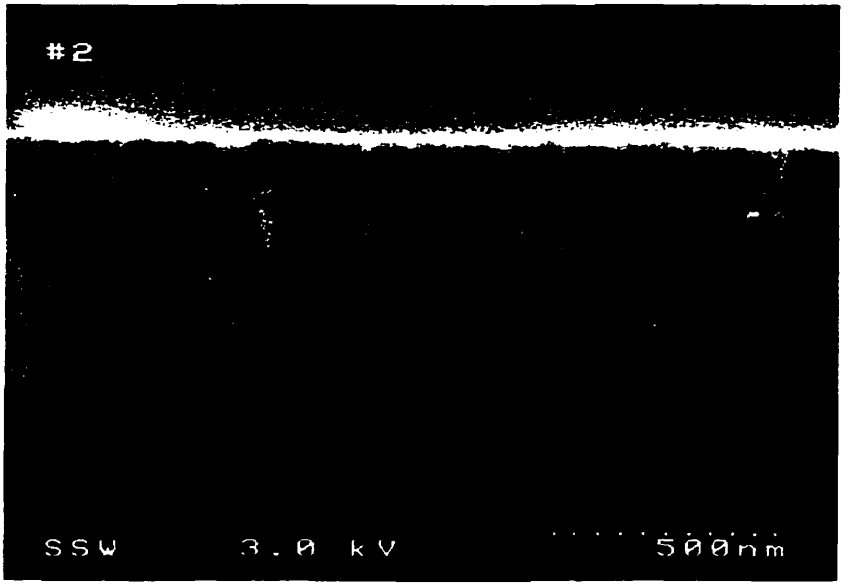


Figure 5.23: SEM cross section image of 500nm thick Mo film deposited at 5mTorr and 400Watts.

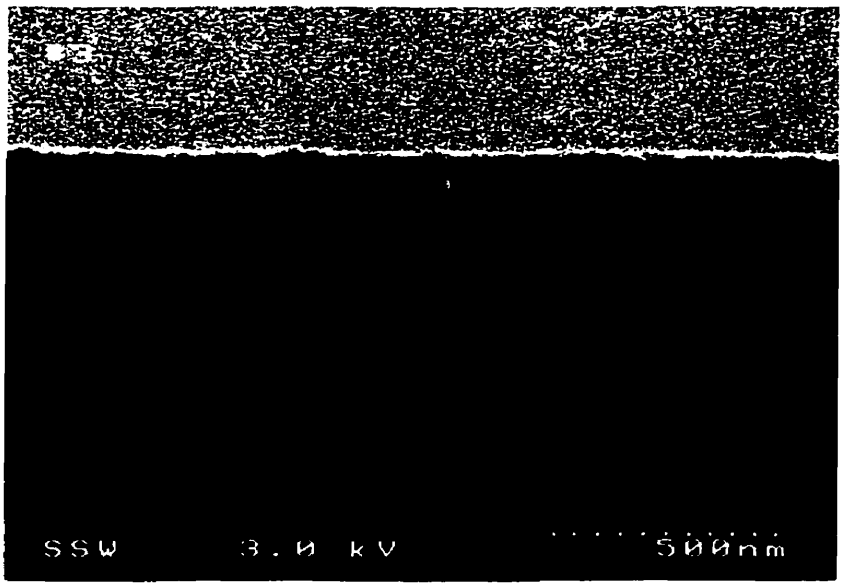


Figure 5.24: SEM cross section image of 500nm thick Mo film deposited at 10mTorr and 400Watts.

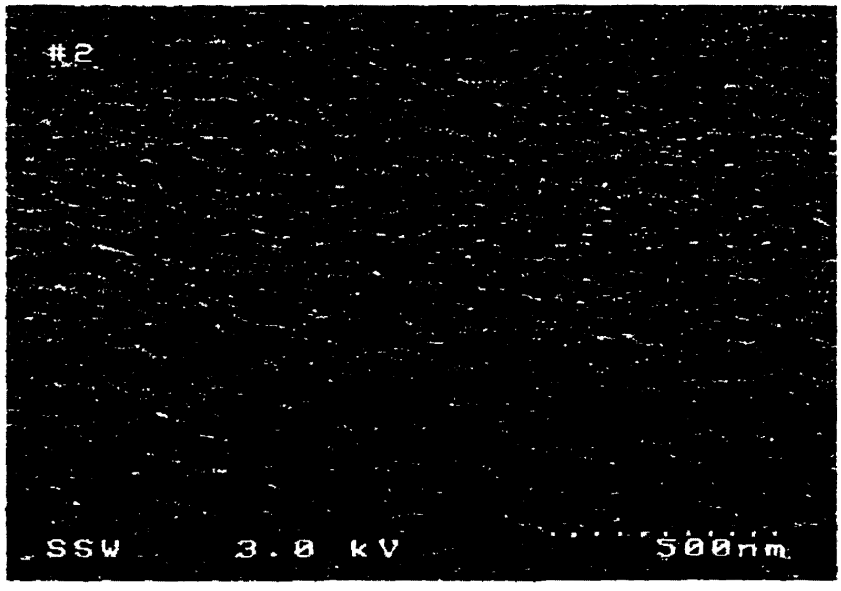


Figure 5.25: SEM surface morphology image of 500nm thick Mo film deposited at 5mTorr and 400Watts.

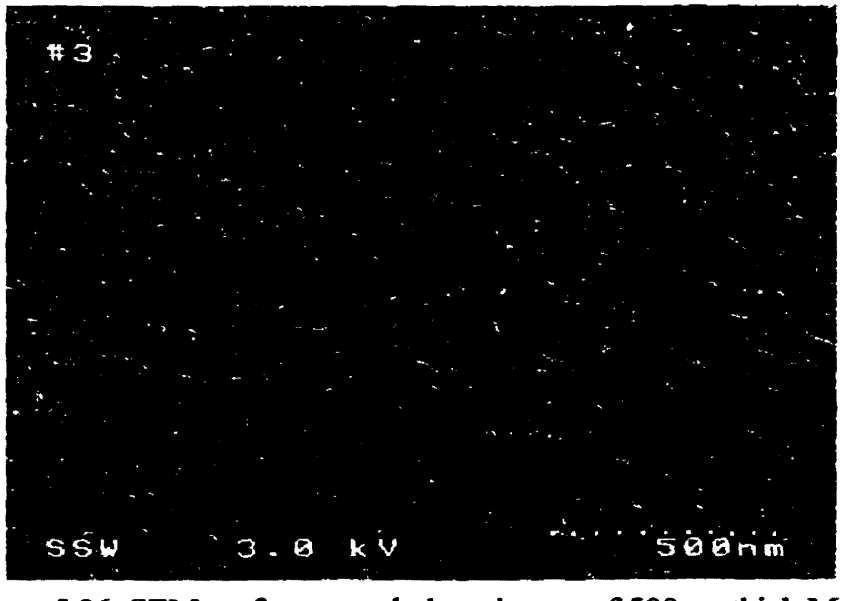


Figure 5.26: SEM surface morphology image of 500nm thick Mo film deposited at 10mTorr and 400Watts.

In Chapter 2, it was observed that the larger the grain size of the film, the higher the conductivity. In the case of Mo deposition, that rule does not apply. The resistivity of Mo film is mainly determined by the porosity of the film. When the film is porous, as in Fig. 5.20, the resistivity is high (10^{-4} ~ 10^{-3} Ω-cm). As the film becomes more stressed with decreasing deposition pressure, the resistivity decreases to ~3 x 10^{-5} Ω-cm.

5.6 Choosing the Process Pressure

The current trend in imaging arrays is towards smaller pixel sizes and higher integration density. Thus, it becomes more preferable that thin film devices be stacked on top of each other to maintain high fill factor requirements. Hence, it is important that the mechanical integrity of the stacked devices be preserved by lowering the intrinsic stress in thin films through careful selection of the right process parameters. This is particularly true in the case of direct imaging of x-rays using Mo/a-Si:H Schottky diodes, whereby the films can crack and peel off the substrate if the film stresses are not lowered by suitably varying process conditions such as RF power and deposition pressure. For example, the stress of Mo films deposited on i-a-Si:H can be lowered from ~10^9 Pa to ~10^7 Pa by increasing the deposition pressure from 3mTorr to 5mTorr, without seriously undermining the film density (2-3% loss) and resistivity (~0.1 μΩ-cm increase).

Chapter 6

Array Fabrication

Based on the technology presented from Chapter 2 to Chapter 5, two array designs are proposed. One of these designs was fabricated and verified for its correct functionality.

6.1 Array Designs

After observing the electrical performance of different pixel configurations, two different array processes were designed. Shown in Fig. 6.1 are masks for a 4x5 x-ray imaging array, a 2x2 array and test structures. This array process design is based on the pixel configuration in Section 4.2.1. This process requires 9 masks and 11 lithography steps. The channel of the TFTs used in this design is 20μm long and 200μm wide. All TFTs have 2μm of overlap area at both sides of gate (drain and source). The diodes are 200μm x 200μm. For these device sizes, the fill factor is 50.6%.

The other array design is based on the pixel configuration in Section 4.2.2. Shown in Fig. 6.2 are a 4x5 array, a 2x2 array and test structures for this design. This process requires only 7 masks and 9 lithography steps. In this pixel configuration, a

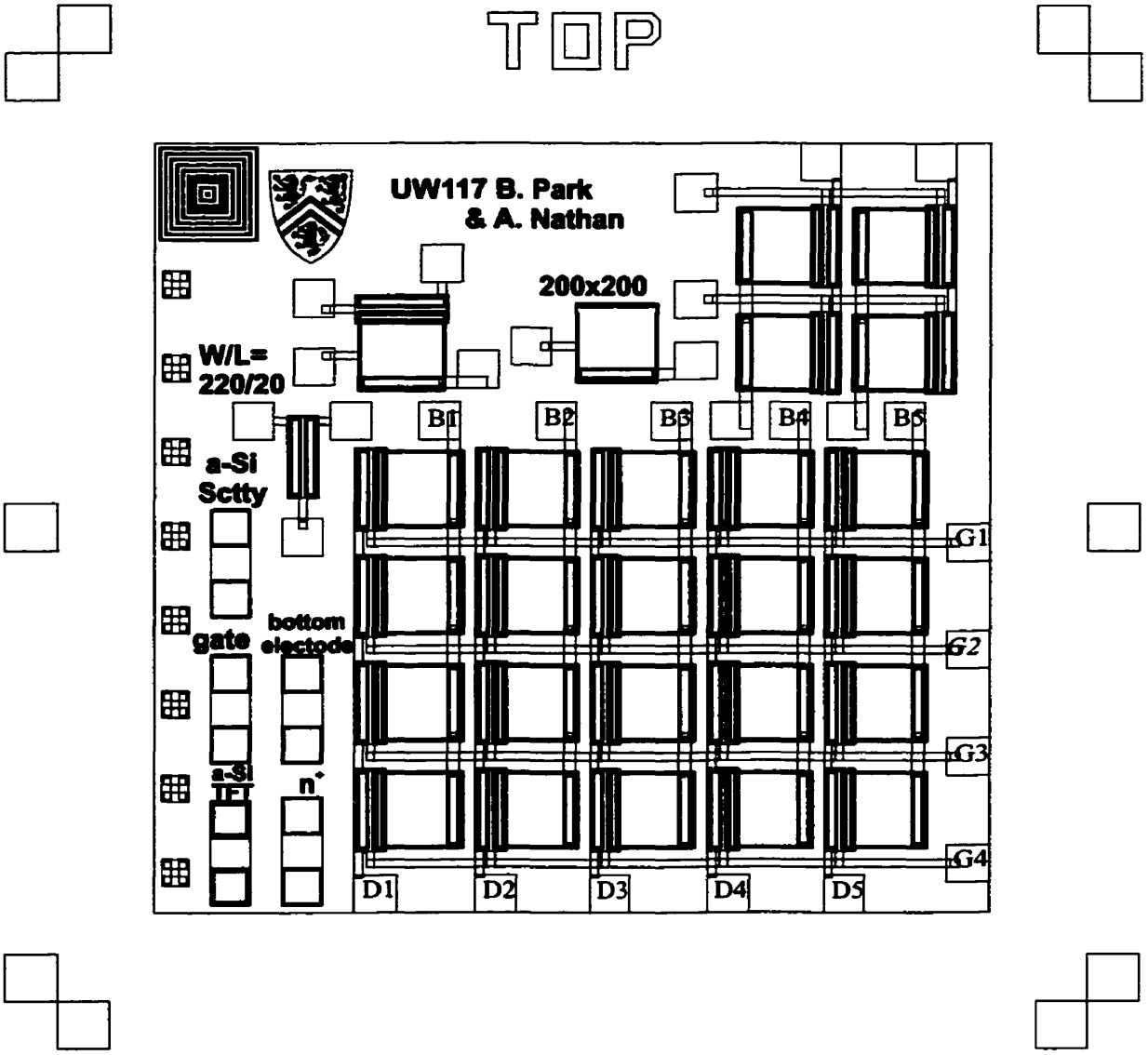


Figure 6.1: X-ray imaging array design based on the pixel configuration presented in section 4.2.1. Schottky diode: 200μm x 200μm. TFT: L 20μm, W 200μm. The top Mo layer can be replaced with ITO for optical imaging.

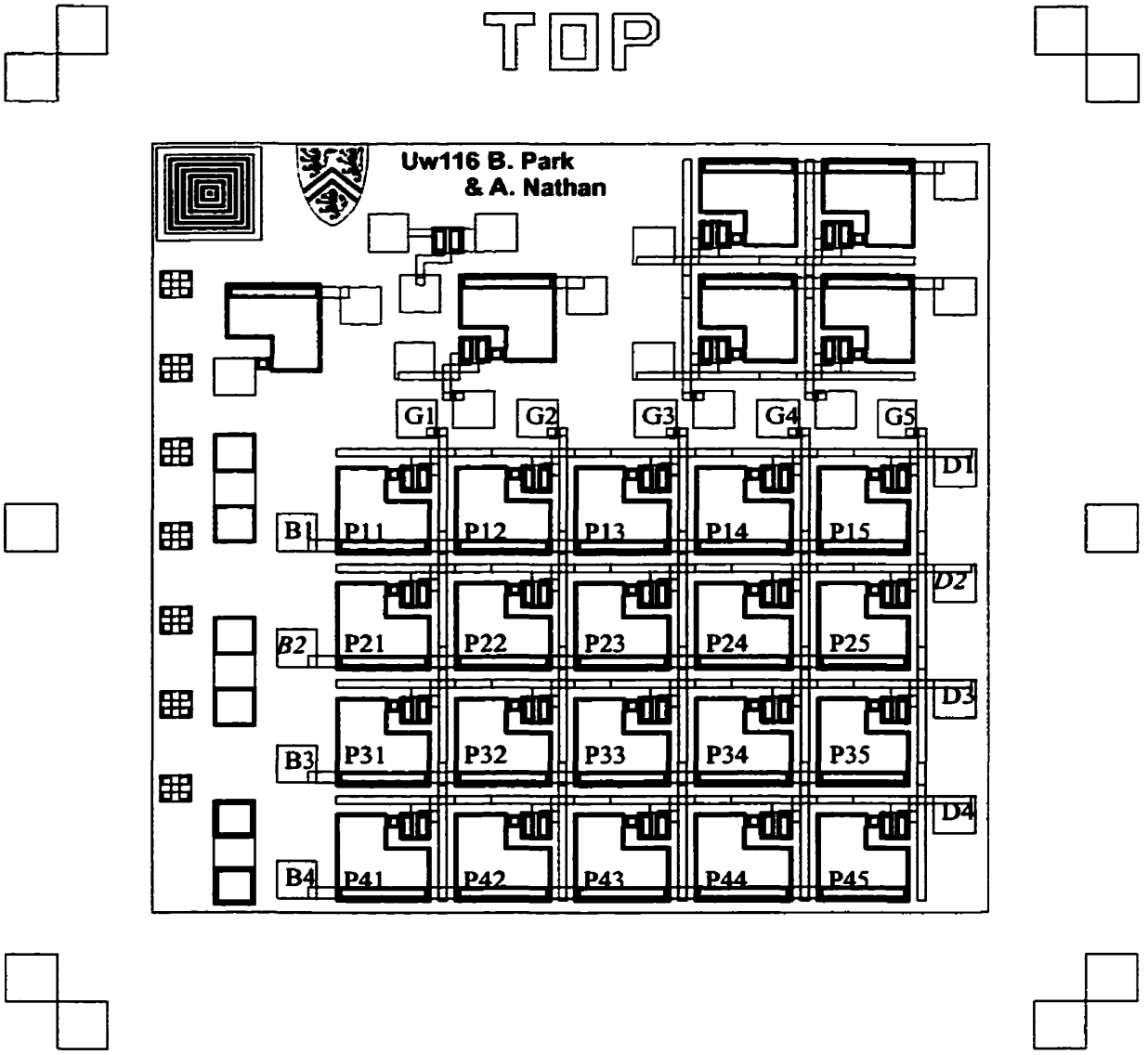


Figure 6.2: X-ray imaging array design based on the pixel configuration presented in section 4.2.2. Schottky diode: 43000μm^2. TFT: L 20μm, W 50μm. The TFT in each pixel occupies an area of 110μm x 90μm.

small portion of the detector area is used to accommodate the transistor (110μm x 90μm). The dimensions of the diodes are increased to 230μm to compensate for this loss in the detection area. The channel of the TFTs is 20μm long and 50μm wide. The overlap area is kept at 2μm. The fill factor of this array design is 48.6%.

In both designs, the top Mo layer can be replaced with a transparent metal (Ex. Indium Tin Oxide) to make an optical imaging array. All other fabrication process steps are compatible to those of the optical imaging array process. The bias lines are not connected in one line over the entire array for testability, which will be discussed further in Section 6.3.

6.2 Fabrication

The array design shown in Fig. 6.2 was fabricated for testing. Shown in Fig. 6.3 is the picture of a die on the wafer after all fabrication steps are carried out. The step-by-step description was presented in Fig. 4.5. Although this process involves fewer fabrication steps than the design proposed in Fig. 6.1, it is still very challenging to make a working device from a 9-step lithographic process at a university laboratory. In addition to that, there has been no discrete set of design rules for the amorphous silicon technology at the fabrication laboratory. It is not in the scope of this thesis to include the design rules. However, in Appendix E, a few critical rules are discussed.

6.3 Testing

The fabricated array has only 4 rows and 5 columns. For this small array size, it is not practical to generate an image with an x-ray phantom. However, each pixel in the array was tested for x-ray response just to verify its correct functionality.

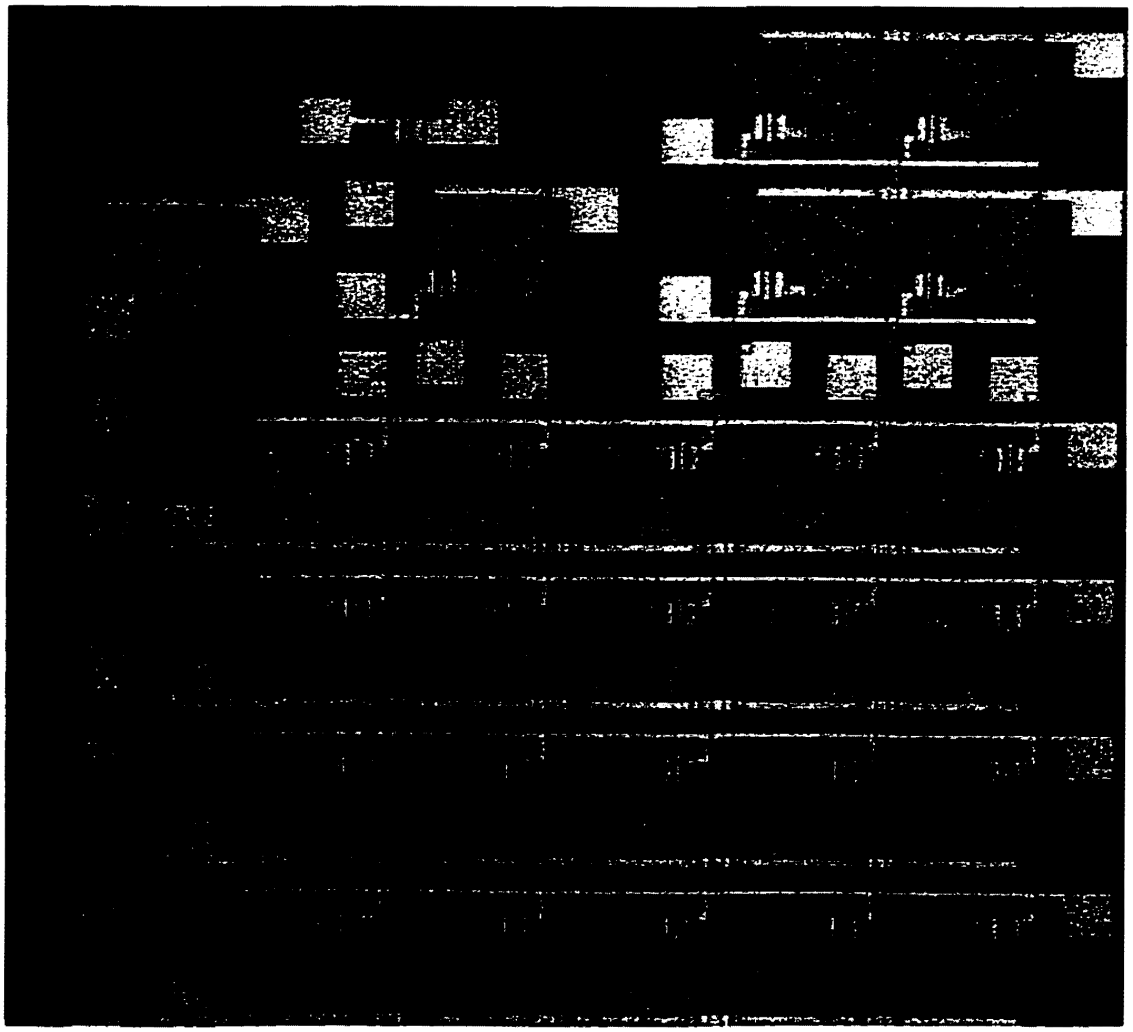


Figure 6.3: X-ray imaging array. The picture was taken after all fabrication steps were completed.

The measurement setup is the same as that described in Section 4.4.2. The biasing of the pixels and the measurement of current were carried out with Keithley 236 Source-Measure Units, remotely controlled by a computer via HPIB. The Schottky diodes were reversed biased with –2V (see Fig. 4.11). As in the case of a single pixel,

the gate of the TFT was pulsed at 1Hz to reset the voltage at the source of the TFT. The x-ray photocurrent was detected through the drain by the Keithley Source-Measure unit for a sampling period of 16.67ms (see Fig. 4.13). The testing was done without charge amplifiers attached to the data lines. Every pixel was tested individually. The pixels were exposed to x-rays for 50ms at an x-ray source voltage of 110kVp, generated by a Mercury Modular x-ray machine with a molybdenum target at 16 degrees. The x-ray radiation was measured with an RTI Solidose 300 Digital Dosimeter. The scatter in the measured x-ray dose was as large as ±25%, ranging from 200kVp to 320kVp. For fair comparisons, data was collected only when the variation in x-ray dose was less than 10% of an average value of 260mR. For supplying biases and recording currents, Keithley SMUs (model 236) were used. In real applications, the bias lines can be connected together. But since all pixels had to be tested individually, the bias lines were connected to the SMUs separately. For testing pixel, P11, in Fig. 6.2, the bias line, B1, was connected to –2V and the gate line, G1, was pulsed at 1Hz. The transferred charge was recorded at D1 for an integration period of 16.67ms. The most difficult part of this measurement was the x-ray on time, which had to be controlled by hand. This was rather a brute-force way of testing an array, but it provided the information of array functionality. Due to the large scatter in the x-ray radiation, only one measurement value per pixel was used to calculate the number of measured electrons in Table 6.1. The off currents of the pixels seem to have relatively small variation. They are within a few tens of femto-amperes (fA) which is the measurement limit of the SMU's. Compared to the off currents, the variation of the x-ray photo currents is quite large. There are several reasons to explain this large variation:

(i) The Schottky interface has large variation as seen in Chapter 3. It was shown in Fig. 3.1 that even at –1V the difference in the

Pixel index	Off current (fA)	% difference from average	X-ray dose (mR)	% difference from average	Photo current (pA)	% difference from average	No. of measured electrons (10^6)
P11	210	0.48	246.5	-3.63	58.0	-40.47	6.02
P12	190	-9.09	263.8	3.13	81.5	-16.35	8.47
P13	200	-4.31	258.7	1.14	92.0	-5.57	9.56
P14	250	19.62	256.0	0.08	175	79.62	18.2
P15	220	5.26	259.1	1.30	14.8	-84.80	1.52
P21	190	-9.09	244.3	-4.49	77.15	-20.82	8.02
P22	200	-4.31	268.7	5.05	104	7.10	10.9
P23	190	-9.09	260.3	1.77	100	2.79	10.4
P24	190	-9.09	230.9	-9.73	81.7	-16.15	8.49
P25	190	-9.09	267.9	4.74	109	11.72	11.3
P31	220	5.26	230.3	-9.96	176	80.64	18.3
P32	240	14.83	262.0	2.43	101	3.66	10.5
P33	210	0.48	271.5	6.14	106	8.54	11.0
P34	190	-9.09	236.0	-7.74	82.5	-15.32	8.58
P35	190	-9.09	261.9	2.39	101	3.61	10.5

Table 6.1: Off currents, photo currents and number of measured electrons of pixels of x-ray imaging array shown in Fig. 6.3.

Pixel index	Off current (fA)	% difference from average	X-ray dose (mR)	% difference from average	Photo current (pA)	% difference from average	No. of measured electrons (10^6)
P41	200	-4.31	236.4	-7.58	78.2	-19.74	8.13
P42	210	0.48	269.4	5.32	105	7.46	10.9
P43	220	5.26	260.9	2.00	100	3.10	10.7
P44	240	14.83	261.9	2.39	101	3.61	10.5
P45	230	10.05	269.2	5.24	105	7.36	10.9
AVE	209.0		255.8		97.43		10.1
STDEV	19.44		13.42		34.42		3.586

Table 6.1: Continued from the previous page.

leakage current density among the diodes of the same dimensions can be very large.

(ii) The hand-triggering of x-ray photons is not accurate. X-ray should be on at the same point in from t = 0s for all pixels. This is hard to achieve without a computer-controlled triggering system.

(iii) It is also possible that the transistor is defective. If the TFT's on current is not as high as it is supposed to be, it can result in low photo current, and hence, reduced number of measured electrons.

Due to the large variation in the photo currents, the number of measured electrons also resulted in a large range of 1.52 million electrons to 18.3 million electrons with the standard deviation of 3.59 million electrons. This crude testing demonstrated that the design of the array is valid. However, for more rigorous testing, it requires a readout circuitry with charge amplifiers and automated x-ray triggering.

6.4 Evaluation

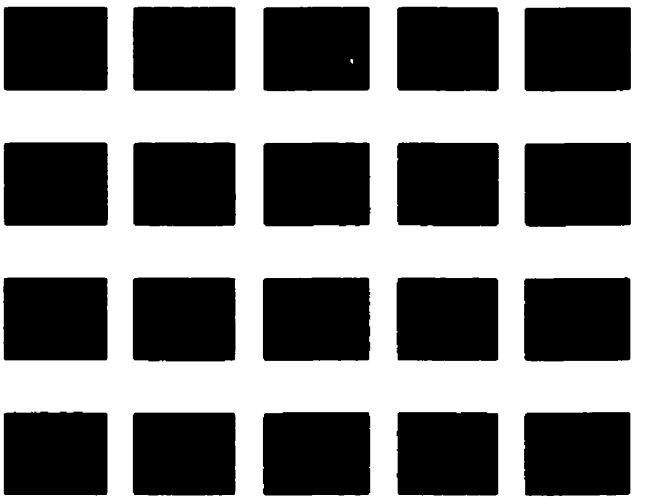
Based on the measured data in Table 6.1, images are produced by applying very simple digital signal processing filters (see Figs. 6.4 and 6.5). The filters used for these images,

$$Y = -\{190 + (\textit{dark current in fA from Table 6.1})\} \times 2 \qquad \{6.1\}$$

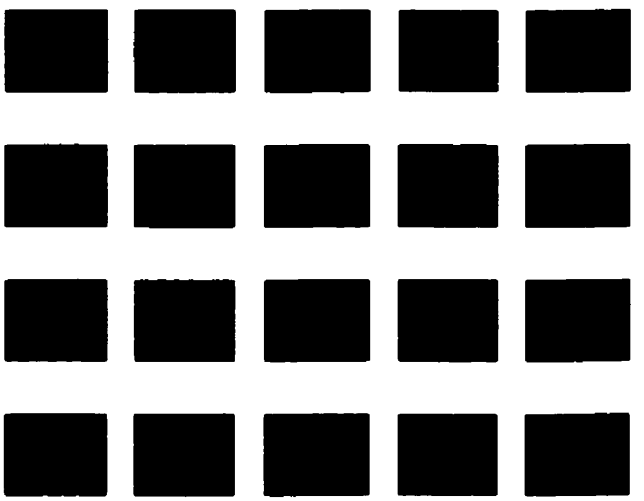
for the image with no illumination and

$$Y = 235 - 1/2(176 - \textit{photo current in pA from Table 6.1}) \qquad \{6.2\}$$

for the image taken with the existence of x-rays, are only for illustrative purposes. The coefficients in these filters are arbitrarily chosen for the best presentation, such that it is easy to see the spatial artifacts seen in Figs. 6.4 and 6.5. Shown in Figure 6.4a) is the image with no c-rays in an ideal case, where the Schottky diodes and the TFTs have low uniform leakage current. All pixels are black. The actual image taken with no x-rays is shown in Fig. 6.4b). As one could have easily predicted from the values in Table 6.1, some pixels are not as dark as the others. But one has to keep in mind that two different filters are used, Eqs. 6.1 and 6.2, to amplify the pixel non-uniformity. If a real world DSP filter is applied, the non-uniformity shown in Figure 6.4b) may not be as bad as it is shown here. An ideal image with x-ray illumination is shown in Fig. 6.5a). In that image, all pixels are uniformly white. The actual image taken with the fabricated array, after being processed by the filter in Eq. 6.2, is shown in Fig. 6.5b). It can be clearly

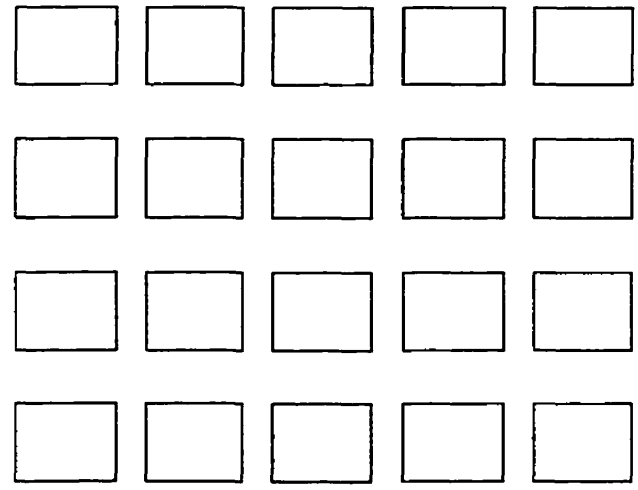


(a)

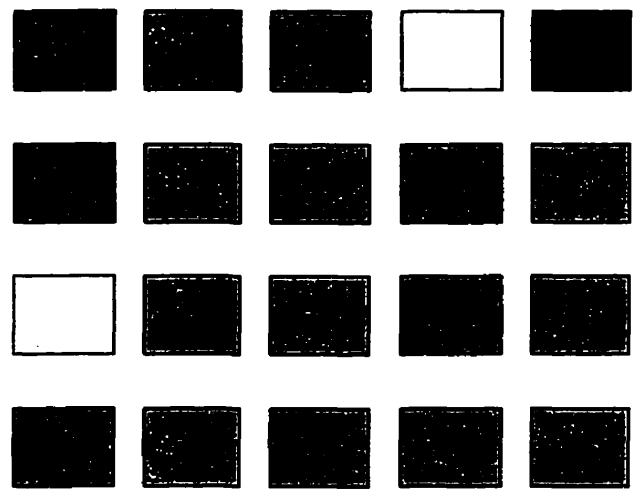


(b)

Figure 6.4: Image taken by the array shown in Fig. 6.3 without the x-ray illumination. (a) shows an ideal case image. (b) is created by a filter in Eq. 6.1.



(a)



(b)

Figure 6.5: Image taken by the array shown in Fig. 6.3 with the presence of x-rays. (a) shows an ideal case image. (b) is created by a filter in Eq. 6.2.

seen here that not all pixels are as white as they can be. The possible reasons for this non-uniformity were discussed in the previous section.

One of the very first questions that should be asked when designing or testing an imaging array is how sensitive are the detectors to the light being captured. This figure of merit is characterized by quantum efficiency, the ratio of the number of electrons collected by the pixel to the number of incident photons, which was already mentioned in Chapter 1. Sensitivity depends on the wavelength of the light. The detector introduced in section 1.4.3 was chosen to have Mo layer thickness of 500nm so that it is most sensitive to the x-rays in the source voltage of 20kVp to 100kVp. Sensitivity also depends on the fill factor, a design requirement that is mentioned at several places in this thesis. Fill factor is the proportion of the pixel area that is actually sensitive to the input signal. The higher the fill factor, the higher the array sensitivity. Especially for energetic x-ray photons that do not get absorbed easily, fill factor is a crucial array figure of merit. The fill factors of arrays in Figs 6.1 and 6.2, ~50%, are limited by the lithographic design rule at the fabrication laboratory. The pixel design in Chapter 4 (see Fig. 4.2) is estimated to accommodate a fill factor of ~80% if the metal line spacing can be as small as 5μm and the line width is as narrow as 8μm.

Another array property that is influenced by the pixel design is the maximum measurable signal, also known as the full well capacity. In this application, with an exception of radiation therapy, the x-ray source voltage range of interest does not exceed ~120kVp. And the radiation coming through an object or (a human body) gets attenuated. Considering these, the x-ray radiation received while testing in section 6.3 is most likely to be higher than what is necessary. In other words, the pixels in this imaging array have big enough well capacity to process the necessary signal.

Dynamic range is defined as the ratio of the maximum possible signal recorded by the array to the noise signal. In Table 6.1 the maximum photocurrent is 176pA and

the lowest dark current is 190fA. The dynamic range of this array is roughly ~1000. If this information is to be digitized, it will require a system with 10-bit long data string.

In Figure 6.5, there appears to be some spatial artifacts, namely fixed pattern noise (FPN). The main source of the FPN is considered to be the non uniformities of the devices that comprise the pixels. In this application, the devices are a Schottky diode and a TFT. In chapter 3, the non uniformity of the Schottky diodes were presented. The FPN in Fig. 6.5b) is most likely to be caused by the poor reproducibility of the Schottky interface, which was discussed in section 1.4.3. Despite of this disadvantage of FPN in using Schottky diodes to detect x-rays, there are a couple of important measures of array quality that do not require paying extra attention to. One of them is image lag, a temporal artifact. Image lag is a crucial figure of merit in Fluoroscopy. Compared to the x-ray detection array with a-Se as the photoconductor, which suffers from image lag due to the poor charge collection in a-Se layer, this array design based on Mo/a-Si:H can process the image as fast as the array with p-i-n diodes. Also, in an array with p-i-n diodes and a phosphor layer, blooming can happen if the incident x-ray photon produces very bright light. The signal that is meant to be read by only one pixel can be picked up by the neighboring pixels, which is also known as spill over. In the array based on Mo/a-Si:H Schottky diode, this blooming is not likely to happen.

The array in Fig. 6.3 is the very first two dimensional array deposited at the University of Waterloo. Although it is demonstrating a FPN, the design is proven to be valid. The project have two main options at this point. The first option is to improve the interface quality of the Schottky diodes. But as explained in section 1.4.3, poor reproducibility is an intrinsic property of the Schottky diode. Inserting a thin nitride layer could improve the quality as it was suggested in Chapter 3. Another option is to investigate the feasibility of developing p^+ Si:H deposition process so that the Schottky diodes can be replaced by p-i-n diodes. In either cases, the mask set used for fabricating the array in Fig. 6.3 can be used.

Chapter 7

Conclusions

This thesis describes the fabrication issues underlying integration of the direct detection Mo/a-Si:H Schottky image sensor with the thin film transistor, along with improvements made on TFT device and fabrication. With the latter, we specifically address the use of n^+ μc-Si:H for the contact layers and Al for the gate material.

The effect of the deposition temperature(T_d) on the structural properties of n^+ doped hydrogenated micro-crystalline silicon (n^+ μC-Si:H) was studied through grazing incidence x-ray diffraction, Raman spectroscopy and Fourier transform infra red spectroscopy measurements. It was observed that the films deposited at low temperatures ($T_d \cong 200^oC$) showed more crystallinity, whereas the films deposited at high temperatures ($T_d \cong 400^oC$) were more amorphous. The elimination of the hydrogen atoms from the film surface appeared to be correlated with the transition from the amorphous to the crystalline phase. It is believed that at low deposition temperatures, the interaction between H atoms, from H_2 dilution and from S-H bonds, forms volatile H_2 molecules and leaves a relaxed Si-Si network on the surface, hence the crystallization occurs. At high deposition temperatures, a transition between the hydrogen out-diffusion from Si-H bonds, and the hydrogen incorporation by H_2 dilution

may lead to formation of Si-H bonds again on the surface at a particular chemical equilibrium, which causes the film to remain amorphous.

The performance of Al-gated a-Si:H TFTs were compared in terms of leakage current, field effect mobility, and threshold voltage shift, in which the sputter deposition conditions of Al were systematically varied in an attempt to reduce surface roughness induced by thermal processing. At low deposition temperatures and process pressures, the deposited films showed a relatively smooth surface, e.g., gate films deposited at 30°C/5mTorr/300W yielded TFT characteristics with low leakage current (~ 10 fA at low V_{DS}), an ON/OFF ratio better than 10^8, and a mobility of 1.1 cm^2/Vs - values comparable to TFTs fabricated using Mo gates.

Different pixel designs were studied in an attempt to integrate of an x-ray sensor and a TFT. The fully overlapped structure, while it better satisfied the fill factor requirement, suffered from high leakage current (~ 100 nA). In contrast, the leakage current of the partially overlapping structure was around 100 fA at low gate voltages. In both structures, the stress of the Mo layer in the Schottky diode had to be reduced in order to preserve the mechanical integrity of the stacked film structure. The stress was not as severe in the non-overlapping structures. Also, the leakage current was small.

The current trend in imaging arrays is geared towards smaller pixel sizes and higher integration density. Thus it becomes imperative that thin film devices be stacked on top of each other to maintain high fill factor requirements. Hence, it is important that the mechanical integrity of the stacked devices be preserved by lowering the intrinsic stress in thin films through careful selection of the right process parameters. This is particularly true in the case of direct imaging of x-rays using Mo/a-Si:H Schottky diodes, whereby the films can crack and peel off the substrate if the film stresses are not lowered by suitably varying process conditions such as RF power and deposition pressure. For example, the stress of Mo films deposited on i-a-Si:H could be lowered from ~10^9 Pa to ~10^7 Pa by increasing the deposition pressure from 3mTorr to 5mTorr,

without seriously undermining the film density (2-3% loss) and resistivity (~0.1 μΩ-cm increase).

In extending the test array design to large area arrays, there are a few technological challenges to be considered. First, as it was demonstrated in chapter 3, the Schottky interface made of the Mo and a-Si:H films shows wide variation in the leakage current. More research is required to reduce the variation in leakage currents of the sensors. One proposal is to insert a thin insulating layer between the metal and silicon to make a m-i-s structure (see Figs. A.1 and A.2). This thin insulating layer may significantly reduce the leakage current. But it requires a process development of hydrogen plasma treatment. Alternatively, the Schottky diode can be replaced with a p-i-n diode. One possible approach is to use hydrogen plasma treatment to improve the electrical integrity of the a-Si:H/insulator interface.

Appendix A

Fabrication Mask Designs

This section presents the mask layouts developed and used for this project. The array designs are presented in Figs. 6.1 and 6.2. It is only a small scale array (4 x 5), but with future upgrade to the university laboratory, a larger scale array can be produced using these small arrays as templates. As mentioned before, the top layer, Mo, can be replaced with ITO for optical imaging. Figure A.1 is the mask design for an m-i-s structure whose side walls will be passivated with silicon nitride. The challenge in this process is a development of hydrogen plasma process. After etching with HF solution (Fig. A.2), the i-a-Si:H surface is exposed to air. Before an insulating layer is deposited on this surface, it is suggested that a cleaning (or even etching) process is applied. The devices in Figure A.3 are the Schottky diodes in parallel. This structure was used to get an average value of many devices. Also, when measuring small leakage current, connecting many devices in parallel and dividing the current is easier than measuring the leakage current of one single device. Shown in Fig. A.4 are the mask layouts for the old Schottky diode process (see Fig. 3.3). Again, the devices are connected in parallel. Fig. A.5 is the mask design for the non-overlapping pixels. The stacked pixel design is presented in Fig. A.6.

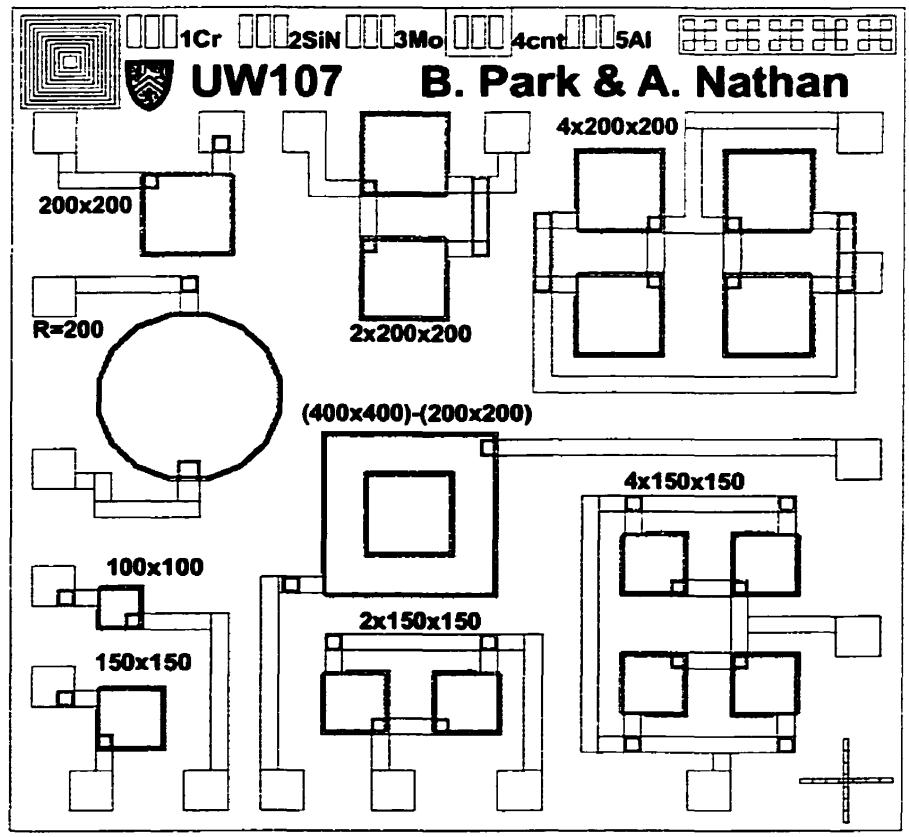


Figure A.1: Mask layout design for an m-i-s structure. The fabrication sequence is illustrated in Fig. A.2. This process requires a hydrogen plasma treatment at the insulator/silicon interface.

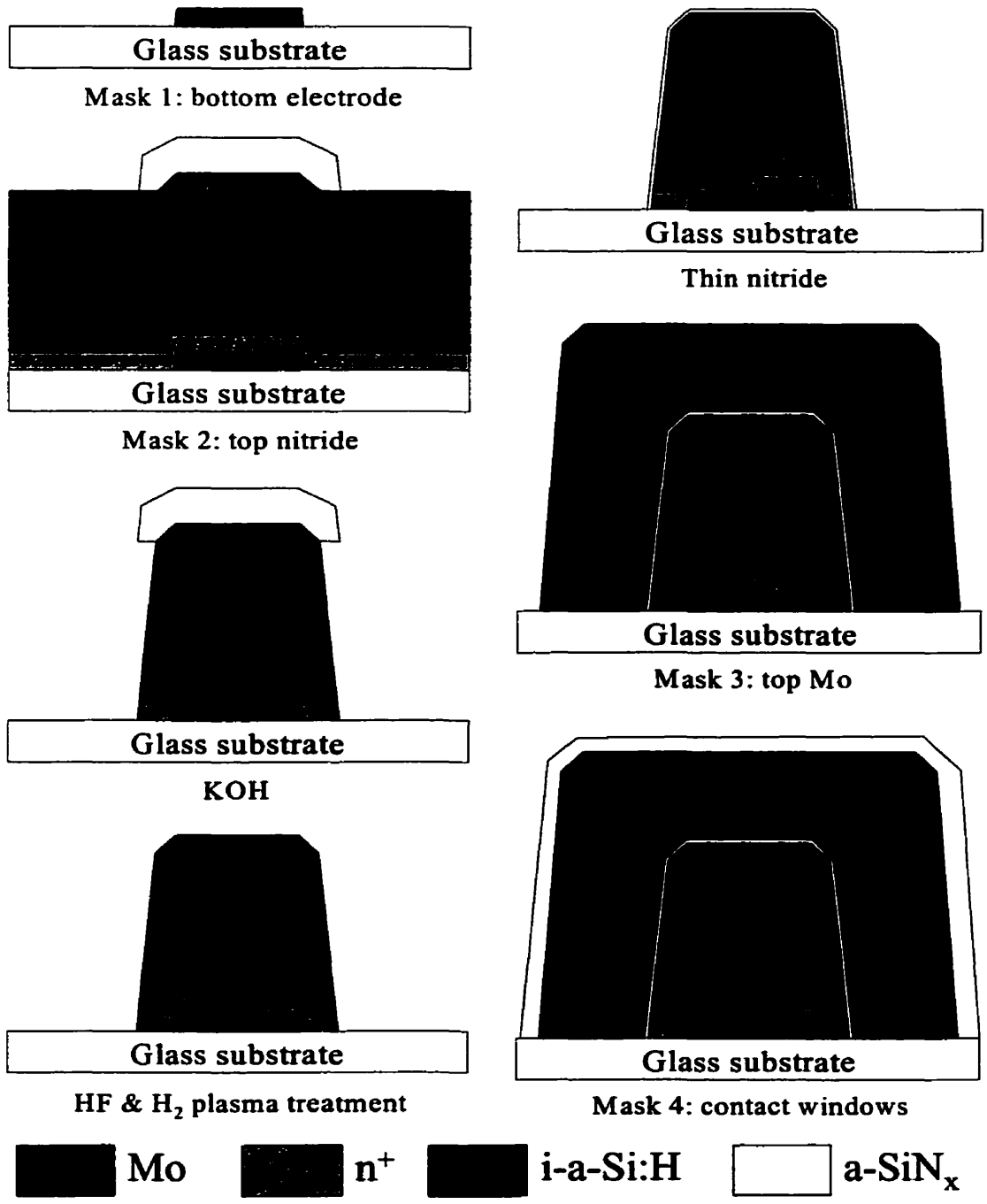


Figure A.2: X-ray sensor fabrication sequence based on m-i-s structure.

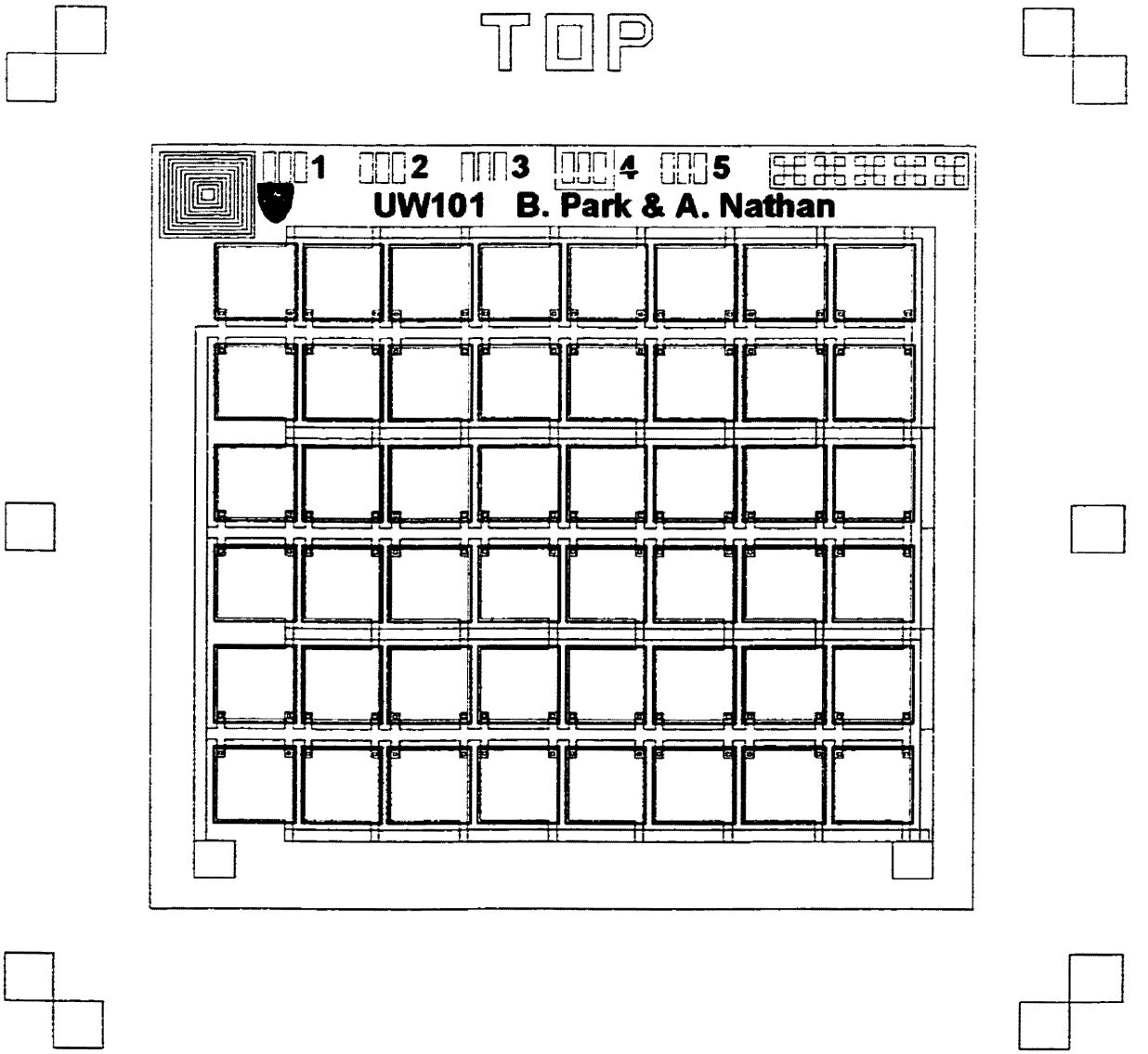


Figure A.3: 48 Schottky diodes connected in parallel. This design was used to measure the leakage current of the diode in section 3.2 and 3.3. All diodes are 200μm x 200μm. The fabrication sequence of this diode process is illustrated in Fig. 3.4.

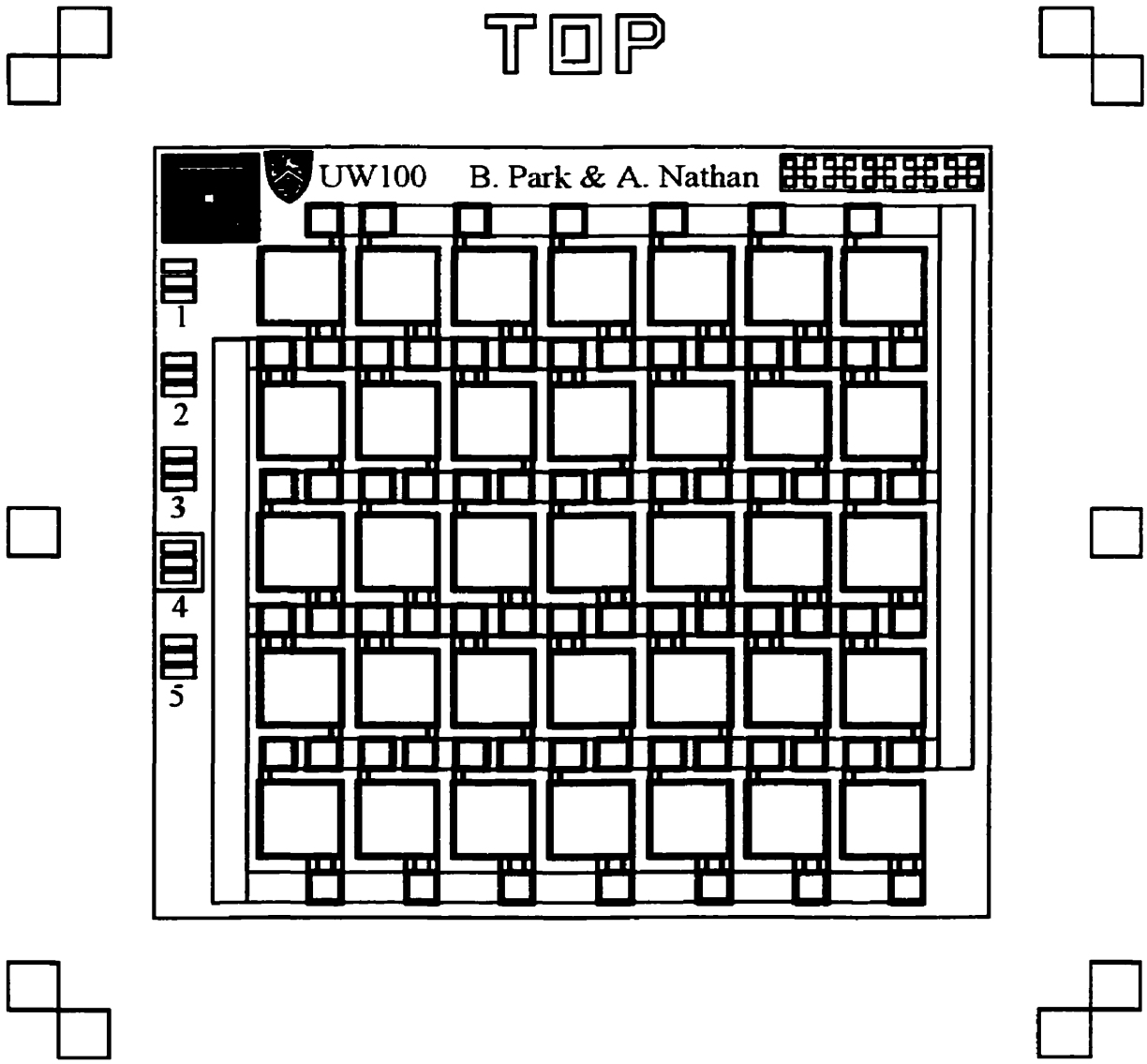


Figure A.4: 35 Schottky diodes connected in parallel. This design was used to measure the leakage current of the diode fabricated with the old process sequence. All diodes are 200μm x 200μm. The fabrication sequence of this diode process is illustrated in Fig. 3.3. The old process is only 4 mask process. An extra step was added here for the final metallization (Al) for easier wire bonding.

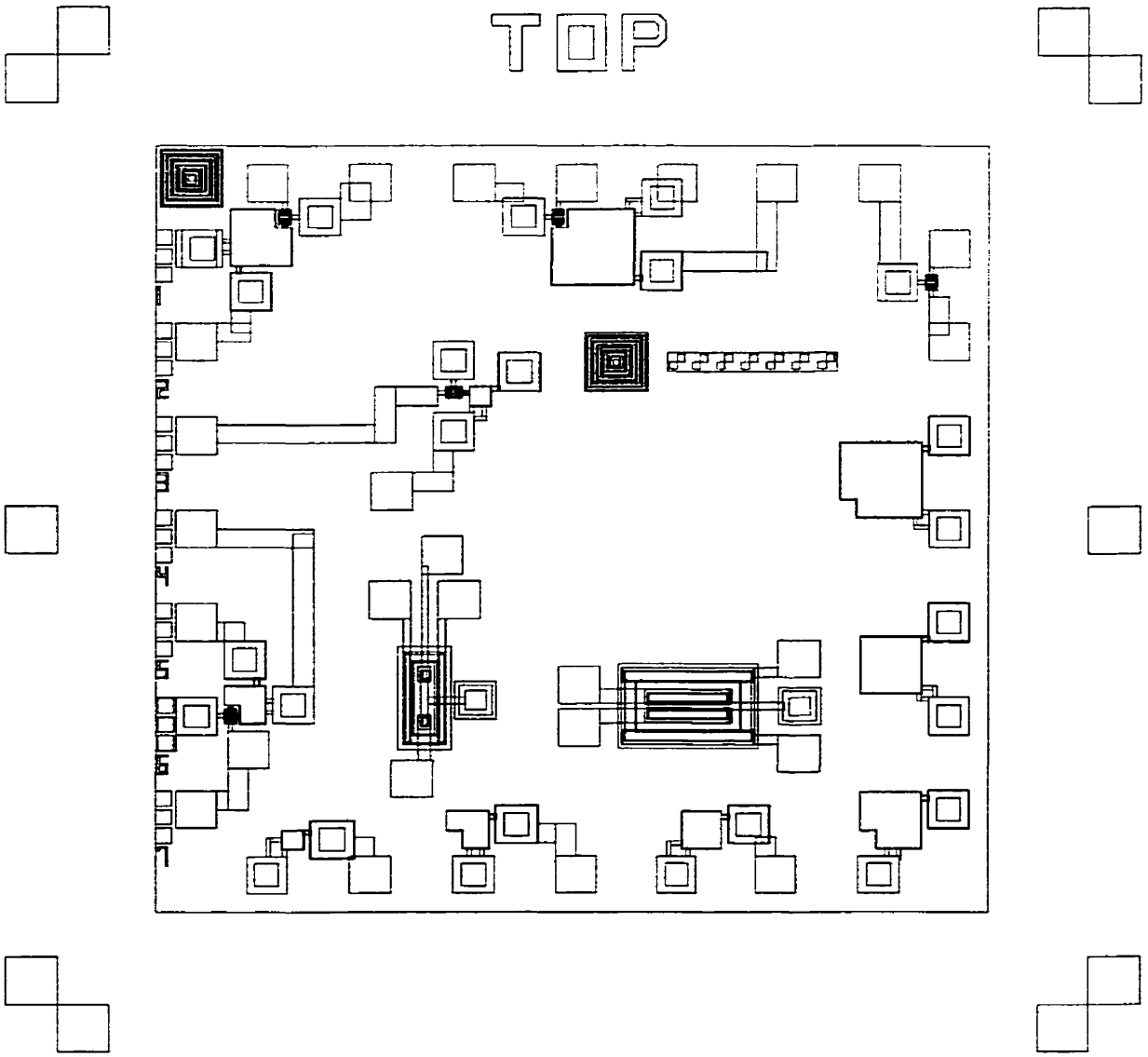


Figure A.5: Non-overlapping pixel designs studied in Chapter 4. The dimensions of the diode are varied from 200μm x 200μm to 50μm x 50μm while the TFT is kept at W: 20μm, L: 10μm.

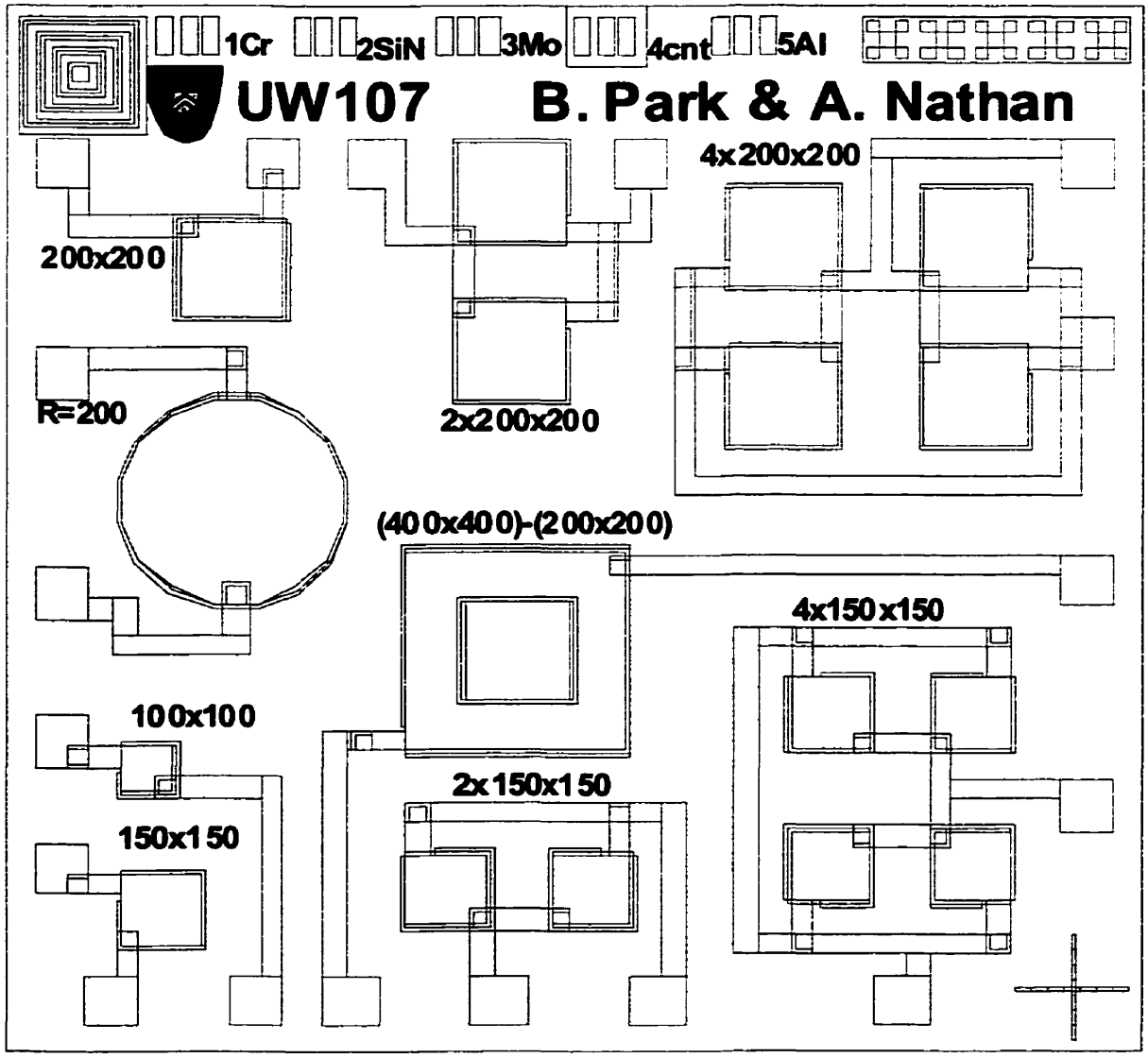


Figure A.6: Stacked pixel designs studied in Chapter 4. The dimensions of the diode are kept at 200μm x 200μm. while the TFT is varied - W: 200μm/L: 20μm, W: 90μm/L: 90μm, and W: 10μm/L: 100μm.

Appendix B

Thermal Stress of Thin Films

As mentioned in section 5.2.3, the thermal stress is caused by a mismatch of the thermal expansion coefficients of the film and the substrate. Table B.1 lists the thermal stress of some films that are deposited at University of Waterloo laboratory.

Film material	Modulus of Elasticity, Y (N/m^2)	Poisson's ratio, ν	Thermal expansion coeff., α ($°K^{-1}$)	Deposition temperature (°C)	Thermal stress from Eq. 5.19, $\sigma_{thermal}$ (Pa)
Mo	32.3×10^9	0.32	5×10^{-6}	30	0
a-SiN_x	210×10^9	0.13	2.8×10^{-6}	260	-3.93×10^7
i-a-Si:H	134×10^9	0.2	2.5×10^{-6}	260	-4.85×10^7
Corning 7059 glass	67.6×10^9	0.28	5×10^{-6}	N/A	N/A

Table B.1: Calculated value of thermal stress of thin films on Corning 7059 glass substrates. "–" sign denotes compressive stress.

Appendix C

Film Deposition Parameters

	Temp. (°C)	Pressure (mTorr)	Power density (mW/cm^2)	Gas flow (sccm)	Dep. Rate (Å/min)
i-a-Si:H	260	250	4.8	SiH_4: 50	110
n^+ a-Si:H	260	150	4.8	1%PH_3+SiH_4: 10	75
n^+ μc-Si:H	200	1000	40	1%PH_3+SiH_4: 10 H_2: 1000	20
a-SiN_x	260	400	44	50%NH_3+N_2: 160 SiH_4: 4	110

Table C.1: Deposition parameters of PECVD films.

	Sputtering	Temp. (°C)	Pressure (mTorr)	Power (W)	Ar flow (sccm)	Dep. Rate (Å/min)
Al	DC	150	10	400	30	135
Cr	DC	30	5	200	30	110
Mo	RF	30	3,5,10,20	200,300,400	20, 30, 40, 60	80-130

Table C.2: Deposition parameters of PVD films.

Appendix D

Film Etchant and Etch Rate

Film	Etchant	Temp.	Etch rate (Å/min)
i-a-Si:H	300mg KOH + 700ml H_2O or 240mg KOH + 800ml H_2O + 230ml methanol	45°C 30°C	525 ± 75 100 ± 25
n^+ a-Si:H	240mg KOH + 800ml H_2O + 230ml methanol	30°C	250 ± 25
n^+ μc-Si:H	240mg KOH + 800ml H_2O + 230ml methanol	30°C	400 ± 25
a-SiN_x	40ml HF + 800ml NH_4F	30°C	5000 ± 500
Al	456ml H_3PO_4 + 36ml CH_3COOH + 18ml HNO_3 + 90ml H_2O	45°C	1000 ± 150
Cr	120mg $Ce(NH_4)_2(NO_3)_6$ + 100ml CH_3COOH + 500ml H_2O	45°C	240 ± 20
Mo	456ml H_3PO_4 + 36ml CH_3COOH + 18ml HNO_3 + 90ml H_2O	30°C	120 ± 10

Table D.1: Etchant, etching temperature and etch rate of all films.

Appendix E

Issues for Large-Area Array Production (Yield)

The ultimate goal of this project is a successful production of large-area (>2") x-ray imaging array. In order to achieve this, it is highly recommended that some research resources be allocated to improve the fabrication yield. There are many little details to consider at every step of fabrication. In this section, a few major issues are addressed in hope that the next engineers will not have to rediscover these points by trial and error.

A hot wash process is necessary after the wafer is dipped into the metal etchant, KOH solutions, and the photoresist stripper. The metal etchant (456ml H_3PO_4 + 36ml CH_3COOH + 18ml HNO_3 + 90ml H_2O) is very viscous and does not get easily washed away. In the metal deposition system, small traces of carbon molecules were found which could have originated from unwashed metal etchant on wafers.

As the PECVD machine gets older, it is showing signs of aging. One of the signs is patterned white spots on the wafers. These white spots are believed to be a byproduct of the chamber cleaning process. The devices on the wafer with white spots do not work or demonstrate distorted performance. This problem can be avoided by first coating the entire PECVD chamber with a very thin film (20nm) of the first layer to be

deposited on the wafer. Also, the engineers must always try to minimize the time that the vacuum chamber is exposed to air.

Another sign of aging that the PECVD machine exhibits is debris of films left on the top of the wafer after the PECVD deposition. According to the previous student's PhD thesis, in the Schottky diode deposition, immediately after the intrinsic amorphous silicon layer is deposited, the wafer is to be loaded into the PVD chamber for the vacuum pump down. Because of the debris, the wafer must be first dipped into HF solution then washed thoroughly before it is loaded into the PVD chamber. The diodes fabricated without this treatment show extremely high leakage currents.

For making discrete devices, line spacing of the first metal layer can be as small as 10μm. For array fabrication, even a small chance of bridge fault cannot be allowed. The minimum line spacing between the gate lines in an array should be 30μm. The line width is determined by the channel length of the TFTs. In Figs. 6.1 and 6.2, the channel length is 20μm. This should be sufficient width to prevent line breaks caused by voids. For the final metallization (Al), the thickness of the line should be more than 1μm to allow good contact when wire bonding. The width of the final metal should be more than 40μm to ensure a continuous coverage over a sharp step (~2μm in height) profiles.

The silicon layers (both intrinsic and n^+ doped) are etched with KOH solutions. There must be enough space between the pixels so that the KOH etch process can successfully isolate all pixels. The minimum space between pixels is 60μm. This number can be decreased substantially with a dry etch process which can replace the current wet etch process.

Very often, the small contact windows on photoresist for final metallization do not get completely removed by the developer. A very thin layer of photoresist can stop the HF solution from making the opening on the silicon nitride films. For array fabrication, the minimum size of via window should be 20μm x 20μm. The wafers must

be left in the photoresist developer for a long enough period to ensure a successful opening of such small windows.

There are many other small details to pay attention to. Unfortunately, most of them can only be learned by repeated practices. For the engineers who enter the lab for the first time, the yield can be as low as 10%.

Appendix F

Wafer Cleaning Process

Prior to being loaded into vacuum chambers, all wafers must be cleaned. The RCA2 step can be skipped for the glass wafers. While rinsing, it is important that the clean DI water is poured directly into the beaker that contains the cleaning solution with the wafers still left inside. This will lead to an overflow which prevents the particles floating at the top from sticking back onto the wafers.

Step	Solution	Ratio (mL)	Temp. (°C)	Time (min)
RCA1	$NH_4OH:H_2O_2:H_2O$	150:150:750	80°C	15
Rinse	H_2O	N/A	RT	5
RCA2	$HCl:H_2O_2:H_2O$	150:150:750	80°C	15
Rinse	H_2O	N/A	RT	5
Hot wash	H_2O	1000	80°C	15
Drying	IPA vapour	N/A	60 ~ 80C	5

Table F.1: RCA wafer cleaning process [113].

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