High IF Digitizer Based on Quantized Feedback

by

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Abstract

This thesis discusses the issues and solutions of quantized feedback for high IF digitizers in wireless communication systems. The first part of the thesis examines different types of architectures that can be used for IF digitizers. In the second part of the thesis. the quantized feedback and its effect on the distortion is examined and compared with the continuous amplitude feedback method. A new sigma-delta modulator architecture is proposed to improve quantized feedback behavior and a brief theoretical analysis is mentioned. Design problems due to the new architecture are investigated and a 400MHz IF digitizer with low distortion using the new technique is designed. The prototype design achieves a very low distortion and suppresses the loop distortion created by conventional architectures by more than 40dB. The IM3 for this prototype is also reduced by more than 20dB.

Acknowledgements

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Chapter 1

Introduction

A conventional digital radio receiver chain consists of a few band-pass filters with different center frequencies, two or three mixers, a low noise amplifier, a frequency synthesizer and an A/D converter. The recent development of advanced technology for VLSI circuits gives one the opportunity to develop a compact system. However, the external components such as the tank circuits for the LNA , image rejection filters, SAW filters, etc. prevent one from reducing the size of the system considerably.

In order to reduce the size considerably, one should get rid of as many of the external components as possible. The oversampled IF digitizer will reduce the number of external components or relax the required performance of the external components. For example, a band-pass sigma-delta modulator eliminates the quadrature mixers which are required at the input of the A/D converter. This will eliminate the mismatch of the two paths. However, the image rejection filter is still required because the IF input is still at low-frequencies (10MHz). Increasing the IF fre-

quency has two advantages: It relaxes the performance of the image rejection filter and eliminates one of the IF stages.

There are many standards, such as DECT, WCPE, PCS1900, GSM, etc. Some of these standards, such as PCS1900 and GSM, have the same specifications in terms of bandwidth, the modulation scheme, data rate per channel, etc. One of the main differences between them is the carrier frequency. Switching between the two standards in the current approach is not easy because of the presence of two carrier frequencies. The system requires either a frequency synthesizer whose function is to sweep both carriers with the same performance or using two different frequency synthesizers. Usually the latter technique is used to have a multi standard system. To make the system compact and simple motivates us to pursue the idea that developing a high IF digitizer the two carriers can be converted to one IF using only one local frequency. Therefore this relaxes the frequency synthesizer requirements. In addition at high IF frequency the image signal frequency is larger than one decade in the frequency domain. This will also reduce the requirements of the filter.

1.1 Research Objectives

The aim of this research is to develop an IF digitizer whose input frequency can be increased as high as 300-400MHz for GSM or PCS1900 application. The main goal is to develop a technique that can digitize the information with minimum distortion. Since this project is intended for wireless applications, being a low power architecture is another goal of this project. Our goal is to reduce the distortion to

12-bit level with only 25 milliwatts of power dissipation.

1.2 Thesis Organization

In chapter 2, two types of oversampled A/D converters are investigated. In this chapter different architectures of sigma-delta modulators are highlighted. A design procedure for two general architectures, that is, a band-pass sigma-delta modulator and a low-pass sigma-delta modulator, are mentioned and a design example for each architecture has been mentioned. At the end, the two architectures are compared.

In chapter 3, quantized feedback is discussed and a new architecture is proposed to reduce the sampling mixer distortion. Simulation results from MATLAB and the advantages of this architecture are discussed.

In chapter 4, the IF digitizer design will be highlighted. Each block in the new architecture will be examined in terms of the circuit performance.

In chapter 5, the issues concerning IC implementation will be discussed and experimental results along with the testing guidelines will be presented.

Concluding remarks and comments on further investigation of this approach are made in chapter 6.

Chapter 2

IF Digitizer Architectures

2.1 A/D converters in wireless and digital communication

In wireless applications, A/D converters are used in the demodulation scheme. After the RF signal is mixed down to IF, it is further demodulated from IF signal to baseband signal. In digital communication systems, the carrier signal is still analog. The message which is carried on the carrier is digital information. After demodulation, the digital information is restored and processed to get the information contained in the digital signals.

2.1.1 Analog and digital domain demodulation

Traditionally in a receiver chain, upon mixing the input signal from RF frequency to IF frequency, subsequent processing can be performed in one of two ways. One is the

conventional way of performing demodulation directly at IF. Traditionally one can do a FM to AM translation (by differentiation) followed by an AM demodulation. Recently, with the advent of high speed ADCs, one can digitize the signal and perform all the demodulation digitally. This has the advantage of having to build only one IF strip and demodulate different modulation schemes (from different standards) using the same strip. An IF digitizer normally consists of an IF mixer (which operates at lower frequency than the RF mixer) that mixes the incoming IF signal to baseband as well as a baseband ADC that digitizes the subsequent baseband signal. In the case of a bandpass sigma-delta modulator, the digitizing is done directly in IF and a separate analog mixer is not needed. An alternative architecture includes a hybrid solution: e.g. one architecture discussed in this thesis includes a mixer which mixes the IF signal down to baseband, performs a coarse digitization, reconverts the coarse signal back to an analog form, mixes the analog signal back up to IF frequency, and subtracts this feedback signal from the incoming IF frequency. In this case the mixing and sampling functions are distinct from one another.

The different ways of implementing demodulators are now discussed in more detail. One is analog demodulation. It can be illustrated in Fig.2.1.

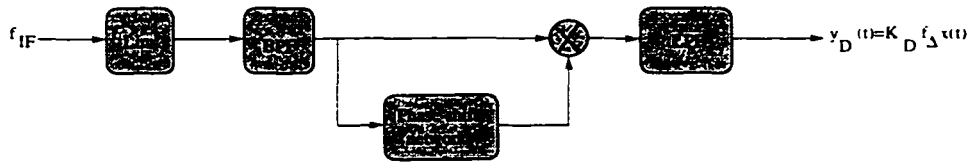


Figure 2.1: Phase-shift discriminator of quadrature detector.

Fig. 2.1 represents a phase-shift discriminator built with a network having

group delay t_1 and carrier delay t_0 such that $\omega_c t_0 = 90°$- which accounts for the name quadrature detector. The phase-shifted signal is proportional to $\cos[\omega_c t - 90° + \phi(t - t_1)] = \sin[\omega_c t + \phi(t - t_1)]$. Multiplication by $\cos[\omega_c t + \phi(t)]$ followed by lowpass filtering yields an output proportional to

$$\sin[\phi(t) - \phi(t - t_1)] \approx \phi(t) - \phi(t - t_1)$$

assuming t_1 is small enough that $|\phi(t) - \phi(t - t_1)| \ll \pi$. Therefore,

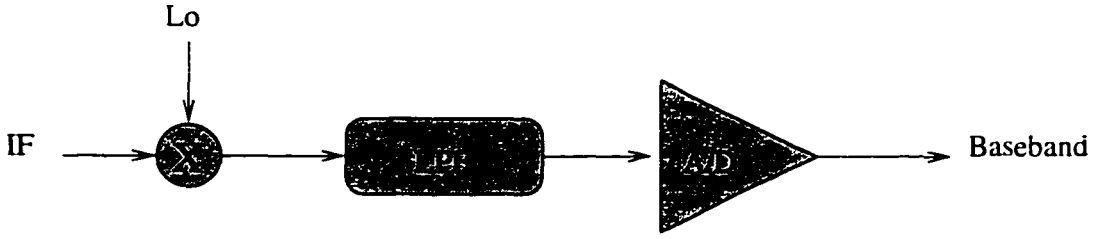
$$y_D(t) \approx K_D f_\Delta x(t)$$

where the detection constant K_D includes t_1. Despite these approximations, a quadrature detector provides better linearity than a balanced discriminator and is often found in high-quality receivers. The IF receiver LMX2240, made by National Semiconductor, is one of the commercial realizations using this approach. This chip consists of a hard limiter at the input with an input impedance of 150 ohms and having a -80 dB sensitivity for the IF signal. A Gilbert-quad mixer is used for the discriminiator in this architecture. To get the quadrature signal an external tank circuit is required whose bandwidth is approximately 1% of the IF frequency and a steep phase response is required. As a result the above approach suffers from

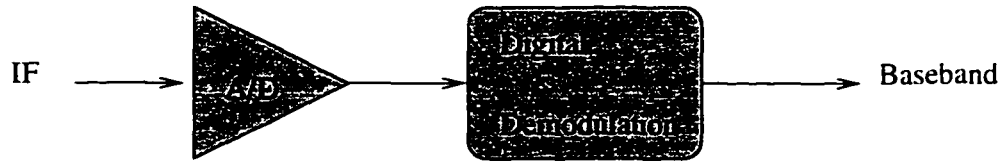
a) Need to have external capacitors and inductors for its tank circuit.

b) Need to have a narrowband analog filter.

To circumvent the above mentioned problems, the approaches shown in Fig. 2.2 can be used.



(a) Baseband A/D demodulation



(b) Pass band A/D demodulation(bandpass conversion)

Figure 2.2: Analog and digital domain demodulation

In Fig. 2.2a, the incoming IF signal is multiplied by the LO signal which is of the same frequency and phase as the carrier signal. After the multiplication, a low pass filter is used to eliminate the frequency component at $(\omega 1 + \omega 2)$. Only the baseband signal is left upon low-pass filtering. A baseband analog-to-digital (A/D) converter is then used to convert the analog signal to its digital form and the baseband digital circuits will perform the demodulation. This approach is given the name "baseband demodulation". An alternative denoted as bandpass demodulation is shown in Fig. 2.2b. This has become possible only after high speed, high accuracy A/D converters became available recently. The IF signal is fed directly into the A/D converter. The A/D digitizes the IF signal directly into its digital form. Then the demodulation is done entirely in the digital domain in the passband.

There are two terms which can easily raise confusion here: digital demodulation and digital domain demodulation. Digital demodulation is named after those methods like PSK, FSK because in these demodulators, the information is in the digital domain, while the demodulation can be done in the analog domain. Digital domain demodulation means the signal representation in the demodulator is in digital form and the information is also in digital form.

Why did digital domain demodulation come into being? This is mainly because of the more and more powerful digital signal processing techniques. The speed and function of DSP has developed quickly and now it is easy for DSP to handle signals with frequency in the order of several hundred MHz. Also digital processing, like filtering, multiplication, is less prone to error than their analog counterparts. The major challenge is that there is an accurate and fast enough A/D converter to convert the IF signal into its digital form. Consequently the design of a high accuracy, high speed A/D converter is a key issue in digital radio.

2.1.2 IF digitization

In digital radio applications [2], the IF signal typically has a center frequency of 10-100 MHz, with bandwidth varying from a few kHz to more than 1 MHz. The A/D converter used in this application needs to handle signals at these frequencies and with these bandwidths, while maintaining of resolution around 70 dB. First, let us take a look at the different A/D converter architectures to see which one is promising for IF digitization.

There are two general ways of doing data conversion at IF: wideband and nar-

rowband conversion. Oversampling A/D converters such as sigma-delta converters fall in the narrowband category. Wideband converters will include architectures such as pipelined and flash converters. Fig.2.3 summarizes the speed and resolution of different A/D converters.

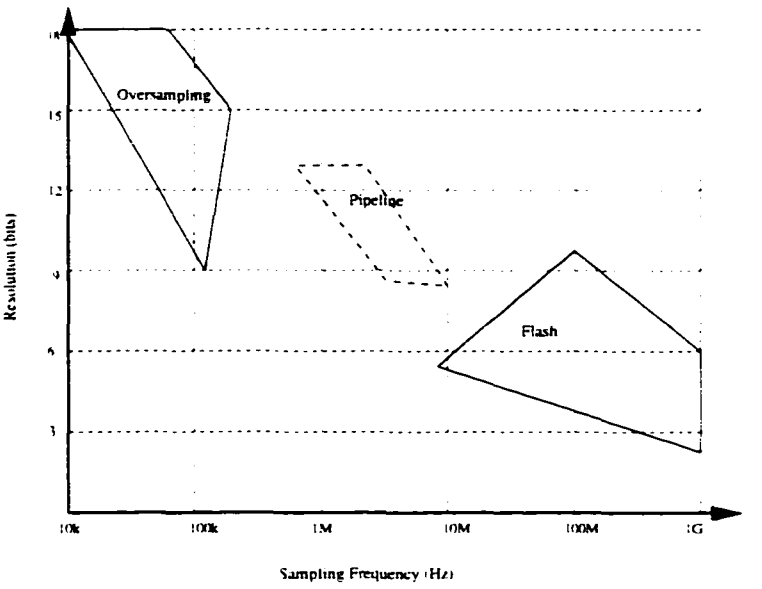


Figure 2.3: Resolution vs. sampling rate for A/D

In wireless communication, there is also a stringent power requirement for A/D converters. Fig.2.4 is the comparison of power consumption in various A/D converters.

In Fig.2.3, we can see that flash A/D converters have the highest speed but the lowest resolution. The oversampling A/D converters have the highest resolution but the lowest sampling rate. Between them are pipelined A/D converters which offer a trade-off between speed and resolution. As shown in Fig.2.4, the flash A/D converters have the highest power consumption. Because there are very few

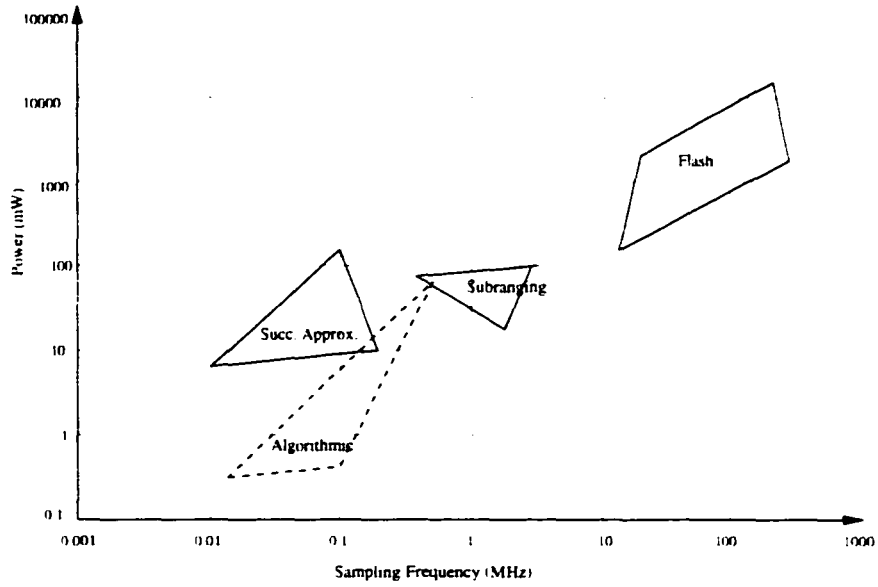


Figure 2.4: Power versus sampling rate for an 8-bit A/D converter implemented in different architecture

oversampling and pipelined A/D converters operating at an 8-bit resolution. they are not presented in this figure. In general oversampling A/D converters have the same order of power consumption as the algorithmic ones and pipelined A/D converters have similar power consumption as subranging A/D converters.

Typically for wide signal bandwidth (such as DECT. CDMA. or wireless video) applications. Nyquist rate ADCs are used. On the other hand. for narrow signal bandwidth applications (such as AMPS. GSM) oversampled architectures will be used. As mentioned above since the power is one of the most important issues in wireless applications. so architectures which dissipate high power are avoided. With this in mind three types of architectures are usually used. For wide signal bandwidth applications pipelined architecture is selected. because its power dissipation is the lowest among high speed Nyquist rate A/D converters (e.g. Flash

type A/D converters and subranging type A/D converters). Note interpolative and folding A/D converters are becoming a big contender in this area. For narrow signal bandwidth applications, two types of sigma-delta modulators are considered: low-pass architecture and band-pass architecture. In this chapter, the important parameters which have to be selected for each architecture in narrow signal bandwidth architectures is explained and a design procedure will be presented to obtain the required parameters for designing an A/D converter for IF applications.

2.2 Sample/Hold Circuit and Sampling Mixer

Even though band-pass sigma-delta modulators do not explicitly need a mixer (its mixer and S/H circuit is merged), it still needs a S/H circuit. As a side note, the other architectures (pipelined, low-pass sigma-delta modulator) can also use a sampling type mixer and then merge it with its sample and hold circuit. Of course they can also have a continuous time mixer in front (like a Gilbert mixer). This section will discuss the S/H circuits and briefly exhibits its difference from the sampling mixer. (Note the S/H circuit is very different from other types of mixer).

Nyquist rate A/D converters and the oversampled architecture both require sample and hold circuits. The location of the S/H depends on the type of architecture employed. If the architecture processes signals in the continuous time domain, the S/H is used at the input to the comparator, whereas, if the signal is processed in discrete time we need a S/H at the input.

In IF digitizers, since the sampling clock frequency is equal to or less than that of the input frequency, the sample and hold is used as the sampling mixer. There

are two types of sampling mixers which are shown in Fig. 2.5. Both of these structures create distortion at the output and degrade the signal quality.

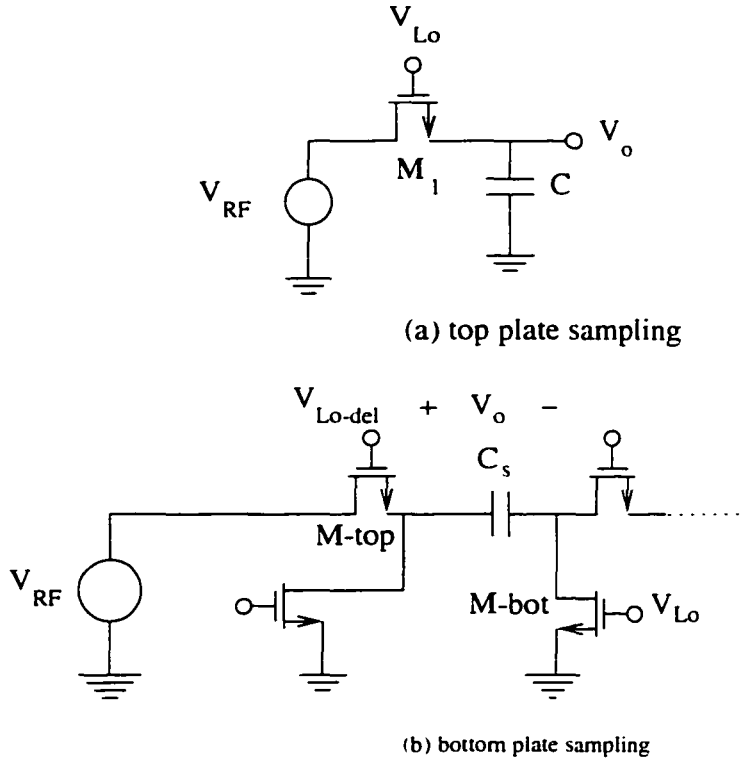


Figure 2.5: Sampling mixer a) top sampling b) bottom sampling

The distortion of this type of mixer has been characterized in [3,4]. Three types of distortion are defined for this type of mixer. The first type is the time invariant distortion, produced by circuit characteristics of the mixer switch. An NMOS transistor can be characterized as a nonlinear resistor when the gate is connected to high voltage. The equivalent circuit for a top sampling mixer is shown in Fig. 2.6. It can easily be shown that the time invariant distortion linearly depends on the frequency as well as the sampling capacitor and is inversely proportional to the size of the switch [3,4].

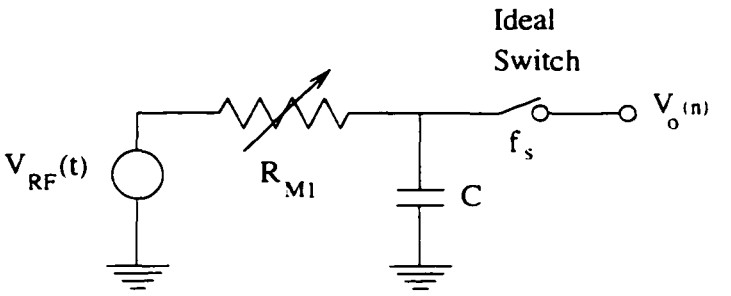


Figure 2.6: Equivalent circuit for top sampling mixer

The second type of distortion is called non uniform distortion. This type of distortion is due to the fall time of the clock edge and the input voltage. Analytical solution shows that the distortion depends on the input frequency and the clock edge fall time in a quadratic fashion.

The third type of distortion is due to the change of the device characteristic during the fall time of the sampling clock. The device characteristic changes with time so the time varying charcteristic creates distortion. In general, calculating this type of distortion is difficult. But in this case the sampling time is important and the distortion is dependent only on the value of the sample instant. Analytical results show that the distortion depends on the cube of the input frequency [5].

The above discussion shows that the sampling mixer distortion changes with input frequency. At low frequency the time invariant distortion dominates. However, at high frequency the other two types dominate. Fig. 2.7 shows a comparison of analytical results of the three type distortion and gives a quick estimation of the dominant distortion sources at different frequencies. It shows that at high enough frequencies the time varying distortion, which increases as the cube of input frequency, dominates. It also gives the motivation that a new architecture, like the

one discussed in this thesis, is needed to achieve acceptable levels of distortion as the IF moves higher.

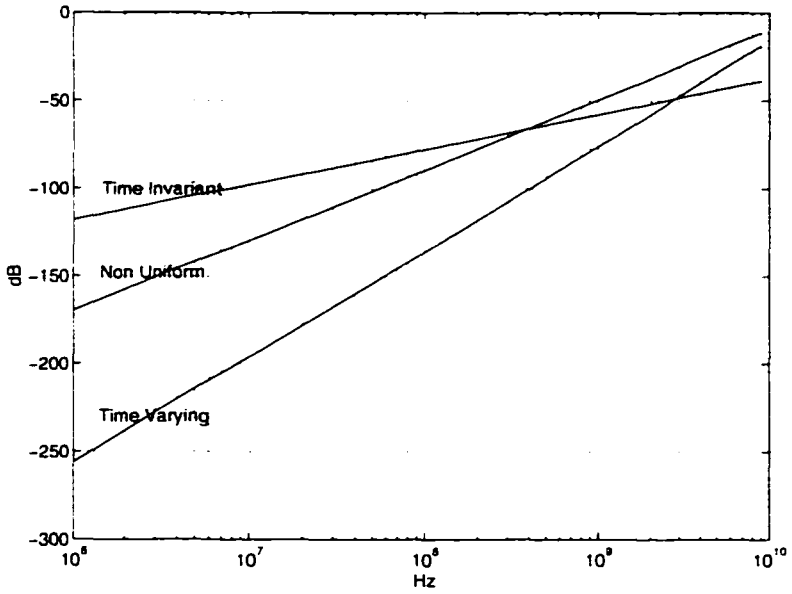


Figure 2.7: Distortion graph regarding the analytical approach

2.3 Low-pass sigma-delta modulator

In this section, a review of the low-pass sigma-delta modulator is presented. This type of A/D converter has been used by industries and researchers because they have fewer problems than the conventional architecture used for A/D converters and D/A converters. This type of architecture is usually used for high resolution requirements and narrowband signals. In IF digitizers, the input frequency is large, but the band of interest compared to the sampling clock frequency is narrow. So this type of architecture can be used to digitize the information directly at IF. Different types of low-pass sigma-delta modulator architectures will be discussed in

this section. Then non idealities that produce degradation of the performance of each architecture will be explained. At the end of this section, a design guide with an example will be explained.

2.3.1 Hardware architectures

Sigma-delta modulators can be categorized into different categories depending on the number of output bits, the number of stages, or the number of loops. These architectures are denoted as: first order, second order, higher order, multi stage, and interpolative architectures. Any of these architectures can be one-bit or multi-bit or both. Each of these categories will be explained below.

2.3.1.1 Single stage architectures

Single stage architectures consist of only one quantizer. The noise shaping is done by a single or multi-loop consisting of one or more integrators as loop filter in the loop. One of the important issues in sigma-delta is the quantization noise. In the following sections in each architecture the quantization noise will be discussed and an estimation of SNR will be given.

2.3.1.1.1 First order architecture A first order architecture is shown in Fig. 2.8. This architecture consists of an integrator and a quantizer. Since the integrator has infinite gain at DC, the loop gain is infinite at DC and therefore the DC component or the average of the output from the feedback D/A converter will be identical to the DC component of the input signal. This means that even though the quantization error at every sample is large because of the use of two level quantizer,

the average of the quantized signal, and therefore the modulator output y_k, tracks the analog signal $x(t)$. This average is computed by a decimation filter that follows the modulator.

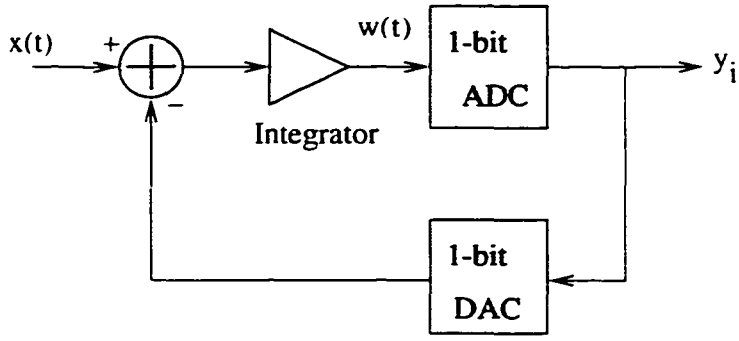


Figure 2.8: First order architecture

In general, the amplitude resolution of the modulator increases when more samples are included in the averaging process, or as the oversampling ratio (OSR) increases. However, the bandwidth is decreased at the same time when the sampling frequency is kept constant. Consequently, the resolution of the modulator is a function of the ratio of the sampling rate to the bandwidth of the modulator. The principle of operation of sigma-delta modulators relies on this fundamental trade-off between resolution and time.

Compared to the Nyquist rate A/D converters, the quantization error is a differential error. In the other words, the modulator tries to cancel the error by subtracting quantization error from two adjacent samples. This principle of reducing the error source by exploiting the statistics between them can be extended to higher order modulators, where more past error samples are involved in the cancelation process to reduce the overall error. Viewed from the frequency domain this

difference operation acts to attenuate the quantization noise at low frequencies. thus shaping the noise. The first order modulator can be proved to be inherently stable. provided that the input is within $[V_r, -V_r]$. where V_r is the output of the feedback D/A converter. or the reference voltage.

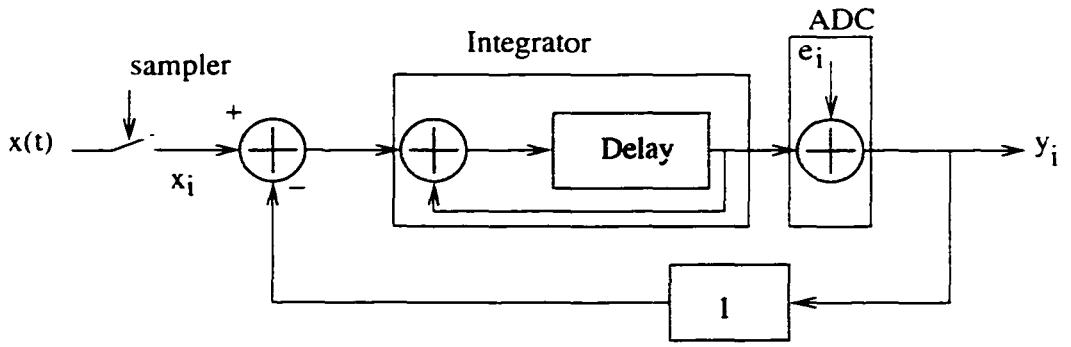


Figure 2.9: Model of first order architecture

Quantization noise in this architecture depends on the input signal. For busy signals the quantization noise is like white noise whereas for dc input the quantization noise is colored. To calculate the effective resolution of the $\Delta\Sigma$ modulator. it is assumed that the input signal is sufficiently busy that the error e behaves like a white noise which is uncorrelated with the input signal. The modulation noise is expressed as:

$$n_i = e_i - e_{i-1} \tag{2.1}$$

and the spectral density may be expressed as:

$$N(f) = E(f)(1 - e^{(-j\omega T)}) \tag{2.2}$$

The noise power density is described as:

$$|N(f)| = 2e_{rms}\sqrt{2T}\sin\left(\frac{\omega T}{2}\right) \tag{2.3}$$

where $\omega = 2\pi f$.

Clearly, feedback around the quantizer reduces the noise at low frequencies but increases it at high frequencies. The total noise power in the signal band is

$$n_0^2 = \int_0^{f_0} |N(f)|^2 df \approx e_{rms}^2 \frac{\pi^2}{3}(2f_0T)^3 \qquad f_s^2 \gg f_0^2 \tag{2.4}$$

where $2f_0T$ is defined as the inverse of the OSR, so its rms value is approximately $e_{rms}\frac{\pi}{\sqrt{3}}(OSR)^{-3/2}$. Each doubling of the OSR of this circuit reduces the noise by 9 dB and provides 1.5 bits of extra resolution. The improvement in the resolution requires that the modulated signal be decimated to the Nyquist rate with a sharply selective digital filter. Otherwise, the high-frequency components of the noise will spoil the resolution when it is sampled at the Nyquist rate.

2.3.1.1.2 Higher-order architecture The procedure for increasing the resolution with feedback can be reiterated by replacing the internal quantizer of a first-order modulator as shown in Fig. 2.10 by an identical first order modulator. The resulting circuit is shown in Fig.2.10 [6]. As before the integrators may or may not contain delays. Usually one does and the other does not. The gains k_1, k_2 are used to optimize the output signal range of the integrators. Modulators with a second-order transfer function involve the cancelation of the two past samples and thus exhibit stronger attenuation at low frequencies. The noise shaping function of

a first and second-order modulator are compared in Fig. 2.11 [7]

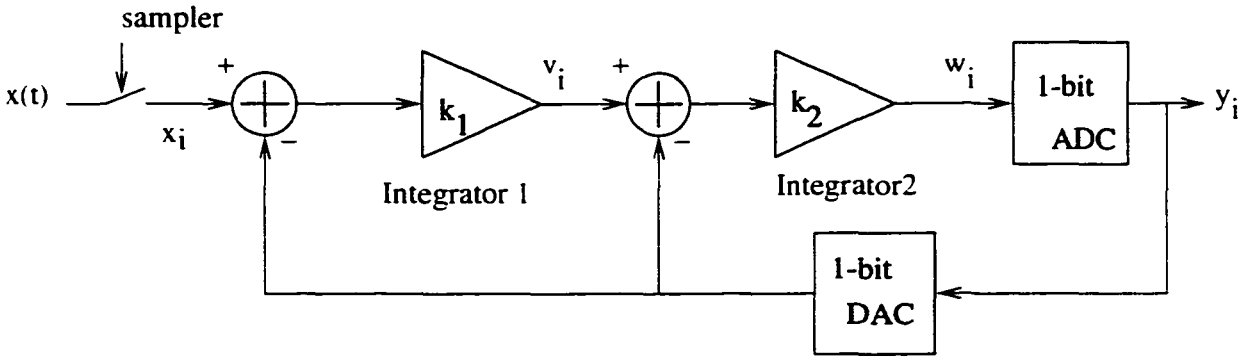


Figure 2.10: Modified architecture of second-order modulator

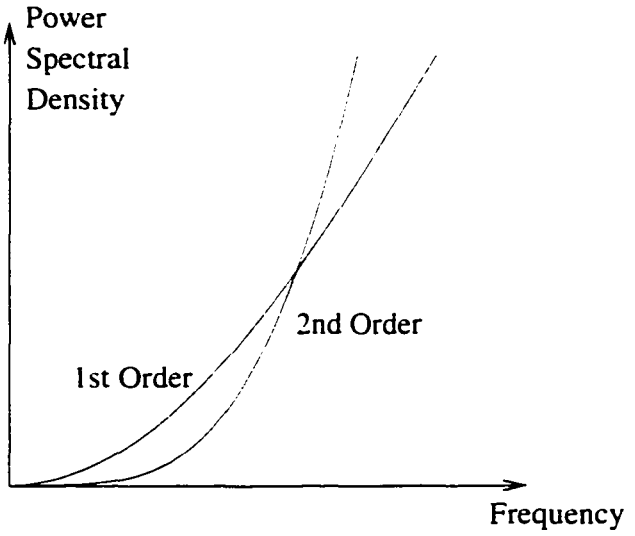


Figure 2.11: Power spectral density for first and second order sigma-delta modulators.

A second-order modulator can be shown to be conditionally stable. The stability depends on total delay in feedback loop, signal amplitude and coefficients k_1, k_2. To avoid saturation, the maximum signal levels at the amplifier outputs should be adjusted by scaling.

The above analysis can be formalized to yield quantitative results for the resolution of sigma-delta modulators, provided that the spectral distribution of the quantization error e_i can be assumed to be uncorrelated [8]. The modulator can be regarded as linear system for which the power spectral density of the noise can be calculated [9].

For a busy signal the system is assumed linear. So the output of the modulator can be expressed as

$$y_i = x_{i-1} + (e_i - 2e_{i-1} + e_{i-2}) \tag{2.5}$$

so that the modulation noise is now the second difference of the quantization error. The spectral density of this noise is

$$N(f) = E(f)\,(1 - \exp(-j\omega T))^2 \tag{2.6}$$

For busy signals

$$|N(f)| = 4e_{rms}\sqrt{2T}\sin^2\left(\frac{\omega T}{2}\right) \tag{2.7}$$

and the rms noise in the signal band is given by

$$n_0 \approx e_{rms}\frac{\pi^2}{\sqrt{5}}(2f_0T)^{5/2} = e_{rms}\frac{\pi^2}{\sqrt{5}}OSR^{-5/2} \qquad f_s^2 \gg f_0^2 \tag{2.8}$$

This noise falls by 15 dB for every doubling of the sampling frequency, providing extra bits of resolution [7.10].

In general, the dynamic range (DR) of an ADC is defined as the ratio of the output power for a full scale sinusoidal input to the output signal power for a small

input whose SNR is unity (0 dB). Extending the above analysis to the second-order sigma-delta modulator yields the following formula for DR [11]

$$DR = \frac{3}{2}\frac{5}{\pi^4}(OSR)^5 \tag{2.9}$$

The white noise technique can be extended to provide higher order predictions by adding more feedback loops to the circuit [7]. In general, when a modulator has L loops and is not overloaded, it can be shown that the spectral density of the modulation noise is

$$|N_L(f)| = e_{rms}\sqrt{2T}\left[2\sin\left(\frac{\omega T}{2}\right)\right]^L \tag{2.10}$$

For oversampling ratios greater than 2, the rms noise in the signal band is given approximately by

$$n_0 = e_{rms}\frac{\pi^L}{\sqrt{2L+1}}(2f_0T)^{L+1/2} \tag{2.11}$$

This noise falls 3(2L+1) dB for every doubling of the sampling rate, providing $(L + \frac{1}{2})$ extra bits of resolution, but we shall see that there are difficulties in implementing circuits containing more than two integrators.

The oscillation of the signal uses up some of the dynamic range of the circuit, and for a non overloaded quantizer the input amplitude to the modulator needs to be limited. Fig. 2.12 shows the range of inputs that can be accommodated in several modulators, each employing six-level quantization. Ordinary PCM requires that its input be restricted to $\pm A$ in order that the quantization error lie in the range $\pm\Delta/2$, where Δ is the output bin. Inputs to a corresponding first-order $\Delta\Sigma$ modulator

need be restricted to $\pm B$ for them to be interpolated by oscillation between two levels. Inputs to a second-order modulator need be restricted to $\pm C$ to prevent frequent overloading of its quantizer. This permits the output to oscillate between three levels, but overload can occur occasionally when the oscillation attempts to step outside this three-level range.

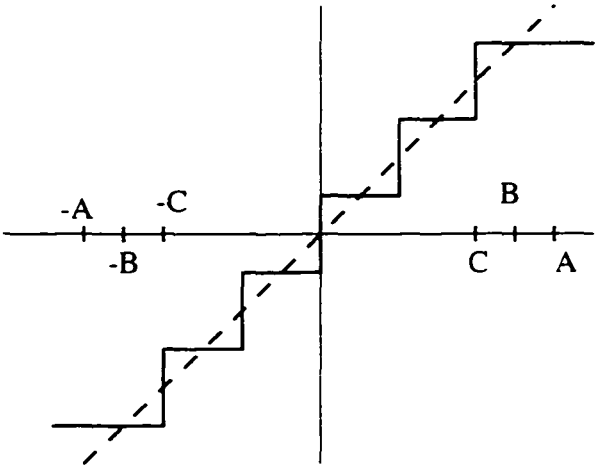


Figure 2.12: Range of amplitudes that can be accommodated by multilevel quantizer

Simple linear theory predicts that the third-order modulator shown in Fig.2.13 has an rms noise given by Eq. (2.11) with $L = 3$. This can be realized in practice with a multilevel quantizer that does not overload [7]: but the circuit is much more sensitive to circuit values than the first and second-order ones. For example, the equivalent linear circuit of this modulator becomes unstable with quantizer gains G in excess of 1.15 compared with 2.0 and 1.33 for first and second-order modulators.

More seriously, the third-order circuit is also unstable when its quantizer gain falls below 0.3. When the quantizer saturates, its effective gain falls, and this usually results in instability in which the circuit settles into a large-amplitude low-frequency

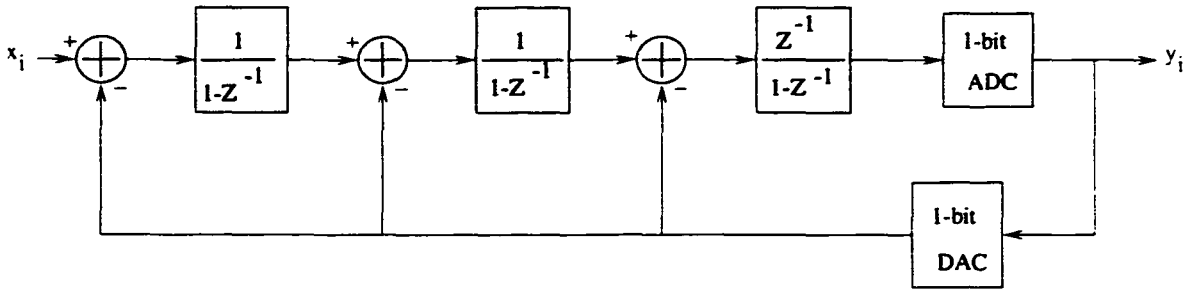


Figure 2.13: Third order sigma-delta modulator

limit cycle. In this state the clipped signals fed back via the two inner feedback paths are small compared with the signal emerging from the integrators. Properties of the outer loop dominate: it contains three integrators and a delay, a strong basis for instability. Unembellished, two-level, third-order $\Delta\Sigma$ modulators cannot escape from this condition. Their circuits can be made stable by clipping the outputs of the integrators or including other nonlinearities that make the inner feedback effective when the quantizer saturates. The noise performance of these modified modulators is considerably worse than Eq.(2.10) predicts. Better performance is obtained by redesigning the filter used in the feedback loop.

The above summarizes the basics of sigma-delta modulators. Below is a list of other alternative architectures:

- Interpolative architecture [12]
- MASH architecture [13]
- Local feedback loop [14, 15]
- Passive Structure [16, 17]

Next we discuss the implementation issues.

2.3.2 Design issues of low-pass sigma-delta Modulator

In real life implementations there are non idealities (such as finite operational amplifier gain, operational amplifier settling time, clock jitter) which appear in the chips and which affect the chip performance. In this section, non ideal issues and their effects will be highlighted.

2.3.2.1 Extra gain in Feed forward path

Our discussion has so far assumed unity gain in every component of the modulator. Fig. 2.14 shows a modulator that includes a constant gain G in the forward path.

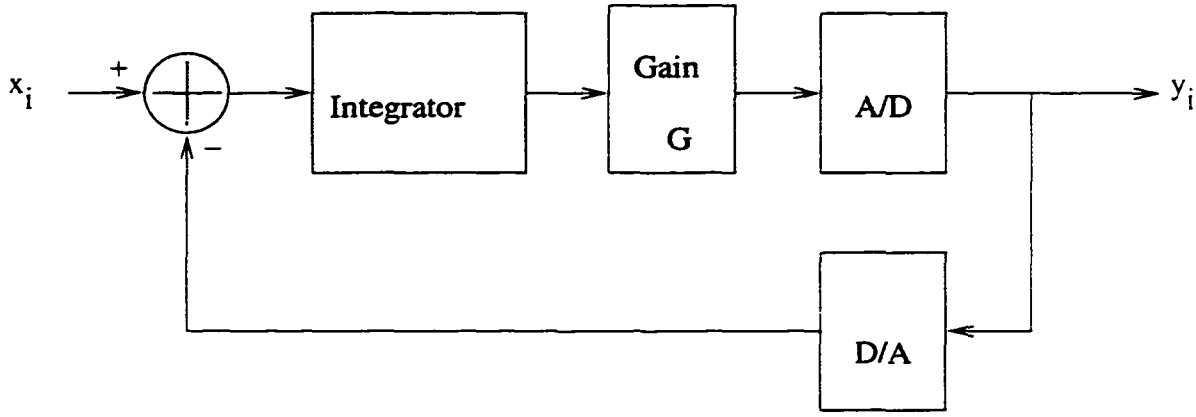


Figure 2.14: Block diagram of a $\Delta\Sigma$ modulator including a gain G in the forward path

In a first order modulator small deviations of this from unity have little effect on the overall properties, provided the net gain in the feedback loop is large. In higher order modulators the extra gain may create instability. The gain of the

accumulator is

$$H(f) = \frac{z^{-1}}{1 - z^{-1}} \approx (j\omega T)^{-1} = [j\pi(2fT)]^{-1} \qquad fT \ll 1 \qquad (2.12)$$

where $z = \exp(j\omega T)$. In the signal band this gain has a modulus greater than one quarter of the OSR.. which is usually sufficiently large. Measurements on real modulators and simulation [7. 18. 19] have demonstrated that with small gains (i.e. $G < 0.7$). the circuit responds sluggishly to changing inputs. With gains greater than 1.3. the quantized signal bounces by more than two levels and eventually goes unstable when the gain exceeds 2. as can be predicted from the linearized model of Fig. 2.8. For most applications 10% gain accuracy is tolerable for this circuit. For higher orders the condition for instability changes. For example. for the second order modulator the maximum gain is 1.3 and for third order this gain reduces to 1.15.

2.3.2.2 Non ideal integrator

In switched-capacitor circuits. an integrator consists of an opamp. two capacitors and some switches. The integrating function is affected by operational amplifier dc gain. bandwidth. settling time and the switch non idealities. In this section. these issues will be addressed.

2.3.2.2.1 Leakage in the integrators First-order modulators need integrators with dc gain H_0 that is greater than the OSR. in order to have low noise. Calculations of noise in second-order modulators indicate that somewhat lower gains

could be tolerated because the gains of two integrator amplifiers are cascaded in the outer loop. But there is another consideration: leakage can permit the oscillation of the quantized signal to settle into regular patterns when there is insufficient long-term memory to randomize it. This is most noticeable at the center of the range where the output can settle into a +1, -1, +1, -1 pattern. The effect is illustrated by Fig. 2.15, which shows the filtered output of a modulator responding to a very slowly changing ramp. The full range of the output signal is ±1V. At the center of the range the output locks into the pattern and the input is ignored in the range ±0.2mV. It may be shown that the width of the dead zone is given approximately by $1.5\Delta H_0^{-2}$, and for this to be less than twice the rms noise requires that the dc gain of each integrator satisfy

$$H_0 \geq (2f_0T)^{-5/4} \tag{2.13}$$

The dead zone is seldom noticeable because it is present only in very slowly changing signals: It takes time for the oscillations to settle into a pattern. For a single-ended configuration of an integrator in a switched-capacitor circuit, the integrator transfer function with finite operational amplifier gain can be expressed as(Fig. 2.16)

$$H(z) = \frac{(C_1/C_2)z^{-1/2}(1 - 1/A - C_1/(AC_2))}{1 - (1 - C_1/(AC_2))z^{-1}} \tag{2.14}$$

2.3.2.2.2 Integrator settling time Incomplete settling of the integrator outputs due to the finite bandwidth of operational amplifiers translates into an equivalent gain error as long as the settling process is linear. As an example, consider an

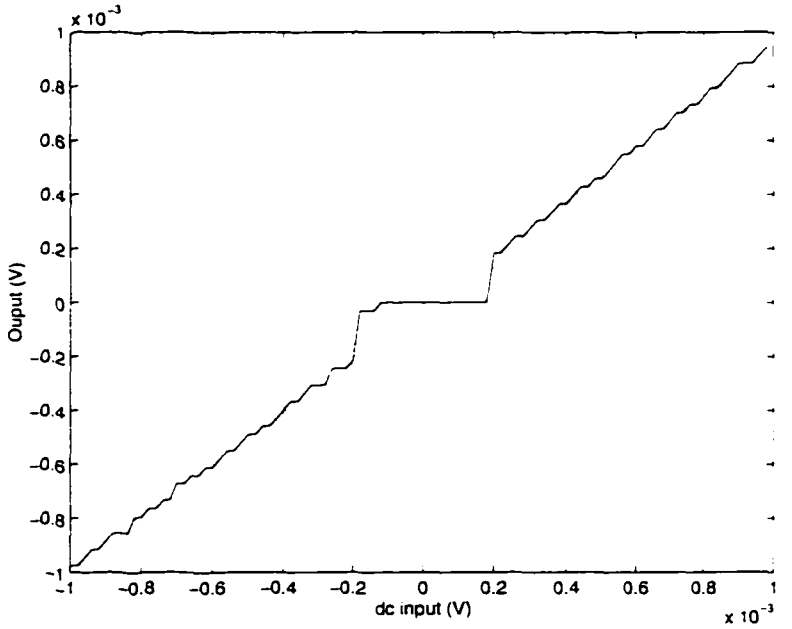


Figure 2.15: Illustration of dead zone caused by leakage in the accumulators of second-order $\Delta\Sigma$ quantization. The dc gain of each accumulator is 64, and the oversampling ratio is also 64. The range of input and output amplitudes that can be accommodated is ± 1V.

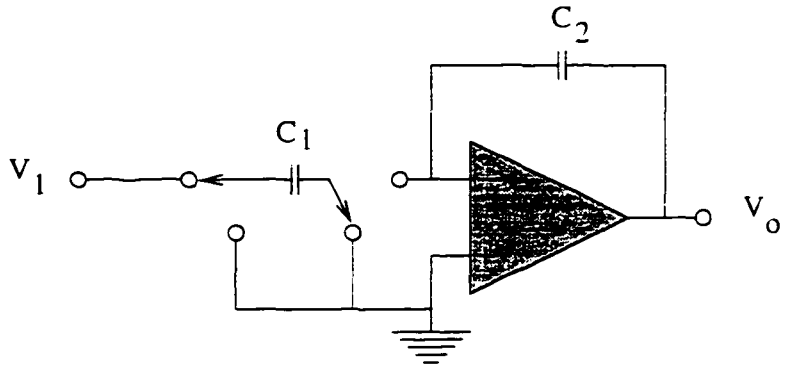


Figure 2.16: Single-ended switched capacitor integrator

integrator whose transient response during each sampling period is characterized

by a single-pole exponential:

$$\Delta V_{out} = V_{in}(1 - e^{-T/\tau}) \tag{2.15}$$

where T is the sampling period and τ is the settling time constant. For a constant sampling period, the term in parentheses represents a constant reduction in the gain of the integrator. A settling time as short as $\frac{T}{4}$ reduces the equivalent gain of the integrator by less than 2%. Slew rate limiting in the response of the integrator causes a departure from the linear settling characterized by Eq.(2.15) and must be avoided.

The maximum speed at which the integrator can be clocked is of particular interest in the design of $\Delta\Sigma$ modulators, because of their oversampled nature and because of the dramatic reduction of in-band quantization noise achieved with increased OSRs. Switched-capacitor circuits operate on the assumption that the complete settling occurs during each time slot. Therefore, unless the signal is used as a continuous-time signal, the manner in which the circuit settles is unimportant. Since the output of an A/D converter is digital, the only place the continuous-time properties of the signal are important is at the sampler input. The only time the value of the voltages at the integrator outputs matters is at the end of each time slot.

The circuit has to settle completely in one time slot. In a two phase clocking scheme, the length of a time slot is equal to one-half of a clock period minus the delays put in for nonoverlap and charge injection reduction purposes. There are basically two factors that determine the settling time of the integrator: the

RC time constants of the MOSFET switches in series with the switched capacitors and the response time of the operational amplifier. The response time of the operational amplifier is determined by the slew rate, the unity-gain bandwidth, and configuration in which it is placed. A very important distinction needs to be made between settling that is signal independent (linear settling) and settling that is signal dependent (nonlinear settling). Nonlinear settling may be due to operational-amp slewing, or the fact that the characteristics of the MOSFET devices will be operating-point dependent. If the integrator does not settle fully but the settling process is linear, then the resultant error shows up as a gain error in the integrator. If, however, the settling process is nonlinear, the resultant error will show up as distortion . Of the two factors, nonlinear settling is by far the more serious problem. A linear settling error has very little effect on the performance of a single-loop modulator, and a linear settling to within 0.1% is more than adequate for most cascaded modulators. A nonlinear settling error, on the other hand, will degrade the performance of both single-loop and cascaded modulators. If the input capacitor of the modulator does not charge completely and the degree of charging is signal dependent, then the effect is the same as if the input capacitor were nonlinear. The error will show up as harmonic distortion and is not affected by the oversampling ratio.

The most straightforward solution for eliminating the effects of nonlinear settling is to make sure the circuit settles completely enough so that no matter what the signal dependence may be, the dynamic range requirements are still satisfied. For example, if the circuit settles to within 0.001% of final value, then a 100-dB dynamic

range is guaranteed regardless of the nature of the settling. Settling problems due to the RC time constant of the MOS switch and the switched capacitor can usually be solved simply by increasing the width of the switch. the limitation being that as the switch becomes larger in comparison to the switched capacitor. the effects due to channel charge injection and the parasitic junction capacitances also increase. The settling of the opamp is a bit more involved since it depends on several factors: slew rate. unity-gain bandwidth. and gain configuration.

To summarize the above discussion for the integrator shown in Fig. 2.16. the integrator transfer function will differ from the ideal because of nonzero switch resistance. and finite opamp bandwidth. With finite opamp bandwidth B (in hertz) the transfer function can be written as

$$H(z) = \frac{(C_1/C_2)z^{-1/2}[(1-\epsilon) + z^{-1}\epsilon C_2/(C_1+C_2)]}{1-z^{-1}} \tag{2.16}$$

where

$$\epsilon = e^{-\pi B T_s}. \tag{2.17}$$

where T_S is the sampling period. For nonzero switch resistance R_{on}. the transfer function is written as

$$H(z) = \frac{(C_1/C_2)z^{-1/2}(1-2e^{-T_s/4R_{on}C_1})}{1-z^{-1}} \tag{2.18}$$

When all of the non idealities are considered together. i.e. the finite gain. the finite bandwidth. and the non ideal switches. they will interact with each other. For a complete analysis see [20].

2.3.2.3 Comparator Requirement

In switched-capacitor circuits the comparator specification is not as important as that of the integrators.If there is any offset, the gain of the integrator will transfer the offset to the input. On the other hand, in the continuous time circuits, the output of the comparator is latched on every clock pulse, and the latched comparator decision is used to apply a $+V_{ref}$ or $-V_{ref}$ voltage to a resistor connected to the integrator summing junction. This voltage is continuously applied to the integrator during the entire clock period. Note that the amount of charge delivered to the integrator is a function of the width of the clock pulse, the rise and fall times of the voltage feedback waveform, and, in the case of unequal rise and fall times, the previous bit decision. The use of a "return-to-zero" scheme can in theory eliminate the effect of previous bit decisions and rise-fall mismatches, but it increases the sensitivity to jitter [21].

2.3.2.4 Clock Jitter

Calculating the effect of clock jitter on a $\Delta\Sigma$ A/D converter implemented in switched-capacitor technology is a fairly simple matter. The operation of switched-capacitor circuits depends on complete charging during each phase of the clock. Once the analog signal has been sampled, the switched-capacitor circuit is similar to an analog sampled-data computer. The lengths of the time slots and the variations in the lengths of the time slots have no direct effect. Therefore, the effect of clock jitter on a switched-capacitor circuit can be analyzed by examining its effect on the sampling of the input signal and on the reconstruction of the output signal.

Since the output of an A/D converter is digital. the effect of clock jitter on the performance of a $\Delta\Sigma$ A/D converter is completely accounted for by taking into account the effect that it has on the sampling of the input signal. This also implies that the effect of clock jitter on switched-capacitor $\Delta\Sigma$ modulator is independent of the structure or order of the modulator.

Consider the effect of clock jitter on the sampling of the input signal. A sinusoidal time jitter with amplitude α and frequency ω will cause the sampling of the input signal at time τ to instead occur at time $\tau + \alpha\sin(\omega\tau)$. (The effect is the same as if the input signal . $A\cos\omega_0\tau$. were instead $A\cos[\omega_0(\tau + \alpha\sin\omega\tau)]$). This can also be written in the form $A\cos(\omega_0\tau + \alpha\omega_0\sin\omega\tau)$. which is recognizable as the expression for frequency modulation (FM). . For $\alpha\omega_0 \ll 1$. the jitter will give rise to a pair of sidebands at $\omega_0 - \omega$ and $\omega_0 + \omega$ with an amplitude $A\alpha\omega_0/2$. It can be seen that the jitter is modulated by the input signal and its power is scaled by the factor $A^2\omega_0^2/2$.Whether oversampling will help to reduce the output error caused by the jitter depends on the nature of the jitter. If the jitter is assumed to be white [6] and has a power $(\Delta\tau)^2$. then the resultant error will have uniform power spectral density from 0 to $f_s/2$. with a total power of $(A\omega_0\Delta\tau)^2/2$. In this case. the in band noise power will be reduced by the OSR. On the other hand. if the clock jitter has a $1/f$ characteristic ("close-in noise"). then the error will have a spectrum that appears as a "skirt " on the spectral line of the fundamental. In this latter case. oversampling will not reduce the in-band noise. and a $\Delta\Sigma$ converter will have the same sensitivity to jitter as a Nyquist-rate converter. Note that for continuous-time loop filters the effects are much more complex and harmful.

2.3.3 Design procedure

In this section we would like to explain the steps to design an IF or RF digitizer using low-pass sigma-delta modulators. In [22-24], complete design techniques for high order or multi-stage sigma-delta modulators for audio applications are shown. Since we are using these architectures for high frequency applications, we should consider other parameters like the distortion in the sample and hold or sampling mixer as well as the parameters discussed in the above mentioned references. The design procedure can be summarized as:

1. SNR, Bandwidth, and dynamic range(DR) have to be chosen.

2. The input carrier frequency is the second parameter which has to be chosen.

3. Using the above information, the order of the modulator for a given OSR is next determined:

   (a) from SNR value, the ideal equations should be used for different architectures to calculate the order of sigma-delta modulators. For example, for a single stage first order modulator the SNR can be determined by

$$SNR_{max} = 6.02N - 3.41 + 30\log(OSR) \tag{2.19}$$

   or for a second-order modulator the SNR can be determined by:

$$SNR_{max} = 6.02N - 11.14 + 50\log(OSR) \tag{2.20}$$

or in general $SNR = 6.02N + 20\log(OSR)^{\frac{L+1}{2}}$. The number of output bits, N, can be chosen arbitrarily. In most applications a one bit structure is required, therefore, the OSR can be calculated for a given order, L.

(b) After determining the OSR, the sampling clock frequency can be calculated for a given bandwidth. If the calculated sampling clock frequency is too large, the order must be increased.

4. The next step is to determine the noise transfer function(NTF) and signal transfer function (STF). The NTF and STF transfer function can be determined by the following steps [22]:

(a) Choose a modulator order and a NTF filter family. Modulator order already has been chosen in the previous step. For the NTF filter family, high-pass Butterworth, Chebyshev, or maximally flat all-pole filters can be chosen.

(b) Pick a value for cut off frequency which is larger than that of the required bandwidth. Then scale the transfer function so that the first sample of the impulse response is 1.

(c) Construct a modulator with this NTF and either simulate it or use the describing function method [25] to determine its maximum stable input and peak SNR. The maximum stable input gives the dynamic range.

(d) If the modulator is unstable, reduce the out-of-band gain of the NTF.

(e) If the modulator is stable but SNR is not adequate, then increase the out-of-band gain of the NTF.

To determine which architecture should be chosen, one of the five following options should be used [23]:

(a) Chain of integrators with weighted feed forward summation.

(b) Chain of integrators with feed forward summation and local resonator feedbacks.

(c) Chain of integrators with distributed feedback

(d) Chain of integrators with distributed feedback and distributed feed forward inputs

(e) Error feedback only.

5. Determine the minimum requirement for each block of the sigma-delta modulator to meet the specification. Designing the architecture in ideal form is not enough. To complete the design, opamp specifications such as dc gain, settling time, unity gain bandwidth have to be found. The important parameters can be summarized as:

(a) Minimum gain for the opamp. One simple rule is that the minimum gain should be $\frac{OSR}{\pi}$.

(b) The settling time as was explained in the previous section is dependent on the sampling clock frequency.

(c) In IF applications the linearity of this circuit is very important. The design guide presented in [3–5] can be used to design a highly linear sampling mixer. That is also used as in the S/H circuit.

In the next section, a design example is discussed in detail to present a step-by-step design framework for the reader.

2.3.3.1 Design Example

In this section, by using the design steps explained in the previous section a complete design cycle for an IF digitizer will be presented.

Example:A 40 MHz IF digitizer with a 200kHz bandwidth and a 70dB SNR is required.

Solution:

Step 1: Finding the order of the modulator, OSR, and the sampling clock frequency: The ideal second order modulator SNR can be written as:

$$SNR_{max} = 6.02M - 11.14 + 50\log(OSR). \tag{2.21}$$

where M is the number of output bits. In general, any number of bits can be chosen. But practically, producing a highly linear multi-bit D/A converter is very difficult. Therefore, usually the designers try to design a single-bit modulator. In this design, a single-bit modulator is designed. Therefore, the above equation can be written as:

$$70 = 6.02 - 11.14 + 50\log OSR \tag{2.22}$$

Or.

$$OSR = 31.79 \tag{2.23}$$

It is round up to 32. With an OSR of 32 and a 200kHz bandwidth. the clock should be chosen to be at least 12.8MHz. To simplify the implementation the ratio of the input frequency to the sampling clock should be an integer. As a result the sampling clock frequency is 20MHz or the OSR is 50.

Step 2: Determine the NTF: A single-bit second-order structure is chosen. so. using the standard second-order design which is shown in [7] can provide the required SNR. For this structure the NTF can be written as:

$$NTF = \frac{4(1 - z^{-1})^2}{3z^{-2} - 6z^{-1} + 4} \tag{2.24}$$

Step 3: Determine the architecture: A chain of integrators with distributed feedback shown in Fig. 2.10 is used for this design.

Step 4: Determining the minimum requirement for each block.

1. **Opamp gain:**The minimum required opamp gain can be calculated using $g > OSR$. Therefore a gain of 150 will satisfy the condition.

2. **Settling time:** Since the clock is chosen to be 20MHz. the integrator output has to settle in 25 ns for a two phase clock. Assume linear settling and 0.1% settling. Let us use equation (2.16) and assume $H(z)$ to settle to 0.1%. The ϵ is to be 0.003. Using equation (2.17) the B (opamp bandwidth) is calculated to be 73MHz.

3. **Sampling Capacitor C_1:** The noise regarding the sampling capacitor is $\frac{KT}{C}$. where K is the Boltzmann constant and T is the room temperature. For a requirement of one volt input. a 0.5pF capacitor for C_I is large enough to exceed a SNR of 70dB. From Fig. 2.10. $C_S = \frac{C_I}{2} = 0.25pF$. Because of noise reduction due to oversampling (3dB/octave). the noise decreases by another 12 dB. therefore. the C can be selected from a 58dB criterion instead of 70dB. As a result the C required can be smaller.

4. **Sampling mixer design:** In the first section of this chapter. the sampling mixer is explained. The sampling capacitor is already chosen due to SNR criteria. The fall time of the clock edge and the switch size are the two parameters that have to be chosen. Since the input frequency is not high. the dominant distortion is from time invariant distortion. HD_3 can be written as: [3–5]

$$HD_3 = \frac{A^2}{4} \frac{\omega C}{K(V_G - V_t)^3} \tag{2.25}$$

in which A. ω. C. K. V_G. and V_t represent the input amplitude. input frequency in rad/sec. sampling capacitor. $\mu_n C_{ox} \frac{W}{L}$. gate voltage. threshold voltage of the sampling switch respectively. The harmonic distortion must now degrade the signal-to-noise plus distortion ratio (SNDR). Arbitrarily set the harmonic distortion (HD) to -80dBm with the 0dBm input for a 50Ω input impedance. 3.3 volts power supply can be used with $0.5\mu m$ CMOS technology. In this technology the NMOS transistor threshold is about 0.8 volts.

The size of the transistor is calculated as:

$$\frac{W}{L} = 255.9 \tag{2.26}$$

therefore, with the minimum length transistor, $154\mu m$ is the width of the sampling mixer transistor. This is one of the three types of distortion which is discussed in detail in [3–5]. The other two types depend on the fall time of the clock and in one of the cases depends on the size as well. Since the sampling mixer is operating at IF (low enough frequency) the other two types of distortion can be ignored. To ignore the other two types of distortion, the maximum allotted fall time of the sampling clock has to be determined. The sampling distortion can be written as:

$$HD_3 = \frac{3A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2 \tag{2.27}$$

in which T_f, V_G, A, and ω represent fall time of the sampling clock, gate voltage of the sampling switch, input signal amplitude, and the input frequecny respectively. When the transistor size was calculated, it was assumed that the allotted distortion was -80dBm for 0dBm input. The fall time of the clock edge must be small enough so that the distortion created by fall time is much smaller than that of the time invariant distortion. Assuming the distortion due to sampling distortion is -100dBm, the fall time can be calculated as:

$$T_f = 214ps \tag{2.28}$$

The time varying distortion can be evaluated to make sure that the distortion produced by this type is much less than that of the time invariant distortion. For the present case this type of distortion can be determined by:

$$HD_3 = \omega^3 \sqrt{\frac{C}{K}} \left(\frac{T_f}{V_G}\right)^{5/2} \times 0.0913 \tag{2.29}$$

Therefore, distortion for the third type is around -100dBm which is acceptable.

In summary, it can be seen as one moves to higher frequencies ($> 100MHz$) designing a low distortion sampling mixer becomes more and more difficult to achieve as $\frac{W}{L}$ becomes unacceptably large. Therefore, the sampling mixer becomes the major bottleneck in the design.

5. **Comparator Speed:** The issue about comparator speed is due to the availability of the output code for less than half of the clock period to do the subtraction properly. In active architectures, the offset or the noise of the comparator is not very important because the effect is noise shaped.

2.4 band-pass architecture

One can do A/D conversion in the passband, thereby eliminating all the problems of the zero IF solution. Such an A/D converter can be Nyquist rate based or sigma-delta based. Because the input signal is narrowband in nature, it almost always makes sense to convert using a sigma-delta approach. Also by doing digitization

sooner, one can get rid of the analog narrowband IF filter (replacing them with the much more easily implemented digital filter). As described in previous sections, the quantization noise of a low-resolution quantizer can be nulled in a narrow frequency range by embedding the quantizer in a feedback loop. This feedback structure allows one to spectrally separate the noise from the input signal. The same principle can also be applied to higher frequency low-bandwidth signals, simply by placing nulls in the quantization noise spectrum across the band of interest. The band-reject noise shaping of these band-pass sigma-delta converters results in high SNRs for narrowband band-pass signals.

Band-pass sigma-delta modulators operate in much the same manner as conventional (low-pass) modulators and retain many of their advantages over Nyquist-rate converters. These advantages include inherent linearity (for single-bit systems), reduced anti alias filter complexity, and a robust analog implementation. The design of band-pass converters has much in common with low-pass modulator design. This section focuses on the aspects of modulator design which are peculiar to band-pass modulators and so only touches lightly on the elements which are the same as those of low-pass modulators.

In a manner analogous to low-pass modulators, a band-pass $\Delta\Sigma$ modulator can be constructed by connecting a filter and quantizer in a loop, as shown in Fig.2.17. The resonator may be implemented as a discrete-time filter using, for example, switched-capacitor or switched-current technology or it may be implemented as a continuous-time filter using, for example, LC or G_mC filters. The quantizer may be multi-bit or single bit, and the loop may use multiple quantizers.

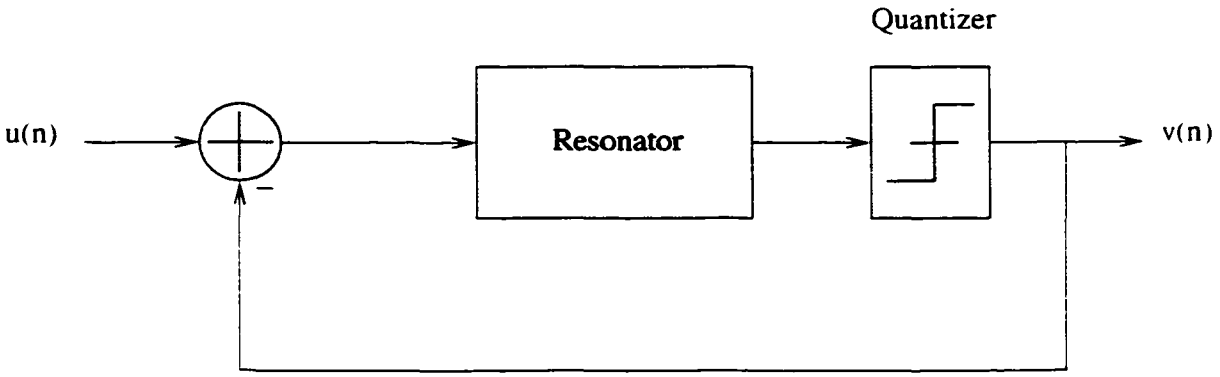


Figure 2.17: A general noise-shaping bandpass structure

In this section it is shown how a low-pass design can be used to implement a band-pass architecture. Then the design limitation of this architecture is discussed and at the end a design procedure for designing a complete band-pass architecture is explained.

Most of the design art for band-pass modulators can be derived from similar art for the more common low-pass case. Later in this section. it will be shown that an arbitrary low-pass sigma-delta converter of order N can be converted to a band-pass modulator of order $2N$ with a center frequency of $f_s/4$ via a simple mathematical transformation that preserves both the stability performance and the noise properties of the original modulator. Another key issue for band-pass sigma-delta modulator is that since there is no mixing at the input. the S/H circuit has to respond to the high frequency (IF) signal. therefore. making its design more challenging than in the case of low-pass sigma-delta or pipelined converters (which are preceded by a mixer). Of course in the case where pipelined and low-pass sigma-delta converters merge their S/H circuit with their mixer (by the use of sampling mixer as opposed to continuous type Gilbert mixer) the S/H circuits in these cases

face the same challenge as in the band-pass sigma-delta modulator case.

2.4.1 Band-Pass structure definition

Most of the design art for a band-pass modulator can be derived from similar art for the more common low-pass case. Later in this section. it will be shown that an arbitrary low-pass sigma-delta converter of order N can be converted to a band-pass modulator of order 2N with a center frequency of $f_s/4$ via a simple mathematical transformation that preserves both the stability performance and the noise properties of the original modulator.

Modeling the quantizer in Fig. 2.17 as a unity gain element with an additive white noise source and generalizing to allow the input and feedback to use different feed-ins to the filter yields the "linear model" that was described in previous sections. The resultant system can be described as shown in Fig. 2.18:

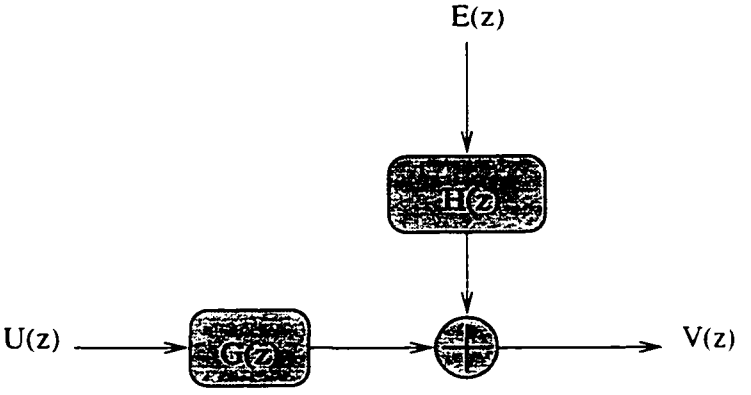


Figure 2.18: Linear model for sigma-delta modulator where the noise transfer function and signal transfer function are separated

$$V(z) = G(z)U(z) + H(z)E(z) \tag{2.30}$$

The key design issue is to choose a noise transfer function $H(z)$ that minimizes the in-band noise under two constraints: causality and stability.

The loop around the quantizer cannot be delay free, so $H - 1$ must be strictly causal (first impulse-response coefficient zero). This constraint forces

$$\lim_{z \to \infty} H(z) = 1 \tag{2.31}$$

which indicates that one cannot just force H to be zero everywhere. Making $|H|$ small in band forces it above unity out of band.

Stability is a more difficult problem. Making the linear model stable does not guarantee that the real nonlinear system (which is difficult to analyze because of the hard nonlinearity of the quantizer) is stable. A complete theory of stability adequate for design is lacking, but in general terms if the out-of-band noise gain gets too high overall, then the internal filter states will become very large. This leads to Lee's rule of thumb for 1-bit quantizers [26], which claims that constraining the peak gain according to

$$|H(e^{j\omega T})| < 1.6 \tag{2.32}$$

will result in a stable modulator. The above form includes some safety margin to allow for component variation and for the approximate nature of the criterion.

These considerations are the same as those used in the design of high-order low-pass modulators and thus band-pass noise transfer function design presents no new hurdles.

In a sampled-data system, frequency bands of interest scale with the sampling

frequency. For a discrete-time $\Delta\Sigma$ modulator, the noise-shaping band center is placed at a fixed angular frequency ω_0 on the unit circle in the z-plane and thus remains at a fixed fraction of the sampling rate.

For a given input signal center frequency and bandwidth, such as 10MHz input with 200kHz bandwidth, the choice of angular center frequency is a trade-off among sampling rate, anti aliasing filter requirements, and OSR. Placing the band near $\omega = 0$ increases the OSR and hence improves the performance achievable by a modulator of a given order. For example, for the OSR of 16, the sampling clock is chosen to be 320MHz. Therefore, the value of ω_0 is equal to $\frac{pi}{16}$. Furthermore, since the first image frequencies that will alias into the signal band are further away, the anti alias filter requirements are relaxed. For example, in the above numbers the bandwidth of anti aliasing filter can be as high as 320MHz. Too small an angular frequency, however, can lead to clock rates so high that the loop filter is unable to settle. In the above exmpale, the loop filter has to settle in less than 3ns. Moving the band closer to $\omega = \pi$ may be necessary to reduce the clock rate to an acceptable level, but this puts increased demands on the anti aliasing filter and on the noise-shaping loop. These trade-offs are similar to those for conventional low-pass modulators.

An additional consideration is that band placement at angular frequencies which are simple fractions of π, such as $\omega_0 = \pi/2$ and $\omega_0 = \pi/4$, allows for innovation in both circuit and decimation algorithm design.

Fig. 2.19 contrasts the pole-zero placements of $H(z)$ for a second-order low-pass modulator and a fourth-order band-pass modulator and illustrates the definitions

of ω_B, the normalized bandwidth, and OSR. In both cases, the modulator will have a small amount of quantization noise in the narrowband surrounding the zeros of $H(z)$, thus ensuring that the modulator output is an accurate representation of the input in the vicinity of those zeros. In the next section it will be explained how to design a band-pass transfer function from a low-pass transfer function.

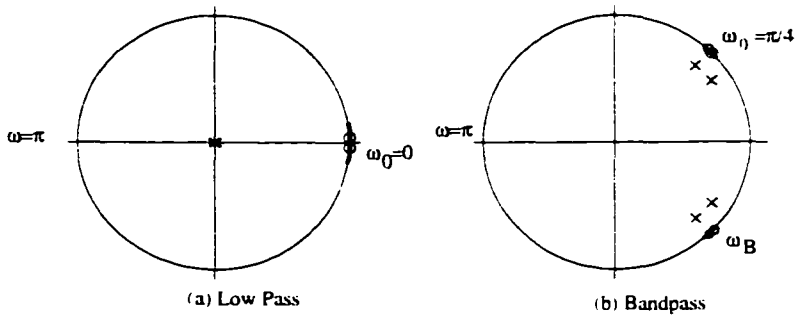


Figure 2.19: The pole/zero locations and pass bands of the noise transfer functions for (a) low-pass and (b) band-pass $\Sigma\Delta$ modulation

2.4.2 Low-pass to band-pass conversion

The simplest way to design $H(z)$ for a band-pass modulator is to start with a suitable low-pass modulator and apply a low-pass-to-band-pass transformation to it. Such transformations of necessity must increase the order of the modulator. The low-pass prototype must be chosen to satisfy the SNR specifications with an OSR that is a function of both the OSR of the band-pass modulator and the transformation employed.

For example, if one were to apply the transformation $z \rightarrow -z^2$ to a low-pass prototype, the zeros of $H(z)$ would be mapped from dc to $\pm\pi/2$ (low-pass to band-pass conversion [27]). This transformation places the center frequency at $\omega_0 = \pi/2$,

and thus for a fixed center frequency the sampling frequency is dictated by the relation $f_s = 4f_0$. Also, since this transformation preserves the OSR, the OSR of the prototype modulator is again determined by the signal parameters: $OSR = 2f_0/B$.

The $z \rightarrow -z^2$ transformation is a particularly attractive one since it does not affect the dynamics of the prototype. Specifically, the modulator behaves as a pair of multiplexed low-pass modulators, with alternate samples of each modulator negated. As a result, the band-pass modulator is stable if and only if the low-pass modulator is stable and the SNR curves of the modulators are identical. In particular, a fourth-order modulator designed this way [28] can be proven stable, because the prototype low-pass second-order modulator is known to be stable. For the competing radio architectures of Fig. 2.20, if the center frequency is to be $f_s/4$, then the band-pass modulator of Fig. 2.20(a) can be implemented by transforming the low-pass modulators of Fig 2.20(b) without altering the SNR performance.

Other transformations, such as generalized N-path transformations and low-pass-to-band-pass transformations, are possible but do not possess all the advantages of the $z \rightarrow -z^2$ transformation. The generalized N-path transformation $z \rightarrow \pm z^N$ preserves modulator dynamics but increases the modulator order unnecessarily for $N > 2$ (putting in unnecessary pass bands) or results in a pass-band centered at $f_s/2$ (where aliasing problems occur) for $z \rightarrow z^2$. On the other hand, generalized second-order low-pass-to-band-pass transformations give full control over the passband location but do not preserve modulator dynamics.

Nonetheless, the discrete-time low-pass-to-band-pass transformation

$$z \rightarrow -z\frac{z+a}{az+1} \qquad \text{where} \quad -1 < a < 1 \tag{2.33}$$

preserves both the realizability and the stability constraints. The case $a = 0$ degenerates to $z \rightarrow -z^2$: negative a gives systems with passband closer to dc: positive a gives systems with pass bands close to $f_s/2$. The effect on a conventional first-order modulator $H_p(z) = 1 - z^{-1}$ is

$$H(z) = H_p\left(-z\frac{z+a}{az+1}\right) = 1 + \frac{az+1}{z(z+a)} = \frac{z^2+2az+1}{z(z+a)} \tag{2.34}$$

This second-order transfer function can have noise zeros anywhere on the unit circle. approaches 1 as $z \rightarrow \infty$. is stable. and has a peak gain of 2 at $z = \pm 1$.

Similarly. transforming the conventional second-order $H_P(z) = (1 - z^{-1})^2$ yields

$$H(z) = \left(\frac{z^2+2az+1}{z(z+a)}\right)^2 \tag{2.35}$$

The performance of the modulator can be obtained through three iterations. The first iteration is the linear model predictions. A simple analysis based on the linear model explained above can be used to estimate the SNR of an Nth-order band-pass modulator [29]. One simply assumes that the quantization noise is white with power $\frac{1}{3}$ and that the noise transfer function has $N/2$ zeros at ω_0. The result is that for every doubling of the OSR the SNR increases by $3N + 3$dB.

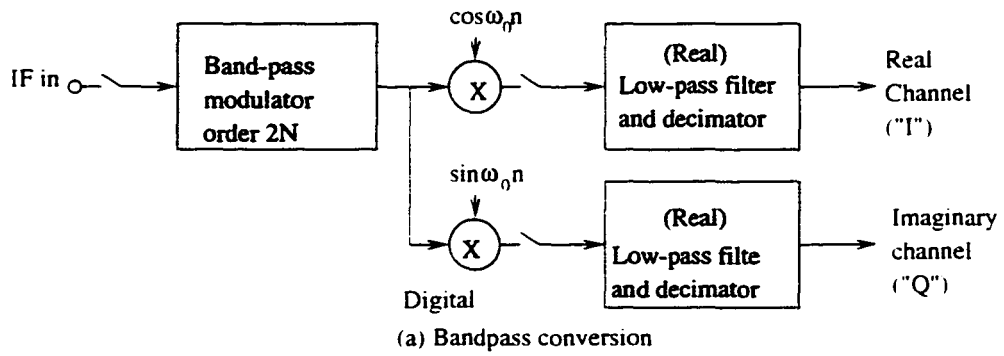
Notice that the total filter order is the same for both radio architectures in Fig. 2.20: For the same signal bandwidth and SNR the band-pass approach needs one modulator of order $2N$ to get the same performance that the zero-IF approach gets

with two modulators of order N. Furthermore, at least when the center frequency is $f_s/4$, a band-pass converter with order $2N$ has the same stability performance as a low-pass converter of order N. Finally, just as for low-pass converters, modulator cost is less than proportional to order, since the early stages dominate analog performance and later stages can be implemented more cheaply.

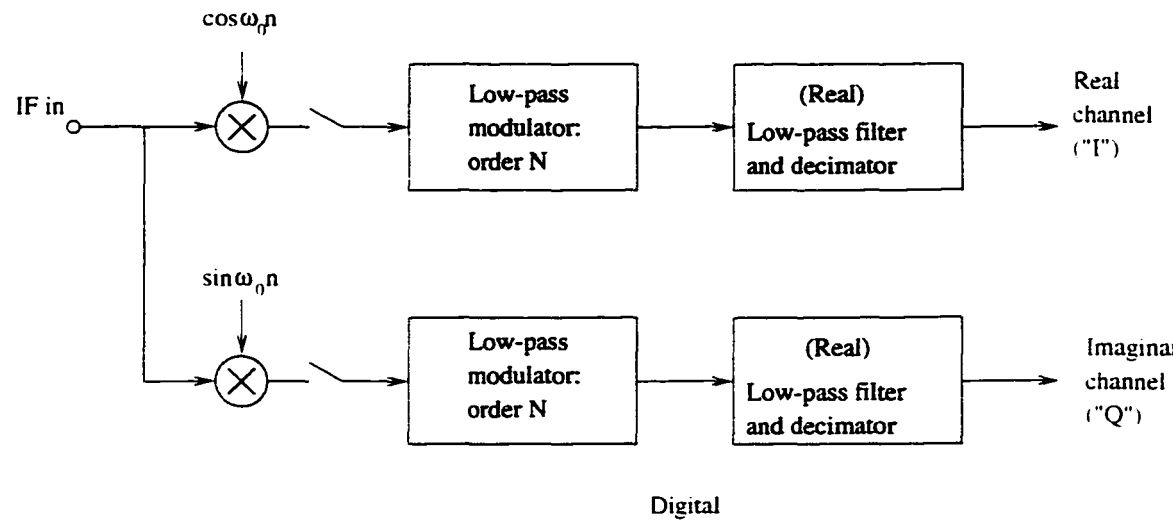
The second iteration is the simulation. The linear analysis gives an estimate of the SNR that is good enough to use for a first design iteration and makes it convenient to use a filter approximator for the basic design. However, the linear model neither guarantees stability nor allows an exact prediction of the input signal level that achieves the maximum SNR. Discrete-time simulations can check these overload characteristics. Output noise can be estimated by taking a Hann weighted discrete Fourier transform (DFT) of the output sequence and summing the power in the in-band "bins," excluding those containing the input tone.

The noise probability design function and spectrum that are assumed in the linear model are also approximate. The difference equation simulator can be used to check these assumptions. If the quantization noise is white, the output noise spectrum will look like a noise estimate of $|H(z)|$, and there will be no distortion or in-band tones. Such tones are known to be a problem with some low-pass $\Delta\Sigma$ converters [30–32]. Fig.2.21 shows a typical spectrum.

Nonetheless, it is possible for a band-pass modulator to suffer from tone problems identical to those found in low-pass modulators. Specifically, a band-pass modulator derived from a low-pass modulator via a $z \rightarrow \pm z^N$ transformation has exactly the same tonal properties as the prototype.



(a) Bandpass conversion



(b) Zero IF

Figure 2.20: Comparison of radios using band-pass $\Delta\Sigma$ and a zero IF with low-pass $\Delta\Sigma$.

Different simulation results predict that the SNR increases fairly smoothly with oversampling, with approximately the predicted $3N + 3$ dB/octave slope. A SNR of 80 dB or more is possible at reasonable oversampling ratios.

Note that the zeros of $H(z)$ can be placed coincidentally at band center or

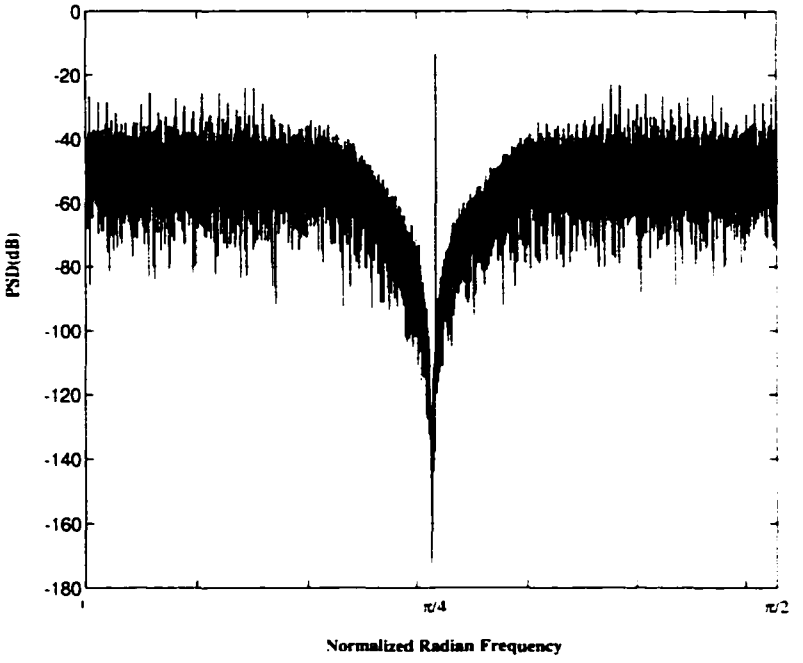


Figure 2.21: The spectrum of an example fourth-order modulator

placed optimally across the band of interest to minimize in-band noise power. A comparison of several modulators (centered at $\pi/2$) shows that a significant SNR advantage is gained with the optimal placement of zeros [33], namely a 5 dB advantage for a spread-zero fourth-order modulator and 10-dB advantage for sixth-order modulator. Although coincident zeros simplify the design process and may allow innovative circuits to be used, standard switched-capacitor circuits can easily incorporate optimized zeros and gain a SNR advantage over circuits that implement coincident zeros.

2.4.3 Hardware requirement

In band-pass architecture we also have the same components as in the low-pass architecture. In this section each of the components in either switched-capacitor circuits or continuous time circuits is considered and the effect of non idealities in the performance of the modulator will be discussed.

2.4.3.1 Capacitor and $1/f$ Noise

The KT/C noise present on each capacitor can be assumed to have a flat spectrum form dc to $f_s/2$. As we are concerned strictly with in-band noise, we gain an oversampling factor reduction in the KT/C noise power. This factor allows the minimum required capacitor size to be reduced by the same factor and proves to be an added benefit of oversampling.

Additionally, many capacitors see noise-shaped transfer functions to the output, again reducing the noise gain and hence the minimum required capacitor size. In the sixth-order cascade-of-resonators structure, for example, any capacitor noise injected to the right of a resonator is shaped by the first resonator's notch, while capacitor noise in the third resonator is shaped by both the first and second resonator notches. The result of these considerations is that the capacitors with the largest contributions to circuit noise are in the first resonator (i.e. the first two opamp stages) and they are generally the largest capacitors in the circuit.

The $1/f$ noise generated by other circuit components will lie well below the band of interest of most band-pass $\Delta\Sigma$ modulators. This noise will be swamped by out-of-band quantization noise and removed by the digital post filter and thus is of

little concern.

Clock feed through and charge injection problems can be reduced by the use of fully differential circuits and early and late clock phases.

2.4.3.2 opamp Speed

Satisfactory opamp bandwidth and slew rate performance are necessary to ensure that sufficient opamp output settling occurs. As is the case with low-pass $\Delta\Sigma$ converters it is possible that integrator outputs will change by their maximum swing in each clock cycle, regardless of the input signal voltage.

In the presence of limited operational amplifier bandwidth, the switched-capacitor integrator of Fig. 2.16 suffers from incomplete settling. If the integrator is assumed to settle linearly with a single-pole response, incomplete settling only manifests itself as an integrator gain error [6]. In this case, the transfer function of the integrator is

$$H(z) = \frac{C_1}{C_2}(1 - g_1)\frac{z^{-1/2}}{1 - z^{-1}} \tag{2.36}$$

where the gain error term g_1 is

$$g_1 = e^{-T/\tau} \tag{2.37}$$

T is the time allotted for settling, and τ is the closed-loop time constant of the integrator. If the resonator is implemented using two-phase, non overlapping clocks with 50% duty cycles, T is slightly less than $T_s/2$, where $1/T_s = f_s$, the sampling frequency. The closed-loop time constant of the integrator τ is approximately

$$\tau \approx \frac{1}{2\pi f_u}\frac{C_1 + C_2 + C_P}{C_2} \tag{2.38}$$

where f_u is the unity-gain frequency of the operational amplifier and C_P is the parasitic capacitance at the input to the operational amplifier. As the sampling rate is increased, the available settling time T decreases, and the gain error in (2.36) becomes increasingly large.

On a side note, it should be noted that, in practice, settling in switched-capacitor circuits is rarely governed by a strictly linear, single-pole response. Rather, the settling process usually includes a signal-dependent slewing component and is influenced by non dominant poles of the amplifier [34, 35], as well as finite switch resistances in the switched-capacitor network. In such cases, errors in a switched-capacitor integrator due to incomplete settling are understated by (2.36)and (2.37), with nonlinearities in the settling process not even reflected in these expressions. For tractability, only linear settling is considered in this analysis.

The effect of incomplete, but linear, integrator settling on the resonator can be assessed by modeling the two switched-capacitor integrators with (2.36) and independent gain error parameters g_1 and g_2. When second-order terms are neglected, the perturbed resonator transfer function is found to be

$$H(z) = G(1 - g_1 - g_2)\frac{z^{-2}}{1 - (2g_1 + 2g_2)z^{-1} + z^{-2}} \tag{2.39}$$

From this result, it follows that the fractional shift in resonator center frequency f_0 due to incomplete settling is approximately

$$\frac{\Delta f_0}{f_0} \approx -\frac{2g_1 + 2g_2}{\pi} \tag{2.40}$$

2.4.3.3 opamp gain

In the presence of finite operational amplifier gain, A, the switched-capacitor integrator implementation in Fig. 2.16 has the transfer function

$$H(z) = \frac{C_1}{C_2}(1 - m_1)\frac{z^{-1/2}}{1 - (1 - p_1)z^{-1}} \tag{2.41}$$

where the terms m_1 and p_1 model perturbations in the gain and pole locations of the integrator, respectively, and are given by

$$m_1 = \frac{1}{A}\left(1 + \frac{C_1}{C_2}\right) \tag{2.42}$$

and

$$p_1 = 1 - \frac{1 + \frac{1}{A}}{1 + \frac{1}{A}\left(1 + \frac{C_1}{C_2}\right)}. \tag{2.43}$$

The effect of finite amplifier gain on the resonator is assessed by modeling the two, nominally identical, switched-capacitor integrators with (2.41) and independent error terms m_1, p_1, m_2, and p_2. The system gains of both integrators, C_S/C_I, are chosen to be one. With this representation, the non ideal transfer function of the resonator is approximated by (2.44), when second-order terms are neglected. When the perturbations are small, namely m_1, p_1, m_2, and $p_2 \ll 1$, the fractional deviation in the center frequency, f_0, of the resonator is shown in (2.45)

$$H(z) = G(1 - m_1 - m_2)\frac{z^{-2}}{1 + (p_1 + p_2 - 2m_1 - 2m_2)z^{-1} + (1 - p_1 - p_2)z^{-2}} \tag{2.44}$$

$$\frac{\Delta f_0}{f_0} \approx \frac{p_1 + p_2 - 2m_1 - 2m_2}{\pi} \tag{2.45}$$

Thus, if the switched-capacitor integrators are implemented with operational amplifiers having a nominal dc gain of 60 dB, it follows from (2.44) and (2.45) that the magnitude peak of the resonator transfer function shifts by only 0.2% of f_0.

2.4.3.4 Sample-and-Hold Circuits

Typical low-pass $\Delta\Sigma$ converters accept inputs with frequencies up to one-hundredth the clock frequency, whereas a band-pass converter may accept input frequencies up to one-half of the clock frequency. Thus, the input slew rate is much greater in a band-pass converter. For example, a signal at $f_s/4$ can potentially change by its peak voltage in one clock cycle. The S/H operation, which samples the input signal at a specific point in time, must therefore perform within a much narrower window of time in order to give the desired accuracy. Any clock jitter or aperture error can severely degrade the accuracy of the sampled signal. However, in zero IF solution, when a sample and hold is used for the sampling mixer, the sampler performance in the low-pass structure is the same as that of the band-pass structure.

2.4.4 Design procedure

In the low-pass section, a design procedure was given to design a low-pass architecture. In this section, steps required for designing a band-pass architecture for IF or RF application is explained. To design a band-pass architecture, the low-pass-to-band-pass transformation approach is chosen. In this method the design steps can be summarized as:

1. From the system specification, the band of interest, SNR, and DR have to be specified.

2. The input signal frequency selection is the next step required for band-pass design.

3. The order of required low-pass transfer function is determined by SNR.

4. Determine the low-pass noise transfer function that is stable and satisfies the dynamic range.

5. Convert the determined low-pass transfer function to a band-pass transfer function with the $z \rightarrow -z^2$ transformation.

6. Convert the transfer function to a block diagram that includes only first order integrators.

7. Determine the minimum requirement for each block of the sigma-delta modulator. The center frequency depends on the location of the poles and zeroes whose positions are dependent on the integrator gain. With any small perturbation the SNR and DR will degrade. So the opamp gain and bandwidth and the ratio of the capacitors has to be specified before starting the transistor level design. The sample and hold circuit and the comparator requirements have to be identified as well.

2.4.4.1 Design Example

In this section, the same design example used in the low-pass architecture is used. Therefore, at the end of article the requirements of both architectures can be com-

pared.

Example: A 40 MHz IF digitizer with a 200kHz bandwidth is required. 70dB SNR for this structure is required.

Methodology:

Step 1: The input signal bandwidth is selected to be 200kHz and the SNR is selected to be 70dB.

Step 2: The input carrier frequency is 40MHz.

Step 3: Unlike the low-pass structure, in the band-pass, the clock is determined by the input frequency. In this example the sampling clock is chosen to be 160MHz. Now the OSR is calculated as:

$$OSR = \frac{2f_0}{B} = \frac{2 \times 40MHz}{200KHz} = 400 \tag{2.46}$$

The approximate SNR for single-bit band-pass architecture in terms of OSR can be written as:

$$SNR = 20\log(OSR)^{\frac{N+1}{2}} \tag{2.47}$$

So,

$$70dB = 20\log(400)^{\frac{N+1}{2}} \Rightarrow N \geq 1.69 \tag{2.48}$$

This is the ideal calculation. To give a margin for getting the values in design, the value of $N = 4$ is chosen. So the order of the low-pass transfer function is 2.

Step 4: To determine the noise transfer function which satisfies the stability and dynamic range, the same transfer function that was used for our low-pass structure in the previous sections will be used . The NTF and STF for the designed system

can be written as:

$$NTF = \frac{4(1 - z^{-1})^2}{3z^{-2} - 6z^{-1} + 4} \tag{2.49}$$

$$STF = \frac{z^{-2}}{3z^{-2} - 6z^{-1} + 4} \tag{2.50}$$

Step 5: The converted transfer functions can be written as:

$$NTF = \frac{4(1 + z^{-2})^2}{3z^{-4} + 6z^{-2} + 4} \tag{2.51}$$

$$STF = \frac{z^{-4}}{3z^{-4} + 6z^{-2} + 4} \tag{2.52}$$

Step 6: The above transfer functions can be realized as Fig. 2.22

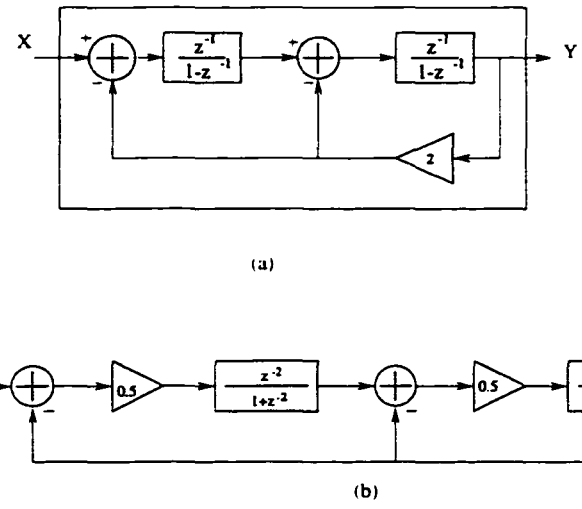


Figure 2.22: Realized band-pass architecture. (a)$\frac{z^{-2}}{1+z^{-2}}$ structure (b) the final realization of the fourth order architecture

Step 7:

1. **Opamp gain** From (2.42), (2.43), and (2.45) the opamp gain can be calculated. If there is only 0.2% perturbation in the peak frequency, the opamp

gain has to be larger than 800. To make sure that this perturbation is less than 0.2%. the required opamp gain is selected to be 1000 or 60dB.

2. **Opamp bandwidth** The required unity gain bandwidth can be calculated from equation (2.40). Assuming the opamp is single pole and there is no nonlinear settling problem due to slow slewing. the required bandwidth has to be at least 500MHz for 0.2% perturbation in peak frequency.

3. $\frac{KT}{C}$ **noise** This part is the same as for the low-pass. So. the same capacitor value is chosen.

4. **Sampling switch size** This one follows the same design criteria as the low-pass sampler mixer design which is difficult to achieve as one moves into higher frequencies ($> 100MHz$). This again will become the bottleneck as IF increases.

5. **Comparator requirement** In this architecture the comparator has to work at very high speed(at least four times input frequency).

2.5 Band-pass vs low-pass

We now compare the architecture in sevtion 2.3 to that in section 2.4 and build up the motivation for the new architecture presented in this thesis. The styles can be very similar. both mathematically and in terms of circuits. with the main distinction being whether quadrature mixing is done on the analog or the digital side. Fig. 2.20 shows how similar the two techniques are. In practical terms. band-

pass converters have to sample faster slewing signals than zero-IF systems but do not need precisely matched analog mixers and modulators. Zero-IF systems can also have difficulties with self-interference, as local oscillators reradiate to the front end, and their converters have to contend with $1/f$ noise. The key observation is that both architectures need highly linear (low distortion) input S/H circuits (or sampling mixers) as input IF frequency increases.

If one wants to compare the two architectures in terms of the hardware specification requirements, the two examples shown in previous sections can give a good comparison. For the low-pass structure the requirements for the opamp and comparator are much less than in the case of the band-pass. The reason is that in the band-pass structure the null frequency is not dc so it is very sensitive to the opamp gain and settling time. On the other hand, in the low-pass structure the null frequency is dc so a change in the gain only changes the noise floor but the null frequency does not change, so the restriction is less. On the other hand for the low-pass structure the sampling clock depends on the bandwidth of interest rather than input carrier frequency in the band-pass case. So the settling time in the low-pass case can be much larger than for the band-pass case. Since the sampling clock frequency is lower, the comparator can work at lower speed. The above comparison is summarized in table 2.1.

Modulator type	Opamp gain	opamp bandwidth	comparator speed
Low-pass	moderate	moderate	low frequency
Band-pass	moderate to high	high	high frequency

Table 2.1: comparison between low-pass and band-pass architecture

There is another thing that has to be considered. In the standard band-pass

structure there is only one path for the analog signal and the I and Q are separated in the digital domain, whereas, in the low-pass structure, two paths for the I and Q are required. So the mismatching in two paths is important.

2.6 Summary

In summary, it is clear that to design a highly linear high IF digitizer (beyond 100MHz) both the conventional band-pass sigma-delta modulator and the conventional low-pass sigma-delta modulator are inadequate. The major bottleneck is the distortion coming from the sampling mixer. A new approach needs to be invented to suppress the distortion component, coming mainly from this mixer. The use of feedback is a viable solution. Putting the mixer inside the sigma-delta modulator feedback loop is appealing because of its simplicity. Due to the presence of a quantizer in this feedback loop, the theory of distortion suppression using the classical linear feedback loop [36] is not adequate. In the next chapter we will present the new theory that quantifies distortion suppression in a **quantized** feedback loop. A new architecture is also presented that allows us to suppress distortion using quantized feedback.

Chapter 3

Theory of Distortion Behavior in a Quantized Feedback Loop

3.1 Introduction

One of the components of a receiver chain in a digital radio is an analog to digital (A/D) converter. Digitizing signals early in the receiver chain at high intermediate frequency (IF) or even in the radio frequency (RF) stage create a flexible and simple architecture. Due to increasing demands on A/D converter specifications for high IF narrow band applications, sigma-delta modulators, either low-pass or band-pass, are the preferred A/D converters for their high resolution capability.

One of the issues in a sigma-delta modulator is the effect of the non-linear characteristic of electronic components on the system performance [37]. In a sigma-delta modulator architecture, feedback is a necessity. This type of feedback is different from the classical feedback used in amplifiers. In the sigma-delta modulator ar-

chitecture, the feedback signal consists of a limited number of values which is dependent on the number of bits. Implementing a feedback loop in the architecture is expected to reduce the effect of the non-linear characteristic on the system performance. It has been shown that in the sigma-delta modulator architecture, its performance depends on the characteristics of the components closer to the input. On the other hand, the distortion is suppressed in the classical feedback system in which the non-linear component closer to the input is affected the most. As a result, the quantized feedback should be different from the classical feedback.

In this chapter, the differences between the classical feedback and the quantized feedback are discussed. First a theory of classical feedback will be presented. Then, the quantized feedback and its effect on the performance of the system will be discussed. Followed by a new technique is presented to improve the behavior of the quantized feedback in low and high frequency applications. then, the stability of the new architecture will be described, and finally, a model for the proposed architecture in both low and high frequency application will be developed.

3.2 Theory of Nonlinear Component's Distortion Behaviour in a Classical Feedback loop

The transfer characteristic of a nonlinear amplifier can be described as:

$$S_o = a_1 S_i + a_2 S_i^2 + a_3 S_i^3 + \cdots \tag{3.1}$$

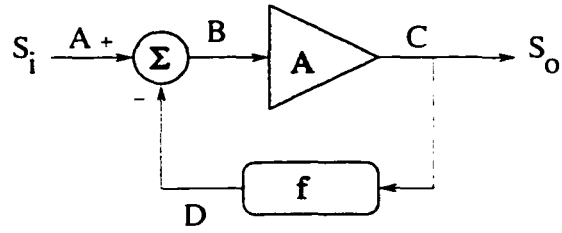


Figure 3.1: A non-linear amplifier in the feedback system

in which S_o, and S_i are output and input signals respectively. In order to suppress distortion, this amplifier is placed in a feedback loop with a feedback factor of f (shown in Fig.3.1). Now the new nonlinear transfer characteristic is expressed as:

$$S_o = b_1 S_i + b_2 S_i^2 + b_3 S_i^3 + \cdots \tag{3.2}$$

in which S_o, and S_i are the output and the input of the system. It can be easily shown that $b_i (i = 1.2.3....)$ are dependent on $a_i (i = 1.2.3....)$ and f. The relationship between the coefficients and feedback factor can be expressed as [36]:

$$b_1 = \frac{a_1}{1 + a_1 f} \tag{3.3a}$$

$$b_2 = \frac{a_2}{(1 + a_1 f)^3} \tag{3.3b}$$

$$b_3 = \frac{a_3(1 + a_1 f) - 2a_2^2 f}{(1 + a_1 f)^5} \tag{3.3c}$$

$$\vdots$$

It is shown that all the b coefficients are less than a coefficients. The harmonic distortion can be calculated through the non-linear coefficients. For example, the

second harmonic distortion for the amplifier without is written as:

$$H_{D_2} = \frac{1}{2}\frac{a_2}{a_1^2} S_{OM} \tag{3.4}$$

and for the amplifier with feedback is written as:

$$H_{D_2} = \frac{1}{2}\frac{b_2}{b_1^2} S_{OM} = \frac{1}{2}\frac{a_2}{a_1^2}\frac{S_{OM}}{(1 + a_1 f)} \tag{3.5}$$

Here S_{OM} is the output amplitude When comparing equation 3.4 and 3.5. it is seen that. the harmonic distortion without feedback is reduced by the open-loop gain of the system shown in Fig.3.1. i.e.. $(1 + a_1 f)$. One may argue that such improvement is misleading since the feedback action reduces the effective signal amplitude at the input of the nonlinear component (amplifier) This argument. however. is invalid since the reduction in signal amplitude has already been taken into consideration by maintaining the same output (rather than input) amplitude S_{OOM}. when comparing equations 3.4 and 3.5. i.e.. the input signal for the amplifier with feedback has been increased such that signal amplitude to the amplifier A with or without the feedback loop is the same. What then explains the suppression of distortion? This is due primarily to the fact that feedback produces a predistorted signal at node **B**. At this node. the level of predistortion is approximately equal and opposite to the distortion introduced by the nonlinearity in A. thus resulting in an output that is almost distortionless.

The above analysis shows the steady state behavior of the system. To understand how predistortion works the response of various nodes during transient will

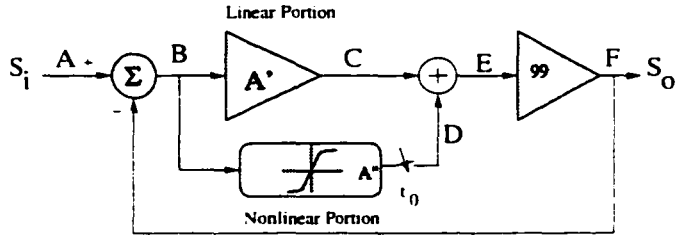


Figure 3.2: A non-linear amplifier in which the linear part and nonlinear part are separated in two paths in the feedback system

investigated. Let us redraw the system in Fig. 3.1 to Fig. 3.2 where the nonlinear amplifier A is separated into a linear part A', a nonlinear part A'', and followed by a gain block with gain equal to 99. Let us assume that the switch in Fig. 3.2 is open at $t < t_0$ and the amplifier is in steady state condition, that is, the output is a single tone for a single tone input. It is assumed that linear part A' has a unity gain. AT $t < t_0$ A'' is disconnected. Then

$$S_o = S_i \frac{99A'}{1 + 99A'f} = S_i \times 0.99 \tag{3.6}$$

Therefore, if S_i is chosen to be one, S_o becomes 0.99. Let us also assume, for illustrative purposes, that the nonlinearity is second order only, i.e.

$$D(t) = 0.01B^2(t) \tag{3.7}$$

To demonstrate how predistortion keeps to suppress distortion, let us examine the frequency spectrum at various node (as shown in Fig. 3.3) as one iterates around loop. Fig. 3.3a shows a single-tone input S_i with unity amplitude and frequency of ω_i at node **A**. In steady state condition the output node (node **F**) is also a single-

tone (Fig. 3.3b)) with amplitude of 0.99 and frequency of ω_i. Spectrum at node **B** consists of a single-tone with amplitude of 0.01 and frequency of ω_i (Fig. 3.3c). Next at $t = t_0$ the switch of the nonlinear path is closed. Assume signal has not traversed through the feedback loop. then spectrum at node **B** stays as depicted in Fig 3.3c. From equation 3.7 thus $B(t)$ (tone at ω_i) generates a $D(t)$ with tone at $2\omega_i$ and amplitude at 5×10^{-5} (Fig. 3.3d). Fig. 3.3d exhibits the spectrum at node **D**. This spectrum is added to the node **C** spectrum and produces spectrum for node **E** as shown in Fig. 3.3e. Therefore. node **F** has a new frequency component at $2\omega_i$ (Fig. 3.3f) when compared to Fig. 3.3c. This signal is fed back (with $V_A(t)$ set to 0) iterates to generate spectrum as shown in Fig. 3.3g (node **B**). At this point in time it should be noted that due to feedback spectrum at node **B** consists of extra component at $2\omega_i$. In time domain the feedback action has predistorted the waveform at **B** to an extent that is a function of the nonlinearity. (Note that the amplitude at $2\omega_i = 4.95^{-2}$ and is related to the coefficient 0.01 in equation 3.7). Also note that this frequency component has a negative sign. It is precisely this negative component that is responsible for cancelling some of the original distortion components. Let us continue the iteration to node **C**. **E** to further highlight this point. Spectrum at node**B** is multiplied by 1 and generates spectrum at node **C** (Fig. 3.3h). Spectrum at node **B** is passing through nonlinearity described in equation 3.7. produces spectrum at node **D** which now has second harmonic and fourth harmonic distortion. (Fig. 3.3i) Note at $2\omega_i$we have 2 components with opposite polarity (4.95^{-3} and 4.9005×10^{-3}) and they cancel out one another. As amplifier gain increase to a larger number their amplitudes become closer and the

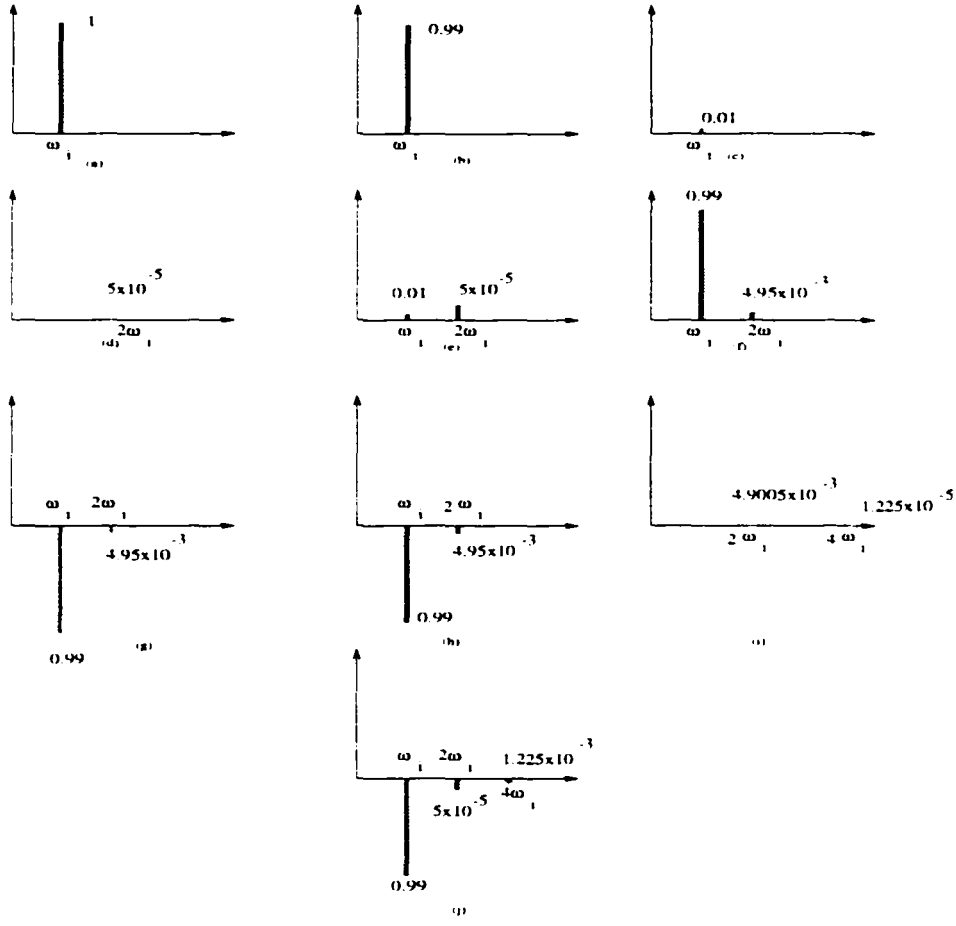


Figure 3.3: Frequency spectrum of the system shown in Fig. 3.2, given a monotone sinusoidal input, during iteration mode a) the spectrum at node **A** b) the spectrum at node **F** in the steady state condition c) the spectrum at node **B** in steady-state d) the spectrum at node **D**at $t > t_0$ e) the spectrum at node **E** f) the spectrum at node **F** g) the spectrum at node **B** h) the spectrum at node **C** i) spectrum at node **D** and j) spectrum at node **E**.

cancelation is more complete. Now, compare spectrum at node **E** in Fig. 3.3e,j and we can see distortion at $2\omega_i$ is reduced from 5×10^{-2} to 4.995×10^{-3}. This step by step iterations shows that the distortion is reduced even if the loop gain is not high. If the loop gain is increased, the suppression will be much more.

In summary, the input signal of the nonlinear component is predistorted due to the feedback path. Consequently, the predistorted signal reduces the overall distortion at the output. Note that the different frequency components in the feedback signal all pass through a nonlinear component whose behavior is the same for all of them. As a result, the nonlinear component will create same distortion for all frequency components. This iterative process demonstrates how a feedback signal in a classical feedback system suppresses distortion.

3.3 1-bit Quantized Feedback

Quantized feedback is a type of feedback whose feedback signal amplitude is discrete in time and consists of a limited number of values. A sigma-delta modulator is a primary example. IF one replace the 1-bit quantizer with a white noise model the modulator becomes a conventional feedback system and one expects it would suppress distortion in the same fashion. This turns out not to be the case. For example, in Fig. 3.4a we put a nonlinearity, labeled by $f(u)$ in front of (and hence outside) a sigma-delta modulator. Fig. 3.5a shows the simulated FFT plot of the output of this system and HD_2 shows up as expected. Next in Fig. 3.4b we put the same nonlinearity $f(u)$ inside the sigma-delta modulator. Fig. 3.5b shows the simulated FFT plot of the output of the system. Contrary to expectation HD_2 does not get suppressed. These simulation results show that quantized feedback system and the conventional feedback loop work differently

The reason that the single-bit quantized feedback loop does not improve the distortion is due to the binary nature of the feedback signal. To show the behaviour

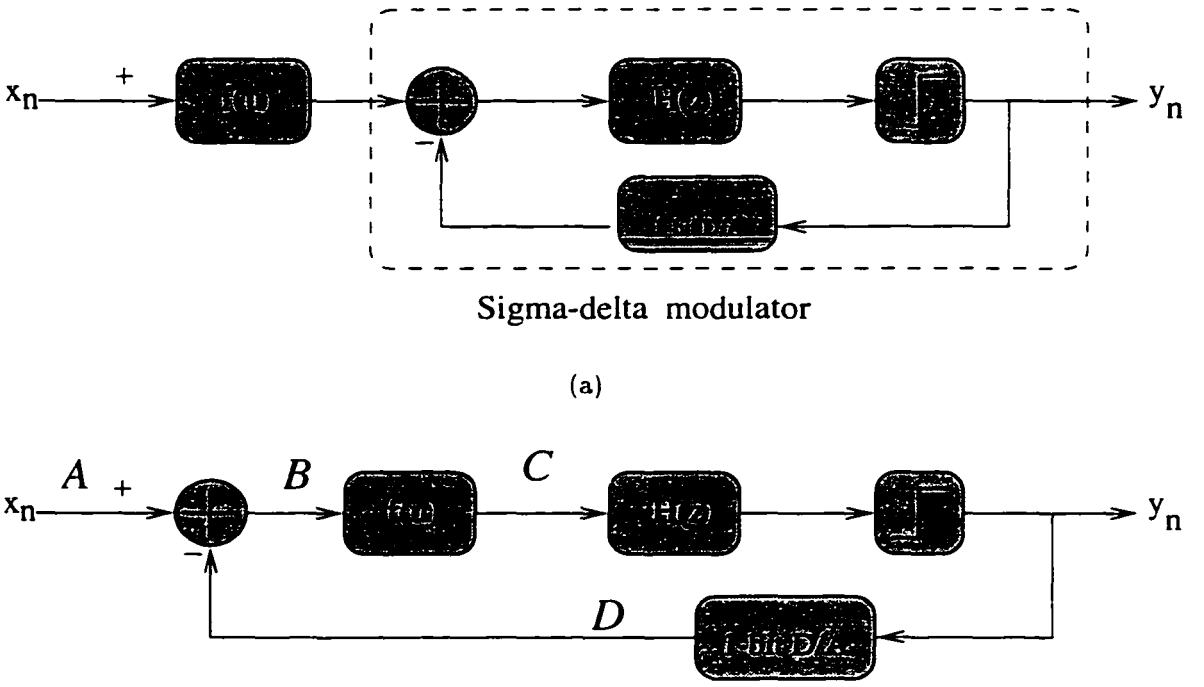
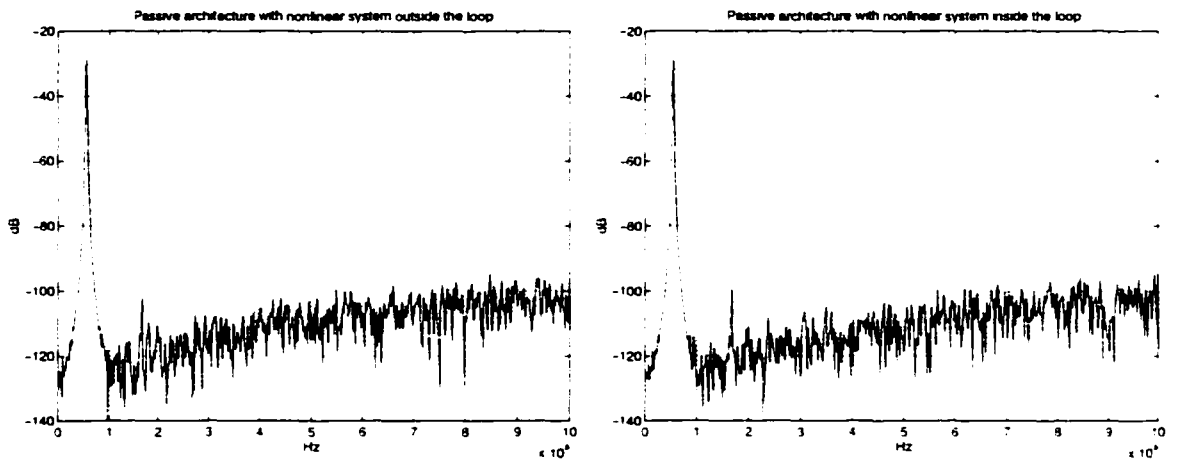


Figure 3.4: A sigma-delta modulator with a third order non-linear component $f(u)$ a)outside the feedback loop b)inside the feedback loop

of applying a quantized signal to a nonlinear component. Let us assume that the input signal of the nonlinear component $f(u)$ shown in Fig. 3.6 consists of discrete levels. Fig. 3.7 shows the output signals for 1-bit and multi-bit inputs. As shown in Fig. 3.7c the response to the 1-bit (binary) signal consists of only 2 levels. Since one can always draw a straight line between 2 levels, the nonlinearity in $f(u)$ does not produce a distorted output signal. On the other hand, 3-bit input signal in Fig. 3.7b creates an output signal with non-uniform increments as shown in Fig. 3.7d. Hence



(a) (b)

Figure 3.5: The frequency response of an original sigma-delta modulator architecture with a non-linear component a) outside the feedback loop(Fig. 3.4a) b) inside the feedback loop (Fig. 3.4b)

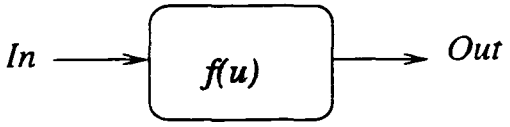


Figure 3.6: A block diagram of a nonlinear component

the output signal is distorted. In summary passing a signal that is represented in binary code through a nonlinearity does not distort the signal. This also means passing a predistorted signal represented in binary code through a nonlinearity does not get a distortion less output. When one applies this observation to node **B**. **C** of Fig. 3.4a. it is seen signal at node **C** remains distorted. This then explains the simulation results in Fig. 3.5b. Next we quantify the observation mathematically.

Assume $f(u)$ the nonlinear component shown in Fig. 3.6 has the following

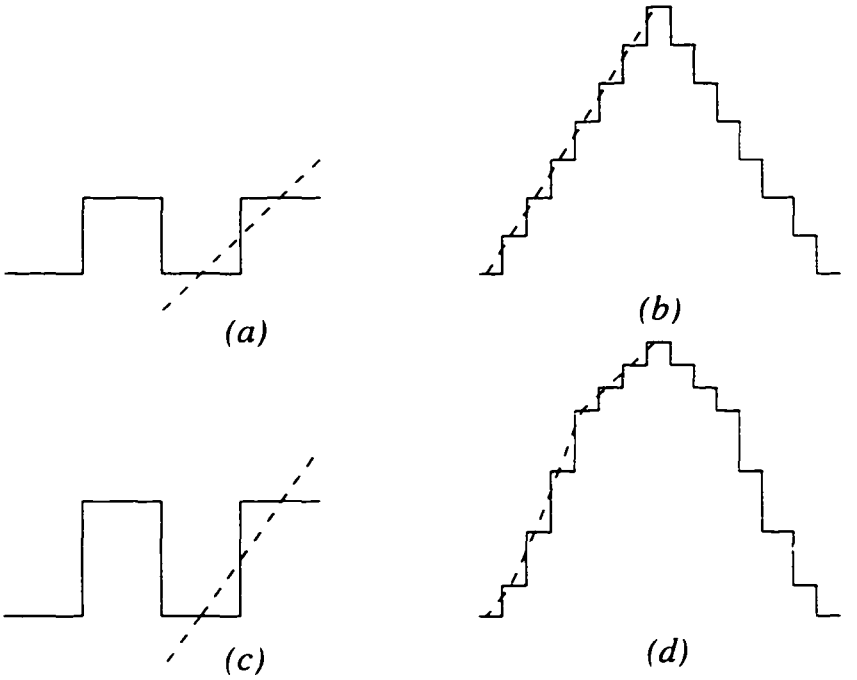


Figure 3.7: Input and output of the nonlinear component shown in Fig. 3.6 a) Single-bit input b) Three-bits input c) Single-bit output d) Three-bits output

input-output relationship:

$$f(u) = \sum_{i=0}^{n} a_i u^i \tag{3.8}$$

Let us assume the input is a binary input i.e. $u = 1$ or -1.

In this case, $f(u)$ can be expanded to contain an odd and an even terms:

$$f(u) = f_{even}(u) + f_{odd}(u) \tag{3.9}$$

in which

$$f_{even}(u) = \sum_{i=0}^{\lfloor \frac{n+1}{2} \rfloor} a_{2i} u^{2i} \tag{3.10}$$

and

$$f_{odd}(u) = \sum_{i=0}^{\lfloor \frac{n+1}{2} \rfloor - 1} a_{2i+1} u^{2i+1} \tag{3.11}$$

Here $\lfloor x \rfloor$ is the maximum integer just below x. Since the input is binary and is normalized to 1 and -1. input raised to an even order of power is always one ($u^{2i} = 1$). Therefore. $f_{even}(u)$ is independent of u and can be written as:

$$f_{even}(u) = \sum_{i=0}^{\lfloor \frac{n+1}{2} \rfloor} a_{2i} \tag{3.12}$$

Again. because of the binary nature. input raised to an odd order of power is the same as u ($u^{2i+1} = u$). As a result. $f_{odd}(u)$ can be written as:

$$f_{odd}(u) = u \sum_{i=0}^{\lfloor \frac{n+1}{2} \rfloor - 1} a_{2i+1} \tag{3.13}$$

Consequently. $f(u)$ can be written as:

$$f(u) = K_1 u + K_2 \tag{3.14}$$

in which K_1 and K_2 are $\sum_{i=0}^{\lfloor \frac{n+1}{2} \rfloor - 1} a_{2i+1}$ and $\sum_{i=0}^{\lfloor \frac{n+1}{2} \rfloor} a_{2i}$ respectively. Equation 3.14 shows that for a binary input u the nonlinear transfer function $f(u)$ is linearly dependent on u. as shown qualitatively in Fig. 3.7c.

To show why the single-bit quantized feedback signal does not have any effect on the distortion. two separate cases are discussed: The first case is data acquisition application where the nonlinear effect comes from the sample-and-hold (S/H) circuit. The nonlinearity from this circuit can be treated as time-invariant. The

second case is the wireless application where the nonlinear effect comes from the sampling mixer. In this case the nonlinearity is time varying.

3.3.1 CASE 1: $f(u)$ is nonlinear but time invariant

Let us refer to Fig. 3.4b. where we represent the S/H circuit's nonlinearity as $f(u)$ and placed it inside the sigma-delta loop. To analyze it let us repeat what has been done (in Fig. 3.3) for conventional feedback.

It is assumed that initially the sigma-delta modulator shown in Fig. 3.4b is in the steady state region with zero input. Therefore, the output frequency response does not consist of any signal in the signal band. It is also assumed that the frequency of limit cycle oscillation due to a zero input is outside of the band of the interest. Also the high frequency quantization noise is not central to our discussion and is omitted in the following frequency spectrum plot. At time $t = 0^+$, a sinusoidal signal with frequency ω_i is applied to the input. Therefore, the spectrum at node **A** is shown in Fig. 3.8a. Assume the signal nonlinearity is just switched in at $t = 0^+$ and so like Fig. 3.3c the signal at node **B** consists of only the input signal (Fig. 3.8b). At this iteration this signal is not binary represented and so upon passing through the nonlinear component $f(u)$ new frequency components at $2\omega_i$ are generated (Fig. 3.8c). This signal now passes through the loop filter and quantizer. Since quantizer/loop filter has gain and since we neglect quantization noise, node **D** has same spectrum as Fig. 3.3f. But the signal is represented in a binary fashion (Fig. 3.8d). Next signal at node **D** is fed back to the input. Upon fed back frequency spectrum at node **B** is shown in Fig. 3.8e. Note up to this point frequency spectrum for quantized feedback (Fig. 3.8a-e) corresponds exactly

to frequency spectrum of conventional feedback (Fig. 3.3a-g). From this point unwards, they will differ. Let us assume that there is no intermodulation between the different frequency components when they are passing through $f(u)$. In the second iteration, notice even though frequency plot at Fig. 3.8e looks the same as Fig. 3.3g, signal represented in Fig. 3.8e is binarily coded. Hence upon passing through the nonlinear, $f(u)$, it does not create any new distortion components, as explained in Fig. 3.7a,c. Hence node **C** has same frequency spectrum as node **B** (Fig. 3.8f) and remains distorted. Since there are no new frequency components as in Fig. 3.3i, no cancellation occurs. In conclusion, the single-bit quantized feedback system has a different behavior from the classical feedback and it does not reduce the distortion.

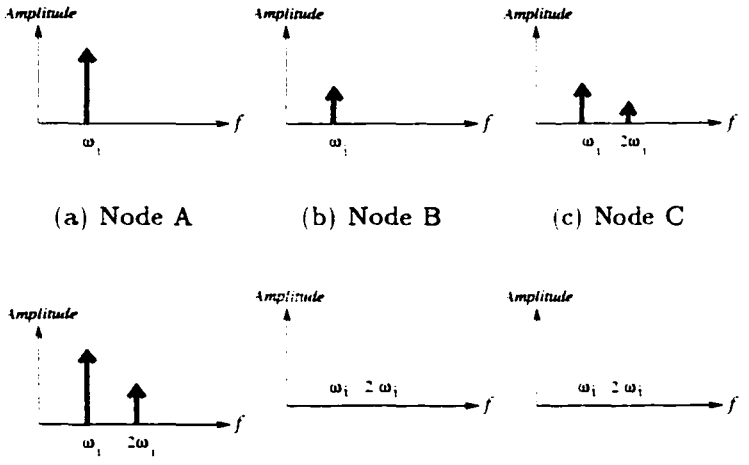
3.3.2 CASE 2: $f(u)$ is nonlinear but time varying

Let us again refer to Fig. 3.4b, where in the present wireless application we would like to put a mixer inside the feedback loop and where this mixer's nonlinearity is represented by $f(u)$. As a digression let us point out in wireless application where one needs to implement an IF digitizer the mixer and the sigma-delta modulator can be used in one of the following two approaches:

1. The mixer is in front of the sigma-delta modulator feedback loop

2. The mixer is inside the sigma-delta modulator feedback loop

The first method is the conventional method used in a receiver chain. The second method the user uses the feedback loop to reduce the mixer distortion. Since a mixer is time-varying, and capable of translating the frequency of an incoming



(a) Node A (b) Node B (c) Node C

(d) Node D (e) Node B. 2nd iteration (f)

Figure 3.8: Frequency spectrum of the system shown in Fig. 3.4(b) during iterations mode a) the spectrum at node **A** b) the spectrum at node **B** in the first iteration c) the spectrum at node **C** d) the spectrum at node **D** e) the spectrum at node **B** in the second iteration f) the spectrum at node **C** The black in the positive amplitude is due to the input signal. The grey is due to the linear frequency response for the feedback signal.

signal at ω_i to an output signal at ω_0. we would want to repeat analysis in case 1(Fig. 3.8). while incorporating this frequency translating property.

first let us investigate what would happen if we simply inco-oparate the mixer in a conventional feedback loop. A mixer alone in the forward path of a classical feedback system creates an unstable system (Fig. 3.9) because S_I is at a different frequency from S_o. Hence. another mixer in the feedback path is required to stabilize the loop (Fig. 3.10). On the other hand. in a sigma-delta feedback loop the output signal is a sampled signal. Therefore. the output spectrum consists of the

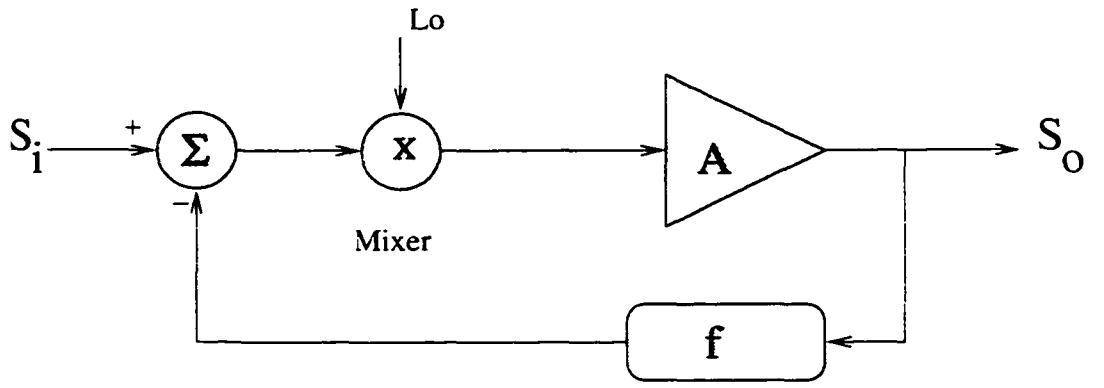


Figure 3.9: A classical feedback system with a mixer in the forward path

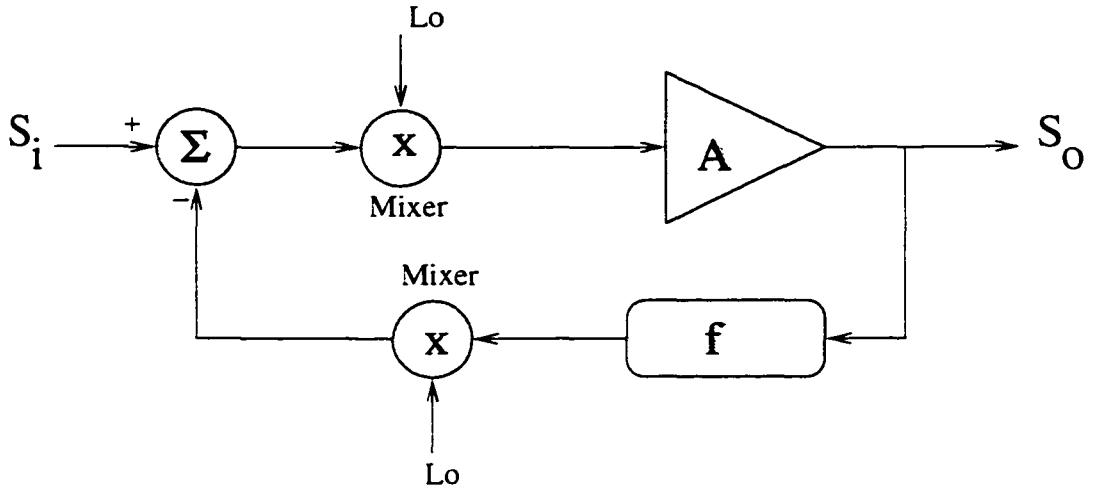


Figure 3.10: A classical feedback system with only a mixer in feedback and forward path

baseband and its images at multiples of the clock frequencies. If the clock frequency is set to be the same as the LO frequency. S_i will be at the same frequency as S_O and the feedback loop will be stabilized. One advantage of a sigma-delta feedback loop over a classical feedback loop is then the elimination of a real physical mixer in the feedback path. This new architecture is shown in Fig. 3.11(a). Where a switch is inserted after the quantizer to illustrate the fact that the output is sam-

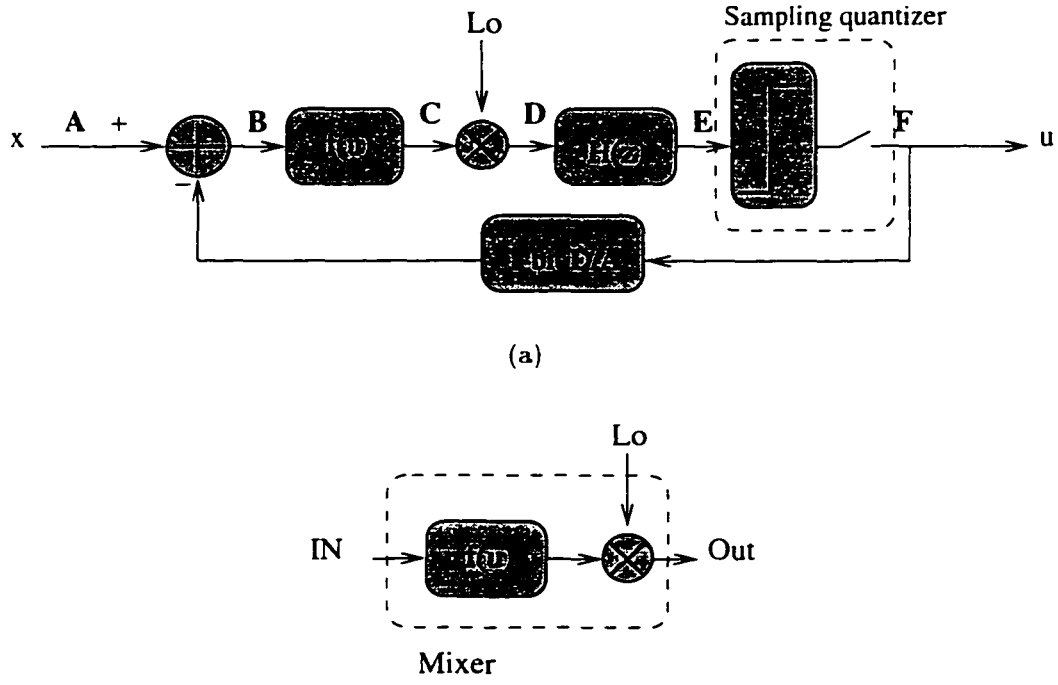


Figure 3.11: a)A quantized feedback system with mixer inside the loop b) A model for a nonlinear mixer

pled, in this case at a clock rate equals to f_{LO}. Please be noted that the mixer in Fig. 3.10has been modeled as a nonlinear component $f(u)$ followed by an ideal multiplier (Fig. 3.11(b)). This model is then applied in Fig 3.11(a). Note the similarity between Fig. 3.11(a) and Fig. 3.4a. The major difference is the frequency translation due to the ideal multiplier . The analysis presented in case 1 (on Fig. 3.4a) will now be repeated to highlight this difference.

As in case 1's analysis, it is assumed that the system initially is in steady state. At time $t = 0^+$, a sinusoidal signal is applied at node A at a frequency of $\omega_1 + \omega_0$ where ω_0 is the carrier frequency and ω_1 is the modulating frequency. In this

analysis, it is assumed that the local oscillator oscillates at ω_0 . Fig. 3.12a shows the frequency spectrum at node **A**. Assume again like Fig. 3.3 that before $t = 0^+$ the nonlinear par t of the mixer is disconnected. Hence the loop is linear. Node **B**, **C** have have one frequency component at $\omega_1 + \omega_0$ (no other distortion components exist yet). Node **D** has a frequency component at $\omega_1, 2\omega_0 + \omega_1$. Because of filtering node **E** has a component at ω_1. Because of $\omega_1 + \omega_0$ etc. The The amplitudes of these components will be calculated as equation 3.7 So similar to Fig. 3.3b . node **F**'s frequency component has a large amplitude, only this time it is at $\omega_1 + \omega_0$. Again like Fig. 3.3c, node **B** has a frequency component at $\omega_1 + \omega_0$ with a small amplitude (Fig. 3.12b). Now at $t = 0^+$, again the nonlinear part of the mixer switches in and hence when signal at node **B** passes through $f(u)$ it produces harmonic distortion at node **C** (Fig. 3.12c). This signal is then down converted and the frequency spectrum at node **D** is shown in Fig. 3.12d. Node **E** is the filtered signal of node **D**. It consists of only the base band (information) signal (Fig. 3.12e). Node **F** consists of the amplified base band signal and its images because of the sampling nature of the sigma-delta modulator (Fig. 3.12f). Note the switch **S** (which normally is included in the 1-bit quantizer) is deliberately shown here to highlight the sampling operation, which is important in the explanation for the present application (case 2). Images beyond ω_0 are not shown for simplicity. Like Fig. 3.3d, even though the plot has $\omega_1, 2\omega_1$ at baseband, it is different from Fig. 3.3e because signals here are binary represented.

Now in the second iteration, signal at node **F** is fed back and the spectrum at node **B** is changed to Fig. 3.12g. The feedback signal is a single-bit signal and

similar to Fig. 3.8e it passes through the nonlinearity $f(u)$ without generating any extra distortion components. As a result, the output of node **C** is changed to Fig. 3.12h. After mixing and filtering the spectrum at node **E** is updated (Fig. 3.12i), and it is observed that node **E** remains as distorted as in the first iteration (as in CASE 1). Therefore, the distortion in this case is not suppressed as well (same as case 1).

In summary,a 1-bit quantized feedback loop does not suppress distortion originating from a nonlinear element, time varying or invariant, that is placed inside the loop. In the next section a new technique is proposed to overcome this shortcoming.

3.4 A new architecture for a single-bit quantized feedback

The difference between a classical feedback system and a 1-bit quantized feedback system lies in the representation of their feedback signal. From simulations it can be shown that the multi-bit quantized feedback loop does suppresses the distortion produced by the nonlinear components in the forward path. A classical feedback loop can be viewed as an extreme case of a multi-bit quantized feedback loop in which the quantizer consists of an infinite number of levels. Therefore, in a single-bit quantized feedback loop the solution is to convert this single-bit feedback signal to a form with multi-level output.

One approach is to pass the 1-bit signal through a reconstruction filter, which can be either digital or analog. The problem with using a digital filter (Fig. 3.13a) is

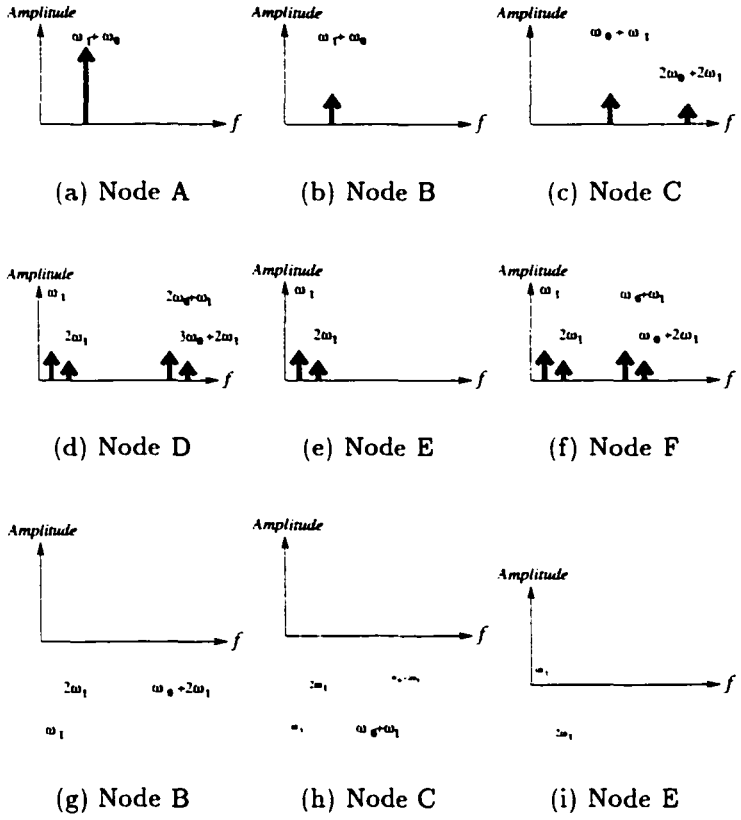


Figure 3.12: Frequency spectrum of the system shown in Fig. 3.11(a). a) Input signal at frequency of $\omega_1+\omega_0$ b) b)node **B** of Fig. 3.11(a)at $t = 0^+$ c) frequency spectrum after the nonlinear component d) frequency spectrum after the ideal mixer e) frequency spectrum of the signal at the output of the loop filter f) frequency spectrum of the output g) frequency spectrum at the input of the nonlinear component h) frequency spectrum at the output of the nonlinear component i)frequency spectrum at the output of the loop filter

that its output is in digital form and a multi-bit digital to analog (D/A) converter in the feedback path is required. This multi-bit D/A converter is a nonlinear component which creates distortion of itself. In order to avoid this problem, an analog reconstruction filter after a single-bit D/A converter is used (Fig. 3.13b).

A single-bit D/A converter is inherently linear and a simple RC analog filter can be made very linear. From simulations a first order analog filter will satisfy the requirement. However. this analog filter produces an extra pole which may affect the stability of the sigma-delta modulator. To prevent this from happening a zero is inserted in the loop (Fig. 3.13c) by adding a direct path from the 1-bit D/A converter output to the input summing node.

3.5 Stability consideration for the new architecture

To investigate the stability of this new architecture. the standard white noise model in s applied to the quantizer in Fig. 3.13c. resulting in Fig. 3.14. where we have a linear system. The signal path in Fig. 3.14 consists of the loop filter and the reconstruction filter. Let us start off by considering the root locus plot of a conventional sigma-delta modulator as shown in Fig. 3.4a. The root locus of this modulator with a second order $H(z)$ is shown in Fig. 3.15a where it is seen that always stays inside the unit circle and thus the modulator is stable. As a comparison shown in Fig. 3.15b is the root locus for the architecture of Fig. 3.13b with the same $H(z)$. It is seen from the plot we have an unstable system. To make the system unconditionally stable, we use the architecture in Fig. 3.13c. Here we make use of the fact that in general if the order of numerator and denominator of the reconstruction filter (designed to be stable) transfer function is equal and the zero of this filter is inside the unit circle then the architecture in Fig. 3.13c in unconditionally stable. As a

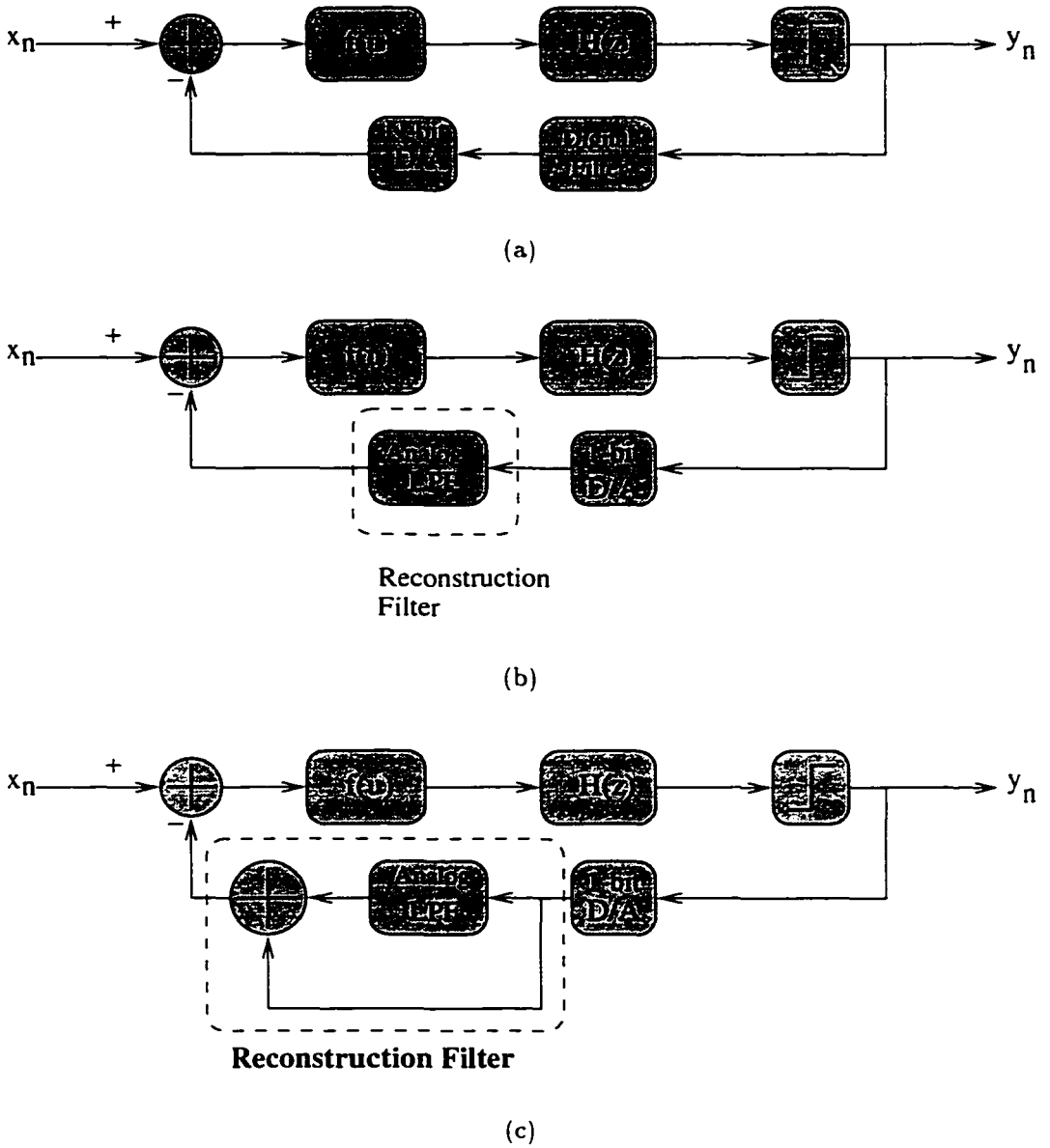


Figure 3.13: A new architecture for sigma-delta modulator to reduce the distortion a)using Digital filter and multi-bit D/A converter in the feedback path b) using single-bit D/A converter and analog filter in the feedback path c) stable architecture with the filter in the feedback path

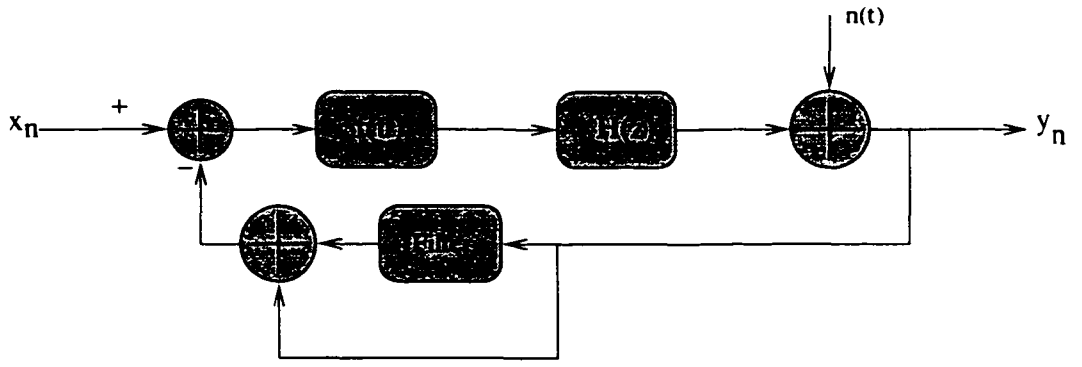


Figure 3.14: White noise model of the new architecture

side note maintaining the same SNR. in our design the poles and zeroes of this filter are selected such that the root locus plot of this new architecture is approximately the same as that of the sigma-delta modulator without the reconstruction filter. The resulting root locus plot is shown in Fig. 3.15c where it is seen to be similar.

3.6 Simulation results

The new architecture can be applied to both case 1 and 2. For both applications requirement and hence design of the reconstruction filter can be the same. Fig. 3.4a and Fig. 3.13c have been simulated. For both figures $H(z)$ is:

$$H(z) = \frac{a - bz^{-1}}{c - dz^{-1} + ez^{-2}} \tag{3.15}$$

in which the coefficients are shown in Table 3.1. $f(u) = u + 0.01u^3$. For Fig. 3.13c the reconstruction filter transfer function is:

$$F(z) = \frac{1 - 0.973z^{-1}}{1 - 0.998z^{-1}} \tag{3.16}$$

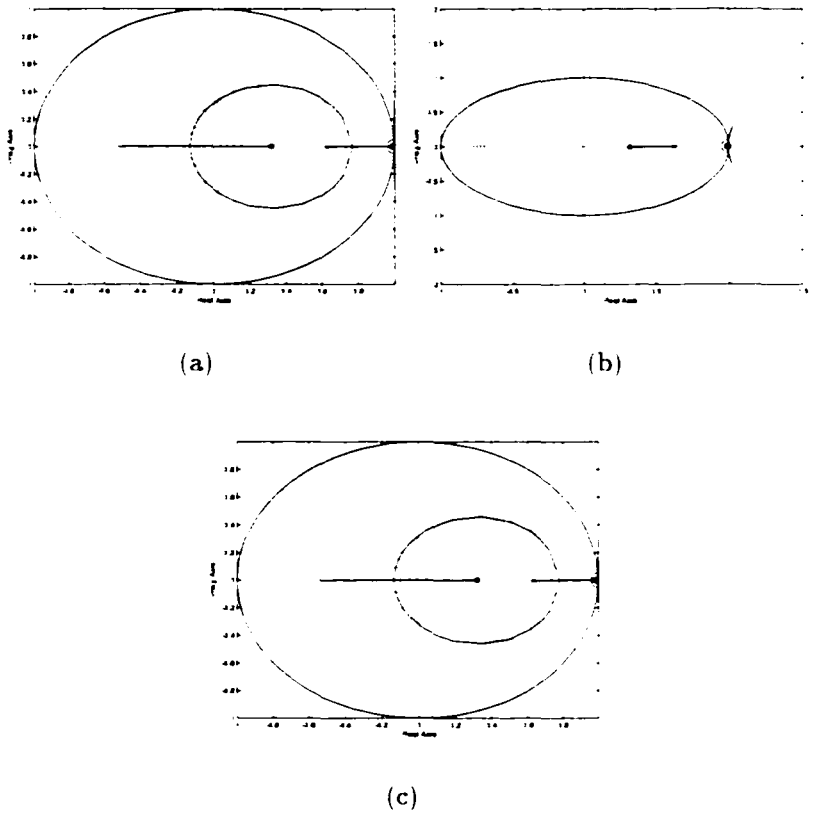
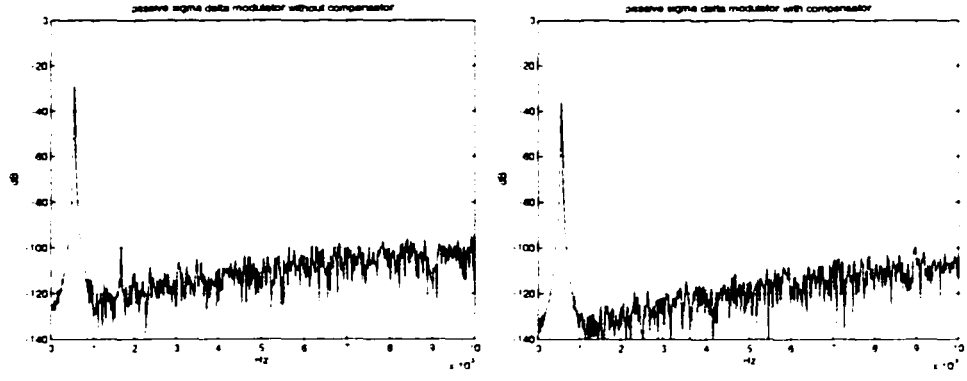


Figure 3.15: The stability issue of the architecture a) root locus plot the original architecture without reconstruction filter b) root locus plot of the architecture in Fig. 3.13b c) root locus plot of the architecture in Fig. 3.13c

An input signal of -30dB at 20kHz are used. Fig. 3.16a shows the frequency spectrum of y_n from Fig. 3.4b and as expected the cubic nonlinearity generates a third harmonic distortion at -70 dB. Fig. 3.16b shows the frequency spectrum of y_n from Fig. 3.13c. As shown the harmonic distortion is reduced to below the noise floor (at least -90 dB). Note even with the same input amplitudes output amplitudes are different because of different loop gain.

Coefficient	Value
a	120.744×10^{-27}
b	38.7×10^{-27}
c	169.28×10^{-24}
d	271.96×10^{-24}
e	104.06×10^{-24}

Table 3.1: The coefficients of the loop filter transfer function



(a) (b)

Figure 3.16: A comparison between the frequency response of the output of the a)new architecture and b) conventional architecture

3.7 White Noise Modeling of the new architecture

In the previous section two applications of the sigma-delta modulator were discussed. The white noise model was not correct for either of the applications because the feedback signal was discrete and it consisted of a limited number of values. In

the new architecture the feedback signal is continuous. As a result, the white noise model should be applied to the new architecture. In the next section, the white noise model for two types of applications of the sigma-delta modulator is discussed.

3.7.1 A white noise model for low frequency applications of the new architecture

In low frequency applications, it is assumed that the S/H circuit is the source of the non-linear characteristic. Fig. 3.14 shows the white noise model. The reconstruction filter is shown as a low pass filter in parallel with a direct path of the output. Regarding the transfer function of the reconstruction filter, $F(z)$ can be modeled as the sum of the filter input and a low pass filter output. As mentioned before the quantized path will not have any effect on the distortion. Therefore, for analysis this path can be removed from the figure. In this analysis, furthermore, only the signal path is discussed; thus, the noise source can also be removed. As a result, Fig. 3.14 is converted to Fig. 3.17. Treating the whole modulator as a non-linear system, the output u can be written in terms of the input signal x as:

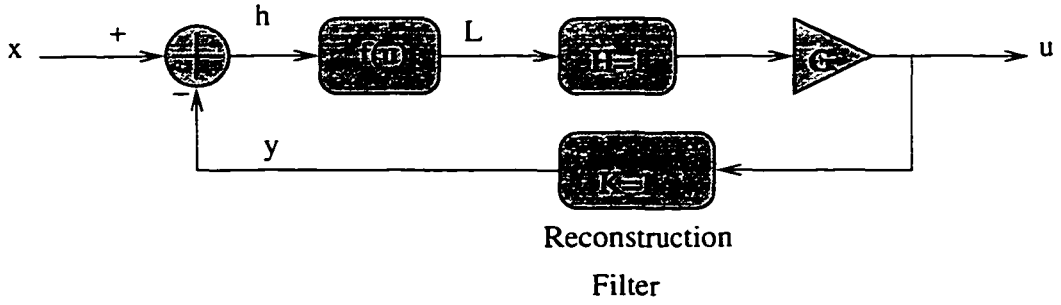


Figure 3.17: A model for the new base-band architecture

$$u = \sum_{i=0}^{n} b_i x^i \tag{3.17}$$

and $y = u$ since $k = 1$. Therefore, the input to the non-linear component $f(u)$ can be written as:

$$h = x - y = (1 - b_1)x - \sum_{i=2}^{n} b_i x^i - b_0. \tag{3.18}$$

and hence, the signal at the output of the non-linear component $f(u)$ can be written as:

$$f(u) = \sum_{j=0}^{m} a_j h^j. \tag{3.19}$$

The output of the modulator u can be written as:

$$u = Gf(u) \tag{3.20}$$

If equations 3.17, 3.18, and 3.19 are substituted in equation 3.20, b_i $(i = 0, 1, 2, \cdots)$, b_i is solved to be:

$$b_1 = \frac{Ga_1}{1 + G_a 1} \tag{3.21a}$$

$$b_2 = \frac{Ga_2}{(1 + Ga_1)^3} \tag{3.21b}$$

$$b_3 = \frac{Ga_3(1 + Ga_1) - 2a_2^2 G^2}{(1 + Ga_1)^5} \tag{3.21c}$$

$$\vdots$$

The above results show that with the reconstruction filter, a quantized feedback system is converted to a classical feedback system. As a result, the distortion of

this quantized feedback system is reduced by the loop gain as was demonstrated in the classical feedback case.

3.7.2 A white noise model for high frequency applications of the new architecture

A model will now be developed for the high frequency architecture in order to prove that the distortion will be suppressed by the feedback in the new quantized feedback system. In this architecture the source of distortion is the mixer placed inside the feedback loop. Fig. 3.18a shows the white noise model of the architecture. The nonlinear mixer has been modeled as a nonlinear component followed by an ideal multiplier (Fig. 3.11(b)). The mixer model with the feedback signal shown in Fig. 3.18b can be simplified to Fig. 3.18c. This will be justified in the following discussion.

Definition Let us assume x_k is a sinusoidal signal at frequency ω_k. For example, x_0 is $\cos\omega_0 t$, x_s is $\cos\omega_s t$, and x_{s+0} is $\cos(\omega_s + \omega_0)t$.

Statement If $x_{k+n}^i x_n^j$ passes through an ideal mixer with Local Oscillator(LO) oscillating at x_k the output can be shown to be x_n^{i+j}.

From Fig. 3.18a and the definition , the feedback signal y can be written as:

$$y = u = \sum_{i=0}^{n} b_i x_0^i \tag{3.22}$$

The input signal is written as x_{s+0}. Therefore, the input to the non-linear compo-

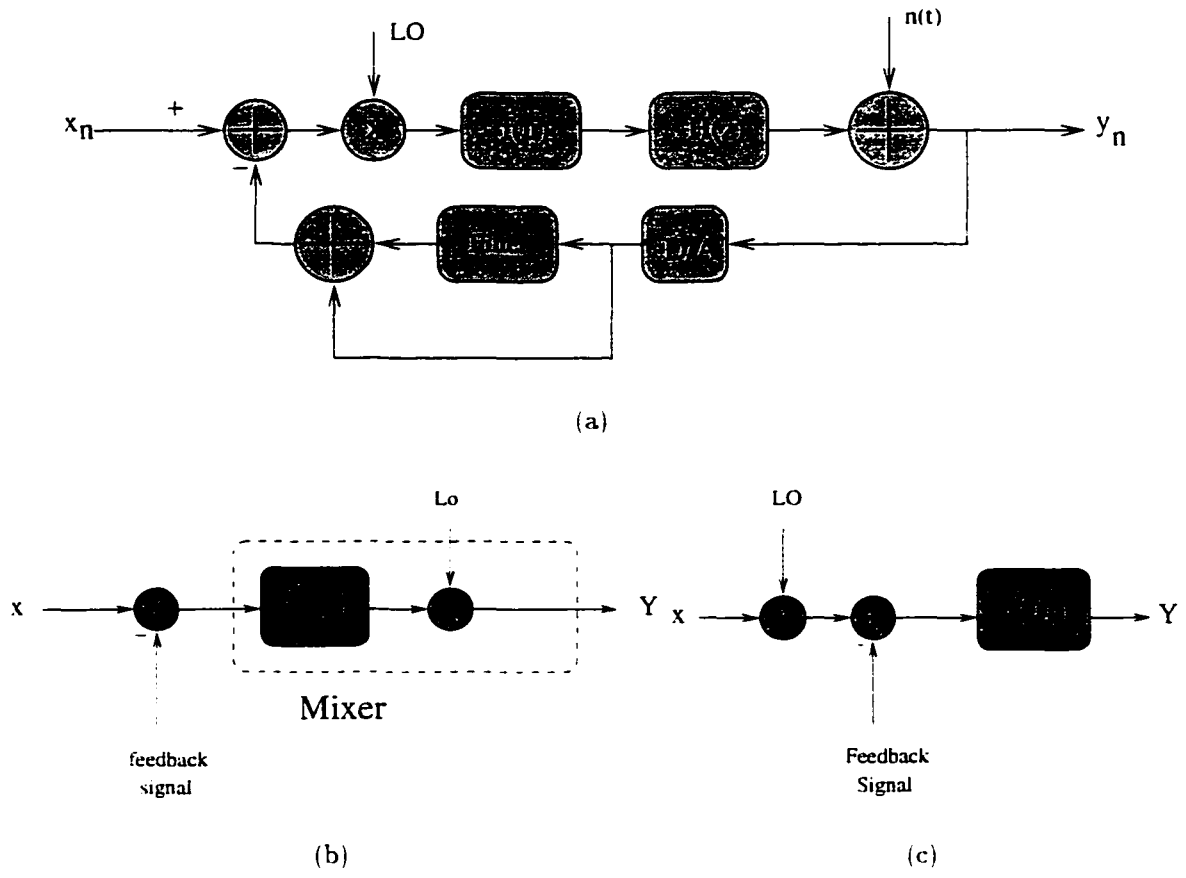


Figure 3.18: a)white noise model of the high frequency architecture b)Mixer model with the feedback c) simplified model of the mixer

nent can be written as:

$$h = (x_{s+0} - \sum_{i=0}^{n} b_i x_0^i) \tag{3.23}$$

and output is as follows:

$$L = \sum_{j=0}^{m} a_j (x_{s+0} - \sum_{i=0}^{n} b_i x_0^i)^j \tag{3.24}$$

Using the statement, the cross terms in equation 3.24 can all be simplified to the baseband component only. Therefore, the non-linear component output can be written as:

$$L' = \sum_{j=0}^{m} a_j (x_0 - \sum_{i=0}^{n} b_i x_0^i)^j \tag{3.25}$$

The above results allow us to simplify the mixer model from Fig. 3.18b to Fig. 3.18c whereby the ideal mixer is moved out of the feedback loop. This justifies why the mixer model in Fig. 3.18b is used in Fig. 3.18c. Substituting the simplified model in Fig. 3.18a and compared with Fig.3.14, it is obvious that the feedback loop for both systems are the same and hence, the high frequency architecture suppresses the distortion just like the low pass modulator architecture.

3.8 Summary

In this chapter, the use of classical feedback and 1-bit quantized feedback loop on distortion suppression were discussed and their differences were highlighted The use of predistortion concept and frequency components cancellation was applied in the investigation.. A new architecture was developed to overcome the inherent limitations in 1-bit quantized feedback loop. The effectiveness of the new architecture was verified by simulations.

Chapter 4

Design of the IF Digitizer

In chapter 2, different types of architectures were discussed and design procedures for two types of oversampled architectures were introduced. Some design steps for an active architecture can also be used for a passive architecture as well. In [5] a complete design procedure of a passive architecture for an IF digitizer is presented. Nevertheless, this design procedure is for the conventional architecture and cannot be completely applied to the proposed architecture introduced in chapter 3. High frequency IF Input for the proposed architecture would not leave any other choice except adding the signals (input and feedback) in continuous time; whereas, other parts of the architecture can be realized in either discrete time or continuous time circuits.

In this chapter, design issues of the new architecture will be described and a design example for all of the existing block in the architecture will be introduced. The design examples are used to implement the architecture in two types of technology: BICMOS and CMOS. In this chapter, the adder circuit whose linearity

and frequency response is crucial to the performance of the architecture will be discussed first. Then the design of the passive loop-filter for the required application will be explained. Thirdly the reconstruction filter design will be investigated. The low-noise comparator design will be discussed next. Finally, the design of the sampling mixer will be explained.

4.1 Adder Design

A switched capacitor sigma-delta modulator incorporates a two phase clock to sum or subtract the signals from one another. At low frequencies this technique is very useful because of the high sampling rate: whereas, at IF frequency this technique may not be useful because the S/H circuit in a switched capacitor architecture becomes a sampling mixer for an IF frequency. Thus the IF signal is down converted and then is summed or subtracted from the feedback code. Consequently, the mixer is automatically placed outside the feedback loop. On the other hand, in continuous time domain circuits, the summing function is usually performed by an operational amplifier. As a result, the maximum input frequency is limited by the bandwidth of the operational amplifier.

The IF digitizer developed in chapter 3 consists of a mixer within the sigma-delta modulator loop. Therefore, the two phase clock technique can only be used if the sampling frequency is many times higher than the input frequency. On the other hand, frequency response of the operational amplifiers (opamp) prevents the signals to be added/subtracted at high frequency. High frequency opamps consumes more power. Therefore, the overall power of the system will increase.

However, the only solution for adding/subtracting high frequency signals is the continuous time approach. The performance of this summer/subtracter in this architecture is very critical because it is the first element that the high frequency signal is passing through. Any nonlinear characteristics in the summing function produces distortion which cannot be improved by any means. As a result, a very high frequency, highly linear summer is required. Two types of approaches can be used to sum two signals: summing currents and summing voltages. There are advantages and disadvantages in using any of these techniques. In this section, the advantages and disadvantages of these approaches is described and a proposed summer circuit for each technique is presented.

4.1.1 An Adder Design Using a Current Approach

Summing currents is very simple. The current of a branch at any node on that branch is total of the currents passing through other branches which have a common intersection with the first branch. Fig. 4.1 illustrates a simple current summing.

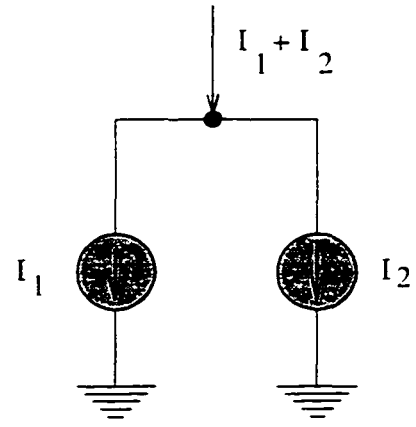


Figure 4.1: A simple summing feature in the current domain

As shown in Fig. 4.1. the output current is equal to total of the current source values. These current sources represent a current or a transconductance amplifier. In spite of the simplicity. this technique suffers from the nonlinear behavior and the frequency response of the current sources.

In any digital radio architecture. the radio frequency (RF) signal is passing through a band-pass filter . a low noise amplifier. one or two mixer stages with their band-pass filter before the signal reaches the digitizer. In any of the above mentioned architecture. the RF signal can be converted to current. However. getting an undistorted signal is difficult. If the signal at IF stage is still voltage. to sum the signals in current. the IF signal has to be converted to current. Therefore. a highly linear voltage to current converter (VIC) is required. The most linear reported circuits [1.38–44] have a total harmonic distortion(THD) of 0.5% which is equal to 60dB of distortion. The amount of distortion depends on the input signal amplitude. Ignoring the frequency response. a highly linear VIC with 0.1 volts input is realizable.

After summing the signals in current. the signal might be used as current in continuous time circuits or converted to voltage in discrete time circuits. The latter case requires a current to voltage converter (IVC) circuit whose linearity is not very crucial but its power consumption is an issue.

Summer output swing is another issue for which a designer should take care of. Maximum summer output swings dependent on the number of inputs. Assume A is amplitude (either input or output). N is a number of inputs and g is gain of VIC.

The output amplitude in current can be written as:

$$A_{MAX} = N \times g \times A_{IN_{MAX}}. \tag{4.1}$$

Provided the total signal is used as voltage, the IVC must be able to convert this current without adding too much distortion. To design a MOS with VIC, two types of biasing region can be used: Biasing the input transistor in linear region or saturation region.

4.1.1.1 Linear Region Technique

A MOS transistor VI characteristic in the triode region is proportional to the input voltage, provided that V_{DS} of the transistor is kept constant and is very small (first order approximation). Fig. 4.2 shows a schematic of a circuit in which the input transistor is biased in the triode region [1].

In Fig. 4.2, $I_2 > I_1$. If both transistors M_3 and M_4 have same size and are biased in saturation, the configuration of $M_2 - M_4$ can keep the variation of V_{DS_1} around 2 mV for an input range of $\pm 3V$ and a power supply of $\pm 5V$ in a first order approximation. However, including the mobility degradation in the analysis will increase the variation which causes more distortion.

Using Fig. 4.2 circuit in a differential configuration, even harmonics in a fully matched circuit are eliminated. However, the circuit common mode gain is huge and any mismatching produces huge second harmonic distortion.

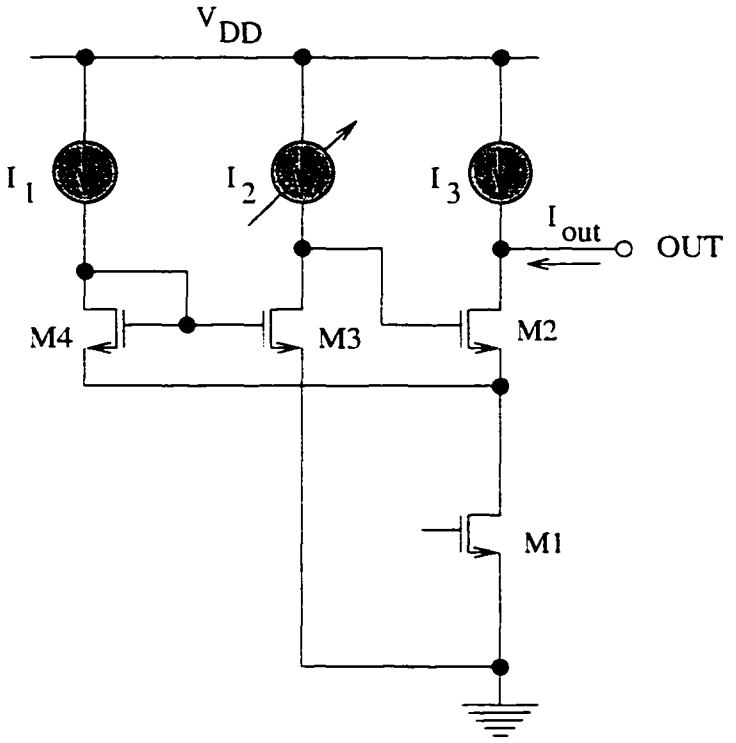


Figure 4.2: A Linear Voltage to Current Converter Whose Input Transistor is in The Triode Region [1]

4.1.1.2 Saturation region technique

Biasing the input transistor in saturation region (M_2. M_4 in Fig. 4.3). a linear VIC circuit in the first order approximation can be developed [43. 44] with fully differential architecture.

The difference of the output currents is linearly dependent on the difference of the input voltages. Although.the linear relationship does not hold when the input transistor enter weak inversion region due to large input signals.

In the first order approximation without body effect and channel length modu-

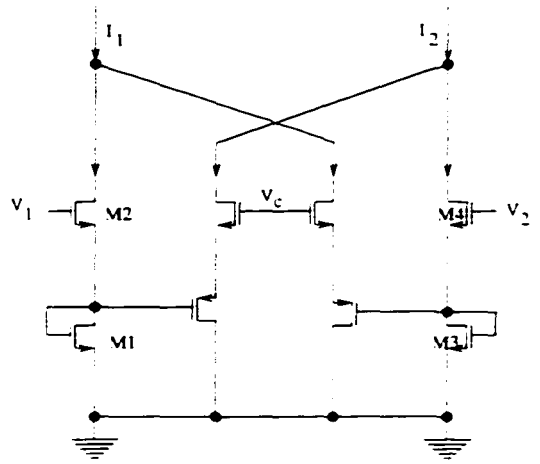


Figure 4.3: A linear composite MOSFET voltage to current converter

lation effect. the output current can be written as:

$$I_2 - I_1 = K(V_c - 2V_{TN0})(V_2 - V_1). \tag{4.2}$$

Equation 4.2 shows that any mismatching in the two side of the circuit will eliminate the linearity. The linear technique compared with the saturation technique is preferred because the input swing can be larger. In the next section a design based on linear technique will be presented.

4.1.1.3 Circuit Design for a Voltage to Current Converter

Fig. 4.2 has common mode problem and V_{DS} variation is large. $(M_2 - M_4)$ configuration is a feedback configuration whose open-loop gain is not large. Fig. 4.4. has solved this problem. A differential configuration with current source is used to decrease the common mode gain. To decrease V_{DS} variation an opamp is use

whose inputs are drain and source to the input transistors. To improve the circuit performance the schematic shown in Fig. 4.4 was used.

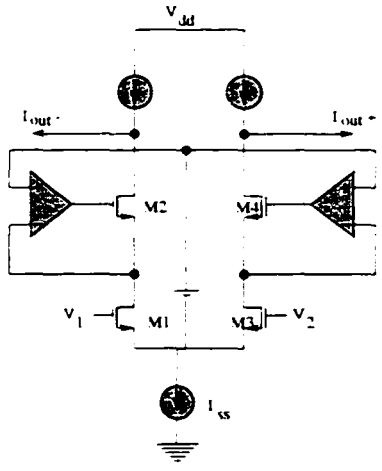


Figure 4.4: The designed circuit schematic for Voltage to current converter

The original idea of this circuit was first introduced in [45]. The battery in Fig. 4.4 can be realized by duplicating M_1, M_2, and the current source. This technique can reduce the variation of V_{DS} by the loop gain of the opamp.

This opamp is a differential pair (Fig. 4.5) with active load.whose input offset can be compensated by the battery value (shown in Fig. 4.4). However, the offset should be minimized.

In [46] two types of offsets have been defined for active loads, a DC systematic offset and a random offset. The DC systematic offset is due to the difference between the two outputs in a differential pair where the both inputs are connected to a common ground. This type of offset can be expressed as:

$$V_{OSS} = \frac{V_{out} - V_{D_{52}}}{2}\left(\frac{V_{GS_5} - V_{TP}}{L_6 V_{EP}} - \frac{V_{GS_1} - V_{T_n}}{L_3 V_{E_n}}\right) \tag{4.3}$$

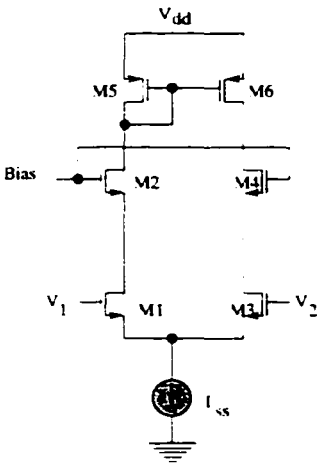


Figure 4.5: The gain block used for the linear VI converter

Where $V_{D_{52}}$ is the voltage between the drains of M_2 and M_5 in Fig. 4.5, and V_{E_N} or V_{E_p} is the Early voltage of a MOS transistor.

The random offset is created by mismatching among components of both sides of the differential pair shown in Fig. 4.5. Threshold voltage and body factor, whose value depends on bulk doping and oxide thickness are the source of mismatching. In addition, the gain factor whose value is dependent on size, mobility, and oxide thickness can also cause mismatching. The random offset can be explained as:

$$V_{osr} = V_{os13} + \frac{V_{GS1} - V_T}{V_{GS5} - V_T}\Delta V_{T56} + \frac{V_{GS1} - V_T}{2}\left(\frac{\Delta K_{13}}{K_{13}}\right) + \frac{V_{GS5} - V_T}{2}\left(\frac{\Delta K_{56}}{K_{56}}\right) \quad (4.4)$$

in which K_{ij} is an average gain factor between transistor M_i and M_j, and V_{os13} is the offset between M_1 and M_3. To have maximum linearity the random offset has to be minimized. For the differential pair, V_{os13} and ΔV_{T56} can be minimized by careful layout. By choosing width and length of a MOS transistor larger than the minimum size, the gain factor mismatching is reduced. Nevertheless, transistors with large

width introduce non-uniform threshold voltage along the gate. Therefore, large transistors are made of parallel transistors with the same size. Assume N transistors with length L and width W are connected in parallel(Fig. 4.6). The equivalent mismatch can be expressed as:

$$\Delta K_{eq} = N\Delta K_1 \tag{4.5}$$

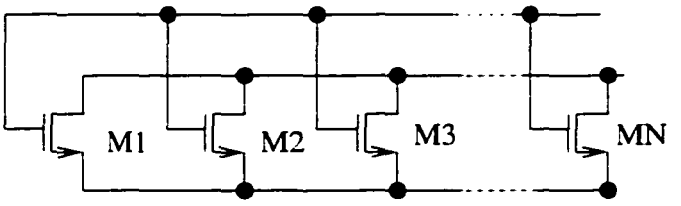


Figure 4.6: N parallel transistor

Assuming the oxide thickness is same for all transistors. ΔK_1 can be expressed as:

$$\Delta K_1 = (\frac{W + 2\Delta W}{L + 2\Delta L} - \frac{W}{L})K_1' \tag{4.6}$$

ΔW is the mismatch in width in terms of minimum width and ΔL is the mismatch in length in terms of minimum length. For example, for a transistor with 10 μm width and $0.8\mu m$ length, in a 0.8 μm technology in which the minimum length is $0.8\mu m$ and minimum width is $1.4\mu m$ with 5% mismatching the tolerance for the length and width are $0.04\mu m$ and $0.07\mu m$ respectively. Therefore,

$$\frac{\Delta K_1}{K_1} = \frac{\frac{W+\Delta W}{L-\Delta L} - \frac{W-\Delta W}{L+\Delta L}}{\frac{W}{L}} = \frac{\frac{10.07}{0.76} - \frac{9.93}{0.84}}{\frac{10}{0.8}} = 0.114 \tag{4.7}$$

If the width is chosen as $20\mu m$ instead of $10\mu m$ the mismatching is equal to 0.107. The above example shows that the larger the length and the width, the less the percentage mismatch. As shown above by using minimum length for high frequency input and large width for high gain, the minimum mismatching due to the size will be close to the length variation. To have low random offset, with minimum length restriction, the biasing current should be small.. Simulation results show that the maximum acquirable linearity is 80dB with a 0.2 volts input signal.

4.1.2 Voltage Summing

Fig. 4.7 shows a typical summer in the voltage domain at low frequency. In fact, an opamp provides the required gain to have an ideal summer with unity gain. Using the superposition technique the voltage at the non-inverting input of the operational amplifier can be written as:

$$V_A = \frac{(V_1 + V_2 + \ldots + V_N)}{N} \tag{4.8}$$

The inverting input is not used as summing point because the feedback resistor has loading effect on the input sources. The feedback circuit provides the required gain so that the output has a unity gain. The above equation shows that the summing operation is introduced by the resistors only and the opamp provides the gain.

If unity gain is not required, the opamp can be removed. In a switched capacitor sigma-delta modulator, the first capacitor introduces an equivalent resistive function in case of the continuous time circuit. Provided the equivalent resistor value is much larger than any of the summing resistors, is not too much and can

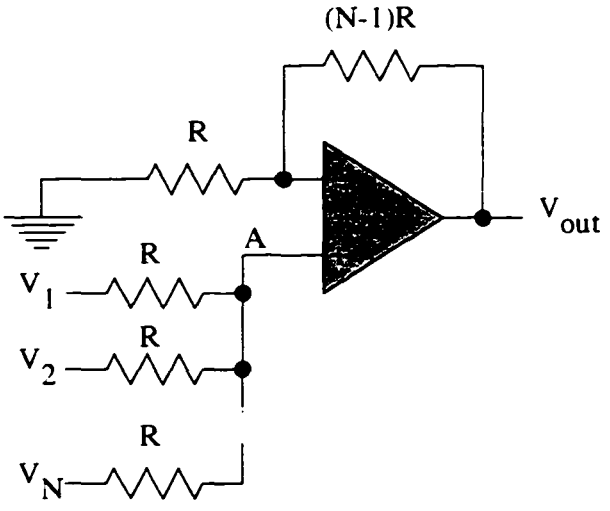


Figure 4.7: An analog adder using operational amplifier to sum the signal in Voltage domain

be ignored. Despite the small loading effect, the linearity of this summer depends on the resistor linearity. In current technologies, a highly linear resistor are available. Simulation results show that the summer gain effect is only 4dB which can be tolerated.

4.2 Loop Filter Design

Unlike an active sigma-delta modulator, a passive sigma-delta modulator performance is dependent on the comparator noise, quantization noise and thermal noise. To minimizer the comparator noise and quantization noise, loop filter pole locations are important [16, 17]. The original passive sigma-delta modulator model is shown in Fig. 4.8. Two sources of noise have a huge influence on the passive architecture performance:quantization noise and comparator noise. The thermal noise can be minimized by the capacitor values. The comparator noise is an important issue in

this architecture because the loop filter does not introduce any gain and the loop gain depends on the comparator gain.

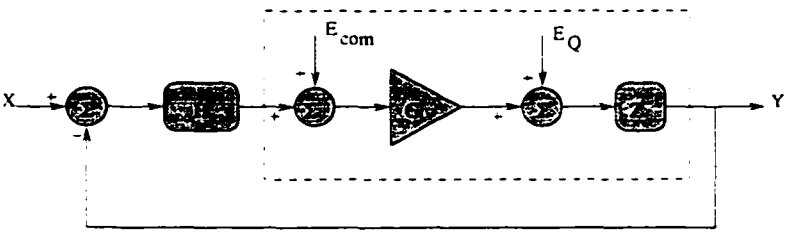


Figure 4.8: A passive sigma-delta modulator with a linear quantizer model

The filter pole locations shape both types of noise. But, each of them passes through a different transfer function. The output of the sigma-delta modulator in terms of the linear model input can be written as [16]:

$$Y = X + \frac{E_Q}{GH} + \frac{E_{com}}{H} \tag{4.9}$$

In which X, E_Q, and E_{com} are the input, quantization noise, and comparator noise respectively. If the pole locations are chosen too low, the comparator noise dominates. On the other hand, if the pole locations are chosen too high, the quantization noise dominates. Fig. 4.9 shows the effect of the pole locations on the noise spectra of each components [16].

To design a loop filter, the optimum point for the pole location has to be selected. If the two noise sources are added together, the graph would have a global minimum, which occurs when both noise sources, (i.e. comparator noise and the quantization noise) are equal. If the loop filter has a zero at 7.5MHz and comparator noise is 14 nV/$\sqrt{Hz}$ the poles frequency for 200kHz bandwidth must be approximately

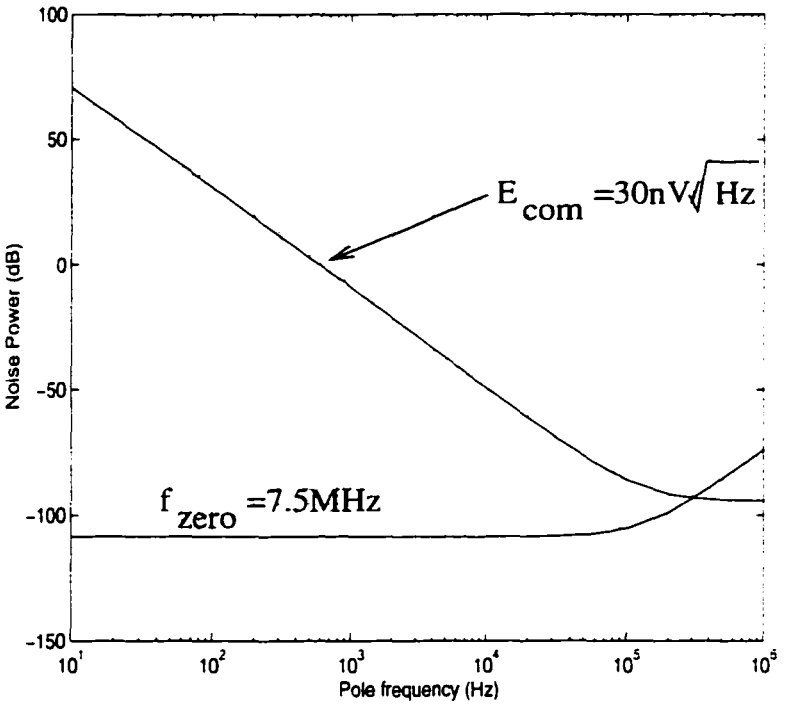


Figure 4.9: Baseband quantization noise and comparator input noise versus frequency(2 identical poles)

180kHz. [16] has assumed that the second order RC filter shown in Fig. 4.10 has two equal poles provided that two first order RC filters do not have any loading effect on one another. However, this assumption is not correct because the second stage RC circuit has loading effect on the first stage. Simulation results show that this effect is less than 3dB [16]. The values of resistors and capacitors for the loop filter shown in Fig. 4.10 are shown in Table 4.1 in the case of equal poles.

In the new architecture, a continuous time summer is used. As a result the delay shown in Fig. 4.8 is not required. Two methods can be used to realize the resistor in switched capacitor circuits: shunt and series [47]. Both of these are shown in Fig. 4.11.

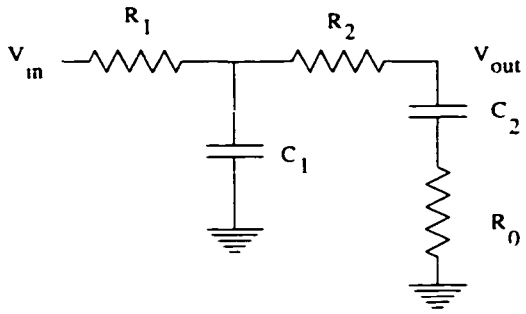


Figure 4.10: Continuous time schematic of the loop design

RC version	SC version
$R_1 = 25k\Omega$	$C_{R_1} = 0.4pF$
$C_1 = 21.22pF$	$C_1 = 21.22pF$
$R_2 = 100k\Omega$	$C_{R_2} = 0.1pF$
$C_2 = 5.3pF$	$C_2 = 5.3pF$
$R_0 = 4k\Omega$	$C_{R_0} = 2.5pF$

Table 4.1: Parameters of RC passive loop filter and its equivalent switched capacitor value at $f_S = 100MHz$

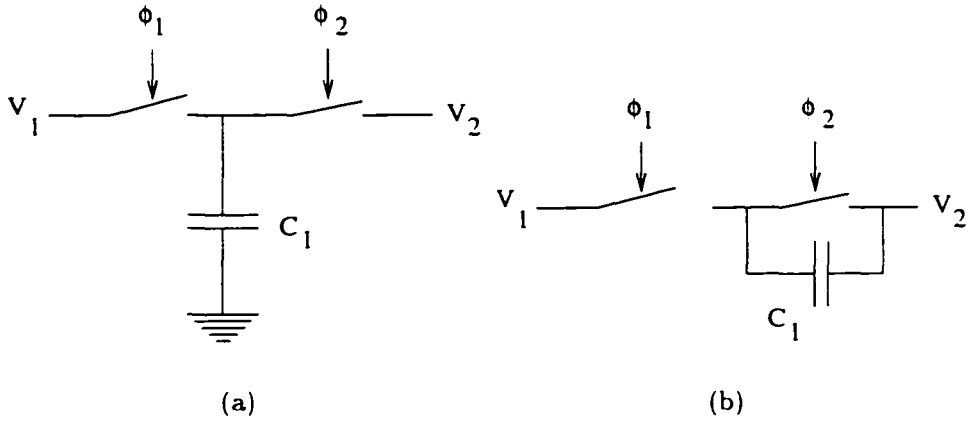


Figure 4.11: Resistor realization in switched capacitor circuits a) Shunt b) Series

Coefficient	Value
a	120.744×10^{-27}
b	-38.7×10^{-27}
c	169.28×10^{-24}
d	-271.96×10^{-24}
e	104.06×10^{-24}

Table 4.2: The coefficients of the loop filter transfer function

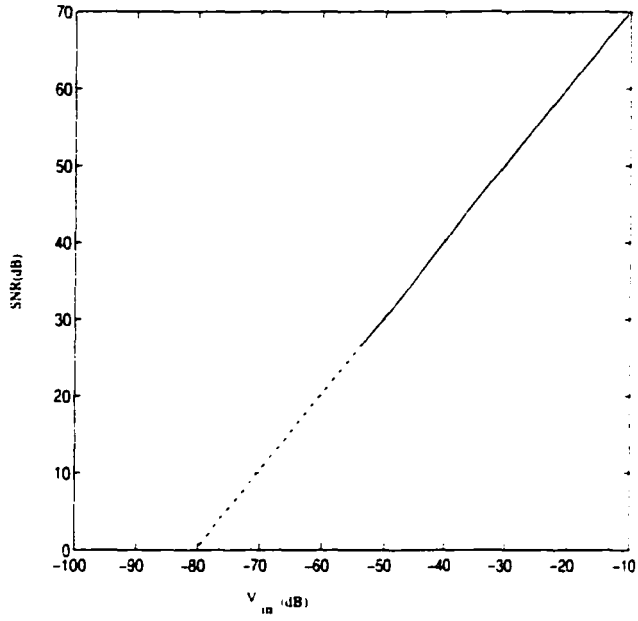


Figure 4.12: Dynamic range of the designed system in simulation

To remove the extra delay from the circuit, the series architecture is used. The coefficients of the loop filter transfer function are shown in Table 4.2:

Simulation results show that the dynamic range is about 72 dB. Fig 4.12 shows the theoretical dynamic range of the system with the designed loop filter.

The loop filter circuit is shown in Fig. 4.13.

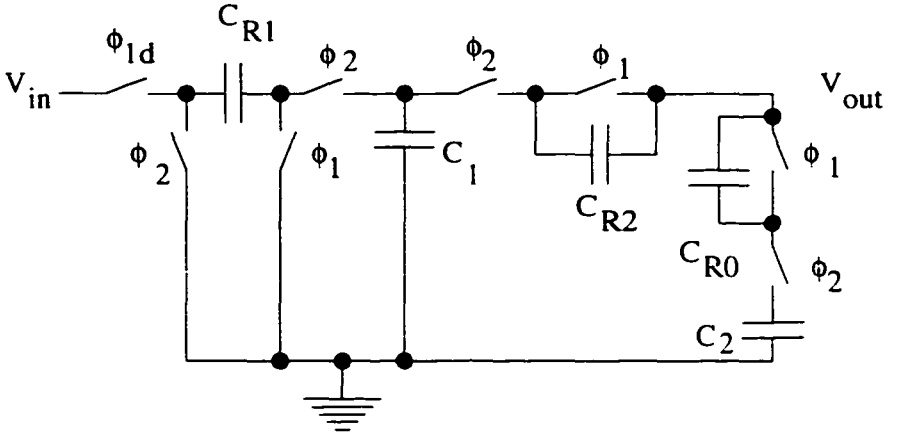


Figure 4.13: Schematic of the loop filter

4.3 Reconstruction Filter Design

As mentioned in the previous chapter, the new architecture has a reconstruction filter in the feedback loop to reduce the distortion. Two issues have to be considered in this filter: bandwidth and linearity. As mentioned before the bandwidth of the filter is not important as long as the noise power at the output of the filter due to the one-bit input signal is not more than that of the reconstructed signal. A large bandwidth reduces the effect of the reconstructed signal on reducing the distortion. On the other hand, a small bandwidth filter does not reconstruct the one-bit signal properly and hence the suppression of the distortion will reduce. The linearity is also important because any nonlinear effects in this filter will be propagated to the output without any suppression.

The order of a filter specifies its transition bandwidth. Before talking about the

transition bandwidth, the bandwidth of the filter has to be defined. Since this architecture is based on a low-pass sigma-delta modulator, the maximum information in a one-bit code at the output of the converter is dependent on the bandwidth of the loop filter. It is required to reconstruct this information and feed it back to the input. Therefore, the minimum bandwidth for the reconstruction filter is the signal bandwidth of the sigma-delta architecture.

Choosing a larger bandwidth will feed larger amount of quantization noise to the input of the sigma-delta modulator. However, the distortion, generated in the forward path, will be fed to the sigma-delta modulator input without any attenuation. To optimize the noise power as well as the amount of distortion fed back to the input, the distortion and noise will be compromised by selecting a large transition bandwidth. As a result the first order filter will be enough to reconstruct the filter. Since reconstruction filter is employed to increase the distortion at the input of sigma-delta modulator, the small band width will attenuate the distortion. This may not suppress the nonlinear effects. Therefore, the bandwidth of this filter is chosen slightly larger than that of the sigma-delta architecture. Next, the linearity of the filter will be investigated.

4.3.1 Linearity of The Reconstruction Filter

Since the reconstruction filter is a first order filter it can be designed using either continuous time circuits or switched capacitor circuits. The nonlinear characteristic of the switches in the switched-capacitor circuit will produce distortion at the output of the filter. On the other hand, continuous time filters can be used to

realize the reconstruction filter. a passive architecture like RC filters can solve the problem.

Realizing a linear resistor and a capacitor in current technologies is possible.As a result. a highly linear filter is realizable. However. the input signal to this passive filter is a single-bit code which is applied by one or two MOS transistors (Fig. 4.14). A single-bit code is inherently linear. but if it is connected to a RC filter the nonlinear characteristic of the switch will affect the linear behavior of the RC filter. The MOS switches are used in both approaches (switched-capacitor circuits and RC filters) so their nonlinear behavior will appear at the output of the circuit.

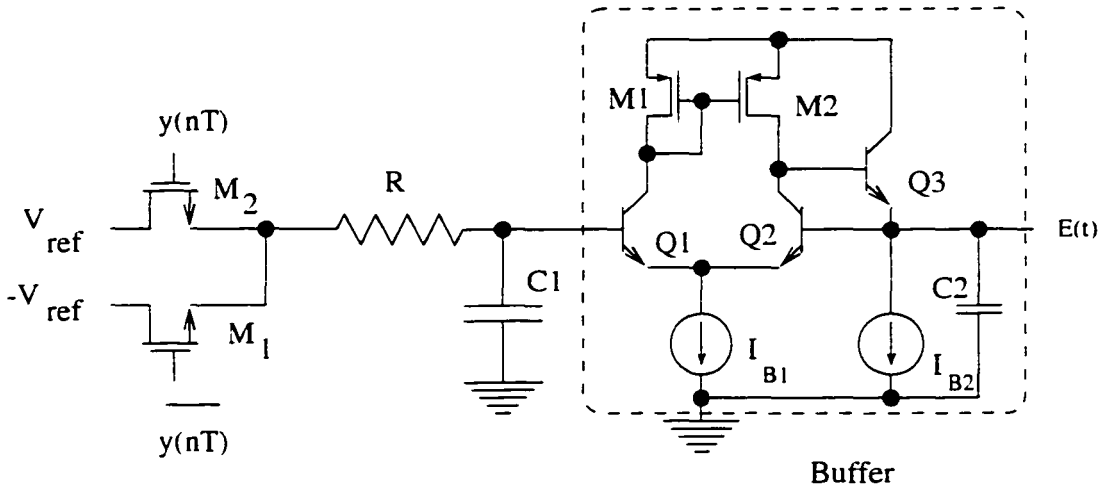


Figure 4.14: Reconstruction filter with MOS switches

If the resistor of the MOS switch is less than 1% of the resistor value of the filter. the distortion is approximately 1%. For example. suppose the resistor in the RC filter is 10kΩ and the switch sizes are chosen such that $\frac{W}{L} = \frac{200}{0.6} = 166.7$. In 0.5 micrometer CMOS technology. the resistance of the switches will be calculated to be 150Ω which is approximately 1.5% of the resistor in the RC filter. System

level simulation results shows that 1% distortion does not affect the output of the architecture performance.

A single-ended schematic of the proposed architecture is shown in Fig. 4.15. Two types of summers were presented in the previous section. The voltage summer was operating with resistors. Resistive load affects the function of reconstruction filter. To avoid this problem, a buffer is required. To reduce the sensitivity to the load and to isolate the filter from the summer as shown in Fig. 4.15: whereas the current summing does not require the buffer because the loading effect is capacitive and it would slightly affect the frequency response of the reconstruction filter. For voltage summing, a design of a unity gain buffer is explained in the following section.

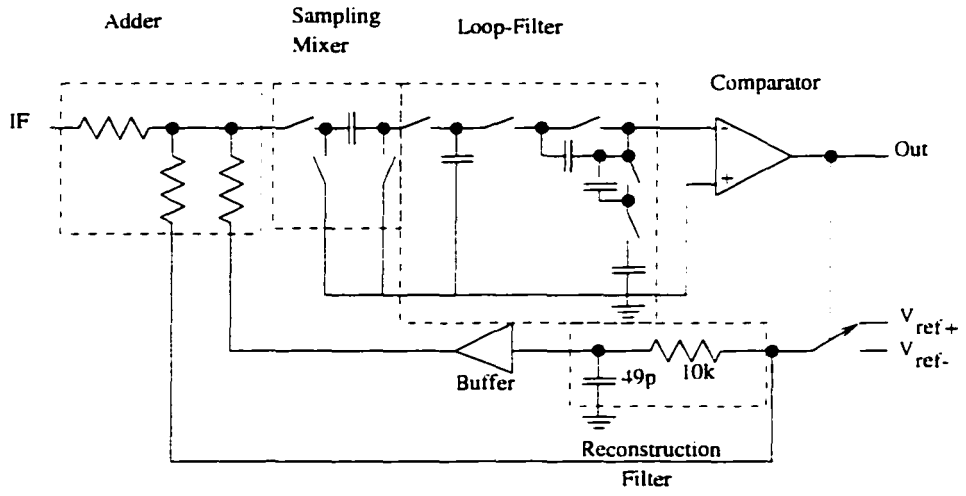


Figure 4.15: A single-ended schematic of the proposed architecture

4.3.2 CMOS Buffer Design

Using the technique discussed in [45], a buffer has been designed whose linearity is approximately 80dB for a 0.3 volt input. Fig. 4.16 shows the schematic of the

buffer.Transistor sizes are shown in Table 4.3

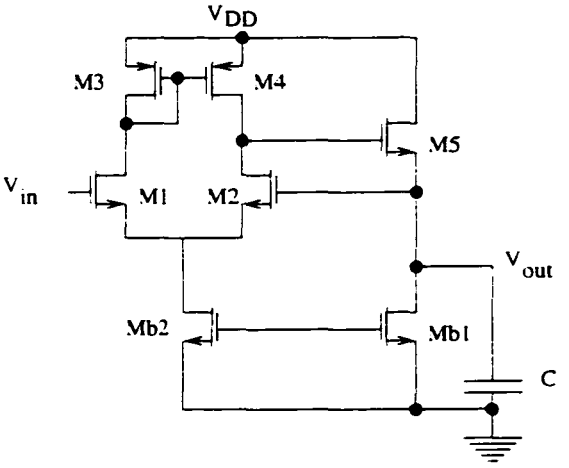


Figure 4.16: Linear Unity gain buffer

Transistor	$\frac{W}{L}$
M_1	$\frac{100}{1}$
M_2	$\frac{100}{1}$
M_3	$\frac{200}{6}$
M_4	$\frac{200}{6}$
M_5	$\frac{400}{0.6}$
M_{b_1}	$\frac{265}{1}$
M_{b_2}	$\frac{20}{1}$

Table 4.3: Transistors size in Buffer

The output current source value is chosen to be 0.8 mA because at the output of this buffer a resistor belonging to the summer (Fig. 4.15) is connected. Three inputs that are added: a high frequency input signal. a reconstruction filter output signal. and a one-bit code signal. The maximum amplitude of each signal is 0.3 volts. As a result. the worst case voltage drop across the resistor at the output of

the buffer shown in Fig. 4.17 is 0.4 volts which means the current passing through the 1k resistor is 0.4 mA. Therefore the output transistor is still in strong saturation region. The distortion due to the source follower and the differential amplifier is reduced by the feedback. The open loop gain of the differential amplifier can be calculated as [48]:

$$A_v = \frac{g_{m_1}}{g_{o_2} + g_{o_4}} \tag{4.10}$$

Therefore the gain will be 113 with a drain current of 13.2 μA. The output capacitor is used to bypass the high frequency signals to ground. The high frequency signals are due to the high frequency IF signal, one-bit code signal, and spikes created by the sampling mixer. The third harmonic distortion of this amplifier with loading effect for 0.2 volts input is -90dBc.

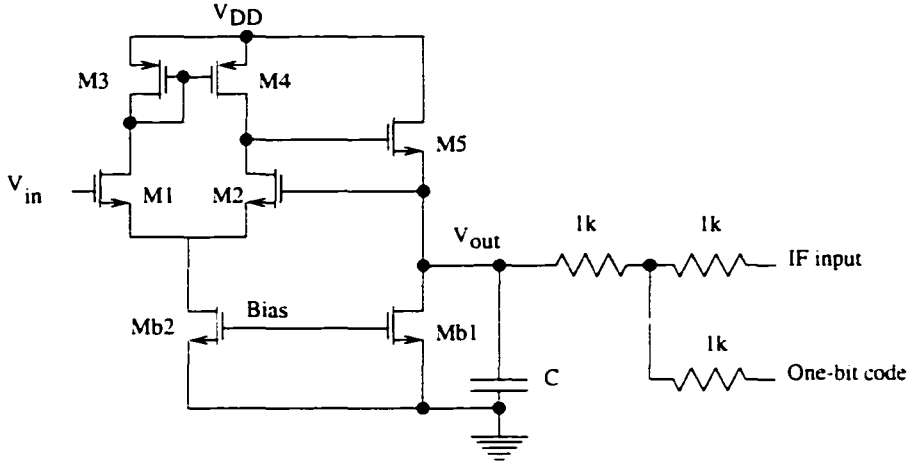


Figure 4.17: Linear Unity gain buffer with the voltage adder

4.3.3 BICMOS Buffer Design

In the case of BiCMOS technology, a BiCMOS buffer was designed to achieve more open-loop gain. Fig. 4.18 shows the schematic of the BiCMOS buffer.

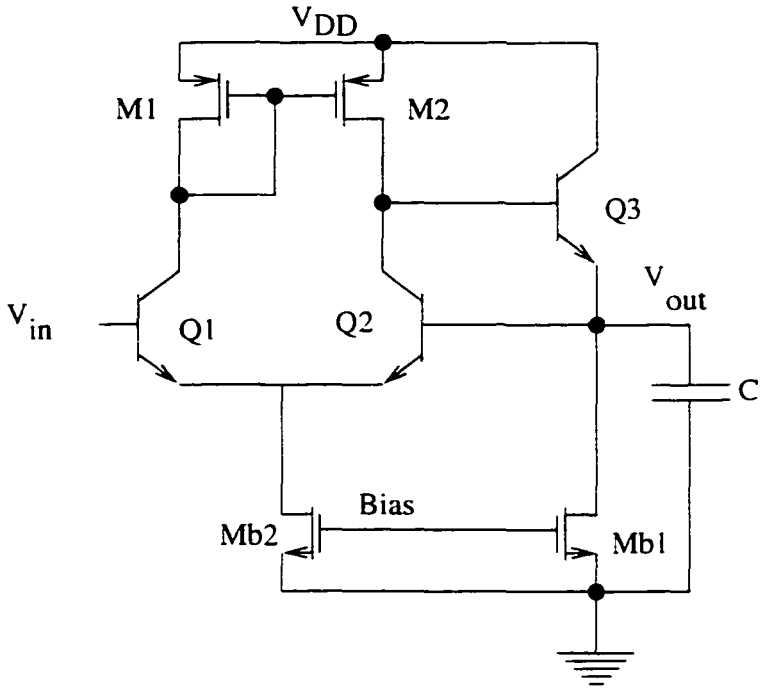


Figure 4.18: Schematic of a buffer in the BiCMOS technology

The open-loop gain of the circuit can be written as:

$$A_v = g_{m_1}(r_{o_{Q_2}} || r_{o_{M_2}} || r_{in_{Q_3}}) \tag{4.11}$$

Q_3 in Fig. 4.18 is biased at 1.3mA and the differential pair is biased at $30\mu A$. The open-loop gain including the input resistance of Q_3 is 985 and the distortion is 96dB with the loading effect for 0.4 volts input. The capacitor at the output bypasses the high frequency signals due to the summer effects.

4.4 Comparator Design

The summer and the loop-filter have already been designed. comparator is the third part of the architecture. The most important issue in this comparator is its noise with which degrades the passive sigma-delta modulator performance. In this section. two types of comparators in two different technologies are described.

4.4.1 CMOS Comparator

In the CMOS design Robert's structure. [49] is employed (Fig. 4.19).

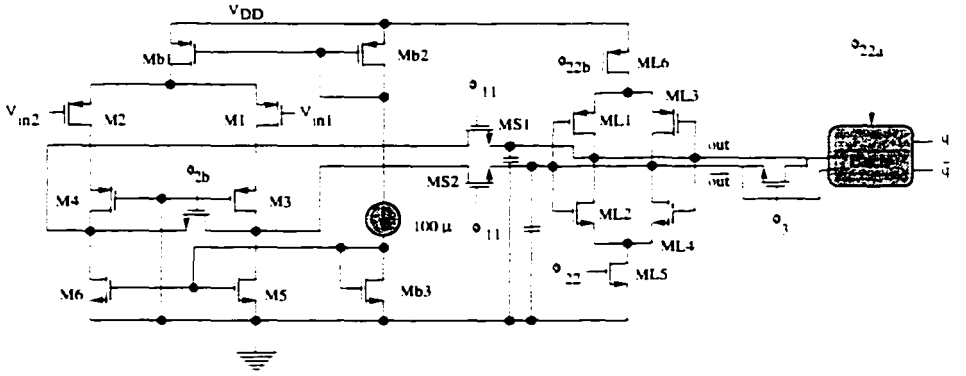


Figure 4.19: Schematic of A low noise CMOS comparator used in IF digitizer

As shown in Fig. 4.19. the comparator consists of two parts. The first part is a pre-amplifier and the second part is a dynamic latch. There is another part in the figure that converts the dynamic output to a static output. The noise of the comparator is due to the pre-amplifier circuit. The comparator noise can be written as [16]:

$$E_{com}^2 = \frac{8kT}{3}\left\{\frac{1}{g_{m_1}} + \left(\frac{g_{m_3}}{g_{m_1}}\right)^2 \frac{1}{g_{m_3}} + \left(\frac{g_{m_5}}{g_{m_1}}\right)^2 \frac{1}{g_{m_5}}\right\} \tag{4.12}$$

The current of the differential pair in the CMOS pre-amplifier is selected to be $100\mu A$ and the size of the input transistor is optimized for minimum noise [16]. Therefore the input noise for the comparator is estimated to be $4.1\text{nV}/\sqrt{Hz}$ and the simulation verifies this.

Power consumption of the comparator is due to two parts of the circuit: the pre-amplifier and the dynamic latch. The total bias current of the pre-amplifier is $I_{bias} = 200\mu A$. Consequently, the power consumption of the pre-amplifier, $I_{bias}V_{DD}$, can be written as:

$$P_{preamp} = I_{bias}V_{DD} = 200\mu \times 3.3 = 0.66mW. \tag{4.13}$$

The dynamic latch requires a capacitor at the input to store the output of the pre-amplifier, therefore in the regeneration phase the latch output will be in the right direction. The comparator requires a specific timing for the clock. The clock scheme is shown in Fig. 4.20.

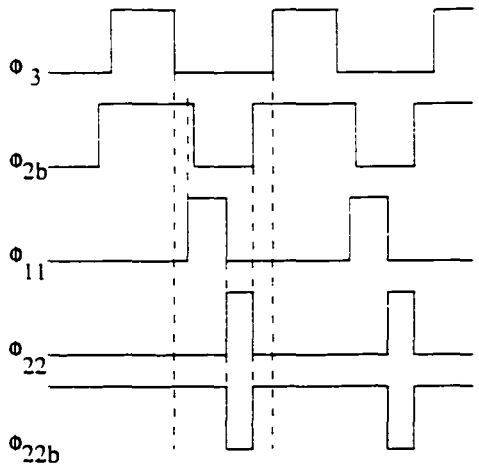


Figure 4.20: The timing schedule for the CMOS comparator

Transistor sizes are given in Table 4.4.

PMOS	Size	NMOS	Size
M_1, M_2	$\frac{460}{0.6}$	M_5, M_6	$\frac{60}{6}$
M_3, M_4	$\frac{20}{0.6}$	M_{b_3}	$\frac{60}{0.6}$
M_{b_2}	$\frac{10}{1}$	M_{s_1}, M_{s_2}	$\frac{5}{0.6}$
M_{b_1}	$\frac{20}{1}$	M_{L_2}, M_{L_4}	$\frac{10}{0.6}$
M_{L_1}, M_{L_3}	$\frac{10}{0.6}$	M_{L_5}	$\frac{50}{0.6}$
M_{L_6}	$\frac{50}{0.6}$		

Table 4.4: Comparator transistor sizes

Total power dissipated by the architecture is estimated to be 18mW when using a 100MHz clock. Table 4.5 shows the power consumed by each section in detail.

Block	Consumed Power (mW)
Buffer	5.412
Comparator	0.974
Loop filter	2.658
Current Sources	1.32
Timing generator	8.6
Total Power	18.944

Table 4.5: Consumed power by each block of the IF digitizer architecture in CMOS technology

4.4.2 BiCMOS Comparator

This comparator consists of three parts: preamplifier, emitter coupled pair (ECL) latch, and ECL to CMOS level converter. The pre-amplifier and the ECL latch are

designed using bipolar transistors, whereas the ECL to CMOS level converter is designed with MOS transistors only. As mentioned in [5] the noise of the comparator depends on the pre-amplifier transistors only. [5] has shown that in switched capacitor circuits the bipolar transistor will produce more noise than a MOS transistor because of the capacitive source. Therefore, the pre-amplifier input transistor is a MOS transistor. Fig. 4.21 shows a schematic of the preamplifier.

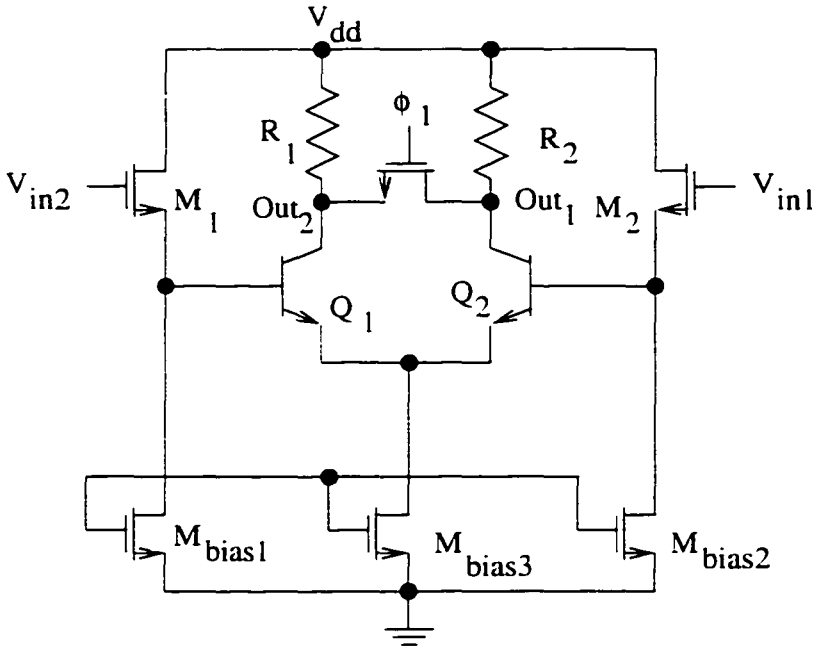


Figure 4.21: Pre-amplifier Schematic in BiCMOS Comparator

The bipolar transistors are biased at 142 μA and the input MOS transistors are biased at 462 μA. From [5] the equivalent comparator noise can be written as:

$$E_{comp} = 8kT\left(\frac{2}{3}\left(\frac{1}{g_m - M_1} + \frac{1}{g_M - M_{bias}}\left(\frac{g_m - Mbias}{g_m - M_1}\right)^2\right)\right)$$
$$+8kT\left(r_b - Q_1\left(\frac{(1 + g_{m-M_1} r_{\pi-Q_1})}{g_{m-M_1} r_{\pi-Q_1}}\right)^2 + R_{sw}\right) \quad (4.14)$$

Substituting the current in the above equation, the noise comparator is calculated to be $10\text{nV}/\sqrt{Hz}$. The bandwidth of the preamplifier is close to 30MHz. The transistors size are shown in Table 4.6.

MOS Transistor	Size
M_1, M_2	$\frac{180}{0.8}$
M_{bias_1}, M_{bias_2}	$\frac{12}{0.8}$
M_{bias_3}	$\frac{40}{0.8}$

Table 4.6: The MOS size in BiCMOS preamplifier

Unlike the CMOS comparator, the input transistors are not optimized for the minimum input noise. The power consumed by the pre-amplifier is 2.43 mW.

The ECL latch is the latch was proposed in [50]. Due to small output swing the latch is fast. Fig. 4.22 shows a schematic of the latch. The latch transistors are biased at 125.7 μA with $R_L = 3.3k\Omega$ the output swing of the latch is 0.4 volts. The total power consumed by the latch is estimated to be 2.84 mW.

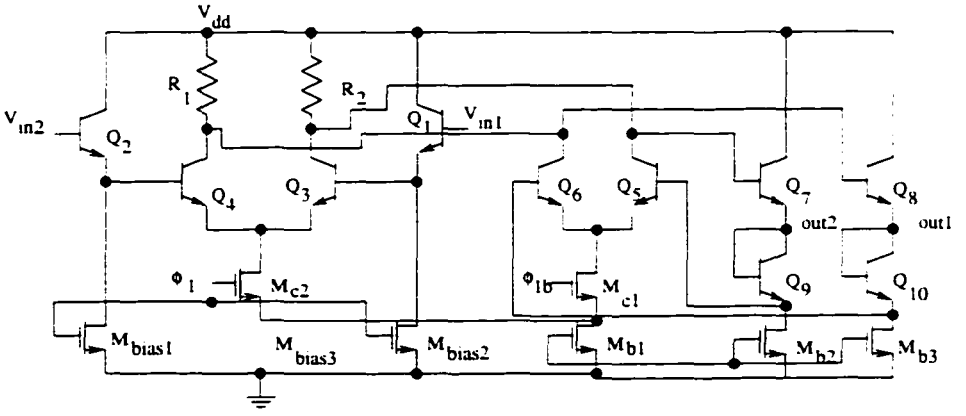


Figure 4.22: ECL latch in BiCMOS comparator

Power consumption of the comparator is summarized in Table 4.7.

Block	Power Consumed (mW)
Comparator	5.414
Loop Filter	2.64
Buffer	11.32
Timing Generator	0.832
Current Source	2
Total Power	22.206

Table 4.7: power consumed by the designed BiCMOS IF architecture

4.5 Sampling Mixer Design

The simulation results in the previous chapter illustrated that the distortion will be reduced approximately 20 dB because of the feedback loop. As a result, to get a 72 dB signal to noise distortion ratio (SNDR), the sampling mixer has to have a linearity close to 52dB. Using [3-5], the sampling mixer switch size can be calculated. However, the equations are valid for a sampling mixer whose input is connected directly to the IF input. Hence the equations can still be used to design the mixer for the proposed architecture. Using a voltage mode approach for the summer, the continuous time distortion, due to the nonlinear characteristic of a MOS switch, will be reduced because of the presence of the resistive summer.

Since the sampling capacitor is already chosen (section 4.2), the size of the sampling switch will control the distortion. Three types of distortion can be written as [3,4]:

$$HD_3 = \frac{A^2}{4}\frac{C\omega}{K'(V_G - V_T)^3} \tag{4.15}$$

$$HD_3 = \frac{3A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2 \tag{4.16}$$

$$HD_3 = \omega^3\sqrt{\frac{C}{K'}}\left(\frac{T_f}{V_G}\right)^{5/2}.0.0913 \tag{4.17}$$

where T_f is the fall time of the sampling clock and $K' = \mu C_{ox}\frac{W}{L}$. If T_f and $\frac{W}{L}$ are selected as 100ps and 162 respectively, the distortion due to continuous time, non-uniform sampling, and time varying would be determined as 60dB, 80dB, and 83dB respectively. As shown, the distortion due to continuous time dominates the other two types.

4.6 Summary

In summary, all the blocks that are required in 300MHz IF digitizer were designed. The design issues of each block were discussed. The circuits that were used in two types of technologies were introduced. In the next chapter, implementation of each design will be discussed and measurement results will be shown.

Chapter 5

Experimental Results

A second-order passive sigma-delta modulator for a 400MHz IF digitizer application has been implemented in three versions. The first version is implemented in BiCMOS 0.8 μm technology using a current summing approach. The second version is implemented in same technology with voltage summing approach. The third version is implemented in CMOS 0.5 μm technology using a voltage summing approach. In this chapter the experimental results of the first two versions will be introduced. The test setup and some testing guidelines will be explained as well.

5.1 IF Digitizer Using A Current Approach for Summing

This IF digitizer architecture was implemented in a 0.8 μm triple-metal double-poly BiCMOS process.

5.1.1 IC Implementation

Several rules are followed in the implementation:

1. A series of substrate contacts is used to isolate the blocks from one another to prevent the interference and substrate noise coupling between any two blocks.

2. The circuit is fully differential to increase the noise immunity for the system particularly the passive loop-filter.

3. Complementary clock and digital outputs are used to reduce the large switching noise in the output.

4. A series-to-parallel converter is used to increase a number of captured samples for more accuracy in the FFT calculation. This block is useful for capturing data at lower speed than that of the sampling clock (5 times).

5. The comparator, the passive loop filter, and the summer are symmetrically designed to reduce the noise. However, the reconstruction filter is not symmetrical because of the limitation on the available design space.

6. To reduce the interference the digital switching transients on the analog ground and power supplies, the power supply and the ground of the analog part are separated from the digital part.

7. The system has an enable pin whose function is to bypass the reconstruction filter so the architecture is converted to a regular sigma-delta modulator. This pin allows one to compare the conventional architecture performance with the performance of the new architecture.

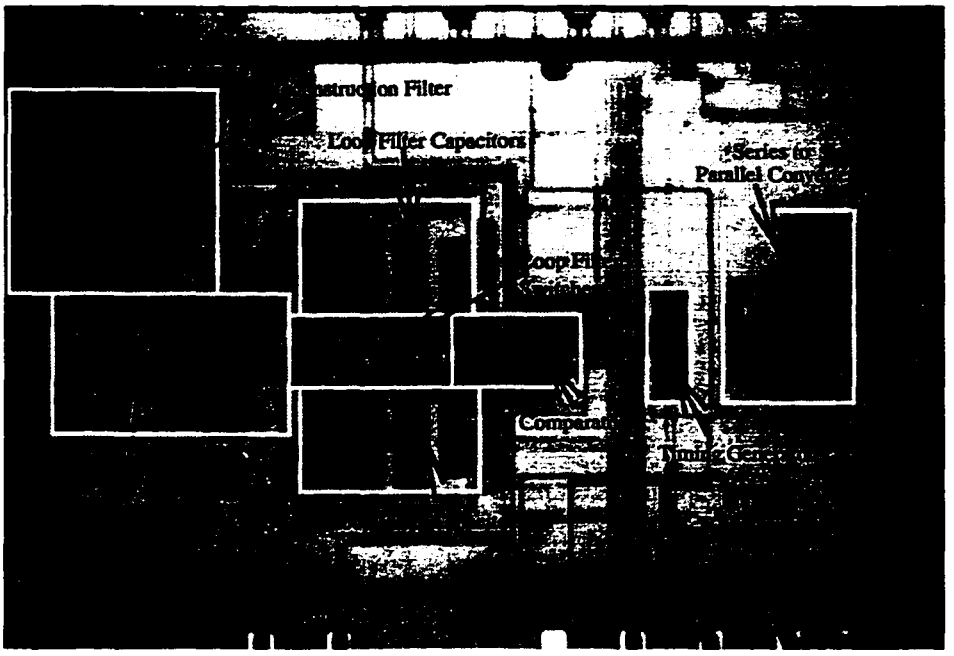


Figure 5.1: Micro photograph of the IF digitizer with current adder

The chip micro photograph is shown in Fig. 5.1. As shown in the figure the digital part of the circuit is separated from the sigma-delta structure by substrate contacts to prevent the digital noise from being transferred to the digitizer section.

5.1.2 Test Results

Since the adder in this chip is adding the current the VIC and IVC both have frequency response limitation which is approved by the HSPICE simulation. the highest IF frequency that the system could respond to was 80MHz. The test was repeated using frequencies of 10MHz, 20MHz and 80MHz with a sampling clock of 10 MHz. For the 10MHz input there is no sub-sampling. The measurement results are shown in Fig. 5.2.

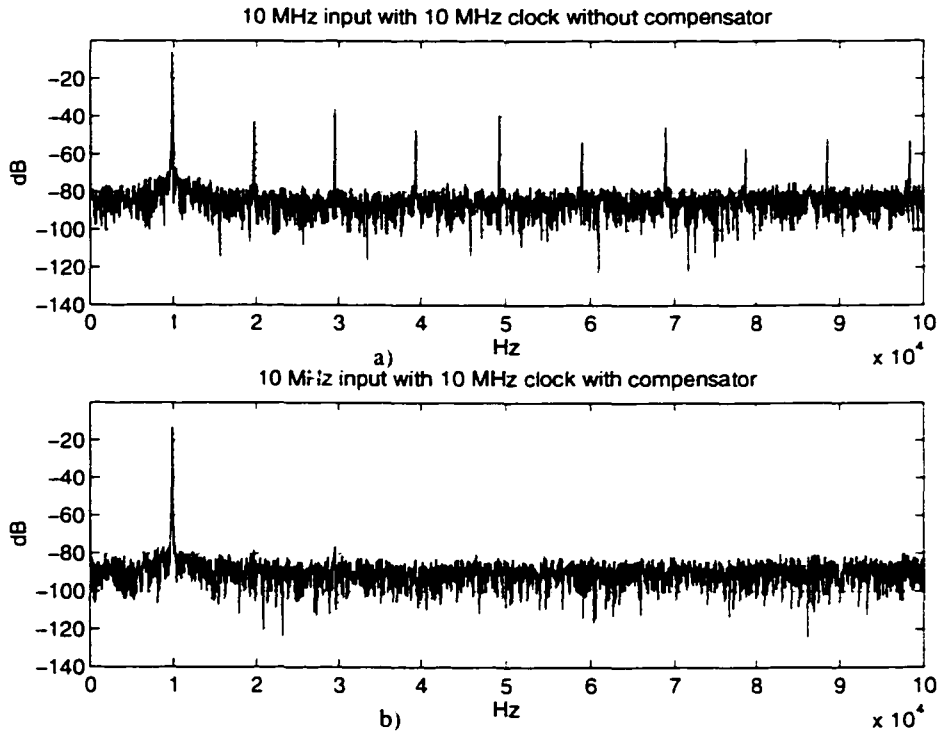


Figure 5.2: Measurement result of the IF digitizer with 10.01MHz input and 10MHz sampling clock a) without the reconstruction filter b) with reconstruction filter

As shown in Fig. 5.2 the distortion is suppressed more than 20dB. The distortion was produced by increasing the input amplitude. This result shows that with reconstruction filter, not only is the distortion suppressed, but the dynamic range is increased. It is known from literature that the clock phase noise creates a skirt around the signal, therefore, the signal-to-noise ratio will decrease. In Fig. 5.2 it is shown that the new architecture will reduce that effect. Fig. 5.2 also shows that the noise floor decreases by approximately 3dB. However, the theoretical reason for this is not known yet.

Fig. 5.3 shows the performance of the system with a 20.01 MHz IF input and

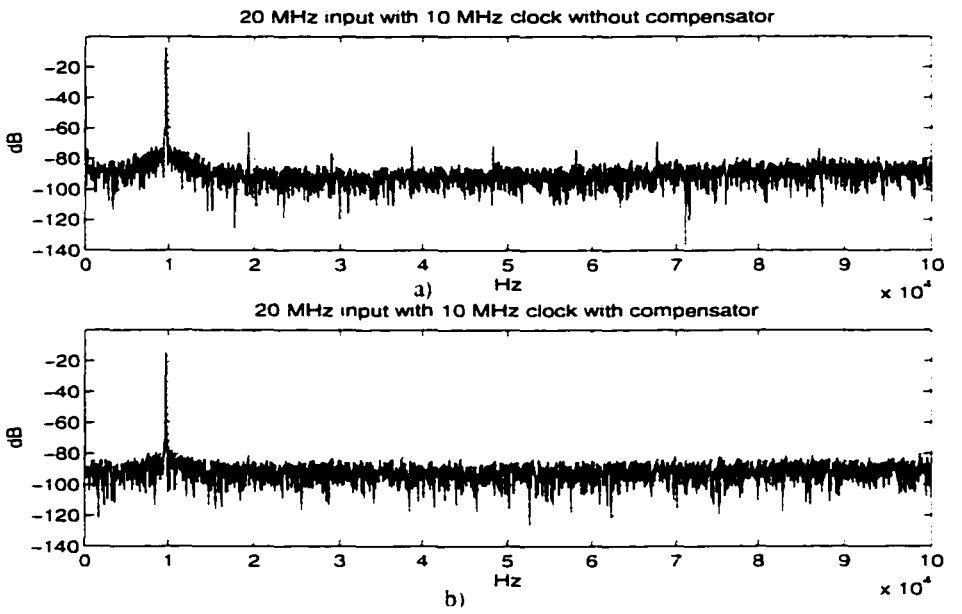


Figure 5.3: Measurement result of the IF digitizer with 20.01MHz input and 10MHz sampling clock a) without the reconstruction filter b) with reconstruction filter

the same sampling clock. The two graphs shows the performance of the system without a reconstruction filter and with a reconstruction filter. Note that subsampling does not change the behavior of the system and the skirt is reduced at 20MHz input frequency.

Fig. 5.4 shows the performance of the system with a 80.01 MHz IF input and the same sampling clock. Fig. 5.4a is the output frequency response of the system without a reconstruction filter and Fig. 5.4b is the output frequency response of the system with a reconstruction filter whose input signal is sampled with 8 times less frequency.. The results show that both the distortion and the skirt has reduced due to the use of the reconstruction filter. The input signal is sampled with 8 times less frequency.

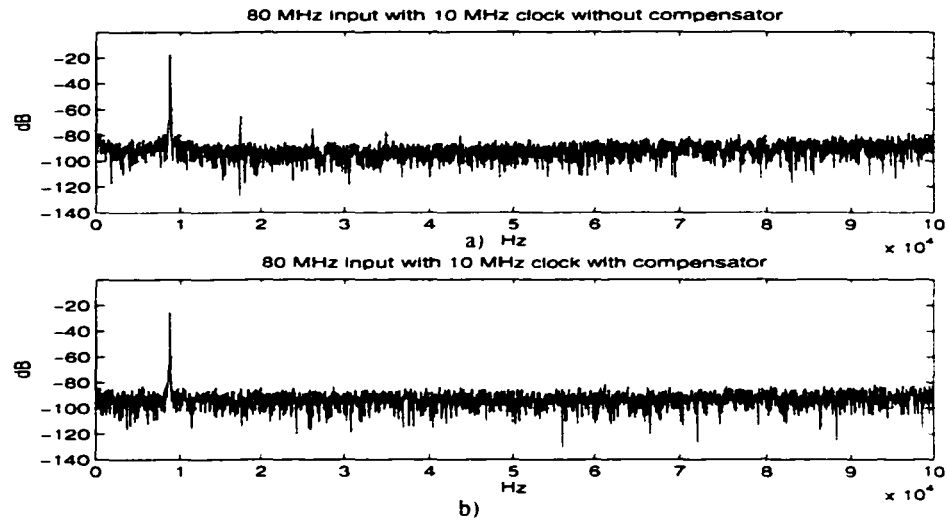


Figure 5.4: Measurement result of the IF digitizer with 80.01MHz input and 10MHz sampling clock a) without the reconstruction filter b) with reconstruction filter

The distortion in Fig. 5.4a is much less than that presents in Fig. 5.2a and Fig. 5.3a. This is because the frequency response of the adder attenuates the input frequency as well as the distortion. Since the current summer was not optimized for power, particularly, the IVC part, the power dissipation of the circuit is high and is more than 20mW. In conclusion, the above measurement results show that the reconstruction filter increases the dynamic range, suppresses the distortion, and suppresses the skirt due to the phase noise of the sampling clock.

5.2 IF Digitizer Using a Voltage Approach for Summing

This IF digitizer was implemented in a 0.8 μm triple-metal double-poly BiCMOS process.

5.2.1 IC Implementation

All the implementation rules used in the previous design were used in this design as well. In addition. the layout is completely symmetrical including the summer part. In order to reduce the mismatch of the loop-filter. summer and reconstruction filter the common centroid technique is also used.

The chip micro photograph is shown in Fig. 5.5. In this design. the digital part of the circuit was separated from the modulator part with a ground produced by substrate contacts.

5.2.2 Test Results

Unlike the current summing approach. this version was not suffering from frequency response. The test was handled in different input frequencies. The measurement results shown in this section are captured at 200MHz and 400MHz IF input with a sampling clock frequency of 20MHz.

As shown in Fig. 5.6 the distortion is suppressed more than 20dB. Fig. 5.6a shows the output performance of the conventional architecture and Fig. 5.6b demonstrates the effect of the new architecture on suppressing the distortion. The

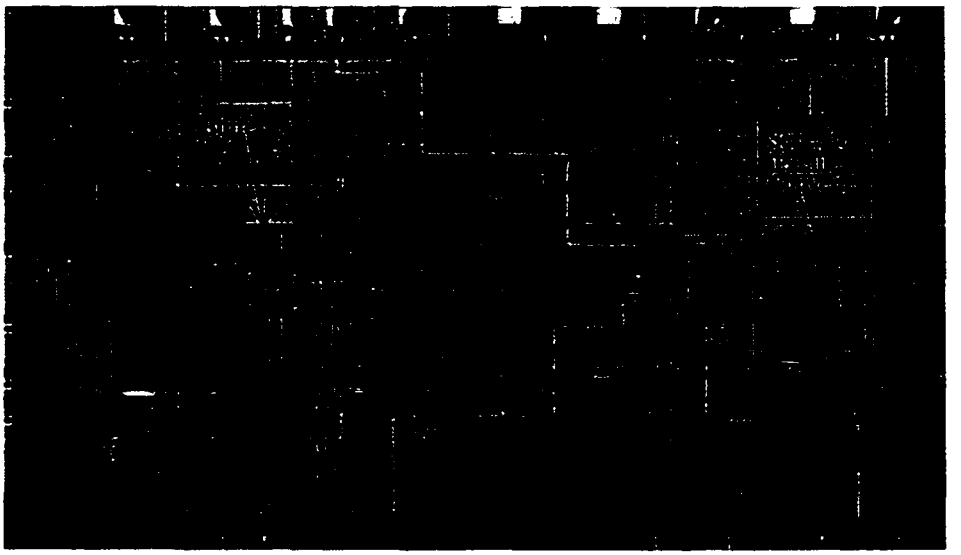


Figure 5.5: Micro photograph of the IF digitizer with voltage adder

main sigma-delta modulator are the same for both graphs. Except for Fig. 5.6b a reconstruction filter is added to the architecture by an enable pin. It can also be seen that the new architecture has lower noise floor than that of the conventional architecture. The fundamental amplitude at the output of the new architecture is slightly less ($< 2dB$) than that of the conventional architecture which is expected due to the linear feedback added to the architecture.

Fig. 5.7 shows the performance of the system at 400MHz input. The sampling clock frequency and the input amplitude has been kept constant. As demonstrated. the new architecture shows a good performance in terms of distortion compare to the conventional architecture. The new feedback path has reduced the distortion below the noise floor. There is a second harmonic distortion in Fig.5.7b due to the signal generator used for the testing and there was not enough filter for removing the harmonics of the source.

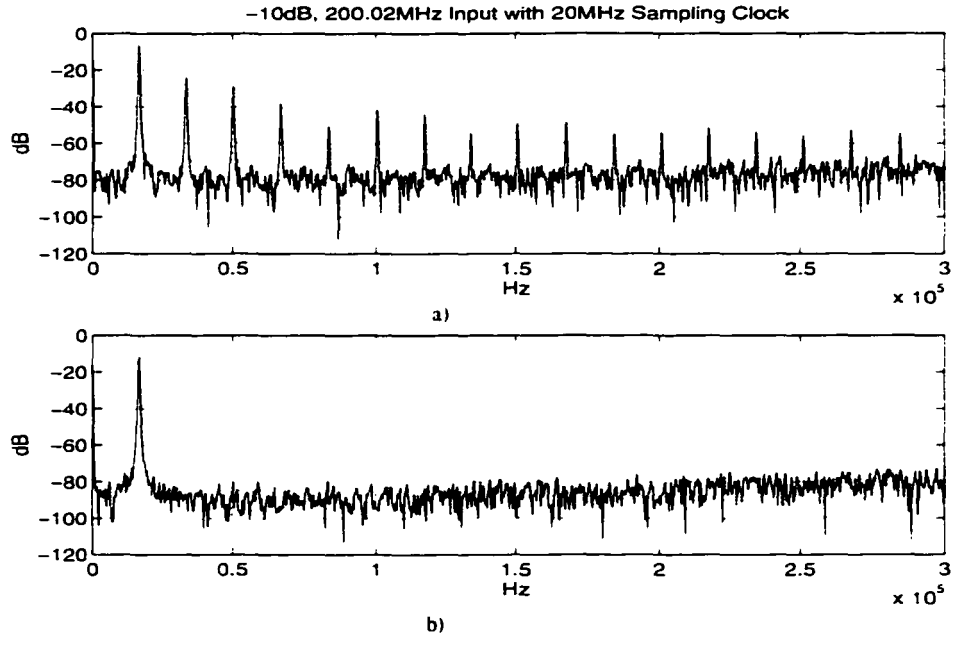


Figure 5.6: Measurement results of the IF digitizer with 200.02MHz input and 20MHz sampling clock a) without the reconstruction filter b) with the reconstruction filter

An Inter modulation test results at 200MHz input frequency with a sampling clock frequency of 20MHz is demonstrated in Fig. 5.8. As shown the third inter modulation (IM3) and other extra distortions due to the presence of two signals are suppressed by the new architecture.

From the above measurement results, one may ask that why the conventional architecture has huge distortion. To answer this question, it has to be mentioned that the purpose of this thesis was to suppress the distortion due to the nonlinear characteristics of different blocks or components. Therefore, the design was not optimized for low distortion output or high resolution circuits. However, the overall result shows that in the optimized circuit the output performance in the new architecture is much better than that of the conventional architecture.

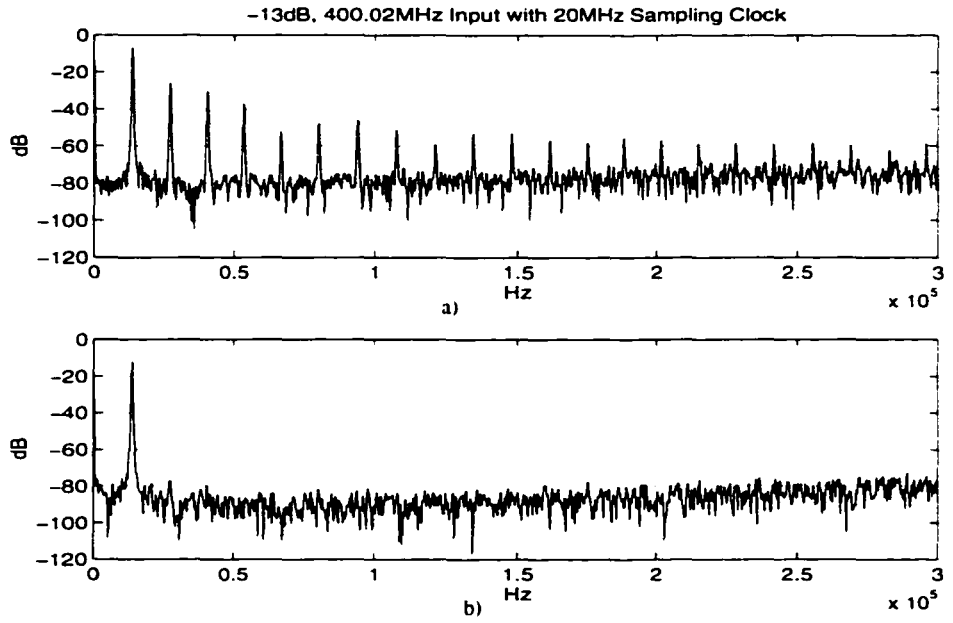


Figure 5.7: Measurement results of the IF digitizer with 400.02MHz input and 20MHz sampling clock a) without the reconstruction filter b) with the reconstruction filter

5.3 Test Setup

To perform the testing some steps was necessary which as follows

1. The printed circuit board (PCB) used for testing should be immune to noise.
2. The package was used for the implemented chip should be able to handle high input frequency properly.
3. To reduce the substrate noise the substrate should be connected to the ground properly.
4. To reduce the effect of digital noise on analog circuits separate digital ground and power supply should be used.

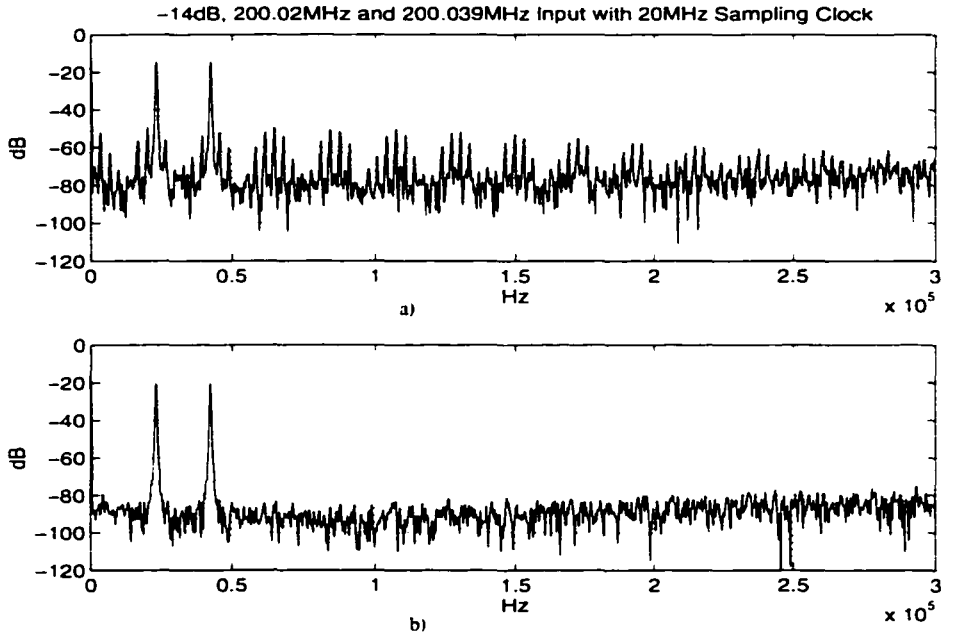


Figure 5.8: Measurement results of the IF digitizer for IM3 with 200.02MHz. and 200.039MHz input and 20MHz sampling clock a) without the reconstruction filter b) with the reconstruction filter

It was tried to use all of the above mentioned steps. For example.a quad-flat package was used for the chip and a multi layer board was designed for testing. The test setup is shown in Fig. 5.9.

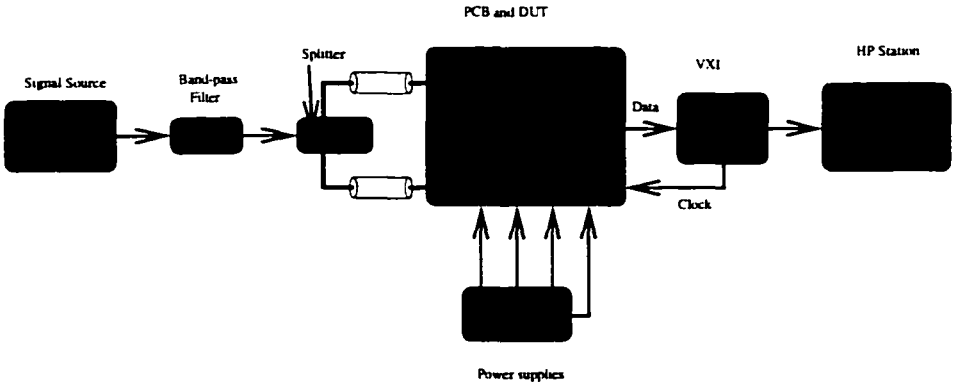


Figure 5.9: A test setup for the implemented IF digitizer

Chapter 6

Conclusions and Future Work

This chapter summarizes key research contributions and results. and provides some recommendation for future work. The distortion at high frequency where design optimization will not improve the overall system performance. Using the technique discussed in this thesis will give people this opportunity to remove some of the extra blocks and replace them with an IF/RF digitizer. This will reduce the size and power and increase the performance of the overall system.

6.1 Key Contributions

The key contributions of this thesis can be summarized as:

1. Investigating the quantized feedback and its effect on reducing the distortion. Comparing the performance of the quantized feedback with the continuous amplitude feedback.

2. Proposing a new architecture whose function is to improve the performance of quantized feedback and suppress the distortion of the overall system.

3. Theoretical analysis of a single-bit quantized feedback and developing a linear model for the new architecture.

4. Implementing the proposed architecture and investigating problems which this new architecture is involved.

6.2 Future Work

The summer in the proposed architecture is a bottleneck of the system. As mentioned in this thesis. two approaches are available. which each involves a lot of design effort. Increasing the input frequency to RF. all of the intermediate blocks will be removed and LNA can be integrated within the architecture. Therefore. designing LNA will not involve the distortion problem. However. designing a summer at the RF frequency is a challenge. The input level at this frequency is very small and loading will be an issue. Another problem that this architecture is facing with is that because of very small signal at RF frequency. the comparator input becomes very small. therefore. a very low noise. low offset comparator is required. At that frequency the noise immunity of the passive architecture has to be investigate in particular the substrate coupling effects on the performance of the passive architecture..

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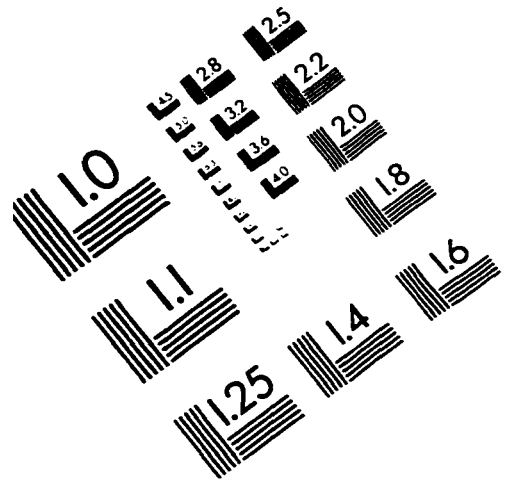
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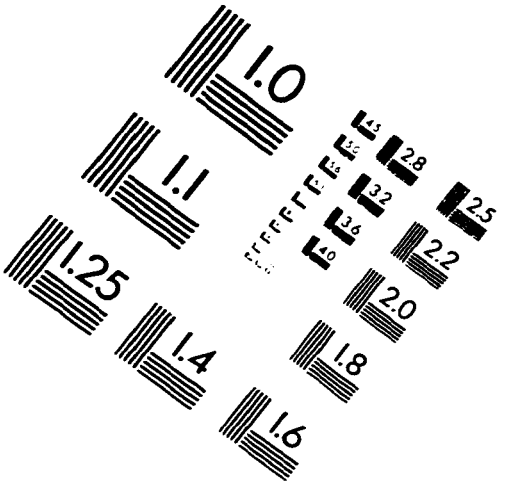
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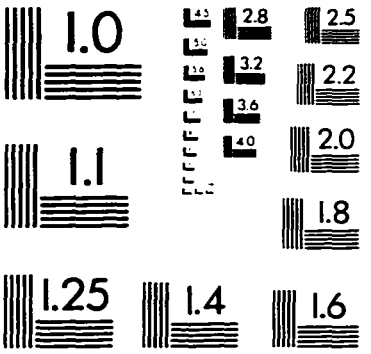
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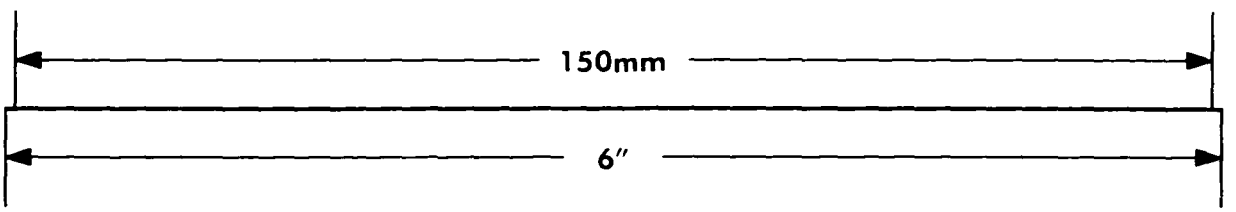
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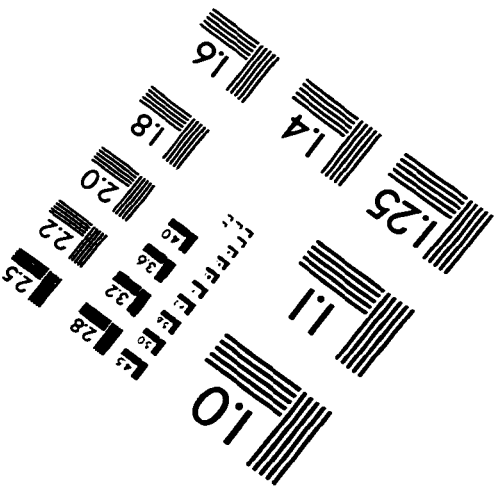
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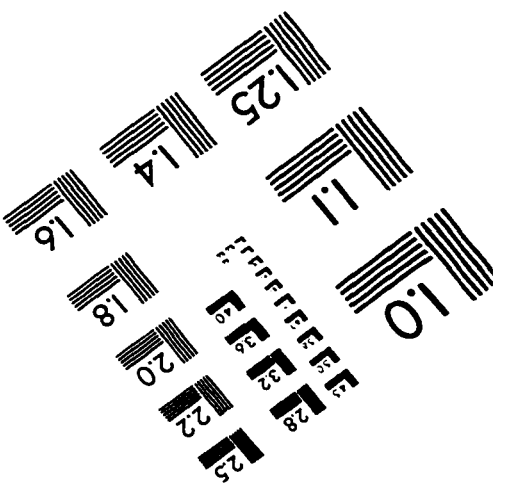












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