Low-power and Radiation Hardened TSPC Registers

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Battery-operated systems require power and energy-efficient circuits to extend their battery life. Flip-flops (FFs) are a basic component of digital circuits, and their power consumption and speed significantly impact the overall performance of a digital system. A clock network in a complex System-on-Chip (SoC) consumes a substantial amount of power. Additionally, often pipelines are used to enhance the system throughput, which puts additional burden on the clock network. Arguably, a flip-flop with fewer clock transistors will reduce its power burden on the clock network. This research proposes three very low-power Single-edge Triggered (SET) True Single-phase Clock (TSPC) FFs with only two and three clock transistors. Moreover, a scan-chain of 256 FFs and AES-128 encryption engine were designed as a benchmark to further investigate the power savings of the proposed FFs. Additionally, we have also designed three very low-power Dual-edge Triggered (DET) latch-multiplexer type TSPC FFs with only eight and ten clock transistors to sample the data at both positive and negative clock edges.

Furthermore, high-performance computations in Integrated Circuits (ICs) are increasingly needed for space and safety-critical applications. ICs are subjected to high-energy ionizing particles in the radiant space environment, which will cause the device performance to degrade or even fail. A Single Event Upset (SEU) occurs in the logic circuit when an ion strikes a device's sensitive node, changing the output from 0 to 1 or from 1 to 0. In radiant applications, ICs contain storage cells like FFs, latches, or Static Random Access Memories (SRAM), and always experience SEU. Although package and process engineering can minimize alpha particles, cosmic neutrons cannot be physically blocked. Therefore, for high reliability systems, soft error tolerant circuit designs are crucial. Traditional Radiation Hardened By Design (RHBD) techniques have some trade-offs between area, speed, power, and energy consumption. Thus, new designs are required to reduce these penalties. This research proposes two high-performance, low-power, low-energy, and low-area RHBD TSPC FFs with only four and five clock transistors suitable for space and safety-critical applications.

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Dedication

This is dedicated to my grand-father whom I lost one-and-half years ago during this journey.

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List of Abbreviations

18TSPC 18T Single-phase Clocked Static Flip-flop xii–xiv, 21–23, 50, 52, 53, 56, 59–61, 64, 98

19TSPC Proposed 19-Transistor TSPC Flip-flop xiii, xiv, 48–50, 52, 53, 55, 56, 59–61, 64, 100

20TSPC Proposed 20-Transistor TSPC Flip-flop xiii, xiv, 47, 50, 52, 53, 55, 59–61, 64

21TSPC Proposed 21-Transistor TSPC Flip-flop xiii, xiv, 47, 50, 52, 53, 56, 59–61, 64, 100

8CTSPC-DET Proposed Ultra Low-power TSPC Dual-edge Triggered Flip-flop xv, 81, 90, 92, 96, 97, 99

ACFF Adaptive Coupling Flip-flop xi, xiii, 19, 50, 52, 53, 59, 64

AES Advanced Encryption Standard 57, 59

ASICs Application Specific Integrated Circuits 57

C^{2}MOS-Quatro C^{2}MOS Quatro D Flip-flop xiii, 39, 41, 70, 71, 73, 75

CMOS Complementary Metal-oxide Semiconductor xi, xiii, xv, 1, 2, 5, 10, 15, 18, 33, 49, 50, 70, 78, 91, 92, 97, 98

DA Data Activity xiii–xvi, 8, 15, 18, 19, 21, 23, 28, 43, 51–54, 56, 57, 60–63, 66, 71–74, 76, 78, 79, 84, 92, 93, 95–97

DAs Data Activities 20, 22, 52, 55, 56, 60, 61, 64, 71, 73, 75, 78, 81, 84, 86, 88, 91, 92, 96–99

DET Dual-edge Triggered viii, xii, 8, 9, 13, 24–27, 29, 80, 81, 84, 88, 90–92, 96, 97, 99

DFF D Flip-flop 33, 76, 78, 79, 99

DICE Dual Interlocked Cell xiii, xiv, 36–40, 42, 65, 68, 69

DUT Design Under Test 51

ECC Error Correction Code 32, 65

EDP Energy-Delay-Product 18, 19

FFs Flip-flops xi, xiv, xvii, 5, 7–10, 12–14, 24, 26, 29, 33, 38, 39, 43, 49, 51–53, 55–57, 59–61, 64–67, 70, 71, 73, 75, 76, 78–81, 90–92, 96–100

FS-TSPC-DET Fully Static True Single-phase Clocked Dual Edge-triggered Flip-flop xii, xv, 27, 92, 96

HLFF Hybrid-latch Flip-flop xi, 12

IC Integrated Circuit 1–3, 8, 9, 65

ICs Integrated Circuits 3, 8, 9, 43, 65, 80

IoT Internet of Things 2, 80, 99

LET Linear Energy Transfer 37

LLFF Low-power at Low data activity Flip-flop xii, xiii, 22, 23, 50, 52, 53, 55, 59, 64

LPHD-DET Proposed Low-power at High Data Activity TSPC Dual-edge Triggered Flip-flop xv, 81, 83, 84, 88–90, 92, 96, 97, 99

LPLD-DET Proposed Low-power at Low Data Activity TSPC Dual-edge Triggered Flip-flop xv, 81, 83–87, 90, 92, 96, 97, 99

MOSFET Metal-oxide Semiconductor Field-Effect Transistor 14

MQ-Quatro Modified Quatro D Flip-flop xiii, 41, 42, 70, 71, 73, 75

MS-DFF Master-Slave Standard D Flip-flop xiii, 39, 70, 71, 73, 75

MS-DICE Master-Slave DICE D Flip-flop xiii, 39, 40, 70, 71, 73, 75

MS-Quatro Master-Slave Quatro D Flip-flop xiii, 39, 40, 70, 71, 73, 75

MTJ Magnetic Tunnel Junction xii, 31, 32

NAND logic "NAND" 44, 83

NMOS N-Channel Metal-oxide Semiconductor Field Effect Transistor 15, 21, 24, 27, 38, 47–49, 51, 66, 68–70, 84, 91

OAI21 logic "OR-AND-INVETER" 44

OR logic "OR" 44, 83

PDP Power-Delay-Product xiii, xvi, 18, 19, 52, 54, 73, 95, 96

PMOS P-Channel Metal-oxide Semiconductor Field Effect Transistor 15, 24, 26, 27, 38, 44, 46, 47, 49, 51, 66–70, 84, 91

PVT Process, Voltage, and Temperature 24

REEF Redundancy-eliminated Flip-flop xii, xiii, 23, 50, 52, 53, 59, 64

RHBD Radiation Hardened By Design 8, 9, 30, 32, 34, 38, 42, 65–68, 70, 71, 73, 75, 76, 78, 79, 98–100

RHBP Radiation-Hardening-By-Process 30

S2CFF Static Single-phase Clocked Flip-flop xi, xiii, 20, 50, 52, 53, 55, 59, 64

SDET Static Dual-edge Triggered Flip-flop xii, xv, 24, 25, 92, 96

SDFF Semi-dynamic Flip-flop xi, 12

SEE Single Event Effect 3, 5

SER Soft Error Rate 99

SET Single-edge Triggered viii, 8, 9, 13, 29, 55, 57, 59, 60, 64, 70, 81, 98

SETs Single Event Transients xi, 5–7, 31, 33, 34, 36, 38, 65, 67–69

SEU Single Event Upset xi, 4–6, 31, 33, 36–38, 65, 66, 68, 70, 71

SNU Single Node Upset 42

SoC System On a Chip 7, 43

SPEs Solar Particle Events 4

SRAM Static Random Access Memory 37

SRAMs Static Random Access Memories 8

STC-DET Low-power Redundant-transition-free TSPC Dual-Edge-Triggiering Flip-flop Using single-transistor-Clocked Buffer xii, xv, 28, 92, 96

TCFF Topologically Compressed Flip-flop xii, xiii, 20, 21, 50, 52, 53, 57, 64

TGFF Transmission Gate Flip-flop xi, xiii, xiv, 8, 10, 11, 21, 50, 52, 53, 59–61, 64, 71, 73, 75, 98

TMR triple modular redundant xii, 33, 34, 36, 37, 42

TQ-Quatro Traditional Quatro D Flip-flop xiii, 41, 42, 71, 73, 75

TSMC Taiwan Semiconductor Manufacturing Company Limited xv, 64, 91, 92, 97–99

TSPC True Single-phase Clock xii, 8, 25, 26, 29, 64, 78, 80, 81, 88, 90, 91, 97–99

TSPC-DICE Proposed Static Contention-free Single-phase Clocked Radiation Hardened Flip-flop using DICE Cell xiv, 68–71, 73, 75, 76, 78, 79, 99

TSPC-Quatro Proposed Static Contention-free Single-phase Clocked Radiation Hardened Flip-flop using Quatro Cell xiv, 66, 67, 71, 73, 75, 76, 78, 79, 99

TSPC-SDET TSPC Static DET Flip-flop xii, xv, 26, 92, 96

VLSI Very Large Scale Integration 43, 80

Chapter 1

Introduction

The development of CMOS transistor, the first commercial CMOS Integrated Circuit (IC), and the creation of the first microprocessor (CPU) were significant turning points in semiconductor microelectronics. Since CMOS scaling began in 1970, the number of transistors has doubled every one-and-half years, a phenomenon known as Moore's Law, as depicted in Figure 1.1.

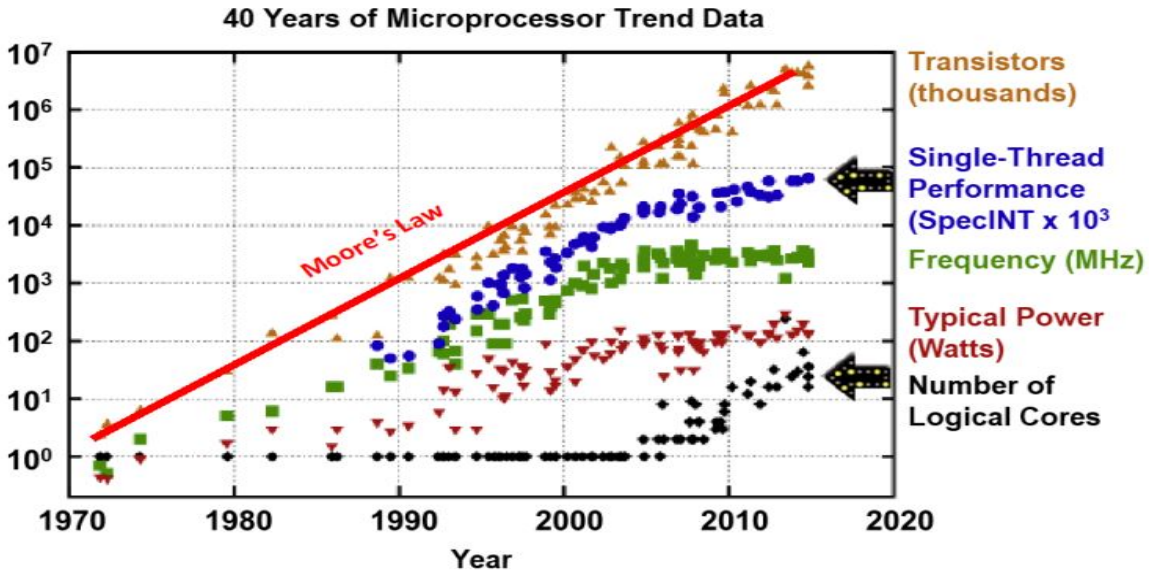


Figure 1.1: CMOS Scaling following Moore's Law [1].

Over the past few decades, Moore's law has significantly advanced semiconductor tech-

nology. Through innovative designs at the transistor, circuit, and system levels, from both manufacturing and packaging, CMOS technology has continued to scale according to Moore's law. It is now relatively usual to integrate more than 50 billion transistors onto a single silicon chip.

The main advantages of CMOS scaling have been density enhancements, chip frequency optimizations, and power savings at a certain frequency [35, 36]. Frequency scaling has slowed down in recent technological nodes, making total chip power (energy per operation at a given frequency) scaling more significant. As a result, the value of scaling has changed to enabling additional applications, more cores, or new functionalities operating at low-power. The possibility of including features and functions in next-generation architectures increases with node-to-node power reduction. Therefore, power consumption is one of the most important design considerations for developing nanoelectronics today.

1.1 Motivation for Power and Energy-efficient Integrated Circuits

Different applications like mobile devices, smart cities, smart homes, autonomous cars, unmanned aerial vehicles, unmanned underwater vehicles etc. require power and energy-efficient Internet of Things (IoT) devices. It is estimated that around 75 billion IoT devices will be connected through the Web by 2025 [37]. As the demand for IoT devices increases, there is a constant push to improve their power, energy, and performance.

Low-power ICs are used for IoT devices to optimize the computational throughput at a given energy budget, mobility by extending the battery life, portability by requiring small or no battery, security by allowing data storage and computation at the edge, delay by avoiding cloud interfaces, cost, and environmental pollution reduction by lowering the carbon footprint of the IC. Therefore, in order to meet the present and future needs of battery-operated or battery-less devices, there is a strong need for research to develop new ideas, methods, architectures, and circuit design techniques for reduction in power and energy consumption.

1.2 Space Radiation and Radiation Effects

1.2.1 Space Radiation

Energy is emitted in the form of waves or particles, and this process is called radiation. When energy particles hit IC, circuit functionality is disturbed, and this phenomenon is called the Single Event Effect (SEE). SEE is categorized into soft errors and hard errors. In soft errors, the circuit works again in normal mode after some amount of time, while in hard errors, there is permanent damage or the circuit must be powered down to be corrected. In space, cosmic rays, gamma rays, and solar flares are the three main radiation sources for SEE. Although plasma may also effect Integrated Circuits (ICs) but due to their low energy ranges, the chances are very low. Ionized particles strike the sensitive nodes within the circuit, resulting in soft errors [2].

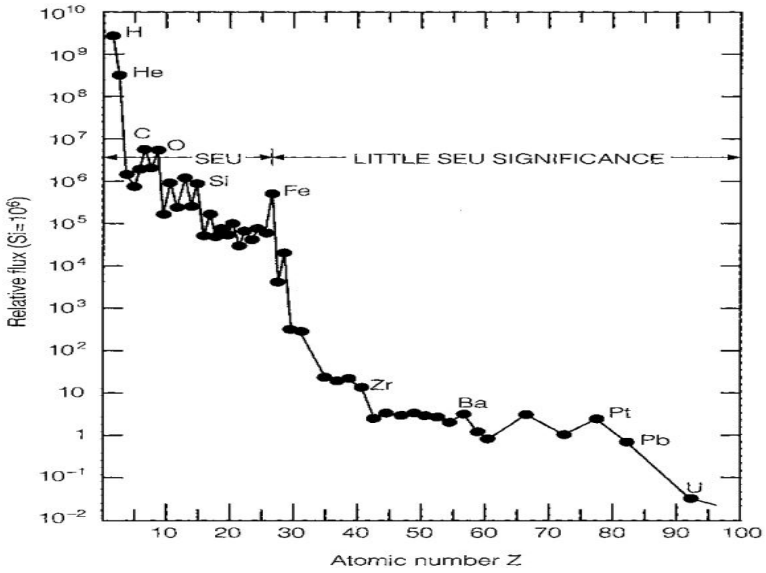


Figure 1.2: Ionized Particle Flux by Atomic Number Relative to Si [2].

Cosmic rays have an impact on electronics in space and on aircraft, and they are the most significant source of deep space radiation for circuits used in high-orbit applications. The energy and ionization of these particles are extremely high. Deep space novas and solar wind are the main sources of cosmic rays. Due to their relative abundance, heavy particles having atomic numbers less than 25 are significant in regard to a SEE type called

a SEU, as shown in Figure 1.2. On the other hand, elements with an atomic number greater than 25 are unable to survive in a space environment and evaporate before reaching earth. Hydrogen, helium, carbon, and oxygen are the four most important elements, and only hydrogen and helium cause 94% and 5%, respectively, of the total amount of high-energy heavy ions found in space.

The magnetosphere, which is located around 10 Earth radii from the planet's centre and faces the sun, shields the Earth from cosmic radiation. Solar wind, or plasma traveling in the magnetic fields of the Earth and other planets, determines the form of the magnetosphere. Inside the magnetosphere, two belts of high SEU concern called Van Allen Belts are shaped at the atmosphere of earth and extending 40000 miles into space. High-energy protons and electrons make up these inner and outer belts. The inner belt traps charged particles for longer periods of time than the outer belt due to stronger magnetic fields closer to the Earth [2], as shown in Figure 1.3.

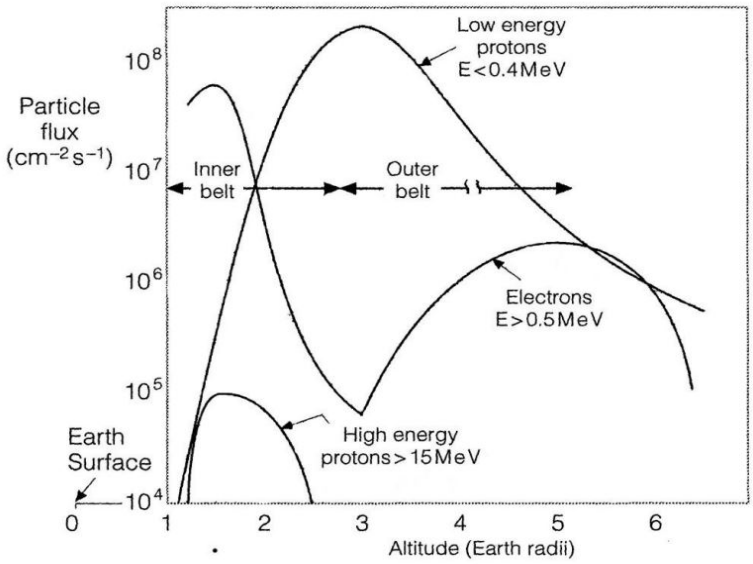


Figure 1.3: Van Allen Belt Equatorial Trapped Particle Flux Versus Altitude [2].

The electromagnetic spectrum contains a variety of waves, but gamma rays, which come from interstellar space or are given off by radioactive substances, have the smallest wavelength and highest energy. This makes it possible for electrons to be ejected from gamma-ray collisions with alpha, proton, and neutron particles in substrates, leading to SEUs in integrated circuits. Solar flares produce radiation in the shape of Solar Particle Events (SPEs) that launch electrons, alpha particles, and heavier particles into space.

Although the particles are capable of penetrating the earth's polar regions to low altitudes, there is a slight possibility that a sizable portion will be injected into the magnetosphere. This means that the majority of solar flares do not threaten the electronics of spacecraft. X-rays that are emitted by solar flares do not damage spacecraft circuitry because of their relatively low flux levels [2].

1.2.2 Radiation Effects

Ionized particles striking a circuit result in SEEs. When an incident particle travels across the substrate of the circuit, a charge is produced because of electrons and holes drift on the node. When this parasitic charge crosses the critical threshold (Q_{CRIT} = C_{NODE} * V_{NODE}) charge of the node, a SEE occurs. Two types of SEE soft errors are popular, SEU, and SETs. A direct ion strike inside the storage element causes SEU, while transient temporary voltage changes from previous logic causes SETs.

Basically, digital logic circuits are divided into sequential circuits and combinational circuits. Because sequential circuits have memory, both the current and the previous inputs can have an impact on the current outputs. In contrast, outputs in combinational circuits depend exclusively on the inputs that are being used at that moment. In these two types of circuits, SEEs operate in different ways. Storage cells that can store data, like latches and FFs, are the primary building blocks of sequential logic circuits. The sensitive node may accumulate enough charge to disturb its state and experience a SEU if an intense charged particle contacts a latch. There are no memory-like structures in combinational logic circuits. The accumulated charge will result in a brief change in current and voltage at the nodes, known as a SETs in the circuits. Furthermore, SEU hard errors such as single event latchup, single event burnout, and single event gate rupture cause unrecoverable failures in CMOS circuits and is not part of this discussion.

1.2.2.1 Single Event Upset (SEU)

SEUs are triggered on by particles hitting a chip if the charge accumulated in the substrate during the hit is greater than the critical threshold charge of nodes electrically coupled to the incident area. Circuitry operating incident nodes has the potential to reverse any voltage shifts and return them to their initial value. However, there are some situations, particularly storage nodes, where the charge won't be absorbed, leading to an upset.

An accumulated charge affects nodes at or close to the strike, causing SEUs in memory or latch storage cells. For example, Figure 1.4 illustrates the results of an ion attack inside

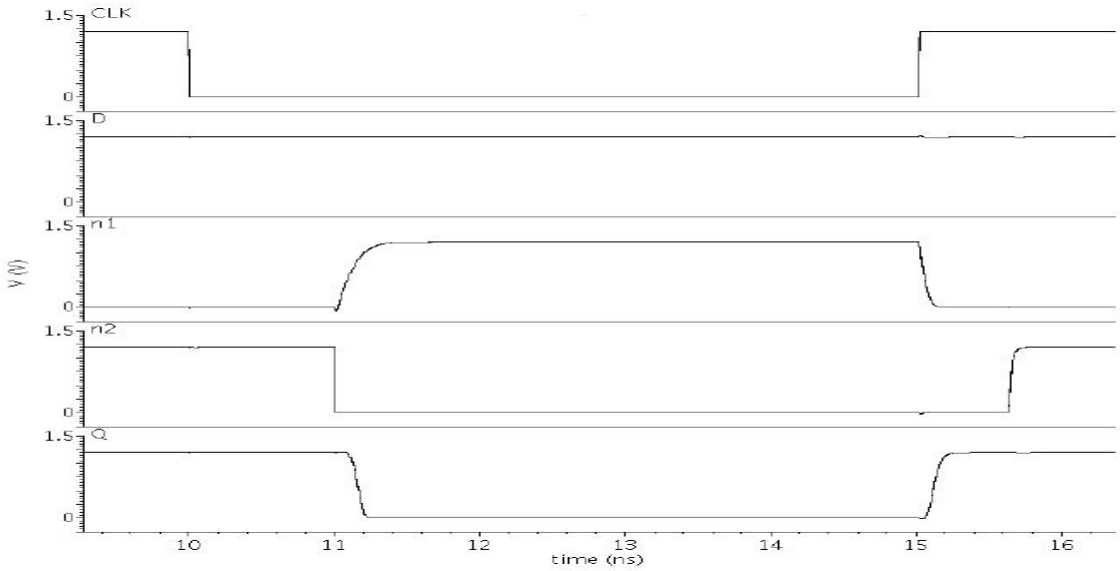


Figure 1.4: SEU on the Storage Node of a Basic Transparent High Latch [3].

a fundamental latch storage node, n2. The node voltage swings to a logic level of 0 when the storage node n2 accumulates negative charge at 11 nanoseconds. This error leads n2 to switch the output of the second inverter to switch state before the collected charge is withdrawn from the incident node because the clock is low and the latch is closed. The inverter change drives n1 high, switching the value stored by the storage cell permanently and interfering with the operation of any circuits after the defective latch. SEUs are irrespective of clock frequency; as ion strikes that can result in this error type can happen at any time. Additionally, since the storage mechanism in many memories and sequential circuits is structurally similar, the ways in which SEUs influence latches also apply to both.

1.2.2.2 Single Event Transients (SETs)

Ionizing particles striking in combinational logic activate off-state devices and are the cause of SETs. Once any accumulated charge has been discharged by the circuitry powering the damaged node, the pulse returns to its normal state. Figure 1.5 depicts this pulse by dividing the charge collecting and diffusion sections into distinct time intervals. Since charge is equal to the product of the node capacitance and the voltage, the recovery process's speed is directly correlated with both of these parameters. Due to this correlation, collected charge poses an increasing threat to reliable circuit functioning as drive strength

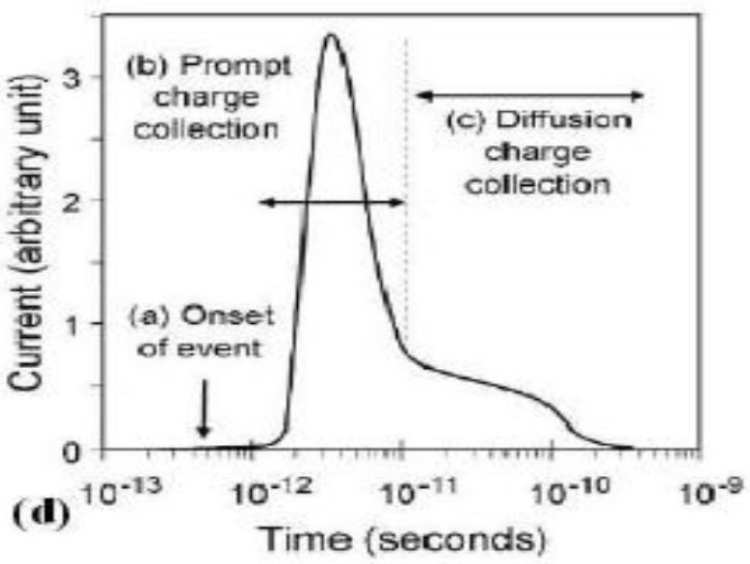


Figure 1.5: SETs Pulse on the Node Due to an Ionized Particle Strike [4].

and node capacitance decline with new fabrication techniques. Generated voltage pulses move through the circuitry until they attenuate or reach a closed latch, which stops them from moving any further.

When SETs reach a storage node near a closing clock edge, they have an irreversible effect on the circuitry. An upset will occur if a SETs occurs during the clock edge's latch setup and hold time because the incorrect value will be recorded. As a result, the likelihood that SETs may disrupt sequential logic is increased by both greater pulse widths and faster clock rates.

1.3 Why TSPC Flip-flops?

Portable devices require power- and energy-efficient circuits to extend their battery life [12, 38, 39, 40, 41, 42, 43, 44, 45, 46]. FFs are a basic component of digital circuits, and their power consumption and speed significantly impact the overall performance of a digital system [13, 16, 47, 14, 48, 15, 49, 50, 51, 52]. Moreover, a clock network in a complex System On a Chip (SoC) consumes substantial power [53, 54, 55, 56, 57, 58, 59, 60, 61], and often pipelines are used to enhance the system throughput, which puts additional

burden on the clock network. Arguably, a flip-flop with fewer clock transistors will reduce its power burden on the clock network.

FFs are used to store both state information and results. Static flip-flops are often preferred in scaled technologies due to their superior reliability, relative robustness, and simpler timing. Traditionally, TGFF is used, which requires a clock and its complement. TGFF often requires up to twelve transistors in clocking, resulting in substantial clock power consumption. Consequently, many circuit techniques have been suggested to lower the clock and overall power consumption in FFs. Some FFs employ conditional clocking to decrease clock power consumption [47, 49, 62]. This technique reduces the clock power consumption but increases the total number of transistors and area. Researchers have also employed pre-charging of internal node(s) in a flip-flop to reduce its clock power [38, 13, 16, 15, 6]. This approach helps to eliminate some clock and data transistors and lower the overall transistor count. The drawback with this technique is that it charges and discharges internal nodes with the clock frequency, which degrades the power-efficiency at low DA. A better technique is to lower the clock-related transistors as much as possible without a pre-charging node [12, 14]. Unfortunately, this strategy increases FFs D-Q delay and data contention power at higher DAs [12]. Thus, research on low-power, low-energy, and high-performance flip-flops using new architectures and techniques continues to improve the overall performance of digital integrated circuits.

Furthermore, process scaling suggests that when a value saved in storage components like FFs or Static Random Access Memories (SRAMs) is reversed, soft errors become a critical concern to degrade the reliability of an IC. Therefore, new flip-flop designs are required to reduce soft-error penalties.

1.4 Thesis Organization

Low-power, low-energy, and high-performance FFs are required to optimize the overall efficiency of digital ICs. In this thesis, we introduced three very low-power SET flip-flop circuits for low DAs with only two and three single-phase clock transistors. In addition to that, three very low-power TSPC DET flip-flop circuits are also presented to sample the data at both the rising and falling edges of the clock. Two very low-power and low-energy TSPC Radiation Hardened By Design (RHBD) flip-flop circuits are also introduced for the safety-critical applications.

This thesis is organized as follows: Chapter 2 is an overview of general types of FFs, performance metrics and state-of-the-art FFs. Chapter 3 discusses radiation-hardened

techniques and existing RHBD FFs. Chapter 4 introduces the proposed very low-power SET FFs. Chapter 5 presents the proposed RHBD FFs. Chapter 6 introduces the proposed DET FFs. In last, conclusion and future work are highlighted.

1.5 Summary

In this chapter, the importance of low-power and low-energy IC is highlighted along with the introduction of space radiation and its effects on ICs. Additionally, the role of the flip-flop is emphasized as a key element to optimize the overall efficiency of digital circuits. Therefore, it is essential to study low-power, low-energy, and high-performance FFs for battery-operated portable devices.

Chapter 2

An Overview of Flip-flops, Performance Metrics, and the State-of-the-art

2.1 Flip-Flops: An Overview

2.1.1 Master-slave and Pulse-triggered

Latches are transparent and can be active low or active high. Any changes made at the input during the active clock level are reflected at the output after a propagation delay. As long as the clock level is active, data is continually accepted. When the clock level switches, the latch opens and the output deviates from the input. For their simplified timing design, robustness, and less risk of race conditions, FFs are chosen over latches. By interconnecting two latches that operate in separate clock phases in sequence, an edge-triggered flip-flop can be created. Typically, the master latch determines the flip-flop's setup time while the slave latch determines the propagation delay. Figure 2.1 shows the block diagram and timing waveform of the master-slave flip-flop.

A master-slave setup is exemplified by the transmission gate flip-flop. Due to its fewer transistors and lower power consumption compared to other CMOS FFs, it is often employed in digital sequential circuits. As shown in Figure 2.2, the TGFF requires a total of 12 transistors for clocking the flip-flop, with the clk and clkn signals coupled to eight transistors of the transmission gates.

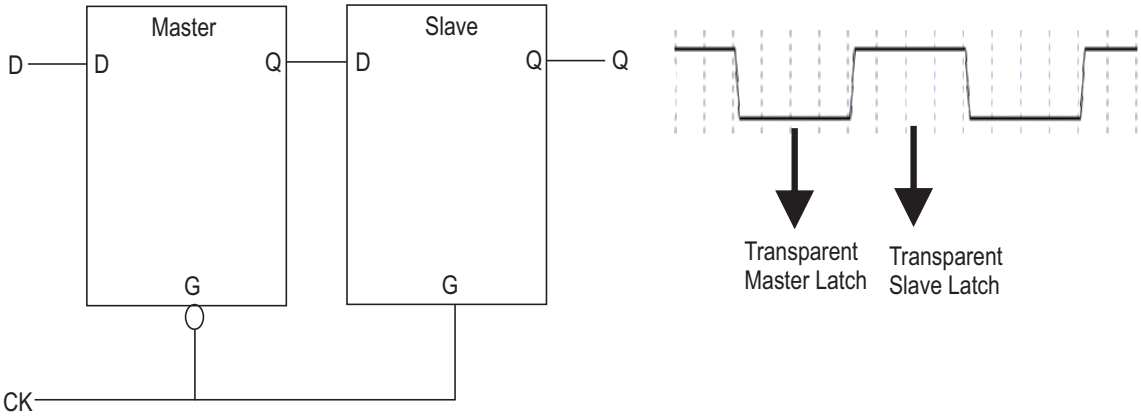


Figure 2.1: Block Diagram and Timing Waveform of Master-Slave Flip-flop.

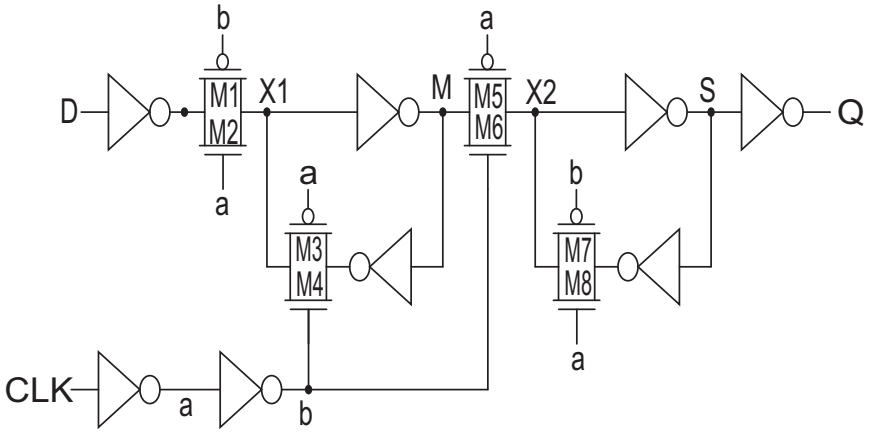


Figure 2.2: The Conventional Static Transmission Gate Flip-flop (TGFF).

Sharp pulses are employed as the clock signal in pulse-triggered latches. When the pulse is active, latch passes the data to the output, while for the rest of the time it is in blocking mode. Throughout the pulse width, the data should remain stable. Using the principle of delaying the signal, a clock signal is supplied at the input of a pulse generator, and a very brief pulse is produced on each clock cycle at the output. The HLFF and SDFF are examples of pulse-triggered FFs, whose performance is enhanced by a reduction in setup time caused by the brief transparent period that the pulse generator creates for data inputs. Additionally, these flip-flops exhibit the soft-edge feature, which increases robustness against clock skew. Schematic diagrams of HLFF and SDFF are shown in Figure 2.3.

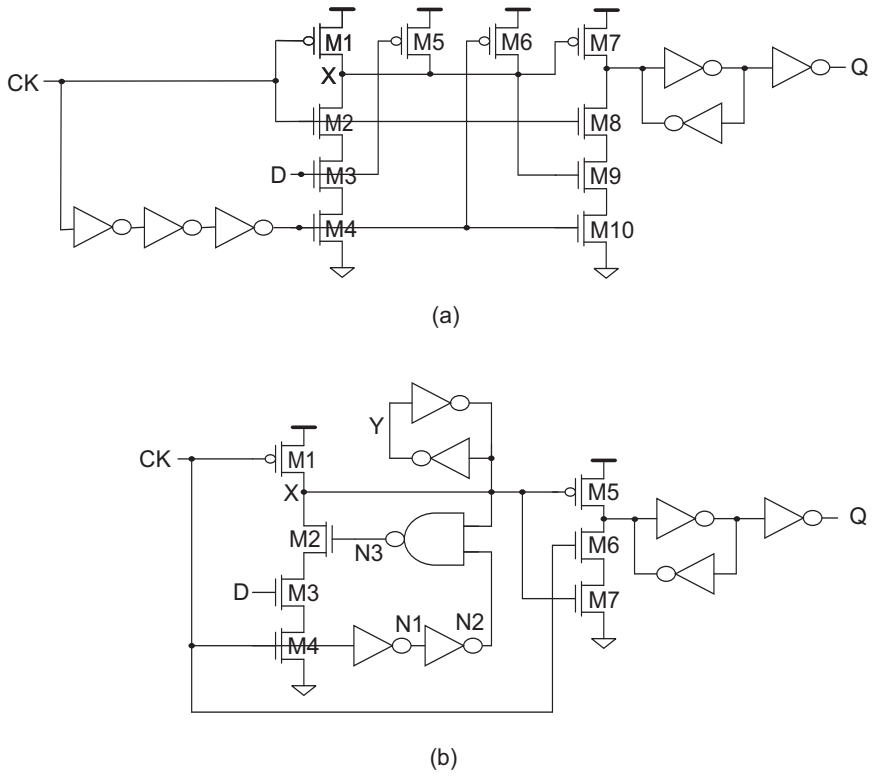


Figure 2.3: Pulse-triggered FFs (a) Hybrid-Latch Flip-flop (HLFF) proposed in [5], and (b) Semi-Dynamic Flip-flop (SDFF) proposed in [6].

2.1.2 Single Clock-phase and Dual Clock-phase

Generally, two latches that operate at different clock phases are connected in a cascaded fashion in master slave FFs. Two clock phases are often required if the structures of the master and slave are identical. However, by making simple adjustments to two latches, the required number of clock phases can be reduced to one. As an illustration, use the complimentary latch of the master for the slave. In this perspective, a real single-phase clock flip-flop is one that only uses one clock phase and typically runs faster than FFs using two clock phases.

2.1.3 Single Edge-triggered SET, and Dual edge-triggered DET

FFs that are SET only operate on the active edges of the clock cycle, whereas DET FFs record data on both clock cycle edges. The block diagram of a DET D flip-flop is shown in Figure 2.4. Positive edge triggered flip-flop samples data during positive clock edge cycles, while negative edge triggered flip-flop samples data during negative clock edge cycles.

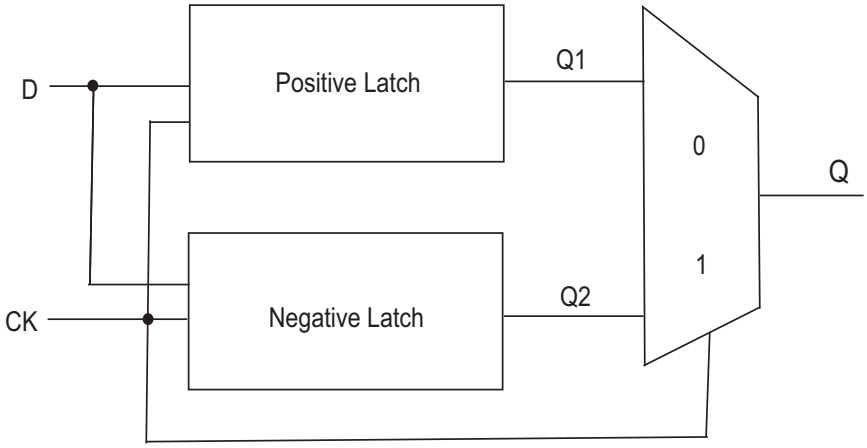


Figure 2.4: Block Diagram of Double Edge-Triggered D Flip-flop [7].

DET FFs which use both edges of the clock signal to capture the input data, are typically desirable for low-power applications. However, they require multiplexers at their outputs and take up more space than standard D flip-flops. Figure 2.5 shows the transistor-level implementation of Figure 2.4. Transistors M1 to M4 make up the positive latch, and transistors M5 to M8 make up the negative latch. Both these master latches operate on

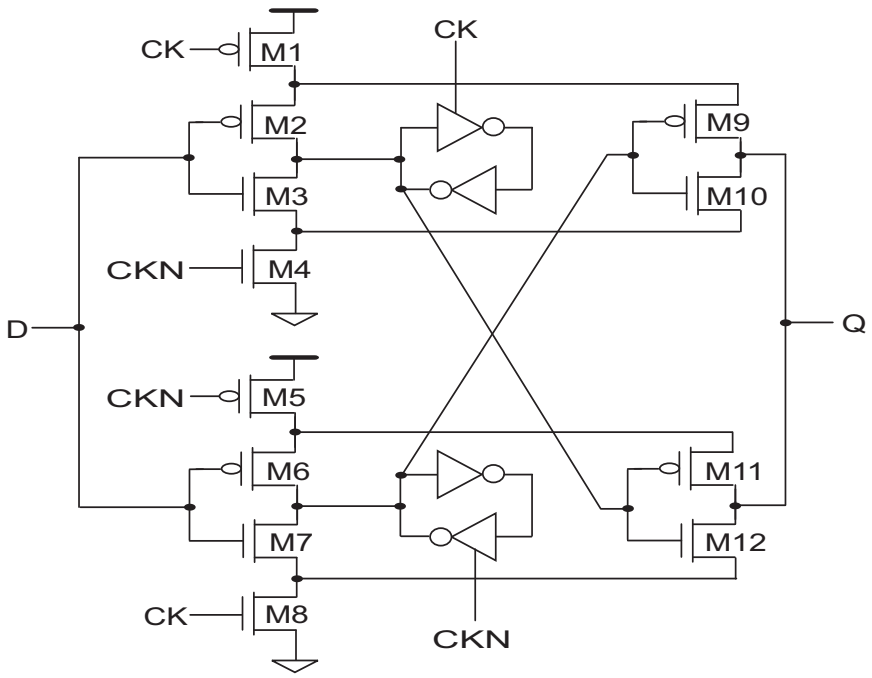


Figure 2.5: Schematic Diagram of Dual-edge Triggered D Flip-flop [8]

opposite phases of the clock. The multiplexer, used in place of slave latch, chooses the result of opaque master. Thus, data changes on both edges of the clock.

2.1.4 Static and Dynamic

In static FFs, stored data is kept even when the clock signal is disabled. Due to their reliability and robustness, these FFs are desirable for widespread use in industrial applications. However, in dynamic flip-flops, stored values are lost if there is a long period of time between refreshes. These FFs are quick, have less clock load, use less energy, and take up less space. But they are prone to noise and cannot operate at low clock frequencies. Only a few applications, like frequency dividers, are viable for these because of their dynamic nature. Sometimes, potential failures also occur in these FFs. Moreover, dynamic nodes discharge due to reverse leakage current in pn junctions and subthreshold leakage in Metal-oxide Semiconductor Field-Effect Transistor (MOSFET). Dynamic FFs can be converted into static FFs with the aid of keepers at dynamic nodes. Figure 2.6 presents the schematic diagrams of static and dynamic FFs.

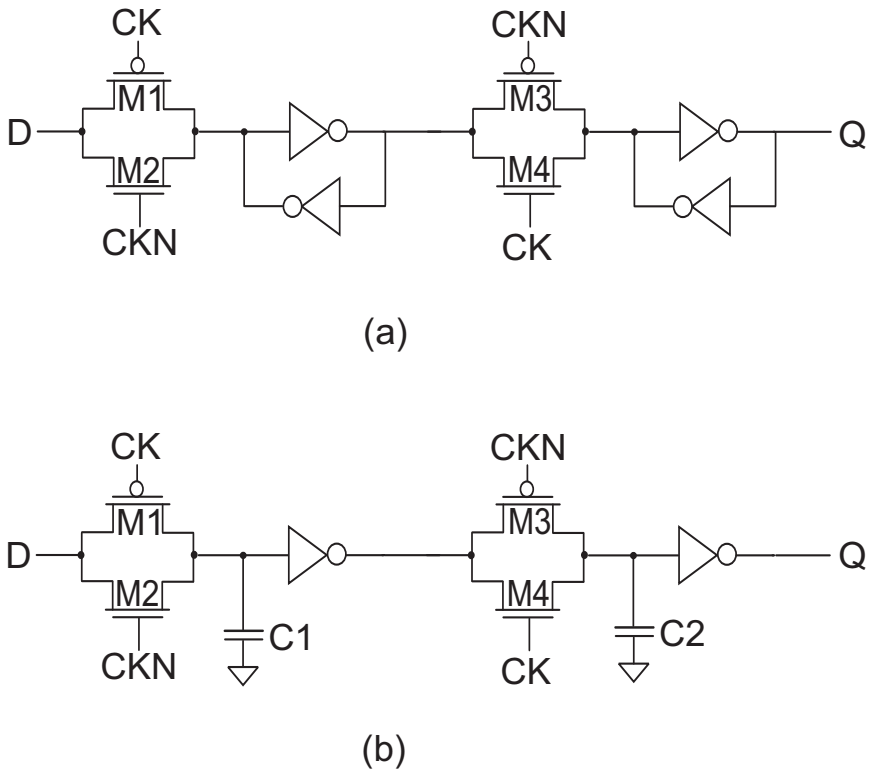


Figure 2.6: (a) Static Flip-flop, and (b) Dynamic Flip-flop [9].

2.2 Flip-flop Performance Metrics

2.2.1 Power

In digital CMOS circuits, there are three primary sources of power consumption, which are enumerated in Equation 2.1.

The first term characterizes the switching element of power, where C_L indicates load capacitance, f_{CK} is the clock frequency, V_{DD} is the supply voltage, and DA is the input DA. The second term denotes the direct-path short-circuit current I_{SC}, which arises when both P-Channel Metal-oxide Semiconductor Field Effect Transistor (PMOS) and N-Channel Metal-oxide Semiconductor Field Effect Transistor (NMOS) transistors are active and current flows directly from supply voltage to ground. The last term represents leakage power, which is getting more and more attention as we progress towards deep sub-

micron technologies [63]. Primary reasons for $I_{leakage}$ are substrate injection, gate leakage, subthreshold effects, etc.

Equation 2.1 specifies flip-flop power consumption depends heavily on its circuit structure and input data activities. All nodes in the circuit involve in total power dissipation of the circuit, so equation 2.1 is applicable to every single node in the circuit. In well-designed sequential circuits, switching component is the dominant term, thus, the goal of a low-power circuit designer should be minimizing it while maintaining the required functionality and finding the cost of such minimization in terms of area and performance.

$$\begin{aligned} P_{total} &= DynamicPower + DirectPathPower(ShortCircuit) + Leakage \\ \implies P_{total} &= DA(C_L V_{DD}^2 f_{CK}) + I_{SC} V_{DD} + I_{Leakage} V_{DD} \end{aligned} \tag{2.1}$$

2.2.2 Timing

The performance of a flip-flop is qualified by four important delay terms which are, D-C (Data-to-Clock), C-Q (Clock-to-Output), D-Q (Data-to-Output) and hold time. D-C and D-Q delays are often referred as setup time and propagation delay, respectively. Setup and hold time define the relationship between clock and input data.

2.2.2.1 Setup Time (D-C Delay)

In order to function correctly, an edge-triggered flip-flop needs input data to be stable some time before the arrival of the active clock edge. The data value must stay stable during this time to ensure that flip-flop retains the correct value at output. Setup time with low-to-high transition of data can be different from high-to-low transition of data. Thus, the maximum value obtained between these transitions is considered as setup time.

$$t_{setup} = max(t_{setupLH}, t_{setupHL}) \tag{2.2}$$

2.2.2.2 Hold Time

Flip-flop correct operation needs data signal to be stable for some time after the passing of clock edge; this time is known as hold time. Hold time can also be negative, which means data can be altered even before the clock edge and still previous value will be stored.

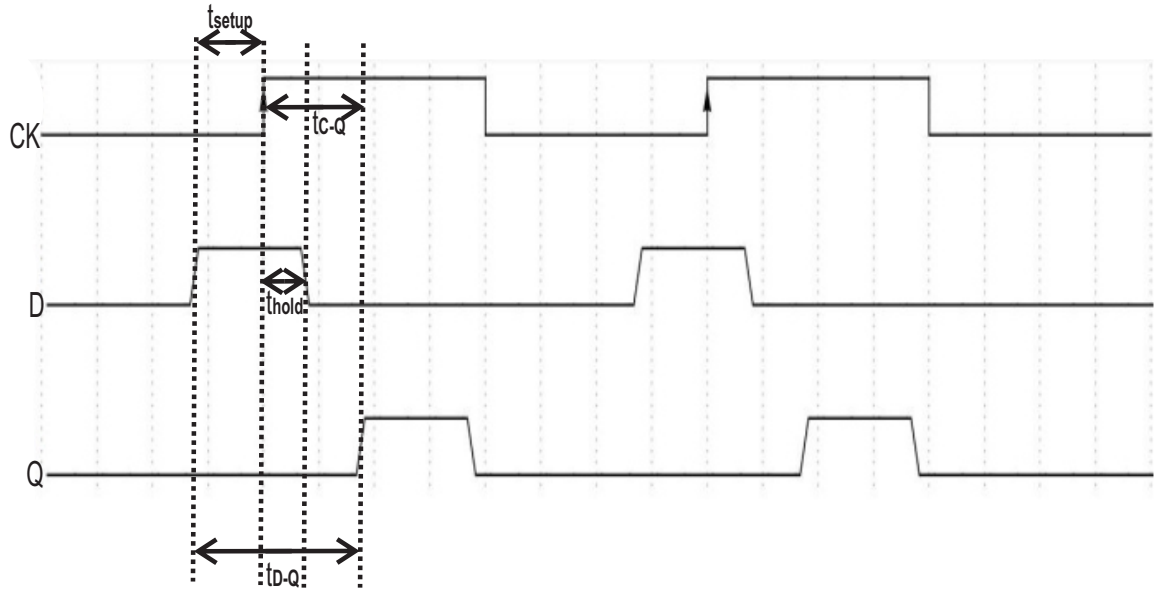


Figure 2.7: Flip-flop Timing Diagram [10].

Again, hold time for low-to-high transition can be different from high-to-low transition of data; thus, the maximum value obtained between them is chosen as a hold time.

$$t_{hold} = max(t_{holdLH}, t_{holdHL}) \tag{2.3}$$

2.2.2.3 C-Q Delay

C-Q delay is the time interval between clock edge and output signal edge. It gives the information that when new output begins being stable after the arrival of clock edge signal.

$$t_{C-Q} = max(t_{CQ_{LH}}, t_{CQ_{HL}}) \tag{2.4}$$

2.2.2.4 Propagation Delay (D-Q)

Propagation delay is the time delay between data signal to propagate at the output. It is sum of D-C and C-Q delays. Mathematically,

$$t_{D-Q} = t_{D-C} + t_{C-Q} \tag{2.5}$$

Generally, propagation delay for low-to-high transitions differs from high-to-low transitions. Therefore, maximum value from these two is chosen as a propagation delay.

$$t_{D-Q} = max(t_{DQ_{LH}}, t_{DQ_{HL}}) \tag{2.6}$$

The definitions of D-C, C-Q, D-Q, and hold time are illustrated in the timing diagram of Figure 2.7.

2.2.3 Power-Delay-Product (PDP), and Energy-Delay-Product (EDP)

PDP is a performance-oriented metric and defined as a product of total power consumption and D-Q delay. It is viewed as the amount of energy consumed in each switching event. Equation 2.7 defines PDP in terms of DA, C_L and V_{DD}.

$$PDP = DA(C_L V_{DD}^2 f_{CK})/f_{CK} = DA(C_L V_{DD}^2) \tag{2.7}$$

An ideal flip-flop is fast in speed and consumes less energy. The Energy-Delay-Product (EDP) is a combined metric that brings those two elements together, and is generally used as the ultimate quality metric [9]. EDP is equivalent to power-delay^2.

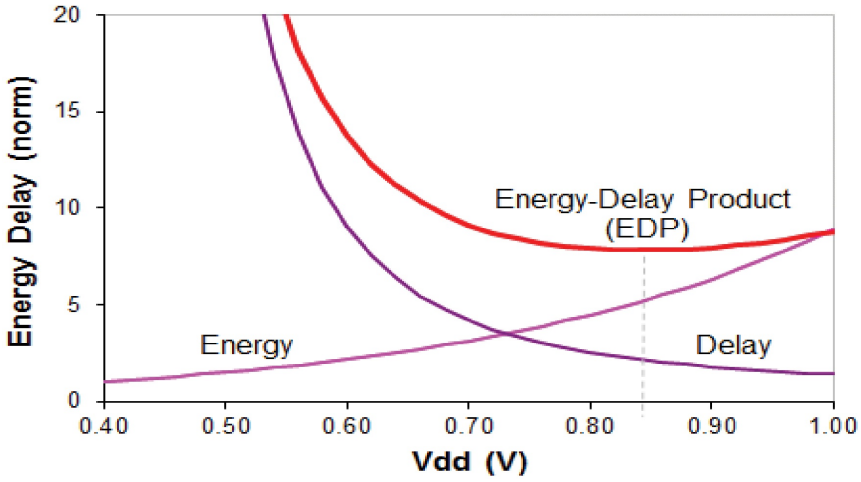


Figure 2.8: Normalized delay, energy, and energy-delay plots for CMOS inverter [11].

When there is a need for low-power and high-speed, PDP and EDP play a vital role. PDP measures energy needed for a switching gate, and it requires optimum voltage as

lowest possible to achieve minimum performance. Low PDP energy-efficient circuits may be slow in performance and in such cases, EDP is preferred as a figure of merit. EDP accounts for both energy and performance. Higher voltages decrease delay but increase energy, similarly, lower voltages decrease energy but increase delay; thus, in both cases, there exists an optimum supply voltage. Figure 2.8 illustrates the trade-off between delay and energy.

2.3 Review of the State-of-the-art Low-power Single-edge Triggered TSPC Flip-flops

2.3.1 Adaptive Coupling Flip-flop (ACFF)

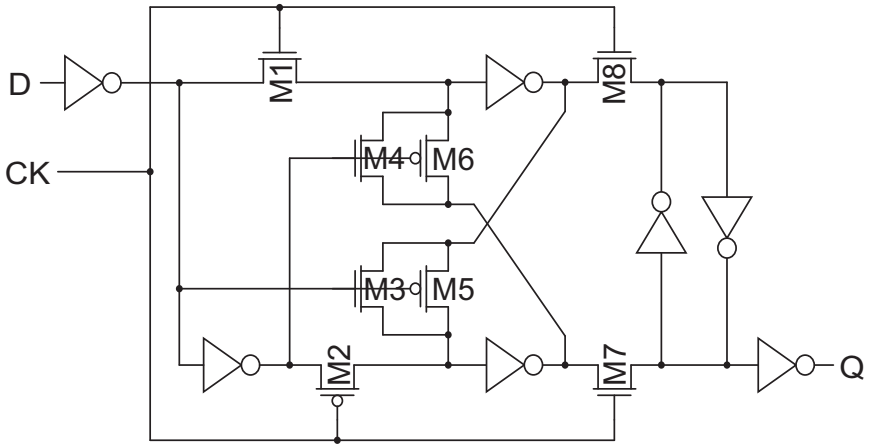


Figure 2.9: Circuit Diagram of the ACFF Proposed in [12].

As illustrative in Figure 2.9, the ACFF was presented in 2011, with the clock load of four transistors. At low DA, ACFF minimizes clock load and power consumption dramatically. However, at high DA and higher clock frequencies, its contention restricts its performance and power-efficiency despite the fact that adaptive coupling is offered to reduce contention when the stored value changes. Furthermore, transistors in contention need to be up sized, thus consuming more area.

2.3.2 Static Single-phase Clocked Flip-flop (S2CFF)

In 2014, a contention-free, pre-charging based S2CFF with five clock transistors (as shown in Figure 2.10) was introduced in [13]. In this flip-flop, node X is pre-charged by M10, which leads to improved power-efficiency at high Data Activities (DAs). However, at low DAs, the power-efficiency is poor as node X is connected to 8-transistors.

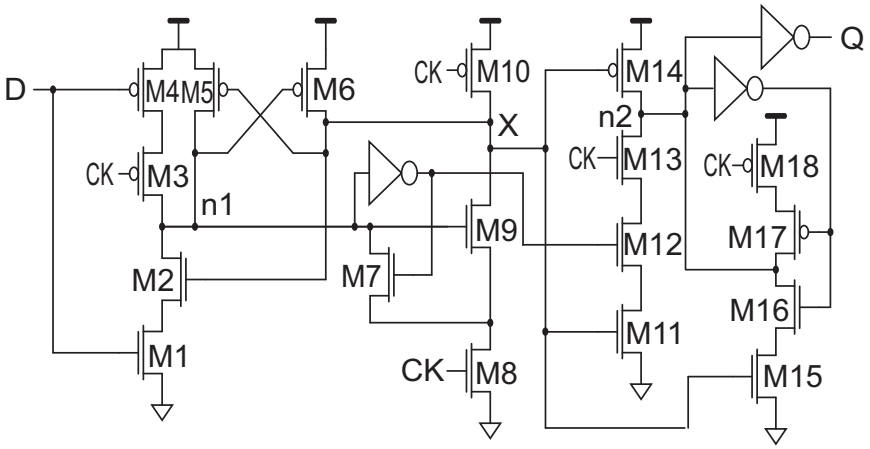


Figure 2.10: Circuit Diagram of the S2CFF Proposed in [13].

2.3.3 Topologically Compressed Flip-flop (TCFF)

A TCFF depicted in Figure 2.11 was presented in [14] to further minimize clock power. For low DAs, TCFF significantly reduces overall power. However, When CK = "0" and data changes from "0" $\rightarrow$ "1", there is a transient short-circuit path (the red path in Figure 2.11) that lowers M6's source voltage (through the blue path), slowing the charging process of node N2. This temporary short-circuit significantly increases the D-Q delay and degrades low-voltage behavior. Therefore, TCFF is a low-power flip-flop with a relatively large D-Q delay, particularly at low voltages.

2.3.4 18-T Low-power Flip-flops

An 18-T low-power flip-flop as illustrated in Figure 2.12 was introduced and implemented in 28 nm FDSOI technology [15]. Four transistors make up the clock load of this flip-flop,

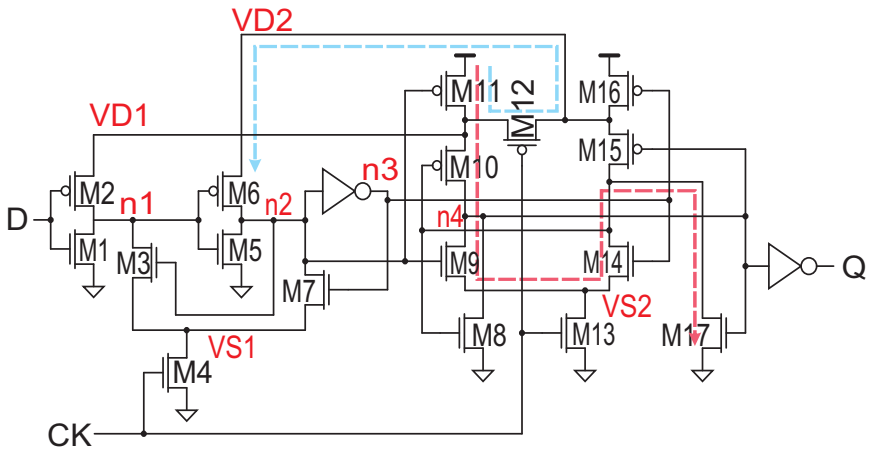


Figure 2.11: Circuit Diagram of the TCFF Proposed in [14].

which is referred to as TSPC18. As reported in [15], the TSPC18 consumes 40% less power compared to TGFF at 0.4 V. However, it has contention and interconnect in poly, and back gate biasing is needed to change the threshold voltages of transistors (M7, M8, M9, M13, M14, and M16) used in feedback paths. Furthermore, the output buffer uses an NMOS (M15) as a pull-up transistor, which makes the logic not fully complementary.

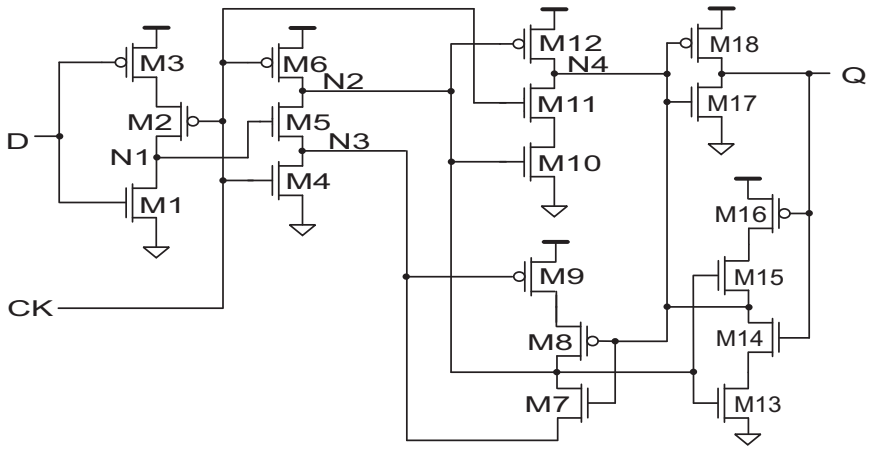


Figure 2.12: Circuit Diagram of the 18-T Low-power Flip-flop (TSPC18) Proposed in [15].

Another 18-T low-power flip-flop, referred as 18TSPC shown in Figure 2.13 was proposed in [16]. This flip-flop has four clock transistors and further enhances the the power-efficiency at high DA.

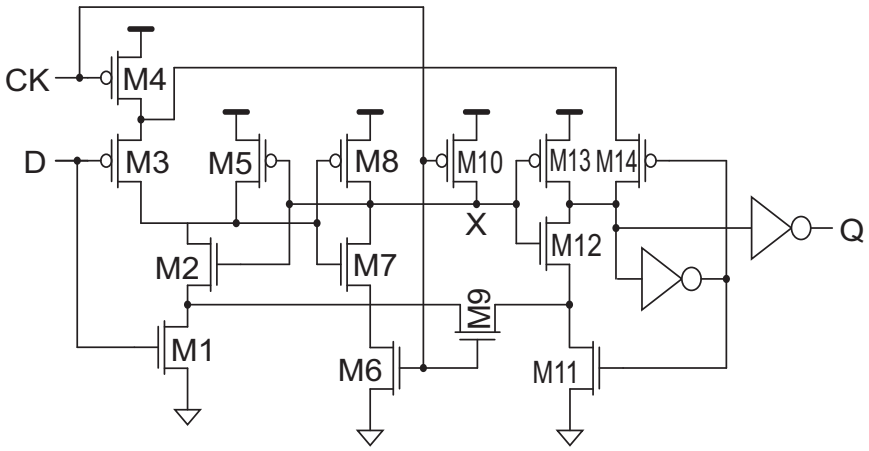


Figure 2.13: Circuit Diagram of the 18TSPC Proposed in [16].

2.3.5 Low-power at Low Data Activity Flip-flop (LLFF)

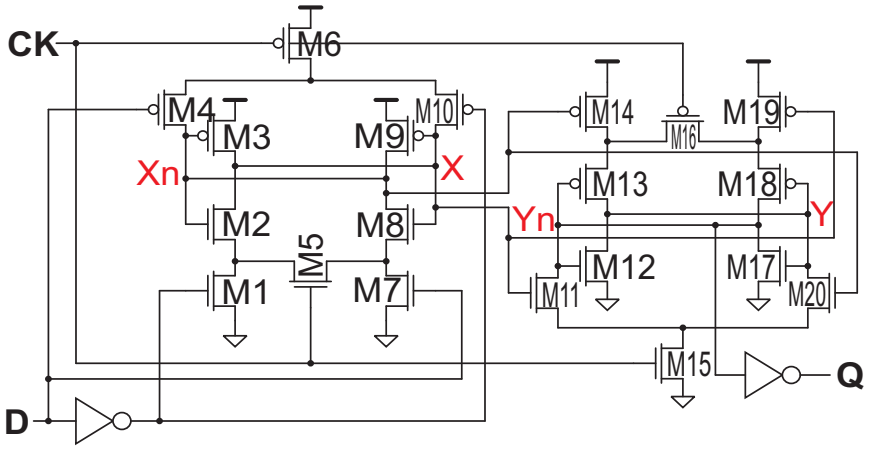


Figure 2.14: Circuit Diagram of the LLFF Proposed in [17].

LLFF was primarily designed to reduce the total power at low DAs. LLFF has a clock load of four transistors and requires differential data input as shown in Figure 2.14 [17]. Master and slave latches complement each other with respect to clock. When CK = "0", M6 and either M4 or M10 are turned on. Meanwhile, M1 or M7 is also turned on. Assuming the initial low data value (X = "0", Xn = "1") is swapped by high. When CK is low, M1, M10 and M6 are switched on while M7, M4, and M5 are switched off. As a

result of this configuration, data writing is free of contention. When CK toggles to high, M6 is switched off and M5 is switched on, ensuring that the data in the master latch is not affected by a subsequent data change. The slave circuit is a mirror of the master circuit, and data is sent to the slave latch when the "0" → "1" transition occurs at CK. A negative edge-triggered LLFF can also be made by swapping the master and slave latches.

2.3.6 Redundancy-eliminated Flip-flop (REEF)

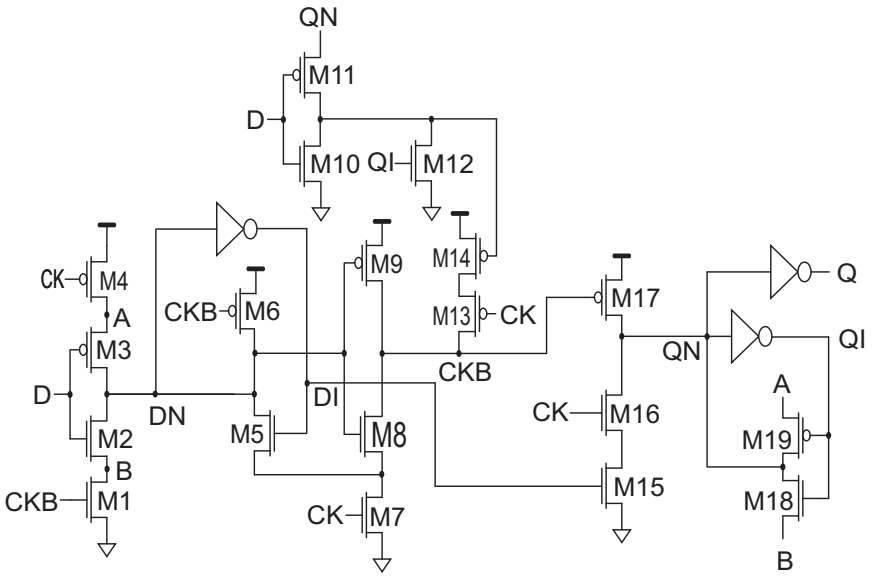


Figure 2.15: Circuit Diagram of the REEF Proposed in [18].

REEF as shown in Figure 2.15 was proposed in [18]. This flip-flop has four clock transistors and removes the unwanted transitions of internal nodes. As in the case of 18TSPC, redundant transition occurs at node X (in Figure 2.13) when D = CK = 0 (assume Q = 0). As illustrated in Fig. 12, the redundant transitions at node CKB are avoided at the expense of additional transistors. Consequently, the REEF has 25 transistors and additional delay compared to 18TSPC. However, at low DA it is power-efficient. Moreover, this flip-flop struggles with low-power, low-energy, and high-performance.

2.4 Review of the State-of-the-art Low-power TSPC DET Flip-flops

Researchers have used several techniques, such as pulsed-latch [64, 65], C-element [66, 67], and latch-multiplexer (latch-mux) [19, 20, 21, 22] to realize DET FFs. Every method has its own merits and demerits. For example, DET FFs with pulsed latch type require a pulse generator and a pulse latch. A synchronized clock pulse is produced by a pulse generator at both rising and falling clock edges. These clock-synchronized pulses serve as triggers for the pulse latches' latching mechanism. In such cases, timing is crucial because pulse width define the transparency window of the latches. Nevertheless, the pulse properties are easily influenced by Process, Voltage, and Temperature (PVT) fluctuations since conventional pulse-generating circuits rely on transistor delay to regulate the pulse length. Because of this, a precise pulse-generation circuit that can withstand PVT fluctuation tolerance is needed, which adds significantly to the overhead in power and area.

In a C-element type DET FFs, the circuit uses components known as C-elements. When two input values for a C-element are the same, the output is updated to reflect the input value; however, when two input values vary, the previous output value is kept. As a result, depending on the input conditions, C-element type DET FFs can latch new data or retain existing data. While C-element-type DET FFs have some benefits, using back-to-back inverters to store data always leads to contention. Consequently, in order to increase reliability and make them work at low-voltage, C-element-based DET FFs need to be carefully designed.

Latch-MUX type DET FFs configuration employs two input latches and a multiplexer at the output, as shown in Figure 2.16 Since the two latches are level-triggered at different clock levels, there is always one opaque latch and one transparent latch. The clock determines the DET's output through control of the multiplexer. In this study, we considered only latch-mux type DETs owing to their potential for low-power, low-voltage operation and ability to tolerate PVT variation as compared to pulse DET or C element type DET FFs.

2.4.1 Static Dual-edge Triggered Flip-flop (SDET)

Figure reffig:SDET depicts a latch-mux type Static DET flip-flop SDET [19]. Each latch in this flip-flop is made up of a transmission gate and two inverters connected back-to-back. The original design of the SDET in [19] employed single NMOS (or PMOS) pass

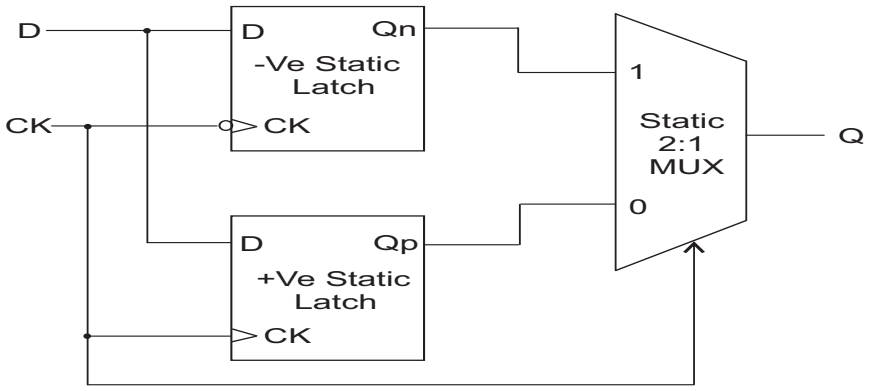


Figure 2.16: Block Diagram of the TSPC DET Flip-flop.

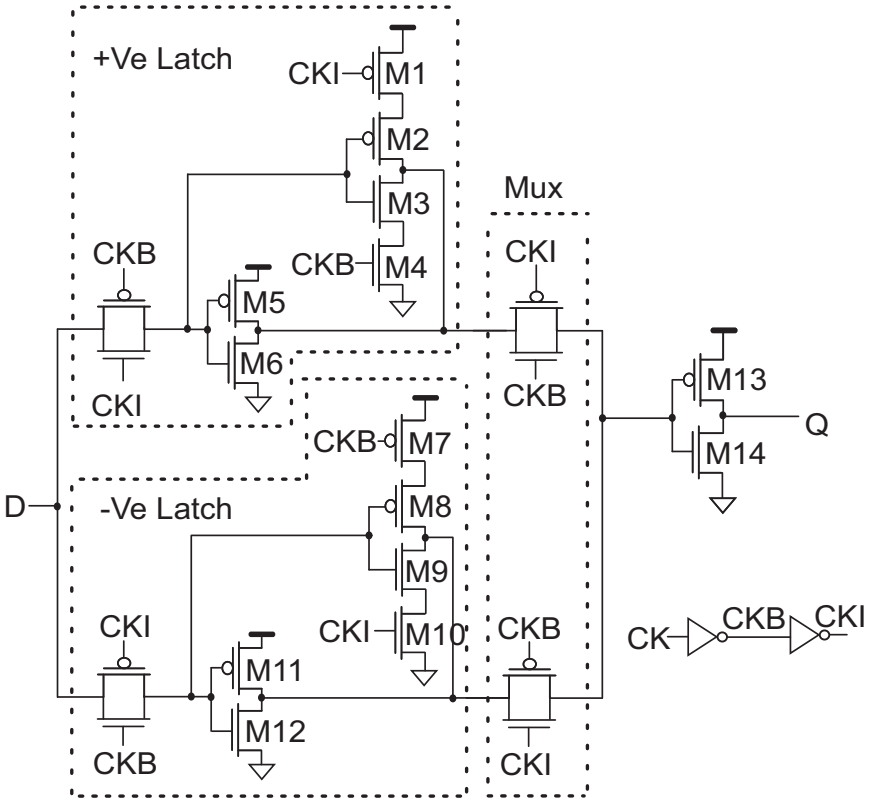


Figure 2.17: Schematic Diagram of the SDET Proposed in [19].

gates, making it vulnerable to variations in voltage and process. To compare with other DET FFs with better reliability, transmission gates are employed in this research instead of pass gates for analysis and simulations. In SDET, the clock input (CK) is converted into complementary internal clock signals (CKB, CKI) using 2-stage inverters, which in turn control two latches and a multiplexer. Since CKB and CKI are produced using two-stage inverters, they may briefly overlap. In low-voltage regimes, when delay variation is amplified, this may get worse. Moreover, during clock overlap, the two transmission gates that make up a multiplexer can be switched on simultaneously, potentially corrupting the data in a latch.

2.4.2 TSPC Static DET Flip-flop (TSPC-SDET)

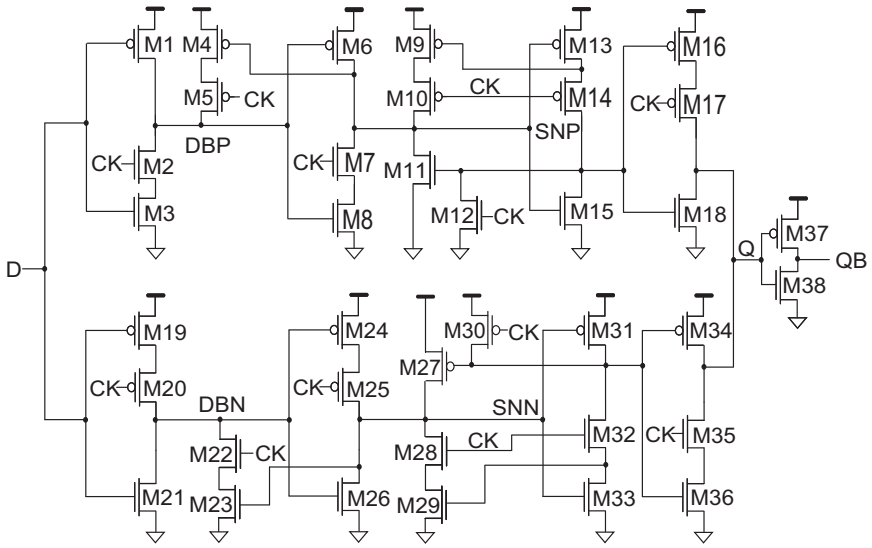


Figure 2.18: Schematic Diagram of the TSPC-SDET Flip-flop Proposed in [20].

Figure 2.18 shows the latch-mux type TSPC Static DET Flip-flop (TSPC-SDET). With the TSPC technique, this flip-flop solves the problem of two-phase clock overlap, albeit at the expense of using more transistors. TSPC-SDET needs a total of 38 transistors, including 12 clock transsitors. Moreover, owing to its weak pull-up and pull-down, the voltage scaling of the TSPC-SDET is limited and susceptible to variation. For instance, a PMOS on the pull-down path prevents the transistor M9's gate from being completely pulled down to ground when CK = 0 and SNP = 1 in the positive latch. As a result, M9 just slightly pulls up M9's drain. Similar to this, the drain of M29 is weakly pushed down

when CK = 1 and SNN = 0 in the negative latch. Because of this, although it makes the claim to be a fully static DET flip-flop, it is not fully static, and as a result, it is not suitable for low-voltage operation.

2.4.3 Fully Static True Single-phase Clocked Dual Edge-triggered Flip-flop (FS-TSPC-SDET)

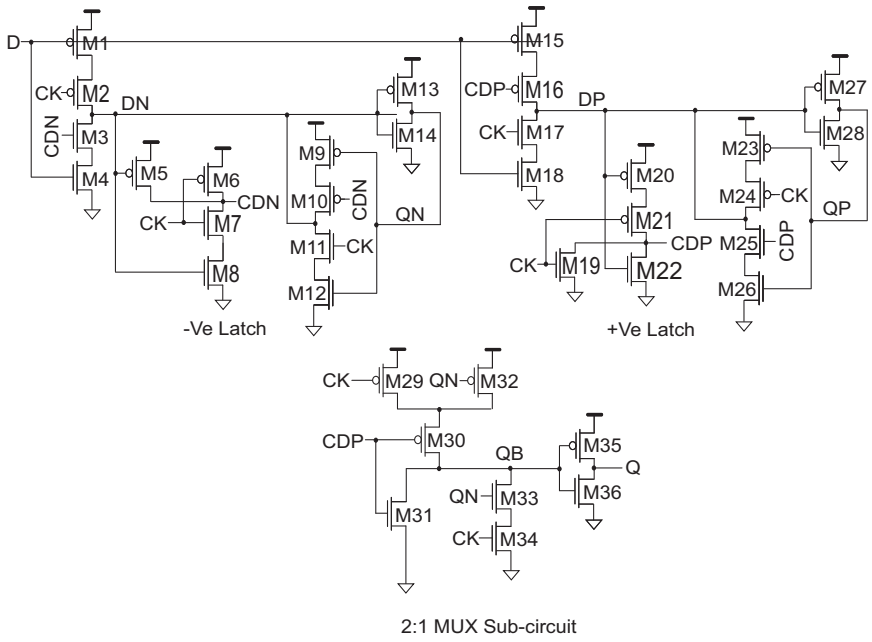


Figure 2.19: Schematic Diagram of the FS-TSPC-DET Proposed in [21].

Figure 2.19 illustrates the schematic diagram of a Fully Static True Single-phase Clocked DET Flip-flop (FS-TSPC-DET) [21]. This flip-flop needs a total of 36 transistors, including 10 clock transistors. FS-TSPC-DET reduced the total power consumption, but it still struggles with the internal redundant transitions. For example, when D stays at logic high, DP will stay at logic low. Transistors M19-M22 follow the logic of an inverter with one clocked PMOS and one clocked NMOS. Therefore, continuous switching of the two clocked transistors causes an implicit redundant transition at node CDP. Similarly, transistors M5-M8 follow the logic of an inverter when DN stays at logic high; thus, the continuous clock-based switching of CDN causes an implicit redundant transition. As a result, FS-TSPC-DET consumes more power and energy.

2.4.4 Low-power Redundant-transition-free TSPC DET Flip-flop Using single-transistor-Clocked Buffer (STC-DET)

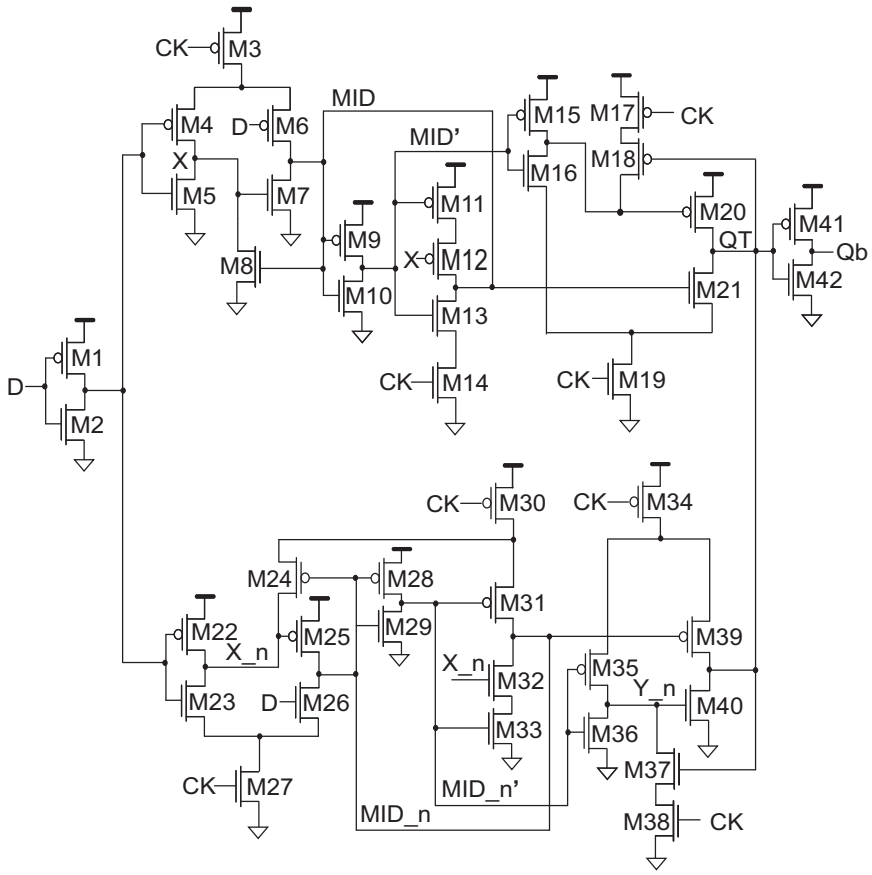


Figure 2.20: Schematic Diagram of the STC-DET Proposed in [22].

Figure 2.20 shows the recently presented Low-power Redundant-transition-free TSPC Dual-edge-triggered Flip-flop using Single-transistor-clocked Buffer (STC-DET) [22]. This flip-flop has one of the lowest power consumptions at low DA; however, increases dramatically with an increase in DA. Moreover, this flip-flop suffers from poor timing because of a large C-Q delay and needs a total of 42 transistors, including 8 clock transistors.

2.5 Summary

In this chapter, we have discussed different general types of FFs along with state-of-the-art SET and DET TSPC FFs. Flip-flop performance metrics such as Power, delay, and energy are also highlighted.

Chapter 3

Radiation Hardening Techniques and RHBD Flip-flops

3.1 Overview of the Radiation Hardened Techniques

Radiation-Hardening-By-Process (RHBP), and RHBD are the two primary types of radiation hardening techniques used in chip design. This chapter will explore several hardening methods.

3.1.1 Radiation-Hardening-By-Process

In this category, radiation hardening is achieved by suitably modifying the fabrication process. It is a complex and costly way to achieve radiation immunity. When compared to RHBD on similar process sizes, process hardening techniques provide a more compact design. However, modern hardened processes are a lot bigger than current industry standard processes.

3.1.1.1 RC Hardening

The best way to reduce specific single event effects is proven to be process hardening. The technologies that make use of these techniques are nonetheless bulky, power-hungry, and inefficient when compared to the benchmarks set by the circuit design industry today. Figure 3.1 illustrates the example of RC hardening [23]. In this figure, thin film resistors

are used between storing nodes to separate the driving devices in a bi-stable memory cell, while capacitors are attached to the transistor gates. This configuration produces a low-pass filter that cancels out all high frequency pulses, including SETs.

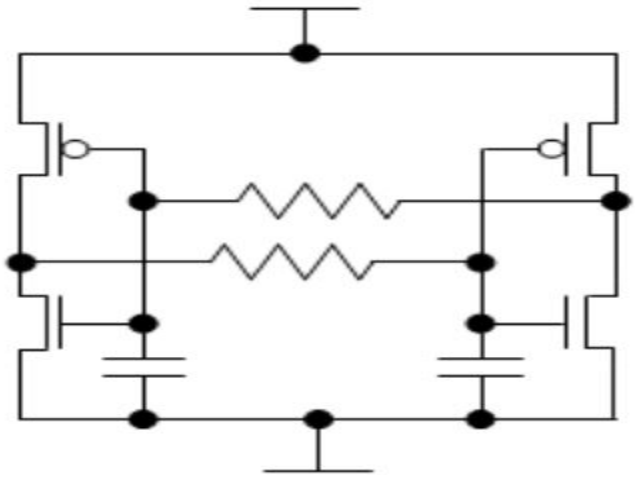


Figure 3.1: Circuit Diagram of RC Hardening as a Low-pass Filter Proposed in [23].

3.1.1.2 Magnetic Tunnel Junction (MTJ) Hardening

In MTJ hardening, the junction is created by separating two ferromagnetic metals with a thin insulating dielectric layer, which causes electrons and holes to produce a tunneling current between the two metals. When a magnetic field is applied, it creates a tunnelling magneto-resistance across the junction, which changes the current direction depending on the magnetization orientation in the metals [68, 69]. In radiation-hardening, tunneling current swiftly eliminates any accumulated holes or electrons caused by ion impacts from nodes, enabling fast SETs and SEU mitigation. Figure 3.2 shows the example of a magnetic hardening latch, where MTJ1 and MTJ2 are used to harden the latch. If an incoming particle destroys the dielectric layer, then magneto-resistance value decreases; as a result, hardening benefits lost [24]. Additionally, just like resistors used in RC hardening, MTJs produce a low-pass filter that restricts the usage of magnetic hardening to low bandwidth applications.

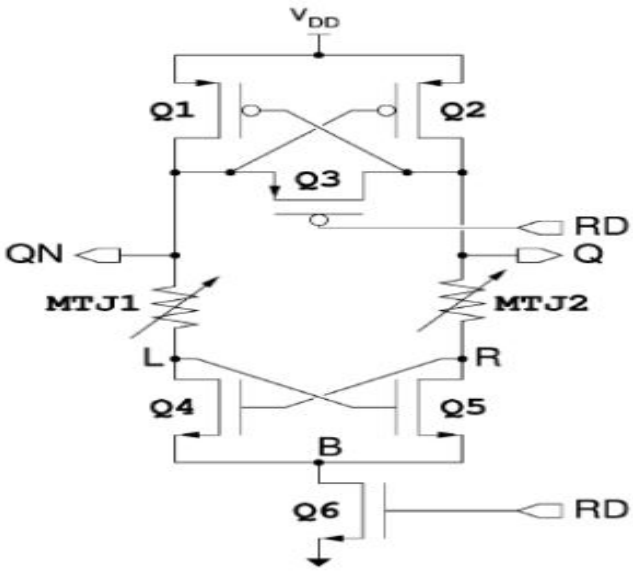


Figure 3.2: Circuit Diagram of the MTJ Hardening Proposed in [24].

3.1.2 Radiation-Hardening-By-Design (RHBD)

RHBD techniques allow current designs to scale with future process sizes. Therefore, RHBD implementation are important for modern processes used in hardened circuits. RHBD techniques are divided into four classes: RHBD at system level, RHBD at architecture level, RHBD at layout level, and RHBD at circuit level. At the system level, radiation hardness can be obtained by software techniques that can filter out accurate information from redundant data. Electronic systems with redundancy must be designed at this level. At the architectural level, Error Correction Code (ECC) circuitry is used to improve the ability of electronic devices to fix errors. In addition, placement techniques can be employed to mitigate the radiation's effects. At layout level, a number of strategies are used throughout the layout design to get rid of the harmful radiation impacts, including physical separation and guard rings. At circuit level, several circuit design strategies are used to create structures. Redundancy is one of the approaches used to decrease the impact of radiation on the circuit. In this thesis, we will be focusing on RHBD techniques at circuit level.

3.1.2.1 Redundant Latches

The basic structure of TMR method is shown in Figure 3.3 [25], where a majority voter is added to vote on the outputs from three identical modules. In sequential circuits, a module can be an unhardened latch or a regular D Flip-flop (DFF). All FFs or latches share the same clock and input data. In this system, if an ion strike affects one of the three circuits and causes a SEU, the majority voter can filter this SEU and output the correct data from the other two unaffected modules. The majority voter is basically a combinational CMOS gate (shown in Figure 3.4), that compares the logic values of three inputs and outputs the value that at least two inputs agree upon. Therefore, TMR is SEU-free and susceptible to SETs. When using TMR techniques, there are considerable size and power drawbacks, generally 3 to 4 times greater than a single module.

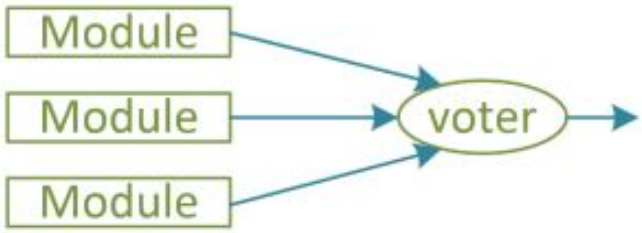


Figure 3.3: Block Diagram of TMR Flip-flop Implementation [25].

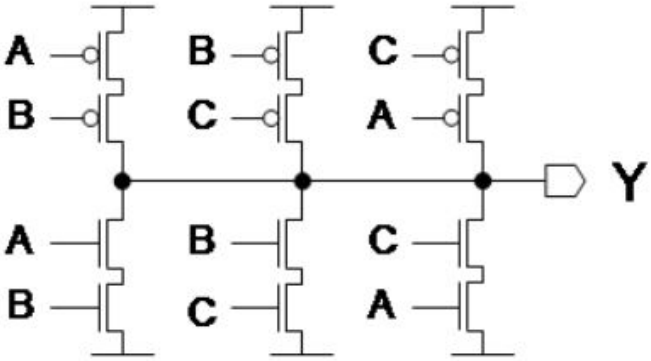


Figure 3.4: Circuit Diagram of Majority Voter with Inputs A, B, and C, along with Output Pin Y [26].

Dual modular redundancy has been tested as a low-power and small-size substitute for TMR, but other methods, like temporal hardening or interlocking, are needed to make

dual redundancy design [70]. Due to this, dual redundancy is generally employed as an error detection technique, and TMR is used for the construction of corrective circuits.

3.1.2.2 Temporal Hardening

Another particularly well-liked RHBD strategy is temporal hardening. This technique achieves temporal redundancy by physically separating nodes through the use of delay elements, as opposed to physically isolating important nodes and constructing several circuits, as done in TMR [71]. Delay elements add a t_δ, propagation delay from input, A, to output, Y. It is possible to use triple and dual redundant types of temporal redundancy.

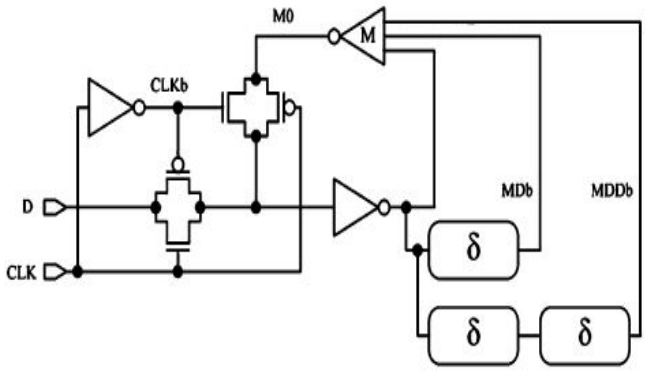


Figure 3.5: Circuit Diagram of a Temporal Latch Depicting Temporal Redundancy with Majority Voters Proposed in [27].

A temporal redundant latch is shown in Figure 3.5. The bi-stable memory cell is made up of an inverter and a feedback majority voter, whose inputs are separated in time by delays of 0, $1t_\delta$, and $2t_\delta$. The t_δ value is selected to be more than the maximum SETs time that the circuit is anticipated to experience. This guarantees that any pulse less than t_δ seen by the nodes Mb, MDb, and MDDb will not reach the majority voter inputs at the same time, and as a result, the latch will mitigate SETs shorter than that duration.

Muller C-element [28] can take the place of the majority voters to optimize both size and speed. This technique is also called guard-gate. This two-input device serves the same purpose as a majority voter in that the inputs must agree for the element to change state. This enables the C element to offer hysteresis when the input nodes are temporally separated. Figure 3.6 shows the schematic diagram of guard-gate. It acts like an inverter when inputs A and B are equal. When input A and input B are different, the guard gate's output is in a high impedance state and retains its previous value.

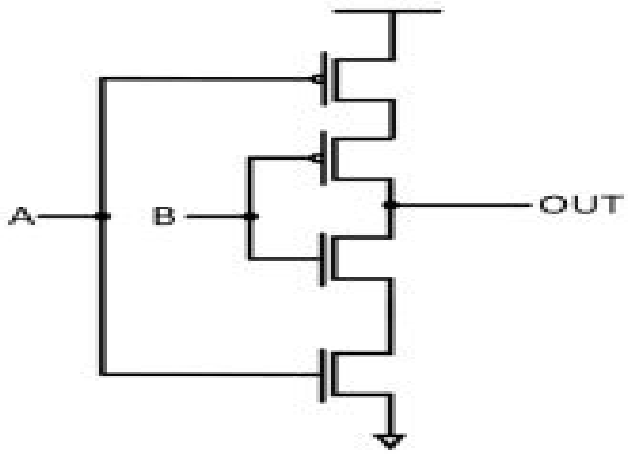


Figure 3.6: Circuit Diagram of Guard-gate [28].

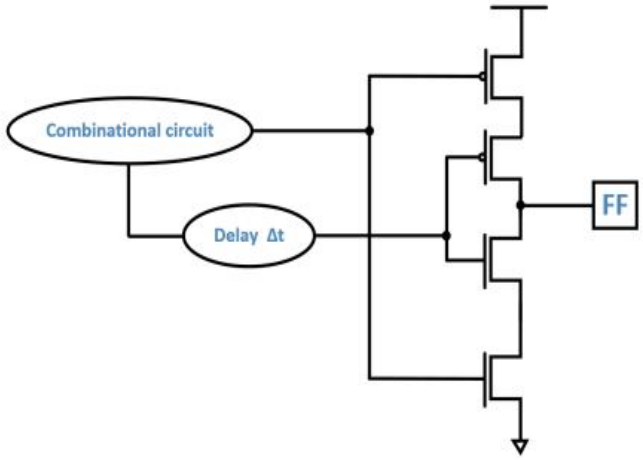


Figure 3.7: Guard-gate Used in a Combinational Circuit [28].

The application of guard-gates in combinational circuits is depicted in Figure 3.7. If the SETs pulse width is less than the delay unit and inputs A and B are substituted by the normal and delayed outputs of a combinational circuit, the guard-gate can eliminate the SETs pulses and output proper data to the subsequent flip-flop.

Similarly to TMR, temporal hardening implementations incur a high cost in terms of size and power. The delay components that provide the temporal separation are the main cause of these expenses. Therefore, particular consideration must be given while designing the delay elements to produce a low-power, compact, temporally hardened circuit.

3.1.2.3 Dual Interlocked Cell (DICE)

A DICE is a type of spatial redundancy design that has been in extensive use since it was first described in 1996 [29]. Figure 3.8 illustrates the basic structure of a DICE cell. It has four storage nodes, X1, X2, X3, and X4. Nodes X3 and X4 are complementary of nodes X1 and X2. For example, assume nodes X1 and X2 are logic '0' and nodes X3 and X4 are logic '1'. Then, transistors M5, M2, M7, and M4 are turned on, whereas M1, M6, M3, and M8 are turned off. The drain of the M1 transistor is sensitive to SETs. Node X1 will experience a positive voltage pulse if a particle hits it. The "ON" transistor M5 will drive node X1 to suppress this positive pulse, which may turn off M2 and turn on M8. Node X3 will be floating and retain its value when transistors M2 and M6 are "OFF". If M8 is turned on, then there will be a contention between M8 and M4. If M8 dominates M4, then M7 will be turned off, and node X2 will be floating and store its value. In the end, when a positive SETs pulse disappears, all storage nodes will restore their previous values. In conclusion, this DICE design is immune to SEU if only a single node is impacted.

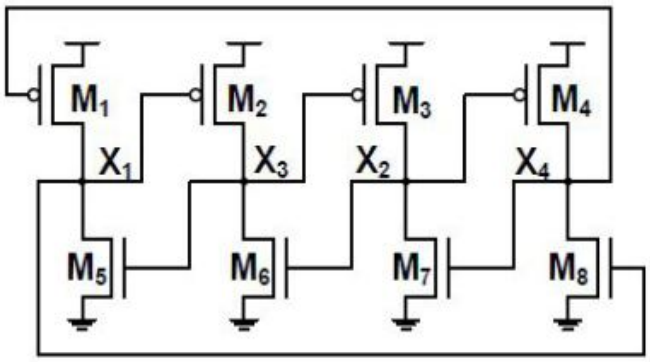


Figure 3.8: Schematic Diagram of the DICE Cell [29].

To successfully perform a write operation into the DICE, at least two nodes must be accessed simultaneously. A DICE cell has a smaller area and lower power consumption than a TMR structure. In static mode, there is no static current path between the VDD and the ground. The DICE has the additional benefit of requiring no fixed sizing of the transistors. Due to these advantages, the DICE structure is often used as a SEU-tolerant storage element. But this design has several flaws as well. The SEU that occurs when two of the nodes are affected simultaneously is the most evident drawback. This problem is solved in [30], where a DICE cell is combined with guard-gate as shown in Figure 3.9, this design is named as 4-TAG latch. During the radiation experiment, it has reported no error even at 175 MeV.cm^2/mg Linear Energy Transfer (LET) value in the AMI 0.5 um process [30].

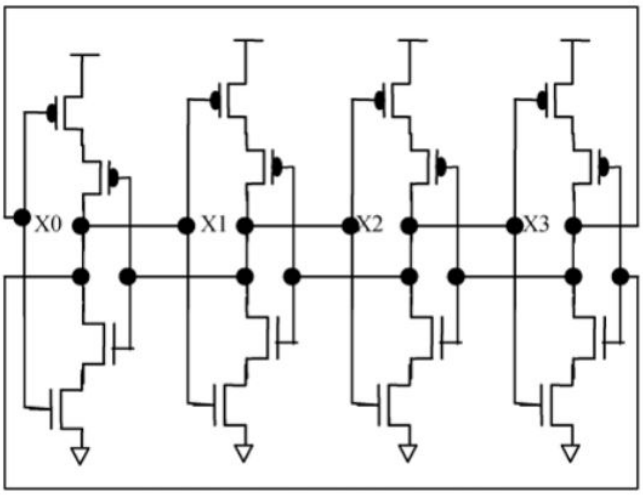


Figure 3.9: DICE Latch with 4 Guard-gate Proposed in [30].

3.1.2.4 Quatro Cell

Quad-node ten transistor cell (Quatro or Quatro-10T) is another well-liked SEU-tolerant storage cell [31]. This Quatro-10T cell was initially proposed as a hardened memory cell for Static Random Access Memory (SRAM). In sequential circuits, it can also be implemented as a latch. Figure 3.10 shows the circuit diagram of Quatro-10T cell [31].

With symmetrical structure, the Quatro cell stores differential data at four nodes X1, X2, X3, and X4. X1 and X3 have the same value, and X2 and X4 have the same value. This Quatro cell is immune to positive pulses at nodes X4 and X3, and negative pulses at

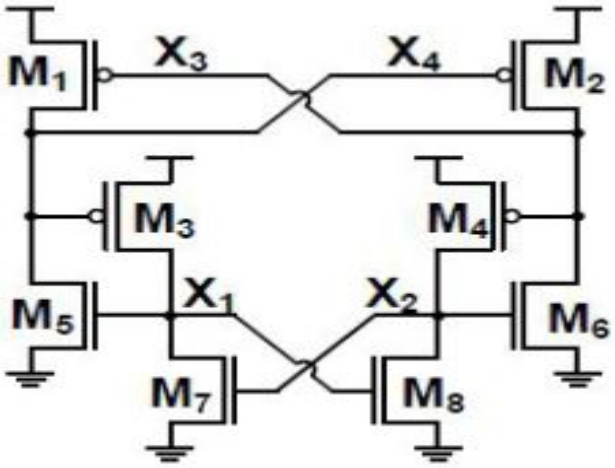


Figure 3.10: Schematic Diagram of the Quatro cell Proposed in [31].

nodes X1 and X2. For example, assume X4 is logic '0', and X3 is logic '1'. If a positive pulse occurs at node X4, the 'ON' PMOS transistors M3 and M2 will be turned off, which in turn causes X1 and X3 to be floating nodes with an unchanged value. If node X1 has a negative SETs pulse, then 'ON' NMOS transistors M5 and M8 will be turned off; as a result, nodes X4 and X2 will be floating and maintaining their values. However, a negative pulse at X4 and X3, and a positive pulse at X1 and X2 may cause SETs. For instance, a negative SETs pulse at node X3 will turn on both PMOS transistors M1 and M4, resulting in contention at nodes X4 and X2. If the SETs pulse is large enough, then this contention may flip the Quatro cell, and a SEU will occur. Proper transistor sizes can weaken this contention and improve the robustness of Quatro cell.

3.2 Existing Radiation-Hardened-By-Design Flip-flops

The 8T DICE proposed in [29] serves as the foundation for the most popular RHBD FFs. These FFs either employ a single DICE cell as the storage element or use two DICE cells in a master-slave arrangement. The flip-flop discussed in [72] is an illustration of the former.

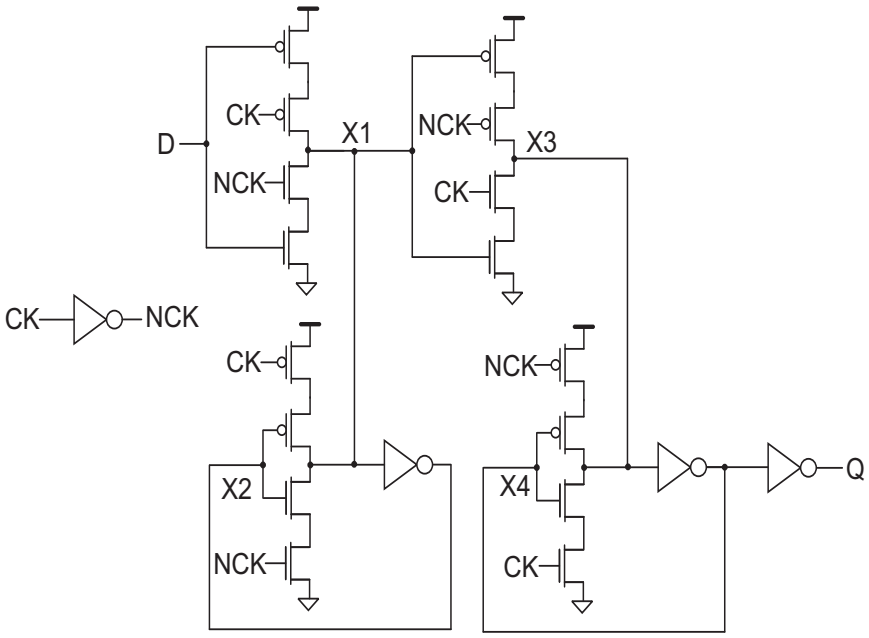


Figure 3.11: Schematic Diagram of the Master-Slave D Flip-flop (MS-DFF) [32].

3.2.1 MS-DICE, and MS-Quatro Flip-flops

In [32], a standard master-slave based D flip-flop (MS-DFF) as shown in Figure 3.11 is used as a regular flip-flop for reference, where cross-coupled inverters are used as a storage element. In this flip-flop storage elements are replaced with corresponding DICE and Quatro cells in master and slave latches and proposed as MS-DICE (as shown in Figure 3.12) and MS-Quatro (as shown in Figure 3.13) flip-flops, respectively. In all three FFs, tri-state inverters are used as transfer gates.

3.2.2 C^{2}MOS Quatro Flip-flop

A C^{2}MOS-Quatro flip-flop as shown in Figure 3.14 was proposed in [33]. This flip-flop has two stages: a C^{2}MOS transfer gate is used to move data in and out to the storage element, while a Quatro cell is used as a storage element. This flip-flop is power-efficient and works like a master-slave flip-flop. However, it suffers with poor performance, which could be improved by upsizing transistors in the transfer gate.

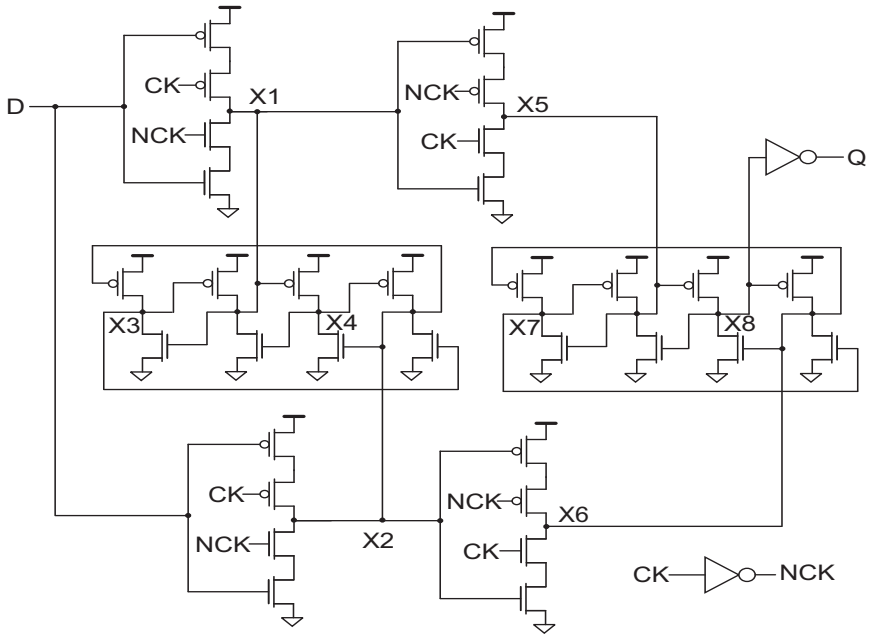


Figure 3.12: Schematic Diagram of the Master-Slave DICE Flip-flop (MS-DICE) [32].

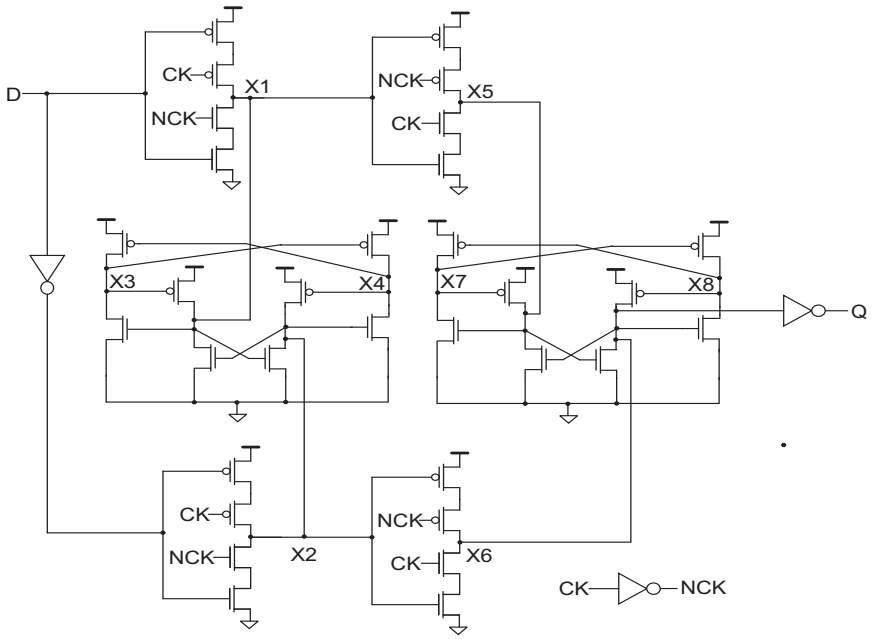


Figure 3.13: Schematic Diagram of the Master-Slave Quatro Flip-flop (MS-Quatro) [32].

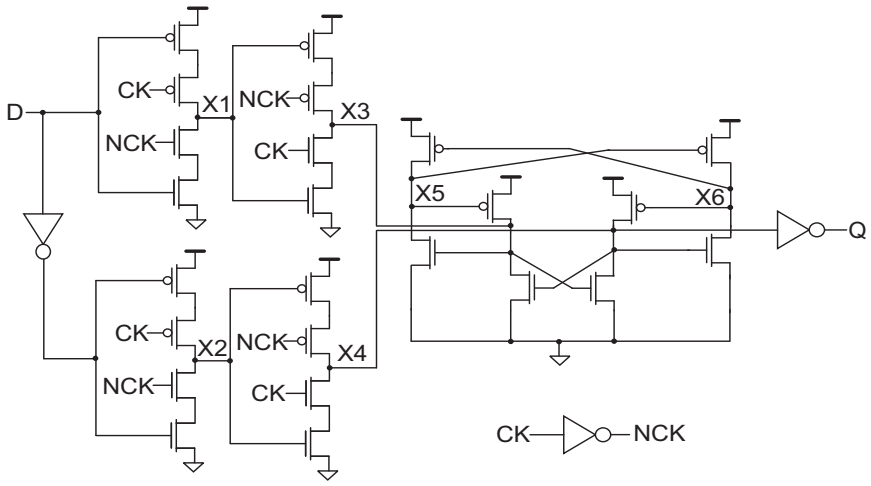


Figure 3.14: Schematic Diagram of the C^{2}MOS Quatro Flip-flop (C^{2}MOS-Quatro) [33].

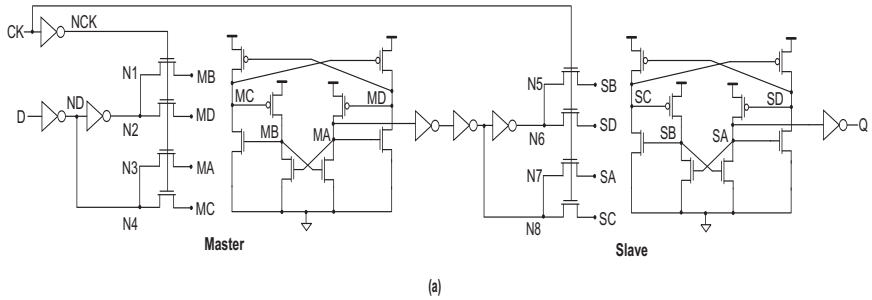


Figure 3.15: Schematic Diagrams of the Radiation Hardened D Flip-flops using (a) Traditional Quatro Cell (TQ-Quatro), and (b) Modified Quatro Cell (MQ-Quatro) [34].

3.2.3 Traditional Quatro (TQ-DFF), and Modified Quatro (MQ-DFF) Flip-flops

In [34], a traditional Quatro TQ-Quatro based D flip-flop (as shown in Figure (a) 3.15) is compared with a proposed modified Quatro (MQ-Quatro) based D flip-flop (as shown in Figure (b) 3.15), where two extra transistors are added in each half output latch of the Quatro cell to make the guard-gates. The integration of C-element mitigates the Single Node Upset (SNU) issues of traditional Quatro cell, however, it pays the penalty of extra area, power, and delay. (TQ-Quatro) has a total transistor count of 36, and (MQ-Quatro) has a total transistor count of 44.

3.3 Summary

In this chapter we have discussed different radiation hardening techniques, with the main focus on RHBD at circuit level. Different designs like TMR, C-element, DICE, and Quatro cell based were elaborated. DICE and Quatro are the two most popular radiation-hardened cells used in the RHBD designs.

Chapter 4

Low-power Single-edge Triggered TSPC Flip-flops

Power and energy consumption is one of the primary design constraints for ICs [73, 74, 75]. Aiming for high-performance computing at lower energy consumption, portable and handheld electronics are becoming more and more popular. In order to reduce the overall cost of manufacturing, a Very Large Scale Integration (VLSI) designer aims to minimize area and complexity while preserving the ideal power-to-delay ratio for a circuit. FFs are a fundamental component of digital circuits. In a typical processor, hundreds of thousands of FFs are used [52]. Therefore, their speed, power, and energy have a significant impact on the overall performance of a digital system [16, 52, 76, 15, 77, 78, 65, 79, 67, 80, 47]. Moreover, a clock network takes up a significant portion of the total power consumption of a modern SoC, the power used by the FFs and clock distribution networks in a typical digital system design can account for 20% to 45% of the system's overall power [81, 82, 83, 84]. Additionally, pipelines are frequently employed to increase system throughput, which adds to the load on the clock network. Therefore, low-power FFs are desirable to reduce the overall power consumption of a digital system.

4.1 Proposed Low-power TSPC SET Flip-flops

Dynamic power consumption of a flip-flop is proportional to the input DA, and the typical DA range for FFs is between 5 to 15% [12, 14]. Therefore, the motivation is to design a low-power flip-flop with the aforementioned DA range. One of the ways to accomplish this

objective is by lowering the clock transistors count in a flip-flop as they toggle at the clock frequency. The proposed flip-flops require a single-phase clock with only two and three clock transistors.

4.1.1 21TSPC Flip-flop with only Three Clock Transistors

Figure 4.1 shows the basic idea behind the proposed flip-flop. The master-slave multiplexer setup, as seen in section (a), serves as the framework for the proposed flip-flop. When CK = 0, latch L1 samples the data, and when CK = 1, latch L2 samples the L1. The expressions L1 = D.CK' + L1.CK and L2 = L1.CK + L2.CK' represent its logical behaviour. Multiplexers are converted into corresponding logical gates in section (b). In section (c), repeated logical gates with the identical inputs (highlighted in red color in section (b)) are eliminated. Section (d) then converts logic gates into corresponding universal logic "NAND" (NAND) gates. A clock and its complement are required for this circuit. By substituting logic "OR" (OR) gates O1 and O2 for NAND gates N2 and N4, respectively, in section (e), the clock inverter is removed. In this design, master latch samples the data when clock is low, and data is transferred to the slave at the positive clock edge transition. Logically, L1 = D'.CK' + L1.CK, L2 = L1.CK + L2.CK'. Section (f) describes how to create the logic "OR-AND-INVETER" (OAI21) compound, which requires only six transistors to implement, using the logical gates O1 and N3, and O2 and N5. The transistor-level schematic of the flip-flop in section (g) can be realized using the complex gate schematic of section (e); this takes 20 transistors total, including 6 clock transistors.

It is possible to compress the red-highlighted clock transistors in section (g) together. It is only necessary to pre-charge node n1 when D = "1", and CK = "0". To eliminate unnecessary internal node transition at n1, a data transistor PMOS M5 is added in series with M1 to make the inverter at node X1 as illustrated in section (h). This node X1 generates complement of data and is connected to the gate of another added PMOS M12 transistor, which turns-on only when D = "1". Similarly, the clock transistors M6, M10, and M16 of section (g) that are indicated in blue can also be combined to form a single clock transistor, M10, as seen in section (h). When the CK = "1" and high data is already latched in the slave, the node X1 should have a path to ground; in this case, a combination of transistors M16 and M10 shorts the node X1 to ground. Clock transistor M10 provides the clock boundary for data transfer from master to slave when D = "1". When CK = "1", D = "1", the transistors M21 and M10 in section (h) pull the node X2 to ground.

Figure 4.2 depicts the working principle of proposed flip-flop for various clock and data states. When CK = "0", D = "0", and Qprev = "1", node L1 becomes high. The node n1

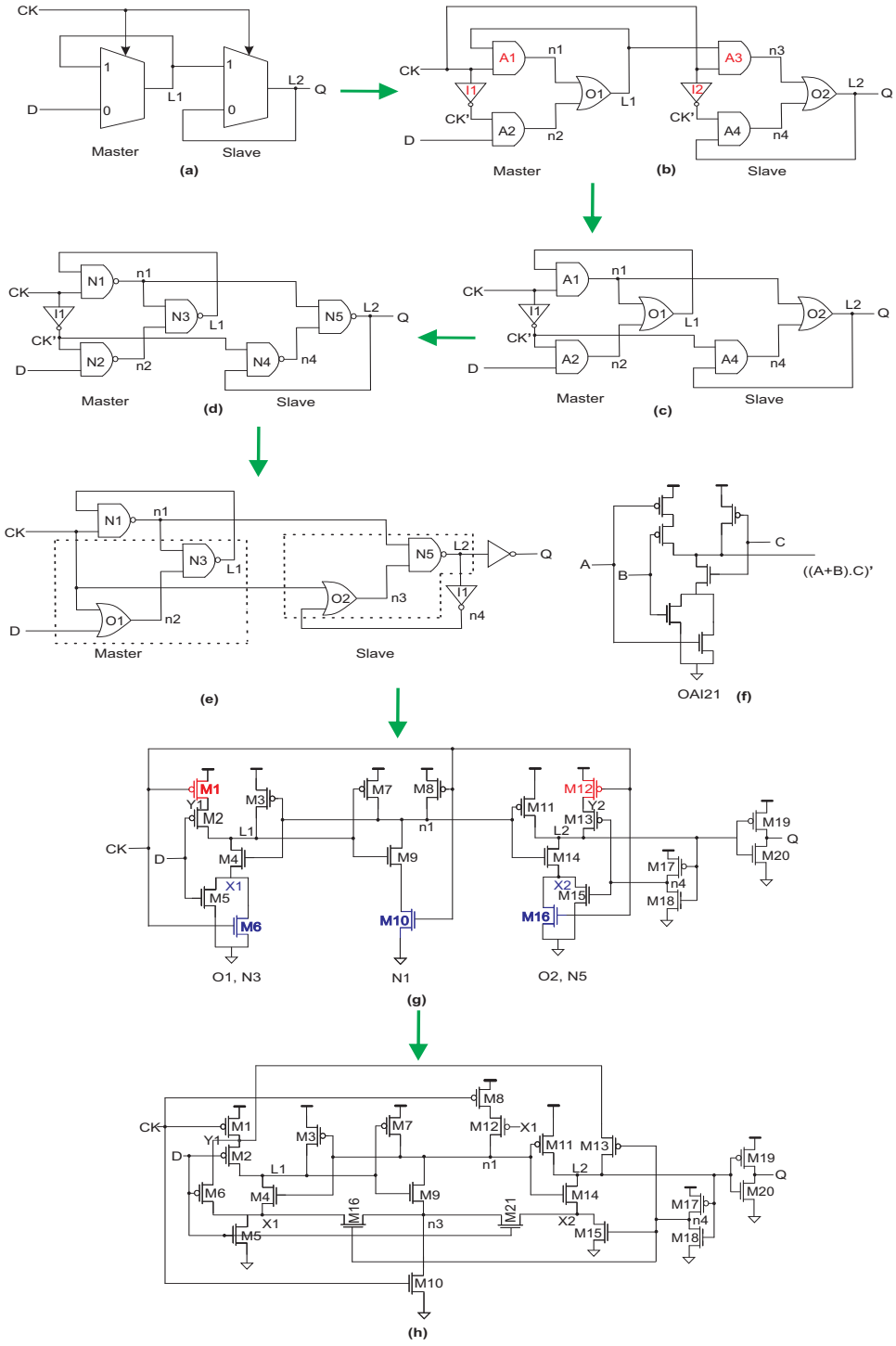


Figure 4.1: Realization of the 21TSPC with Only Three Clock Transistors.

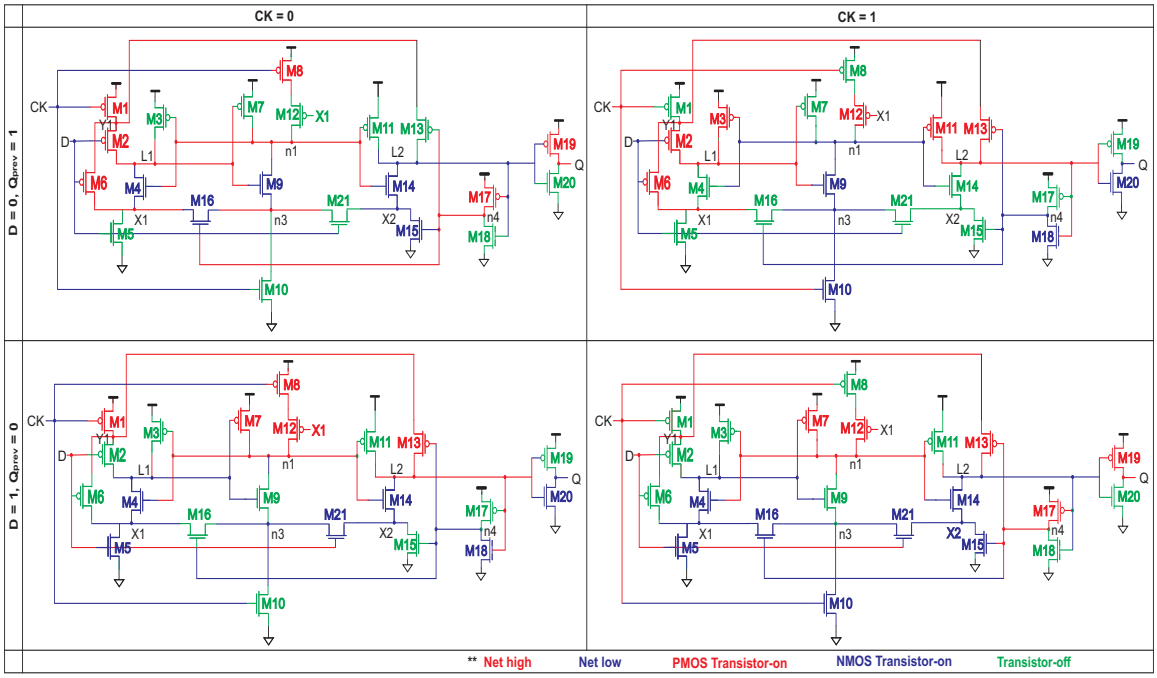


Figure 4.2: Working principle of the 21TSPC for different clock and data states, highlighting on and off transistors, high, and low logic nets.

turns to (V_{DD}-V_{Tn}) through M1, M6, M16, and M9. As a result, node L2 goes to ground through M14 and M15, and Q stays high. Node n1 discharges to ground through M9 and M10 when CK switches from "0" $\rightarrow$ "1", activating M3 driving node L1 high. Following that, L2 rises high, which drives Q low.

On the other hand, when CK = "0", D = "1", and Qprev = "0", node n1 goes high, activating M4, and causing L1 to discharge to ground. Subsequently, M7 turns-on, keeping node n1 connected to VDD. Node L2 stays isolated, though, until CK rises and activates M10. After that, L2 switches from "1" $\rightarrow$ "0" through M14, M21, and M10, therefore, Q switches from "0" $\rightarrow$ "1".

4.1.2 20TSPC Flip-flop with only Three Clock Transistors

The node n1 in Figure 4.1 (g) needs to be pre-charged only when D = "1" and CK = "0". Arguably, M1 and another transistor in series can be used for this purpose. If it is a PMOS transistor, an inverter is needed to complement the data and drive the gate of the

PMOS transistor. On the other hand, an NMOS can also be used for the same, eliminating the inverter. However, the node n1 in this case gets a pre-charge voltage of (V_{DD}-V_{Tn}). The logic behavior of the flip-flop remains unchanged irrespective of whether the NMOS or PMOS transistor is used. The usage of NMOS transistor degrades C-Q delay while conserving its dynamic power consumption. We chose the NMOS transistor to reduce the power consumption in the proposed 20TSPC as shown in Figure 4.3. The n1 node is pulled up to VDD through M7, while node L1 is being pulled down to ground by high input data. This flip-flop is contention-free, and needs only three clock transistors for its clock circuitry with an overall transistor count of 20. It works in master-slave configuration, and has the same working mechanism as 21TSPC.

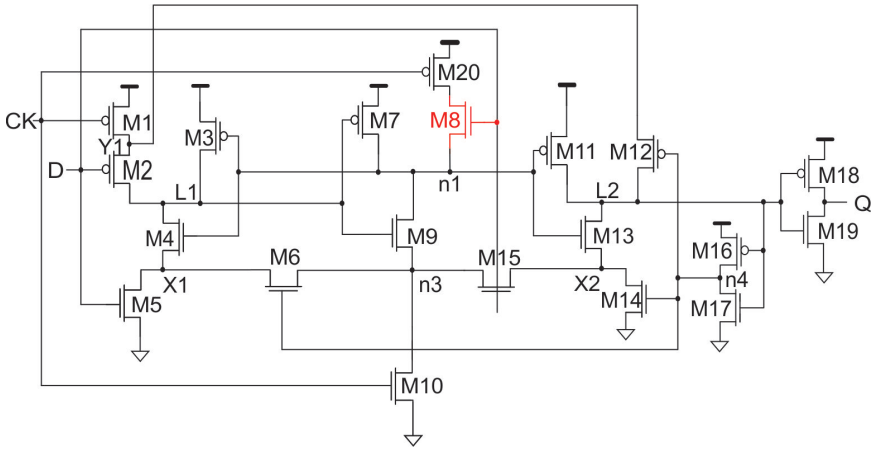


Figure 4.3: Proposed 20TSPC Flip-flop.

4.1.3 19TSPC Flip-flop with only Two Clock Transistors

Similar like 20TSPC, the internal redundant transition at node n1 in this flip-flop is blocked by an NMOS transistor as shown in the Figure 4.4. The main features of this flip-flop is that, it only needs two clock transistors for its clock circuitry with an overall transistor count of 19.

The clock transistor M12 in Figure 4.1 (g) is redundant, as the clock transistor M10 provides the clock boundary of data transfer from the master to the slave. However, the presence of the clock transistor M12 can reduce the delay at the cost of higher clock power consumption and makes the circuit contention-free. We choose to lower the clock load at

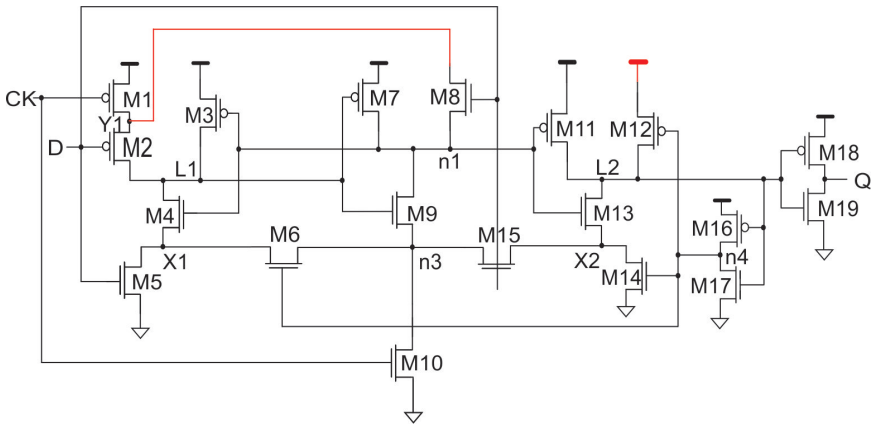


Figure 4.4: Proposed 19TSPC Flip-flop.

the expense of the marginal extra delay for the proposed 19TSPC to make it functional with only two clock transistors.

In Figure 4.4, NMOS data transistor, M8, causes pre-charge voltage of (V_{DD}-V_{Tn}) at node n1 when CK = "0" and D = "1". The n1 node is pulled up to full VDD through M7, while node L1 is being pulled down to ground by high input data. The node X1 should have a path to the ground when the CK = "1" and high data is already latched in the slave, and a combination of M6 and M10 transistors short node X1 to ground under this condition. Similarly, transistors M15 and M10 pull the node X2 to ground when CK = "1" and D = "1". The flip-flop shows transient contention when D = 1, previous D = 0, and CK is making a positive transition. The L2 node is pulled down by the path consists of M13, M15, and M10. The transistor M12 is also on, however, an appropriately sized aforementioned pull-down path and a M12 can resolve it such that node L2 is discharge which results in n4 pulled high and turning off transistor M12.

Figure 4.5 depicts the working principle of the proposed flip-flop for various clocks and data states. Assuming initially, Q = "0". When CK = "0" and D = "0", node L1 goes high, and node n1 is in a high impedance state and holds its previous value. When the CK changes from "0" $\rightarrow$ "1", node n1 is discharged to ground through M9 and M10, which turn on M3, driving node L1 high. Thereafter, L2 goes high, as a result, Q is driven low. In contrast, when CK = "0" and D = "1", node n1 is charged to (V_{DD}-V_{Tn}) which turns on M4, thus, L1 is discharged to the ground. As a result, M7 turns on, which restores node n1 to full VDD. However, node L2 remains isolated till CK goes high and turning on M10. Subsequently, L2 changes from "1" $\rightarrow$ "0" through M13, M15, and M10, which in turn causes Q to change from "0" $\rightarrow$ "1".

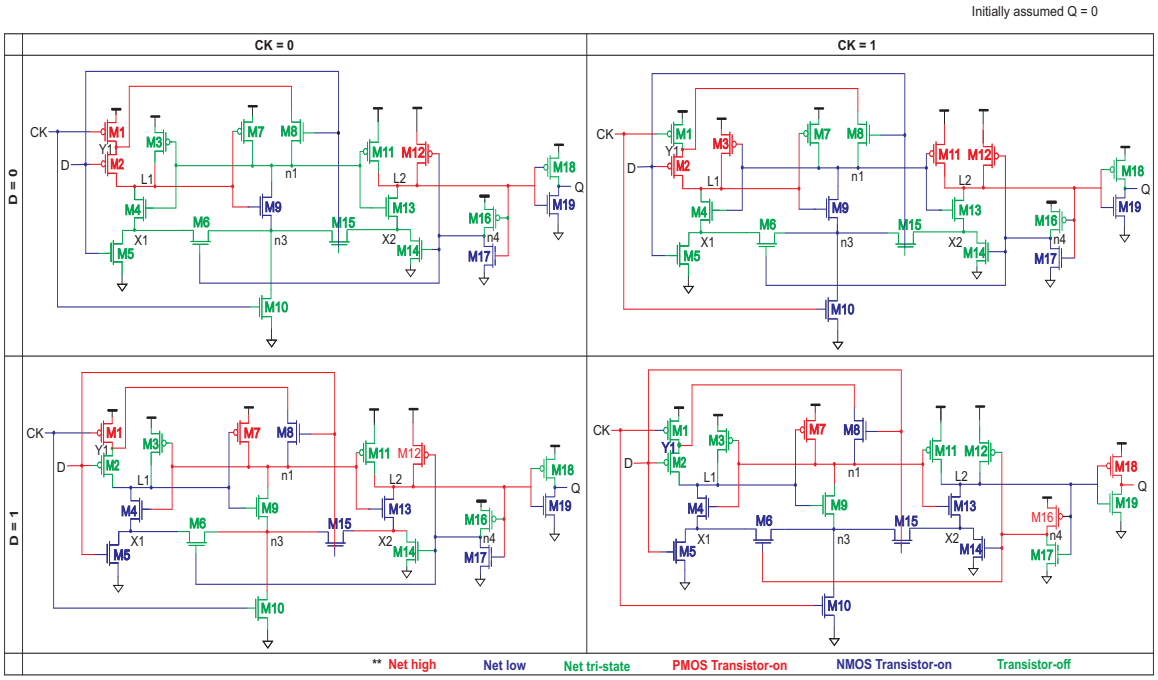


Figure 4.5: Working Principle of the 19TSPC for Different Clock and Data States, Highlighting On and Off Transistors, High, Low, and Tri-state Logic Nets.

4.2 Post-layout Simulation Results

All investigated FFs were laid out in 65 nm CMOS technology, as shown in Fig. 4.6. All FFs were optimized for low-power and low-energy consumption and designed to work over a voltage range of 0.6–1.0 V. Where possible, transistor sizes were kept at minimum channel length, 60 nm, and a width of 200 nm and 400 nm for NMOS and PMOS, respectively. For the 19TSPC to work optimally, M3, M11, M12, and M17 needed to be weaker; thus, they are kept at W = 150 nm. M10, M13, and M15 needed to be stronger; thus, they are kept at W = 400 nm, and M7 is kept at W = 600 nm. All layouts were drawn using the same approach, and only metal layers 1 and 2 were used for the interconnects.

4.2.1 Testbench for Simulation

A testbench was created as shown in Figure 4.7 [78, 80, 85, 86] to measure power, delay and energy of all investigated FFs. The testbench includes clock and data buffers, and



Figure 4.6: The Cell Layout of (a) 18TSPC, (b) 20TSPC, (c) 21TSPC, (d) ACFF, (e) 19TSPC, (f) TCFF, (g) S2CFF, (h) LLFF, (i) TGFF, and (j) REEF in 65 nm CMOS Technology.

the output buffer with a 10 fF load. The input buffers are designed with minimum-size transistors. The output buffer's inverter-1 (white) has NMOS = 300 nm and PMOS = 600 nm widths, while inverter-2 (gray) has NMOS = 450 nm and PMOS = 900 nm widths.

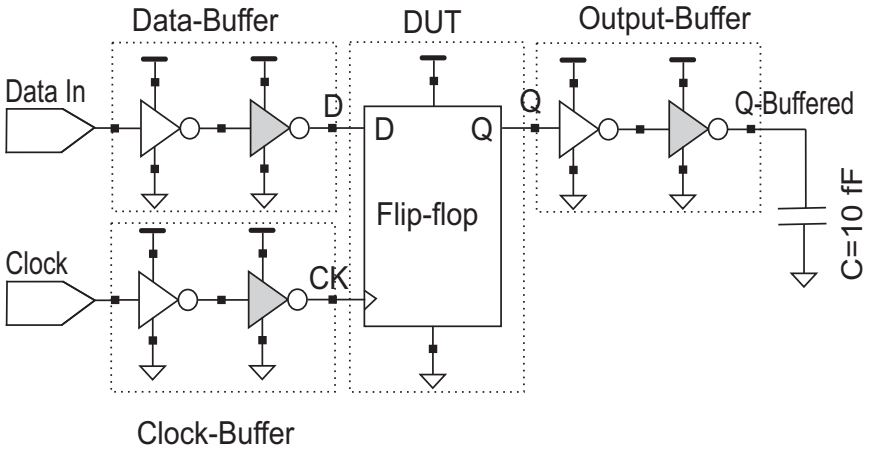


Figure 4.7: Simulation Testbench.

The flip-flop's total power consumption is the addition of 3 separate power components.

- Data power utilization is defined by gray inverter power consumption, as indicated in Data-Buffer region of Figure 4.7.
- Clock power utilization is defined by gray inverter power consumption, as indicated in Clock-Buffer region of Figure 4.7.
- Flip-flop power utilization is defined by Flip-flop power consumption, as indicated in Design Under Test (DUT) region of Figure 4.7. The inherent switching power of flip-flop internal nodes is represented by this power utilization.

Since all considered FFs use the same testbench, power consumption of the output buffer is identical for all FFs for a given DA. The average power is computed on a time frame of 101 clock cycles with the first clock cycle serving as the data reset.

In the same way, D-C and C-Q delays combined make up the D-Q delay.

- D-C delay is the time span between D and CK signals as indicated in the Data and Clock-Buffer regions of Figure 4.7.
- C-Q delay is the time span between CK and Q signals, as illustrated in Clock-Buffer and DUT portions of Figure 4.7.

4.2.2 Single Flip-flop Simulation

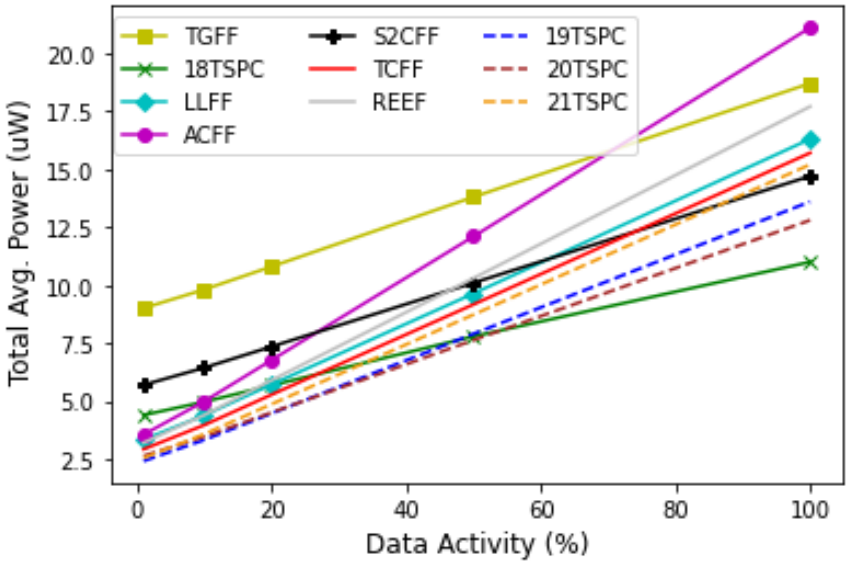


Figure 4.8: Total Average Power Versus DA at VDD = 1 V, CK = 1 GHz.

Different power and timing simulations on extracted layouts were carried out at a nominal voltage of 1 V, a clock of 1 GHz, and at low-voltage of 0.6 V, a clock of 50 MHz. Figure 4.8 and Figure 4.9 depict a comparison of the total average power as a function of DA for all investigated FFs at a voltage of 1 V, a clock of 1 GHz, and a voltage of 0.6 V, a clock of 50 MHz, respectively. Post-layout simulation results show that proposed FFs 19TSPC, 20TSPC, and 21TSPC are most power-efficient for low DAs up to 45%, 50%, and 30%, respectively, whereas 18TSPC is most power-efficient for higher DAs.

Table 4.1 depicts the worst-case timing of all FFs tested at voltages of 1 V and 0.6 V. TGFF has the lowest D-C delay (i.e., setup time) amongst all considered FFs. D-Q delay is the total of setup time and C-Q delay. At nominal conditions, the TGFF has the shortest D-Q delay, followed by 18TSPC, LLFF, REEF, 19TSPC, ACFF, 20TSPC, 21TSPC, TCFF, and S2CFF. At VDD = 0.6 V, 20TSPC and 19TSPC provide the highest D-to-C delay, which in turn increases their D-to-Q delay.

Figure 4.10 and Figure 4.11 compare the PDP of FFs for various DAs at voltages of 1 V and 0.6 V. At VDD = 1 V, LLFF offers the lowest PDP for DA = 1%, and 10%, followed by 18TSPC, 19TSPC, 20TSPC, and 21TSPC. For higher DAs 18TSPC becomes

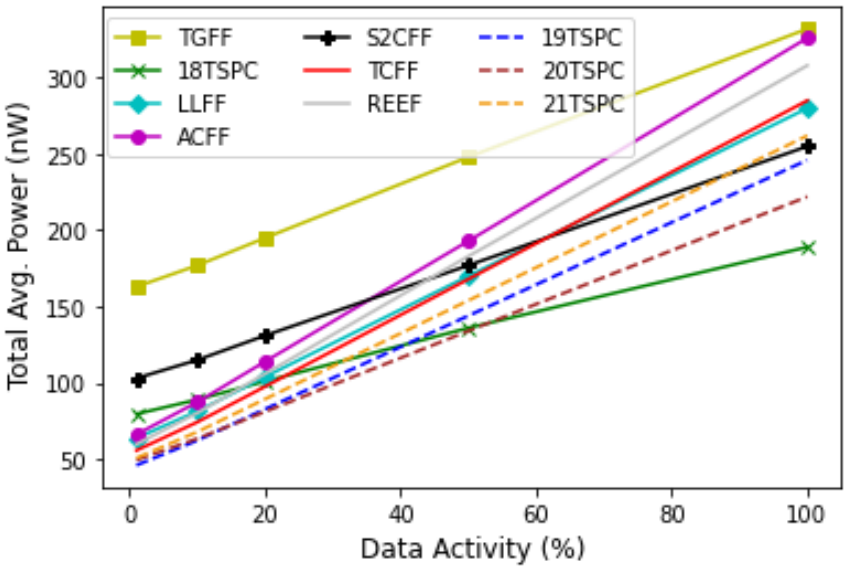


Figure 4.9: Total Average Power Versus DA at VDD = 0.6 V, CK = 50 MHz.

Table 4.1: Post-layout Worst-case Delays For All Analyzed FFs.

Flip-flop	**Delay (ps)**							
	Voltage = 1 V, Clock = 1 GHz				**Voltage = 0.6 V, Clock = 50 MHz**			
	D-C	**C-Q**	**D-Q**	**Hold-time**	**D-C**	**C-Q**	**D-Q**	**Hold-time**
TGFF	22	110	132	-11.70	62	295	357	-52.41
S2CFF	63	198	261	-55.61	131	977	1108	-120.40
ACFF	114	116	230	-60.47	254	152	406	-108.20
TCFF	150	103	253	-39.50	271	358	629	-84.27
18TSPC	44	102	146	37.09	108	227	335	80.86
LLFF	61	86	147	-48.03	123	172	295	-92.58
REEF	82	117	199	-46.40	292	540	832	-92.25
19TSPC	**124**	**104**	**228**	**57**	**757**	**336**	**1093**	**125**
20TSPC	**127**	**111**	**238**	**56**	**881**	**433**	**1314**	**125**
21TSPC	**88**	**156**	**244**	**57**	**192**	**663**	**855**	**126.1**

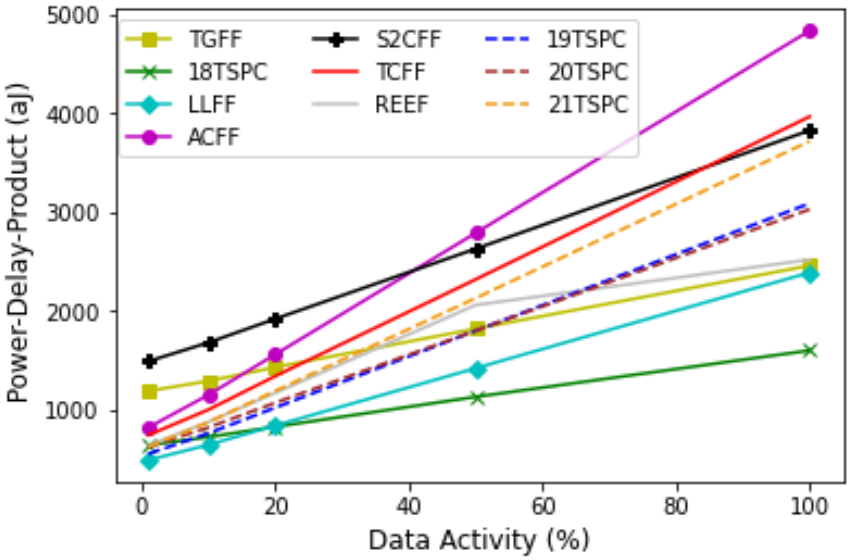


Figure 4.10: PDP Versus DA at VDD = 1 V, CK = 1 GHz.

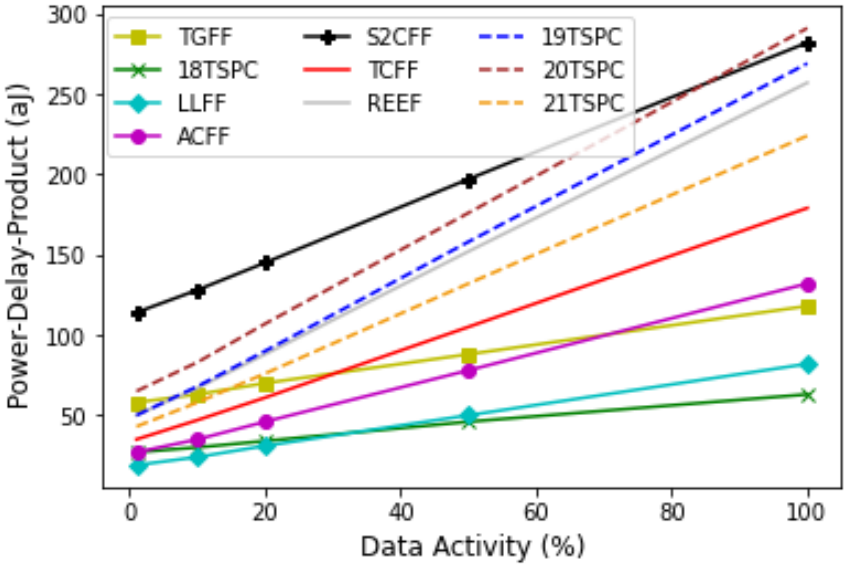


Figure 4.11: PDP Versus DA at VDD = 0.6 V, CK = 50 MHz.

most energy-efficient followed by LLFF, 19TSPC, and 20TSPC. At low-voltage S2CFF has the highest energy consumption at low DAs, and at a higher DAs it follows 20TSPC.

4.3 Proposed Flip-flops Applied in Applications

4.3.1 Scan-chain of 256 Flip-flops

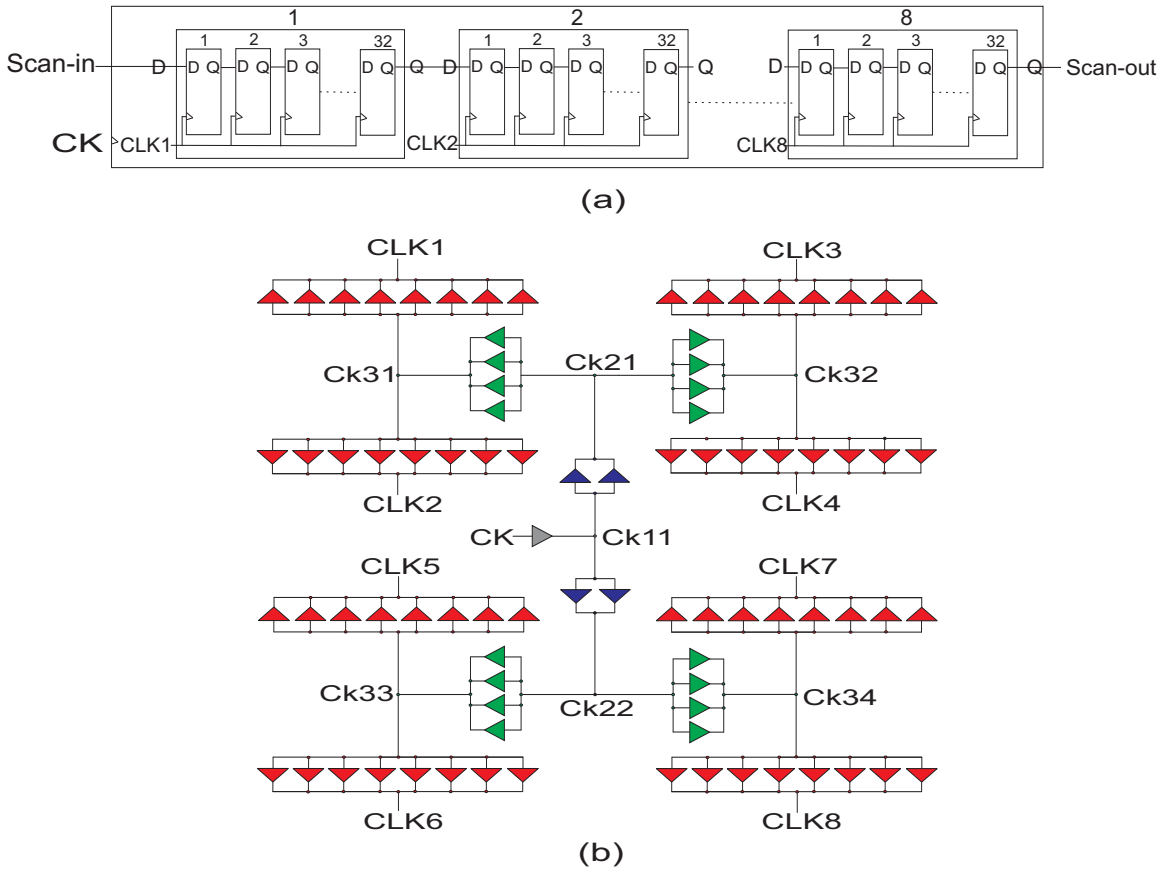


Figure 4.12: Block Diagram for a 256-bit Flip-flop Scan-chain (a), and Clock Distribution Network (b).

In order to further validate the low-power properties of the proposed SET FFs, we implemented 256-bit scan-chains for all investigated FFs (Figure 4.12). A 4-stage clock

H-Tree is designed as shown in Figure 4.12 (b) to provide clock signals to the scan-chain of 256 FFs. Each next stage has twice the number of parallel clock buffers than previous stage to get the higher driver strength. The final stage has 8 parallel buffers, which drive the clock load of 32 FFs.

An extracted layout simulation is run on 256 flip-flop scan-chains for various DAs at voltage of 1 V, clock of 50 MHz, and voltage of 0.6 V, clock of 20 MHz. As 256 clock cycles are required to fill the scan-chain with the proper DA sequence, a total of 356 clock cycles are used for the power simulation. Total average power is estimated using a 257 to 356 clock-cycles timing window and includes the power utilization of clock buffers, data buffers, and the 256 flip-flop scan-chain. To ensure consistent filling of the data pipeline, all data sequences given to the scan-chain are periodic [85, 10]. Each flip-flop input receives a new data on every clock cycle with 100% DA. Each flip-flop input gets a new data on every two clock cycles with 50% DA, and so on.

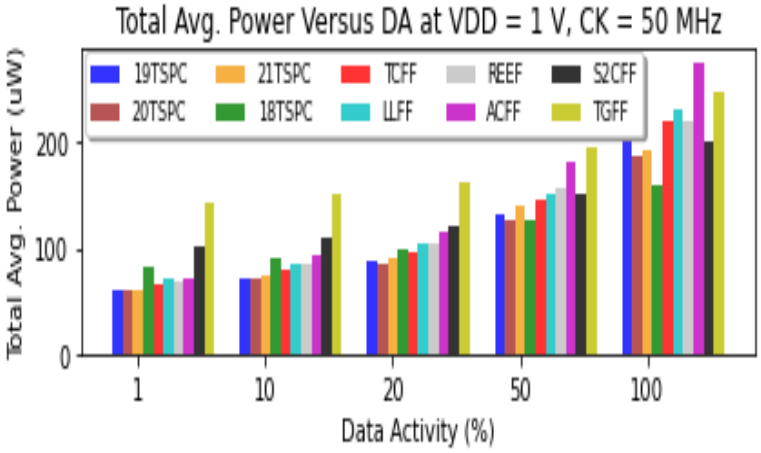


Figure 4.13: Total Average Power Versus DA for Scan-chain of 256 FFs at VDD = 1 V and CK = 50 MHz.

Figure 4.13 and Figure 4.14 illustrate total average power against DA for the 256 flip-flop scan-chain at VDD = 1 V and 0.6 V, respectively. These results show a pattern similar to the single flip-flop simulations. Scan-chains consist of proposed FFs, and 18TSPC are power-efficient at low DA and high DA, respectively. For example, at a nominal voltage of 1.0 V and 10% DA, the 19TSPC based scan-chain consumes 23% less power, and the 21TSPC based scan-chain consumes 19% less power compared to the 18TSPC based scan-chain.

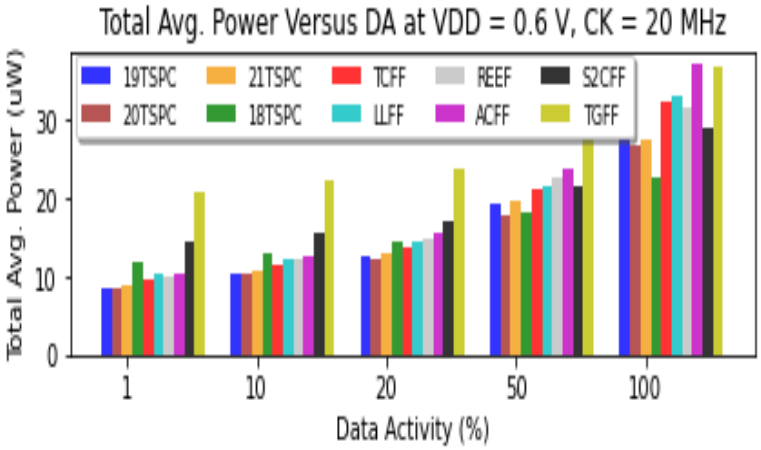


Figure 4.14: Total Average Power Versus DA for Scan-chain of 256 Flip-flops at VDD = 0.6 V and CK = 20 MHz.

4.3.2 Advanced Encryption Standard (AES)

In modern communication systems, cryptographic algorithms have been deployed to encrypt and decrypt data for secure transmission. The Advanced Encryption Standard (AES) algorithm has become the default choice for various security services in numerous applications. AES is basically a symmetric block cipher that processes data in 128-bit blocks [87]. It supports key sizes of 128, 192, and 256 bits and consists of 10, 12, and 14 iteration rounds, respectively [88]. Each round mixes the data with a round key, which is generated from the encryption key. Decryption inverts the iterations, resulting in partially different data paths. The block diagram of the AES-128 encryption engine is shown in Figure 4.15.

To further validate the power savings of the proposed low-power SET FFs and their compatibility with the Cadence industry standard Application Specific Integrated Circuits (ASICs) tools, we have designed the AES-128 encryption engine using all the considered FFs. To reduce the number of input and output pins, we have used two 8-bit serial-in-parallel-out shift-registers to capture the plain text and encryption key from the input side, and one 8-bit parallel-in-serial-out shift-register at the output side to generate the encrypted data out serially. A fixed floorplan area of 120 um * 80 um is used for each AES-128 design. TCFF failed to work in the flow.

Table 4.2 compares the synthesis-level simulation results. Each AES-128 requires 376 corresponding FFs. Three different power simulations were carried out at VDD = 1 V, corner = TT, VDD = 0.9 V, corner = SS, and VDD = 1.1 V, corner = FF. A 50 MHz

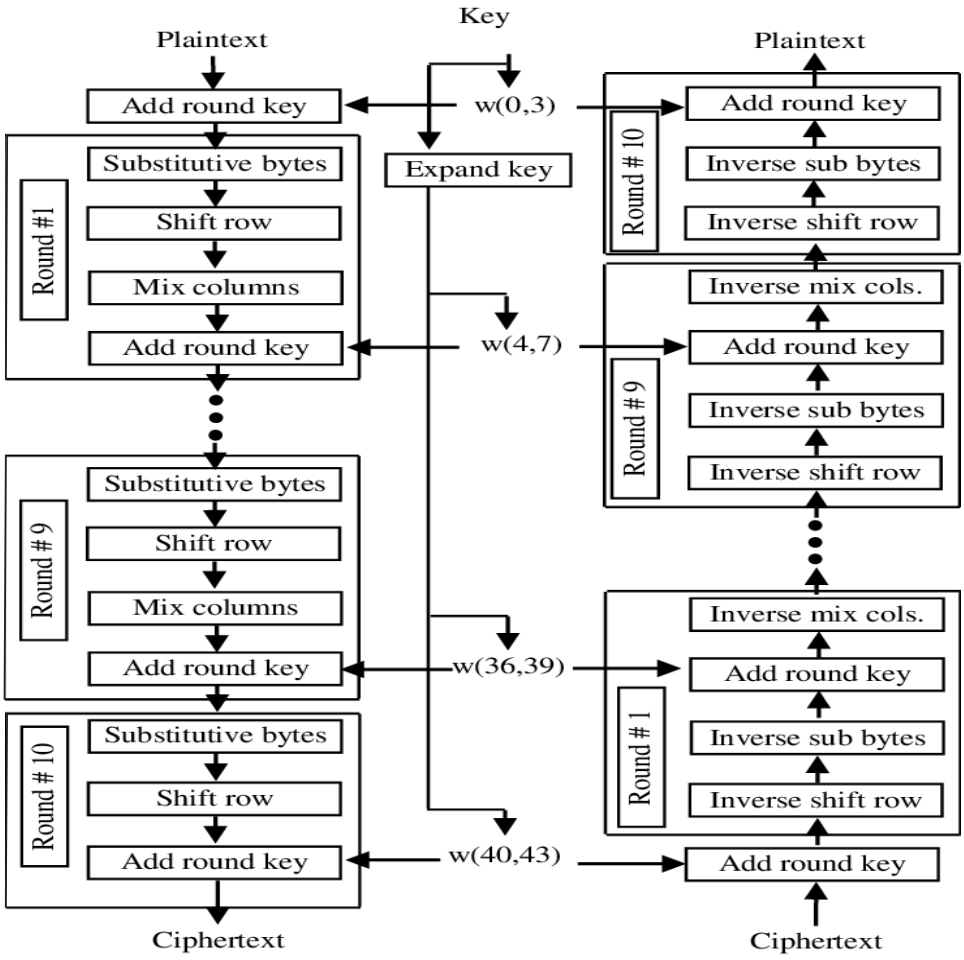


Figure 4.15: Block Diagram of AES-128.

Table 4.2: AES-128 Netlist Power Consumption.

Flip-flop	Total Power (uW) Consumption			Number of FFs Used
	VDD = 0.9 V, Corner = SS	VDD = 1 V, Corner = TT	VDD = 1.1 V, Corner = FF	
TGFF	117	158	338	376
S2CFF	108	142	302	376
ACFF	115	179	488	376
18TSPC	87	113	248	376
LLFF	104	139	303	376
REEF	118	157	323	376
19TSPC	76	82	206	376
20TSPC	81	99	245	376
21TSPC	77	83	207	376

Table 4.3: AES-128 Post-layout Power Simulation at VDD = 0.9 V, Corner = SS.

Flip-flop	TGFF	S2CFF	ACFF	18TSPC	LLFF	REEF	19TSPC	20TSPC	21TSPC
Short Circuit Power (uW)	345.63	328.4	335	302.45	290.9	322.9	273	280	277.38
Dynamic Power (uW)	80.76	120	131	126.13	133	138	132	139	136.33
Leakage Power (uW)	29.38	30.6	32	31.42	29.1	30.1	30.58	30.1	30.95
Total Power (uW)	455.77	479	498	460	453	491	435.58	449.1	444.66

clock frequency is used for the shift registers, and 6.25 MHz clock frequency is used for the internal AES-128 operation. The power consumption of the proposed SET FFs is lower than the referenced FFs, as can be seen in Table 4.2.

Table 4.3 shows the worst-case post-layout power simulation results at VDD = 0.9 V for the SS corner, using 50 MHz clock frequency for the shift-registers and 6.25 MHz for AES-128 circuitry. As can be seen, the proposed SET FFs consume lesser power than the referenced FFs for the following given input signals:

key-in = 128'h2b7e151628aed2a6abf7158809cf4f3c
data-in = 128'h3243f6a8885a308d313198a2e0370734
Ciphered-out = 0x3925841d02dc09fbdc118597196a0b32

4.4 Test-chip Measurement Results

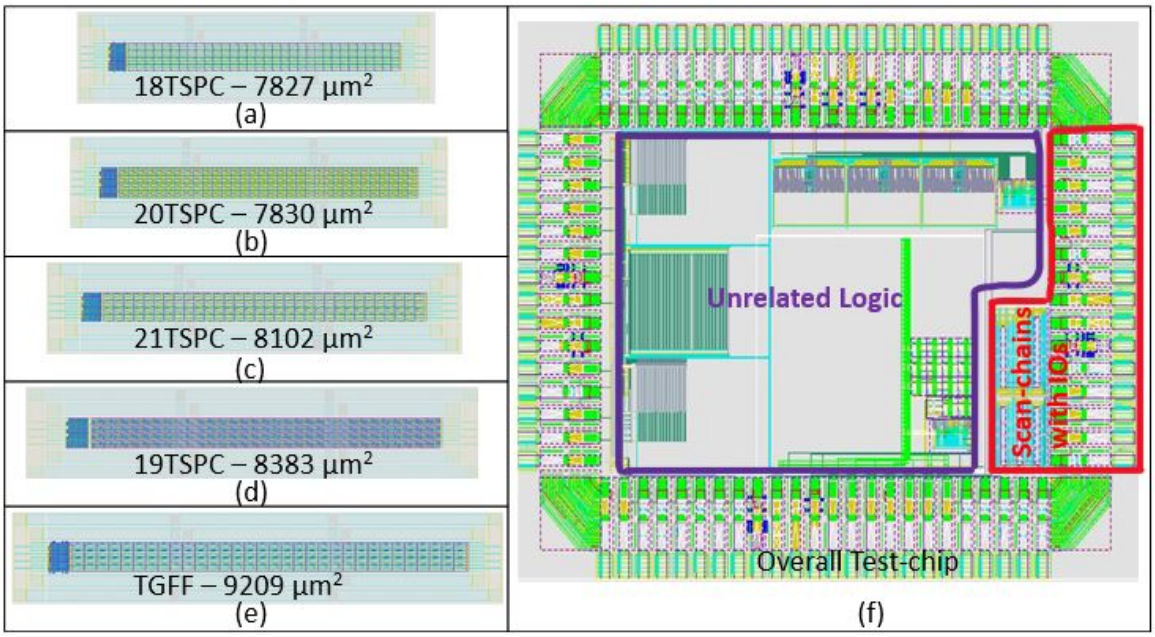


Figure 4.16: Implementation of 256-flip-flop Scan-chains: (a) 18TSPC, (b) 20TSPC (c) 21TSPC, (d) 19TSPC, (e) TGFF, and (d) Overall Test-chip.

To experimentally validate the power-efficiency of the proposed SET FFs, five 256-flip-flop scan-chains (19TSPC, 20TSPC, 21TSPC, 18TSPC, and TGFF) without hold buffers in between flip-flop stages and with synthesized clock trees were implemented as shown in Figure 4.16.

The test-chip measurement setup is shown in Figure 4.17. A Nexys A7 FPGA board is used to generate the clock and corresponding DA input signals. A 4-channel oscilloscope is used to verify the corresponding waveform patterns, and average current consumption is measured on DC power-supply screen.

Figure 4.18 and Figure 4.19 illustrate total power consumption against DA for the 256-flip-flop scan-chains at VDD = 1 V, and CK = 10 MHz and 25 MHz, respectively. For 10 MHz clock frequency, the proposed SET FFs scan-chains show power-efficiency for low DAs, and then these follow an 18TSPC-based scan-chain as can be seen in Figure 4.18. As frequency increases, power-efficiency of the proposed FFs scan-chain as compared to the other considered flip-flop scan-chains improves further because of the lower number of

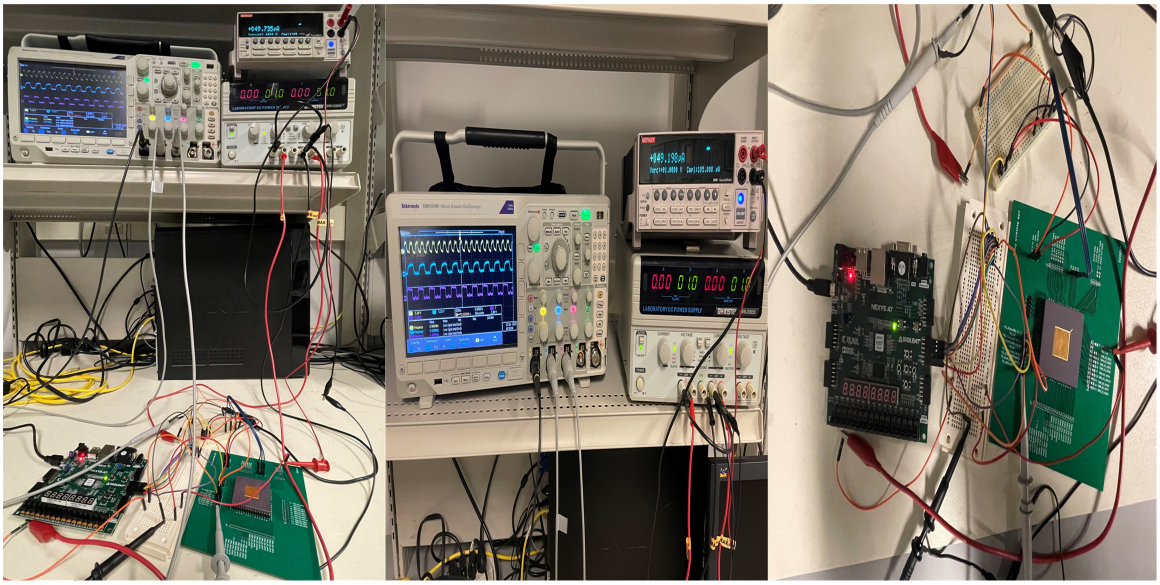


Figure 4.17: Test-chip Measurement Setup.

clock transistors and the removal of unnecessary internal node transitions in the proposed FFs. Consequently, these become most power-efficient for all DAs, as illustrated in Figure 4.19.

Figure 4.20 depicts 256-flip-flop scan-chains total power consumption versus VDD at CK = 25 MHz and DA = 12.5%. The proposed FFs scan-chains show low-power consumption as compared to 18TSPC and TGFF based scan-chains for the voltage range from 0.9 V to 1.2 V. Implemented scan-chains were also measured under different temperatures. For these measurements, the test-chip was put in the SH-241 temperature chamber, and measurements were carried out at VDD = 1 V, CK = 25 MHz, and DA = 12.5%. As can be seen from Figure 4.21, proposed flip-flop scan-chains show the power savings with respect to that of 18TSPC and TGFF scan-chains over the temperature range of 0 to 80 ^{0}C.

Table 4.4 makes an overall comparison of all analyzed FFs. The proposed FFs (19TSPC, 20TSPC, and 21TSPC) have only two and three clock transistors. They are most power-efficient for low DAs at low and high votlage. This comparison illustrates that the proposed FFs are attractive for low-power applications with low-to-moderate DA. Test-chip measurement result verifies that the proposed 19TSPC, 20TSPC, and 21TSPC FFs are the most-power efficient for low DAs.

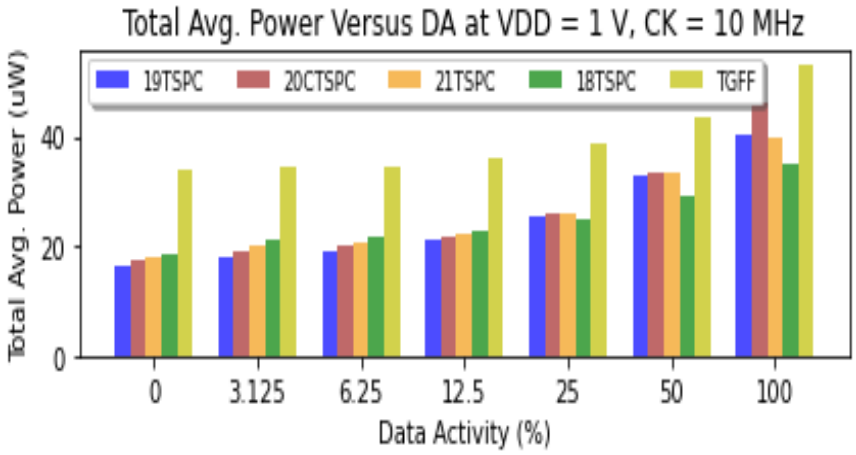


Figure 4.18: Total Power Consumption of 256-flip-flop Scan-chains as a Function of DA at VDD = 1 V and CK = 10 MHz.

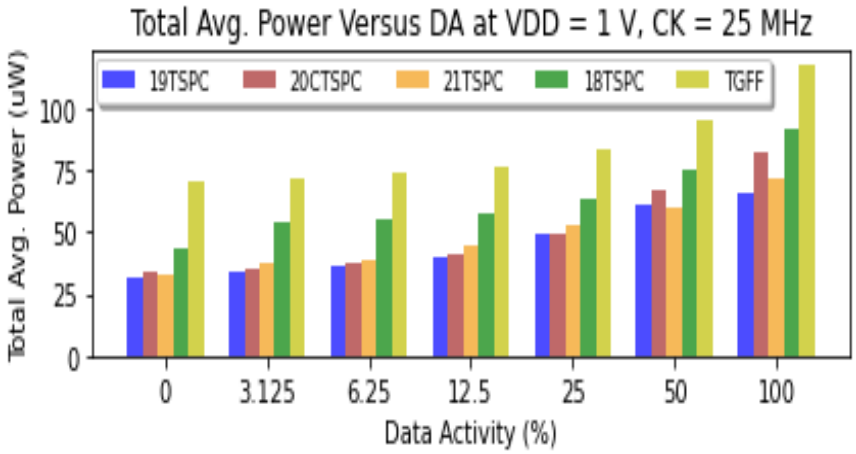


Figure 4.19: Total Power Consumption of 256-flip-flop Scan-chains as a Function of DA at VDD = 1 V and CK = 25 MHz.

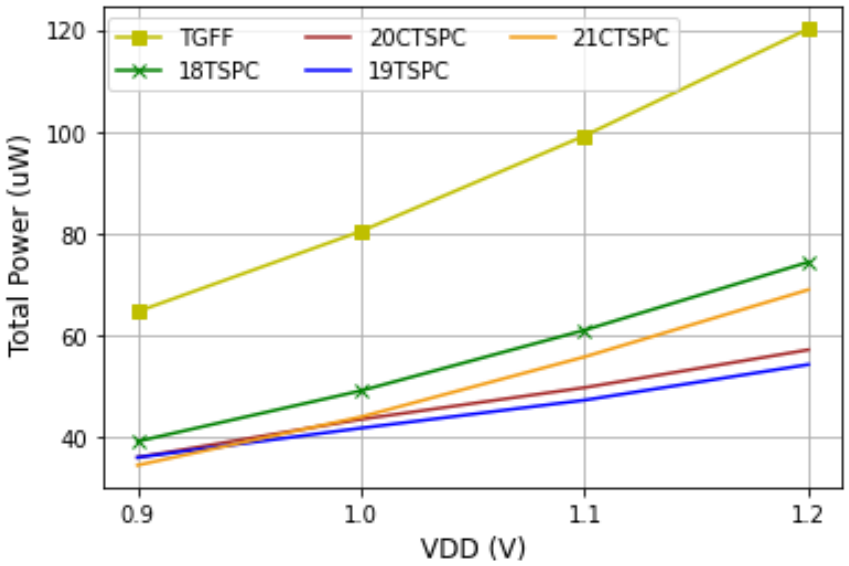


Figure 4.20: Total Power Consumption of 256-flip-flop Scan-chains as a Function of Voltage at DA = 12.5% and CK = 25 MHz.

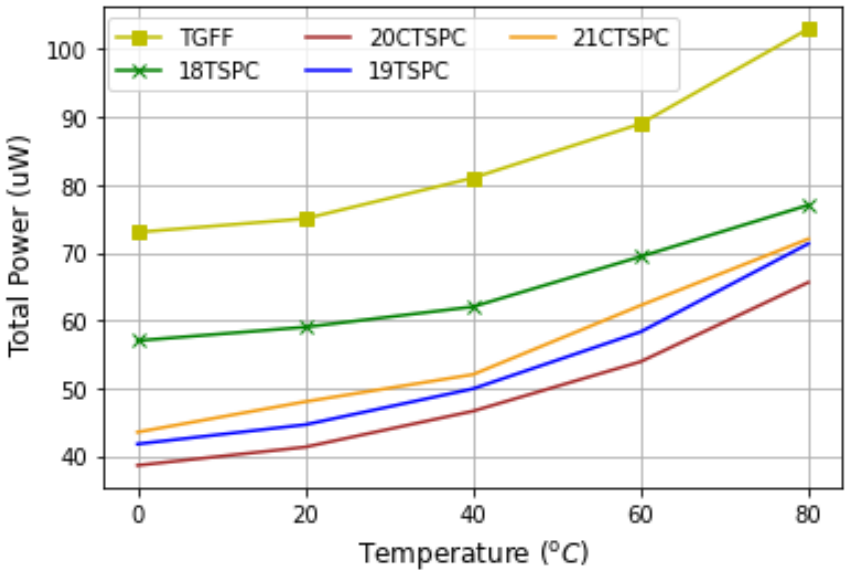


Figure 4.21: Total Power Consumption of 256-flip-flop Scan-chains as a Function of Temperature at DA = 12.5%, VDD = 1 V, and CK = 25 MHz.

Table 4.4: Overall Comparison Of All Considered Single-edge Triggered Flip-flops.

Characteristic	Flip-flop									
	TGFF	S2CFF	ACFF	TCFF	18TSPC	LLFF	REEF	19TSPC	20TSPC	21TSPC
Presented Year	Std-Cell	ISSC'14 [13]	ISSC'11 [12]	JSSC'14 [14]	JSSC'19 [16]	SOCC'19 [17]	JSSC'21 [18]	This work	This work	This work
Single-phase	X	✓	✓	✓	✓	✓	✓	✓	✓	✓
CK Transistors	12	5	4	3	4	4	4	**2**	**3**	**3**
Tot. Transistors	24	24	22	21	18	24	25	**19**	**20**	**21**
Area (um^2)	9.72	8.64	8.28	8.64	7.92	9	10.44	**8.64**	**7.92**	**8.28**
Voltage = 1 V, Clock = 1 GHz (TT/25°C)										
Leakage (nW)	61.10	77.80	76.20	39.90	46.90	59.10	96.80	**53.80**	**56.75**	**61.74**
Tot. Power (uW) DA = 10%, 20%	9.81, 10.80	6.44, 7.35	4.99, 6.77	3.97, 5.28	4.97, 5.68	4.39, 5.72	4.40, 5.90	**3.33, 4.47**	**3.47, 4.51**	**3.58, 4.87**
D-Q Delay (ps)	132	261	230	253	146	147	199	**228**	**238**	**244**
PDP (aJ) DA = 10%, 20%	1290, 1430	1680, 1920	1150, 1560	1000, 1340	723, 827	644, 839	876, 1170	**761, 1020**	**820, 1070**	**874, 1190**
Voltage = 0.6 V, Clock = 50 MHz (TT/25°C)										
Leakage (nW)	12.90	17.10	17.40	11.60	14.70	18.70	8.76	**14.90**	**6.20**	**15.75**
Tot. Power (nW) DA = 10%, 20%	177, 195	115, 131	87.4, 114	74.3, 97.6	89, 101	81.4, 104	80.3, 106	**62.3, 82.8**	**63.5, 81.1**	**67.9, 89.4**
D-Q Delay (ps)	357	1108	406	629	335	295	832	**1093**	**1314**	**855**
PDP (aJ) DA = 10%, 20%	63, 70	128, 145	35, 46	47, 61	30, 34	24, 31	67, 88	**68, 90**	**83, 107**	**58, 76**
Post-layout Simulation: 256-flip-flop Scan-chains at VDD = 1 V and CK = 25 MHz (TT/25°C)										
Tot. Power (uW) DA (%) = 12.5, 25	82.3, 89.2	60.9, 67.4	54.6, 69.3	46.2, 56.8	50.2, 55.9	50.3, 60.8	50.0, 61.5	**44.1, 53.7**	**43.7, 53.1**	**44.1, 54.1**
Measurement: 256-flip-flop Scan-chains at VDD = 1 V and CK = 25 MHz										
Tot. Power (uW) DA (%) = 12.5, 25	80.35, 87.9	-	-	-	49.1, 54.71	-	-	**42.03, 51.46**	**42.5, 52.5**	**43.96, 53.3**

4.5 Summary

In this chapter, we propose three very low-power SET TSPC FFs with only two and three clock transistors. Post-layout simulation results in TSMC 65 nm technology point out that the proposed 19TSPC, 20TSPC, and 21TSPC SET FFs are the most power-efficient for low DAs compared to other state-of-the-art SET TSPC FFs. The test-chip measurement result has validated the power-savings of the proposed FFs.

Chapter 5

Low-power Radiation Hardened By Design Flip-flops

Nanoscale ICs are highly vulnerable to particle-induced SETs because of low signal charge and lower noise margin. Alpha particles and cosmic neutrons, which come from packaging and intergalactic rays, respectively, are the main contributors of SETs [89]. These particles, when strike an IC, produce excess charge in silicon by direct or indirect ionization, which is collected by sensitive nodes and results in voltage transients at those nodes [90]. If a sensitive node is part of a latch and the voltage transient is large enough, it may cause data upset, often known as SEU. As it does not result in long-term device damage, an SEU is sometimes known as a "soft error" [91, 92]. Modern microprocessors and other digital circuits need to be protected from soft errors since they might cause system failures [72, 93]. Memory is more prone to soft errors than logic circuits because of its higher packing density and lack of error-masking measures [94]. With scaling of technology, soft error, particularly in memories, have become a challenge. ECCs and memories with soft error hardened cells have been proposed to mitigate against soft errors [95, 96]. ECC is generally preferred for memories for a variety of reasons: lower implementation cost, ability to mitigate against weak cells, etc. However, ECC is not a viable option for FFs which are typically scattered over the chip. Many soft error tolerant cells have previously been proposed. In this chapter, two RHBD cells, DICE [29], and Quatro [31] will be explored to design proposed RHBD FFs.

5.1 Proposed Radiation-Hardened-By-Design (RHBD) TSPC Flip-flops

For a typical FFs, its power and energy consumption depend on its DA as well as on the number of clock transistors in the flip-flop. The DA varies significantly for a flip-flop to flip-flop in a given chip, and for an average flip-flop DA considered to be in the range of 5 to 15% [12, 14]. At the higher range of DA, flip-flop's power and energy consumption is dominated by the data, while at the lower end of the DA, it is dominated by the clock-related power and energy consumption. All investigated RHBD FFs in Chapter 3 have at least ten clock transistors, which substantially contribute to their power and energy consumption [97, 93]. Therefore, our objective is to design low-power and low-energy radiation hardened FFs with fewer clock transistors.

5.1.1 TSPC-Quatro Flip-flop With only Five Clock Transistors

Fig. 5.1 shows the proposed RHBD TSPC-Quatro flip-flop, which is static, contention-free, true single-phase clocked, and needs a total of 35 transistors, out of which 5 are used for its clock circuitry. TSPC-Quatro uses Quatro cell in master and slave latches to enhance its radiation immunity.

In TSPC-Quatro master and slave latches are complement to each other in terms of data sampling with respect to the clock. When CK = "0" and D = "0", M1, M2, and M14 are turned-on in the master latch which cause nodes X1 and Xn to go high, while X2 and X to low through M9 and M14. In the same way, when CK = "0" and D = "1", nodes X1 and Xn to go low through M7 and M12, and X2 and X to high. Thus, new data and its complement is sampled at node X1 and X2, respectively. During this time, slave latch holds its previous value. When the clock signal goes low-to-high, M1 and M16 are turned off, while M13, M30 and M31 are turned on. Thus, master latch stops to sample new data, while nodes X1 and Xn, and X2 and X4 holds its current values. On the other hand, slave latch samples the master data at nodes Y and Y2, and its complement at Y1 and Yn nodes. Therefore, new output is available at Q on the rising edge of the clock signal.

A negative edge-triggered TSPC-Quatro can also be made by swapping the master and slave latches. The channel length of all transistors is kept at the minimum, while the width of PMOS is kept at 2 times the NMOS width. In terms of SEU immunity, nodes X1 and X2 are vulnerable in master latch; thus, their immunity is improved by enlarging transistor

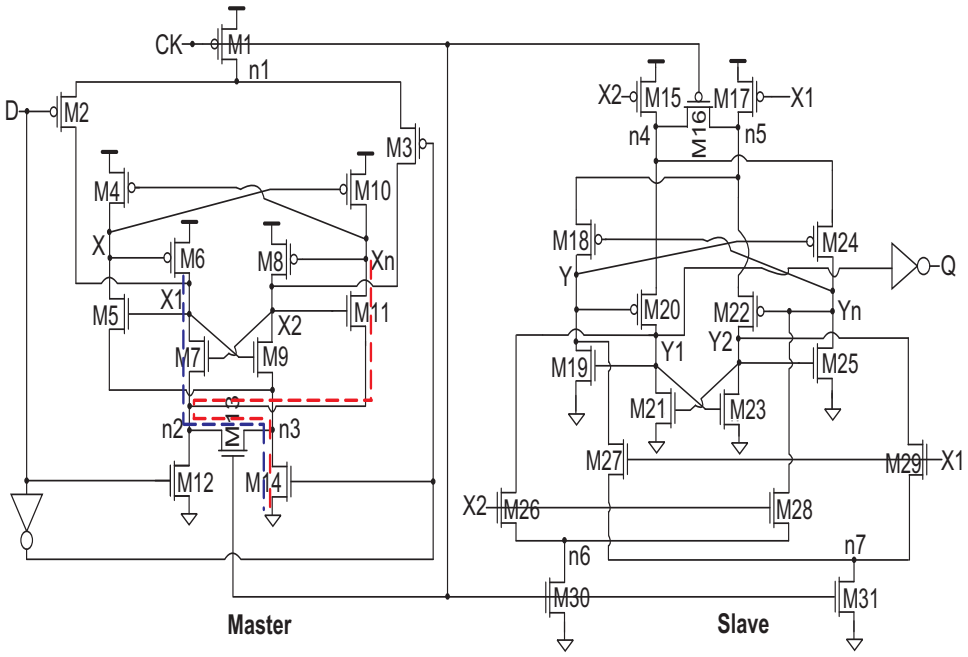


Figure 5.1: A Static Contention-free Single-phase Clocked Radiation Hardened Flip-flop using Quatro Cell (TSPC-Quatro).

sizes (width is kept twice the minimum size) for M7 and M9. Similarly, Y and Yn are vulnerable in slave latch, and PMOS transistors M15-M18 and M24 are kept at twice the width. As a result, critical charge increases at these nodes, and a larger current is required to flip the logic at these nodes.

In Quatro cell, every node has the ability to recover from a $1 \rightarrow 0$ SETs. Conversely, nodes X and Xn can recover from a $0 \rightarrow 1$ SETs, while if a large enough $0 \rightarrow 1$ SETs occurs at node X1 or X2, the data in the cell can be flipped [31]. However, in an RHBD FFs we must also consider the state of the clock and data while considering its radiation hardness besides the innate capability of the hardened cell. For example, consider the case of TSPC-Quatro (Fig. 5.1), and assume CK = "0", D = "0", and for master latch nodes states are {X, X1, X2, Xn} = {0, 1, 0, 1}. When a SETs hits any of these nodes, then affected node recovers after the SETs event owing to the data buffer. During this time, slave latch is isolated from master; as a result, cell's logic and flip-flop's output does not flip. When CK = "1", there is always a ground path available for nodes X1 and X2, regardless of the data value. when a large $0 \rightarrow 1$ SETs hits node X2, then M7 and M11 are turned on and connect the nodes X1 and Xn, respectively, to the ground through M13

and M14 (as shown in blue and red dotted paths in Fig. 5.1). As a result, the cell logic's value flips, which in turn causes Q to flip.

Similarly, for slave latch, consider CK = "1", {X1, X2} = {1, 0}, and {Y, Y1, Y2, Yn} = {0, 1, 0, 1}. When a SETs hits any of the nodes in the slave latch, then affected node recovers and gets its value back once SETs is gone; as a result, the cell's logic and the flip-flop's output remain the same. When CK = "0", and a large 0 → 1 SETs occurs at node Y2, then it causes M21 and M25 to be turned on, which connect nodes Y1 and Yn to ground, respectively. Consequently, M19 turned off, and M18 and M22 turned on, making node Y and Y2 to logic high. Thus, cell's logic flips, and therefore, it causes the flip-flop's output to flip. Upsizing the NMOS transistors M7 and M9 in master latch for nodes X1, and X2, respectively, and PMOS transistors M18 and M24 in slave latch for nodes Y and Yn, respectively, improves the critical charge of the critical nodes, and hence, that of the flip-flop.

5.1.2 TSPC-DICE Flip-flop With only Four Clock Transistors

Fig. 5.2 shows the proposed RHBD TSPC-DICE flip-flop, which is static, contention-free, true single-phase clocked, and needs a total of 36 transistors, out of which 4 are used for its clock circuitry. TSPC-DICE uses DICE cell in master and slave latches to enhance its radiation immunity.

In TSPC-DICE, master and slave latches are also complement in terms of data sampling with respect to clock. Assuming initially Q = "0". When CK = "0" and D = "0", nodes X1 and Xn go high, and X2 and X go low. And when D changes 0 to 1, nodes X1 and Xn go low, and X2 and X go high. Thus, the master latch samples the data and its complement, while the slave latch holds its previous value. When the clock rises, M1 and M19 are turned off while M14 and M32 are turned on. As a result, master latch stops to sample the new data and holds its previous value, while slave latch samples the output of master latch at nodes Y and Y2, and its complement at Y1 and Yn. Thus, nodes Y1 and Yn go low, and nodes Y and Y2 go high. An inverted is used as an output buffer connected to node Y1, which makes the output switch from low to high. Therefore, new data is available at the output node in the next clock cycle.

In DICE cell, if a charge particle hits any of the single node, then unaffected nodes help in the recovery of the affected node in order to prevent it from SEU [89]. For example, consider the case of TSPC-DICE (Fig. 5.2), and assume CK = "0", D = "1", {X, X1, X2, Xn} = {1, 0, 1, 0} in the master latch. When a 1 → 0 SETs hits node X, its logic state changes; as a result, it causes on-transistor M13 to turn off and off-transistor M8 to

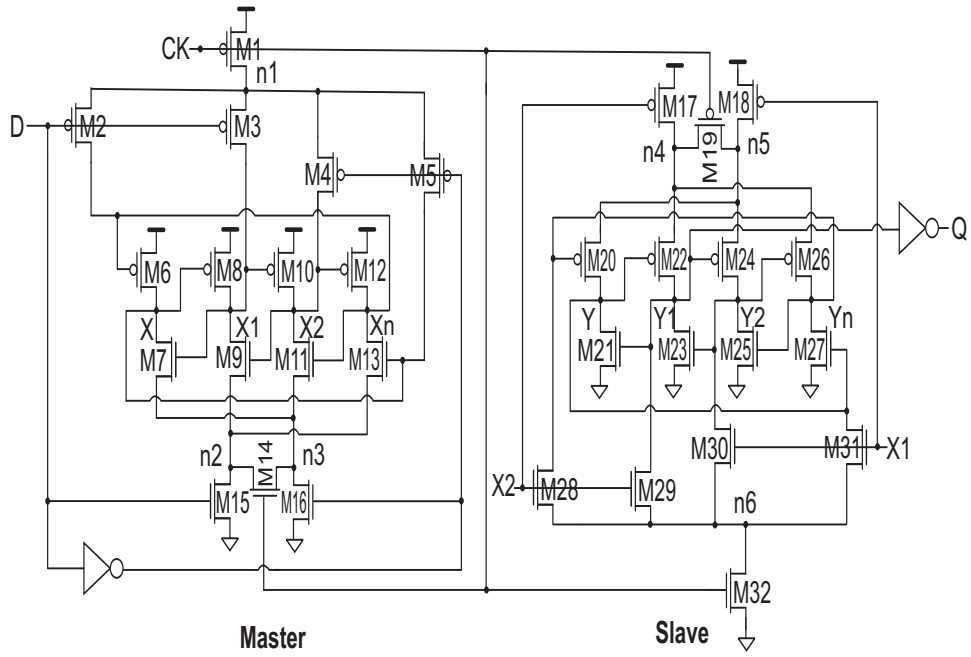


Figure 5.2: A Static Contention-free Single-phase Clocked Radiation Hardened Flip-flop using DICE Cell (TSPC-DICE).

turn on. Thus, node Xn stays floating with logic level low, and it doesn't disturb node X2. Node X1 goes low since NMOS is stronger than PMOS. Therefore, node X doesn't disturb any other unaffected node and gets its original state back once particle charge is gone. During this time, the master is isolated from the slave. When CK = "1", node n2 and n3 are shorted to ground, but again there is no change to unaffected nodes as M13 is turned off.

Similarly, consider CK = "1", {X1, X2} = {0, 1}, and {Y, Y1, Y2, Yn} = {1, 0, 1, 0} for slave latch. When a 1 → 0 SETs hits node Y, it causes M27 to turn off and M22 to turn on. Thus, node Yn stays floating with logic level low, and it doesn't disturb node Y2. Node Y1 goes to logic low since NMOS is stronger than PMOS. Therefore, node Y doesn't disturb any other unaffected node and gets its original value back once SETs is gone. When CK = "0", nodes n4 and n5 are shorted with logic high, but it does not bring any change in the unaffected nodes, as node Yn is a floating node with logic level low. But in this case, if several nodes are affected simultaneously by a SETs hit, then the DICE cell's logic flips, and consequently, the flip-flop's output flips. Therefore, all the critical nodes X, X1, X2, and Xn in master latch and Y, Y1, Y2, and Yn in slave latch of the

proposed TSPC-DICE are separated by a minimum space of 0.71 um in order to overcome the charge-sharing issue.

5.2 Simulation Results

In order to ensure a fair comparison on critical charge, power, energy, and performance, layouts of all the considered FFs were designed in a consistent manner in CMOS 65 nm technology with minimum size transistor lengths of 60 nm and widths for NMOS = 200 nm and PMOS = 400 nm. Only metal layers 1 and 2 were used for the interconnect. An output buffer is placed at the output of MS-DFF, MS-DICE, MS-Quatro, and C^{2}MOS-Quatro FFs. The transistors in the transfer gates of these FFs were kept twice in width, while in soft error tolerant storage cells and cross-coupled inverters these are kept at minimum size. The minimum space of 0.71 um is maintained between critical nodes of all considered RHBD FFs to avoid charge-sharing issues. To evaluate the performance metrics of all the FFs under investigation, the same test bench of Figure 4.7 was used to measure the power, delay and energy of the proposed RHBD FFs.

5.2.1 Critical Charge Simulation

A double exponential current source is injected to mimic the behavior of SEU. The injected current source is given by equation 5.1, where Q is total collected charge $\tau_\alpha(= 200ps)$ and $\tau_\beta(= 50ps)$ are the collection time constants of a junction and initial ion track establishing time constant, respectively [97]. The minimum charge accumulated at a sensitive node, known as the critical charge (Q_c), is sufficient to modify data that was previously kept in a storage node. The Q_c of all the sensitive nodes are estimated, and the lowest of them is considered as the cell's effective Q_c, which indicates its tolerance for SEU. A Verilog code is used in Cadence Virtuoso to generate the current source of equation 5.1.

$$Inj(t) = \frac{Q}{\tau_\alpha - \tau_\beta}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \tag{5.1}$$

Table 5.1 compares the single node SEU sensitivity of all considered FFs at VDD = 1 V and CK = 1 GHz. The Q_c of every single node is estimated, and vulnerable nodes which cause soft errors are analyzed for SET $0 \rightarrow 1$ and $1 \rightarrow 0$ at CK = 0, and CK = 1. As it can be seen, Q_c of the proposed FFs is better than regular FFs and MQ-Quatro, while it

is comparable with other RHBD FFs. In the case of MS-DICE, no soft error is observed on single node SEU simulation for the charge range from 0 to 200 fC.

Table 5.1: Critical Charge Comparison of All Considered Flip-flops @ (1V/1GHz/TT/25°C).

Flip-flop	Flip-flop SEU vulnerable nodes and their corresponding critical charge (fC)			
	CK = 0		CK = 1	
	SETs 1 → 0	**SETs 0 → 1**	**SETs 1 → 0**	**SETs 0 → 1**
TGFF	X3 = 19, X4 = 31	X3 = 23, X4 = 38	X1 = 19, X2 = 35, X3 = 34	X1 = 23, X2 = 39, M = 19
MS-DFF	X3 = 1	X3 = 1	X1 = 2, X3 = 8, X4 = 88	X1 = 2, X3 = 4
MS-DICE	-	-	-	-
MS-Quatro	X7 = 36, X8 = 36	X5 = 39, X6 = 40	X3 = 37, X4 = 36, X7 = 37, X8 = 37	X1 = 41, X2 = 41, X5 = 108, X6 = 110
C²MOS-Quatro	X5 = 37, X6 = 36	X3 = 39, X4 = 40	X5 = 37, X6 = 36	X3 = 114, X4 = 117
TQ-Quatro	SC=37, SD = 37	SA = 42, SB = 39	MA = 66, MC = 37, MD = 37, SA = 124, SC = 102, SD = 108	MA = 41, MB = 39, SA = 101, SB = 95
MQ-Quatro	SC = 21, SD = 21	-	MA = 54, MC = 21, MD = 21, SA = 124, SC = 70, SD = 71	MA = 41, MB = 39, SA = 142
TSPC-Quatro	**Y1 = 32, Y2 = 35, Yn = 29, Y = 28**	**Y1 = Y2 = 36**	**X = 33**	**X1 = 28, Xn = 42**
TSPC-DICE	**X = 92, Xn = 142, Y1 = 45, Y2 = 32, Yn = 43, Y = 32**	**X1 = 29, X2 = 29, Y1 = 54, Y2 = 68, Yn = 52, Y = 65**	**X1 = 57, X2 = Xn = X = 56, Y1 = 136, Y2 = 139, Y = Yn = 138, n1 = 70**	-

5.2.2 Power, Delay, and Energy: Post-layout Simulations

Average DA, along with its D-to-Q delay play an important role in determining which flip-flop is power and energy optimum in a given design. As highlighted by researchers [12, 14], the average DA for the vast majority of FFs in digital circuits is between 5-15%. Various power and timing simulations were carried out at VDD = 1 V and CK = 1 GHz, and VDD = 0.5 V and CK = 50 MHz.

Figure 5.3 and Figure 5.4 depict comparison of the total average power as a function of DA of all investigated FFs. Post-layout power simulation results show that proposed TSPC-Quatro and TSPC-DICE are the most power-efficient amongst all investigated RHBD FFs for all DAs at VDD = 1 V, and at VDD = 0.5 V. For example, at VDD = 1 V, and DA = 10%, TSPC-Quatro consumes 63%, 71%, and 55% less power than MS-DICE, MS-Quatro, and C²MOS-Quatro, respectively. Similarly, TSPC-DICE consumes 63%, 70%, and 54% less power than MS-DICE, MS-Quatro, and C²MOS-Quatro, respectively. These results also highlight that proposed TSPC-Quatro and TSPC-DICE are even more power-efficient than regular FFs, TGFF and MS-DFF for DA less than 10%. Moreover, MS-DICE does not work at low-voltage, and TSPC-Quatro even consumes less power than TSPC-DICE for all DAs. Therefore, the proposed FFs are low-power RHBD FFs.

Figure 5.5 depicts the clock buffer power against DA at VDD = 1 V and 0.5 V. The number of clock transistors in a flip-flop determines how much power the clock buffer

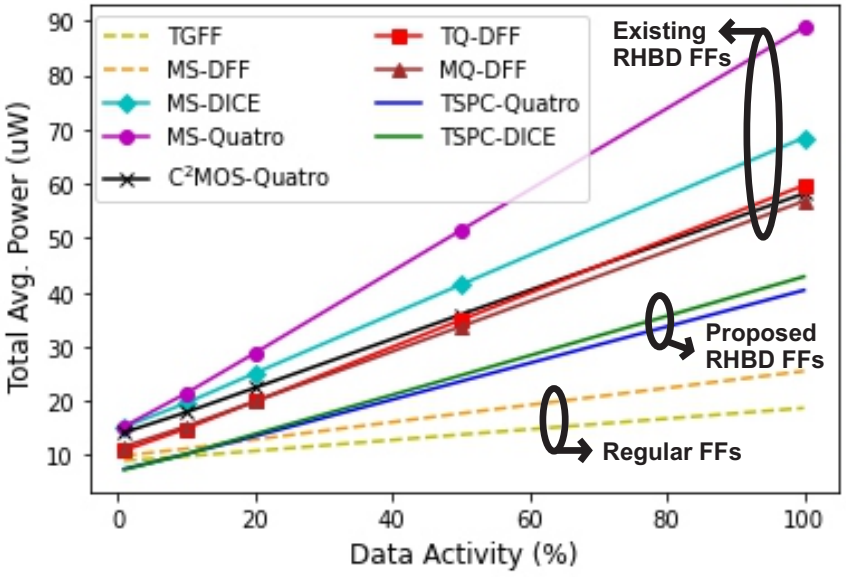


Figure 5.3: Total Average Power Versus DA at VDD = 1 V, CK = 1 GHz.

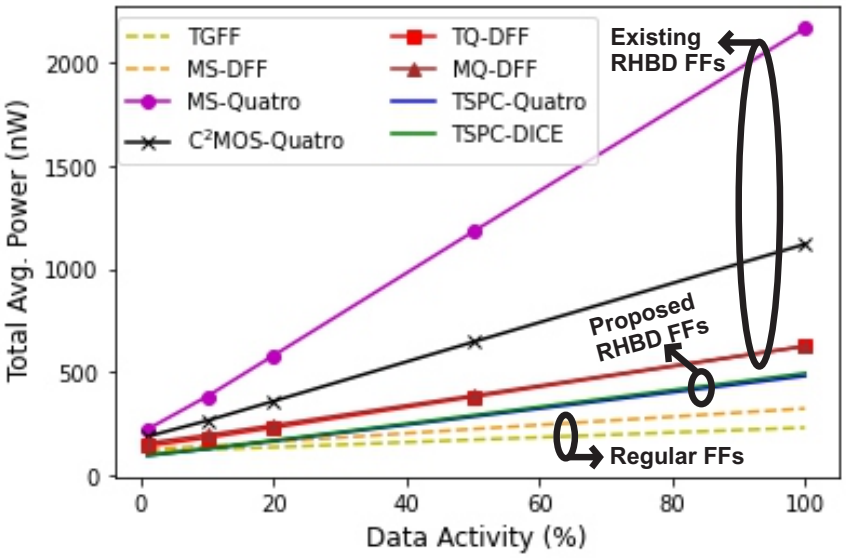


Figure 5.4: Total Average Power Versus DA at VDD = 0.5 V, CK = 50 MHz.

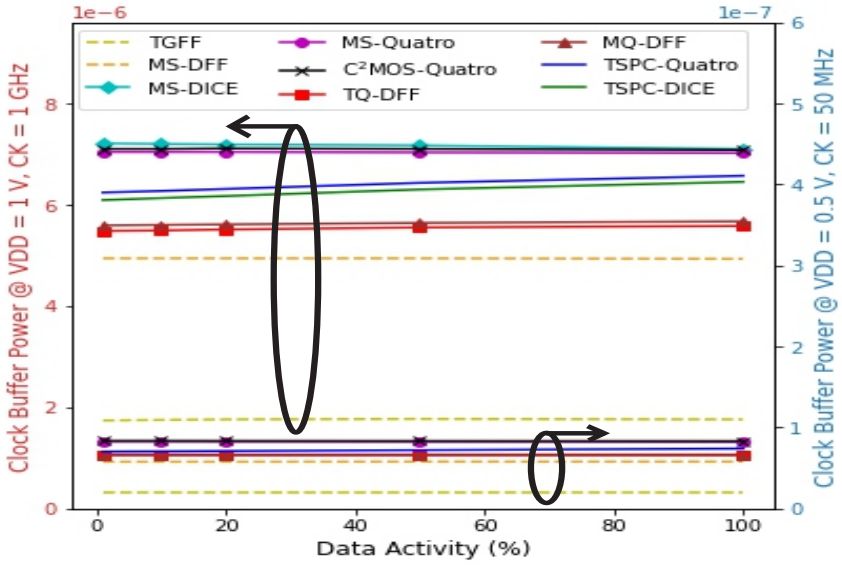


Figure 5.5: Clock Power Versus DA at VDD = 1 V, CK = 1 GHz, and VDD = 0.5 V, CK = 50 MHz.

uses. The proposed FFs, TSPC-Quatro and TSPC-DICE, consume the lowest clock power amongst all examined RHBD FFs. Here, TGFF, MQ-Quatro, and TQ-Quatro exhibit the lowest clock buffer power compared to the proposed FFs. It is because the internal clock buffers drive every internal clock transistor; thus, the portion of their power consumption related to the clock is added to the flip-flop's power consumption.

Figure 5.6 and Figure 5.7 compares the PDP of FFs for various DAs at voltages of 1 V and 0.5 V. Proposed TSPC-Quatro and TSPC-DICE show energy-efficiency amongst all considered RHBD FFs for all DAs at VDD = 1 V and 0.5 V. For example, at VDD = 1 V, and DA = 10%, TSPC-Quatro consumes 82%, 60%, and 45% less energy than MS-DICE, MS-Quatro, and C^{2}MOS-Quatro, respectively. Similarly, TSPC-DICE consumes 84%, 63%, and 48% less energy than MS-DICE, MS-Quatro, and C^{2}MOS-Quatro, respectively. Furthermore, at low-voltage, their energy-efficiency further improves. For instance, at low DA, they even become more energy-efficient than regular flip-flop MS-DFF, and follows only TGFF. This simulation verifies that proposed FFs are suitable for low-energy, soft error tolerant applications.

Table 5.2 depicts worst-case timing of all considered FFs tested at voltages of 1 V and 0.5 V. At VDD = 1 V, regular FFs, TGFF, and MS-DFF have the lowest D-Q delay, followed by C^{2}MOS-Quatro, MS-Quatro, TSPC-DICE, and TSPC-Quatro. At low-voltage,

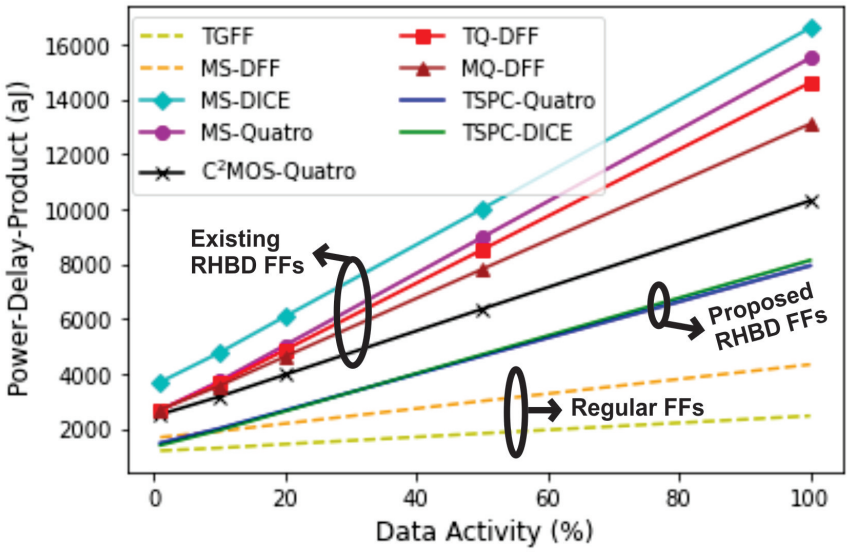


Figure 5.6: Total Average Power Versus DA at VDD = 1 V, CK = 1 GHz.

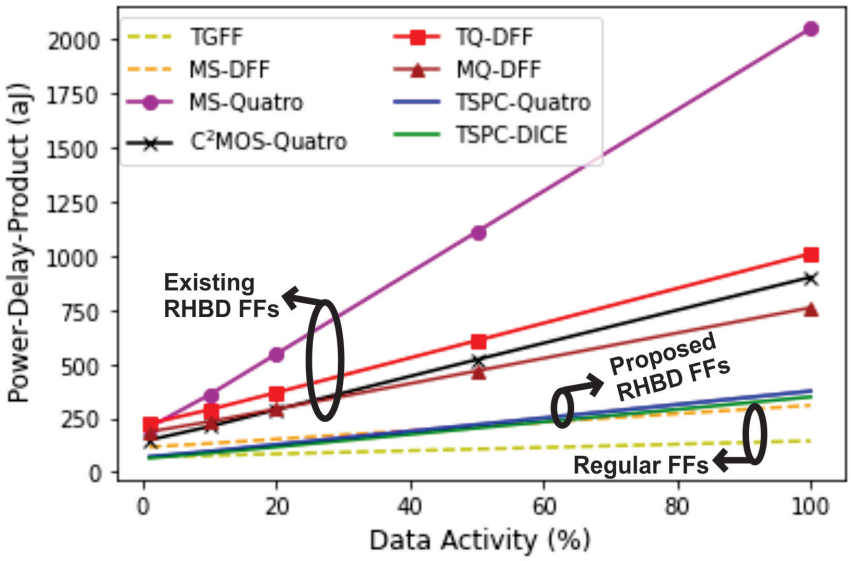


Figure 5.7: Total Average Power Versus DA at VDD = 0.5 V, CK = 50 MHz.

Table 5.2: Post-layout Worst-case Delays For All Analyzed RHBD Flip-flops @ (TT/25°C).

Flip-flop	Delay (ps)							
	Voltage = 1 V, Clock = 1 GHz				Voltage = 0.5 V, Clock = 50 MHz			
	D-CK	CK-Q	D-Q	Hold time	D-CK	CK-Q	D-Q	Hold time
TGFF	22	110	132	-11.70	169	466	635	-136.1
MS-DFF	52	118	170	-48.14	493	469	962	-539.8
MS-DICE	99	144	243	-73.68	-	-	-	-
MS-Quatro	86	88	174	-77.82	383	560	943	-697.4
C^{2}MOS-Quatro	60	117	177	-22.76	271	537	808	-156.6
TQ-Quatro	67	171	244	-63.23	648	965	1613	-586.9
MQ-Quatro	57	174	231	-53.77	419	799	1218	-481.5
TSPC-Quatro	**85**	**111**	**196**	**-49.45**	**298**	**484**	**782**	**-463.5**
TSPC-DICE	**79**	**111**	**190**	**-54.38**	**288**	**418**	**706**	**-480.1**

TSPC-DICE and TSPC-Quatro show better performance compared to other other considered RHBD FFs, and they only follows TGFF. This post-layout simulation result verifies that the proposed FFs are suitable for high-performance soft error tolerant applications, particularly at low-voltage.

Table 5.3 makes an overall comparison amongst all analyzed FFs at VDD = 1 V, CK = 1 MHz. Proposed TSPC-DICE and TSPC-Quatro only need four and five clock transistors, respectively, for their clock circuitry. TSPC-DICE and TSPC-Quatro require a total transistor count of of 36 and 35, respectively, which not only makes these area-efficient but also power- and energy-efficient amongst all considered RHBD FFs for all DAs. This comparison illustrates that the proposed RHBD FFs are attractive for low-power, low-energy, low-voltage, and high-performance space and safety-critical related applications. TSPC-Quatro is suggested for low-power applications, and TSPC-DICE is suggested for low-energy and high-performance applications.

Table 5.3: Overall Comparison Of All Investigated Flip-flops @ (1V/1GHz/TT/25°C).

Flip-flop	# of CK Trans.	Total # of Trans.	Area (um^2)	D-Q Delay (ps)	Power (uW) at 20%, 50 % DA	PDP (fJ) at 20%, 50 % DA	Qcritical (fC)
TGFF [Std Cell]	12	24	11.50	132	10.8, 13.8	1.43, 1.82	19
MS-DFF[32]	10	24	11.50	170	12.9, 17.7	2.18, 3.00	1
MS-DICE[32]	10	36	21.73	243	25.1, 41.4	6.08, 10.00	-
MS-Quatro[32]	10	38	21.73	174	28.8, 51.4	5.03, 8.96	36
C^{2}MOS-Quatro[33]	10	30	17.89	177	22.4, 35.9	3.96, 6.35	36
TQ-Quatro[34]	10	36	19.60	244	19.9, 34.9	4.86, 8.51	37
MQ-Quatro[34]	10	44	21.30	231	19.9, 33.7	4.62, 7.80	21
TSPC-Quatro [This Work]	**5**	**35**	**19.17**	**196**	**13.5, 23.6**	**2.66, 4.64**	**28**
TSPC-DICE [This Work]	**4**	**36**	**19.17**	**190**	**13.9, 24.7**	**2.63, 4.69**	**29**

5.3 Test-chip Measurement Results

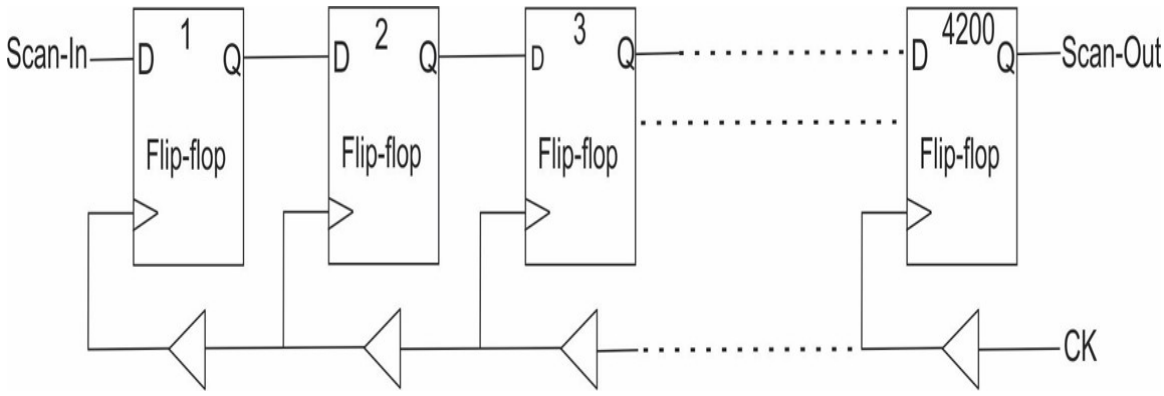


Figure 5.8: Block Diagram of the Scan-chain of 4200 Flip-flops with Reverse Clocking Scheme.

To further validate the power-savings of the proposed RHBD FFs and their radiation immunity, three scan-chain of 4200 FFs each are implemented for regular DFF, and proposed TSPC-DICE and TSPC-Quatro FFs, and are shown in Figure 5.8. The clock is routed opposite to the data flow direction to avoid hold time violations. The flip-flop cells were optimized for the area and implemented like a standard library cell. Only metal layers 1 and 2 were used for the interconnects within a flip-flop.

Figure 5.9 shows the overall test-chip implementation and die micrograph. In terms of area, TSPC-Quatro scan-chain consumes 37%, and TSPC-DICE scan-chain consumes 41% more area than DFF scan-chain.

5.3.1 Power Measurement

Figure 5.10 illustrates the test-chip's power measurement setup. A pattern generator is used to generate the clock signal and the corresponding DA signal, and a 4-channel oscilloscope is used to view the corresponding input and output signal waveforms. A 3.3 (also 2.5 V) supply is used for the IOs, 1.2 (also 1 V) is used for the core voltage, and 1 V (also variable) is used for the VDD pin of the scan-chain. The average current is noted down on the power supply screen used for the scan-chain VDD pin for the corresponding DA, and multiplied with the corresponding voltage to get the total power consumption.

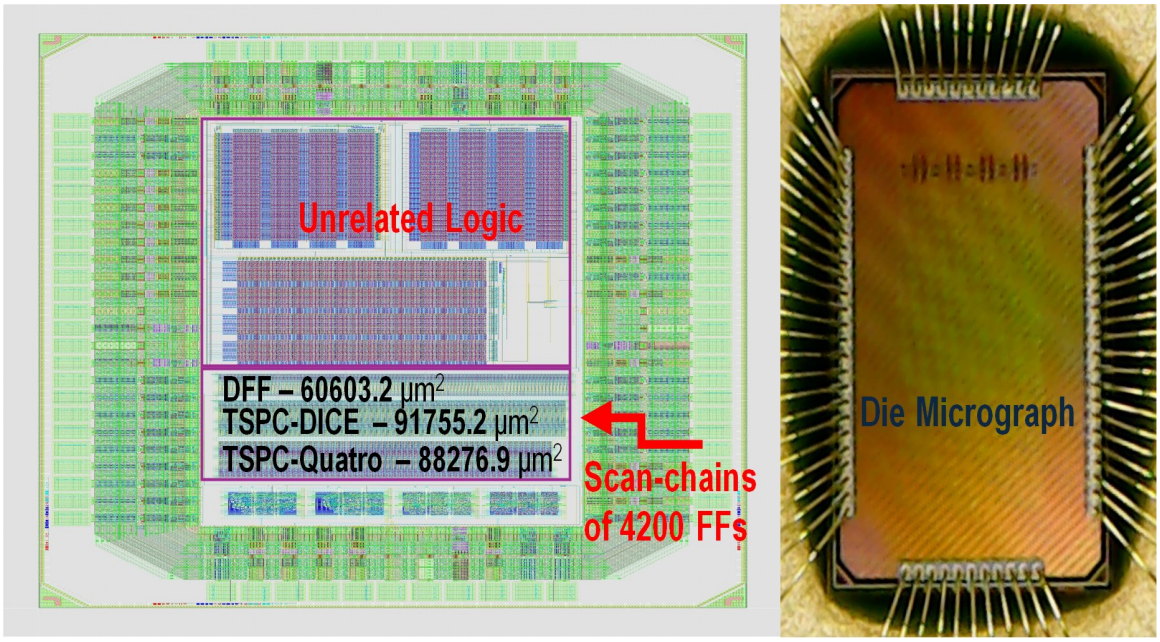


Figure 5.9: Overall Test-chip and Die Micrograph.

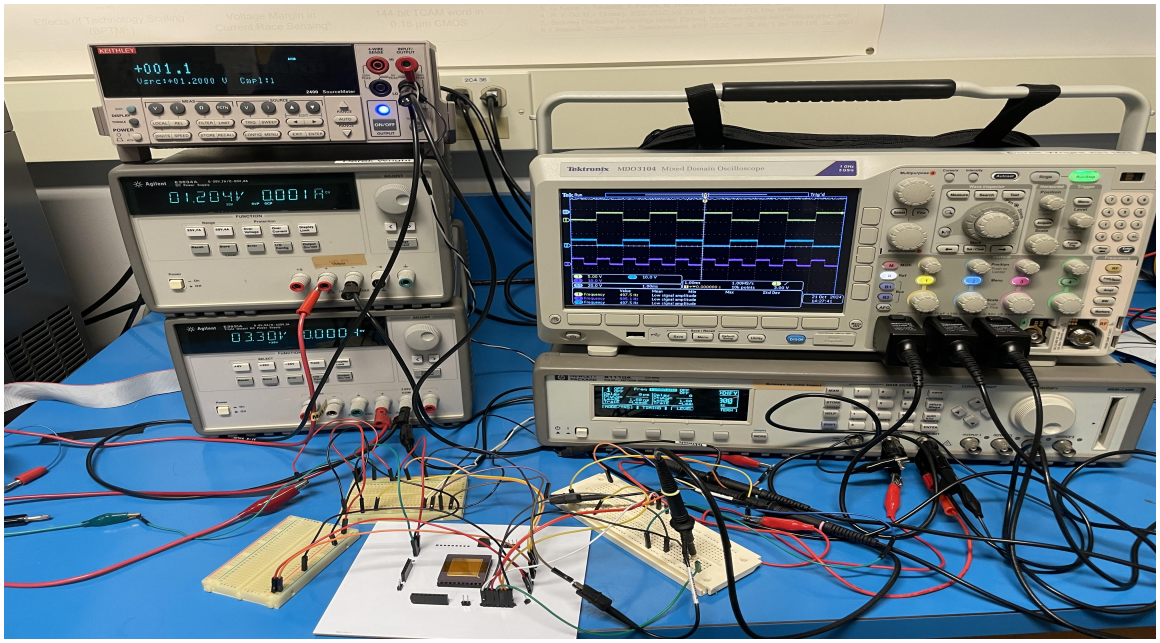


Figure 5.10: Test-chip Power Measurement Setup.

Figure 5.11 and Figure 5.12 show the test-chip power measurement results for the scan-chains of 4200 FFs at various DAs and voltages. TSPC-DICE and TSPC-Quatro scan-chains show power-efficiency over the regular DFF scan-chain for the DAs around 35% or lower. For example, in Figure 5.11 at DA = 6.25%, VDD = 1 V, and CK = 5 MHz, scan-chains of TSPC-DICE, and TSPC-Quatro consume 11%, and 9% less power than the DFF scan-chain. Figure 5.12 illustrates power consumption of three scan chains at VDD from 0.8 – 1.2 V with DA = 12.5%, CK = 5 MHz. Measurement results show that TSPC-DICE and TSPC-Quatro scan-chains consume less power compared to the DFF scan chain. Table in Fig. 6 provides an overall comparison for all investigated FFs. Owing to fewer clock transistors, the TSPC-DICE and TSPC-Quatro are at least 50% power-efficient at 20% DA, and at least 39% energy-efficient with respect to other RHBD FFs making them attractive for low-power, low-energy, and safety-critical applications.

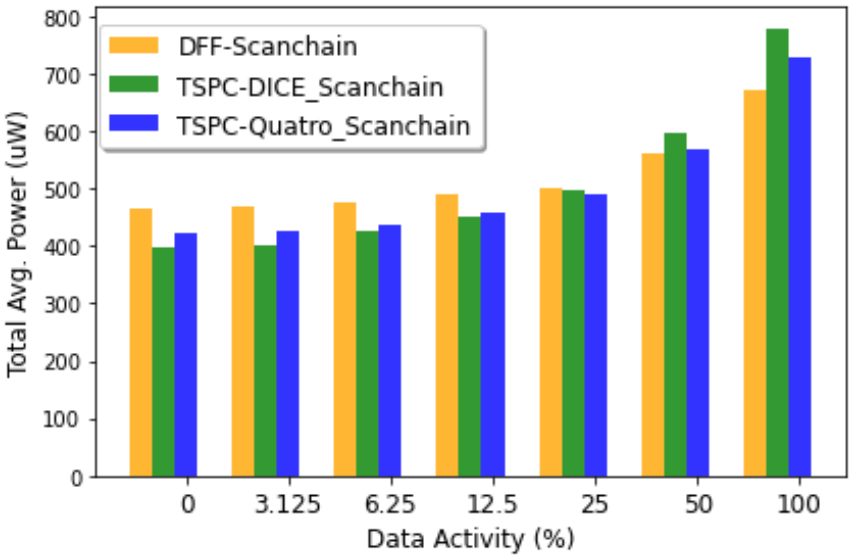


Figure 5.11: Power Consumption Versus DA @ VDD = 1 V, CK = 5 MHz.

5.4 Summary

In this chapter, We propose two static, contention-free, master-slave based soft error tolerant, TSPC FFs named as TSPC-Quatro, and TSPC-DICE. Post-layout simulation results in CMOS 65 nm technology show that TSPC-Quatro and TSPC-DICE are the most power

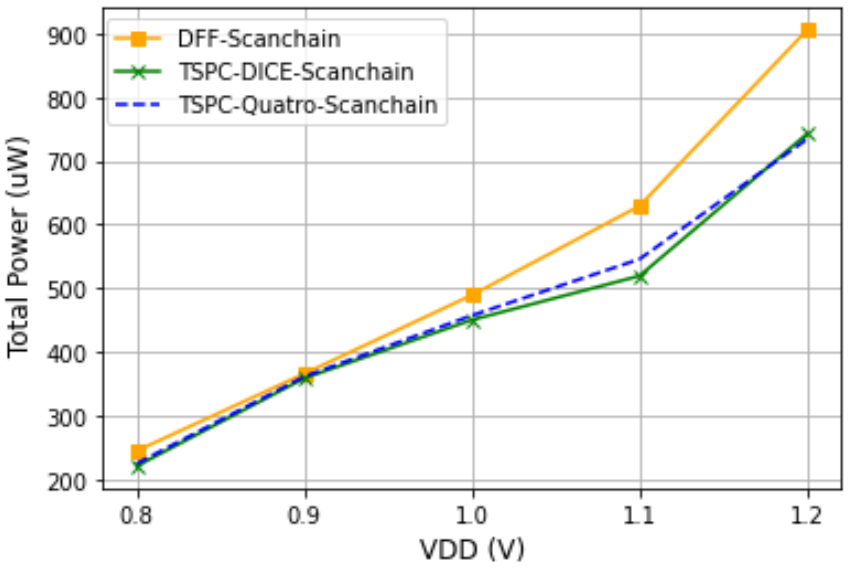


Figure 5.12: Power Consumption Versus VDD @ DA = 12.5%, CK = 5 MHz.

and energy-efficient amongst all considered RHBD FFs. At low-voltage, the power and energy-efficiency of these proposed FFs improve further. TSPC-Quatro and TSPC-DICE have a critical charge of 28 fC, and 29 fC, respectively, and in terms of radiation immunity, they are comparable with other state-of-the-art RHBD FFs. Test-chip measurement results show that TSPC-DICE and TSPC-Quatro scan-chains consume less power compared to the DFF scan chain. Therefore, TSPC-Quatro is suitable for low-power, and TSPC-DICE is suitable for low-energy, and high-performance safety-critical related applications.

Chapter 6

Low-power Dual Edge-triggered TSPC Flip-flops

Power and energy consumption is one of the primary design constraints for ICs [73, 74, 75]. Aiming for high-performance computing at lower energy consumption, portable and hand-held electronics are becoming more and more popular. In order to reduce the overall cost of manufacturing, a VLSI designer aims to minimize area and complexity while preserving the optimal power-to-delay ratio for a circuit. FFs are a fundamental component of digital circuits. In a typical processor, hundreds of thousand of FFs are used [52]. Therefore, their speed, power, and energy have a significant impact on the overall performance of a digital system [16, 52, 76, 15, 77, 65, 79, 67, 80].

Voltage scaling is a popular and commonly used design technique in electronics systems to optimize the power-efficiency. A quadratic reduction in the dynamic power consumption can be achieved by scaling down the supply voltage. Therefore, voltage scaling is commonly used in power- and energy-constrained battery-operated miniature sensors and IoT applications. When applying such voltage scaling to FFs, one of the main challenges is the aggressive voltage scalability. Furthermore, battery-powered applications want low sensitivity to supply voltage since battery voltage drops over time. Ensuring robust flip-flop operation at low supply voltage is a non-trivial challenge, particularly with advanced technologies where process variation is becoming increasingly problematic because of the increased sensitivity to the processed variation in the low-voltage regimes.

It has been demonstrated that TSPC is an effective method for achieving very high-speed digital VLSI design [98]. A DET flip-flop is an effective approach to enhance the performance and reduce the power consumption generally in digital circuits and particularly

in clock distribution networks. In contrast to SET FFs, this method uses a flip-flop to sample data on both the rising and falling edges of the clock, requiring only half the clock frequency to achieve the same data throughput [99, 100, 58].

In this chapter, we propose three very low-power latch-mux type TSPC DET FFs referred to as LPLD-DET, LPHD-DET, and 8CTSPC-DET suitable for aggressive voltage scaling down to a voltage regime close to the threshold. The main contributions are:

Proposed FFs are the first of its kind, which use a lower number of clocks and an overall number of transistors in a latch-MUX type configuration while maintaining static, contention-free, true single-phase clock operation.

6.1 Proposed TSPC DET Flip-flops

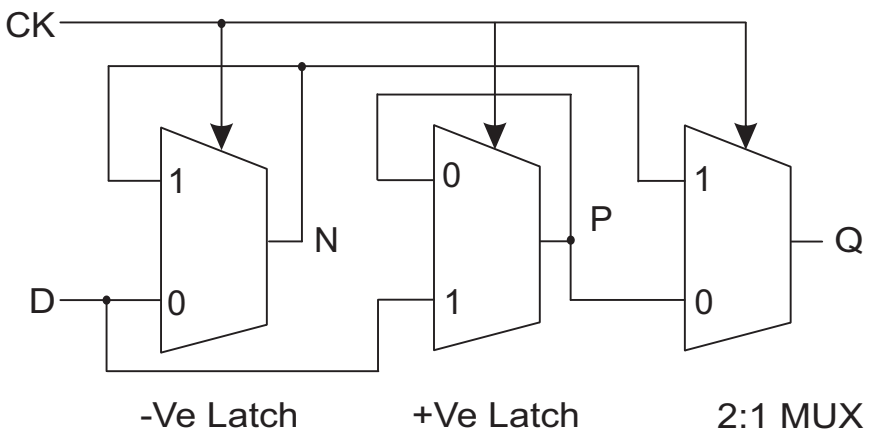


Figure 6.1: Block Diagram of the Proposed Low-power LPLD-DET, and LPHD-DET Flip-flops.

Figure 6.1 depicts the core concept of the proposed static, contention-free, power and energy-efficient latch-mux type TSPC DET FFs for low and high DAs. For LPLD-DET, and LPHD-DET, a 2:1 multiplexer is used as a latch. This arrangement employs a negative latch to sample the data when the clock is low, a positive latch to sample the data when the clock is high, and a single-phase clocked 2:1 multiplexer to send the negative latch and positive latch outputs' data at its output Q on the rising and falling clock edges, respectively.

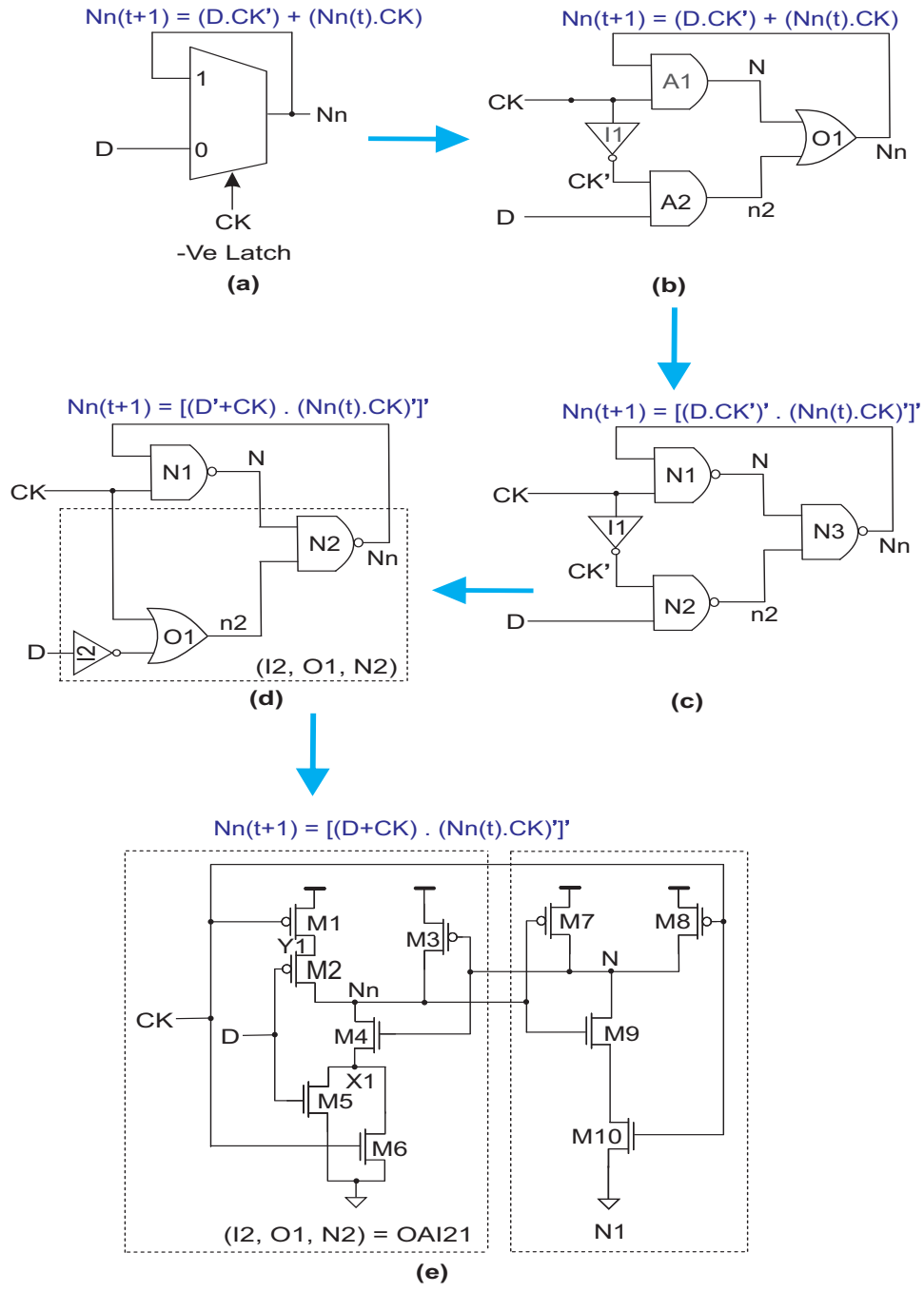


Figure 6.2: Core Concept of the Proposed LPLD-DET and LPHD-DET Flip-flops Using Negative Latch.

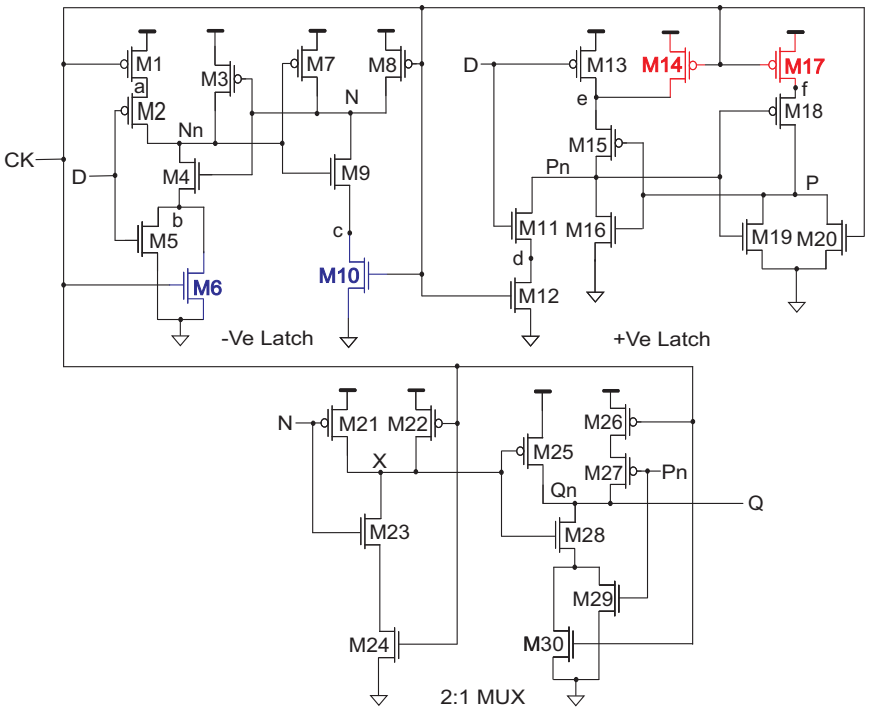


Figure 6.3: Transistor-level Equivalent of the Fig. 6.1 of the Proposed LPLD-DET and LPHD-DET Flip-flops.

Figure 6.2 illustrates the intermediate stages of converting the block diagram of Figure 6.1 into a transistor-level circuit diagram. For the sake of simplicity, only the negative latch is taken as a reference, as the positive latch is just the complement of it w.r.t. the clock. Figure 6.2(a) is a negative latch that samples the new data when the clock is low and holds the previous data when the clock is high, as seen in Equation 6.1. Figure 6.2(b) translates the block diagram into equivalent logical gates. Figure 6.2(c) converts logical gates into universal NAND gates, as shown in Equation 6.2. At this stage, we still need two-phase clocks, CK, and CK'. To get rid of CK', NAND gate, N2, and Inverter, I1, are converted into equivalent OR gate, O1, and the data was complemented by an Inverter, I2, in Figure 6.2(d) and mathematically described in Equation 6.3. This circuit samples the data at node Nn when the clock is low and holds its previous value when the clock is high. Hence, the circuit operates on the single-phase of the clock only.

It can be observed in Figure 6.2(d) that gates I2, O1, and N2 are equivalent to the OAI21 compound gate, which only needs six transistors to implement. Figure 6.2(e) is the transistor level equivalent of Figure 6.2(d). This schematic diagram samples the comple-

ment of data when the clock is low, and holds the value of previous data when the clock is high, as seen in Equation 6.4. Thus, negative latch needs a total of ten transistors, including four single-phase clock transistors. Hence, a full static DET flip-flop of Figure 6.1 can be drawn with a total of 30 transistors, including 12 clock transistors, as shown in Figure 6.3. Where the positive latch is just the complement of the negative latch and needs ten transistors to implement. Another ten transistors, that include four clock transistors, are needed to implement the output multiplexer. The proposed DET design can be further optimized for DA - Low Power Low Data (LPLD-DET), and Low Power High Data (LPHD-DET) as described below.

Mathematically,

$$Nn(t+1) = (D.CK') + (Nn(t).CK). \tag{6.1}$$

where Nn(t) is the present state output (previous state input data), Nn(t+1) is the next state output, and D is the present state input data

$$Nn(t+1) = [(D.CK')'.(Nn(t).CK)']' \tag{6.2}$$

$$Nn(t+1) = [(D' + CK).(Nn(t).CK)']' \tag{6.3}$$

$$Nn(t+1) = [(D + CK).(Nn(t).CK)']' \tag{6.4}$$

6.1.1 Low-power at Low DA TSPC DET (LPLD-DET) Flip-flop With only Eight Clock Transistors

Figure 6.4 shows a low-power and low-energy TSPC DET flip-flop for low DAs, referred to as LPLD-DET, and is an optimized version of Figure 6.3 with a total of 34 transistors, including only 8 clock transistors. An inverter with PMOS M7 and NMOS M8 is used to complement the data. An output buffer with transistors M33 and M34 is added to increase the robustness of the flip-flop for low-voltage operation, and the inputs of multiplexers are connected to nodes Nn and P to accommodate the logic of the output buffer. The clock transistors M6 and M10 in Figure 6.3 (highlighted in blue) are used to provide ground connections to nodes b and c; costing two clock transistors. In the Figure 6.4, they are merged into one (M6) as shown.

An NMOS DN-driven transistor M12 is added at node C, which makes sure that nodes b and c always have a ground path when CK = 1. Similarly, clock transistors M14 and M17 in Figure 6.3 (highlighted in red) are merged into a single clock transistor, M18 in Figure 6.4. A PMOS DN-driven transistor is added at node f to make sure nodes e and f always

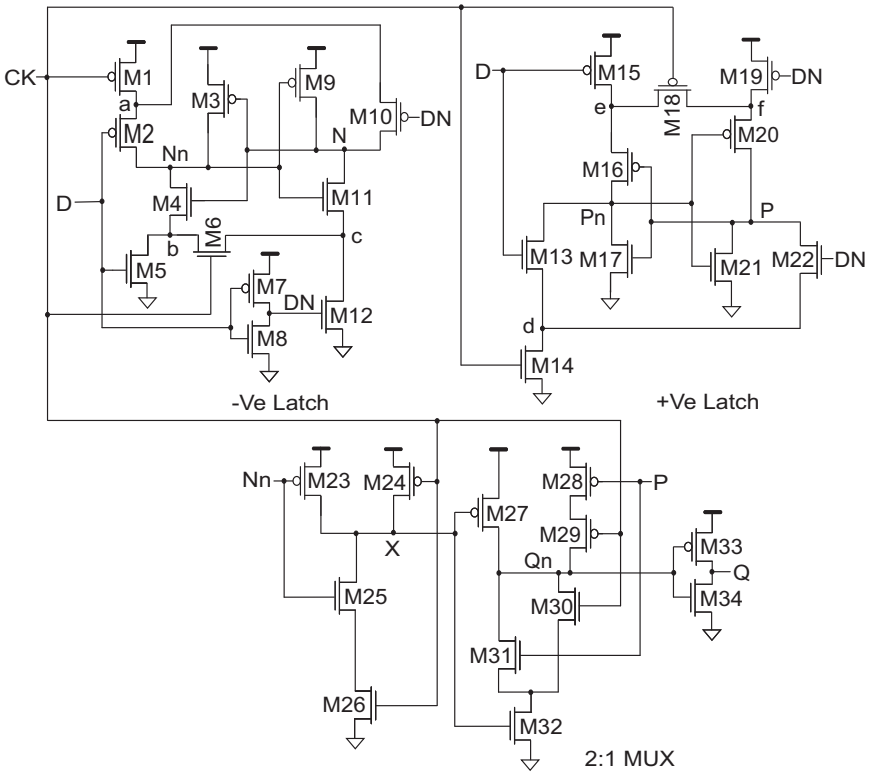


Figure 6.4: Schematic Diagram of the Proposed LPLD-DET Flip-flop.

have a VDD path when CK = 0. A clock transistor M8 of Figure 6.3 is replaced with the DN-driven transistor M10, and its source is connected with the drain of clock transistor M1 at node a. This approach eliminates the unnecessary internal redundant transition at node N. Similarly, M20 in Figure 6.3 is replaced with the DN-driven transistor M22, and its source is connected with the drain of clock transistor M14 at node d. This approach eliminates the unnecessary internal redundant transitions at node P. Thus, the circuit is redundant transition-free, which makes LPLD-DET attractive for low DAs.

Figure 6.5 illustrates the working principle of the proposed LPLD-DET flip-flop for different clock and data states, highlighting on and off transistors, and high and low logic nets. When CK = 0, D = 0, and Qprev = 1, the negative latch samples the complement of new data at node Nn through transistors M1 and M2. Node P of the positive latch holds its previous state value to logic high through transistors M15, M18, and M20, which turn on M17 to connect node Pn to the ground. The 2:1 MUX samples the node P logic value at the output node Q through transistors M31-M33. Thus, output stays at logic high. When CK is rising, node N of the negative latch holds its previous state value to logic low. Thus, M3 is always turned on to make sure node Nn is holding its previous state value to logic high. The positive latch samples the new data at node P through transistors M22 and M14, which turn on M16 to make Pn at logic high. The 2:1 MUX samples the output of node Nn at output Q through nodes X and Qn via transistors M25-27. Thus, Q makes a high-to-low transition during the rising edge of the clock.

On the other hand, when CK = 0, D = 1, and Qprev = 0, node N goes to logic high through transistors M1 and M10; thus, M4 is turned on to connect node Nn to the ground through M5. Node Pn holds its previous state value to logic high through transistors M16, M18, and M19, which turn on M21 to wire node P to the ground. A 2:1 MUX samples the output of node P at output Q through M28, M29, and M34; thus, output stays at logic low. When CK is rising, node Nn of the negative latch holds its previous state value to logic low through M4 and M5. As a result, M9 is always turned on to make node N to logic high. In positive latch, node Pn samples the complement of data and turns on transistor M20 to make node P at logic high. A 2:1 MUX at the output samples the output of node Nn through transistors M23, M30, M32, and M33; as a result, Q makes a low-to-high transition.

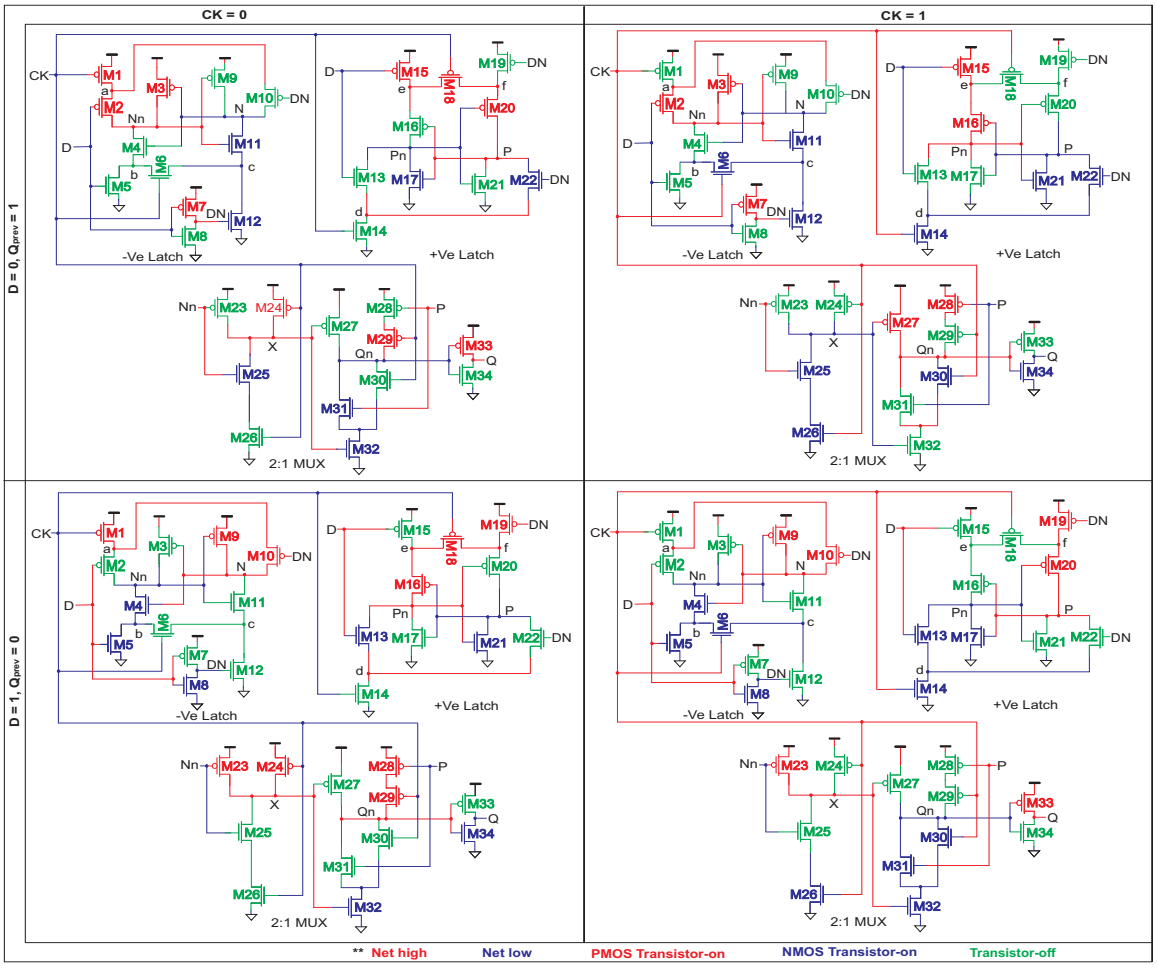


Figure 6.5: Working principle of the LPLD-DET for different clock and data states, highlighting on and off transistors and high and low logic nets.

6.1.2 Low-power at High DA TSPC DET Flip-flop (LPHD-DET) With only Ten Clock Transistors

Figure 6.6 shows a low-power and low-energy TSPC DET flip-flop suitable for high DAs, referred to as LPHD-DET, and is an optimized version of Figure 6.3 with a total of 30 transistors, including 10 clock transistors. Clock transistor M10 in Figure 6.3 is eliminated, and the source of M9 is connected with the drain of M11 at node d. Similarly, clock transistor M14 in Figure 6.3 is eliminated, and the source of clock transistor M22 is connected at node e. Thus, node e goes logic value high when clock is low through transistors M19 and M20 when D = 1, and through transistor M12 when D = 0. An output buffer with transistors M29 and M30 is added in the multiplexer to increase the robustness of the flip-flop in low-voltage operation, and inputs of multiplexers are connected to nodes Nn and P to accommodate the logic of the output buffer. Therefore, the proposed LPHD-DET only requires a total of 30 transistors, including 10 clock transistors, while maintaining static, contention-free, and single-phase clock operation for near-the-threshold voltage applications.

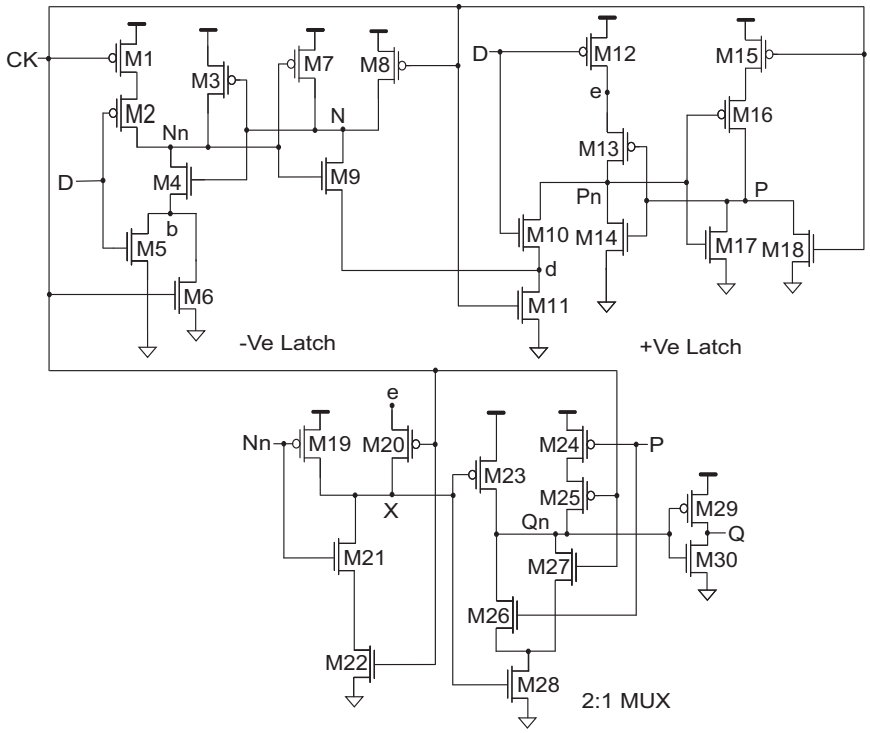


Figure 6.6: Schematic Diagram of the Proposed LPHD-DET Flip-flop.

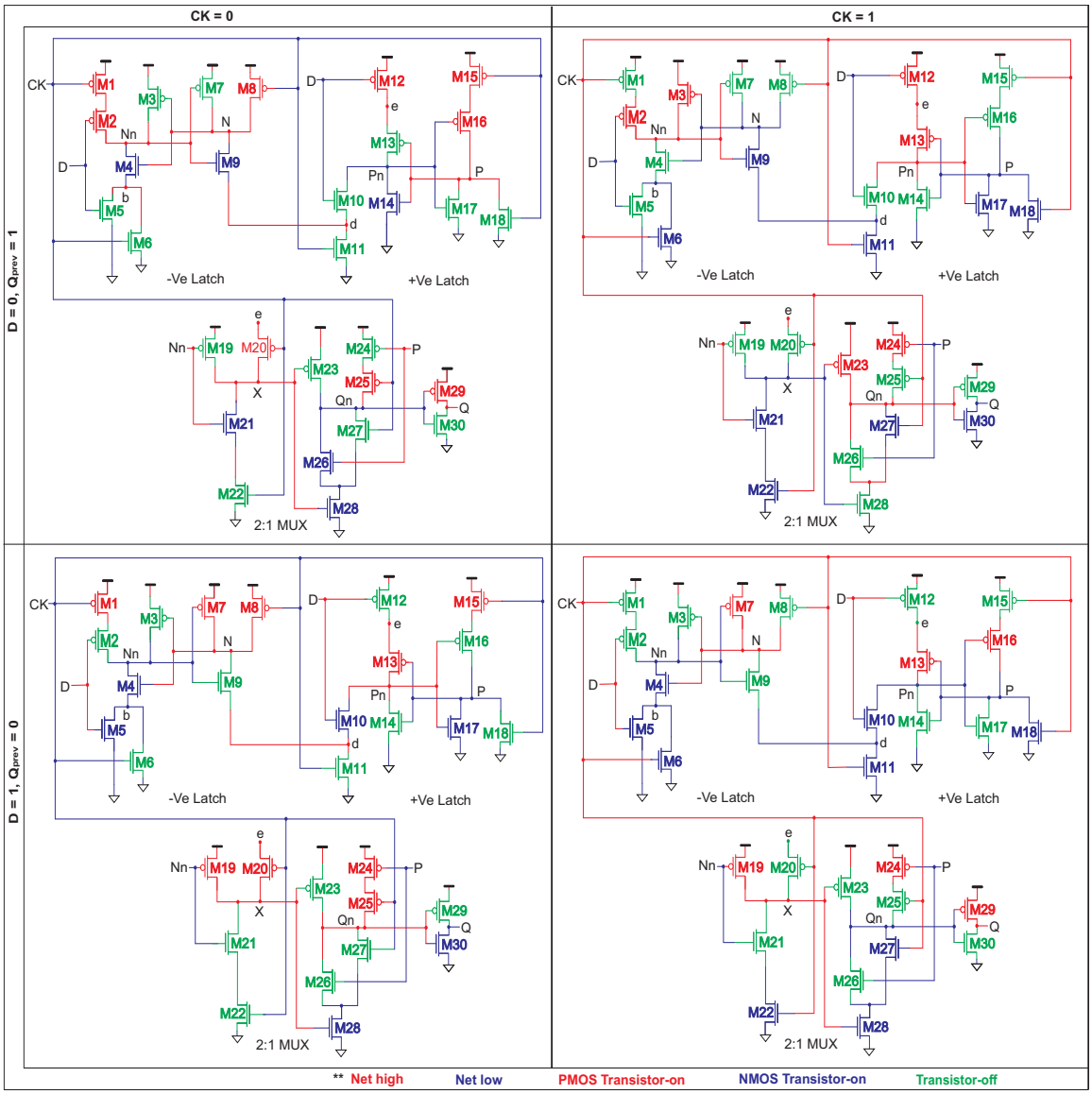


Figure 6.7: Working principle of the LPHD-DET For Different Clock and Data States, Highlighting On and Off Transistors and High and Low Logic Nets.

The working principle of LPHD-DET is similar to LPLD-DET, as illustrated in Figure 6.7. When CK = 0, D = 0, and Qprev = 1, the negative latch samples the complement of new data at node Nn through transistors M1 and M2. The node P holds its previous state value to logic high through transistors M15 and M16, which turn on M14 to connect node P to the ground. Thus, Q stays at logic high through transistors M26, M28, and M29. When CK rises, node N is wired to ground through M9 and M11, which turn on M13; thus, node Nn holds its previous state value to logic high. Node P is connected to ground through M18, which turns on M13 to make node Pn to logic high. The output of node Nn is transferred to Q through nodes X and Qn via transistors M21-23; as a result, Q makes a positive-to-negative transition.

Similarly, when CK = 0, D = 1, and Qprev = 0, node N goes high to connect Nn to ground through transistors M4 and M5. Node P holds its previous state value to logic low; thus, output stays at logic low though transistors M24, M25, and M30. When CK rises, node Nn stops sampling the complement of new data and holds its previous state value. Node p goes to ground through M18, and node Pn samples the complement of data through transistors M10 and M11. Node X goes high through M19, which makes node Qn to logic low through M27 and M28. As a result, Q makes a low-to-high transition.

6.1.3 Ultra Low-power TSPC DET Flip-flop (8CTSPC-DET) With only Eight Clock Transistors

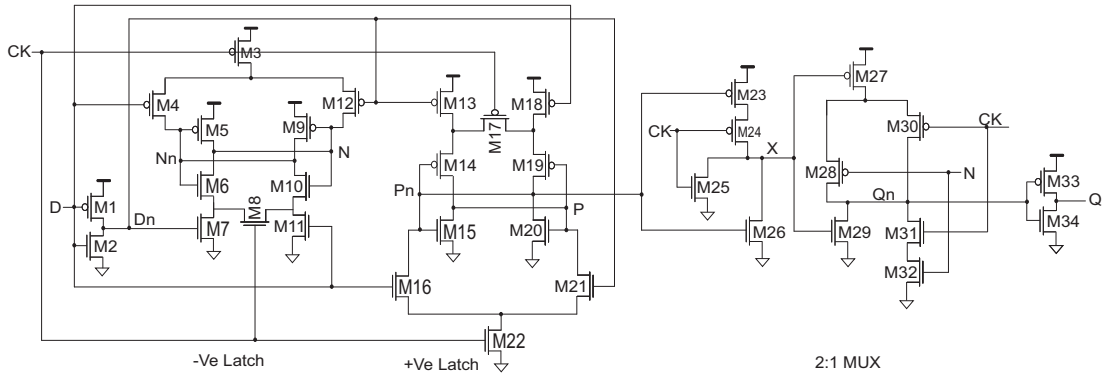


Figure 6.8: Schematic Diagram of the Proposed 8CTSPC-DET Flip-flop.

Another novel very low-power TSPC DET flip-flop is shown in the Figure 6.8 referred to as "8CTSPC-DET". The working functionality of this flip-flop is similar like LPLD-DET and LPHD-DET FFs, but with a different latch circuit mechanism. 8CTSPC-DET even

further saves the power-efficiency at low DAs and needs a total of 34 transistors, including 8 clock transistors.

When CK = 0, D = 0, Qprev = 1, transistors M3 and M4 are turned on to make node Nn to logic high; thus, M6 is turned on to connect node N to ground through M7. Therefore, negative latch samples the new data. Positive latch holds its previous state values, Pn = 0, and P = 1, and sends this data to the output of 2:1 MUX through nodes X and Qn. Thus, node X goes to logic high through transistors M23 and M23, which turn on M29 to make Qn logic low; thus, Q stays high. When CK changes to high, nodes N and Nn stop sampling and hold their previous state values. Nodes P and Pn sample the new data and its complement values, respectively. Therefore, 2:1 mux samples the output of node N at output Q through nodes X and Qn. Transistor M25 is turned on to make node X logic high, which turns on M24. Thus, Qn goes to logic high through transistors M27 and M28. As a result, Q makes a positive to negative transition.

On the other hand, when CK = 0, D = 1, Qprev = 0, node N goes to logic high through transistors M3 and M12; as a result, M10 is turned on to connect node Nn to ground through M11. Nodes P and Pn hold their previous state values to logic low and high, respectively. A 2:1 mux samples the output of node Pn to output Q through nodes X and Qn. Node X is wired to ground through M26, which turns on M27. Thus, node Qn goes to logic high through M27 and M28. As a result, Q stays at logic low. When CK is rising, nodes N and Nn hold their previous state values to logic high and low, respectively. Nodes P and Pn sample the new data and its complement, respectively. Transistor M25 is turned on to make node X at logic low and activates M27. Node Qn is wired to ground through M31 and M32; thus, Q makes a low to high transition.

6.2 Post-layout Simulation Results

In order to ensure a fair comparison on power, energy, performance, and area, layouts of all the considered latch-mux type DET FFs (as shown in Figure 6.9) were designed like a standard library cell in TSMC CMOS 65 nm technology with minimum size transistor lengths of 60 nm and widths for all NMOS transistors = 200 nm and all PMOS transistors = 400 nm. To evaluate the performance metrics of all the DET FFs under investigation, the same test bench as in Figure 4.7 was used to measure the power, delay, and energy.

Several post-layout power and timing simulations were carried out to characterize the power, delay, and energy of the TSPC DET FFs. Figure 6.10 and Figure 6.11 show the total power consumption of DET FFs at VDD = 1 V, CK = 1 GHZ, and VDD = 0.5, CK = 50 MHz.

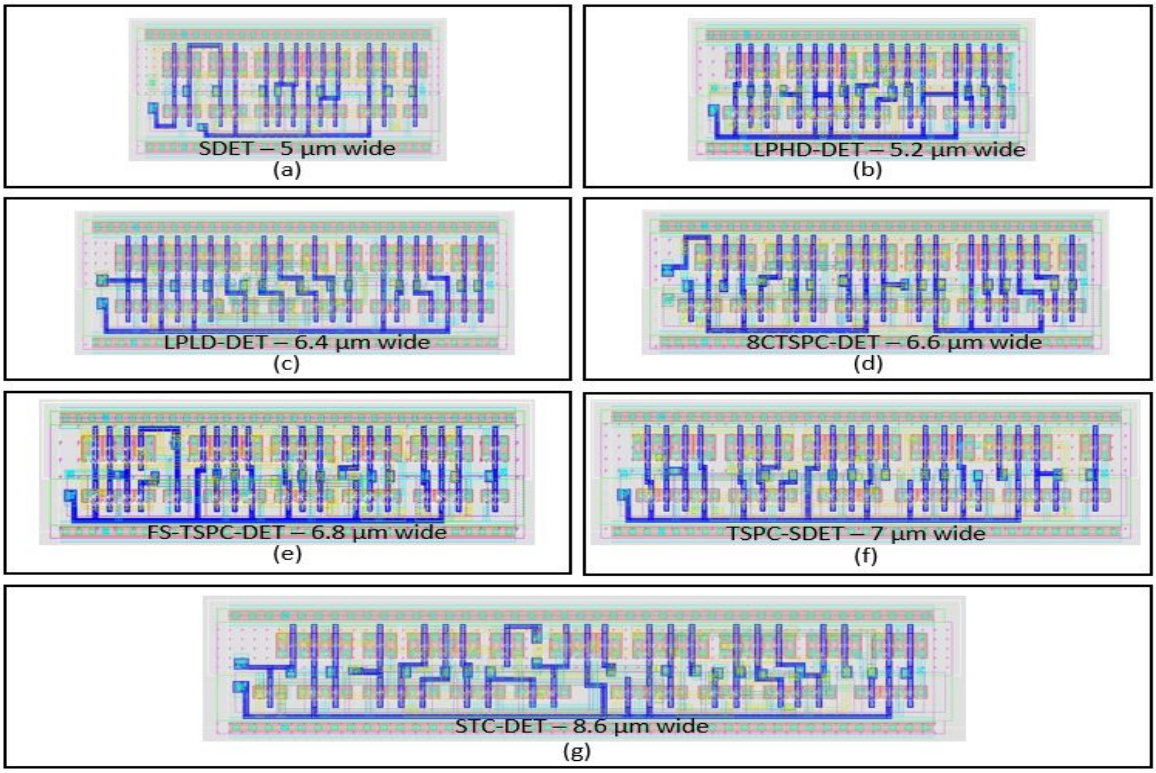


Figure 6.9: The Cell Layout of (a) SDET, (b) LPHD-DET, (c) LPLD-DET, (d) 8CTSPC-DET, (e) FS-TSPC-DET, (f) TSPC-SDET, and (g) STC-DET in TSMC 65 nm CMOS Technology.

As can be seen, the proposed 8CTSPC-DET, and LPLD-DET are power-efficient for low DAs between 3-30%, and LPHD-DET is for higher DAs from 45% amongst all considered DET FFs. For example, at nominal voltage and DA = 25%, 8CTSPC-DET and LPLD-DET consume 14% less power compared to their closet DET, TSPC-SDET, in the comparison group. Similarly, in higher DA scenario with DA = 100% at nominal voltage, the LPHD-DET consumes 33% less power compared to its closet DET, FS-TSPC-DET, in the comparison group. The STC-DET is the most power-efficient for DAs less than 3%, followed by 8CTSPC-DET and LPLD-DET. The power consumption of STC-DET increases dramatically as DA increases slightly; hence, it consumes the highest power amongst all.

Figure 6.12 and Figure 6.13 compare the worst-case D-Q delay of all considered DET FFs at VDD = 1 V, CK = 1 GHZ, and VDD = 0.5, CK = 50 MHz. As can be seen, LPHD-DET has the lowest D-Q delay amongst all investigated FFs, followed by TSPC-

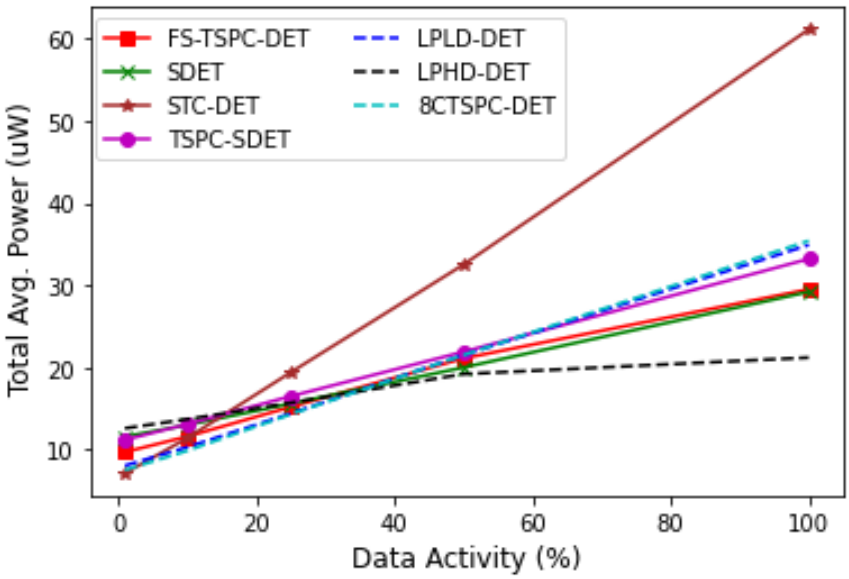


Figure 6.10: Total Average Power Versus DA at VDD = 1 V, CK = 1 GHz.

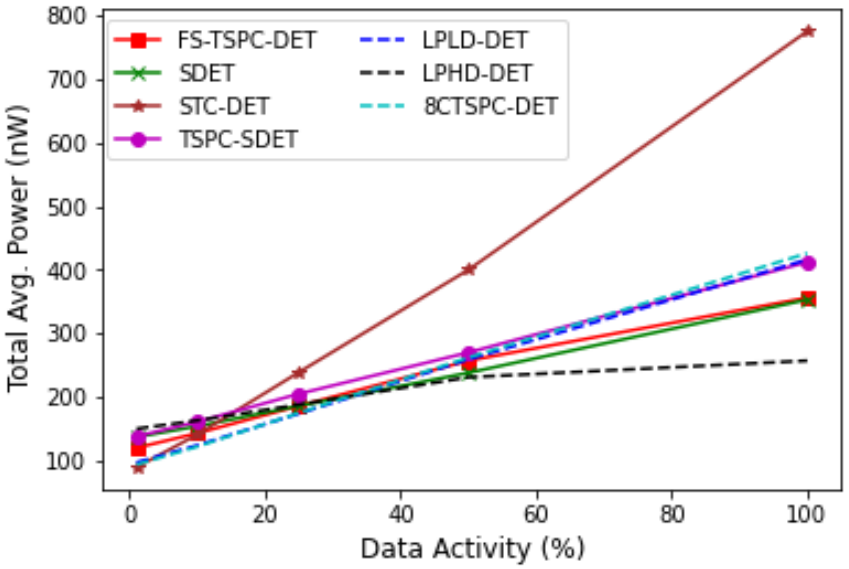


Figure 6.11: Total Average Power Versus DA at VDD = 0.5 V, CK = 50 MHz.

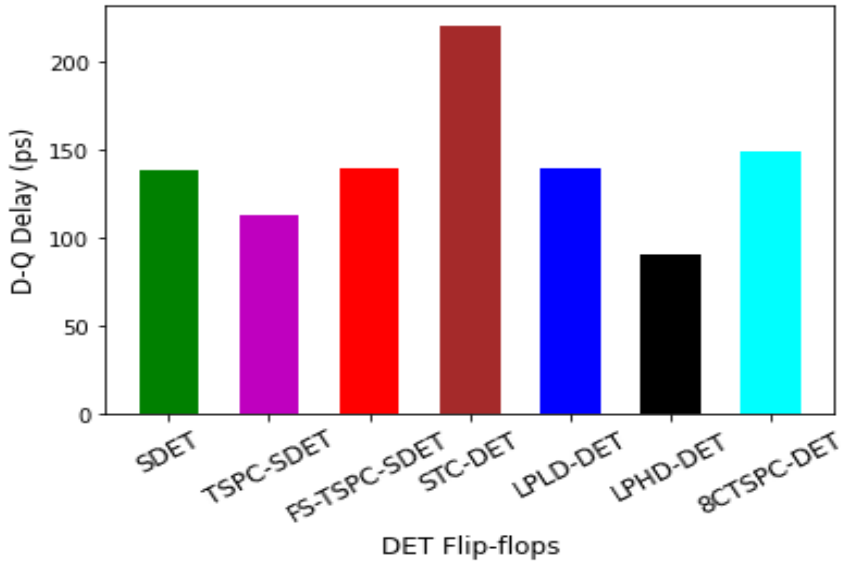


Figure 6.12: Worst-case D-Q Delay at VDD = 1 V, CK = 1 GHz.

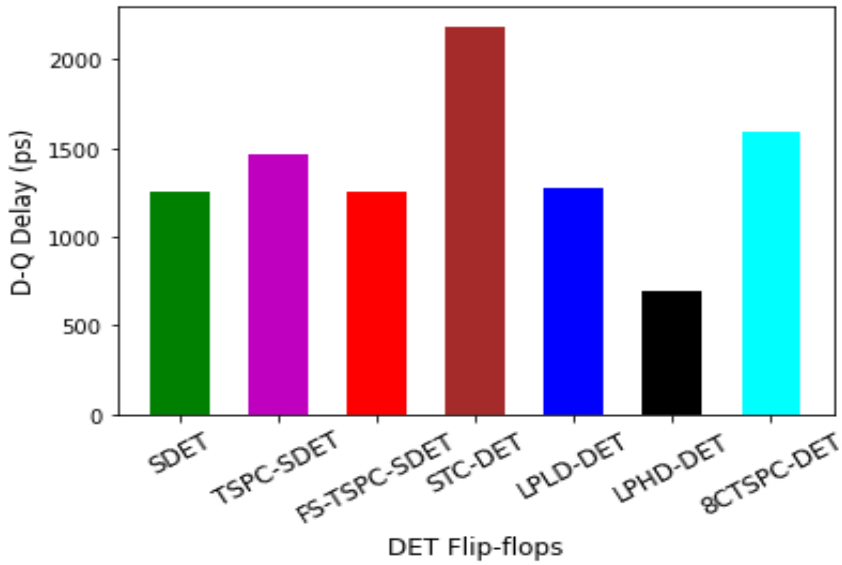


Figure 6.13: Worst-case D-Q Delay at VDD = 0.5 V, CK = 50 MHz.

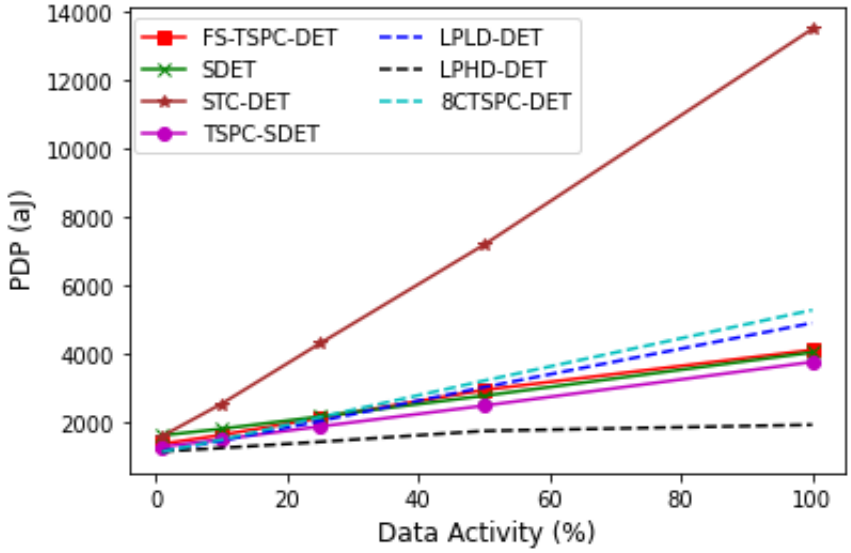


Figure 6.14: PDP Versus DA at VDD = 1 V, CK = 1 GHz.

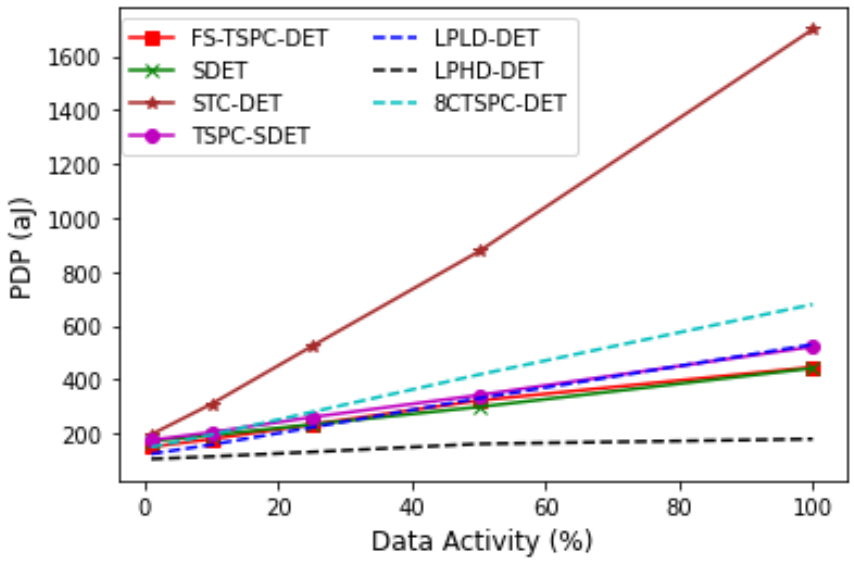


Figure 6.15: PDP Versus DA at VDD = 0.5 V, CK = 50 MHz.

Table 6.1: Overall Comparison Of All Considered DET Flip-flops.

Characteristic	Dual-edge Triggered Flip-flops						
	SDET [19]	TSPC-SDET [20]	FS-TSPC-DET [21]	STC-DET [22]	LPLD-DET [This work]	LPHD-DET [This work]	8CTSPC-DET [This work]
Type	Latch-MUX	Latch-MUX	Latch-MUX	Latch-MUX	**Latch-MUX**	**Latch-MUX**	**Latch-MUX**
Static	Yes	Yes	Yes	Yes	**Yes**	**Yes**	**Yes**
TSPC	No	Yes	Yes	Yes	**Yes**	**Yes**	**Yes**
Total Transistors/ Clock Count	26/16	38/12	36/10	42/8	**34/8**	**30/10**	**34/8**
Area (um^2)	9	12.6	12.24	15.48	**11.52**	**9.36**	**11.88**
Post-layout Simulation Results at VDD = 1 V, CK = 1 GHz, T= 25 °C, Corner = TT							
Setup time (ps)	12	51	12	63	**69**	**10**	**84**
Hold time (ps)	32	-44	52	-78	**-37**	**-36**	**-41**
C-Q Delay (ps)	126	62	127	158	**71**	**80**	**65**
D-Q Delay (ps)	138	113	139	221	**140**	**90**	**149**
Power (uW) @ DA 10%, 25%, 100%	13, 15.6, 29.2	13.1, 16.5, 33.2	11.6, 15.2. 29.5	11.4, 19.4, 61.1	**10.3, 14.4, 34.9**	**13.7, 15.2, 21.2**	**9.87, 14.3, 35.4**
PDP (aJ) @ DA 10%, 25%, 100%	1790, 2150, 4030	1480, 1860, 3750	1610, 2110, 4100	2520, 4290, 13500	**1440, 2020, 4890**	**1230, 1410, 1910**	**1470, 2130, 5270**
Post-layout Simulation Results at VDD = 0.5 V, CK = 50 MHz, T= 25 °C, Corner = TT							
Setup time (ps)	16	537	119	562	**600**	**163**	**746**
Hold time (ps)	189	374	66	403	**-245**	**-484**	**-472**
C-Q Delay (ps)	1236	930	1135	1626	**674**	**535**	**849**
D-Q Delay (ps)	1252	1467	1254	2188	**1274**	**698**	**1595**
Power (nW) @ DA 10%, 25%, 100%	154, 186, 353	161, 205, 412	143, 186, 356	141, 239, 775	**124, 174, 416**	**163, 188, 257**	**122, 175, 426**
PDP (aJ) @ DA 10%, 25%, 100%	176, 212, 402	204, 260, 522	179, 233, 446	309, 523, 1700	**158, 222, 530**	**114, 131, 179**	**195, 279, 679**

SDET at the nominal voltage. The D-Q delay of SDET, FS-TSPC-DET, and LPLD-DET are similar to each other. STC-DET has the longest D-Q delay, followed by 8CTSPC-DET.

Figure 6.14 and Figure 6.15 show the PDP of all considered DET FFs at VDD = 1 V, CK = 1 GHZ, and VDD = 0.5, CK = 50 MHz. As can be seen, the LPHD-DET is most energy-efficient amongst all considered DET FFs, regardless of the DA and voltage. For instance, at VDD = 1 V, and DA = 100%, the LPHD-DET consumes 65% and 73%, less energy compared to its closet DET FFs, TSPC-SDET and FS-TSPC-DET, respectively, in the comparison group. At nominal voltage, LPLD-DET and 8CTSPC-DET are the second and third most energy-efficient at low DAs around 15% compared to the other considered DET FFs. At low-voltage, LPLD-DET's energy-efficiency improves further, and it becomes the second most energy-efficient around 30% DAs compared to the other referenced DET FFs.

Table 6.1 makes an overall comparison of all considered latch-mux type dual-edge triggered flip-flops. The proposed 8CTSPC-DET, LPLD-DET, and LPHD-DET need only 8, 8, and 10 single-phase clock transistors, respectively. In terms of propagation delay, LPHD-DET is the fastest of all considered DET FFs , followed by TSPC-SDET, FS-TSPC-DET, and LPLD-DET. In terms of PDP, LPHD-DET is the most energy-efficient amongst all regardless of the DAs, and voltage. In terms of power, 8CTSPC-DET and LPLD-DET are the first and second most power-efficient FFs for low DAs, respectively, and LPHD-

DET is the most power-efficient for high DAs. Therefore, the proposed 8CTSPC-DET and LPLD-DET FFs are suitable for low-power and low DA applications, and LPHD-DET is for low-power high DAs, applications, including near-the-threshold voltage applications.

6.3 Summary

In this chapter, we propose three low-power, static, contention-free, latch-mux type TSPC DET FFs for near-the-threshold voltage applications. Post-layout simulation results in TSMC 65 nm CMOS technology show that the proposed FFs, 8CTSPC-DET, and LPLD-DET are suitable for low DA applications and each need 34 transistors, including 8 single-phase clock transistors. The proposed LPHD-DET is desirable for high DA applications and needs only 30 transistors, including 10 single-phase clock transistors.

Chapter 7

Conclusions

7.1 Major Contributions

Battery-operated systems require power- and energy-efficient circuits to extend their battery life. Registers or FFs are a basic component of digital circuits, and their power consumption and speed significantly impact the overall performance of a digital system. In a typical processor, there could be more than a million FFs. Therefore, there is a constant push to develop the new designs and circuits for registers to further enhance the power and energy-efficiency of FFs, and hence, digital systems. In this thesis, we have focused on exploring new low-power TSPC FFs designs with the fewer number of clock transistors. This approach not only reduces the power consumption of FFs, but also reduces power burden of the clock distribution network.

We initially investigated the TSPC single-edge triggered FFs. We have designed three low-power flip-flops with only two and three single-phase clock transistors. The post-layout simulation results show that the proposed TSPC single-edge triggered FFs are power-efficient for low DAs up to 30% compared to state-of-the-art TSPC SET FFs. To further validate the power-savings of these proposed FFs, we implemented five scan-chains of 256 FFs each, three for the proposed FFs, and two for the reference FFs - TGFF and 18TSPC, in TSMC 65 nm CMOS technology. Measurement results match the scan-chain post-layout simulation results.

The second major contribution is low-power and low-energy TSPC RHBD FFs. Many safety-critical applications like banking systems, autonomous cars, medical devices, servers, and aerospace, etc. require soft error tolerant and reliable designs, which should be power

Table 7.1: Major Contributions

Year	Article	Publisher	Title	Authors	Status
2024	Patent	US Patent	Low-power and Radiation Hardened Flip-flops	Manoj Sachdev, Yugal Maheshwari	Filed
2024	Journal	Elsevier Integration	VLFF—A very low-power flip-flop with only two clock transistors	Yugal Kishore Maheshwari, Manoj Sachdev	Published
2024	Journal	Elsevier Microelectronics	A power-efficient, single-phase, contention-free flip-flop with only three clock transistors	Yugal Kishore Maheshwari, Manoj Sachdev	Published
2023	Conference	IEEE SOCC	VLFF—A very low-power flip-flop with only two clock transistors	Yugal Kishore Maheshwari, Manoj Sachdev	Published
2021	Conference	IEEE ICECS	Ultra Low-power, Low-energy Static Single-phase Clocked Flip-flop	Yugal Maheshwari, Kleber Stangherlin, Derek Wright, Manoj Sachdev	Published

and energy efficient. However, the power and energy overhead of existing RHBD FFs is substantial compared to the conventional data flip-flop. A typical master slave RHBD flip-flop needs 10 or more clock transistors for it to work. In this work, we presented two TSPC RHBD FFs, referred to as TSPC-DICE, and TSPC-Quatro, that reduce the number of clock transistors to four and five, respectively. These FFs consume lower power and energy costs compared to all investigated RHBD FFs while maintaining a desirable Soft Error Rate (SER). To further validate the power-savings of the proposed FFs, and their radiation immunity, three scan-chains of 4200 FFs each are implemented for regular DFF, the proposed TSPC-DICE and TSPC-Quatro flip-flops. Test-chip designed in TSMC 65 nm technology measurement results highlight that TSPC-DICE and TSPC-Quatro scan-chains show power-efficiency over the regular DFF scan-chain for the DAs around 35% or lower. The proposed RHBD FFs are the first of its kind with a true single-phase clock with only four and five clock transistors with a total of 35 and 34 transistors, respectively.

Another significant contribution of this thesis is the proposed very low-power latch-mux type TSPC DET FFs for low and high data activities, referred to as LPLD-DET, LPHD-DET, and 8CTSPC-DET. Post-layout simulation results in TSMC 65 nm technology show that the proposed LPLD-DET and 8CTSPC-DET are suitable for low DAs up to 30%, and LPHD-DET for higher DAs from 45% for low-power applications, including the IoT and battery-operated low-voltage applications.

Table 7.1 illustrates the publications coming out of the research described in this the-

sis in various international conferences, journals, and patent. For example, the proposed 19TSPC flip-flop (referred to as "VLFF") is published in the IEEE SOCC-2023 conference [86], followed by an extended journal version in Elsevier Integration in 2024 in [78]. The proposed 21TSPC flip-flop (referred to as "3CTSPC") is published in the Elsevier Microelectronics journal in 2024 in [80]. We have also filed a US final patent in August 2024, followed by a provisional patent, which was submitted in August 2023 with the title "Low-power and Radiation Hardened Flip-flops".

7.2 Future Work

To further expand the scope of this research conducted in this thesis, there are several areas that can be explored in all three aspects discussed. For example, all the proposed FFs could be used in the hardware security applications to address side-channel power attacks. Since the number of clock transistors is reduced in the proposed FFs, thus, there would be a substantial change in the overall power consumption of the hardware security circuits or digital systems such as address encryption engines. Thus, it will reduce the risk of side-channel power attacks.

Furthermore, RHBD FFs can be explored in safety-critical applications such as autonomous cars, banking systems, servers, aerospace, healthcare equipment, etc. to reduce the power, energy, and area cost of the digital circuits and systems while maintaining the same features. The test-chip we have designed for RHBD FFs will go under neutron radiation testing in summer 2025 once we get our scheduled space in TRIUMF Lab, Vancouver, BC, Canada.

References

[1] "2021 executive summary. https://irds.ieee.org/images/files/pdf/2021/2021irds_es.pdf."

[2] G. C. Messenger, M. S. Ash, G. C. Messenger, and M. S. Ash, *Single event phenomena I.* Springer, 1997.

[3] B. Matush, *An Innovative Radiation Hardened By Design Flip-Flop.* Arizona State University, 2010.

[4] F. Wang and V. D. Agrawal, "Single event upset: An embedded tutorial," in *21st International Conference on VLSI Design (VLSID 2008)*, pp. 429–434, IEEE, 2008.

[5] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *1996 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, ISSCC*, pp. 138–139, IEEE, 1996.

[6] F. Klass, "Semi-dynamic and dynamic flip-flops with embedded logic," in *1998 Symposium on VLSI Circuits. Digest of Technical Papers (Cat. No. 98CH36215)*, pp. 108–109, IEEE, 1998.

[7] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Comparative analysis of double-edge versus single-edge triggered clocked storage elements," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No. 02CH37353)*, vol. 5, pp. V–V, IEEE, 2002.

[8] N. H. Weste and D. Harris, *CMOS VLSI design: a circuits and systems perspective.* Pearson Education India, 2015.

[9] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolić, *Digital integrated circuits: a design perspective*, vol. 7. Pearson Education Upper Saddle River, NJ, 2003.

[10] Y. K. Maheshwari, "A comparative analysis for low-voltage, low-power, and low-energy flip-flops," Master's thesis, University of Waterloo, 2020.

[11] J. Samandari-Rad and R. Hughey, "Power/energy minimization techniques for variability-aware high-performance 16-nm 6t-sram," *IEEE Access*, vol. 4, pp. 594–613, 2016.

[12] C. K. Teh, T. Fujita, H. Hara, and M. Hamada, "A 77% energy-saving 22-transistor single-phase-clocking d-flip-flop with adaptive-coupling configuration in 40nm cmos," in *2011 IEEE International Solid-State Circuits Conference*, pp. 338–340, IEEE, 2011.

[13] Y. Kim, W. Jung, I. Lee, Q. Dong, M. Henry, D. Sylvester, and D. Blaauw, "A static contention-free single-phase-clocked 24t flip-flop in 45nm for low-power applications," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 466–467, IEEE, 2014.

[14] N. Kawai, S. Takayama, J. Masumi, N. Kikuchi, Y. Itoh, K. Ogawa, A. Ugawa, H. Suzuki, and Y. Tanaka, "A fully static topologically-compressed 21-transistor flip-flop with 75% power saving," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2526–2533, 2014.

[15] F. Stas and D. Bol, "A 0.4-v 0.66-fj/cycle retentive true-single-phase-clock 18t flip-flop in 28-nm fully-depleted soi cmos," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 3, pp. 935–945, 2017.

[16] Y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell, and T. J. Kazmierski, "Ultra-low power 18-transistor fully static contention-free single-phase clocked flip-flop in 65-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 550–559, 2018.

[17] A. Khorami, M. Sachdev, and M. Sharifkhani, "A contention-free, static, single-phase flip-flop for low data activity applications," in *2019 32nd IEEE International System-on-Chip Conference (SOCC)*.

[18] G. Shin, E. Lee, J. Lee, Y. Lee, and Y. Lee, "An ultra-low-power fully-static contention-free flip-flop with complete redundant clock transition and transistor elimination," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 10, pp. 3039–3048, 2021.

[19] R. Hossain, L. D. Wronski, and A. Albicki, "Low power design using double edge triggered flip-flops," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 2, no. 2, pp. 261–265, 1994.

[20] A. Bonetti, A. Teman, and A. Burg, "An overlap-contention free true-single-phase clock dual-edge-triggered flip-flop," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1850–1853, IEEE, 2015.

[21] Y. Lee, G. Shin, and Y. Lee, "A fully static true-single-phase-clocked dual-edge-triggered flip-flop for near-threshold voltage operation in iot applications," *IEEE Access*, vol. 8, pp. 40232–40245, 2020.

[22] Z. Wang, P. Zhao, T. Springer, C. Zhu, J. Mau, A. Wells, Y. Xia, and L. Wang, "Low-power redundant-transition-free tspc dual-edge-triggering flip-flop using single-transistor-clocked buffer," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 31, no. 5, pp. 706–710, 2023.

[23] T. Hoang, J. Ross, S. Doyle, D. Rea, E. Chan, W. Neiderer, and A. Bumgarner, "A radiation hardened 16-mb sram for space applications," in *2007 IEEE Aerospace Conference*, pp. 1–6, IEEE, 2007.

[24] K. J. Hass, G. W. Donohoe, Y.-K. Hong, and B. C. Choi, "Magnetic flip flops for space applications," *IEEE transactions on magnetics*, vol. 42, no. 10, pp. 2751–2753, 2006.

[25] R. E. Lyons and W. Vanderkulk, "The use of triple-modular redundancy to improve computer reliability," *IBM journal of research and development*, vol. 6, no. 2, pp. 200–209, 1962.

[26] O. Schrape, M. Andjelković, A. Breitenreiter, S. Zeidler, A. Balashov, and M. Krstić, "Design and evaluation of radiation-hardened standard cell flip-flops," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 11, pp. 4796–4809, 2021.

[27] J. E. Knudsen and L. T. Clark, "An area and power efficient radiation hardened by design flip-flop," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3392–3399, 2006.

[28] R. Shuler, A. Balasubramanian, B. Narasimham, B. Bhuva, P. O'Neill, and C. Kouba, "The effectiveness of tag or guard-gates in set suppression using delay and dual-rail

configurations at 0.35 μm," *IEEE transactions on nuclear science*, vol. 53, no. 6, pp. 3428–3431, 2006.

[29] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron cmos technology," *IEEE Transactions on nuclear science*, vol. 43, no. 6, pp. 2874–2878, 1996.

[30] R. L. Shuler, C. Kouba, and P. M. O'Neill, "Seu performance of tag based flip-flops," *IEEE transactions on nuclear science*, vol. 52, no. 6, pp. 2550–2553, 2005.

[31] S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10t sram bit-cell with differential read capability," *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3768–3773, 2009.

[32] D. Rennie, D. Li, M. Sachdev, B. L. Bhuva, S. Jagannathan, S. Wen, and R. Wong, "Performance, metastability, and soft-error robustness trade-offs for flip-flops in 40 nm cmos," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 8, pp. 1626–1634, 2012.

[33] D. J. Rennie and M. Sachdev, "Novel soft error robust flip-flops in 65nm cmos," *IEEE Transactions on Nuclear Science*, vol. 58, no. 5, pp. 2470–2476, 2011.

[34] Y.-Q. Li, H.-B. Wang, R. Liu, L. Chen, I. Nofal, S.-T. Shi, A.-L. He, G. Guo, S. Baeg, S.-J. Wen, *et al.*, "A quatro-based 65-nm flip-flop circuit for soft-error resilience," *IEEE Transactions on Nuclear Science*, vol. 64, no. 6, pp. 1554–1561, 2017.

[35] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer mosfet design," *IEEE Transactions on Electron Devices*, vol. 31, no. 4, pp. 452–462, 1984.

[36] G. E. Moore *et al.*, "Progress in digital integrated electronics," in *Electron devices meeting*, vol. 21, pp. 11–13, Washington, DC, 1975.

[37] "https://www.statista.com/statistics/471264/iot-number-of-connected-devices-worldwide/."

[38] A. Hirata, K. Nakanishi, M. Nozoe, and A. Miyoshi, "The cross charge-control flip-flop: A low-power and high-speed flip-flop suitable for mobile application socs," in *Digest of Technical Papers. 2005 Symposium on VLSI Circuits, 2005.*, pp. 306–307, IEEE, 2005.

[39] S.-Y. Peng, T.-C. Huang, Y.-H. Lee, C.-C. Chiu, K.-H. Chen, Y.-H. Lin, C.-C. Lee, T.-Y. Tsai, C.-C. Huang, L.-D. Chen, *et al.*, "Instruction-cycle-based dynamic voltage scaling power management for low-power digital signal processor with 53% power savings," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 11, pp. 2649–2661, 2013.

[40] J. P. Cerqueira, T. J. Repetti, Y. Pu, S. Priyadarshi, M. A. Kim, and M. Seok, "Catena: A near-threshold, sub-0.4-mw, 16-core programmable spatial array accelerator for the ultralow-power mobile and embedded internet of things," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 8, pp. 2270–2284, 2020.

[41] T. Tekeste, H. Saleh, B. Mohammad, and M. Ismail, "Ultra-low power qrs detection and ecg compression architecture for iot healthcare devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 2, pp. 669–679, 2018.

[42] A. Pullini, D. Rossi, I. Loi, G. Tagliavini, and L. Benini, "Mr. wolf: An energy-precision scalable parallel ultra low power soc for iot edge processing," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 7, pp. 1970–1981, 2019.

[43] T. Tekeste, H. Saleh, B. Mohammad, A. Khandoker, and M. Ismail, "A nano-watt ecg feature extraction engine in 65-nm technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 8, pp. 1099–1103, 2017.

[44] K. Mohammad, T. Tekeste, B. Mohammad, H. Saleh, and M. Qurran, "Embedded memory options for ultra-low power iot devices," *Microelectronics Journal*, vol. 93, p. 104634, 2019.

[45] J. Shen, L. Geng, G. Xiang, and J. Liang, "Low-power level converting flip-flop with a conditional clock technique in dual supply systems," *Microelectronics journal*, vol. 45, no. 7, pp. 857–863, 2014.

[46] B. Joo and B.-S. Kong, "Low-power high-speed sense-amplifier-based flip-flops with conditional bridging," *IEEE Access*, 2023.

[47] M. Hamada, H. Hara, T. Fujita, C. K. Teh, T. Shimazawa, N. Kawabe, T. Kitahara, Y. Kikuchi, T. Nishikawa, M. Takahashi, *et al.*, "A conditional clocking flip-flop for low power h. 264/mpeg-4 audio/visual codec lsi," in *Proceedings of the IEEE 2005 Custom Integrated Circuits Conference, 2005.*, pp. 527–530, IEEE, 2005.

[48] K. Absel, L. Manuel, and R. Kavitha, "Low-power dual dynamic node pulsed hybrid flip-flop featuring efficient embedded logic," *IEEE transactions on very large scale integration (vlsi) systems*, vol. 21, no. 9, pp. 1693–1704, 2012.

[49] B.-S. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, 2001.

[50] F. Safipoor, R. F. Mirzaee, and M. Zare, "High-performance quaternary latch and d-type flip-flop with selective outputs," *Microelectronics Journal*, vol. 113, p. 105079, 2021.

[51] A. Karimi, A. Rezai, and M. M. Hajhashemkhani, "A novel design for ultra-low power pulse-triggered d-flip-flop with optimized leakage power," *Integration*, vol. 60, pp. 160–166, 2018.

[52] J. L. Shin, R. Golla, H. Li, S. Dash, Y. Choi, A. Smith, H. Sathianathan, M. Joshi, H. Park, M. Elgebaly, *et al.*, "The next generation 64b sparc core in a t4 soc processor," *IEEE journal of solid-state circuits*, vol. 48, no. 1, pp. 82–90, 2012.

[53] S. Hsu, A. Agarwal, S. Realov, M. Anders, G. Chen, M. Kar, R. Kumar, H. Sumbul, P. Knag, H. Kaul, V. Suresh, S. Mathew, I. Rajwani, S. Damaraju, R. Krishnamurthy, and V. De, "Low-clock-power digital standard cell ips for high-performance graphics/ai processors in 10nm cmos," in *2020 IEEE Symposium on VLSI Circuits*, pp. 1–2, 2020.

[54] M. Asyaei and A. Peiravi, "Low power wide gates for modern power efficient processors," *Integration*, vol. 47, no. 2, pp. 272–283, 2014.

[55] S. Purohit, M. Lanuzza, S. Perri, P. Corsonello, and M. Margala, "Design and evaluation of an energy-delay-area efficient datapath for coarse-grain reconfigurable computing systems," *Journal of Low Power Electronics*, vol. 5, no. 3, pp. 326–338, 2009.

[56] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (rcsff) for 63% power reduction," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 807–811, 1998.

[57] M. Alioto, E. Consoli, and G. Palumbo, "Flip-flop energy/performance versus clock slope and impact on the clock network design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 6, pp. 1273–1286, 2009.

[58] N. Nedovic and V. G. Oklobdzija, "Dual-edge triggered storage elements and clocking strategy for low-power systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 5, pp. 577–590, 2005.

[59] A. Cantoni, J. Walker, and T.-D. Tomlin, "Characterization of a flip-flop metastability measurement method," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 5, pp. 1032–1040, 2007.

[60] E. Mahmoodi and M. Gholipour, "Design space exploration of low-power flip-flops in finfet technology," *Integration*, vol. 75, pp. 52–62, 2020.

[61] R. Murugasami and U. Ragupathy, "Performance analysis of clock pulse generators and design of low power area efficient shift register using multiplexer based clock pulse generator," *Microelectronics Journal*, vol. 105, p. 104891, 2020.

[62] Y. Ueda, H. Yamauchi, M. Mukuno, S. Furuichi, M. Fujisawa, F. Qiao, and H. Yang, "6.33 mw mpeg audio decoding on a multimedia processor," in *2006 IEEE International Solid State Circuits Conference-Digest of Technical Papers*, pp. 1636–1645, IEEE, 2006.

[63] S. Kumar, S. Sharma, and B. Kaur, "Leakage power estimation for iscas c17 benchmark circuit," in *2019 6th International Conference on Computing for Sustainable Global Development (INDIACom)*, pp. 108–112, 2019.

[64] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional pre-charge techniques for power-efficient dual-edge clocking," in *Proceedings of the 2002 international symposium on Low power electronics and design*, pp. 56–59, 2002.

[65] M. W. Phyu, K. Fu, W. L. Goh, and K.-S. Yeo, "Power-efficient explicit-pulsed dual-edge triggered sense-amplifier flip-flops," *IEEE transactions on very large scale integration (vlsi) systems*, vol. 19, no. 1, pp. 1–9, 2009.

[66] S. V. Devarapalli, P. Zarkesh-Ha, and S. C. Suddarth, "A robust and low power dual data rate (ddr) flip-flop using c-elements," in *2010 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 147–150, IEEE, 2010.

[67] S. Lapshev and S. R. Hasan, "New low glitch and low power det flip-flops using multiple c-elements," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 10, pp. 1673–1681, 2016.

[68] J. Slaughter, E. Chen, R. Whig, B. Engel, J. Janesky, and S. Tehrani, "Magnetic tunnel junction materials for electronic applications," *JOM(USA)*, vol. 52, no. 6, p. 11, 2000.

[69] S. J. Kim, D. Im, C. Kim, and C. Yoon, "Thermal stability of magnetic tunnel junctions with feo/sub x/doped tunnel barrier," *IEEE transactions on magnetics*, vol. 40, no. 4, pp. 2284–2286, 2004.

[70] H. Zhengfeng and L. Huaguo, "A novel radiation hardened by design latch," *Journal of Semiconductors*, vol. 30, no. 3, p. 035007, 2009.

[71] T. A. Fjeldly, Y. Deng, M. S. Shur, H. P. Hjalmarson, A. Muyshondt, and T. Ytterdal, "Modeling of high-dose-rate transient ionizing radiation effects in bipolar devices," *IEEE Transactions on Nuclear Science*, vol. 48, no. 5, pp. 1721–1730, 2001.

[72] D. Krueger, E. Francom, and J. Langsdorf, "Circuit design for voltage scaling and ser immunity on a quad-core itanium® processor," in *2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*, pp. 94–95, IEEE, 2008.

[73] T. Singh, A. Schaefer, S. Rangarajan, D. John, C. Henrion, R. Schreiber, M. Rodriguez, S. Kosonocky, S. Naffziger, and A. Novak, "Zen: An energy-efficient high-performance × 86 core," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 102–114, 2018.

[74] E. Korczynski, "Iot demands: Are we ready?," *Solid State Technology*, vol. 59, no. 4, pp. 19–23, 2016.

[75] N. Lotze and Y. Manoli, "Ultra-sub-threshold operation of always-on digital circuits for iot applications by use of schmitt trigger gates," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 11, pp. 2920–2933, 2017.

[76] D. Pan, C. Ma, L. Cheng, and H. Min, "A highly efficient conditional feedthrough pulsed flip-flop for high-speed applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 1, pp. 243–251, 2019.

[77] L. Moreau, R. Dekimpe, and D. Bol, "A 0.4 v 0.5 fj/cycle tspc flip-flop in 65nm lp cmos with retention mode controlled by clock-gating cells," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, IEEE, 2019.

[78] Y. K. Maheshwari and M. Sachdev, "Vlff—a very low-power flip-flop with only two clock transistors," *Integration*, vol. 100, p. 102300, 2024.

[79] P. Zhao, J. McNeely, P. Golconda, M. A. Bayoumi, R. A. Barcenas, and W. Kuang, "Low-power clock branch sharing double-edge triggered flip-flop," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 15, no. 3, pp. 338–345, 2007.

[80] Y. K. Maheshwari and M. Sachdev, "A power-efficient, single-phase, contention-free flip-flop with only three clock transistors," *Microelectronics Journal*, vol. 152, p. 106390, 2024.

[81] S. Hsu, A. Agarwal, S. Realov, M. Anders, G. Chen, M. Kar, R. Kumar, H. Sumbul, P. Knag, H. Kaul, *et al.*, "Low-clock-power digital standard cell ips for high-performance graphics/ai processors in 10nm cmos," in *2020 IEEE Symposium on VLSI Circuits*, pp. 1–2, IEEE, 2020.

[82] J.-F. Lin, M.-H. Sheu, Y.-T. Hwang, C.-S. Wong, and M.-Y. Tsai, "Low-power 19-transistor true single-phase clocking flip-flop design based on logic structure reduction schemes," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 25, no. 11, pp. 3033–3044, 2017.

[83] V. G. Oklobdzija, V. M. Stojanovic, D. M. Markovic, and N. M. Nedovic, *Digital system clocking: high-performance and low-power aspects*. John Wiley & Sons, 2005.

[84] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital integrated circuits*, vol. 2. Prentice hall Englewood Cliffs, 2002.

[85] Y. Maheshwari, K. Stangherlin, D. Wright, and M. Sachdev, "Ultra low-power, low-energy static single-phase clocked flip-flop," in *2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, pp. 1–4, IEEE, 2021.

[86] Y. Maheshwari and M. Sachdev, "Vlff - a very low-power flip-flop with only two clock transistors," in *2023 IEEE 36th International System-on-Chip Conference (SOCC)*, pp. 1–6, 2023.

[87] D. E. S. NIST, "Advanced encryption standard (aes)(fips–197)," *National Institute of Standards and Technology*, 2001.

[88] P. Hamalainen, T. Alho, M. Hannikainen, and T. D. Hamalainen, "Design and implementation of low-area and low-power aes encryption hardware core," in *9th EUROMICRO conference on digital system design (DSD'06)*, pp. 577–583, IEEE, 2006.

[89] T. Karnik and P. Hazucha, "Characterization of soft errors caused by single event upsets in cmos processes," *IEEE Transactions on Dependable and secure Computing*, vol. 1, no. 2, pp. 128–143, 2004.

[90] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Transactions on nuclear Science*, vol. 50, no. 3, pp. 583–602, 2003.

[91] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Transactions on Device and materials reliability*, vol. 5, no. 3, pp. 305–316, 2005.

[92] J. Guo, L. Zhu, Y. Sun, H. Cao, H. Huang, T. Wang, C. Qi, R. Zhang, X. Cao, L. Xiao, *et al.*, "Design of area-efficient and highly reliable rhbd 10t memory cell for aerospace applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 5, pp. 991–994, 2018.

[93] A. Jain, A. M. Veggetti, D. Crippa, A. Benfante, S. Gerardin, and M. Bagatin, "Radiation tolerant multi-bit flip-flop system with embedded timing pre-error sensing," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 9, pp. 2878–2890, 2022.

[94] E. Ibe, H. Taniguchi, Y. Yahagi, K.-i. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in srams from a 250 nm to a 22 nm design rule," *IEEE Transactions on Electron Devices*, vol. 57, no. 7, pp. 1527–1538, 2010.

[95] R. Giterman, L. Atias, and A. Teman, "Area and energy-efficient complementary dual-modular redundancy dynamic memory for space applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 2, pp. 502–509, 2016.

[96] R. Bishnoi, F. Oboril, and M. B. Tahoori, "Design of defect and fault-tolerant nonvolatile spintronic flip-flops," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 4, pp. 1421–1432, 2016.

[97] S. Pal, W.-H. Ki, and C.-Y. Tsui, "Soft-error-aware read-stability-enhanced low-power 12t sram with multi-node upset recoverability for aerospace applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 4, pp. 1560–1570, 2022.

[98] J. Yuan and C. Svensson, "High-speed cmos circuit technique," *IEEE journal of solid-state circuits*, vol. 24, no. 1, pp. 62–70, 1989.

[99] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered & dual edge-triggered pulsed flip-flops for

high-performance microprocessors," in *Proceedings of the 2001 international symposium on Low power electronics and design*, pp. 147–152, 2001.

[100] A. G. Strollo, E. Napoli, and C. Cimino, "Analysis of power dissipation in double edge-triggered flip-flops," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 5, pp. 624–629, 2000.

[101] D. Henriquez, "High performance spaceflight computing (hpsc)," 2016.

[102] S. Whitaker, J. Canaris, and K. Liu, "Seu hardened memory cells for a ccsds reed-solomon encoder," *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, pp. 1471–1477, 1991.

APPENDICES

Appendix A

Verilog Code for the Double Exponential Current Equation

A.1 Dobule Exponential Current Equation in Virtuoso

```
‘include "constants.vams"
‘include "disciplines.vams"

module SEU_Current(P, N, Qcoll, ta_coeff);


input Qcoll, ta_coeff; // variable parameters
output P, N;
electrical Qcoll, ta_coeff, P, N;
//Defining real parameters
parameter real TA= 1.0E-12; // tau alpha or falling time (ps)
parameter real TB= 50.0E-12; // tau beta or rise time (ps)
parameter real DELAYTIME =12.2E-9; // delay constant (ns)
analog
 if($abstime < DELAYTIME)
 I(P,N) <+ 0;
 else
 I(P,N) <+ (V(Qcoll)/((TA*V(ta_coeff)) - TB)) * (exp(-1*($abstime -
```

```
DELAYTIME)/(TA*V(ta_coeff))) - exp(-1*($abstime - DELAYTIME)/TB));

endmodule
```

Glossary

microprocessor (CPU) A programmable machine that receives input data, stores and manipulates the data, and provides formatted output 1

soft error A soft error is a temporary malfunction in a semiconductor or memory chip that occurs when a signal or data is incorrect. Soft errors are caused by external factors, such as radiation, and do not damage the semiconductor itself. 3, 8, 65, 70, 71, 73, 75, 78, 98