

High-Q On-chip Passive Components and Low-Phase-Noise CMOS Bridge Oscillator Design

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

High-Q passives are the key design components for a proposed resonator circuit. This thesis focuses on designing and optimizing passive components (transmission lines, capacitors, and inductors) implemented in a production 22-nm SOI-CMOS technology. Custom-designed inductors with inductances of 1 nH and 2 nH are employed, achieving quality factors (Q) greater than 30 at 10 GHz. These inductors are realized through the utilization of BEOL Stack 11 and Stack 19 configurations in the 22-nm technology with varying shielding patterns. Additionally, high-Q capacitors are implemented exhibiting Q factors surpassing 500 at 10 GHz, and an operational range validated by measurements up to 60 GHz. Balanced transmission lines with Q factor greater than 150 at 25 GHz are also designed and implemented. This high-Q value is explained with a new lumped-element equivalent circuit model developed in this work.

A state-of-the-art, fully-integrated bridge resonator with a quality factor (Q) exceeding 50 at 8.5 GHz is introduced in this thesis. This level of performance is realized through circuit design techniques and the integration of the custom inductor and capacitor designs. Furthermore, the potential for application of this high-Q bridge resonator in the design of a low-phase-noise RF oscillator is demonstrated, with post-layout simulations predicting a phase noise below -131 dBc/Hz at 1 MHz offset for 8-GHz carrier frequency.

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Last but not the least, I would like to acknowledge my family and friends, for their love and unwavering support throughout my academic journey. Their encouragement and belief in me have been a constant source of motivation.

Thank you all.

Dedication

I dedicate this thesis to my loving family, whose unconditional love and support have been the cornerstone of my success. To my husband, Anjoom, your strong belief in me has inspired me to strive for excellence. I could not have come this far without your constant support and encouragement. Thank you for your patience, understanding, and belief in me, even during the most challenging times. And to our precious future child, though you have yet to arrive, you are already the greatest motivation for my hard work, pursuit of knowledge and success. To my parents, your sacrifices and constant encouragement have shaped me into the person I am today. I am forever grateful for their guidance, love, and encouragement.

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Chapter 1

Introduction

Oscillators play a vital role in determining the overall performance of advanced data transceivers. A key component in frequency reference generators, oscillators ensure the accuracy, stability, and synchronization of electronic systems across a wide range of applications, spanning from consumer electronics (e.g., computers, signal generators, audio equipment) to critical infrastructure (e.g., medical devices, navigation systems, defense, etc.) [1].

Oscillators are characterized primarily by their phase noise, frequency tuning range, and output power level specifications. Phase noise is a measure of frequency stability, and refers to short-term random fluctuations in frequency or phase. In many systems, the oscillator characteristics set the performance and accuracy limits of the system. In a data transceiver, for example, phase noise can affect data modulation and bit-error rate (BER) performance of a communication link [2]. In a Doppler radar system, oscillator (carrier) noise reduces the ability of the system to detect slow moving targets [3] [4]. In a phase-locked loop (PLL), the output sees multiplication of the reference oscillator phase noise by a factor of $20 \log_{10}(N)$, in dB [5], where N is the multiplication factor. This can limit the maximum usable frequency of the synthesizer.

1.1 Motivations

The main motivation of this thesis is to develop high-Q passive components and resonator circuits for use in higher performance oscillators. The output frequency of these oscillators can range from a few GHz to hundreds of GHz, depending on the modulation scheme and communication standard (wireless or optical fibre). The theory of oscillator phase noise explained in Chapter 2 of this thesis, predicts that it is important to have a resonator comprised of high-quality-factor (Q-factor) passive components. In typical L-C oscillators, a resonator circuit is implemented using an inductor (L) and a capacitor (C) connected in parallel [6]. These

are low to medium Q (i.e., less than 20) on-chip resonators. High-Q resonators are typically built using off-chip components.

A bridge-oscillator with high-Q discrete crystal resonator was first reported by Meachem [7]. The Meachem's Bridge Oscillator (MBO) system was implemented using discrete components in a low-frequency oscillator, as shown in Fig. 1.1.

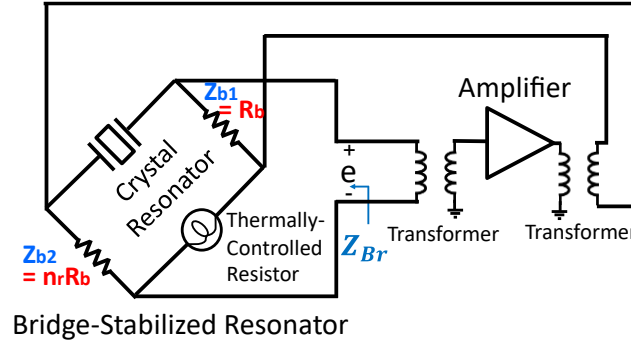


Fig. 1.1. Meachem's Bridge Stabilized Oscillator (MBO) [7]

The bridge is comprised of four arms, one of them incorporating a crystal resonator. Opposite the crystal is a thermally controlled resistive element, and impedances Z_{b1} and Z_{b2} comprise the bridge balancing arms. The 'balance point' (i.e., $|V_{out}| \rightarrow 0$, $\angle V_{out} = 0$) occurs when all four arms have equal impedances. If there is a difference between the impedances in the balancing arms, an output voltage is created. Meachem's bridge used two resistors with slightly different values (e.g., $Z_{b1} = R_b$ and $Z_{b2} = n_r R_b$, where n_r is a scaling constant) to output a small voltage amplitude and a rapid phase change at the resonant frequency of the crystal. The sharp narrowband response and 180° phase shift at balance gives the bridge resonator higher selectivity and Q-factor than a comparable series or parallel L-C resonator.

The demand for a compact, small-size, and low-cost design for commercial applications can be satisfied by monolithic integration. Compared to a simple series or parallel L-C resonator, a bridge resonator holds the potential for improved Q-factor and oscillator phase noise performance, thus forming the motivation behind this thesis. However, the MBO concept has received little attention from on-chip oscillator designers. Partially monolithic prototypes were

published that use the MBO topology in high-frequency oscillators [8] [9]. However, none of the reported designs are implemented on a single chip. Also, previous work has focused on off-chip, high-Q resonators (crystal, resonant cavity, etc.). The aim of this thesis is to develop a monolithic bridge resonator oscillator design with phase noise performance superior to current L-C oscillators in the GHz frequency range. All passive components, biasing and tuning networks must therefore be implemented on-chip to realize a fully integrated prototype. The target phase noise for this work is <-130 dBc/Hz at 1-MHz offset from an 8-GHz carrier.

A fully depleted silicon-on-insulator (FD-SOI) CMOS technology from GLOBALFOUNDRIES® [10] is used in this work to design and verify a prototype bridge resonator circuit and design a low-phase-noise oscillator. Shrinking the MOSFET channel length to 22 nm leads to a high gain-bandwidth product (f_T), which enables circuit implementations of millimetre-wave (mm-wave) frequencies. A buried oxide under the FET channel raises the well breakdown voltage, which permits integration of cascode amplifiers with output voltage swings beyond the 0.9 V supply. The capability to bias the back-gate of SOI transistors enables speed to be traded off with power consumption via the control of the threshold voltage [10].

1.2 Low-Phase-Noise Implementation with a Bridge Resonator

A simplified block diagram of the proposed oscillator is shown in Fig. 1.2. The circuit employs an on-chip bridge resonator and two amplifier stages in a closed loop. The bridge resonator offers the potential of higher selectivity and Q-factor to lower the oscillator phase-noise, as described in Section 1.4.2. Two stages of amplification are employed: a low-gain preamplifier first stage and a high-gain limiting amplifier second stage. The low-gain preamplifier improves the output signal-to-noise (SNR) ratio of the gain stages, and dominates phase noise performance.

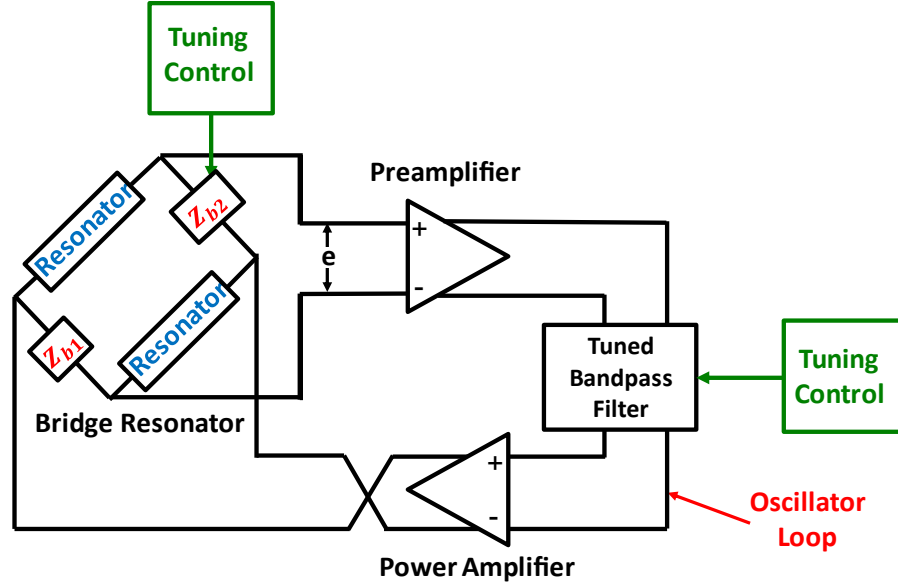


Fig. 1.2. Block diagram of the proposed IC bridge oscillator

1.3 Potential Applications

The proposed oscillator is a potential candidate for use in high-speed data networks. Global internet data traffic grew 100-fold in the past decade, and it is projected to reach 5000 exabytes/month by 2030 [11]. One cause of this enormous increase in data usage is the deployment of internet of things (IoT) devices. The demand for such high data rates is also driven by new services for 5th generation (5G) communication systems [12] [13]. In a 5G network, this growth implies a requirement for 1-10 Gb/s rates to wireless subscribers, 100 Gb/s in the wireless backhaul network, 1 Tb/s in a metropolitan-area network (MAN), and 1 Pb/s for the core data transport network [14].

Optical fibre, with its comparatively large bandwidth, is employed in inter- and intra-datacentre networks [14]. The high information carrying capacity (> 2 Pb/s) of fibre makes it the perfect choice for backhaul data transport. Fig. 1.3 illustrates a simplified network diagram for both wireless and optical fibre communication. Transceiver base stations (BTS) are connected to the network by optical fibres.

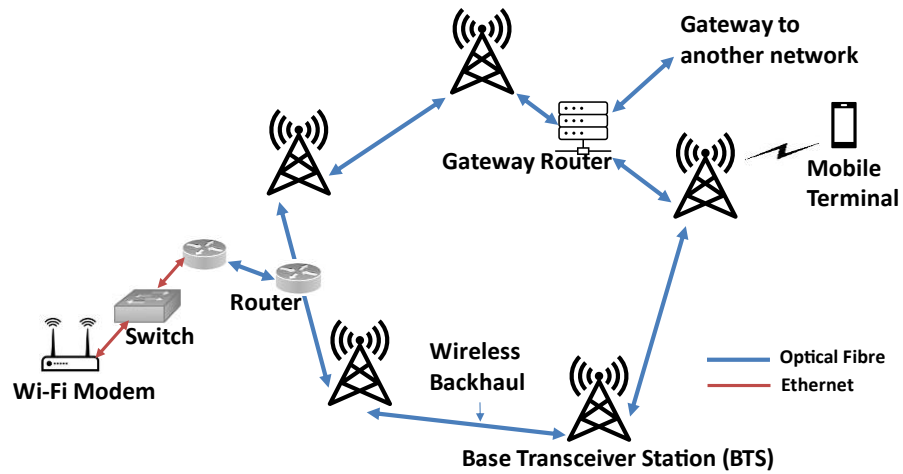


Fig. 1.3. Transceiver Basestation

Wireless sub-networks (e.g. Wi-Fi modems and mobile users) are connected to base stations through routers. The local network is connected to other networks through gateways as shown in Fig. 1.3. To support demand, systems capable of handling larger data throughputs are the subject of intense research and development. From a high-frequency circuits point of view, this has led a focus on wideband and low-noise analog interfaces. Fig. 1.4 shows the block diagram of an optical transmitter, which is typically located at the BTS (see Fig. 1.3).

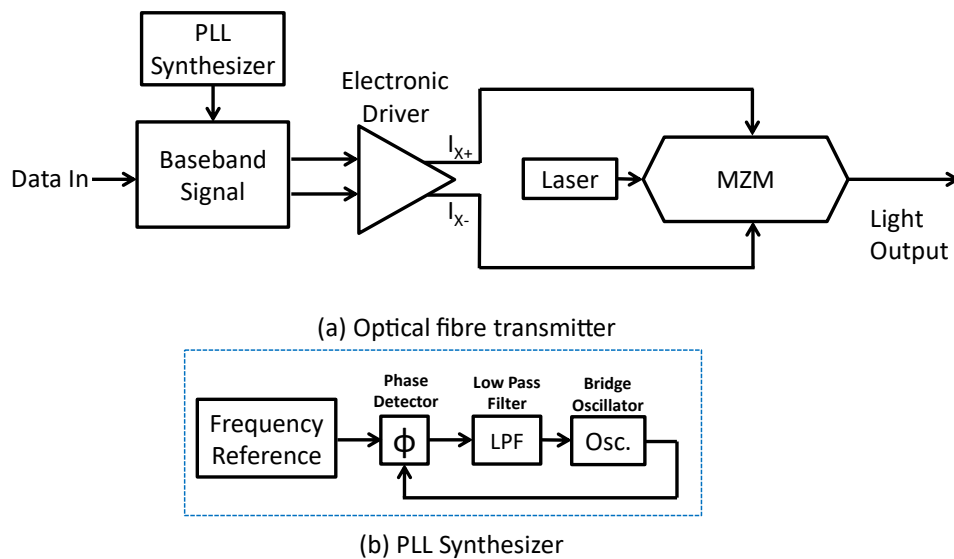


Fig. 1.4. Block diagram of an optical transmitter

It employs an optical modulator interfaced to an electronic driver (Fig. 1.4a) and a PLL synthesizer (Fig. 1.4b). The oscillator is a key high-frequency building block of every PLL frequency synthesizer (ref. Fig. 1.4b). The performance of the oscillator significantly affects the overall efficiency of the data network.

1.4 Design Objectives and Challenges

In this section, specifications of a low-phase-noise oscillator using a bridge resonator are described, and design specifications are linked to a simple phase-noise model.

1.4.1 Ultra-Low Phase Noise

Frequency stability of an oscillator is typically characterized by long- and short-term stability. Long-term frequency instability is commonly caused by temperature variations that modify the electrical parameters of various components, or by ageing of components in a system, particularly the resonator [15]. Temperature shifts often cause a gradual drift in the frequency of the output waveform. Short-term instability is caused by electronic noise within the system, and it results in phase (PM) and amplitude (AM) modulation of the output waveform. These modulations are a result of the additive noise from passive components in the oscillator, as well as the effects of low-frequency noise (e.g., 1/f noise) from active devices on the output carrier [16]. Therefore, short-term stability depends on the performance of the circuit. In a typical L-C oscillator, the output signal is limited in amplitude, and AM noise is negligible. The output signal ($V_o(t)$) of the oscillator is therefore, dominated by PM noise, which can be modelled as,

$$V_o(t) \cong A_{osc} \cos(\omega_{osc}t) + \frac{A_{osc}\varphi_p}{2} \left[\cos((\omega_{osc} - \omega_p)t) - \cos((\omega_{osc} + \omega_p)t) \right], \quad (1.1)$$

where $\omega_p t$ represents the random phase variation (PM noise), and φ_p is the modulation index [17]. Eq. (1.1) predicts that small phase or frequency changes in the output of the oscillator result in modulation side bands at frequencies $(\omega_{osc} + \omega_p)$ and $(\omega_{osc} - \omega_p)$. If the phase and

frequency deviations are the result of a random noise process, the frequency spectrum will take the form shown in Fig. 1.5.

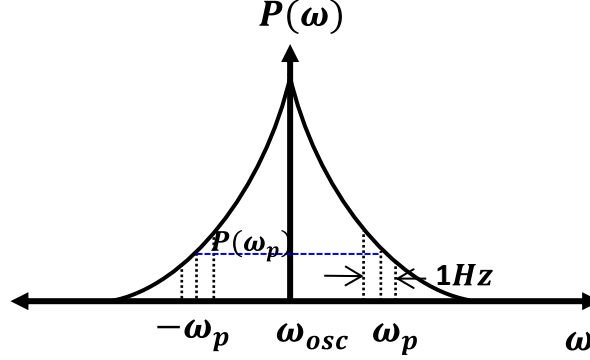


Fig. 1.5. Oscillator output power spectral density vs frequency (ω)

Phase noise $L(\omega_p)$ is defined as the ratio of the single side-band phase noise power in a 1-Hz bandwidth at a given offset frequency, ω_p , to the total carrier power.

1.4.1.1 Leeson's Phase Noise Model

Leeson [18] predicted that oscillator phase noise, $L(f_p)$, in the region where $L(f_p)$ is proportional to the square of offset frequency f_p :

$$L(f_p) = \frac{FkT\Delta f}{2P_{avg}} \left[1 + \left(\frac{f_{osc}}{2f_pQ_L} \right)^2 \right]. \quad (1.2)$$

In eq. (1.2), f_{osc} is the oscillation frequency, P_{avg} is the average carrier power, Q_L is the resonator's loaded quality factor, f_p is the offset frequency from carrier, k is Boltzmann's constant, T is absolute temperature, F is the amplifier noise factor (with respect to the resonator impedance at resonance), and Δf is the noise bandwidth (typically 1 Hz is assumed).

Eq. (1.2) predicts that Q_L is a key parameter for low-phase-noise designs. It is dependent on the electrical performance of the passive components in the resonator. The numerator $FkT\Delta f$ is driven by F , which cannot be calculated in a straightforward way. For example, Andreani [19] proposed an estimate for F of $4(1 + \gamma_n)$ for a cross-coupled L-C oscillator, where γ_n is

the channel noise factor of NMOS transistor. For long-channel devices, γ_n is 2/3 and $FkT\Delta f$ is -195.5 dB at room temperature (Δf is 1-Hz).

Leeson's equation also predicts that raising the carrier power lowers phase noise. For example, signal power P_{avg} for a class-A amplifier depends on the supply voltage (V_{DC}) and bias current (I_{DC}),

$$P_{avg} = V_{rms} \cdot I_{rms} = \frac{V_{DC}}{\sqrt{2}} \cdot \frac{I_{DC}}{\sqrt{2}}. \quad (1.3)$$

Power stages that produce greater P_{avg} are therefore very relevant to low-phase-noise design. To achieve a phase noise of -137 dBc/Hz at 1 MHz offset at 8-GHz, eq. (1.2) predicts that a Q_L of 20 and P_{avg} of 30 mW are required. This requires a supply voltage of at least 1.2 V with a bias current of 50 mA, when estimated from eq. (1.3). In summary, a high-Q resonator (i.e., $Q_L > 20$) and low-noise amplifier circuits (i.e., minimal 1/f noise, and $\frac{FkT\Delta f}{2P_{avg}} < -180$ dB) together can lead to a phase-noise performance better than -130 dBc/Hz as predicted from Leeson's formula.

1.4.2 High-Q Passives and Resonator

The resonator block of a simple L-C oscillator is typically comprised of an inductor (L) and a capacitor (C) in parallel [20]. To sustain oscillations, a voltage or current is injected into the resonator, and the inductive (X_L) and capacitive (X_C) reactances transfer energy back and forth at the resonant frequency,

$$\omega_{osc} = \frac{1}{\sqrt{LC}}. \quad (1.4)$$

In practice, there are energy losses present in the inductor and the capacitor. This loss is characterized by the quality factor (Q factor).

In the frequency response of the L-C resonator, the resonator Q factor at oscillation frequency determines the ratio of frequency (ω_{osc}) to bandwidth ($\Delta\omega$) [17].

$$Q(\omega \rightarrow \omega_{osc}) = \frac{\omega_{osc}}{\Delta\omega}. \quad (1.5)$$

A medium- to high-Q resonator (i.e., $Q_L > 20$ at oscillation frequency of 8 GHz) is comprised of low-loss L-C components, and is crucial to the design of low-phase-noise oscillators. This work targets designing inductors with Q greater than 30 and capacitors with Q better than 150 in the 22-nm FD-SOI CMOS technology.

The differential bridge resonator (ref. Fig. 1.2) designed in this thesis has four bridge arms, two of them comprised of L-C resonators, and the remaining two (i.e., Z_{b1} and Z_{b2}) are balancing arms. If there is an impedance imbalance between the balancing arms (i.e., $Z_{b1} \neq Z_{b2}$), an output voltage is created at the output of the resonator. The resonator impedance is inductive below resonance and capacitive at higher frequencies, with a 180-degree phase shift as the frequency passes through resonance. Also, a phase discontinuity is caused by the error voltage changing sign as the frequency passes through resonance. An example plot of gain and phase response of a bridge resonator is shown in Fig. 1.6 for a resonant frequency (ω_{osc}) of 8 GHz.

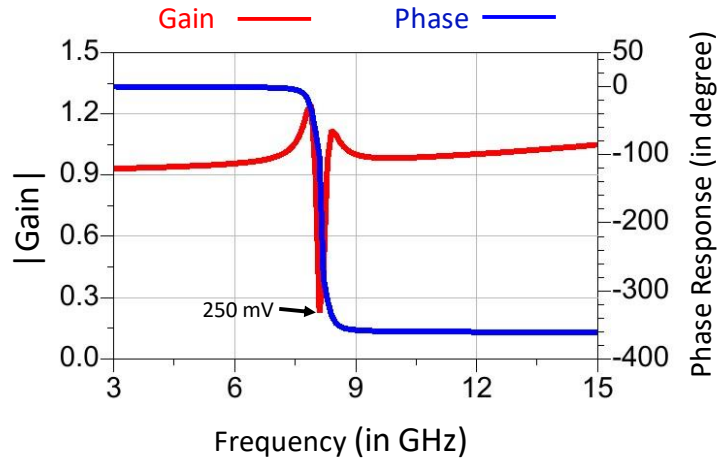


Fig. 1.6. Gain and phase of gain plot for the proposed bridge resonator

A non-zero error voltage ('e' in Fig. 1.2) of 250 mV is also present at the output at 8 GHz due to a slight imbalance. Note that the phase response has a sharp discontinuity at resonance, with a phase slope of 450°/GHz. This sharp, narrowband response is unique to the bridge resonator, and leads to a high Q factor due to small $\Delta\omega$ in eq.(1.5). The value of $\Delta\omega$ is 0.28 GHz, which gives a Q of 29.

1.4.3 Benchmarking and Modelling Passive Performance

Benchmarking the performance of the passive components (e.g. transmission lines, inductors, capacitors) in 22-nm FD-SOI CMOS technology is important for implementing high-performance RF resonator and oscillator. Therefore, one of the objectives of this thesis is to benchmark the performance of these passives by optimizing the designs and verifying their performance. Moreover, the process design kit (PDK) does not provide some other passive components necessary to implement the low-phase-noise RF oscillator proposed in this work, such as autotransformer (discussed in Chapter 7). Therefore, custom layout passive designs are crucial for ensuring optimum performance of the proposed on-chip design.

Considerable attention is also directed towards modelling the high-Q (> 150) transmission lines demonstrated in this thesis. The objective is to develop a new lumped-element model for such high-Q balanced transmission lines with floating shields with parameters which can be extracted from measured or simulated data (e.g., from electromagnetic simulation).

1.4.4 Interfacing Circuit Blocks

Interfacing sub-blocks in the oscillator circuit has a significant effect on the circuit's performance. It affects the loading seen by each block, and therefore sets the gain of individual sub-circuits in the loop. Therefore, the circuit blocks must be designed for specific input and output impedances to maintain a high-Q response. This challenge is addressed by proper selection of the loop and individual circuit topologies, and by adding tuning circuits where necessary.

1.4.5 Gain Control

For oscillation to begin, the circuit has to meet the two conditions [20]

$$L(\omega_{osc}) > 1 \quad (1.6)$$

$$\angle L(\omega_{osc}) = 2\pi n. \text{ where } n = 0, 1, 2 \dots \quad (1.7)$$

where $L(\omega_{osc})$ is the magnitude of the closed-loop gain, ω_{osc} is the frequency of oscillation, and eq. (1.7) defines the phase of the closed-loop gain function. When these conditions are satisfied, the oscillation builds up gradually. However, there must also be a mechanism to limit the gain once the desired output amplitude is achieved. Hence, oscillators require gain control [17].

There are two gain control schemes applied in most on-chip oscillator designs: automatic gain control (AGC), or amplitude limiting. The choice depends on the performance requirements. With the AGC approach, additional circuitry is needed which increases the complexity, area, and power consumption [21]. A limiter (Chapter 8, Section 8.5 in [17]), while simpler, can degrade the phase noise performance because of its non-linearity. In the proposed design, the supply voltage and operating regions of the transistor limit the voltage swing and the final oscillation output. The power amplifier of the proposed topology (see Fig. 1.2), is used as the limiting block, as it clips the output amplitude when driven by a large signal. The output voltage swing of the amplifier is limited by the supply voltage. High-breakdown-voltage (1.8-V nominal supply) transistors are used to maximize the output voltage swing, and hence the P_{avg} in eq. (1.2) to reduce phase noise.

1.4.6 Robustness

It is important to provide robustness to processing and parameter variations, as designers do not have full control over these physical phenomena. For example, high-Q resonators are sensitive to manufacturing variations [22]. To address this challenge, the design needs to have adequate margin for changes in manufacture, temperature, and supply voltage. This proposed oscillator is provided with 5% – 8% performance margin to achieve the desired robustness

determined by extreme case simulations, which consider the maximum and minimum variations of capacitances and resistances provided by the 22-nm FD-SOI CMOS process design kit (PDK).

Gain and frequency adjustments are incorporated into the design prototype to improve its robustness. Loop gain is varied by tuning balancing component L_b in Fig. 1.2. This changes the bridge gain and the overall loop gain. The frequency of oscillation is controlled to within $\pm 4\%$ by varying a capacitor inside each resonator block. To minimize the additional circuit noise, an array of switched metal-oxide-metal capacitors is used in the proposed design to adjust the circuit [23]. A tuning circuit is also incorporated in the bandpass filter network at the output of the preamplifier to control its centre frequency, as it controls both the oscillation frequency and the loop gain. In this way, the peak-gain of the preamplifier is maintained within the desired range. A digital code is used to control the switches used for tuning control.

1.4.7 Supply Voltage Constraints

The 22-nm SOI-CMOS technology used in this work offers transistors with a nominal supply voltage of 0.8 V. The preamplifier stage of the oscillator prototype utilizes the 0.8-V transistors. However, the relatively low supply voltage constrains the signal power at the power amplifier output and thus the phase noise performance. To lower the phase noise, it is crucial to have a large output signal power, as seen from eq. (1.2) and discussed in Section 1.4.1. Therefore, 1.8-V breakdown transistors are used in the power amplifier stage to facilitate larger output voltage swings and lower phase noise.

Also, the capacitors and switches have breakdown voltage limits (e.g., maximum voltage limit for capacitors is typically 10 V). Therefore, signals across each of these should not cause stress or damage. Custom designed capacitors are therefore used to achieve higher voltage operation.

1.5 Summary and Thesis Organization

The goal of this thesis is to achieve the lowest possible phase noise by designing and integrating a novel circuit. Digital tuning is used to accommodate processing variations and provide robustness. Power consumption is not a primary design consideration for this work. However, it is an important area for future work.

The thesis is comprised of seven chapters. In Chapter 2, a literature survey of previous work in low-phase-noise RF oscillators is presented. Passive components for use in the oscillator, and their performance in the 22-nm SOI-CMOS technology are benchmarked in Chapter 3 (inductors and capacitors). Chapter 4 describes the design and implementation of novel on-chip, high-Q bridge resonator. Advanced transmission line designs intended for application as high frequency resonators are described in Chapter 5. In Chapter 6, the proposed oscillator circuit topology and methodology for its design are described. Chapter 7 demonstrates the design of active circuit blocks, and the system integration of the oscillator. This chapter also documents post-layout simulation results for the complete prototype. Finally, concluding remarks and a proposal for future work are presented in the last chapter of the thesis.

Chapter 2

Background and Literature Review

In this chapter, fundamental concepts of RF oscillators and their theory of operation are explained. A literature survey of previous work in RF and mm-wave oscillator design for integrated circuits is also presented.

2.1 Fundamentals of Resonators and RF Oscillators

An RF oscillator is a non-linear circuit that converts DC power to an RF waveform. There are several techniques that are used to construct an oscillator. Two approaches are: 1) use of positive feedback through a frequency selective element, or 2) destabilizing a resonator with a negative resistance [17]. A block diagram illustrating a positive feedback oscillator is shown in Fig. 2.1. The major circuit blocks of an oscillator are: the frequency-selective filter $\beta(\omega)$, and $A(\omega)$, which is an amplifier.

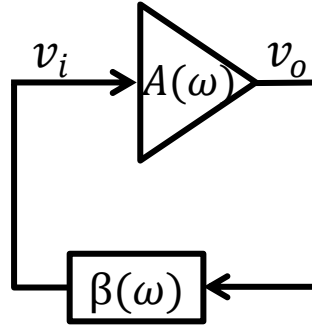


Fig. 2.1. Feedback oscillator block diagram

A linear model for the oscillator may be used to capture the start-up phase of operation, when v_o is a small signal [23]. The gain of the amplifier, $A(\omega)$, is a function of angular frequency, ω . From linear circuit theory, the output voltage v_o is given by

$$v_o = \frac{A(\omega)}{1 - \beta(\omega)A(\omega)} v_i. \quad (2.1)$$

The feedback network is a bandpass filter with resonant frequency, ω_{osc} . When the denominator in eq. (2.1) is zero, the small-signal closed-loop gain approaches infinity, and an oscillation starts at ω_{osc} , which is the resonant frequency of the $\beta(\omega)$ filter block.

$$|1 - \beta(\omega_{osc}) \cdot A(\omega_{osc})| = 0, \quad (2.2)$$

which gives $L(\omega_{osc}) = \beta(\omega_{osc}) \cdot A(\omega_{osc}) = 1$. (2.3)

The conditions for oscillation are described by Barkhausen's criteria [24] in eq. (1.6) and (1.7). Eq. (1.6) states that, the gain of the amplifier at ω_{osc} (i.e., $A(\omega_{osc})$) must be sufficient to compensate for losses in the filter, $\beta(\omega_{osc})$. The second condition (eq. (1.7)), states that the closed-loop phase shift must be an integer multiple of 360° . For an oscillation to start, there must be an initial disturbance in the feedback loop. This may arise from a start-up transient or thermal noise present in the oscillator components. At start up, the loop gain is greater than one and electronic noise is amplified and filtered by the loop. As the oscillation progresses and the amplitude increases, the output voltage of the amplifier also increases. If there is no dedicated gain control circuit, it reaches the non-linear limits of the amplifier circuit, which constrain the oscillation voltage, v_o to v_{osc} . At this point, the loop gain is unity. Amplitude limiting is often determined by boundary conditions such as the supply voltage and triode or cut-off regions of the FET transistors in the amplifier.

2.2 Ideal Oscillator Characteristics

For an ideal oscillator, all RF output energy is confined to a single frequency. The frequency spectrum consists of a single tone with infinitely narrow bandwidth centred at the operating frequency of the oscillator, ω_{osc} . Fig. 2.2a shows the spectrum of an ideal oscillator.

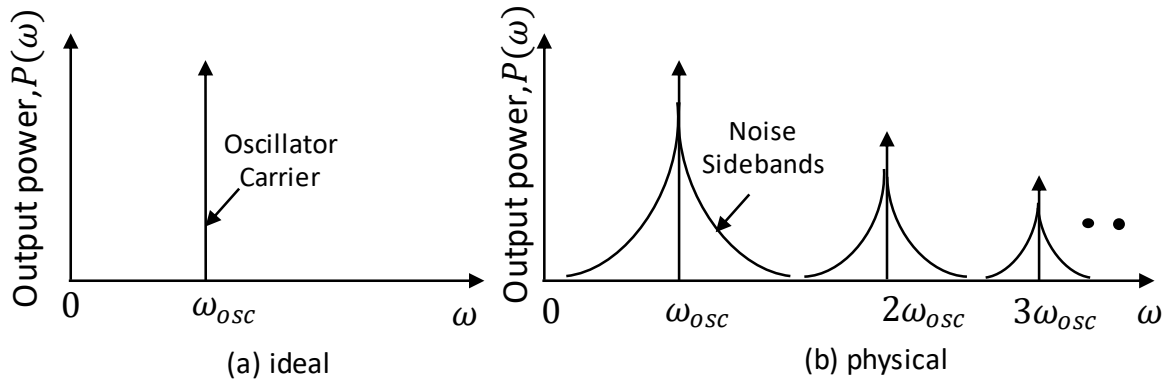


Fig. 2.2. Oscillator output spectrum

The output from any practical circuit is modulated by random amplitude and phase fluctuations. This results in unwanted sidebands in the spectrum as shown in Fig. 2.2b. Along with sidebands associated with the fundamental frequency, there are also harmonics with noise sidebands in the spectrum at higher frequencies generated by non-linearities (e.g., amplitude limiting) of the oscillator circuit.

2.3 Importance of Resonator Q from Oscillator Phase Noise Model

As mentioned in Section 1.4.1, phase noise is the short-term instability of the oscillator output caused primarily by phase modulation. The fundamentals of phase noise are explained in detail in Appendix A. Modelling the phase noise of the oscillator analytically with respect to the transistor bias current, transistor size, and values of the resonator components is important for design purposes. In this section, a linear theory that estimates the phase noise in an oscillator is presented.

2.3.1 Leeson's Model

In this section, Leeson's model is analysed for further understanding [18]. The model is developed from the oscillator feedback block diagram of Fig. 2.1. However, the response of the amplifier and the bandpass filter inputs and outputs are described in the phase (rather than

voltage) domain. The model applies to frequency-selective feedback oscillators with moderate- and high-Q resonators.

The one-sided transfer function $\beta(f_p)$ of a bandpass filter resonator centred at f_{osc} is the low-pass response [17]

$$\beta(f_p) = \frac{1}{1 + jQ \left(\frac{f_p}{f_{osc}} - \frac{f_{osc}}{f_p} \right)} = \frac{1}{1 + j \left(\frac{2f_p Q_L}{f_{osc}} \right)}, \quad (2.4)$$

where f_p is a frequency offset from the carrier f_{osc} that is assumed to be much smaller than f_{osc} . Parameter Q_L is the loaded Q of the resonator. In Leeson's model, a noise-free amplifier is preceded by a phase modulator, as illustrated in Fig. 2.3.

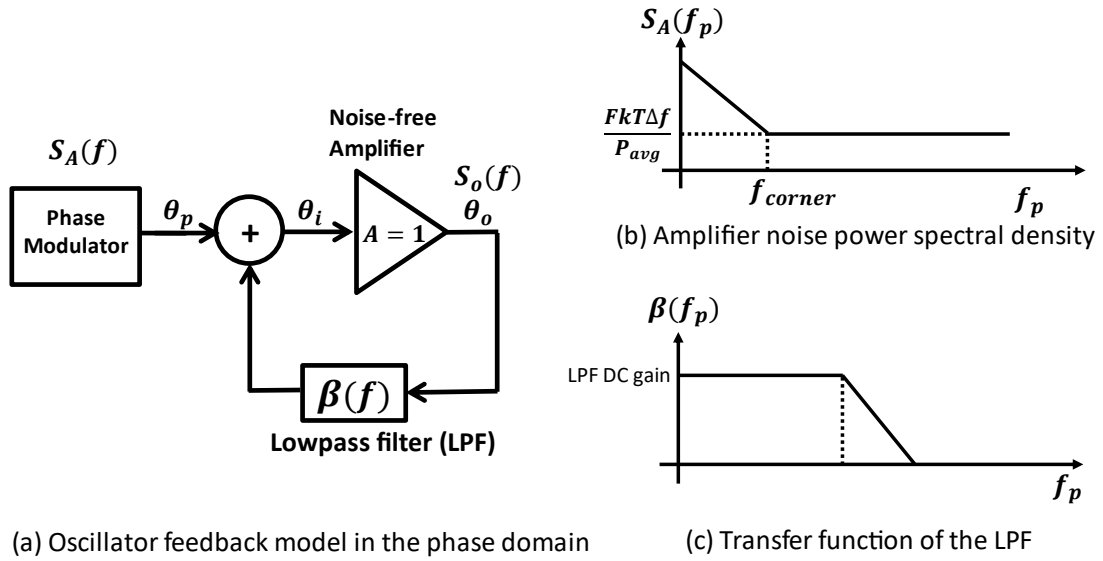


Fig. 2.3. Leeson's linear feedback model [17]

The noise power spectral density (PSD) of the amplifier drives the phase modulator. The PSD has a $1/f$ spectral density region from DC up to the $1/f$ noise corner frequency, f_{corner} , and a white noise region, with a constant power spectral density kTF , above the $1/f$ corner frequency. Here, F is the amplifier noise factor with respect to resonator impedance seen at f_{osc} .

The phase variable at the output of the loop ($\theta_o(f_p)$) can be written as

$$\theta_o(f_p) \beta(f_p) + \theta_p(f_p) = \theta_o(f_p), \quad (2.5)$$

$$\theta_o(f_p) = \frac{\theta_p(f_p)}{1 - \beta(f_p)} = \theta_p(f_p) \left(1 + j \frac{f_{osc}}{2f_p Q_L} \right). \quad (2.6)$$

The output noise power spectral density, $S_o(f_p)$, defined from $S_A(f_p)$ and $\beta(f_p)$ in Fig. 2.3 is

$$S_o(f_p) = \frac{S_A(f_p)}{|1 - \beta(f_p)|^2} = \frac{FkT\Delta f}{P_{avg}} \left(1 + \frac{f_{corner}}{f_p} \right) \left[1 + \left(\frac{f_{osc}}{2f_p Q_L} \right)^2 \right]. \quad (2.7)$$

The single-sideband phase noise, $L(f_p)$, is the single-sided noise power spectral density in a 1-Hz bandwidth (Δf).

$$L(f_p) = \frac{S_o(f_p)}{2} = \frac{FkT\Delta f}{2P_{avg}} \left[1 + \left(\frac{f_{osc}}{2f_p Q_L} \right)^2 \right] \left(1 + \frac{f_{corner}}{f_p} \right). \quad (2.8)$$

From eq. (2.8) it is noted that, there are four distinct spectral regions: $1/f^3$, $1/f^2$, $1/f$, and $1/f^0$ (i.e., flat, as seen in Fig. 2.4). For low- to medium-Q resonators (e.g., Q factor less than 50), the $1/f^3$, $1/f^2$, and $1/f^0$ regions dominate. The $1/f$ regime appears only for very high-Q resonators (e.g., a quartz-crystal resonator with Q-factor greater than 100). Raising the signal power (P_{avg}) lowers the phase noise, $L(f_p)$. Therefore, amplifier stages in an oscillator that produce greater P_{avg} gives better phase noise performance. The focus of this work is on $1/f^2$ regime performance, because a low-Q resonator is assumed. A phase-locked loop (PLL) synthesizer typically suppresses phase noise in the $1/f^3$ and a portion of the $1/f^2$ regimes. Finally, maximizing the loaded Q-factor (i.e., Q_L) is a key parameter that demands attention to the design of the resonator circuit.

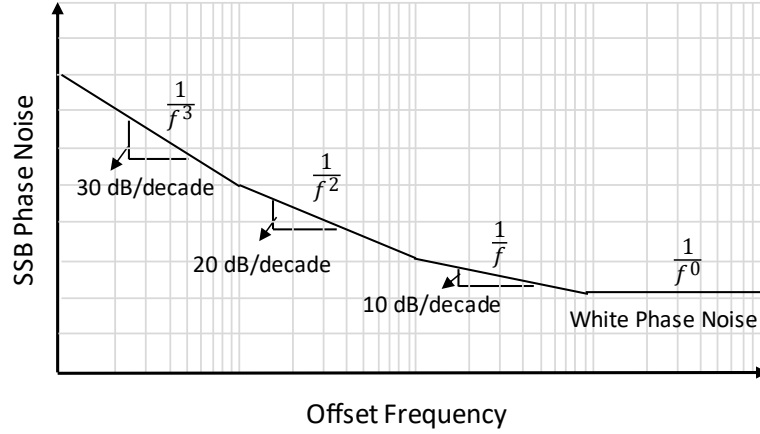


Fig. 2.4. Phase noise regimes defined

2.4 Literature Review of Passive Components

Leeson's formula predicts the significance of high-Q passive components in the design of low-phase-noise oscillators. Numerous work have been done towards improvement of on-chip RF passive components such as inductors, capacitors and transmission lines.

Transmission lines (TLs) are used as interconnects, resonators, inductors, and transformers on an integrated circuit (IC) [25]. Single microstrip lines in 0.13 μm CMOS technology were reported with peak Q of 23 at 30 GHz in [26] and 28 at 25 GHz in [27]. Reduced metal thickness and spacing, and dielectric permittivity (κ) between interconnects of scaled technology create challenges for high-Q designs because of increased equivalent series resistance (r). Transmission lines resonators used in low-phase-noise oscillators requires Q greater than 50, or low attenuation constant for a narrow-band operation [28]. No literature has documented the realization of on-chip transmission lines in silicon with Q values greater than 100. This work presents design of transmission lines with Q value greater than 100 for narrow-band operation around 10 GHz (in Chapter 5).

The drive to build higher performance RF circuits in the millimetre-wave (mm-wave) frequency bands (30 GHz-300 GHz, in air) is motivating electrical modelling of transmission lines on a silicon chip. A lumped-element circuit model of transmission lines that is compatible

with time-domain (e.g., SPICE) simulators is required for circuit design [29], [30], [31], [32]. In [33], J. Zheng, et al, proposed models for both CPW and microstrip coupled lines that use modified quasi-static spectral domain electromagnetic approaches, hybrid conformal mapping technique, and complex image method to extract the frequency-dependent elements, which makes this approach cumbersome for practical design work. A lumped-model for coupled CPW-type lines is proposed in [34], where a frequency asymptotic technique is used to calculate model parameters from distributed parameters. This does not provide closed-form equations for the model parameters. On the other hand, a model based on simpler structural or geometrical calculation is demonstrated in [35]. However, this model is only described for a single line. The reported lines in the above mentioned work are not shielded from substrate loss, and do not consider high Q-factors (i.e., greater than 100). Therefore, a model that can accurately predict the behaviour of balanced and single-ended lines on silicon is required, which is compatible with differential circuits, and can also be applied to both shielded and unshielded implementations.

Capacitors and inductors are typically used to implement L-C resonator circuits on a chip. Two capacitor implementations in the 22-nm CMOS technology are metal-oxide-metal (MOM) and alternative polarity MOM (APMOM). MOM capacitors are formed with interdigitated metal fingers. ASPMOM capacitors have similar interdigitated fingers but also alternative polarity fingers placed in the vertical direction. MOS capacitors are also used widely due to their voltage controlled tuning property. However, they have lower Q-factor than MOM/APMOM capacitors. Capacitors constructed using BEOL metals offer better linearity, high Q-factor, and very small temperature variations [36]. MOM capacitors are often preferred for RF and mm-wave integrated circuits (ICs) over APMOM because of their lower fabrication cost and high capacitance density [37]. This is why, they are used extensively in RF/mm-wave circuits where high-Q capacitors are required. In addition to minimising energy loss due to small equivalent series resistance, high-Q capacitors reduce thermal noise which helps in maintaining desired signal-to-noise ratios.

Table 2.2 shows performance of selected capacitors and inductors offered by the 22-nm FD-SOI CMOS process design kit (PDK) [38]. Two types of capacitors are shown: 1) MOM and 2) alternative polarity MOM (APMOM). The maximum operating frequency is defined by self-resonant frequency (SRF) in Table 2.2. The PDK capacitor cells are implemented using lower-level BEOL metals, but not the thick top metals. This increases capacitance density but also the electrode series resistance is increased. The limited oxide thickness between the capacitor electrodes and the shield increases their parasitic capacitance. Therefore, custom capacitor designs are required to achieve Q greater than 100 (at 10 GHz) and higher operating frequency. In Table 2.2, operating voltage is also mentioned (e.g., MOM-7V has operating voltage limit of 7 V).

Table 2.1. Performance of passive PDK cells in 22-nm FD-SOI CMOS technology [38]

Passive type	Layout type	BEOL option	Capacitance (pF)	Q factor At 10 GHz	SRF (GHz)
Capacitor	MOM-7V	Stack 11 Stack 19	1.95	19	>50
	MOM-10V	Stack 11 Stack 19	0.80	21	>50
	APMOM-5V	Stack 11 Stack 19	1.00	26	>50
Passive type	Layout type	BEOL option	Inductance (nH)	Single Ended Peak Q factor	SRF (GHz)
Inductor	Symmetric	Stack 11	0.35	17.6 at 18 GHz	78
	Symmetric	Stack 11	2.80	13.6 at 2 GHz	11
	Symmetric	Stack 19	0.45	21 at 18 GHz	>50
	Symmetric	Stack 19	2.00	19 at 8 GHz	40

The symmetric inductor PDK cell performance for multiple inductance values is also shown in Table 2.1. Q factor values in the range of 20 are achievable from the 2-nH PDK inductors. Their performance is also limited in breakdown voltage and peak Q factor like the capacitor.

2.5 Resonator based Oscillator Topologies and Literature Review

The oscillator circuit topologies of interest for RF/mm-wave applications may be classified according to the type of resonator, e.g., a crystal oscillator or a cross coupled LC-VCO (voltage-controlled oscillator). Crystal oscillators use high-Q, off-chip quartz-crystal resonators. The parallel inductor-capacitor (i.e., L-C) resonator, or tank, of the LC-VCO is often found in on-chip implementations. Notable work in the development of low-noise RF L-C oscillators is reviewed in this section.

2.5.1 L-C Oscillator Topologies

L-C oscillators hold a prominent position in the published literature of RF integrated oscillators. There are multiple ways of constructing an L-C bandpass filter network and amplifier to form an L-C oscillator. Common types of feedback L-C oscillators are the Hartley [39], Colpitts [40], Armstrong [41], and Clapp [42] circuits.

The Colpitts oscillator remains a fundamental component in RF oscillator design due to its simplicity, reliability, and performance. However, phase noise performance of the Colpitts oscillator was shown theoretically by Andreani, *et al.* [43] to be inferior to the cross coupled L-C circuit.

L-C oscillators may be classified according to the class of amplifier employed. This is determined from the design and DC biasing of the amplifier in the feedback loop (e.g., classes A, B, C, and F). The load of the amplifier in the cross coupled L-C oscillator is the resonator tank. The amplifier's class of operation depends on the DC bias condition which controls the power efficiency (η_p) of the amplifier, given by [17]

$$\eta_p = \frac{P_{avg}}{P_{DC}} = \frac{I_{rms} \cdot V_{rms}}{I_{DC} \cdot V_{DC}} = \eta_I \cdot \eta_V , \quad (2.9)$$

where I_{rms} and V_{rms} are the effective values for the fundamental components of current and voltage at the amplifier output. The supply voltage and bias current are V_{DC} and I_{DC} , respectively. Parameter η_I is the current efficiency, and η_V is the voltage efficiency. The

different classes can be explained from the transistor bias or quiescent point (Q-point). This is illustrated in Fig. 2.5 [44].

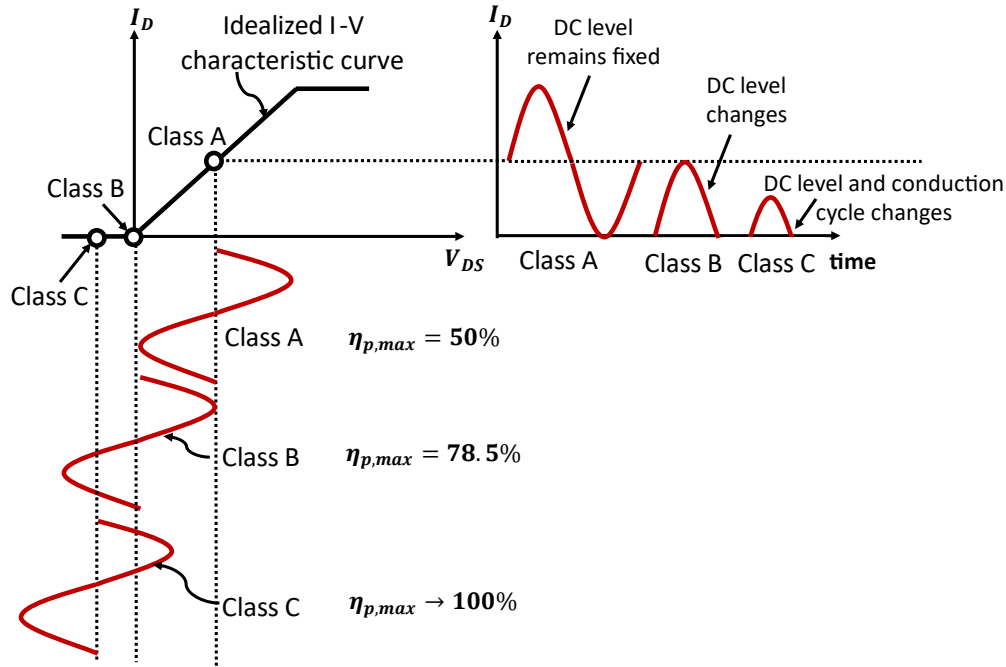


Fig. 2.5. Bias points for different amplifier classes [44]

Fig. 2.5 shows the idealized I_D vs V_{DS} characteristics of a MOSFET, which is the DC drain current (I_D) plotted against varying drain to source voltage (V_{DS}). Different bias points (i.e., I_D and V_{DS}) for the different classes of operation are also shown. For class-A operation, the bias point is in the linear region of the transfer characteristic. Therefore, the output current has a complete swing for the full cycle as shown in the red curves. The percentage of conduction per cycle gradually decreases for class-B and class-C, as the bias point moves close to the cut-off point (marked as class-B and class-C in Fig. 2.5). This increases efficiency (η_p) from 50% for class-A to close to 100% for class-C (as the current waveform approaches an impulse response). Other classes of operation (e.g., D, E, F, etc.) have been developed to optimize the efficiency further [45] [46]. For example, class-F amplifiers are formed by adding filters at the output of the amplifier to shape the output waveform and increase RF efficiency [47].

Typically, efficiency improves at the expense of lower small-signal gain (required for oscillator start up).

The amplifier DC bias therefore controls the power efficiency (η_p) and rms output power, P_{avg} of the oscillator, which affects the phase noise. The relationship between $L(f_p)$ and η_p of the oscillator can be derived by substituting eq. (2.9) in eq. (2.8)

$$L(f_p) = \frac{FkT\Delta f}{2 P_{DC} \cdot \eta_p} \left[1 + \left(\frac{f_{osc}}{2f_p Q_L} \right)^2 \right] \left(1 + \frac{f_{corner}}{f_p} \right). \quad (2.10)$$

Eq. (2.10) demonstrates that phase noise decreases with the increase of power efficiency. All of the above mentioned classes of amplifier topologies have been used to build high-frequency and low-phase-noise oscillators. For example, for an L-C cross coupled oscillator, the current waveform defines the class of operation, because the filtering by the parallel L-C tank results in a sinusoidal output voltage for all amplifier classes. When operated in class-A, the current flowing in the tank is sinusoidal with a conduction angle of 360 degrees. In classes B and C, the conduction angle of the drive current is considerably less than 360 degrees, which conserves DC power and can improve oscillator efficiency [48], [49], [50]. Some examples of different classes of cross coupled L-C oscillators are described in the following sub-sections.

2.5.1.1 Cross Coupled L-C Tank Oscillators

The cross coupled L-C oscillator (see Fig. 2.6) dominates the RFIC literature due to their simple topology and relatively good phase noise performance. It consists of a differential amplifier driving a parallel L-C resonator with unity feedback. Components L and C_T in parallel with R_T (representing the ohmic loss of L and C_T) form the resonator tank.

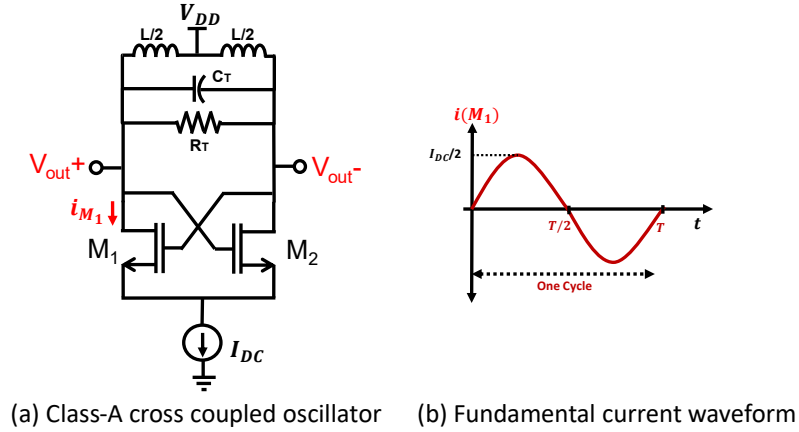


Fig. 2.6. Class-A cross coupled L-C oscillator

The Q-points of M_1 and M_2 are set near the middle of the transfer curve so that the transistor avoids triode and cut-off regions and therefore operates in class-A at start-up. Therefore, both transistors conduct current for the full cycle of the output waveform. This means the maximum current in each transistor during a cycle is I_{DC} . The maximum differential output voltage-swing across R_T can reach to $4V_{DD}$ because of energy storage in the inductor. The maximum possible power efficiency is thus calculated from eq. (2.2)

$$\eta_{pA-max} = \frac{I_{rms} \cdot V_{rms}}{I_{DC} \cdot V_{DC}} = \frac{\frac{I_{DC}}{\sqrt{2}} \cdot \frac{4V_{DD}}{\sqrt{2}}}{I_{DC} \cdot V_{DD}} = 0.5 \times 100\% = 50\% . \quad (2.11)$$

At steady state the oscillator operates in class-B where only one transistor conducts current for only half of the time period increasing the power efficiency [19].

Cross coupled L-C oscillators are one of the simplest topologies to implement. Therefore, they have made a significant impact on RF oscillator literature [19] [51]. In [19], Andreani demonstrated 2.3-GHz L-C oscillator that shows a phase noise of -144 dBc/Hz at 3 MHz offset.

In practical cases, the tail current generator I_{DC} (Fig. 2.6a) also produces phase noise. The phase noise can be improved by placing an additional LC-tank, resonating at $2\omega_{osc}$, at the tail [52] [48] [49]. This is known as explicit common-mode (CM) resonance technique. This is

shown in Fig. 2.7a. The high impedance due to resonance at $2\omega_{osc}$ filters out noise current of the tail current source at $2\omega_{osc}$.

A potential drawback of the explicit CM resonance technique is the requirement for a second L-C tank. In addition, the common-mode impedance of the main tank at $2\omega_{osc}$ degrades the effectiveness of the tail inductor. These factors can be mitigated by using a single tank that has two distinct resonant modes: a differential mode that resonates at ω_{osc} , and a common mode that resonates at $2\omega_{osc}$. This can be done by introducing coupling between the inductors in the main tank ($L/2$) [53]. The common-mode resonance is tuned by the coupling factor k (see Fig. 2.7b). However, in common-mode, the coupling between the two tank inductors reduces the effective inductance by a factor of $2(k\sqrt{L})$.

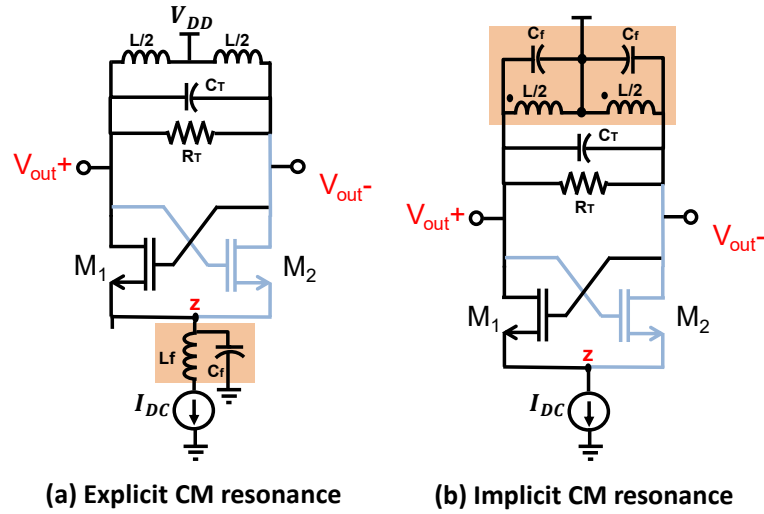


Fig. 2.7. Implicit and explicit common-mode resonance techniques

Optimized performance is achieved by combining the implicit and explicit resonances as proposed in [48] and [49]. In [49], Hong presented the dual common-mode (CM) resonance technique in a high-frequency oscillator implementation. The low implicit CM impedance problem is addressed by introducing a low-loss CM current return path to maintain a required resistive CM impedance across the entire $2\omega_{osc}$ band. Hong's oscillator shows phase noise of -121.7 dBc/Hz at 1-MHz offset frequency from an 8-GHz carrier.

In a class-C amplifier, the bias point is chosen such that the device current is zero for more than one-half cycle of the sinusoidal input signal (see Fig. 2.5). Class-C oscillators show better phase noise performance than class-B by shaping the fundamental drain current into an impulse-like waveform with a tail capacitor. However, class-C oscillators exhibit inevitable start-up problems owing to low-gate bias voltage (i.e., lower than threshold voltage as shown in Fig. 2.5), which causes insufficient MOSFET transconductance and amplifier gain of the cross-coupled differential pair.

In a recent work, a 19.7-GHz class-C, oscillator implemented in 65-nm CMOS that ensures a robust start-up is reported in [50]. The proposed start-up scheme uses a voltage converter that supplies a time-varying bias voltage to the core transistors depending on the output state of the oscillator. The circuitry is enabled during start up, so power consumption is minimized without phase noise degradation. The measured minimum phase noise at a 1-MHz offset is reported to be -106.33 dBc/Hz at an oscillation frequency of 19.7 GHz (ref. Table 2.1 column 6).

2.5.2 Other L-C Oscillator Topologies

There are other oscillator topologies reported in the literature which were developed to optimize the resonator Q. In some cases, combining two or more of the previously described topologies leads to a circuit with better phase noise. Examples are transformer coupling applied with other amplifier classes [54] [55], cascode transistor techniques [56] [57], and common-mode resonance techniques by using multi-resonator tanks [55].

2.5.2.1 Transformer-Coupled Oscillator

A transformer-based tuned oscillator concept illustrated in Fig. 2.8a was initially proposed by Visweswaran, *et al.*, in [58]. Hard limiting of the output voltage swing is proposed. Even or odd harmonics are filtered with tuned transformers to shape the output signal for better power efficiency. This concept was later used by Babaie and Staszewski to demonstrate a harmonic-tuned L-C tank with transformer coupling in a class-F oscillator [59] (ref. Table 2.1 column 2). One drawback of using a transformer is that it increases the complexity of the tank

design because of loading requirements, as on-chip transformers typically have lower quality factors than simple inductors. The drawback is mitigated by the steeper phase response offered by the transformer-based resonators with respect to a simple L-C tank for the same Q-factor [60].

In [61], another transformer based 1.6-GHz class-F2 oscillator that makes use of second harmonic tuning was reported by Babaie and Staszewski. This utilizes the explicit CM resonance concept discussed in Section 2.5.1.1. It exhibits phase noise of -139 dBc/Hz at 3-MHz offset from an 8.7 GHz carrier (ref. Table 2.1 column 5).

The transformer coupled harmonic tuning concept may be extended to other oscillator classes. In [54], transformer coupling is implemented in a class-C oscillator where the resonator is comprised of two asymmetric L-C tanks which are transformer coupled. The circuit is shown in Fig. 2.8a. The coupling coefficient of the transformer is designed to be as high as possible to increase the resonator Q factor.

2.5.2.2 Stacked Oscillator

For low-phase-noise performance, it is important to maximize the output signal power, leading to high output voltage swings as seen from eq. (2.8). Cascoding, or ‘stacking’ multiple transistors (illustrated in Fig. 2.8b [57]) realizes greater output voltage swing although, the transistors still operate within their safe operating range. Total output voltage swing can be higher than each transistor’s breakdown voltage.

A 5-GHz oscillator that uses high-Q (e.g., more than 20), single-turn, nested differential inductors to achieve even-harmonic shaping, was proposed by El-Aassar, *et al.* [57]. The complementary nature of NMOS and PMOS transistors is exploited to achieve second- and fourth-harmonic common-mode resonances using differentially driven symmetric inductors with 1.3 times peak Q-factor compared to the conventional single-ended tail filter [62]. The oscillator phase noise is reported -127.6 dBc/Hz at 1-MHz offset at 5.4 GHz oscillation frequency (ref. Table 2.1 column 4).

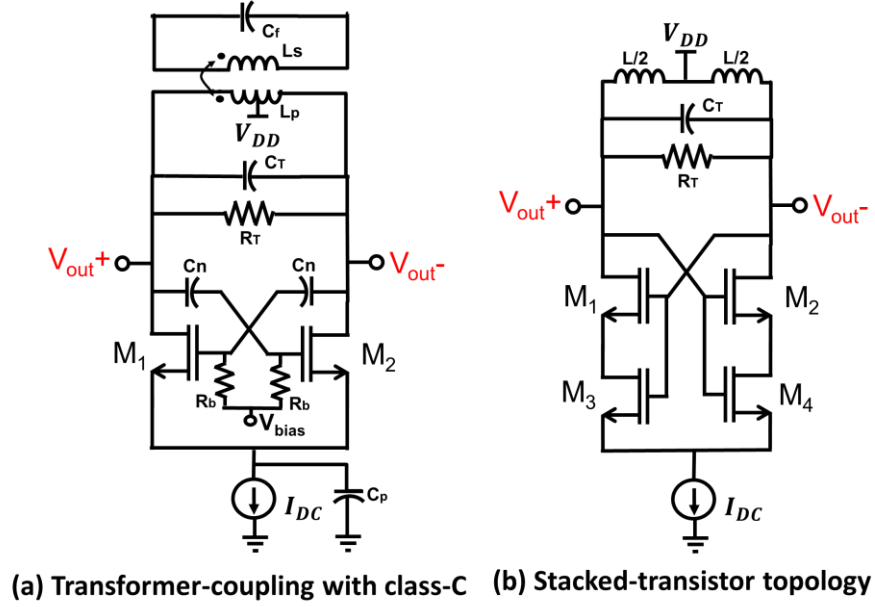


Fig. 2.8. Transformer coupled and stacked transistor topologies

2.5.2.3 Multi-resonant Tank Oscillator

Instead of using a single resonator tuned to a harmonic, multiple resonators may be used to suppress more than one harmonic component of the output signal current. A class-F23 amplifier is proposed in [55], where a combination of second- and third-harmonic common-mode (CM) resonance technique is applied to increase the resonator Q . It exhibits -112.2 dBc/Hz at 1-MHz offset for an oscillation frequency of 16.8 GHz.

2.5.2.4 Performance Summary of L-C Oscillators

Table 2.1 summarizes the performance data of the topologies covered in previous sections. The table includes state-of-the-art prototypes based on their phase noise performance.

Table 2.2. Performance summary of selected RF L-C oscillators from the recent literature

References	JSSC'13 [59]	JSSC'15 [61]	SSC-L'20 [57]	JSSC'21 [63]	TCAS I' 22 [50]	JSSC'17 [53]
Technology	65nm CMOS	65nm CMOS	22nm FD-SOI	22nm FD-SOI	65nm CMOS	28nm CMOS
Topology	Class-F with 1 trans- former	Class-F2 with 2 trans- formers	Cascode Comple- mentary	Dual- Core Folded CM	Dual CM Resonance	Implicit CM Reso- nance
Frequency (GHz)	7.4	8.7	4.75-5.4	8 to 17	8 to 11.15	4.7-5.4
V_{DD} (V)	1.25	1.3	0.6	0.45	1	0.7
P_{DC} (mW)	15	41.6	18.2 to 15.2	17 to 33	5 to 6	0.5
PN (dBc/Hz) @ 1MHz	-125	-128.5	-127.6 to -128.7	-119.1 to -112.3	-121.7 to -114.8	-
PN (dBc/Hz) Normalized to 8-GHz f_{osc} , 1-MHz offset	-124.32	-129.23	-125.29	-119.1	-121.7	-113.74
FOM (dBc/Hz) @ 10 MHz	192.5	191.6	191 to 193	197.8 to 208.8	190 to 192.3	194-196
Core Area (mm ²)	0.13	0.2	0.2	0.39	0.126	0.18

Phase noise (PN) is normalized to a specific offset (f_{p2}) and carrier frequency (f_2), for ease of comparison. The normalization formula used in Table 2.2 is

$$L(f_{p2})|_{f_2} = L(f_{p1})|_{f_1} - 20 \log_{10} \left(\frac{f_1}{f_2} \right) + 20 \log_{10} \left(\frac{f_{p1}}{f_{p2}} \right), \quad (2.12)$$

Where $L(f_{p2})|_{f_2}$ is the phase noise at offset f_{p2} for carrier frequency f_2 , and $L(f_{p1})|_{f_1}$ is the phase noise at offset f_{p1} for carrier frequency f_1 .

From the normalized PN row, it is seen that a class-F circuit offers the best performance [59] [61]. Multi-resonator tanks offer improved phase noise for any class of oscillator [63], [50]. Also, for scaled CMOS technologies, the core area decreases for similar phase noise performance.

2.5.3 Crystal Oscillator Topologies

Crystal oscillators emerged during the 1920s [64] [65]. Noteworthy contributions include Sabaroff's quartz crystal version of the Colpitts L-C oscillator in 1937 [66], and Meacham's bridge stabilized oscillator circuit in 1938 (ref. Fig. 1.1) [7]. The post-World War II era witnessed a significant infusion of resources into quartz crystal development. A major reason for the wide use of crystal oscillators is their high Q factor. A typical Q value for a quartz oscillator ranges from 10^4 to 10^6 , compared to less than 100 for an L-C oscillator [6]. High-Q crystal resonators have minimal energy losses at resonance. The amplifier in a traditional L-C cross coupled oscillator produces negative equivalent resistance [17], as shown in Fig. 2.9.

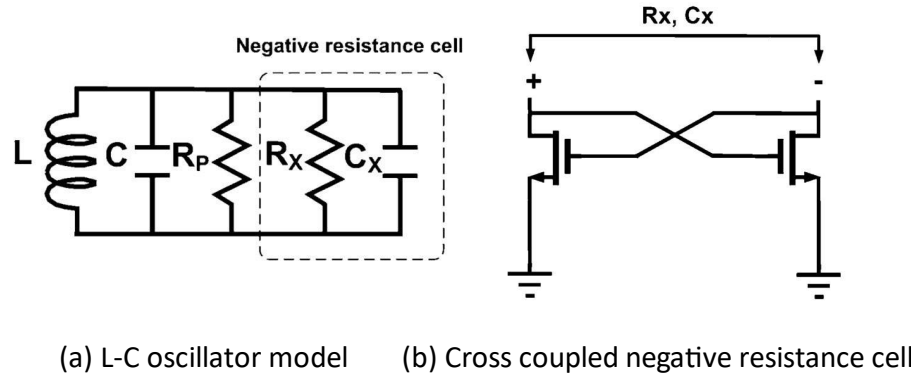


Fig. 2.9. Cross coupled L-C oscillator model [67]

Quartz-crystal resonators are typically modelled as series resonators. The equivalent series resistance of a high-Q quartz-crystal resonator is very small due to minimal energy losses at resonance. To implement an L-C topology with a quartz-crystal resonator having low equivalent series resistance therefore needs the absolute resistance value of the negative resistance cell to be also low. It is seen that this negative resistance value is inversely proportional to the g_m of the FET transistor [17]. Therefore, to achieve a lower absolute value of resistance (e.g., less than $|-1| \Omega$), the g_m needs to be very high. Because of this, implementing a cross-coupled L-C oscillator topology with a high-Q crystal oscillator is not a great choice.

Fig. 2.10 shows a block diagram of a quartz-crystal oscillator [68], where a discrete crystal resonator is used with an amplifier and a phase shifter in the positive feedback loop.

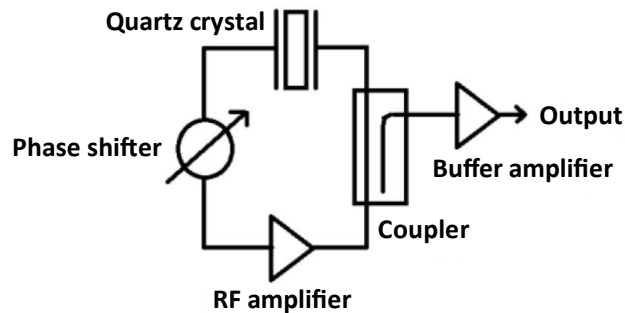


Fig. 2.10. Quartz-crystal oscillator [68]

Development of VHF (very high frequency) crystal oscillators [69] using vacuum-tube amplifiers [70] dominated the 1950s decade. However, vacuum-tube oscillators have limitations in lifespan and maintenance. Efforts were directed towards optimizing single-tube oscillator circuits, driven by the advantage of reduced maintenance compared to their two-tube counterparts. Amplifying this trend, Firth's 1965 design handbook extensively delved into the Pierce circuit and the Butler common-base harmonic circuit [71]. Vacuum tubes allow for substantial voltage swings operating within power supply voltages of 150-300 V. The use of large voltage swings introduced risks such as exceeding the crystal's dissipation limit or inducing fractures in the crystal. The pursuit of efficient oscillator circuits required a delicate balance between maximizing power output and mitigating potential drawbacks associated with vacuum-tube technology [6].

With the advent of transistor and integrated circuit (IC) technologies, the focus shifted towards reoptimizing the oscillator performance. The adoption of scaled size and lower power supply voltages in transistor circuits mitigated problems such as crystal overdrive (large power driven by the crystal), rendering them more manageable.

2.6 Bridge Oscillator for Low Phase Noise

The bridge-stabilized crystal oscillator was disclosed by Meacham in 1934 [7]. The block diagram is illustrated in Fig. 2.11 is comprised of a bridge resonator with four branches (crystal, R_2 , R_1 , and lamp). An error voltage (e) is created at the output of the resonator when R_1 is unequal to R_2 (i.e., the bridge is unbalanced). This can give a steep phase response in the error voltage 'e' at the resonant frequency (as described in Section 1.4.2).

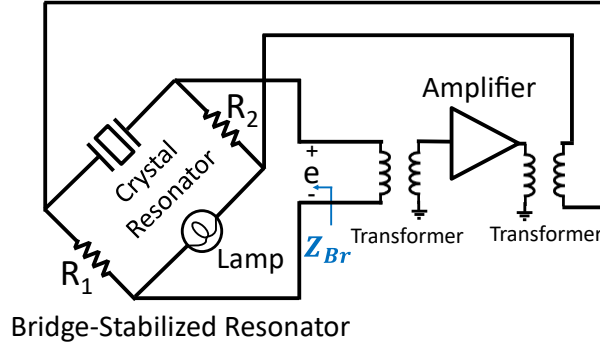


Fig. 2.11. Meacham bridge crystal oscillator [7]

The Meacham bridge oscillator (MBO) was demonstrated as a low-frequency discrete circuit. Other prototypes were published using the MBO topology in high-frequency oscillators. Among them, Sooy, *et. al.*, used a resonant cavity and travelling-wave tube amplifier to build an X-band oscillator [8]. Another work by Papez and Papezova describes a differential circuit with series L-C resonators [72], but in simulation only (i.e., implementation results were not shown). An op-amp version of the MBO oscillator is presented in [9]. Previous work has demonstrated excellent performance with off-chip, high-Q resonators (e.g., crystals, resonant cavity, etc.).

2.7 Summary

This chapter covered the fundamental ideas and theories related to low-phase-noise RF oscillators. The significance of designing a high-Q resonator based on theoretical principles was explained. The literature review included an overview of resonator types like traditional on-chip L-C oscillators and off-chip high-Q crystal oscillators. Finally, the motivation of this work, which is the discrete MBO crystal oscillator from 1934, is outlined along with the design implementation challenges.

Chapter 3

Lumped-element On-chip Passive Design

This chapter describes lumped-element passive design in the 22-nm SOI-CMOS technology. Inductors and capacitors are designed, fabricated, and their performance are characterized. The purpose is to benchmark library models and to develop custom designs for the RF and mm-wave frequency range that may be applied to an integrated bridge oscillator. Two back-end of line (BEOL) metal options are used for this study.

3.1 Inductors

This section describes inductor specifications, designs, and physical parameters. Inductor design and benchmarking are major tasks of this project, as inductors are commonly used in resonators, matching and filter circuits on-chip. In this work, inductors will be used in the design of bridge and the bandpass filter circuits. Spiral inductors of 1-nH and 2-nH values were developed with two different substrate shielding patterns to benchmark the 22-nm SOI-CMOS technology using BEOL options Stack 11 and Stack 19. Stack 11 has three top metal layers of 2.9- μm (LB), 3.3- μm (OI), and 1.04- μm (JA) thickness, whereas Stack19 has 2.9- μm (LB), 3- μm (QB), and 3- μm (QA) thickness top metals.

An important figure of merit for the inductor is the quality factor (Q_{ind}) [73]

$$Q_{ind} = -\frac{\omega_0}{2} \frac{d}{d\omega} \left[\tan^{-1} \left(\frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})} \right) \right] \Big|_{\omega=\omega_0}, \quad (3.1)$$

where ω_0 is the frequency where the derivative is calculated, and Y_{11} is the one-port Y-parameter of the inductor. The ratio of imaginary and real parts of Y_{11} inside the arctan function of eq. (3.1) is very often and incorrectly referred to as the inductor Q-factor in the literature

$$Q_{conv} = \frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})}. \quad (3.2)$$

At the self-resonant frequency (SRF), Q_{conv} is zero, although the actual Q factor (Q_{ind}) is finite.

3.1.1 Stack-11 and Stack-19 inductors

Inductors designed using different BEOL metals and substrate shield types are fabricated in the 22-nm SOI-CMOS technology and characterized. The custom designed inductors are referenced in this thesis by the name: ‘Metal_shieldX_stackY_ZnH’. ‘Metal’ is the metal layer used for the coil, ‘X’ is the shield type (1 or 2 as discussed in Section 3.1.1.1), ‘Y’ is the stack number (11 or 19), and ‘Z’ is the inductance value (1 nH or 2 nH). To compare the performance with inductors available in the PDK library, two inductor layouts with comparable inductance values are selected. They are named ‘Metal_symindp_layout_stackY_ZnH’.

Top-metal LB in Stack 11 is used for one set of designs, as it gives the thickest dielectric separating the coil and the substrate. To increase the effective conductor thickness, LB and OI metals are shorted together (LBOI stack) in a second set of designs. Similar approaches are taken to the design of inductors implemented in Stack 19 where LB and QB are shorted. To take advantage of thicker QB and QA metal layers in Stack 19, a separate set of QBQA stacked inductors are designed. However, the dimensions and number of turns of these stacked metal inductors differ from LB-only planar inductors, to optimize both Q factor and physical area for the same inductance value. Stacking of metals increases the effective conductor thickness and reduces both resistance and inductance of the coil. Because of this, the 1-nH stacked inductors have 3-turns to compensate for the inductance reduction due to the increase in effective metal thickness realized by metal stacking. Physical layouts of the prototype inductors are shown in Fig. 3.1 and Fig. 3.2.

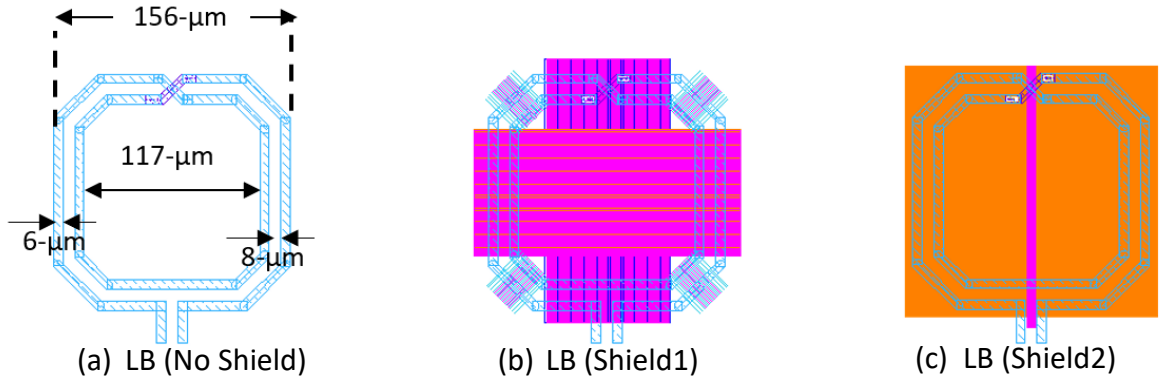


Fig. 3.1. Top view of the physical layouts of 1-nH LB inductors and substrate shields

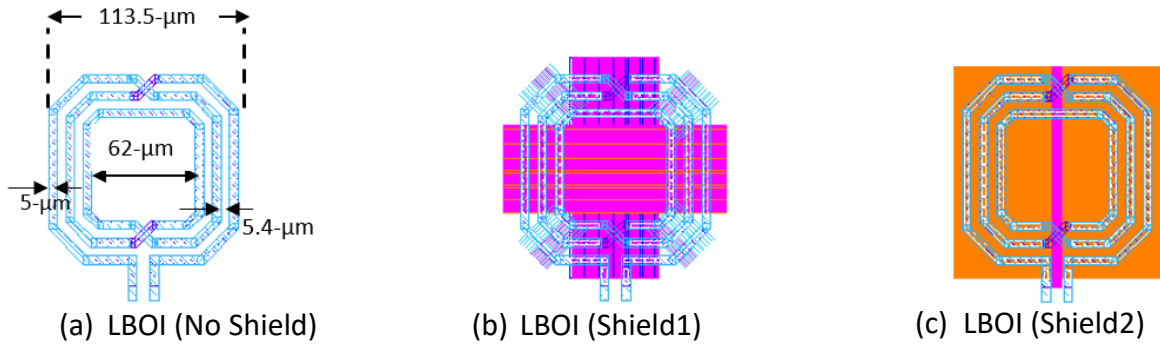


Fig. 3.2. Top view of the physical layouts of 1-nH LBOI stack inductors and substrate shields

3.1.1.1 Inductor shielding

Two different substrate shields are designed. Floating shield1 (Fig. 3.1b and Fig. 3.2b) is designed with overlapped floating shield fingers in C1 and C2 metals. Fingers are placed horizontally, vertically, and at a 45° angle to shield all segments of the coil, as shown in the top view of the physical layouts of Fig. 3.1b and Fig. 3.2b. Floating shield2 (Fig. 3.1c and Fig. 3.2c) is designed with only horizontal fingers implemented in C1 and C2 metals. Floating shield1 offers greater shielding of the coil from the substrate compared to floating shield2 due to the 45° (angled) segments shielding each corner. Simulation results comparing Q_{ind} of shielded and unshielded inductors are illustrated in Fig. 3.3 for the ‘LB_stack11_1nH’ test

structures and the PDK 1-nH inductor. As seen from Fig. 3.3, the floating shield increases the peak Q factor by reducing the substrate loss.

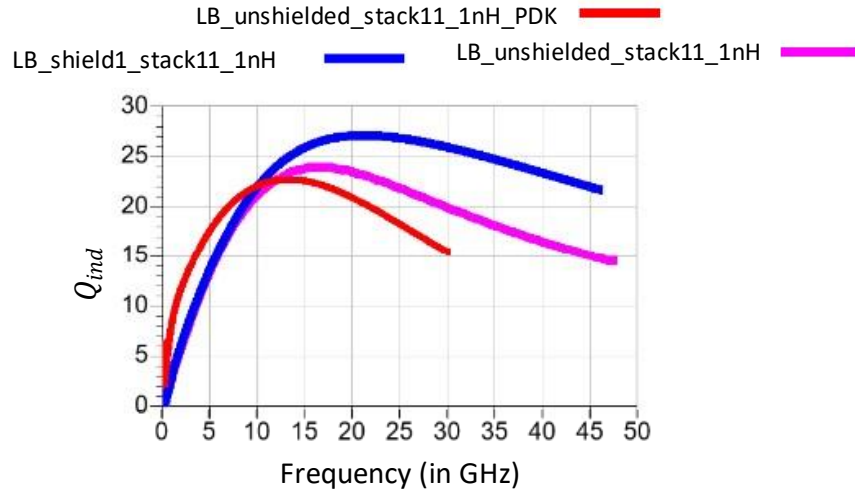


Fig. 3.3. Comparison between shielded and unshielded simulation results for the ‘LB_stack11_1nH’ test structure

3.1.2 Measurement Results

Die photos of inductors designed and implemented using the two different stacks are shown in Fig. 3.4. On-wafer probing is used to measure the 2-port S-parameters of each inductor test structure, which is comprised of a GSGSG (ground-signal-ground-signal-ground) pad set, interconnect, and the inductor.

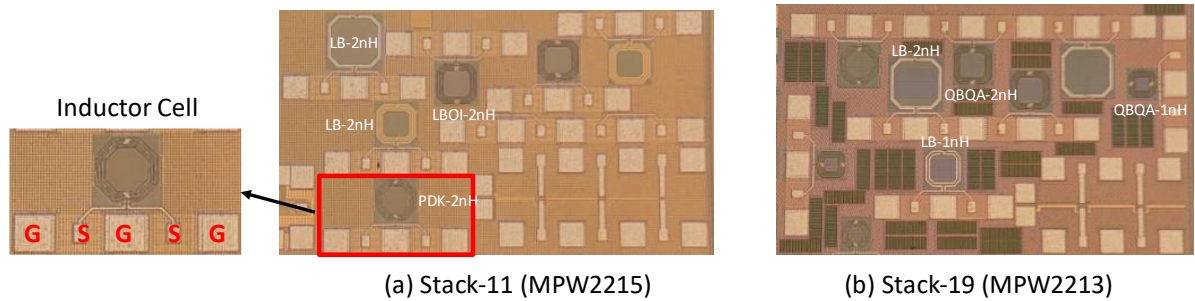


Fig. 3.4. Die photos of the inductors implemented in two different stacks

Thru de-embedding [74] is used to extract the 2-port S-parameters of the inductor from the measured S-parameters of the DUT. Dedicated thru de-embedding structures are fabricated on-chip for this purpose. The de-embedded, 2-port S-parameters are used to determine the inductance and Q.

Fig. 3.5 show Q_{ind} plots of the 1 nH and 2 nH test inductors from deembedded measured data. The performance of inductors from the PDK library for 1-nH and 2-nH are also shown for comparison. They are named ‘LBOI_symin dp_layout_stack11’ in Fig. 3.5a and ‘LBQB_symin dp_layout_stack19’ in Fig. 3.5b. The measured data shows a maximum Q_{ind} of 35 at 11 GHz for a 2-nH inductor (red curve in Fig. 3.5b). These values are 1.2 times better than the library inductors (sky blue curve) as seen from the plots. The network analyser used in measurements shows fluctuations in the data points for high frequency range. This is prominent for very small values of measured data (e.g. resistive ohmic losses of high-Q components). Therefore, the plots in Fig. 3.5 show fluctuations, especially at high frequency.

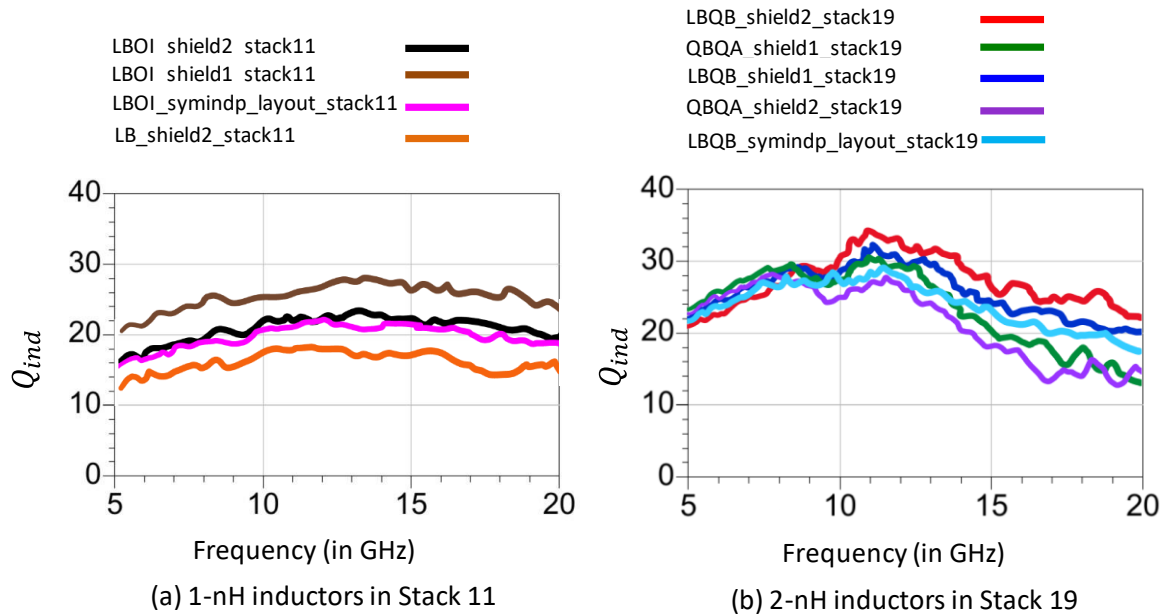


Fig. 3.5. Q_{ind} for 1-nH and 2-nH inductors from measured data

3.1.2.1 Comparison between Stack-11 and Stack-19 results

To compare the performance of Stack-11 and Stack-19 inductors, the Q_{ind} of 2-nH LBOI, LBQB, and QBQA inductors are plotted in Fig. 3.6.

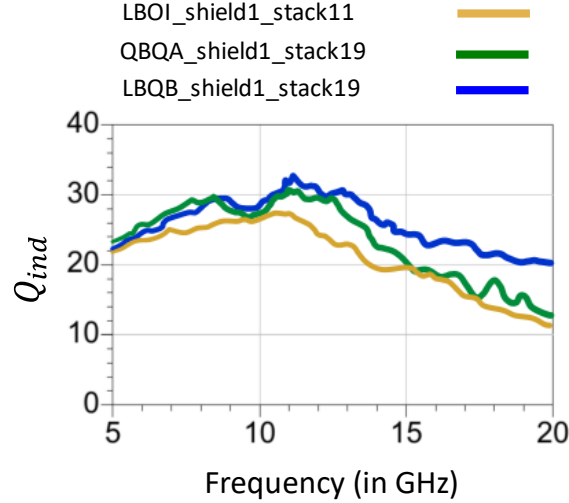


Fig. 3.6. Q_{ind} for 2-nH shield1-type inductors in Stack-11 and Stack-19

From Fig. 3.6, it is clear that shorting the top two metal layers (LBQB) provides a higher peak Q-factor (blue curve) with Stack-19 compared to the results from Stack-11 (LBOI, brown curve). The QBQA metal inductor in Stack-19 (green curve) also has a higher Q-factor at all frequencies compared to the LBOI inductor in Stack-11 (brown curve). Between the LBQB (blue) and QBQA (green) designs, the LBQB coil has a thicker dielectric layer between the conductor and the shield, as it uses the top two metals. Therefore, it demonstrates the benefits of lower parasitic capacitance and substrate loss, resulting in a broader Q peak and higher peak-Q value.

3.1.2.2 Comparison with Simulation

Fig. 3.7 compares measured and simulated performance for a 2-nH LBOI shield2 inductor. Simulations are performed using the Keysight MomentumTM tool. Measurements agree well with simulations. The agreement between the measured data of other inductors in Fig. 3.5b and their Momentum simulations is similar to that in Fig. 3.7.

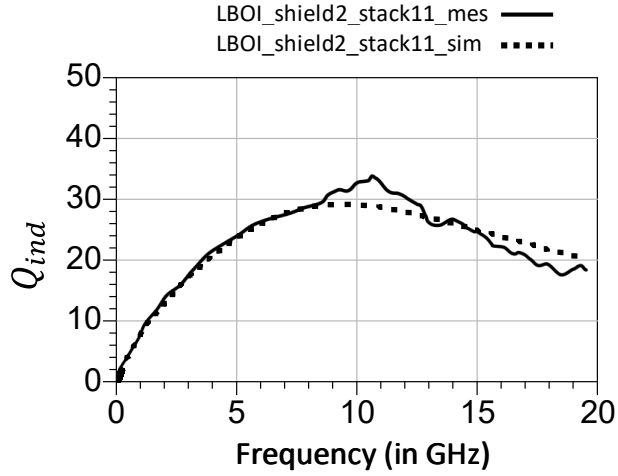


Fig. 3.7. Measurement vs. simulation results for 2-nH inductor

3.1.3 Summary of Measurement Results

Measurement results for the custom designed inductors are summarized in Table 3.1 and Table 3.2. Measurements were performed using the Keysight™ N5245A PNA-X Microwave Network Analyzer. The system was calibrated to the probe-tip reference planes using the SOLT calibration method [75]. Due to testchip area limits, only 2-nH inductor designs are fabricated in Stack 19. The self-resonant frequency is calculated from electromagnetic simulation. As seen from Table 3.1 and Table 3.2, there is a trade-off between inductor Q_{ind} and SRF.

Table 3.1. Measurement results for 1-nH inductors

Inductor type	Stack option	Metal	Shield type	Inductance at 10 MHz (nH)	Differential Peak Q-factor	Frequency at peak Q (GHz)	SRF (GHz) (from simulation)
Custom	Stack-11	LB	Shield2	1.018	16	13.9	45.426
Custom	Stack-11	LBOI	Shield1	1.026	27	13	34.210
Custom	Stack-11	LBOI	Shield2	1.035	22.5	13.1	32.110
PDK model	Stack-11	LBOI	Grounded shield	1.071	21.6	14	28.910

Table 3.2. Measurement results for 2-nH inductors

Inductor type	Stack option	Metal	Shield type	Inductance at 10 MHz (nH)	Differential Peak Q-factor	Frequency at peak Q (GHz)	SRF (GHz) (from simulation)
Custom	Stack-11	LBOI	Shield1	2.013	26.9	11.0	18.128
Custom	Stack-19	LBQB	Shield1	2.013	32.4	11.2	20.128
Custom	Stack-19	QBQA	Shield1	2.040	30.1	11.14	19.085
Custom	Stack-19	LBQB	Shield2	2.065	34.9	11.0	19.972
Custom	Stack-19	QBQA	Shield2	2.050	26.3	12.1	18.770
PDK model	Stack-19	LBQB	Grounded shield	2.015	29.5	11.8	17.088

In general, inductors in Stack 19 have higher peak Q-factors than Stack 11 inductors for a comparable SRF due to the thicker metals in Stack 19. Shorting metal layers to implement the coil improves performance. Both LBQB and QBQA structures in Stack 19 provide higher peak Q and SRF compared to LBOI structure in Stack 11. Floating shield1 increases the Q for LB inductors, whereas floating shield2 is slightly better for LBOI, LBQB and QBQA inductors, as these stacked inductors use multiple top metals, reducing the oxide thickness between the coil and shield. Therefore, lower shield metals used by shield2 reduce the parasitic capacitance and improves the Q factor.

3.2 Capacitors

Capacitors are used in the proposed bridge circuit, L-C filter, and tuning control circuits. Metal-oxide-metal (MOM) structures are formed with oxide sandwiched between two or more metal plates [37]. MOS varactors are also used widely because their capacitance can be voltage controlled. However, they have lower Q-factor than MOM capacitors. Metal capacitors also

offer better linearity, high Q-factor, and smaller variation with respect to temperature changes than MOS varactors.

3.2.1 MOM and Custom Designed Capacitors

Stack 11 is used to design capacitor values greater than 500 fF for benchmarking purposes. The capacitor Q factor may be improved by applying custom designed floating substrate shields [76]. Three capacitors are developed in this work: two interdigitated metal-finger capacitors similar to the PDK MOM capacitors (as in Fig. 3.8b), and a vertical parallel plate, full-custom capacitor (shown in Fig. 3.8a).

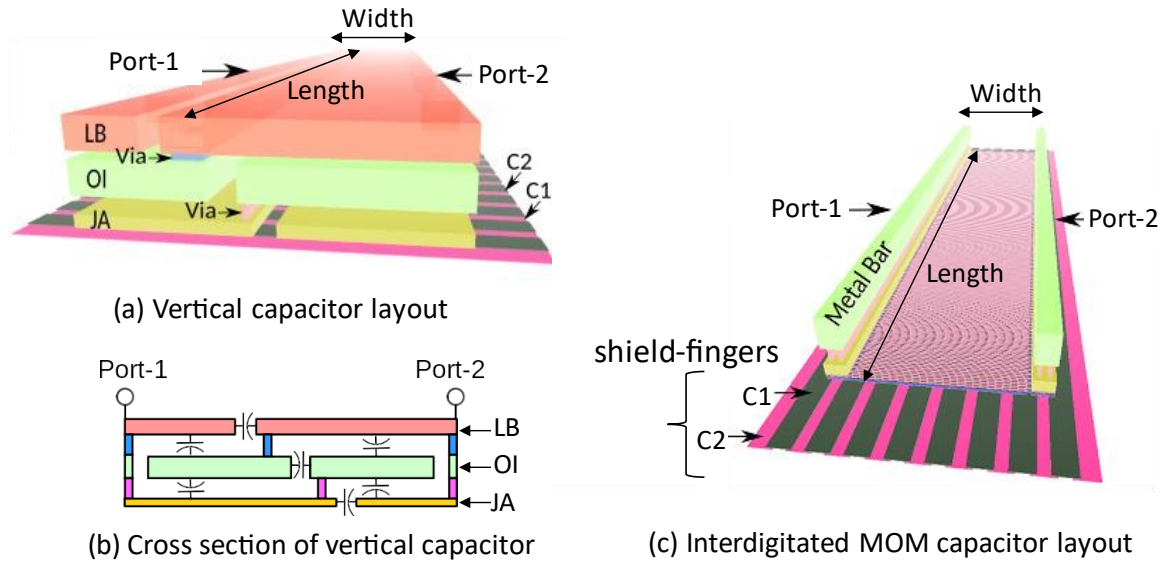


Fig. 3.8. Interdigitated MOM and custom vertical parallel plate capacitor layouts

The two MOM capacitor prototypes are named ‘MOM_C15’ and ‘MOM_C35’. The vertical, custom-drawn capacitor is named ‘Vertical_LBOIJA’. MOM_C15 and MOM_C35 are built with interdigitated C1 to C5 and interdigitated C3 to C5 lower metal layers (thickness less than 90 nm), respectively. MOM_C15 has a cell width of 16 μm and length of 54 μm , and MOM_C35 has a cell width of 16 μm and length of 89 μm . In both cases, the metal fingers of the capacitor are vialess, and all fingers connect to a bar on the side which shorts the fingers together (see Fig. 3.8c). The Vertical_LBOIJA uses three, thick top-metal layers to form plates

that are interdigitated horizontally, and overlaid (or stacked) vertically as shown in Fig. 3.8b. The cell width and length are 33 μm and 150 μm , respectively.

3.2.2 Performance Improvement

The electrical performance of a capacitor is typically characterized by its series capacitance, C and quality factor, Q . These are extracted from the admittance seen across the capacitor terminals as a one-port to ground

$$C = \text{imag}(Y_{11})/2\pi f, \quad (3.3)$$

$$Q = -\frac{\text{imag}\left(\frac{1}{Y_{11}}\right)}{\text{real}\left(\frac{1}{Y_{11}}\right)}. \quad (3.4)$$

The equivalent admittance of the capacitor as a 1-port network (see Fig. 3.11b) is Y_{11} , and f is the frequency. Another parameter of interest to circuit designers is the self-resonant frequency (SRF), which defines the highest useable frequency of operation as a capacitor. Depending on the structure, there are trade-offs between Q , SRF, and chip area occupied by the capacitor.

3.2.2.1 Layout Modification for Low Dissipation

The capacitor physical layout and dimensions are designed to optimize the Q factor. A simple lumped-element equivalent circuit model for the capacitor is shown in Fig. 3.9.

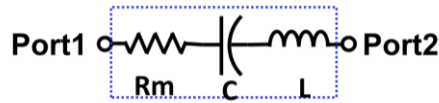


Fig. 3.9. R-L-C lumped-element model for a capacitor

The main component is C , which represents the desired capacitance. Ohmic loss is modelled by series resistance R_m , which arises from losses in the metal fingers or plates of the capacitor. The parasitic series inductance of the physical layout is modelled by L .

Q is related to the series capacitance (C) and series resistance (R_m) by the equation (ignoring L)

$$Q = \frac{1}{\omega R_m C}, \quad (3.5)$$

where ω is the radian frequency. For a fixed capacitance, Q is improved by reducing R_m . For example, the metal bar that connects all the fingers to each port of a MOM capacitor (in Fig. 3.8b) is a major contributor to R_m . Therefore, the dimensions are optimized to minimize R_m . Moreover, a stack of thick, top metal layers is used to reduce the resistance of the metal bars. This comes at the cost of SRF, as series inductance (L in Fig. 3.9) is added with this approach.

Another parameter that gives a clear ranking of the capacitor performance is the time constant (τ). The time constant is the product of series resistance (R_m) and capacitance (C), and is independent of frequency, unlike Q , which is the inverse of the product of radian frequency and the time constant. The lower the time constant, the better the performance.

3.2.2.2 Substrate Shielding

Various shielding options, such as N-well and poly shielding are provided for the PDK capacitor p-cells. In this work, a floating substrate shield that does not require an explicit ground connection (similar to the inductor and TL floating shield pattern) is designed, as shown in Fig. 3.8b. The shield is comprised of thin and narrow floating metal fingers on lower-level metals such as C1 and C2, which overlap with each other. Finger width and gap of the shield metals were optimized from simulation to be 2 μm of finger width, 1 μm gap and 0.5 μm of overlap. Simulation results comparing the performance between shielded and unshielded capacitors are plotted in Fig. 3.10 for the ‘Vertical_LBOIJA’ capacitor. As seen from Fig. 3.10, the floating shield reduces the time constant τ (thereby increasing Q) by lowering the substrate loss, especially around the frequency of interest for the oscillator circuit (8 GHz).

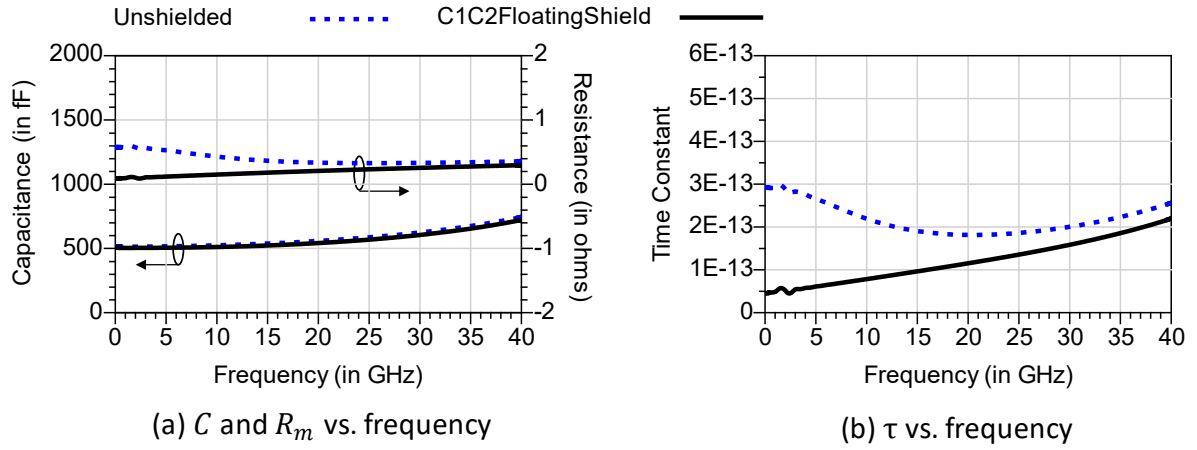


Fig. 3.10. Comparison between shielded and unshielded simulation results for the 'Vertical_LBOIJA' test structure

3.2.3 Measurement Results

All capacitors are fabricated with GSG pads connected to both sides of the capacitor to create the device under test (DUT) for characterization. Measurements were performed using the Keysight™ N5245A PNA-X Microwave Network Analyzer. The system was calibrated to the probe-tip reference planes using the SOLT calibration method [75]. Measurements of the 2-port S-parameters are taken on each cell comprised of the left GSG pad, capacitor test structure, and right GSG pad connected in series, as illustrated in Fig. 3.11. The measurement setup is shown in Fig. 3.11a.

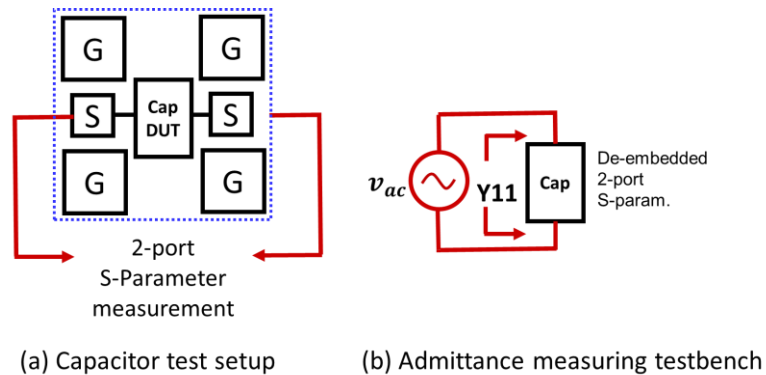


Fig. 3.11. Test setup for capacitor measurements

Thru de-embedding [74] is used to extract the 2-port S-parameters of the capacitor from the measured S-parameters of the DUT. Dedicated thru de-embedding structures are fabricated on-chip for this purpose. The de-embedded, 2-port S-parameters are used to compute Y_{11} (see Fig. 3.11b) extract C , R_m , and Q using eqs. (3.3) to (3.5). Fig. 3.12 shows the die photo of the fabricated test structures.

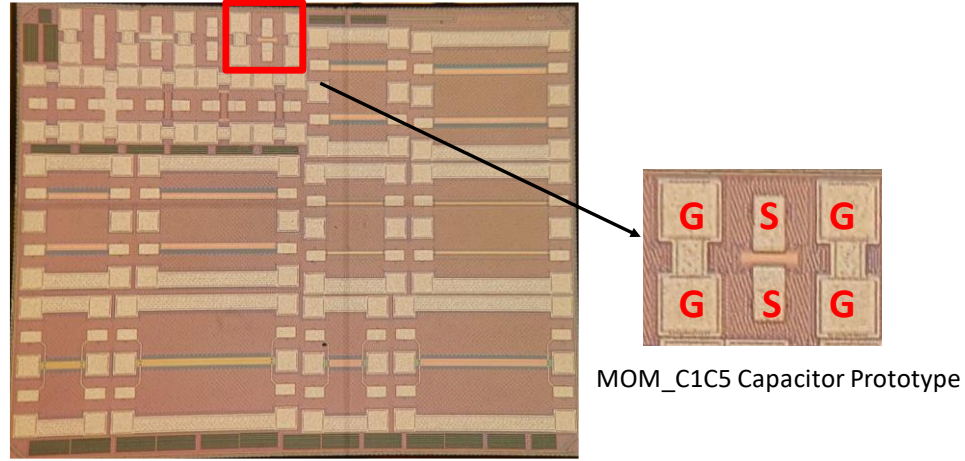


Fig. 3.12. MPW2225 die photo for Stack 11 capacitors

3.2.3.1 Comparison with PDK Capacitors

Measurement results are shown in Fig. 3.13. The capacitance C of the measured capacitors are 550 fF, as seen from Fig. 3.13a. 'MOM_C3C5' (red) and 'Vertical_LBOIJA' (light-orange) provide higher SRF than 'MOM_C1C5', as predicted from Fig. 3.13a. This is because they use thick top metals, which reduces the electrode series resistance and increases the oxide thickness between the capacitor electrodes and the shield, thereby reducing the parasitic capacitance.

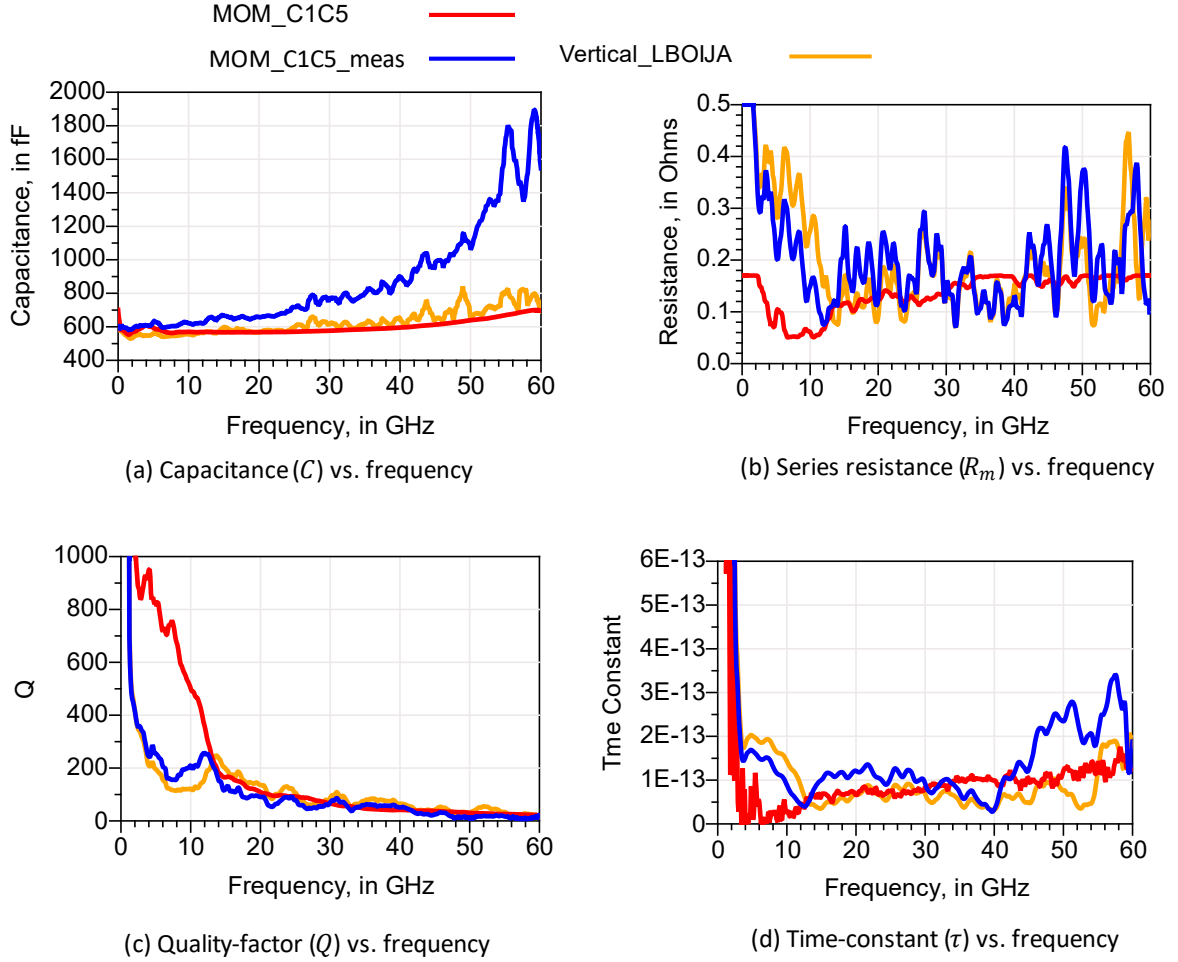


Fig. 3.13. Measurement results for the capacitor test structures

Fig. 3.13c and Fig. 3.13d show the Q factor and time constant (τ) measurements of the proposed capacitors. The red τ trace of MOM_C3C5 shows the lowest value, making it the best performer up to 10 GHz. This gives a Q of more 500 below 10 GHz. The custom-designed vertical capacitor offers better τ at higher frequency. For example, improvement of τ by a factor of 3 is seen for the vertical test structure measurements at 50 GHz, as compared to the MOM_C3C5 interdigitated capacitor. The network analyser used in measurements shows fluctuations in the data points for high frequency range, especially for very small values of measured data (e.g. resistive ohmic losses of high- Q components). Therefore, the resistance

plots in Fig. 3.13b have more fluctuations. Multiple measurements taken in a smaller frequency range and averaging them could give smoother plots.

3.2.3.2 Comparison with Simulation

Fig. 3.14 compares measured and simulated performance for the Vertical_LBOIJA capacitor up to 60 GHz. Simulations are performed using the Keysight Momentum™ tool. Measurements agree well with simulations across the 60-GHz frequency range.

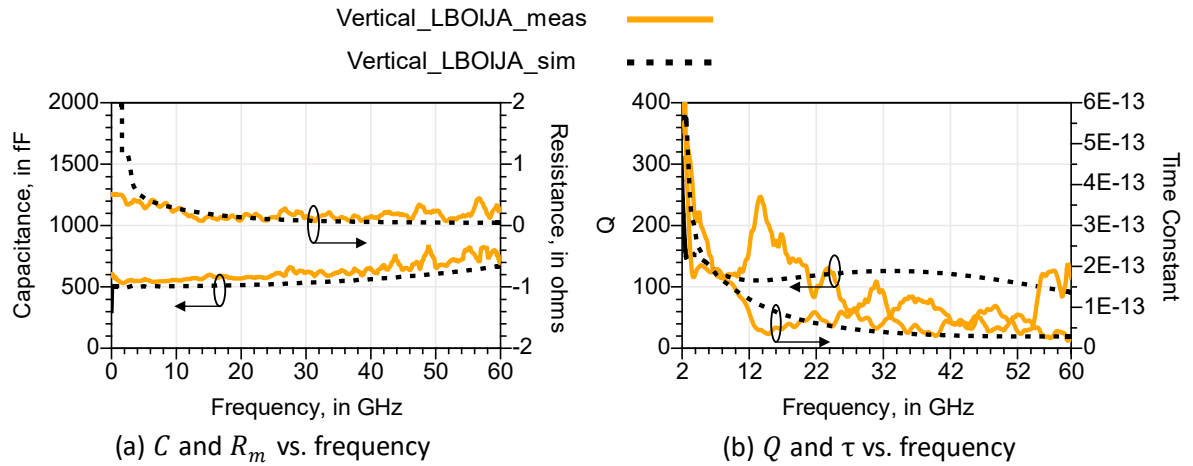


Fig. 3.14. Capacitor measurement vs. simulation results

3.2.4 Summary of Measurement Results

The performance of the capacitors designed in this work is summarized in Table 3.3.

Table 3.3. Summary of 500-fF capacitor results

Capacitor type	Metal layers used	Capacitance (fF) at 10 GHz	Resistance (Ω) at 10 GHz	Q factor at 10 GHz	Time constant at 10 GHz	SRF from simulation (GHz)	Area ($\mu\text{m} \times \mu\text{m}$)
MOM	C1 to C5	633.877	0.147	204	1×10^{-13}	88	16×54
MOM	C3 to C5	601.038	0.067	498	9×10^{-14}	95	16×90
MIM	LB, OL, JA	515.726	0.240	112	1.4×10^{-13}	>100	33×150

It is seen from the 5th and 8th columns of Table 3.3 that there is a trade-off between Q and the physical size of the MOM capacitors. MOM_C3C5 capacitor, designed carefully with regard to layout and shield dimensions, gives the highest Q (498 at 10 GHz) at the cost of larger physical size.

3.3 Summary

This chapter presented the design of high-Q on-chip inductors and capacitors fabricated in 22-nm FD-SOI-CMOS technology. Layout improvement and floating substrate shielding were demonstrated in Stack-11 and Stack-19 BEOL technology options that showed improved Q factor. Measurement results show a Q factor of 35 at 11 GHz for 2-nH inductor and a Q factor of 500 at 10 GHz for a 601-fF capacitor making them suitable for applications in high-Q, narrowband resonators. Custom design of a 515-fF capacitor utilizing thick metals offers 3 times better Q factor at higher frequencies (> 30 GHz) compared to the traditional interdigitated MOM capacitor, as verified by the measurement data.

Chapter 4

Bridge Resonator Design

A crystal bridge resonator was used by Meacham in 1934 to demonstrate a discrete, low-frequency oscillator (see Fig. 2.11) [7]. Compared to a series or parallel L-C resonator, a bridge resonator holds the potential to enhance the Q-factor, thus forming the motivation behind this study. Bridges also find applications in RF power measurement, high-accuracy sensing of voltage and impedance, component characterization, and more. This work implements a fully-integrated L-C bridge resonator, harnessing the high-Q potential of the Meacham's bridge topology. It is implemented in 22-nm SOI-CMOS technology. It is specifically targeted towards narrowband applications and aims to improve upon the signal-to-noise performance of Meacham's circuit for RF and mm-wave frequency applications.

4.1 Bridge Resonator Circuit

The proposed bridge resonator is shown in Fig. 4.1. It is comprised of four arms, two of them incorporating resonators and the remaining two (i.e., Z_{b1} and Z_{b2}) forming balancing arms. Two series resonators with inductor L_r in series with a capacitor C_r are used. The resonant frequency (ω_o) of the series resonator is

$$\omega_o = \frac{1}{\sqrt{L_r C_r}}. \quad (4.1)$$

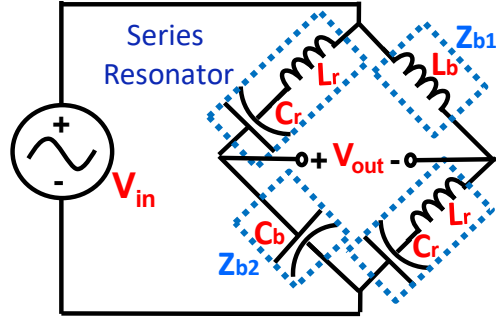


Fig. 4.1. Proposed bridge circuit

Balancing branches Z_{b1} and Z_{b2} may be designed in two ways. Meacham's design [7] used two resistors with slightly different values (e.g., $Z_{b1}(\omega_{osc}) = R_b$ and $Z_{b2}(\omega_{osc}) = n_r R_b$, where n_r is a scaling constant). However, resistors add thermal noise from the ohmic losses of R_b and $n_r R_b$. An alternative is to use an inductor ($Z_{b1}(\omega_{osc}) = jX_b$), and a capacitor ($Z_{b2}(\omega_{osc}) = -jX_b$) to cancel the reactive components in the voltage transfer function ($G_{br} = V_{out}/V_{in}$) at ω_{osc} . This way, a real value of V_{out} is achieved at resonance such that Barkhausen's criteria for oscillation are satisfied. As the real parts of the inductive and capacitive impedances are small for high-Q L_r and C_r , the signal-to-noise ratio (SNR) is improved by this approach.

Fig. 4.2 compares the magnitude ($|G_{br}|$) and phase responses ($\varphi(\omega)$) between resistor and L-C balancing of an 8-GHz bridge circuit example, close to but not exactly at balance, for an open-circuit output load. As depicted by Fig. 4.2b, the L-C approach (red solid curve) produces a sharper change in the phase response at resonance than the resistor approach (blue dotted curve) for the gain of 0.01 V/V in Fig. 4.2a. A discontinuity in phase occurs when the circuit transitions from leading to lagging due to a sign change of V_{out} as the frequency is swept from below to above the resonant frequency. The rapid phase change results in a high Q factor, as Q depends on the derivative of the phase response according to $\left[\frac{\omega_{osc}}{2} \cdot \frac{d\varphi(\omega)}{d\omega} \right]$ [77].

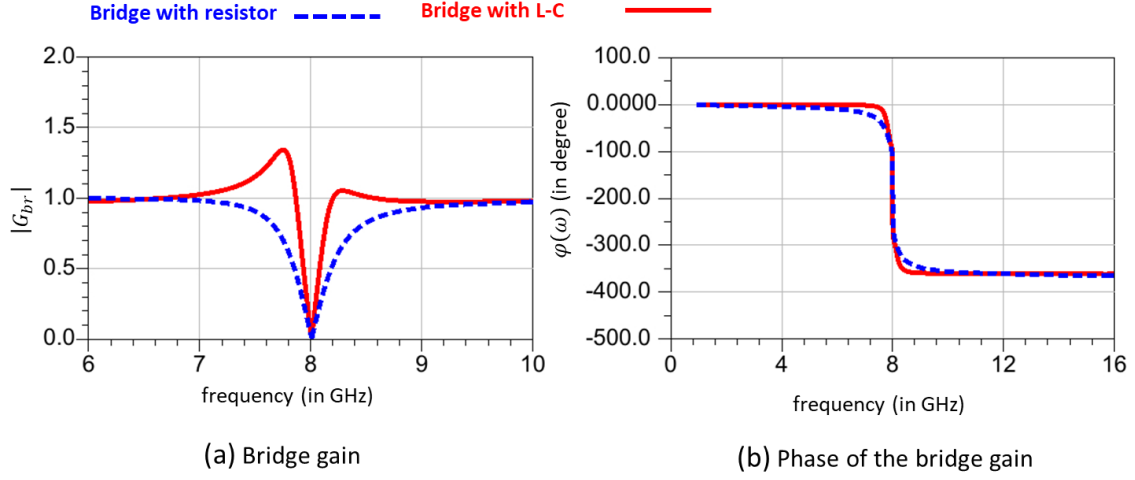


Fig. 4.2. Gain and phase responses of resistor and L-C type bridges

4.2 Design and Performance Characterization

This section details the performance parameters (e.g., gain, Q-factor, SNR etc.) for the proposed bridge resonator circuit.

4.2.1 Voltage Transfer Function and Quality Factor

Assuming that the equivalent impedance of the resonator is Z_{rsn} (see Fig. 4.1), the voltage transfer function (G_{br}) of the bridge circuit is derived from the voltage divider rule

$$G_{br} = \frac{V_{out}}{V_{in}} = \frac{Z_{rsn}}{Z_{rsn} + Z_{b1}} - \frac{Z_{b2}}{Z_{rsn} + Z_{b2}}. \quad (4.2)$$

Substituting jX_b , and $-jX_b$ for Z_{b1} and Z_{b2} , respectively, in eq. (4.2) at frequency ω_{osc} gives

$$G_{br}(\omega_{osc}) = \frac{Z_{rsn}(\omega_{osc})^2 - X_b^2}{Z_{rsn}(\omega_{osc})^2 + X_b^2}. \quad (4.3)$$

The resonator impedance (Z_{rsn}) is defined as

$$Z_{rsn} = R_{rsn} + jX_{rsn}, \quad (4.4)$$

$$\text{and } Z_{rsn}^2 = R_{rsn}^2 + j2R_{rsn}X_{rsn} - X_{rsn}^2, \quad (4.5)$$

where R_{rsn} and X_{rsn} are the real and imaginary parts of Z_{rsn} , respectively. At resonance, the reactive part approaches zero, and Z_{rsn} becomes real (i.e., $Z_{rsn}(\omega_{osc}) = R_{rsn}$). The magnitude of the bridge gain at resonance from eq. (4.3) is therefore

$$|G_{br}(\omega_{osc})| = \frac{|R_{rsn}^2 - X_b^2|}{R_{rsn}^2 + X_b^2} = \frac{\Delta}{R_{rsn}^2 + X_b^2}, \quad (4.6)$$

where Δ is the difference between R_{rsn}^2 and X_b^2 . The gain, $G_{br}(\omega_{osc})$, becomes zero for X_b equal to R_{rsn} , resulting in a zero error voltage (V_{out}) at ω_{osc} . This is called the balanced state.

The phase response of G_{br} , $\varphi(\omega)$ is

$$\begin{aligned} \varphi(\omega) &= \angle G_{br}(\omega) = \angle \left[\frac{Z_{rsn}(\omega)}{Z_{rsn}(\omega) + Z_{b1}(\omega)} - \frac{Z_{b2}(\omega)}{Z_{rsn}(\omega) + Z_{b2}(\omega)} \right] \\ &= \tan^{-1} \left[\frac{\text{Im}(G_{br}(\omega))}{\text{Re}(G_{br}(\omega))} \right] = \tan^{-1} v(\omega), \end{aligned} \quad (4.7)$$

where $v(\omega)$ is

$$v(\omega) = \frac{\text{Im}(G_{br}(\omega))}{\text{Re}(G_{br}(\omega))}. \quad (4.8)$$

The Q-factor of the bridge circuit can be determined from $\varphi(\omega)$ as [77]

$$\begin{aligned} Q_{br} &= \frac{\omega_{osc}}{2} \cdot \frac{d\varphi(\omega)}{d\omega} = \frac{\omega_{osc}}{2} \cdot \frac{d[\tan^{-1} v(\omega)]}{d\omega} \\ &= \frac{\omega_{osc}}{2} \cdot \frac{1}{1 + |v(\omega)|^2} \frac{dv(\omega)}{d\omega}. \end{aligned} \quad (4.9)$$

Eq. (4.9) is derived using the trigonometric arctan differentiation formula. In the vicinity of resonance, $|v(\omega)|$ is very small for a low-loss resonator. Therefore, $\frac{1}{1+|v(\omega)|^2}$ can be assumed to be unity in eq. (4.9) when computing the phase. Substituting eq. (4.5) in (4.3), and neglecting the second-order reactive term (X_{rsn}^2) in the vicinity of resonance, $v(\omega \rightarrow \omega_{osc})$ is found to be

$$v(\omega \rightarrow \omega_{osc}) = \frac{Im(G_{br}(\omega \rightarrow \omega_{osc}))}{Re(G_{br}(\omega \rightarrow \omega_{osc}))} = \frac{4R_{rsn}X_{rsn}X_b^2}{(R_{rsn}^2 + X_{rsn}^2)^2 - (X_b^2)^2}. \quad (4.10)$$

Substituting eq. (4.10) in eq. (4.9) gives

$$\begin{aligned} Q_{br,ser} &= 2\omega_{osc}R_{rsn}X_b^2 \cdot \frac{d \left[\frac{X_{rsn}}{(R_{rsn}^2 + X_{rsn}^2)^2 - (X_b^2)^2} \right]}{d\omega} \\ &= 2\omega_{osc}R_{rsn}X_b^2 \cdot \frac{d}{d\omega} \left[\frac{X_{rsn}}{f_d} \right], \end{aligned} \quad (4.11)$$

where f_d is the denominator of $v(\omega \rightarrow \omega_o)$. Using the differential quotient formula, the derivative of $\frac{d}{d\omega} \left[\frac{X_{rsn}}{f_d} \right]$ is calculated

$$\frac{d}{d\omega} \left[\frac{X_{rsn}}{f_d} \right] = \frac{f_d \cdot \frac{dX_{rsn}(\omega)}{d\omega} - X_{rsn}(\omega) \cdot \frac{df_d}{d\omega}}{f_d^2}. \quad (4.12)$$

At resonance, $X_{rsn}(\omega_o)$ is ideally zero, which gives

$$\frac{d}{d\omega} \left[\frac{X_{rsn}}{f_d} \right] \cong \frac{1}{f_d} \cdot \frac{dX_{rsn}(\omega)}{d\omega}. \quad (4.13)$$

The reactance (X_{rsn}) of the series resonator is the series combination of the coil and the capacitor reactances. Assuming that ω^2 is $1/L_r C_r$ in the vicinity of ω_{osc} ,

$$\frac{dX_{rsn}(\omega)}{d\omega} = \frac{d \left[\omega L_r - \frac{1}{\omega C_r} \right]}{d\omega} = L_r + \frac{1}{\omega^2 C_r} \cong 2L_r. \quad (4.14)$$

Substituting eq. (4.14) and (4.13) in eq. (4.11), $Q_{br,ser}$ for the series-resonator bridge at resonance is calculated as follows

$$\begin{aligned} Q_{br,ser}(\omega \rightarrow \omega_{osc}) &= 2\omega_{osc} R_{rsn} X_b^2 \cdot \frac{1}{f_{d(\omega \rightarrow \omega_{osc})}} \cdot \frac{dX_{rsn}(\omega)}{d\omega} \\ &= 2\omega_{osc} R_{rsn} X_b^2 \cdot \frac{2L_r}{f_{d(\omega \rightarrow \omega_o)}} \cong \frac{2\omega_{osc} R_{rsn} X_b^2 L_r}{(R_{rsn}^2)^2 - (X_b^2)^2}. \end{aligned} \quad (4.15)$$

Equation (4.15) predicts that there is a trade-off between Q_{br} and gain. Increasing Δ increases $|G_{br}(\omega_o)|$ in eq. (4.3) but degrades $Q_{br,ser}$.

4.2.2 Noise Performance

Noise performance of the bridge circuit is characterized by signal-to-noise ratio (SNR). Fig. 4.3 shows equivalent bridge circuit with noise generators assuming resistors R_{rsn} , R_{b1} and R_{b2} in the arms as the sources of thermal noise.

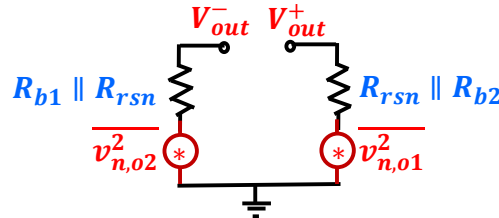


Fig. 4.3. Noise source representation for four resistors in the Meacham bridge

The output referred mean-square noise voltages $\overline{v_{n,o1}^2}$ at the negative output node, and $\overline{v_{n,o2}^2}$ at the positive output are determined from superposition for each noise contribution

$$\overline{v_{n,o1}^2} = (\overline{i_{nb1}^2} + \overline{i_{nr}^2}) \cdot |R_{b1} \parallel R_{rsn}|^2, \quad (4.16)$$

$$\overline{v_{n,o2}^2} = (\overline{i_{nb2}^2} + \overline{i_{nr}^2}) \cdot |R_{b2} \parallel R_{rsn}|^2, \quad (4.17)$$

where $\overline{i_{nr}^2}$, $\overline{i_{nb1}^2}$, and $\overline{i_{nb2}^2}$ are mean-square thermal noise currents generated from the resistors R_{rsn} , R_{b1} , and R_{b2} , respectively. The differential, output referred mean-square noise voltage is given by

$$\overline{v_{n,o}^2} = 4kT \cdot \left[(R_{b1} \parallel R_{rsn}) + (R_{b2} \parallel R_{rsn}) - 2\sqrt{(R_{b1} \parallel R_{rsn})(R_{b2} \parallel R_{rsn})} \right]. \quad (4.18)$$

The output SNR of the bridge is given by

$$SNR = \frac{V_{out}^2}{\overline{v_{n,o}^2}} = \frac{V_{in}^2 \cdot |G_{br}|^2}{\overline{v_{n,o}^2}}. \quad (4.19)$$

The Meacham bridge with $R_{b1} = R_b$ and $R_{b2} = n_r R_b$ (where $R_b = R_{rsn}$) has $\overline{v_{n,o}^2}$ of $4kT \frac{R_{rsn}}{2} \left(\frac{3n_r+1}{n_r+1} - \sqrt{\frac{2n_r}{n_r+1}} \right)$ calculated from eq. (4.18). Whereas $\overline{v_{n,o}^2}$ of the proposed L-C circuit calculated from eq. (4.18), assuming that R_{b1} and R_{b2} are significantly smaller than R_{rsn} for high-Q C_b and L_b balancing components (see Fig. 4.1), is given by

$$\overline{v_{n,o}^2} \Big|_{LC} = 4kT \left(\frac{1}{\omega_{osc} C_b Q_C} + \frac{\omega_{osc} L_b}{Q_L} - 2 \sqrt{\frac{L_b}{C_b Q_C Q_L}} \right). \quad (4.20)$$

where Q_C is the Q-factor of the balancing capacitor C_b and is equal to $1/\omega_{osc} C_b R_{b1}$. Parameter Q_L is the Q-factor of the balancing capacitor L_b and is equal to $\omega_{osc} L_b / R_{b2}$.

Therefore, SNR of the L-C bridge circuit, calculated from eq. (4.19), is given by

$$SNR = \frac{V_{in}^2 \cdot |G_{br}|^2}{4kT \left(\frac{1}{\omega_{osc} C_b Q_c} + \frac{\omega_{osc} L_b}{Q_L} - 2\sqrt{\frac{L_b}{C_b Q_c Q_L}} \right)}. \quad (4.21)$$

Equation (4.21) predicts that for a fixed G_{br} , SNR is improved significantly by high-Q balancing components L_b and C_b . For example, for 112-pH L_b with Q_L of 25 and 3-pF C_b with Q_c of 150, SNR is improved by 39 times in the proposed bridge from the resistive bridge with 5- Ω of R_{rsn} , 5- Ω of R_{b1} and 7.2- Ω of R_{b1} for a gain of 0.18 V/V.

4.2.3 Design for High Q

Inductors close to 1.8-nH inductance value, designed in 22-nm SOI CMOS technology, give peak Q factor and a resistance of approximately 5 Ω at 8.5 GHz. Therefore, bridge impedance (R_{rsn}) value is chosen to be 5 Ω at ω_{osc} . The coil size (L_r) is designed to achieve an equivalent resistance of 5 Ω at ω_{osc} . The $Q_{br,ser}$ is therefore greater than 150 in the vicinity of balance ($X_b \approx R_{rsn}$). If a non-zero error voltage is needed at the bridge output at resonance, an X_b greater than R_{rsn} (e.g. 6 Ω for a $G_{br}(\omega_{osc})$ of 0.12 V/V) is required from eq. (4.3). The $Q_{br,ser}$ for 0.12-V/V gain is therefore calculated to be 49, with R_{rsn} of 5 Ω , X_b of 6 Ω , and L_r equal to 1.8 nH.

4.3 Prototype Layout and Performance Verification

The physical layout of the bridge circuit prototype in 22-nm FD-SOI CMOS technology for a 0.12 V/V gain performance is illustrated in Fig. 4.4. The Stack 19 BEOL option is used for the prototype.

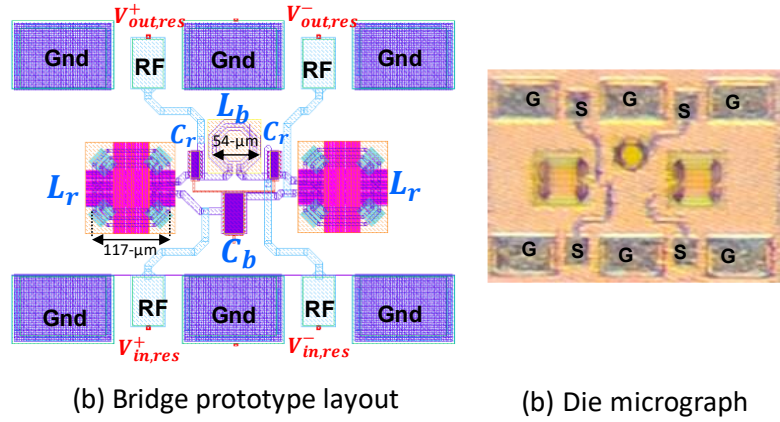


Fig. 4.4. Series bridge resonator prototype

The 1.8-nH resonator coil L_r is implemented as an octagonal 3-turn shielded inductor in QB layer. The outer dimension is 117 μm with 3.5- μm conductor width and 4- μm spacing between conductors. The 220-fF C_r needed to resonate at 8.5-GHz is realized with metal-oxide-metal (MOM) capacitors implemented in M1 to C5 metal layers. The balancing inductor (L_b) is a 2-turn coil in QB layer with 54- μm outer dimension, 6- μm conductor width, and 4- μm spacing between the adjacent conductors. The balancing MOM (PDK cell) capacitor (C_b) is implemented in C1 to C5 metal layers.

Measurement results for the voltage gain of the bridge with R_{rsn} of 5 Ω and X_b of 6 Ω are shown in Fig. 4.5. The magnitude of the measured gain at resonance (Fig. 4.5a) is -18 dB (i.e., $|G_{br}| = 0.12$ at 8.5 GHz). A sharp phase response (i.e., 500°/GHz) is observed at 8.5 GHz (see Fig. 4.5b), which according to a $Q_{br,ser}$ of 50, as shown in Fig. 4.5c.

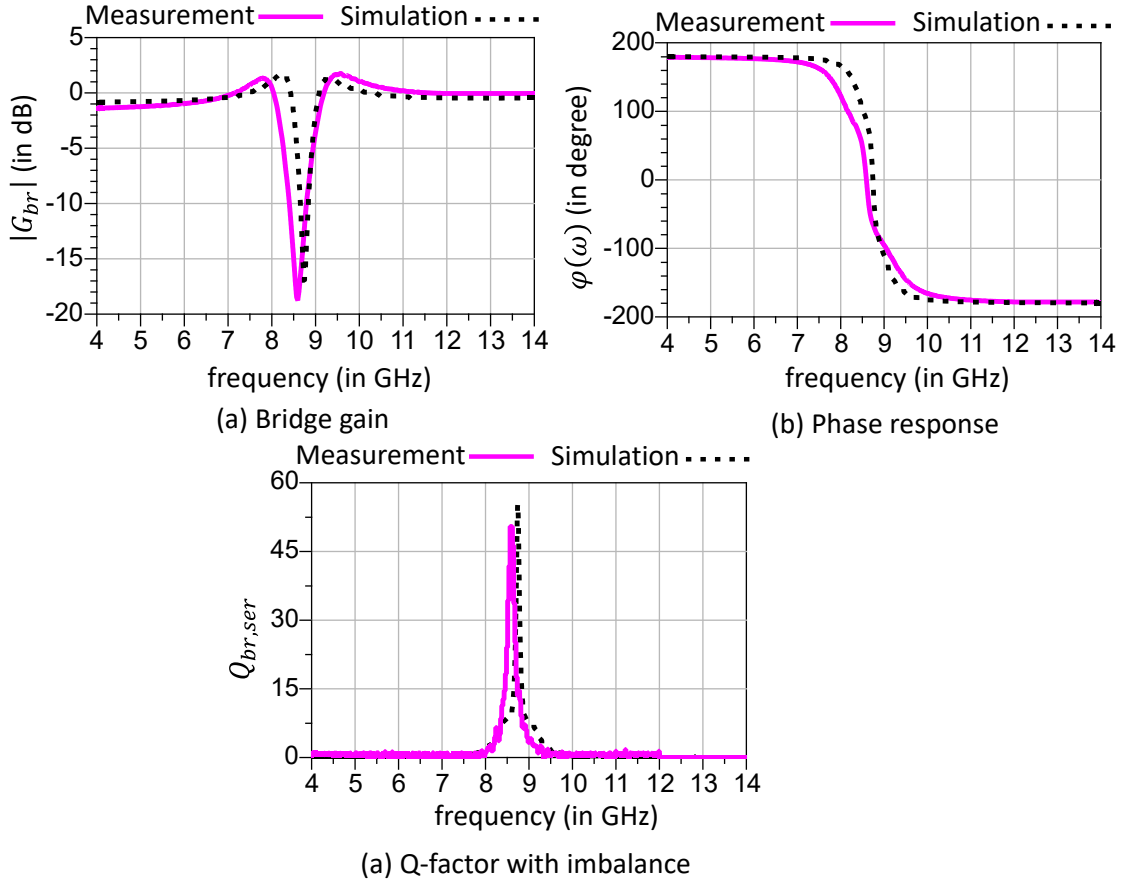


Fig. 4.5. Measurement vs. simulation results of the series bridge circuit

Electromagnetic simulation results are also plotted (dotted curves) in Fig. 4.5 for comparison. It can be seen that the measured data agrees well with the simulation data, given that there are processing variations in the measured samples. The quality factor at ω_{osc} is above 50 for the design, which is 2.7 times larger than Q-factor of the series L-C resonator alone, and 1.9 times larger than the resistive bridge with $5\ \Omega$ for R_{rsn} and R_{b1} and $7.2\ \Omega$ for R_{b1} . This offers the high-Q advantage of the L-C bridge resonator to be used in low-phase-noise and high selectivity oscillators.

4.4 Summary

A fully integrated bridge resonator circuit with high Q-factor (>150 for an open-circuit output) performance is presented in this chapter. The bridge resonator is implemented for series resonance at 8.5 GHz in 22-nm FD-SOI CMOS technology. Measurement results show an open-circuit Q of more than 150 close to its balanced state (i.e., gain close to zero). Equations derived for the Q-factor and gain of the bridge show a trade-off between the two parameters. Therefore, Q drops from 150 (at balance) for a gain larger than zero. A Q of 50 is achieved for a gain of 0.12 V/V. A sharp phase response slope of $500^\circ/\text{GHz}$ for 120 mV of output voltage is achieved due to the high-Q bridge performance, as Q is proportional to the derivative of the phase response with respect to frequency.

Chapter 5

High-Q Transmission Line Design

This chapter describes the design of high-Q ($Q > 100$) transmission lines and their performance in the 22-nm SOI-CMOS technology. The purpose is to verify and model the performance of custom designs across a broad range with a special focus on narrow-band filter optimization, and benchmark the new designs against a state-of-the-art PDK library model.

The drive to build higher performance RF circuits in the millimetre-wave (mm-wave) frequency bands (30 GHz-300 GHz, in air) motivates electrical modelling of transmission lines on a silicon chip. Transmission lines (TLs) are used as interconnects on-chip and at chip boundaries, and to implement matching networks, inductors, and transformers on an integrated circuit (IC) [78]. They are also used as differential interconnects in this thesis. Signal attenuation increases with frequency due to phenomena such as the skin effect, and substrate loss [27], [79]. The Q-factor figure of merit (Q_{TL}) characterizes insertion loss of the TL for a given phase shift [80].

This study benchmarks the performance of on-chip TLs fabricated in the 22-nm SOI-CMOS technology. Coupled transmission lines are designed with optimized physical layouts and shielding to achieve improved Q-factor (4.5 times their non-shielded counterparts at 25-GHz) for differential applications. Also, it is shown that a peak Q greater than 100 is achievable across a narrow band of frequency through proper design of the line. The peak in Q-factor arises from a dip in the attenuation constant (α) of the transmission line at the desired frequency. The dip is caused by current induced in the shield fingers. A new lumped-element equivalent circuit model is also developed for design and simulation purposes.

5.1 Balanced transmission line

Balanced transmission lines provide a send and return path in a symmetrical physical layout, as shown in Fig. 5.1a.

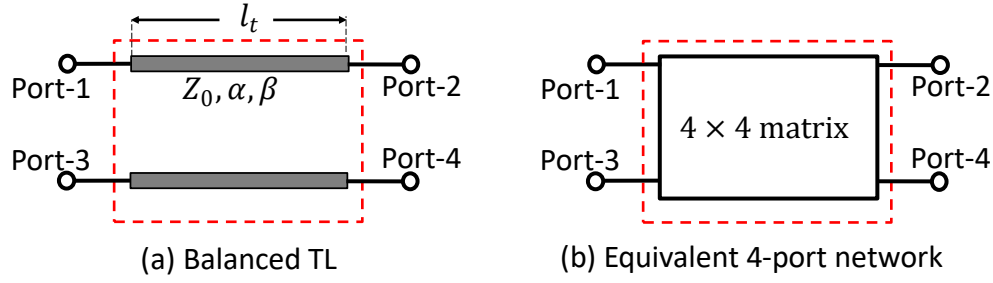


Fig. 5.1. Balanced 4-port transmission line

The electrical performance of a transmission line is characterized by its attenuation constant (α), phase constant (β), and characteristic impedance (Z_0). These are extracted from the Y and Z balanced two-port parameters (measured from the 4-port network in Fig. 5.1b) of the line from the relations

$$Z_0 = \sqrt{\frac{Z_{11}}{Y_{11}}}, \quad (5.1)$$

$$\gamma = \tanh^{-1}\left(\frac{1}{Y_{11}Z_0}\right) = \alpha + j\beta, \quad (5.2)$$

where Y_{11} is measured from the 4x4 Y-matrix of the 4-port device, and γ is the propagation constant. All parameters in eq. (5.1) and eq. (5.2) are per unit length of the transmission line. Assuming propagation in the quasi-transverse electromagnetic (Q-TEM) mode [81], Q-factor Q_{TL} can be defined in terms of frequency (f), α , and the velocity of the travelling wave, v_p

$$Q_{TL} = \frac{\pi f}{\alpha v_p} = \frac{\beta}{2\alpha}. \quad (5.3)$$

For Q-TEM propagation, Fig. 5.2 illustrates the *rlgc* lumped-element circuit model for 3 sections of a balanced transmission line, where Δx is the length of each section. For 3 section model, the total length of the transmission line (l_t) is equal to $3\Delta x$. For a quarter-wave line, l_t is equal to $v_p/4f$. The number of sections used to model a line depends on the frequency range for the application. The frequency-dependent *rlgc* parameters may be extracted from the propagation constant and Z_0

$$\begin{aligned}
r &= \text{real}(\gamma \cdot Z_0), & l &= \frac{\text{imag}(\gamma \cdot Z_0)}{\omega}, \\
g &= \text{real}\left(\frac{\gamma}{Z_0}\right), & c &= \frac{\text{imag}(\gamma \cdot Z_0)}{\omega}.
\end{aligned} \tag{5.4}$$

where r is the series resistance of each conductor per unit length, l is the inductance of each conductor per unit length, g is the shunt conductance per unit length, and c is the total parasitic capacitance between conductors per unit length.

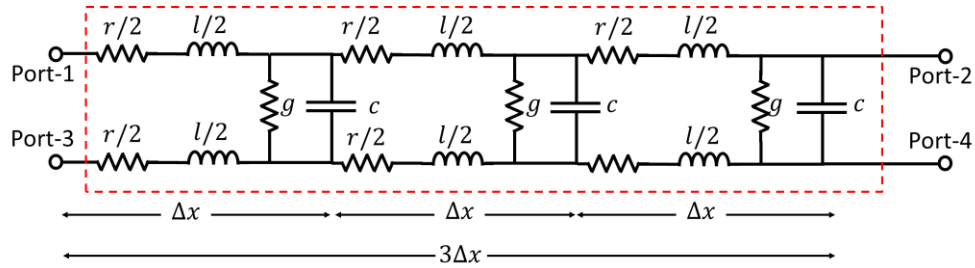


Fig. 5.2. Lumped-element circuit model for a transmission line

The total Q-factor of a shielded transmission line (ignoring radiation) is given by [81]

$$Q_{TL} = Q_{conductor} || Q_{substrate}, \tag{5.5}$$

where $Q_{conductor}$ is the Q-factor associated with the signal and ground plane metals, and losses due to current induced in the substrate by magnetic coupling. The $Q_{substrate}$ is the quality factor of the shunt parasitics (e.g., dissipation of the electric field in the silicon substrate). Both $Q_{conductor}$ and $Q_{substrate}$ can be expressed in terms of lumped-element (i.e., r, l, g, c) parameters

$$Q_{conductor} = \frac{\omega l}{r}, \tag{5.6}$$

and

$$Q_{substrate} = \frac{\omega c}{g}, \tag{5.7}$$

where ω is radian frequency. At low frequency, $Q_{substrate}$ is larger than $Q_{conductor}$. For transmission lines fabricated on medium resistivity silicon substrates (1-100 Ω -cm), $Q_{conductor}$ is typically higher than $Q_{substrate}$ at mm-wave frequencies, which makes the total

Q of the line dependent only on $Q_{\text{substrate}}$ [76]. Thus, increasing conductor metal thickness to increase $Q_{\text{conductor}}$ does not have a large effect on the total Q-factor. The greatest improvement in Q typically comes from the improvement in $Q_{\text{substrate}}$.

5.2 Layout Modification for Improving $Q_{\text{conductor}}$

Transmission line dimensions in this study are designed to optimize the $Q_{\text{conductor}}$ in the frequency range of interest. It is seen from eq.(5.6) that $Q_{\text{conductor}}$ increases with increasing series inductance (l) and decreasing series resistance (r). For a balanced or differential line, l is defined in terms of self- (l_s) and mutual inductance (l_M) between the coupled lines,

$$l = l_s - l_M. \quad (5.8)$$

For a fixed length, and thus fixed self-inductance, l as well as $Q_{\text{conductor}}$ can be increased by reducing l_M . Therefore, a wider gap between coupled lines results in improved $Q_{\text{conductor}}$. Moreover, wider signal lines reduce the series resistance (r), which also improves $Q_{\text{conductor}}$. However, skin effect increases with line width, limiting the improvement for very wide lines (e.g., greater than 15 μm). Selection of width also affects the characteristic impedance of the line.

5.3 BEOL Metal Stack

Multiple BEOL stack options are available in the 22-nm SOI CMOS technology. The stack-11 option is used for the lines reported in this section. Stack 11 has three top metal layers: 2.9- μm (LB), 3.3- μm thick (OI), and (JA) of 1- μm thickness. Coupled microstrip line models supported by the PDK library use either LB or OI as the signal line, with a ground shield option implemented in a mesh pattern of thinner first-metal (M1). The proposed prototypes use OI as transmission line metal, and C1 (third metal from bottom) and C2 (fourth layer from bottom) as the shield fingers. Fig. 5.3 shows the meal stack for the fabricated prototypes.

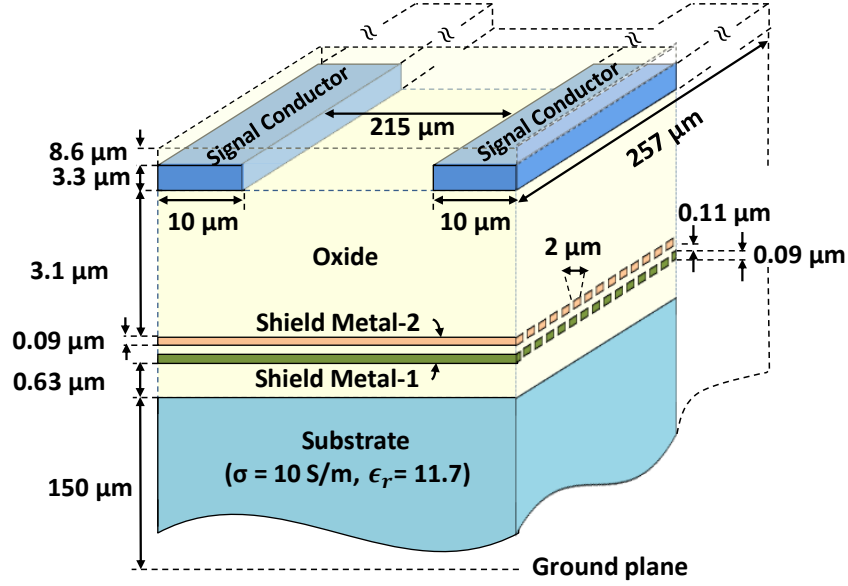


Fig. 5.3. Metal dimensions

5.4 Substrate Shielding for Improving $Q_{\text{substrate}}$

Custom designed substrate shielding and modified layouts from the PDK library that improve Q are proposed. For benchmarking, transmission lines with two different dimensions: 1) 10- μm line width and 215- μm gap between lines (‘wide gap’ of Fig. 5.4a), 2), and 2) 5- μm line width and 10- μm gap between lines (‘narrow gap’ of Fig. 5.4b) are described. Two different types of shielding are used: 1) a floating shield [81], and 2) a PDK provided ground shield in M1. The wide-gap prototype has a differential characteristic impedance (Z_0) of 60 Ω and the narrow-gap line has a differential Z_0 of 50 Ω . Characteristic impedances greater than 50 Ω facilitate embedding of circuitry in a distributed amplifier [47]. The signal conductor is implemented using the OI layer, as it is the thickest metal giving the lowest resistance, r .

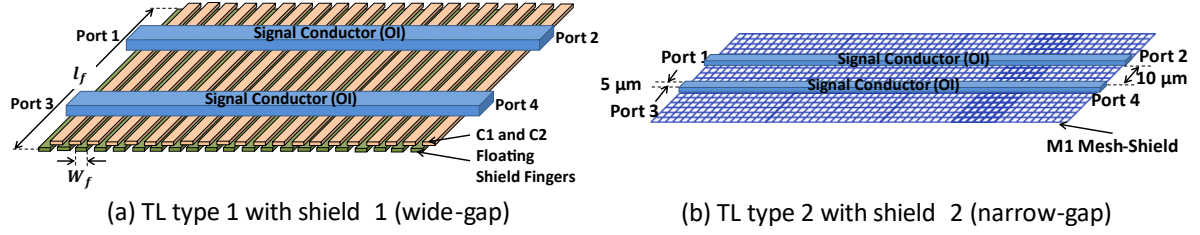


Fig. 5.4. Balanced transmission line layouts

Various shielding options are provided for the PDK TL models, but they require explicit ground connections. The floating substrate shield (shield 1) used in this work does not require an explicit ground connection [81]. Thin and narrow overlapping fingers of floating metals are used as shown in Fig. 5.4a. Narrow finger widths (e.g., 2- μm) prevent induced currents in the direction of signal flow, and overlapping adjacent fingers lowers leakage through the shield to the substrate. Electric induction creates a virtual ground along the floating shield fingers, thereby blocking the electric field from entering the silicon substrate. Lower-level metals C1 and C2 with thickness less than 90-nm (i.e., close to the silicon substrate) are used which span both signal conductors (length l_f). Finger width and gap of the shield metals are 2- μm and 1- μm , respectively, with 0.5- μm of overlap. These dimensions were optimized using electromagnetic (EM) simulations.

Simulation results comparing the performance between shielded and unshielded TL are illustrated in Fig. 5.5 for the wide-gap prototype. As seen from Fig. 5.5a, the floating shield reduces the attenuation constant by reducing the substrate loss. Therefore, Q is improved with an optimized floating shielding design, as shown in Fig. 5.5b.

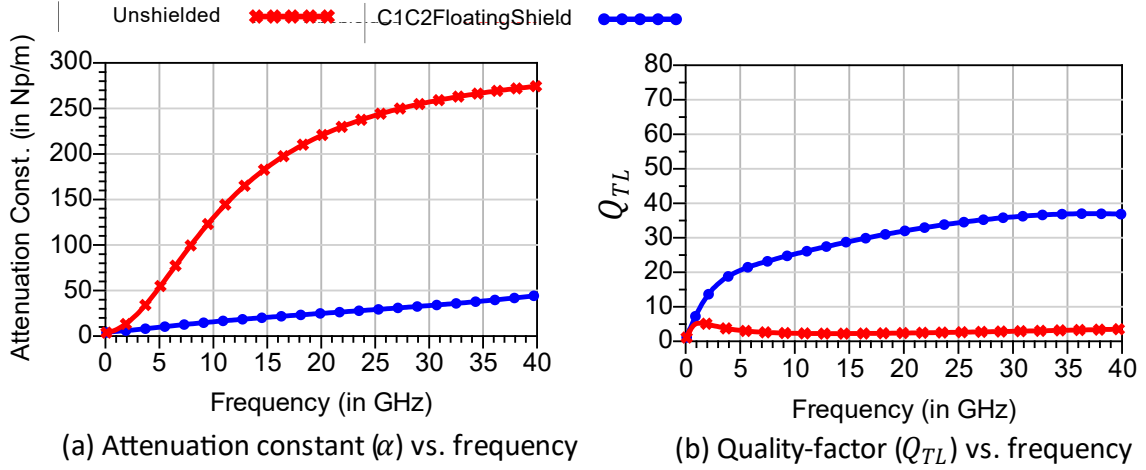


Fig. 5.5. Comparison between shielded and unshielded simulation results for the type1, shield1 wide-gap test structure

5.4.1 Prototype Design and Physical Layout

All TL test structures are fabricated with GSGSG pads connected to the coupled lines to create the device under test (DUT). Measurements of the 4-port S-parameters (ref. Fig. 5.6a) are performed on each DUT, which is comprised of the GSGSG padset (left), TL test cell, and right GSGSG padset (right) connected in series. Balanced measurements are performed to determine the differential 2x2 S-matrix. The differential measurement setup is shown in Fig. 5.6b. Next, LiLj de-embedding [79] is performed to extract the 2x2 differential S-parameters for the TL sell from the measured data. Two different lengths (L_i and L_j , for $L_j > L_i$) of the same design are fabricated to employ LiLj de-embedding for each test line. Lengths L_i of 514 μm and L_j of 257 μm are fabricated for test lines with 10- μm width and 215- μm gap, whereas LiLj pairs of 150 μm - 573 μm are fabricated for test lines with 5- μm width and 10- μm gap. Fig. 5.7 shows the die photo for the fabricated TL prototypes. Parameters α , β and Q are computed using eq. (5.1) to (5.3) from the de-embedded 2x2 S-matrix.

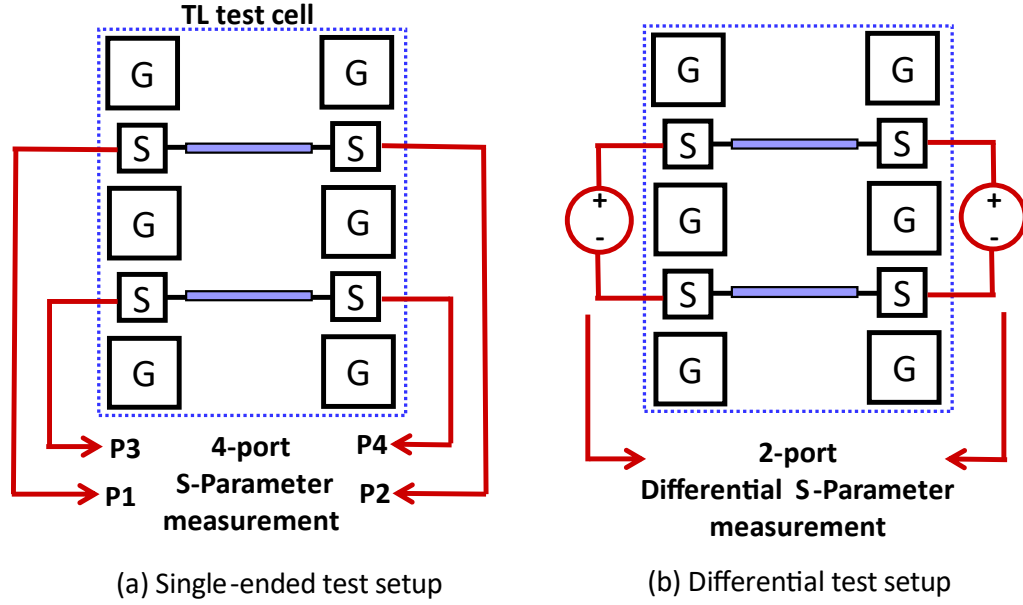


Fig. 5.6. Test configurations

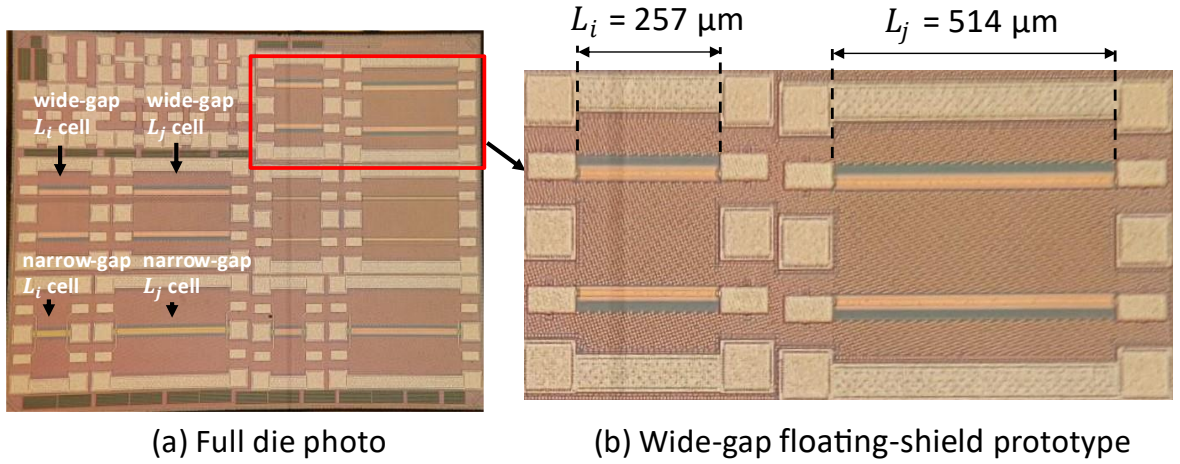


Fig. 5.7. MPW2225 Die Photo

5.4.2 Measurement Results

The de-embedded measurement results for α , β , and Q_{TL} are shown in Fig. 5.8. The custom designed TL results are compared with the microstrip narrow-gap coupled line PDK model (brown curve) that is fabricated on the test chip. The same narrow-gap top conductors, but with

the floating shield is shown in purple. The floating shield improves the Q-factor by 4x at 40GHz, as shown in Fig. 5.8d. Finally, the design (magenta) which optimizes both the top conductor layout (10- μm width and 215- μm gap) and the shield (floating) has a measured maximum Q-factor of 160 at 25 GHz.

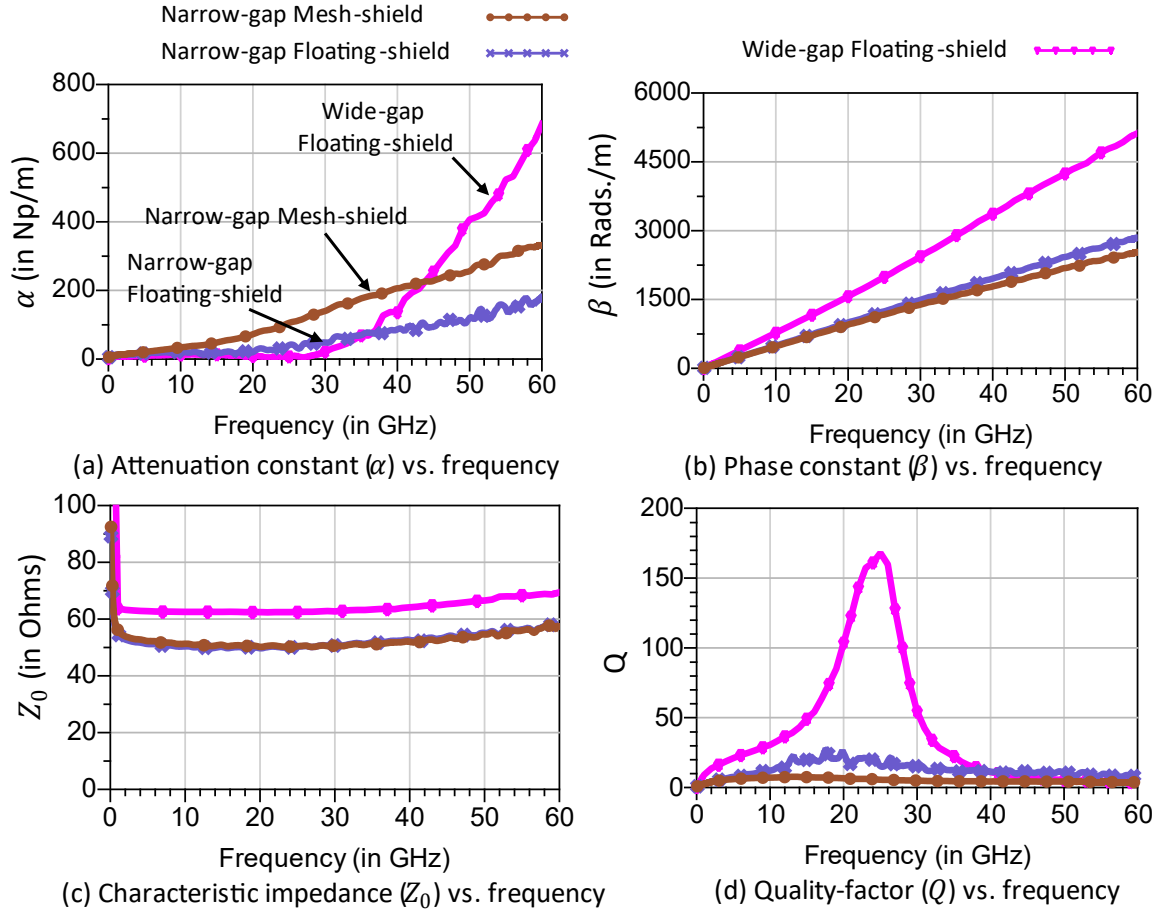


Fig. 5.8. Measured TL parameters for custom designed test structures (wide-gap TL length is 257 μm and narrow-gap TL length is 423 μm)

The magenta and the purple curves in Fig. 5.8c compare the Q-factors of lines with different sets of physical parameters (width and gap), but the same floating shield. The wider gap reduces the electric and magnetic coupling between the lines, which increases the self-inductance of the lines and improves the Q-factor in the range between 20 GHz and 30 GHz.

The increase in attenuation beyond 30 GHz seen in Fig. 5.8a is due to the resonance between the oxide capacitance and the inductance of the shield (L_{sh} and C_{ox} in Fig. 5.13).

5.4.2.1 Modelling the dip in attenuation constant (α) with increasing frequency

The dip in the attenuation constant (α) observed for the wide-gap floating shielded line is a significant development as it leads to a large Q-factor. Fig. 5.9 shows the simulation results for the wide-gap floating shield prototype. In Fig. 5.9a, the dip in α occurs between 20 GHz and 30 GHz with a minimum of 18 Np/m at 24 GHz. The peak Q for the transmission line is greater than 85 at 24 GHz as shown in Fig. 5.9a which coincides with the α dip.

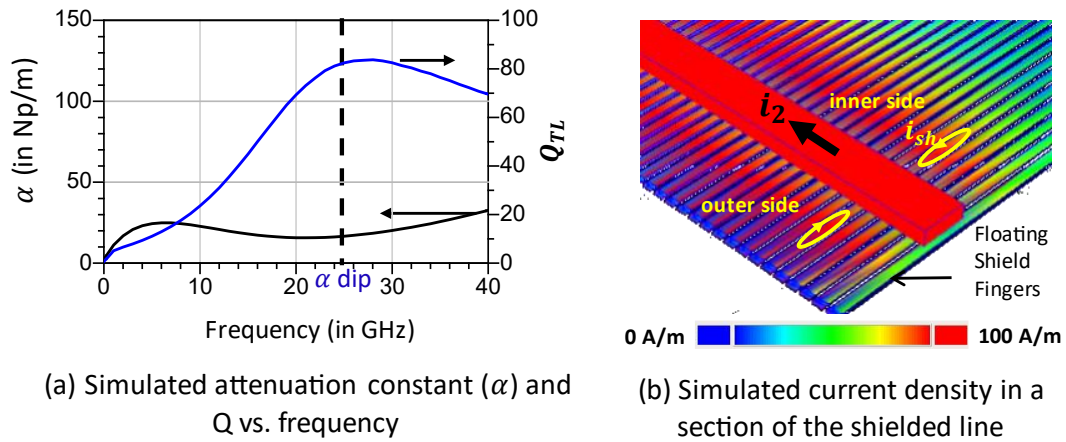


Fig. 5.9. Attenuation constant and current density of a shielded line from simulation

Fig. 5.9b illustrates the current density in the top conductor and shield metals from a method of moments simulation at 25 GHz. Current flowing in the top conductor (i_2) induces a loop current (i_{sh}) flowing counterclockwise on the inner side of the shield finger, in accordance with Ampere's law. The direction of current flow in the top conductor is marked by i_2 , and the loop current in the shield finger is denoted by i_{sh} in Fig. 5.9b. Current i_{sh} induced on the outer sides of the shield finger is clockwise for the same reason. Therefore, the net current flow on each shield finger directly beneath the top conductor is zero.

Fig. 5.10 presents a simplified physical layout and a lumped-element circuit used to model the physical phenomenon causing the dip in α . Voltages v_1 and v_2 are applied to port1 and

port2, respectively, and the currents flowing into the network from the corresponding ports are given by i_1 and i_2 . Parasitic capacitance between the signal conductor and shield finger is modelled by C_{ox} . Each shield finger is modelled by a sub-network comprised of resistor (R_{sh}) and inductor (L_{sh}) to capture the resistance and inductance of the shield. The mutual inductance resulting from magnetic coupling between the signal and shield conductors is M . Resistor R_{si} and capacitor C_{si} model dielectric relaxation and dissipation of the silicon substrate. For substrates with higher resistivity ($>10 \Omega\text{-cm}$), this branch can be ignored as any current drawn by the reactance of C_{si} in parallel with R_{si} is negligible in the frequency range of interest. Impedance Z_{shunt} is seen from node v_1 to ground, as shown in Fig. 5.10b

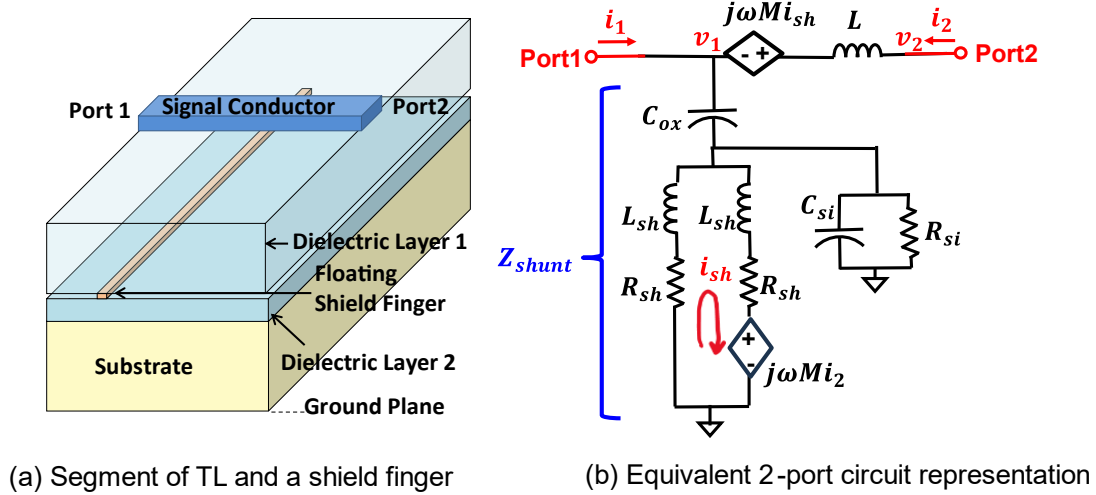


Fig. 5.10. Model for the magnetic coupling between the signal conductor and one shield finger

For the network of Fig. 5.10, the mesh equations corresponding to currents i_1 , i_2 , and i_{sh} are

$$(Z_{cox} + Z_{sh})i_1 + Z_{cox} \cdot i_2 - Z_{sh} \cdot i_{sh} = v_1 \quad (5.9)$$

and
$$-Z_{sh} \cdot i_1 + (Z_{sh} + Z_m)i_2 + 2 \cdot Z_{sh} \cdot i_{sh} = 0. \quad (5.10)$$

The impedance variables used in the equations correspond to the following circuit components in Fig. 5.10b:

$$\begin{aligned} Z_{cox} &= 1/j\omega C_{ox} \\ Z_{sh} &= R_{sh} + j\omega L_{sh} \\ Z_m &= j\omega M. \end{aligned} \tag{5.11}$$

Multiplying eq. (5.9) by two and adding the result to eq. (5.23) gives,

$$(2Z_{cox} + Z_{sh})i_1 + (2Z_{cox} + Z_{sh} + Z_m)i_2 = 2v_1. \tag{5.12}$$

Dividing both sides of eq. (5.12) by $2(i_1 + i_2)$ gives,

$$\frac{v_1}{(i_1 + i_2)} = \left(Z_{cox} + \frac{Z_{sh}}{2}\right)\frac{i_1}{(i_1 + i_2)} + \left(Z_{cox} + \frac{Z_{sh}}{2} + \frac{Z_m}{2}\right)\frac{i_2}{(i_1 + i_2)}. \tag{5.13}$$

Impedance Z_{shunt} is therefore,

$$Z_{shunt} = \frac{v_1}{(i_1 + i_2)} = Z_{cox} + \frac{Z_{sh}}{2} + \frac{Z_m}{2} \cdot \frac{i_2}{(i_1 + i_2)}. \tag{5.14}$$

Port currents i_1 and i_2 can be related by the phase constant of the transmission line, β . Assuming i_2 as the reference current with a value of $I_2 \angle 0^\circ$, it sees a phase shift of βl as it flows through the length (l) of the transmission line. Therefore, the port current into port 1 has a phase of βl (i.e., $i_1 = I_1 \angle \beta l$), as illustrated in Fig. 5.11.

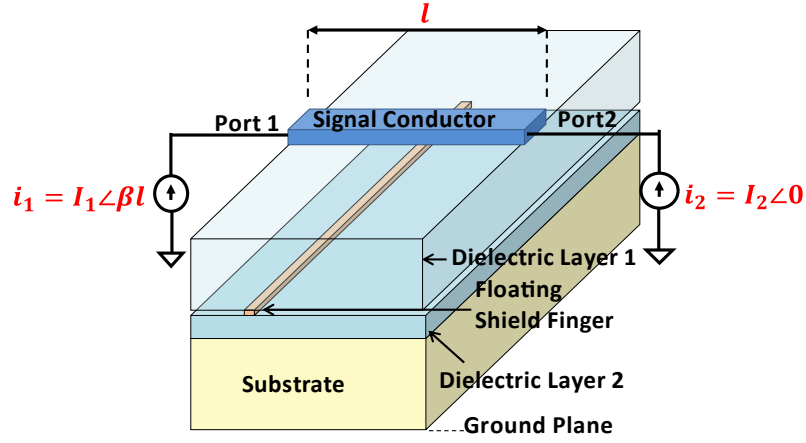


Fig. 5.11. Signal phase shift occurring through the transmission line of length l

$$i_1 = I_1 \angle \beta l = I_1 \cos \beta l + j I_1 \sin \beta l \quad (5.15)$$

Assuming phasor notation for the currents (i.e., $i_1 = I_1 \angle \beta l$ and $i_2 = I_2 \angle 0^\circ$) the ratio $\frac{i_2}{(i_1 + i_2)}$ is

$$\frac{i_2}{(i_1 + i_2)} = \frac{I_2}{(I_2 + I_1 \cos \beta l + j I_1 \sin \beta l)} = \frac{I_2}{(a + jb)} = \frac{I_2 a}{(a^2 + b^2)} - j \frac{I_2 b}{(a^2 + b^2)}, \quad (5.16)$$

where

$$a = I_2 + I_1 \cos \beta l$$

and

$$b = I_1 \sin \beta l. \quad (5.17)$$

Substituting eqs. (5.16) and (5.17) in eq. (5.14) yields Z_{shunt}

$$Z_{shunt} = Z_{cox} + \frac{Z_{sh}}{2} + \frac{Z_m}{2} \cdot \frac{I_2 a}{(a^2 + b^2)} - j \frac{Z_m}{2} \cdot \frac{I_2 b}{(a^2 + b^2)}. \quad (5.18)$$

Also, substituting eq. (5.25) in eq. (5.30),

$$\begin{aligned} Z_{shunt} &= m + jn \\ &= -\frac{j}{\omega C_{cox}} + \frac{R_{sh} + j\omega L_{sh}}{2} + \frac{j\omega M_1}{2} \cdot \frac{I_2 a}{(a^2 + b^2)} + \frac{\omega M_1}{2} \cdot \frac{I_2 b}{(a^2 + b^2)}, \end{aligned} \quad (5.19)$$

where m and n are the real and imaginary parts of Z_{shunt} , respectively. From eq. (5.17), m and n are

$$m = \frac{R_{sh}}{2} + \frac{\omega M_1}{2} \cdot \frac{I_1 I_2 \sin \beta l}{(I_1^2 + 2I_1 I_2 \cos \beta l + I_2^2)} \quad (5.20)$$

$$n = \frac{\omega L_{sh}}{2} - \frac{1}{\omega C_{cox}} + \frac{\omega M_1}{2} \cdot \frac{I_2^2 + I_1 I_2 \cos \beta l}{(I_1^2 + 2I_1 I_2 \cos \beta l + I_2^2)}. \quad (5.21)$$

The shunt conductance (g) is then calculated from Z_{shunt}

$$g = \text{real}(1/Z_{shunt}) = \text{real}\left(\frac{m - jn}{m^2 + n^2}\right) = \frac{m}{m^2 + n^2}. \quad (5.22)$$

Eq. (15) predicts that shunt conductance is negative when m is a negative value. The value of m is negative for lengths of transmission line where $\sin \beta l$ is negative and $\left[\omega M_1 \cdot \frac{I_2 I_1 \sin \beta l}{(I_1^2 + 2I_1 I_2 \cos \beta l + I_2^2)}\right] \gg R_{sh}$. This gives a range of positive and negative values for m with sinusoidal periodicity.

This negative shunt admittance is a consequence of the magnetic coupling between the conductor and the shield, and the phase change of the AC current flowing in the top conductor with frequency. In the equivalent $rlcg$ circuit of a transmission line (see Fig. 5.2), this effect reduces the attenuation of the signal in frequency ranges where m is negative, creating a local dip or minimum in the attenuation constant (α) at the corresponding frequencies. This phenomenon makes the proposed transmission line potential for use in narrow band application, such as resonators.

5.4.2.2 Transmission Line Resonator with Dip in Attenuation Constant (α)

The transmission line with dip in α , or high peak Q at a specific frequency (e.g., 160 at 25 GHz from Fig. 5.8d) may be modelled as a parallel resonant circuit, as shown in Fig. 5.12.

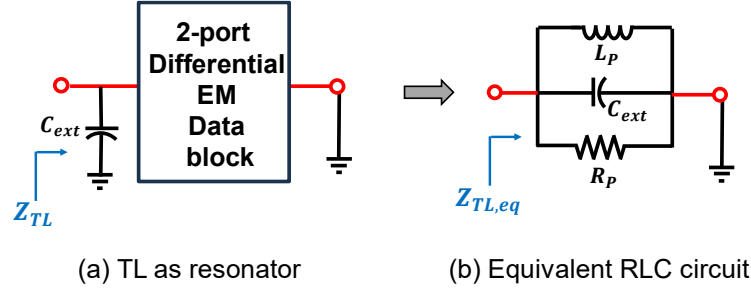


Fig. 5.12. Setup for transmission line as resonator

Fig. 5.12a shows the simulation configuring the transmission line as a resonator using 2-port differential S-parameters from measurement. One port is connected to the ground, and an ideal capacitor (C_{ext}) shunts at the other port to tune the resonant frequency. Fig. 5.12b shows the parallel RLC circuit equivalent of the TL resonator. The value of C_{ext} is tuned to 80 fF to align the peak in the input impedance (Z_{TL}) to the α dip at 25 GHz for the prototype TL. The peak value of Z_{TL} at resonance determines the value of the resistor R_p in Fig. 5.12b ($R_p = 1301 \Omega$ from simulation). The Q factor for both cases is measured from the bandwidth (i.e., $Q = \omega_{osc}/\Delta\omega$) of the Z_{TL} and $Z_{TL,eq}$, and is verified to be 160.

This proves that the high-Q TL with dip in α can be modelled as parallel RLC resonator with Q peaking at the resonant frequency. Active resonator concepts often exhibit higher selectivity compared to passive resonators. However, this increase in quality (Q) factor often comes at the expense of signal-to-noise ratio (SNR) performance and dynamic range. The objective is to demonstrate that the SNR performance of the TL resonator remains consistent with the energy dissipated by the resonator when at resonance. Essentially, there should be no decrease in SNR despite the increase in Q factor from shielding. Moreover, it is noteworthy that the dynamic range is excellent, as the third-order intercept (TOI) is substantial for a passive resonator in comparison to active circuits. To achieve this, it needs to be illustrated that the noise power at resonance is $4kTR_p$. Therefore, the output mean-square noise voltage is measured from simulation for both the cases (measured data and RLC circuit), and found to be 4.6 nV (which is $4kTR_p$ for R_p of 1301 Ω) for both.. This further verifies that there is no excess noise attributed to the boost in Q factor from shielding.

5.4.3 Modelling the Balanced Transmission Line

A schematic diagram of the proposed lumped-element circuit model for shielded, balanced transmission lines proposed in this thesis is shown in Fig. 5.13. The model is applicable to single ended, unshielded and ground shielded lines. For instance, the unshielded line model would exclude the shield-loop branch, and ground shielded model would have the shield-loop branch connected to the ground on both nodes. The π -section model contains a series branch and two divided shunt branches.

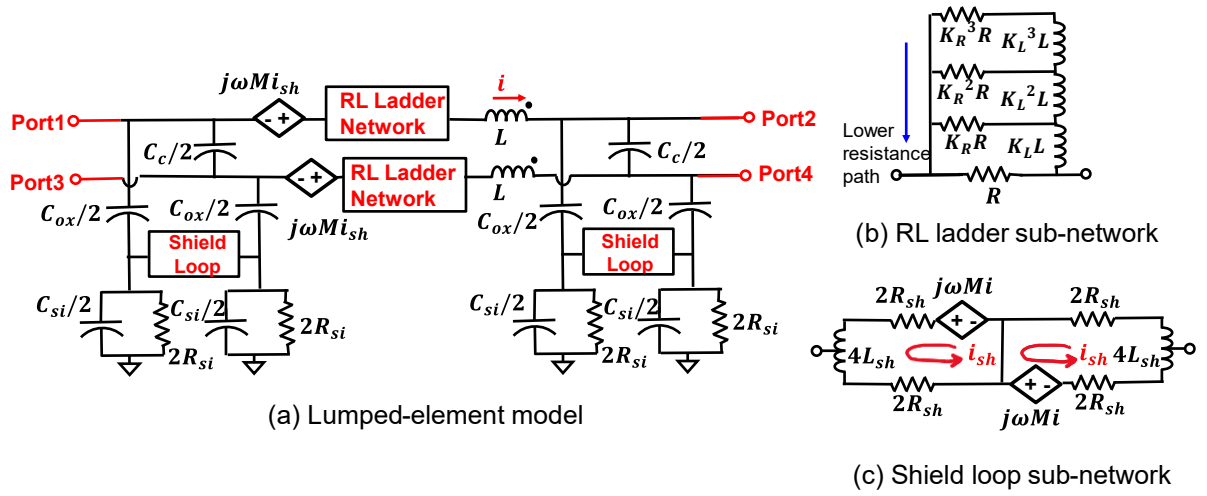


Fig. 5.13. Single-section lumped-element model for a coupled transmission line with floating shield

A. Shunt Branch

Capacitors $C_c/2$ model the electric coupling between the signal conductors. Parasitic capacitance between the signal lines and shield is modelled by capacitors $C_{ox}/2$ in shunt with each port. These 4 capacitors and the 4 parallel R-C networks comprised of resistors $2R_{si}$ and capacitors $C_{si}/2$ model dielectric relaxation and dissipation of the silicon substrate [82]. Each shield finger is modelled by a sub-circuit comprised of a resistor (R_{sh}) and an inductor (L_{sh}). The shield sub-network of Fig. 5.13c shows the loop current (i_{sh}) induced by current flowing in the signal conductors (i). A current controlled voltage source models the magnetic inductor with mutual inductance, M . When there is no current in the signal conductor (i.e., $i = 0$), there

is no induced loop current (i.e, $i_{sh} = 0$) and the shield sub-network of Fig. 5.13c can be simplified to the circuit shown in Fig. 5.14.

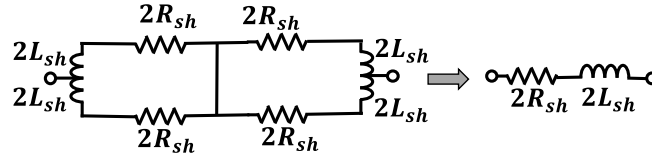


Fig. 5.14. Shield loop network from Fig. 5.13c, for $i = 0$.

B. Series Branch

In Fig. 5.13b, inductor L defines the self-inductance and resistor R defines the DC resistance between ports 1-2 (and ports 3-4) of the 4-terminal network multiplied by some arbitrary constants K_R . The value of K_R depends on DC and AC resistance of the signal conductor, which is frequency dependent [30]. An R-L ladder network [83], [30] models losses in the signal conductors due to the skin and proximity effects with increasing frequency. Constants K_L and K_R define the constant ratio between two consecutive branch's inductor and resistor, respectively. The progressive reduction of the resistance value towards R (from $K_R^3 R$ to R marked with an arrow in Fig. 5.13b) signifies the presence of a non-uniform resistive path with lower resistance on the surface of the conductor, which is caused by the skin effect. The frequency-dependent series resistance of an on-chip TL, $R(f)$, may be approximated by the equation [84]

$$R(f) = R_{DC} + R_{sk} = R_{DC} + k_{sk} f^n,$$

where R_{DC} is the resistance of the R-L ladder at DC. Resistor R_{sk} models the dissipation caused by skin effect and proximity effects with increasing frequency. For substrate resistivities ($1/\sigma$) greater than $1 \text{ } \Omega\text{-cm}$, exponent ' n ' is typically 0.5, giving a square-root of frequency dependence. The number of parallel branches in the R-L ladder is ' q '. Two parallel branches [30] are sufficient to capture the frequency dependent loss across a 60-GHz range for 500- μm long microstrip lines. The number of parallel branches along with K_r and K_l coefficients may

be adjusted to extend the model accuracy and frequency range. The shape of the attenuation constant vs frequency depends on the number of R-L branches, as illustrated in Fig. 5.15.

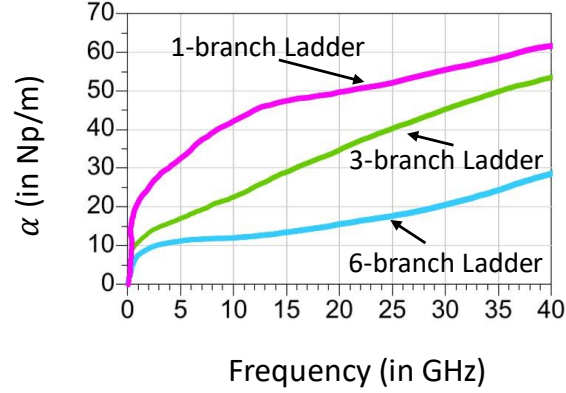


Fig. 5.15. L-E model attenuation constant for different number of parallel branches in R-L ladder with $K_r = 1$, $K_r = 0.5$ for narrow-gap floating-shield TL

Fig. 5.15 shows that for a smaller number of branches, the attenuation constant has approximately a $\sqrt{f}$ dependency (1-branch curve). Increasing the number of branches to 6 yields an f^2 relationship with increasing frequency. The 22-nm FD-SOI CMOS technology has a resistivity of 10 Ω -cm, and 3 branches are chosen to model the skin-effect for the prototype TLs.

The number of lumped-element sections required to model a transmission line depends on physical length of the line and the desired frequency range (i.e., minimum wavelength λ). Lines greater than approximately $\lambda/10$ in length (i.e., $\lambda = c/(f \cdot \sqrt{\epsilon_r})$, where c is the velocity of light and ϵ_r is the relative permittivity of the medium), require multiple single-section models connected in series, as shown in Fig. 5.13. The attenuation constant (α) for the 423- μ m long narrow-gap floating-shielded line is compared to 1- and 2-section lumped-element models in Fig. 5.16. Electromagnetic (EM) simulation data of the line is taken as a reference. The single section-model begins to deviate significantly from the EM data around 45 GHz, while the 2-section model replicates the data up to almost 70 GHz. Therefore, a single-section model may be used to model test structures for lengths below 500 μ m for a frequency range up to

$\lambda/10$, which is 60 GHz for free space (45 GHz for the transmission line, as velocity is lower for the TL than free space).

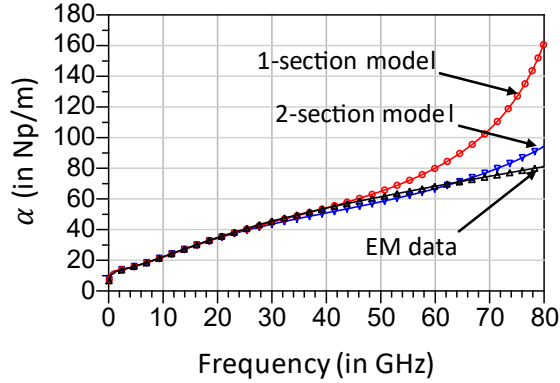


Fig. 5.16. Number of sections vs. EM data of narrow-gap floating-shield TL with 5- μm width, 423- μm length and 10- μm gap between lines

5.4.3.1 Model Parameter Extraction from *rlgc* and EM Simulation

Component parameters for the model may be extracted from measured or simulated 4-port data sets. In this section a step-by-step extraction process is described. S-parameter data obtained from EM simulation are used for the example described.

- *Extraction of C_{ox} , C_c , C_{si} , and R_{si}*

The first step is to extract parameter values for components C_{ox} , C_c , C_{si} , and R_{si} with the input ports driven in the common-mode. Shunt elements C_{ox} , C_{si} , and R_{si} define the impedance to ground (Z_{shunt}) when all of the ports are short-circuited (ref. Fig. 5.17), as voltage or current does not flow through the other model components.

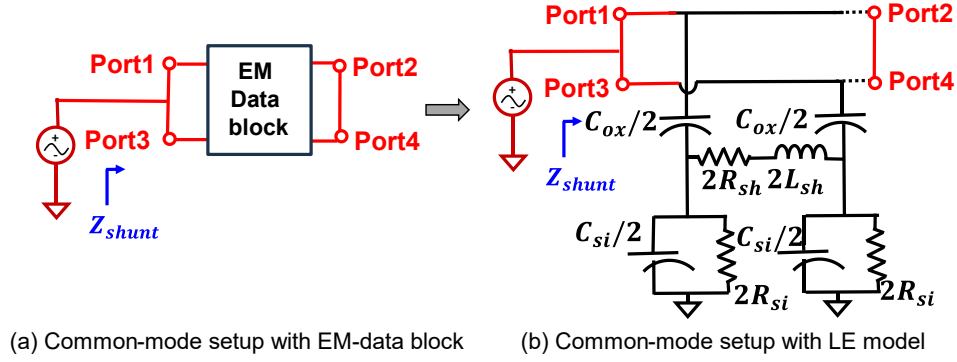


Fig. 5.17. Shunt branch of the proposed model (without shield) in the common-mode

From Fig. 5.17, the impedance to ground (Z_{shunt}) in the common mode is given by

$$\begin{aligned}
 Z_{shunt}(\omega) &= \left[\frac{1}{j\omega C_{ox}} + \left(\frac{1}{j\omega C_{si}} \parallel R_{si} \right) \right] \frac{1}{2}, \\
 &= \left[\frac{R_{si}}{1 + (\omega R_{si} C_{si})^2} - j \left(\frac{1}{\omega C_{ox}} + \frac{\omega C_{si}}{\frac{1}{R_{si}^2} + (\omega C_{si})^2} \right) \right] \frac{1}{2}, \\
 &= [Re(Z_{shunt}) - j Im(Z_{shunt})].
 \end{aligned} \tag{5.23}$$

The cut-off frequency in the quasi-TEM mode of a microstrip line on silicon defined by Hasegawa in [82] is

$$f_c = \frac{1}{2\pi\epsilon_0\epsilon_{si}\rho_{si}}, \tag{5.24}$$

where ϵ_{si} and ϵ_0 are dielectric constants of silicon and air, respectively. Parameter ρ_{si} in eq. (5.24) is the substrate resistivity.

For frequencies well below f_c , eq. (5.23) is approximated by,

$$Z_{shunt}(\omega \ll 2\pi f_c) \approx \frac{R_{si}}{2} + \frac{1}{j\omega 2C_{ox}}. \tag{5.25}$$

Parameters R_{si} and C_{ox} of the L-E model are therefore extracted using (5.25). Substitution of (5.25) into eq. (5.23) yields an expression for capacitance C_{si}

$$C_{si} = \frac{Y_{shunt}(\omega)}{2\omega} = \left[Z_{shunt}(\omega) - \frac{R_{si}}{2} - \frac{1}{j\omega 2C_{ox}} \right]^{-1} / 2\omega. \quad (5.26)$$

Line-to-line capacitance, C_c is connected between ports 1-3 and 2-4. It is determined from backend extraction of the physical layout of the TL using the process design kit (PDK) for the 22-nm technology. It is negligible for widely separated (e.g., gap = 250 μm) conductors. However, for the narrow-gap (e.g., gap = 10 μm) transmission lines, it defines the electrical coupling. Parameters C_{ox} and C_{si} may also be extracted from the node-to-ground capacitances extracted from the physical layout (using the PDK tools) as an alternative to the approach discussed above.

▪ *Extraction of R_{sh} and L_{sh}*

To extract shield elements R_{sh} and L_{sh} , the 4-ports of the transmission line are excited differentially, as shown in Fig. 5.18.

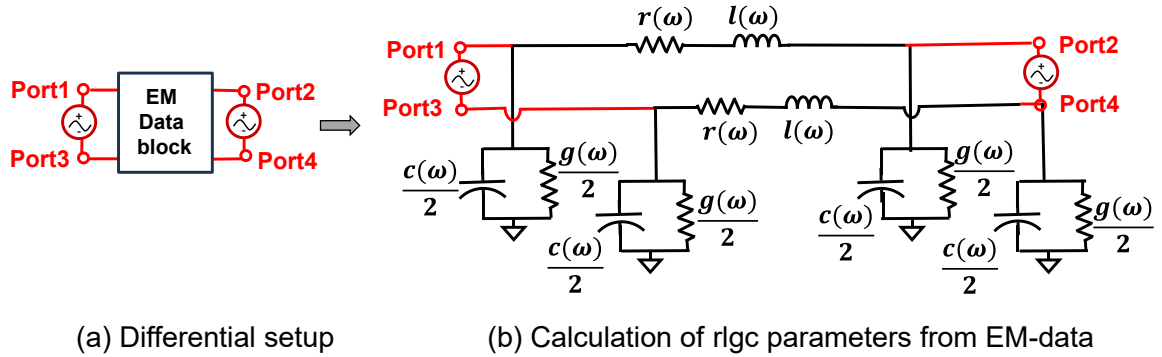


Fig. 5.18. Differential excitation for calculation of RLCG parameters from a 4-port data set

The frequency-dependent *rlcg* parameters [85] of the model are calculated from the differential 2-port ABCD parameters using eq. (5.4). Shield elements R_{sh} and L_{sh} , (ref. Fig. 5.13) are then computed. Ports 1 and 2, and ports 3 and 4 are excited differentially, as shown in Fig. 5.18a. In this configuration, the R-L ladder network and L series branches are short circuited. However, a self-resonance occurs between the shield inductance (L_{sh}) and equivalent

capacitance of the network in Fig. 5.19b (i.e., combination of C_{ox} , C_c , and C_{si}). However, C_{ox} dominates and contributes the most to the resonance among the three capacitors.

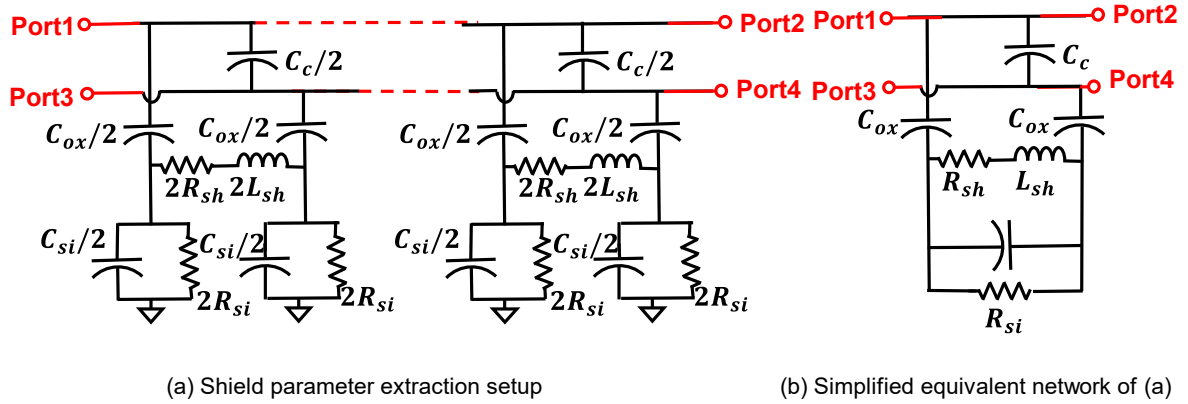


Fig. 5.19. Shield parameter extraction setup with ports 1 and 2, and ports 3 and 4 shorted for differential excitation

The self-resonant frequency (f_{sh}) of the shield is noted from the simulated data for $c(\omega)$. Parameter L_{sh} is calculated from

$$f_{sh} = 1 / 2\pi \sqrt{\left(L_{sh} \left(C_{si} + \frac{C_{ox}}{2} \right) \right)}. \quad (5.27)$$

For example, if the f_{sh} is 100 GHz as observed from the $c(\omega)$ plot, L_{sh} for a C_{ox} of 50 fF, C_{si} of 1 fF, and C_c of 0.6 fF is 50 pH from eq. (5.27). The shield resistance, R_{sh} is typically small (i.e., $\sim 1 \Omega$), because dissipation of metal shield fingers across the length of a single section is low when the shield is properly designed. From the values of C_{ox} , C_{si} , R_{si} , and L_{sh} extracted previously, R_{sh} is determined by fitting its value so that calculated shunt g -parameter, $g_{cal}(\omega)$ for the model (ref. Fig. 5.20b) equals $g(\omega)$ for data set (ref. Fig. 5.20a) at low frequency (i.e., $f \ll f_c$). Measured S-parameter or ABCD parameter data may also be used for these extraction steps.

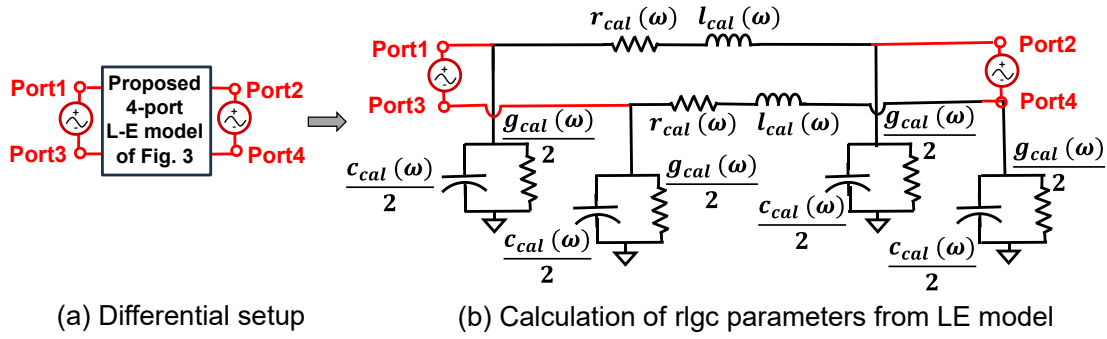


Fig. 5.20. Differential excitation and calculation of $rlcg$ parameters for the lumped-element model

- *Extraction of series components R , L , k , K_R , and K_L*

The impedances connected in series between the ports 1-2 and 3-4 (i.e., R and L in Fig. 5.13) are determined from $rlcg$ parameters, $r(\omega)$ and $l(\omega)$, calculated from a measured or simulated data set.

$$\begin{aligned}
 Z_{series}(\omega) &= [r(\omega) + j\omega l(\omega)] \times \text{length of the line}, \\
 &= \left[R + j\omega L + \frac{1}{\sum_{i=1}^3 (1/(K_R^i R + j\omega K_L^i L))} \right], \\
 &= [r_{cal}(\omega) + j\omega l_{cal}(\omega)] \times \text{length of the line}
 \end{aligned} \tag{5.28}$$

The number of parallel branches in the R-L ladder is represented by i . The series branch parameters of the model (R , L , k , K_R , and K_L) are extracted by fitting the calculated $r_{cal}(\omega)$ and $l_{cal}(\omega)$ values from eq. (5.28) to frequency-dependent polynomials that represent $r(\omega)$ and $l(\omega)$ of data set.

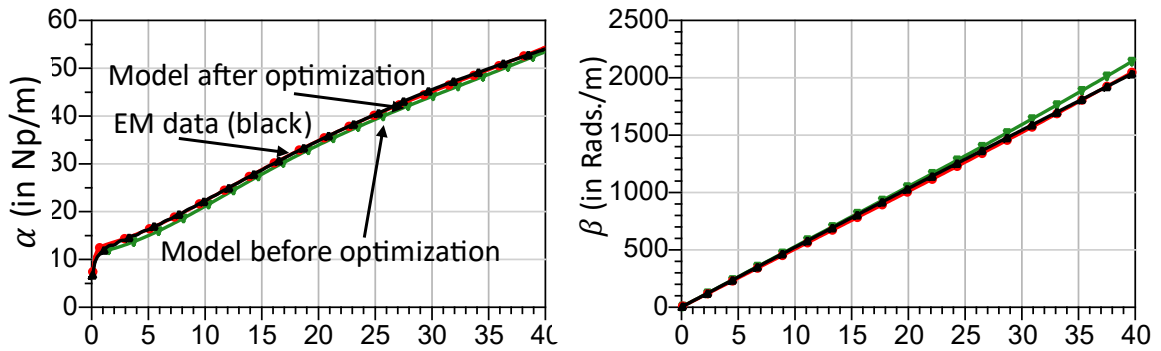
The coefficients of these polynomials (e.g., r_{DC} and k_{sk} for $r(\omega)$ in (2)) are compared to solve for R , L , k , K_R , and K_L values from the fitting functions

$$F_r(\omega) = |r(\omega) - r_{cal}(\omega)|, \quad (5.29)$$

$$F_l(\omega) = |l(\omega) - l_{cal}(\omega)|. \quad (5.30)$$

▪ *Fine-tuning performance with optimization*

Numerical optimization may be used to fine tune the lumped-element model parameter values to minimize (5.29) and (5.30). The plots of Fig. 5.21 illustrate the quality of fit for the model parameters before and after optimization for the simulated data set of the narrow-gap floating-shield test structure. It is seen that the optimization process do not result in a substantial improvement in the quality of fit, as the model parameters extracted from the above mentioned approach already offer a good fit with the TL data..



(a) Attenuation constant (α) vs. frequency

(b) Phase constant (β) vs. frequency

Fig. 5.21. Lumped-element model performance before and after optimization for the narrow-gap line with 5- μ m width, 423- μ m length and 10- μ m gap between lines

5.4.3.2 Model Performance

The performance of the lumped-element model is shown in Fig. 5.22. Goodness of fit is characterized by the R-square value (percentage of the variance in the dependent variable), is

87% for α and 99.7% for β across the 10 MHz – 60 GHz range. Cascading multiple lumped-element sections (i.e., 3 sections in this case) is sufficient for this wide frequency range. Fit of the model in the common mode has a goodness of fit of 88% for α , and 99.8% for β .

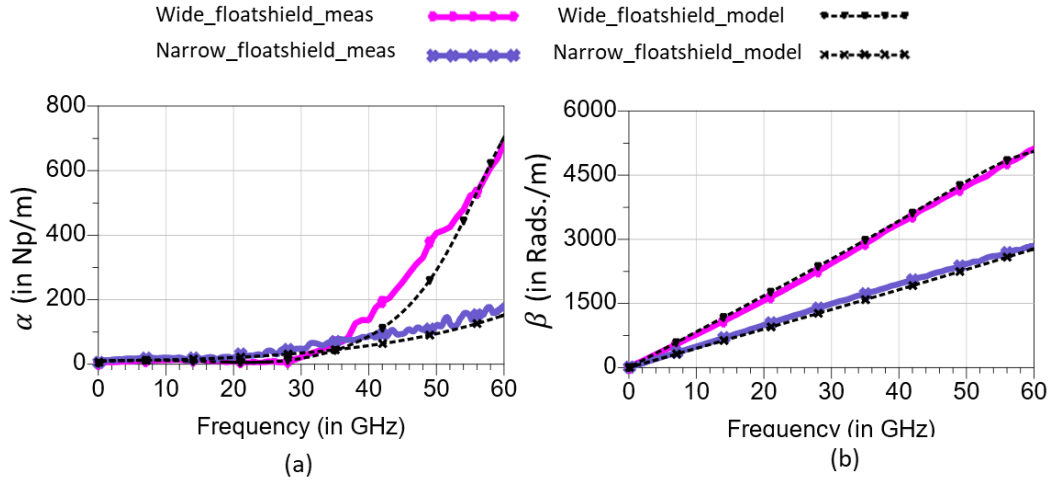


Fig. 5.22. Measured vs. model performance of Fig. 5.13 (a) attenuation and (b) phase constant for floating shielded wide and narrow gap TLs

Fig. 5.22 shows the performance comparison for wide- and narrow-gap TLs with a floating shield. It models the behaviour of both slow-wave and TEM modes accurately. Fig. 5.23 illustrates the α and β results of the model a model of the narrow-gap TL with a grounded mesh shield. In this case, parameters R_{si} and C_{si} from Fig. 5.13 are set to zero.

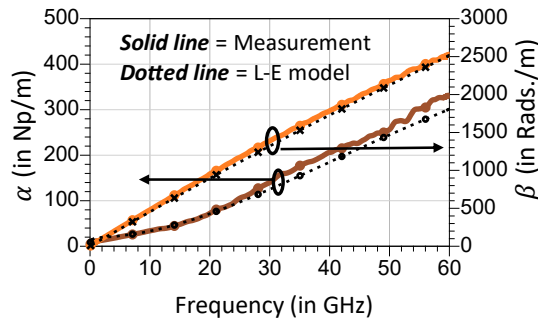


Fig. 5.23. Measured vs. model attenuation and phase constant for the narrow-gap-mesh shield.

In Fig. 5.24, Q-factors for the three test structures are plotted. The plots of Fig. 5.8c are compared with the corresponding Q plot from the model. It can be seen that the agreement between the proposed lumped-element model and the measured data is very good. The lumped-element model captures the electrical behaviours of shielded or unshielded TLs and is applicable to static and dynamic simulations of circuits.

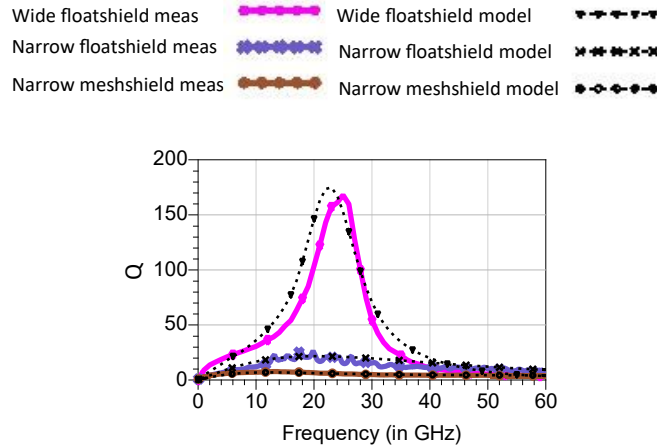


Fig. 5.24. Measured vs. L-E model Q factor plots

5.5 Summary

This chapter presented the design of high-Q, on-chip transmission lines fabricated in 22-nm FD-SOI-CMOS technology. Layout improvements and floating substrate shielding designs were demonstrated for the Stack-11 BEOL option of the technology that showed improved Q-factor. Measurement results show a peak Q-factor of 160 at 25-GHz for the 257-um long wide-gap coupled lines, and demonstrate their potential for applications in low-loss RF/mm-wave interconnects and narrow-band transmission line resonators. The high Q is caused by a dip in attenuation constant which is modelled in this work. The physical phenomenon supporting the model is also explained.

A lumped-element model for these high-Q shielded lines is also presented. The equivalent circuit accurately models single-ended and balanced transmission lines at mm-wave frequencies for both substrate shielded and unshielded variants. Scalability without loss of

accuracy is realized by employing multiple sections of the lumped-element model, as required. Parameter extraction for a multi-section, lumped-element model of a balanced on-chip transmission lines with floating shields was described in detail. Accuracy of the model is verified for on-chip transmission lines fabricated in 22-nm FD-SOI CMOS technology. The model characterizes both differential and common-mode behaviours making it a complete and accurate model for small-signal and time-domain simulation of on-chip transmission lines.

Chapter 6

Integrated Bridge Oscillator Circuit Design

The bridge stabilized oscillator has the potential for low phase noise performance. In this chapter, a fully integrated 8-GHz bridge oscillator design is described that targets -130 dBc/Hz phase noise at 1-MHz offset. The on-chip L-C bridge resonator proposed in Chapter 4 is utilized in the design of the oscillator. The amplifier stages in the oscillator must be designed carefully when attempting to realize low phase noise. For this work, a two-stage amplifier is proposed for high efficiency and low-noise performance. Close attention is paid to interstage interfacing of the amplifiers and the bridge to realize the desired phase noise target.

6.1 Proposed Oscillator Topology

A top-level block diagram of the integrated bridge oscillator is illustrated in Fig. 6.1. The design consists of a bridge resonator circuit, a low-gain preamplifier with a tuned bandpass filter load, and a power amplifier stage.

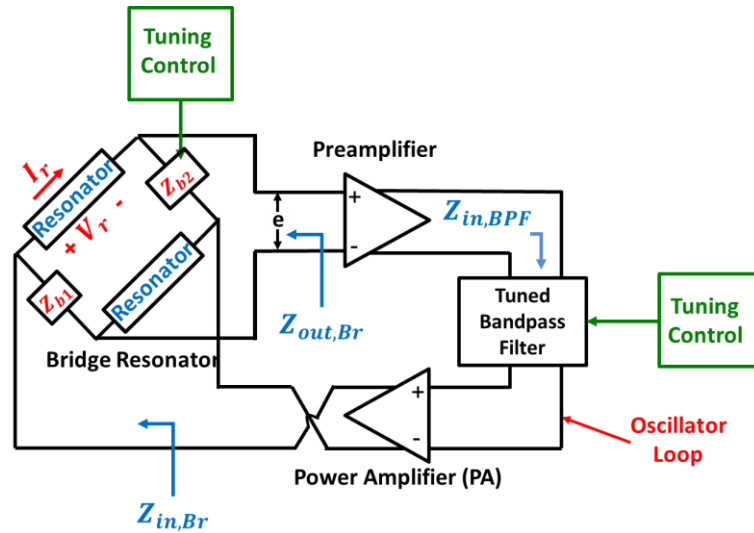


Fig. 6.1. Block diagram of the proposed integrated bridge oscillator

The prime objective of the proposed design is to achieve low phase noise. The bridge circuit is described in Chapter 4. The bridge output is the error voltage (e). The resonators are tuned to the desired oscillation frequency (f_{osc}).

A sharp transition in the phase response of voltage ‘e’ (i.e., $\frac{\partial \phi}{\partial \omega}$) is seen close to f_{osc} . The gain of the bridge also shows a null point at f_{osc} . The gain is designed such that error voltage (e) is 0.1 V/V when the phase shift is 180° . The two amplifier stages then boost the error voltage to provide sufficient loop gain for sustained oscillation. The open-loop voltage gain ($G_{v,OL}$) of the circuit in Fig. 6.1 is

$$G_{v,OL} = (G_{br} \cdot G_{PreA} \cdot G_{PA}), \quad (6.1)$$

where G_{br} , G_{PreA} , and G_{PA} are open-loop voltage gains (including loading effects) of the bridge, preamplifier tuned with the bandpass filter, and the PA, respectively. According to Barkhausen’s criteria presented by eq. (1.6) and (1.7), $G_{v,OL}$ should be greater than unity, with a phase shift of at least 360° for a sustained oscillation. As discussed in Section 2.1, these conditions refer to small-signal operation of the loop at start up, where the preamplifier and PA can be modelled by the equivalent circuit of Fig. 6.2. In the model, g_m is the transconductance, and $c_{in} \parallel r_{in}$ and $c_{out} \parallel r_{out}$ model the input and output impedances, respectively.

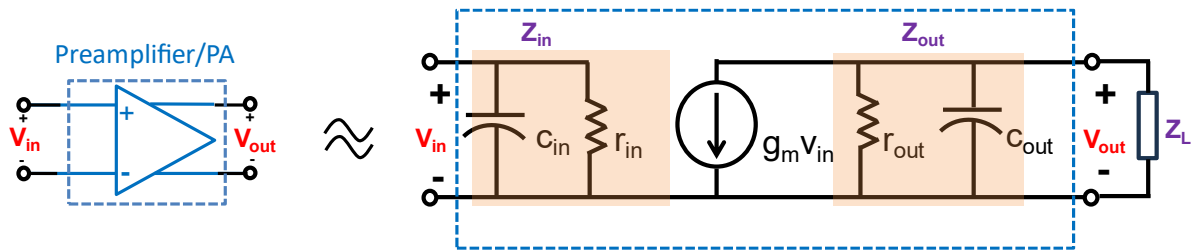


Fig. 6.2. Small-signal amplifier model

The voltage gain of the amplifier from the small-signal model is

$$G_{PreA/PA} = \frac{v_{out}}{v_{in}} = -g_m \cdot z_{out} \parallel z_L, \quad (6.2)$$

where z_{out} is the output impedance of the amplifier (i.e., $r_{out} \parallel c_{out}$), and z_L is the load, which in this case is the impedance seen looking into the input of the next stage. Substituting eq. (6.2) in eq. (6.1) gives the open-loop gain

$$G_{v,OL} = G_{br} \cdot \left[-g_{m,PreA} \cdot \frac{z_{out,PreA} \cdot z_{L,PreA}}{z_{out,PreA} + z_{L,PreA}} \right] \cdot \left[-g_{m,PA} \cdot \frac{z_{out,PA} \cdot z_{L,PA}}{z_{out,PA} + z_{L,PA}} \right], \quad (6.3)$$

Impedance z_{L-PreA} is seen at the output of the preamplifier looking into the bandpass filter network ($z_{in,BPF}$ in Fig. 6.1), and $z_{L,PA}$ is the impedance seen at the output of the PA looking into the bridge ($z_{in,Br}$ in Fig. 6.1). The loading present at the interfaces between stages, has a significant effect on the loop gain ($G_{v,OL}$), as seen from eq. (6.3). Therefore, each stage is designed to provide the required gain, including loading effects, while offering a suitable input impedance to interface with the preceding stage.

6.2 Tapped Resonator

The resonator for the bridge circuit can be a series L-C, parallel L-C, or a combination of both series and parallel L-C networks, as depicted in parts b, c, and d of Fig. 6.3.

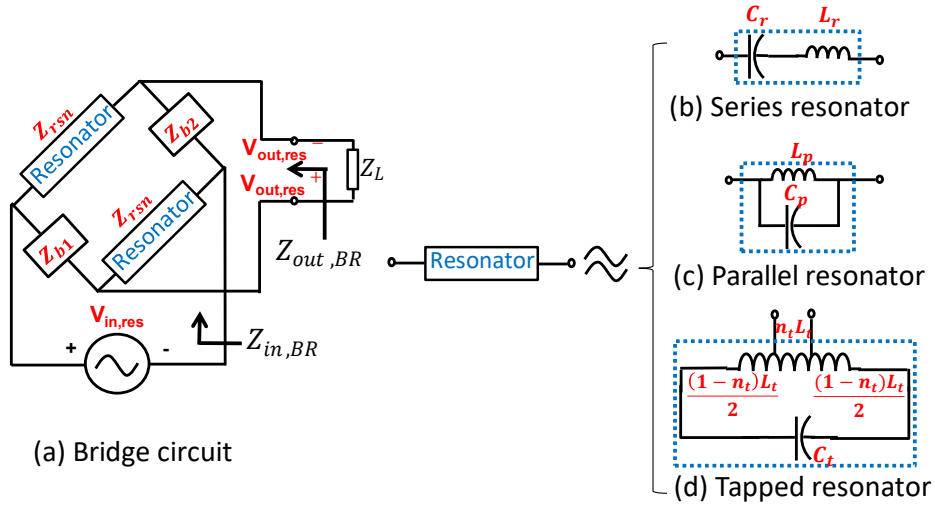


Fig. 6.3. Proposed bridge circuit with different L-C resonators

The small $R_{r,sn}$ value of 5Ω for the series bridge resonator (demonstrated in Chapter 4) results in an input impedance $Z_{in,BR}$ (e.g., see Fig. 4.1a) for the bridge which loads the PA stage driving the bridge in the oscillator. Moreover, the potential for breakdown of the series capacitor (C_r) due to the voltage swing (i.e., > 10 V) across it at resonance must be avoided. A parallel L-C resonator has an impedance peak at ω_{osc} , and lower values at frequencies away from resonance. However, a large $R_{r,sn}$ is also a problem from an oscillator design perspective, as it increases $Z_{out,BR}$ (e.g., see Fig. 4.1a). In other words, the source impedance seen by the stage following the bridge (i.e., preamplifier) must be considered as well.

A combination of both series and parallel resonances, as illustrated in Fig. 6.3Fig. 4.1d, is selected in this work for integrating the bridge resonator into an oscillator implantation to overcome the challenges of simple series or parallel resonators. It is realized using a tapped autotransformer. The exact value of $R_{r,sn}$ is determined from the physical layout. The coil inductance (L) is selected to optimize its Q factor at ω_{osc} . In Chapter 3, it is demonstrated that the Q-factor of a 2.5-nH inductor in the 22-nm FD-SOI CMOS technology peaks at 8 GHz (e.g., see Fig. 3.5b). A tapped autotransformer designed with a total self inductance of 2.5 nH (at low frequency), and tuned to 8 GHz gives an impedance value of 100Ω at resonance.

The resonant frequency (ω_{osc}) is

$$\omega_{osc} \approx \frac{1}{\sqrt{L_t C_t}}, \quad (6.4)$$

where L_t is the total inductance of the coil, and C_t is the capacitance across the inductor as shown in Fig. 4.1d. Assuming jX_b and $-jX_b$ for Z_{b1} and Z_{b2} , respectively, the voltage transfer function ($G_{br,t}$) of the tapped bridge circuit at ω_{osc} is derived from the voltage divider rule

$$G_{br,t}(\omega_{osc}) = \frac{V_{out}(\omega_{osc})}{V_{in}(\omega_{osc})} = \frac{Z_{rsn}(\omega_{osc})^2 - X_b^2}{Z_{rsn}(\omega_{osc})^2 + X_b^2}. \quad (6.5)$$

The equivalent impedance (Z_{rsn}) of the tapped resonator is the parallel combination of the $n_t L_t$ segment of the coil and the rest of the coil, $(1 - n_t)L_t$ in series with C_t . Neglecting the resistive loss (R_{rsn}), Z_{rsn} is therefore given by

$$Z_{rsn} \approx jX_{rsn} = j\omega n_t L_t \parallel j \left[\omega(1 - n_t)L_t - \frac{1}{\omega} \right] = \frac{j\omega n_t L_t [\omega^2(1 - n_t)L_t C_t - 1]}{\omega^2 L_t C_t - 1}, \quad (6.6)$$

where n_t is the ratio of the inductance across the tapped nodes with respect to L_t .

Since $\omega^2 L_t C_t$ is close to unity near resonance,

$$X_{rsn} \approx \frac{\omega n_t L_t [\omega^2(-n_t)L_t C_t]}{\omega^2 L_t C_t - 1} \quad (6.7)$$

and
$$\frac{dX_{rsn}(\omega)}{d\omega} \approx 2n_t^2 L_t. \quad (6.8)$$

A general formula for Q for the bridge circuit is given by eq. (4.9) in Chapter 4

$$Q_{br} = \frac{\omega_{osc}}{2} \cdot \frac{1}{1 + |v(\omega)|^2} \frac{dv(\omega)}{d\omega}, \quad (6.9)$$

where $v(\omega)$ is $\left[\text{Im} \left(G_{br,t}(\omega) \right) / \text{Re} \left(G_{br,t}(\omega) \right) \right]$.

Substituting eq. (6.6) in (6.5), and neglecting the second-order reactive term (X_{rsn}^2) in the vicinity of resonance, $v(\omega \rightarrow \omega_{osc})$ is given by

$$\begin{aligned} v(\omega \rightarrow \omega_{osc}) &= \frac{Im(G_{br,t}(\omega_{osc}))}{Re(G_{br,t}(\omega_{osc}))} \approx \frac{Im(Z_{rsn}(\omega_{osc})^2 - X_b^2)}{Re(Z_{rsn}(\omega_{osc})^2 - X_b^2)} \\ &= \frac{Im(R_{rsn}^2 + j2R_{rsn}X_{rsn} - X_{rsn}^2 - X_b^2)}{Re(R_{rsn}^2 + j2R_{rsn}X_{rsn} - X_{rsn}^2 - X_b^2)} = \frac{2R_{rsn}X_{rsn}}{R_{rsn}^2 - X_b^2}. \end{aligned} \quad (6.10)$$

Substituting eq. (6.10) in eq. (6.9) and neglecting $\frac{1}{1+|v(\omega)|^2}$, as $|v(\omega)|$ is significantly smaller than 1 near resonance, the loaded Q factor of the tapped bridge ($Q_{br,t,load}$) is given by

$$Q_{br,t,load} = \frac{\omega_{osc}}{2} \cdot \frac{dv(\omega)}{d\omega} = \omega_{osc} \cdot \frac{R_{rsn}}{R_{rsn}^2 - X_b^2} \cdot \frac{dX_{rsn}(\omega)}{d\omega} \cdot F_i. \quad (6.11)$$

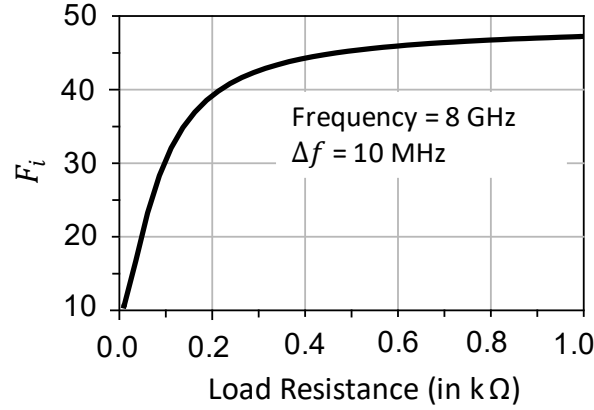
Parameter F_i is an empirical factor which is a function of frequency (it carries the discontinuity in phase response of the bridge), frequency step (Δf) for $\frac{d\varphi(\omega)}{d\omega}$, and value of the load impedance (Z_L) at the bridge output. The formula of $Q_{br,t,load}$ has two terms. One is $\left[\omega_{osc} \cdot \frac{R_{rsn}}{R_{rsn}^2 - X_b^2} \cdot \frac{dX_{rsn}(\omega)}{d\omega} \right]$, which depends on the intrinsic physical characteristics of the bridge. The other one is the empirical parameter F_i , which incorporates the impact of loading and discontinuity on the phase response of the bridge during closed-loop operation. Therefore, the first part is only derived to understand the design approach for the bridge circuit for high-Q performance. For simplicity, the derivation of F_i is not performed in this section.

Substituting eq. (6.8) in eq. (6.11), $Q_{br,t,load}$ for the tapped-resonator bridge is approximated by

$$Q_{br,t,load} = \frac{R_{rsn} \cdot \omega_{osc} \cdot n_t(1 - n_t)L_t}{(R_{rsn}^2 - X_b^2)} \cdot F_i = \frac{R_{rsn} \cdot \omega_{osc} \cdot 2n_t^2 L_t}{\Delta} \cdot F_i, \quad (6.12)$$

where Δ is $(R_{rsn}^2 - X_b^2)$. Fig. 6.4 shows the simulation results of F_i vs. load impedance at the bridge output (Z_L) for the tapped-resonator bridge and a frequency step of 10 MHz. The

value ranges from 10 to 47 for a load resistance of 10 Ω -1 k Ω at the bridge output, as shown in Fig. 6.4. Therefore, increasing the load increases the $Q_{br,t,load}$.



(b) F_i vs load Resistance (Z_L)

Fig. 6.4. Dependence of F_i on load resistance

Eq. (6.12) predicts that the quality factor of the tapped resonator bridge circuit depends on design parameters R_{rsn} , Δ , and the ratio n_t . There is a trade-off between $Q_{br,t,load}$ and gain, which is determined by R_{rsn} and Δ . Increasing Δ increases the gain but degrades $Q_{br,t,load}$. For a fixed Δ , a larger R_{rsn} gives lower gain and higher $Q_{br,t,load}$. To achieve a gain of 0.1 V/V at resonance for a 100- Ω R_{rsn} , an X_b of around 91 Ω is required from eq. (4.3). Physical layout of this 100- Ω tapped resonator are described in Section 6.2.2.

Eq. (6.12) also predicts that $Q_{br,t,load}$ is proportional to $n_t(1 - n_t)$. A value of 0.5 is chosen for the resonator, which maximizes $n_t(1 - n_t)$ and therefore $Q_{br,t,load}$. Fig. 6.4b predicts the F_i value for an open-circuit load is 95. The Q for an open-circuit load is therefore calculated from eq. (6.12) to be 140, with $R_{rsn} = 100 \Omega$, $X_b = 90 \Omega$, $n_t = 0.2$, $L_t = 2.5$ nH, and $F_i = 47$.

6.2.1 Closed-loop Performance of the Proposed Bridge

In a closed loop, the bridge is loaded by the input impedance of the preamplifier. The loading effect is analysed by simulating the bridge performance for different load impedances, as

illustrated in Fig. 6.5. In Fig. 6.5a, $|G_{br,t}|_{loaded}$ is the voltage gain of the bridge circuit when connected to a differential load (Z_L) at the output.

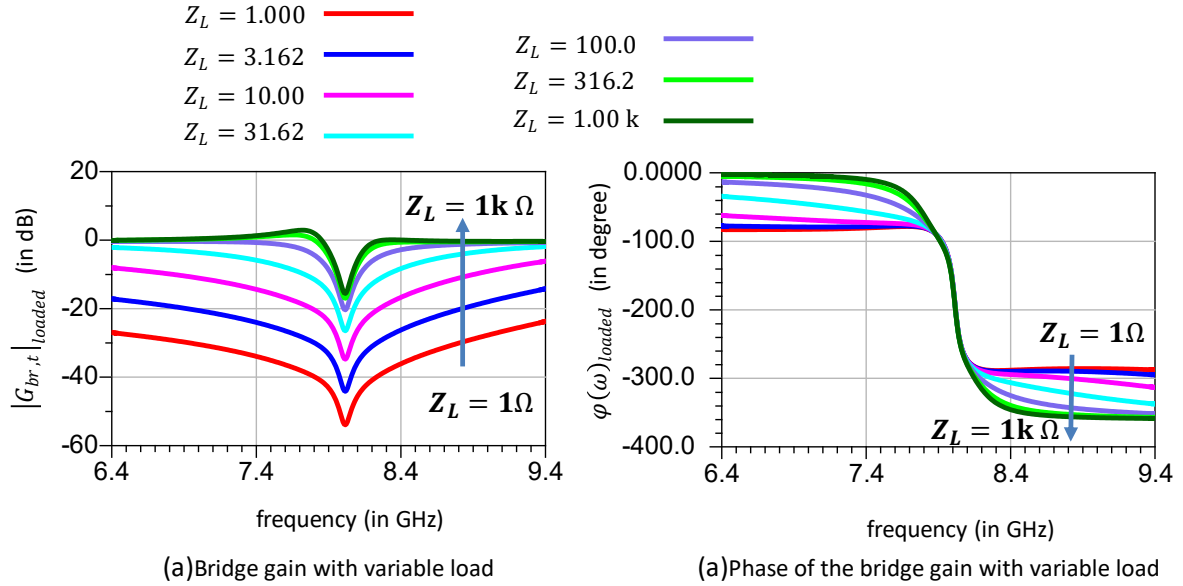


Fig. 6.5. Simulation results to show loading effects on bridge response

Fig. 6.5 shows that increasing the load increases the gain. However, from the phase plot in Fig. 6.5b, it is seen that increasing Z_L also increases the phase shift at frequencies above f_{osc} . In addition to this phase shift, there are also phase shifts caused by high-frequency poles from the L-C networks in the bridge and caused by parasitic capacitances of the amplifiers. These additional phase shifts can contribute to an overall phase shift of more than 720° in the phase response of the loop gain for the full oscillator. This creates the possibility of a secondary or unwanted parasitic oscillation. Lowering Z_L at the bridge output helps to suppress the secondary oscillation. A value between $10\text{--}80\ \Omega$ provides a phase lead of $15^\circ\text{--}70^\circ$ above f_{osc} , as compared to the phase shift for an open-circuit load (Fig. 6.5b). Therefore, the preamplifier input impedance target is set to $35\ \Omega$ to for a phase lead of 20° above f_{osc} .

6.2.2 Autotransformer Layout Design for Tapped Resonator

The tapped autotransformer is comprised of an inductor coil (L_t) and a tuning capacitor (C_t) as illustrated in Fig. 6.6. The ends of the coil (i.e., P3 and P4 ports) are the primary terminals, and the tapped nodes taken out of the coil (i.e., P1 and P2) are the secondary nodes.

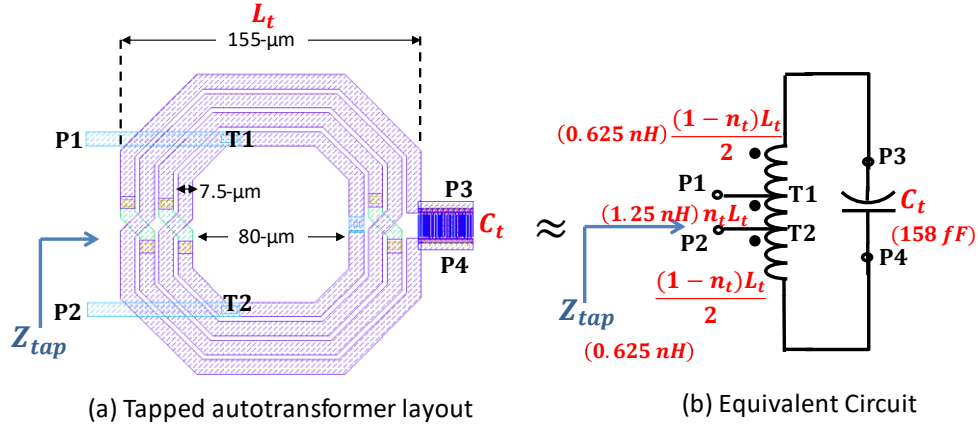


Fig. 6.6. Proposed tapped resonator

The impedance (Z_{tap}) seen between nodes P1 and P2 for the simplified equivalent circuit of Fig. 6.6 is given by eq. (6.6). The right side of eq. (6.6) has two complex conjugate poles and three zeros. The zero frequencies (ω_{z1} and $\pm\omega_{z2}$) are determined by equating the numerator terms ($\omega n_t L_t$) and $[\omega^2(1 - n_t)L_t C_t - 1]$ to zero. Similarly, the pole frequencies ($\pm\omega_{p1}$) are achieved by equating the denominator term ($\omega^2 LC - 1$) to zero:

$$\omega_{z1} = 0, \quad (6.13)$$

$$\omega_{z2} = \pm j \frac{1}{\sqrt{(1-n_t)L_t C_t}}, \quad (6.14)$$

$$\omega_{p1} = \pm j \frac{1}{\sqrt{L_t C_t}}. \quad (6.15)$$

The poles and zeroes lie on the imaginary axis of the s-plane. However, a practical autotransformer will have a real component resulting from losses that are ignored in the simplified calculation. The self inductance (L_t) and capacitance (C_t) are designed applying the

concepts (i.e., custom layout and floating shield optimization) from Section 3.1 and 3.2 to achieve a peak frequency (ω_{p1}) of 8 GHz (i.e., the desired resonant frequency) from eq. (6.15).

A 4-turn autotransformer physical layout is shown in Fig. 6.6a. An outer dimension of 155 μm , is chosen to realize the required inductance of 2.5 nH which gives Q peak at 8 GHz and an equivalent resistance of 108 Ω at ω_{osc} of 8 GHz. Capacitor (C_t) is designed to achieve a resonant frequency of 8 GHz. Thick (3 μm) copper metal layer, QB is used to implement the resonator coil. Postlayout electromagnetic simulation results of the magnitude and phase responses of Z_{tap} for the autotransformer are illustrated in Fig. 6.7.

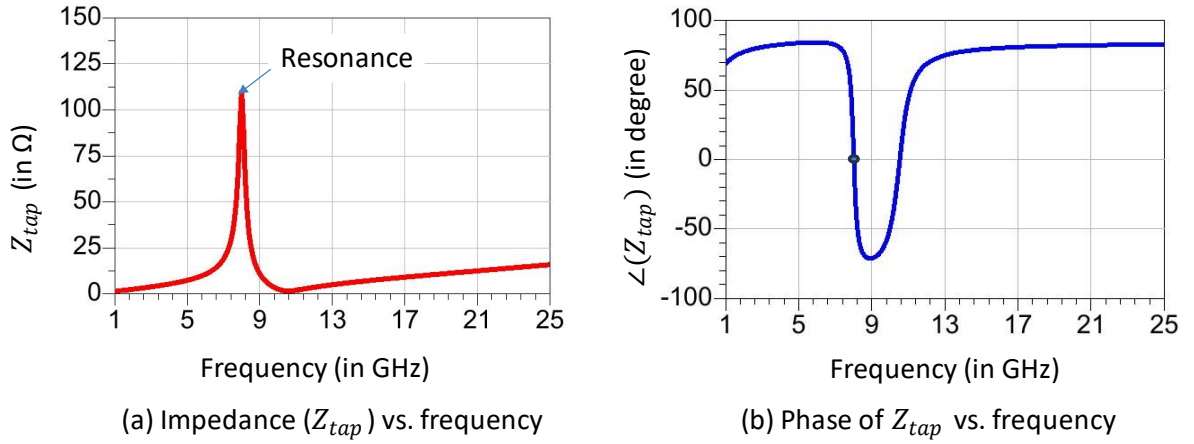


Fig. 6.7. Simulation results for resonator autotransformer

The magnitude of the impedance is 108.6 Ω at 8.1 GHz, as shown in Fig. 6.7a. The phase response from Fig. 6.7b illustrates the location of the zero at 11 GHz (blue curve). This is determined by the values of n_t , L_t , and C_t using eq. (6.14). The Q factor of the autotransformer (Q_{autoXF}), measured from the derivative of the phase of Z_{tap} , is plotted in Fig. 6.8. The result shows a Q of 27.8 at 8 GHz.

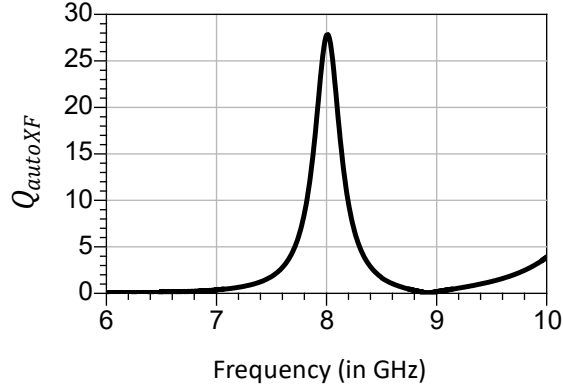


Fig. 6.8. Q factor of the tapped L-C autotransformer

6.2.3 Tapped Bridge Resonator Performance

This section presents details of the physical layout design of the full bridge circuit with a tapped resonator. The layout is formed by connecting two identical resonator autotransformers and the balancing inductor and capacitor, as illustrated in Fig. 6.9.

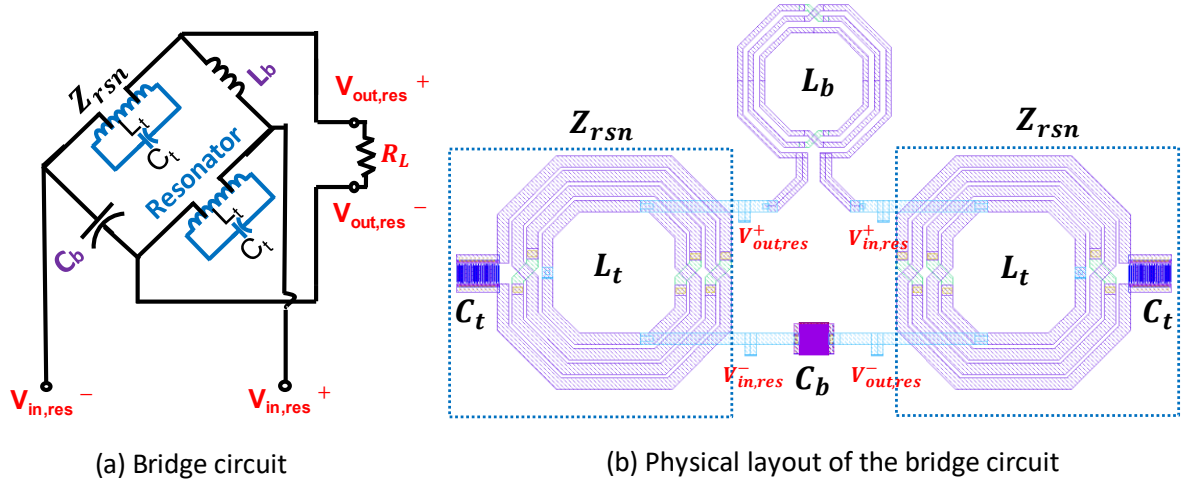


Fig. 6.9. Full bridge circuit layout

The load (R_L) value is $35 \, \Omega$ for the desired phase performance, as described in Section 6.2.1 from the closed-loop performance of the bridge. The balancing inductor (L_b) is a 3-turn coil in QB layer with 111- μm outer dimension, 3.5- μm conductor width, and 4- μm spacing between

the adjacent conductors, to realize an inductance of 1.8 nH (impedance X_b of $90\ \Omega$ as required for the bridge gain of 0.1 V/V for a $35\ \Omega$ load). The 221-fF balancing MOM capacitor (C_b) is implemented in C1, C2, and C3 metal layers with a cell dimension of $18.5\ \mu\text{m} \times 19\ \mu\text{m}$.

The component interconnects in Fig. 6.9b add unwanted inductance and capacitance. To minimize parasitics, interconnects are designed with thick top metals (i.e., LB, QB, and QA). Postlayout EM simulation results for voltage gain of the bridge with R_{rsn} of $108\ \Omega$ and X_b of $90\ \Omega$ (i.e., L_b of 1.8 nH and C_b of 221 fF) for a load (R_L) value of $35\ \Omega$ are shown in Fig. 6.10.

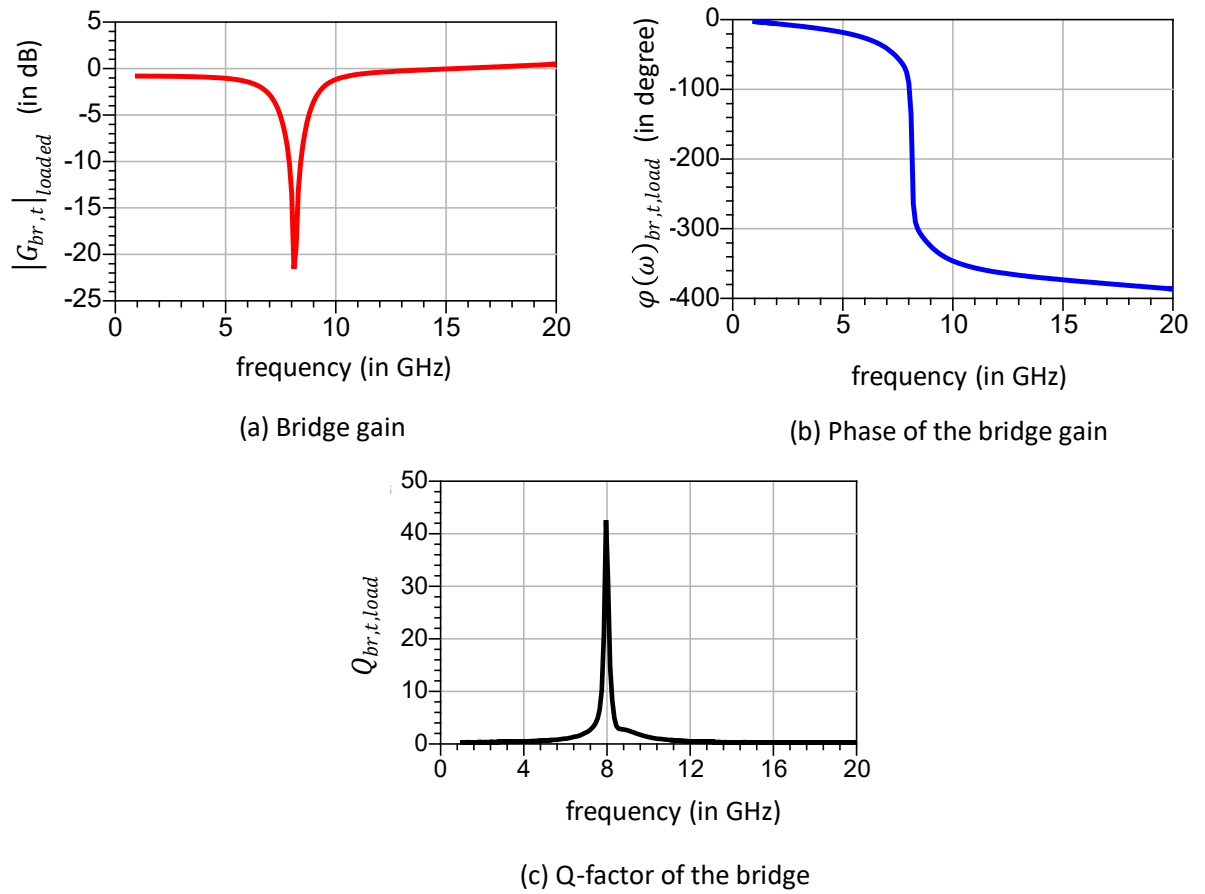


Fig. 6.10. Simulation results of the bridge circuit

The magnitude of the gain at resonance (Fig. 6.10a) is -20 dB (i.e., $|G_{br,t}|_{loaded} = 0.1$ at 8 GHz), which agrees with the value calculated from eq. (6.5) for R_{rsn} of $108\ \Omega$ and X_b of $98\ \Omega$.

A sharp phase response is noticed at 8 GHz from Fig. 6.10b, which predicts a loaded Q factor ($Q_{br,t,load}$) of 45 (see Fig. 6.10c) for 35- Ω load resistance (i.e., the input resistance of the preamplifier). The active circuits in the oscillator are designed to compensate for -20 dB loss of the loaded bridge circuit.

6.3 Phase-Noise Analysis

The bridge consists of only L and C passive components, designed for minimal ohmic losses. Therefore, there is minimal thermal noise and no flicker noise sources in the bridge circuit. With high-Q bridge components, the dominant noise sources are thermal and flicker noise generated by transistors in the amplifiers. These noise sources are modelled by equivalent noise sources connected at the amplifier inputs and outputs, as shown in Fig. 6.11. Three noise current sources ($\overline{i_{n1}^2}$, $\overline{i_{n2}^2}$, and $\overline{i_{n3}^2}$) placed on the three interface nodes A, B, and C are shown in Fig. 6.11.

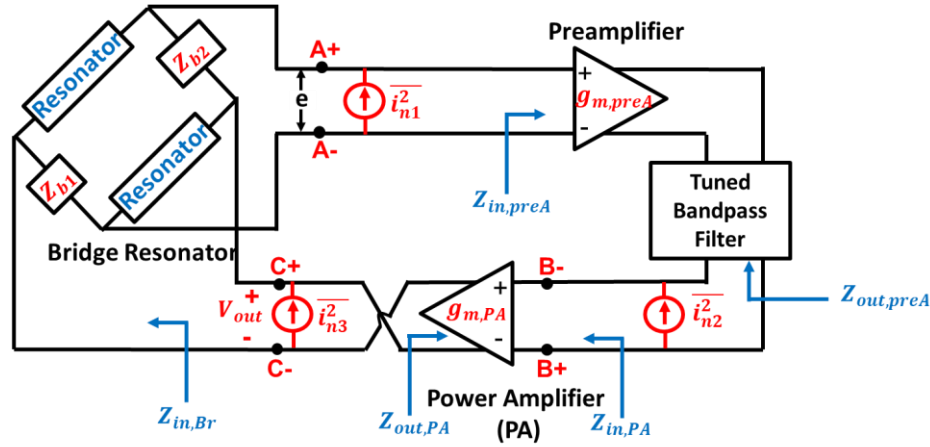


Fig. 6.11. Noise model for the bridge oscillator circuit

The mean-square noise voltage at node A ($\overline{v_{n1}^2}$) is defined to be the product of mean-square noise current ($\overline{i_{n1}^2}$) and the square of the magnitude of the impedance seen by $\overline{i_{n1}^2}$, which is

$$\overline{v_{n1}^2} = \overline{i_{n1}^2} \cdot |Z_{in,preA} \parallel Z_{out,Br}|^2. \quad (6.16)$$

At node B, the noise due to $\overline{i_{n1}^2}$ is

$$\overline{i_{n1}^2}\Big|_{at\ B} = \overline{v_{n1}^2} \cdot |g_{m,preA}|^2, \quad (6.17)$$

where $g_{m,preA}$ is the transconductance of the preamplifier stage. The total noise power at node B is therefore

$$\overline{i_{nB}^2} = \overline{i_{n1}^2}\Big|_{at\ B} + \overline{i_{n2}^2}. \quad (6.18)$$

The total mean-square noise current at node C is derived similarly as

$$\begin{aligned} \overline{i_{nC}^2} &= \overline{i_{nB}^2} \cdot |Z_{in,PA} \parallel Z_{out,preA}|^2 \cdot (g_{m,PA})^2 + \overline{i_{n3}^2} \\ &= [(Z_{in,preA} \parallel Z_{out,Br}) \cdot g_{m,preA} \cdot (Z_{in,PA} \parallel Z_{out,preA}) \\ &\quad \cdot (g_{m,PA})]^2 \overline{i_{n1}^2} \\ &\quad + [(Z_{in,PA} \parallel Z_{out,preA}) \cdot (g_{m,PA})]^2 \overline{i_{n2}^2} + \overline{i_{n3}^2}. \end{aligned} \quad (6.19)$$

Eq. (6.19) reveals that $\overline{i_{n1}^2}$ has the largest effect on $\overline{i_{nC}^2}$, as it is multiplied by both the preamplifier and PA gains. This effect was verified by system-level phase noise simulations described in Appendix B (see Fig. B. 3). Therefore, noise generated at the input of the preamplifier will typically dominate the total noise power of the oscillator.

The phase noise of the oscillator circuit is derived applying the Leeson's linear feedback model described in Section 2.3.1:

$$L(\omega_p) = \frac{\overline{v_{nC}^2}/V_{out,peak}^2}{|1 - H_{br}(\omega_p)|^2} = \frac{|Z_{in,Br}(\omega_0 + \omega_p)|^2 \cdot \overline{i_{nC}^2}}{V_{out,peak}^2} \cdot \left[1 + \left(\frac{\omega_0}{2\omega_p Q_{br}} \right)^2 \right], \quad (6.20)$$

where $H_{br}(\omega_p)$ is the low-pass equivalent transfer function of the band-pass bridge circuit with a half-bandwidth of $\omega_0/2Q_{br}$.

In eq. (6.20), $Z_{out,PA}(\omega_0 + \omega_p)$ is assumed to be significantly larger than $Z_{in,Br}(\omega_0 + \omega_p)$. The bridge impedance ($Z_{in,Br}$) is given by

$$Z_{in,Br}(\omega) = [Z_{rsn}(\omega) + jX_b(\omega)] \parallel [Z_{rsn}(\omega) - jX_b(\omega)] , \quad (6.21)$$

$$Z_{in,Br}(\omega_0 + \omega_p) = \frac{R_{rsn}^2 + X_b^2 + jR_{rsn}X_b \left[(1+m) - \frac{1}{1+m} \right]}{2R_{rsn} + jX_b \left[(1+m) - \frac{1}{1+m} \right]} . \quad (6.22)$$

Parameter m is the ratio of ω_0 to ω_p (ω_p/ω_0). For ω_p of 1 MHz and ω_0 of 8 GHz, m is significantly smaller than 1, and $\left[(1+m) - \frac{1}{1+m} \right]$ is approximated by just m . Assuming that $(R_{rsn}^2 + X_b^2)$ is significantly larger than $R_{rsn}X_b m$ and that $2R_{rsn}$ is significantly larger than $X_b m$, eq. (6.22) can be simplified to

$$Z_{in,Br}(\omega_0 + \omega_p) = \frac{R_{rsn}^2 + X_b^2}{2R_{rsn}} . \quad (6.23)$$

Using eqs. (4.6) and (6.12) from Chapter 4 to determine $\frac{R_{rsn}^2 + X_b^2}{2R_{rsn}}$ and substituting the result in to eq. (6.23) gives

$$|Z_{in,Br}(\omega_0 + \omega_p)| = \frac{\omega_0 n_t (1-n_t) L_t}{2G_{br,t}(Q_{br,t,load}/F_i)} . \quad (6.24)$$

Finally, the phase noise of the bridge oscillator is obtained by substituting eq. (6.24) in eq. (6.20),

$$L(\omega_p) = \frac{\overline{i_{nC}^2}}{V_{out,peak}^2} \cdot \left[\frac{\omega_0 n_t^2 L_t}{G_{br,t}(Q_{br,t,load}/F_i)} \right]^2 \cdot \left[1 + \left(\frac{\omega_0}{2\omega_p Q_{br}} \right)^2 \right] . \quad (6.25)$$

Eq. (6.25) gives useful insights into a low-phase-noise bridge oscillator design. The design variables are chosen to achieve the target phase noise (i.e., < -130 dBc/Hz at 1 MHz offset). Table 6.1 shows an example calculation of phase noise using eq. (6.25) for the bridge proposed in the previous section.

Table 6.1. Phase noise calculation example

Parameters	Values
$G_{br,t}$	0.1 V/V
$Q_{br,t,load}$	40
L_t	2.5 nH
f_0	8 GHz
n_t	0.5
$V_{out,peak}$ (achieved by cascoding a 1.8-V breakdown MOSFET with a 0.8-V breakdown MOSFET from the 22-nm FD-SOI technology to maximize output voltage swing)	2.6 V
$\overline{i_{nc}^2}$ (measured from simulation)	$4 \times 10^{-21} \frac{A^2}{Hz}$
F_i for a bridge load of 35Ω (ref. Fig. 6.4).	16
$L(1 MHz)$ calculated from eq. (6.25)	-137.1 dBc/Hz

Eq. (6.25) is validated by system-level simulation shown in Appendix B. Using the same design values used for above calculation, the simulation shows a phase noise of -136.8 dBc/Hz at 1-MHz offset (see Fig. B. 2 on page 143) which is very close to the calculated value.

6.4 Summary and Design Approach for Low Phase-Noise

A theoretical analysis of the proposed integrated bridge oscillator and its performance is presented in this chapter. As predicted from the phase noise formula in eq. (6.25), the resonator autotransformer parameters (n_t and L), the loaded bridge gain G_{br} and the loaded Q factor of the bridge Q_{br} are important passive design parameters.

Higher output power from the PA is needed to realize low phase noise from the oscillator (ref. eq. (6.25)), which is achieved by increasing the PA output voltage swing $V_{out,peak}$. For the 1.8-V breakdown EGSLVT transistors available in the 22-nm SOI-CMOS technology,

2.6-V peak swing is achievable using a cascode topology. Internal voltage swings also depend on breakdown voltages of the passive devices in the technology. There are several high-voltage passive options in the 22-nm SOI-CMOS technology (e.g., 10-V MOM capacitors). This limit is raised by using custom designs in the passive layout as discussed in Chapter 3. Thicker top metals are utilized to design robust, and high-breakdown (> 30 V) passive components.

Another factor contributing to the phase noise is the mean-square noise current, $\overline{i_{nC}^2}$. This is dependent (thermal and flicker noise in the MOSFET preamplifier). Designing the preamplifier for lowest phase noise is therefore critical to the oscillator performance.

As seen from eq. (6.19), the gain of the PA stage should be made small for better phase noise performance, while providing gain sufficient to sustain oscillation. A small-signal gain of 4 V/V for the PA is therefore targeted for the proposed design. These leaves a gain requirement of 10 V/V from the preamplifier for a loop gain of 4 V/V assuming a bridge circuit gain (G_{br}) of 0.1 V/V. Amplifier designs are presented in Chapter 7.

Chapter 7

Integrated Bridge Oscillator Implementation

In this chapter, the design of a fully integrated oscillator using a bridge resonator in 22-nm FD-SOI CMOS technology is described.

7.1 Active Circuit Blocks

Design of the active circuit blocks (i.e., preamplifier and PA blocks) is facilitated by the 22-nm technology, which offers several different types of MOSFETs.

7.1.1 Transistor Options in 22-nm SOI CMOS Technology

The 22-nm SOI-CMOS technology offers body bias trimming of a fully depleted SOI transistor. This permits adjustment of the threshold voltage (V_{TH}), which affects the transistor's DC bias current and transconductance [25]. Forward body bias (i.e., applying a positive voltage to the body of an NFET, or negative voltage to the body of a PFET with respect to the source) lowers V_{TH} , resulting in a higher bias current. Similarly, a reverse body bias raises V_{TH} to lower the drain current, which is used in digital ICs to control leakage currents in the 'off' state.

The technology process design kit (PDK) offers two types of transistors with varying V_{TH} (i.e., SLVT and LVT). The PDK also offers multiple back-end-of-line (BEOL) options. Transistor p-cell models include the interconnect parasitics of transistor metallization up to the first metal layer (M1), or metals up to the fifth layer (C3) for RF applications. The differences between the models is primarily the additional parasitic capacitances between transistor terminals caused by metal interconnections. Thick-gate-oxide transistors are also offered (e.g., EGSLVT and EGLVT). The thicker oxide provides higher breakdown and a wider operating voltage range (e.g., instead of SLVT with 0.8V nominal supply, EGSLVTs support 1.2 V, 1.5 V, or 1.8 V supplies). The SLVT transistors have lower V_{TH} limit, and higher transconductance than the LVTs. Therefore, SLVT transistors are a good choice for low-noise and high-gain analog/RF designs. To endure the voltage swing anticipated at the output of the

oscillator in large-signal operation, the EGSLVT transistors with more than 4-V drain-to-source breakdown voltage are selected for the power amplifier design.

7.1.2 Power Amplifier Circuit

The purpose of the power amplifier (PA) in the oscillator is to provide small-signal gain (~ 4 V/V) and limit the oscillator output voltage swing for sustained oscillation. A MOSFET common-source amplifier is a good option for limiting, as the output voltage is clipped due to the finite power supply.

7.1.2.1 Topology and Design Methods

The PA topology used in this design is illustrated in Fig. 7.1a. It is a differential NMOS cascode amplifier designed for high-output voltage swing. High-breakdown (drain-to-source breakdown voltage of more than 4 V) EGSLVT NFET transistors are used as M_n and M_c to realize higher output voltage swing.

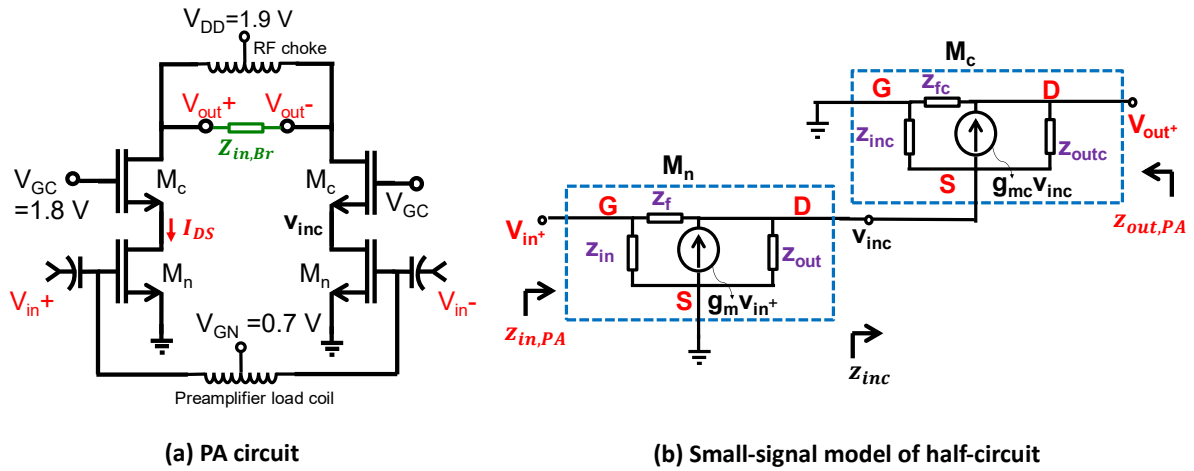


Fig. 7.1. Power amplifier circuit

The cascode topology allows a (single ended) maximum peak voltage swing of $V_{DD} - 2V_{DS,sat}$, where $V_{DS,sat}$ is the knee voltage of the transistor.

The average output power (P_{avg}), in terms of differential peak output voltage swing (V_{od-p}) and differential bridge impedance ($Z_{in,Br}$, ref. Fig. 6.1), is given by

$$P_{avg} = \left(\frac{V_{od-p}}{\sqrt{2}} \right)^2 \frac{1}{Z_{in,Br}}. \quad (7.1)$$

A P_{avg} of 35 mW dissipated by a $100\text{-}\Omega$ $Z_{in,Br}$ is targeted to realize an oscillator phase noise of below -130 dBc/Hz at 1-MHz offset. This gives a V_{od-p} of 2.5 V from eq. (7.1). Assuming a $V_{DS,sat}$ of 0.3 V for the EGSLVT NFET and V_{DD} of 1.9 V

$$V_{od-p} = 2(V_{DD} - 2V_{DS,sat}) = 2.5 \text{ V}. \quad (7.2)$$

The transistor widths are determined by the required small-signal voltage gain. The voltage gain (G_{preA}), input ($z_{in,preA}$) and output ($z_{out,preA}$) impedances from a small-signal analysis of the half-circuit model in Fig. 7.1b. Ignoring z_f and z_{fc} for simplicity, these are given by

$$G_{PA} \approx -g_m(z_{out,PA} \parallel Z_{in,Br}/2), \quad (7.3)$$

$$z_{out,PA} \approx (1 + g_{mc}z_{outc})z_{out} + \frac{z_{out,pc}}{z_{out}}, \quad (7.4)$$

$$z_{in,PA} \approx z_{in}, \quad (7.5)$$

where g_m , z_{in} , and z_{out} are the transconductance, gate-to-source, and drain-to-source impedances of M_n , respectively. The transconductance, gate-to-source, and drain-to-source impedances of M_c are g_{mc} , z_{inc} , and z_{outc} , respectively. Assuming $z_{out,PA}$ is significantly larger than $Z_{in,Br}$ in eq. (7.3), a g_m for M_n of 80 mS is required for a voltage gain of 4 V/V when $Z_{in,Br}$ is $100\text{ }\Omega$. The V_{GS} for M_n is set close to the threshold voltage to ensure operation between class-A and class-B for higher efficiency while keeping the swing large (ref. Fig. 2.5 in Section 2.5.1). Therefore, the V_{GS} is chosen to be 0.7 V with a DC bias current of 16 mA. For these V_{GS} and g_m values, the width of the transistor is determined to be 192- μm . For simplicity, the width of M_c is made the same.

7.1.2.2 Simulation Results

Small-signal post-layout simulation results for the PA are shown in Fig. 7.2. A voltage gain of 3.95 V/V at 8-GHz is achieved as depicted by Fig. 7.2a. A phase shift of approximately 30° is seen at 8-GHz. This output phase shift is caused by the parasitic capacitances of the transistors (dominated by z_{outc} in Fig. 7.1a). In the oscillator, the phase lag is compensated by the phase-lead of the preamplifier.

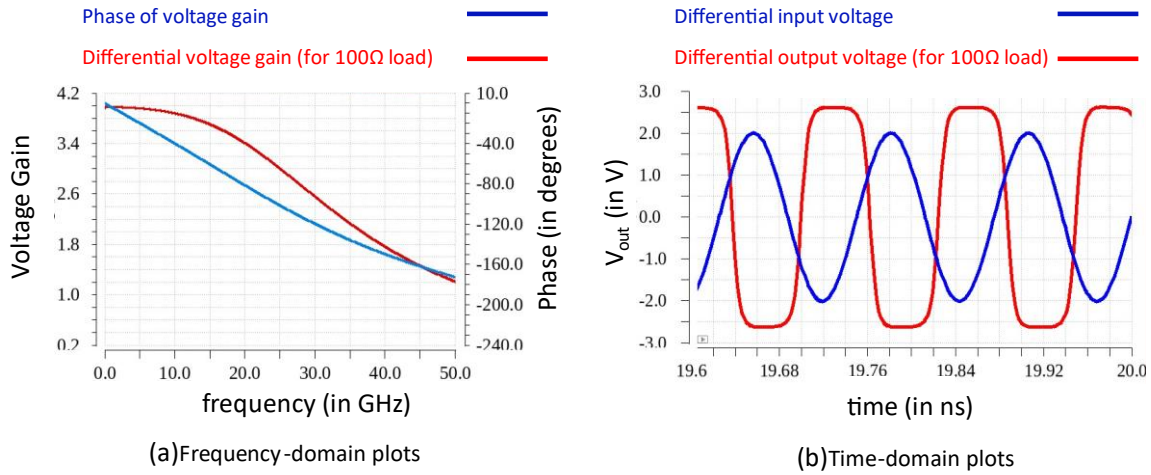


Fig. 7.2. Post-layout simulation results for the PA

The time-domain results are illustrated in Fig. 7.2b. It shows that the output differential voltage is limited at approximately 2.5-V by clipping, which agrees with the estimation made in Section 7.1.2.1. The large-signal post-layout simulation result for the transfer curve (i.e., V_{out} vs V_{in}) is illustrated in Fig. 7.3. Limiting of the output voltage swing is achieved by the PA at $2.5 V_{pk}$.

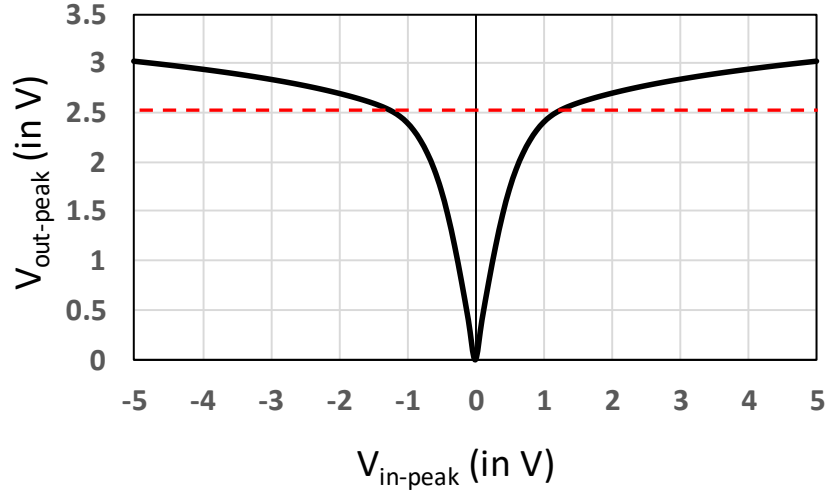


Fig. 7.3. Transfer curve for large-signal post-layout simulations of the PA

7.1.3 Pre-Amplifier Circuit

To achieve a loop gain greater than unity, the resonator is coupled to two stages of amplification. The preamplifier first stage loads the bridge and determines its closed-loop behaviour. This section provides details of the preamplifier design, and post-layout simulation results.

7.1.3.1 Proposed Topology and Design Methods

An oscillator loop gain greater than one is necessary for oscillation, as seen from eq.). Therefore, the target for the small-signal loop gain ($G_{v,OL}$) is 4 to maintain a safe margin. With a bridge stage gain (G_{br}) of 0.1 V/V (from Section 4.1), and a PA gain of 4 V/V, the voltage gain required from the preamplifier (G_{preA}) is approximately 10 V/V.

The proposed preamplifier circuit is illustrated in Fig. 7.4a. A common-gate (CG) cascode topology is implemented with PMOS transistors M_p and M_{pc} .

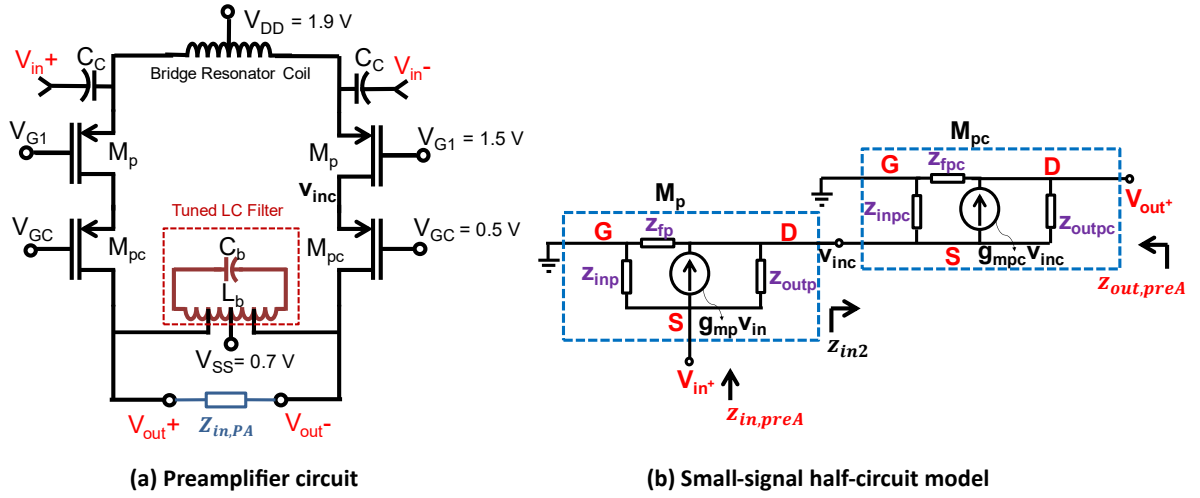


Fig. 7.4. Preamplifier circuit

A PMOS topology is used to simply biasing of the PA input when DC coupled to the preamplifier output. The drain of preamplifier output transistor (M_{pc}) is connected to the gate of the transistor at the PA input at node B (ref. Fig. 6.11). The DC voltage applied to the gate of the transistor must exceed the gate oxide breakdown voltage. For example, the SLVT transistors in the 22-nm FD-SOI CMOS technology has a V_{GS} limit of ± 0.9 V, whereas the V_{DS} breakdown voltage is specified at more than 3 V, depending on the width of the transistor. Therefore, an interface of NMOS gate with a PMOS drain allows a low bias voltage of 0.7 V. In this way, breakdown is avoided for high voltage swings at this node.

The noise generated by the preamplifier affects the phase-noise performance of the oscillator, as seen from eq. (6.19). The preamplifier design is therefore optimized for low-noise performance. To minimize noise, the input transistor M_p is biased at the optimum current density $\left(\frac{I_{DS}}{W}\right)$ for minimum mean-square noise voltage referred to the input of the amplifier. The mean-square noise voltage at the source of common-gate SLVT PFET with 10- μm width and 20-nm length is plotted in Fig. 7.5 against $\left|\frac{I_{DS}}{W}\right|$ and V_{SG} ($V_{SD} = 0.8$ V). Of the different types of transistors offered by the technology, the SLVT PFET has one of the lowest mean-square

noise voltage values for an $\left|\frac{I_{DS}}{W}\right|$ between 0.1-0.2 mA/ μ m, as shown in Fig. 7.5a. This gives a V_{SG} of 0.4 V for M_p , as seen from Fig. 7.5b.

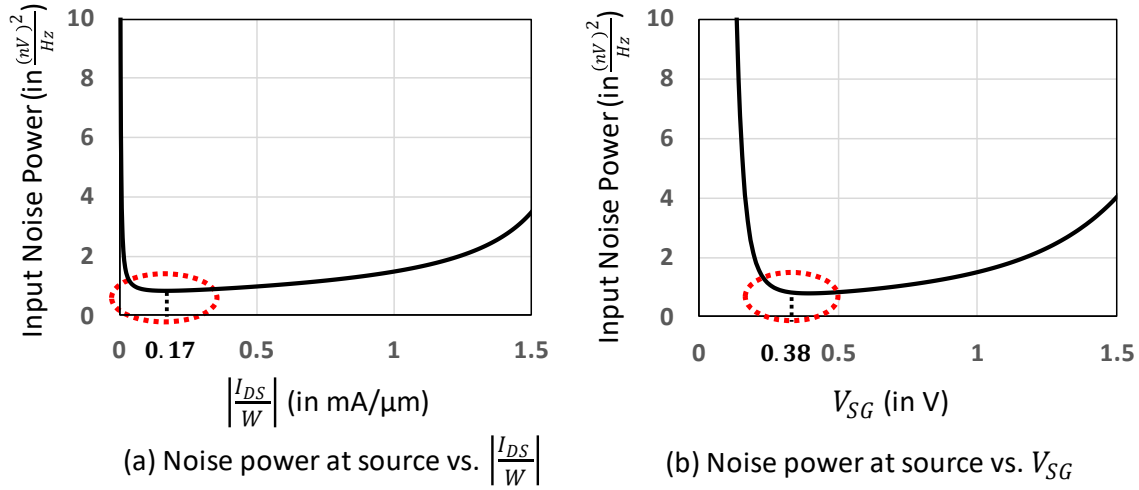


Fig. 7.5. Mean-square noise voltage at the source of a SLVT PMOS transistor

The width of M_p is then determined by the transconductance required for a voltage gain of 10 V/V. The voltage gain (G_{preA}), input ($z_{in,preA}$) and output ($z_{out,preA}$) impedances are determined from small-signal analysis of the half-circuit in Fig. 7.4b. Ignoring z_{fp} and z_{fpc} for simplicity, as their values are negligible at low frequency, these are given by

$$G_{preA} \approx g_{mp}(z_{out,preA} \parallel (z_{in,PA} \parallel z_{lc})/2), \quad (7.6)$$

$$z_{out,preA} \approx (1 + g_{mpc}z_{outpc})[(1 + g_{mp}z_{outp})z_{outbr} + z_{outp}] + z_{out,pc}, \quad (7.7)$$

$$z_{in,preA} \approx \frac{z_{in2} + z_{outp}}{(1 + g_{mp}z_{outp})}, \quad (7.8)$$

where g_{mp} , z_{inp} , and z_{outp} are the transconductance, gate-to-source, and drain-to-source impedances of M_p , respectively (ref. Fig. 7.4b). The transconductance, gate-to-source, and drain-to-source impedances of M_{pc} are g_{mpc} , z_{inpc} , and z_{outpc} , respectively. The impedance seen looking into the source of M_{pc} is z_{in2} .

The preamplifier input impedance ($z_{in,preA}$) affects the closed-loop phase response of the bridge. If $z_{in,preA}$ is too small, it loads the bridge output and reduces the closed-loop gain. On the other hand, when $z_{in,preA}$ is large, it increases the closed-loop phase shift of the bridge at high frequency, increasing the likelihood of oscillation at $2 \times 360^\circ$ phase, as discussed in Section 6.2.1. The optimum value of load impedance for the bridge (determined from simulations, see Fig. 6.5) is between 30Ω and 40Ω . The g_{mp} required to realize a $z_{in,preA}$ of 33Ω is calculated from eq. (7.8) to be 65 mS. The width for M_p that results in a g_{mp} of 65 mS, for a V_{SG} of 0.4 V (ref. Fig. 7.5b) is $30 \mu\text{m}$.

The cascode topology with M_{pc} improves the output voltage swing, as it allows the single-ended maximum peak voltage swing to be $(V_{DD} - V_{ss} - 2V_{SD,sat})$, where $V_{SD,sat}$ is the knee voltage for the transistors. The input of the preamplifier is connected to the PA output node via a resonator (see Fig. 6.11). Therefore, bias current is sourced from the 1.9-V supply PA. The preamplifier output, on the other hand, is connected to the PA input. Therefore, V_{ss} is sourced from the gate bias of the PA transistor's input, which is set to 0.7 V. This gives a maximum single-ended swing of approximately 1 V. To endure this large-signal voltage at the drain of M_{pc} , a 1.8-V EGSLVT high-breakdown transistor is chosen from the 22-nm technology library. The cascode topology increases the output impedance of the amplifier ($z_{out,preA}$). The width of the M_{pc} transistors for the preamplifier are chosen to be $90 \mu\text{m}$, which results in a $z_{out,preA}$ of $1 \text{ k}\Omega$.

With g_{mp} of M_{pc} determined from noise consideration, and making $z_{out,preA}$ as large as possible, the preamplifier gain (G_{preA} in eq. (7.6)), is dependent on the filter impedance, Z_{lc} . For this reason, Z_{lc} is optimized by the coil physical layout, as described in the following section.

7.1.3.2 Preamplifier Output Shaping

The L-C bandpass filter load of the preamplifier in Fig. 7.4 causes the voltage gain to peak at f_{osc} . As the output impedance of the preamplifier ($z_{out,preA}$) and the input impedance of the

PA ($z_{in,PA}$) are designed to be higher than 1 k Ω , the preamplifier load is determined by the impedance of the L-C filter (Z_{lc}) in eq. (7.6). The design of the tapped autotransformer for the preamplifier L-C filter load is similar to that of the tapped resonator discussed in Section 6.2.2. Selecting a larger inductance coil (L) gives a higher Z_{lc} (ref. eq. (6.6)), but at the cost of higher parasitic and ohmic loss as the metal footprint increases. The load network is designed to have a Z_{lc} of 600 Ω . This gives a voltage gain of approximately 12 V/V from eq. (7.6) assuming $z_{in,PA}$ of 2 k Ω and $z_{out,preA}$ of 1 k Ω .

7.1.3.2.1 Tapped Autotransformer for L-C Filter

The 5-turn coil designed for the preamplifier L-C filter with outer dimension of 142 μm and conductor width of 6.5 μm , is shown in Fig. 7.6a. It has an inductance of 3.4-nH for peak Z_{tap} of 678 Ω . The poles ($\pm\omega_{p1}$) and zeros (ω_{z1} and $\pm\omega_{z2}$) are

$$\omega_{z1} = 0 , \quad (7.9)$$

$$\omega_{z2} = \pm \frac{1}{\sqrt{(1-n_t)LC}} , \quad (7.10)$$

$$\omega_{p1} = \pm \frac{1}{\sqrt{LC}} . \quad (7.11)$$

A capacitance of 62 fF is added to tune the load to 8 GHz. The capacitor is implemented in top-metal layers QB and QA (same as the coil) to simplify the physical layout, and reduce parasitic capacitance between the interconnect metal and the substrate. The post-layout electromagnetic (EM) simulation results for the tuned circuit are illustrated in Fig. 7.7. The magnitude of the impedance is 678 Ω at 8.1 GHz (see Fig. 7.7a.) The phase response from Fig. 7.7b illustrates the location of the zero at 14 GHz (blue curve).

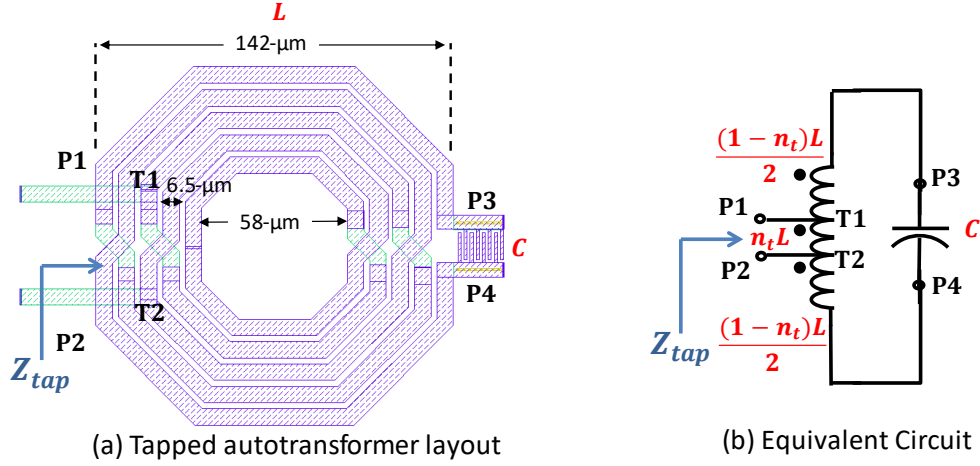


Fig. 7.6. Tapped autotransformer design

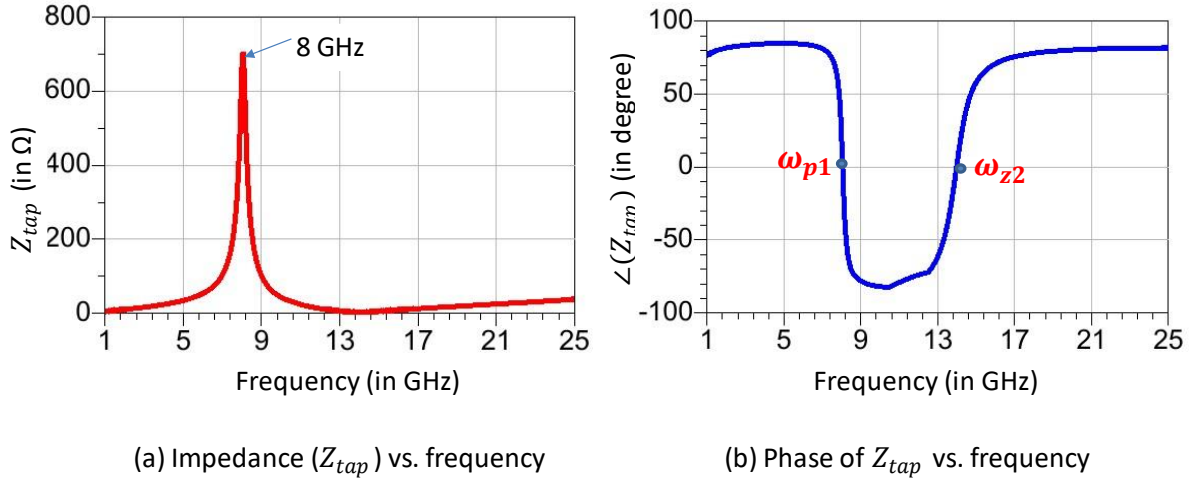


Fig. 7.7. Impedance of tapped autotransformer for the preamplifier L-C filter

The frequency of the zero (ω_{z2}) is tuned by selecting the tapping ratio (n_t), as predicted from eq. (7.11). This ratio varies with the location of terminals T1 and T2 in Fig. 7.6a. A ratio of 0.67 sets ω_{z2} to 14 GHz, which causes the 180° change in the phase response of Fig. 7.7b.

A ω_{z2} closer to ω_{p1} is desired to prevent the loop phase shift of an oscillator exceeding -720° , which is necessary to prevent secondary oscillation. On the other hand, a higher Z_{tap} is desired for achieving higher gain from the preamplifier. A balance is therefore made, with peak

Z_{tap} of 678Ω and ω_{z2} of 14 GHz, as determined from the oscillator loop gain requirements described in Chapter 6.

7.1.3.3 Simulation Results of the Preamplifier

Small-signal post-layout simulation results of the preamplifier are shown in Fig. 7.8a. As shown in the solid red plot, a voltage gain (G_{preA}) of 10 V/V is achieved for a 1 k Ω load at a frequency of 7.99-GHz. The dashed traces represent the gain and phase for the preamplifier only (without the L-C load filter). This illustrates the shifts in peak gain and change in voltage gain at the desired oscillation frequency (i.e., peak of the solid red plot is at 8 GHz) as the L-C bandpass filter is added. Large-signal simulation results are shown in Fig. 7.8b. A voltage gain of 10 V/V for an input of 100-mV is obtained. The mean-square noise current at the input of the preamplifier is $7.4 \times 10^{-22} \frac{A^2}{Hz}$ from simulation.

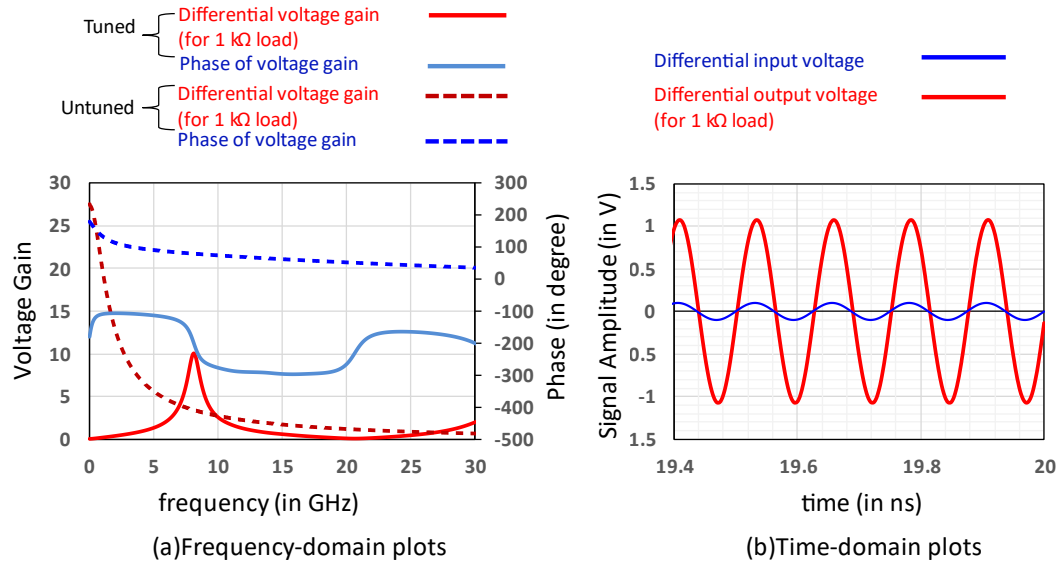


Fig. 7.8. Post-layout simulation results for the preamplifier

7.2 Biasing of Active Circuits

The biasing scheme used in this work is illustrated in Fig. 7.9. The active circuits need bias voltages at the gates of M_p , M_{pc} , and M_c . These are provided through the DC bias pads marked

in yellow as V_{g1} , V_{gpc} , and V_{gc} , respectively. The gate of M_n and the drain of M_{pc} shares the bias voltage at node B. Coil L_B of the tuned L-C filter network is used to supply bias to node B from the DC pad marked V_{ss} . Node A and node C in Fig. 7.9 share bias voltages supplied through the L_r coils of the bridge circuit. The bias voltage at this node is applied at the tap of one of the L_r coils from bias pad, V_{DD} . In this way, the drain of M_c and the source of M_p are connected to the V_{DD} supply. All bias nodes act as small-signal grounds, reducing the effect of thermal noise from voltage references on the phase noise of the oscillator. Laboratory power supplies are used as bias sources for the prototype developed in this work. However, the effects of noise produced by on-chip bias sources on performance is a subject for further study of the bridge resonator oscillator.

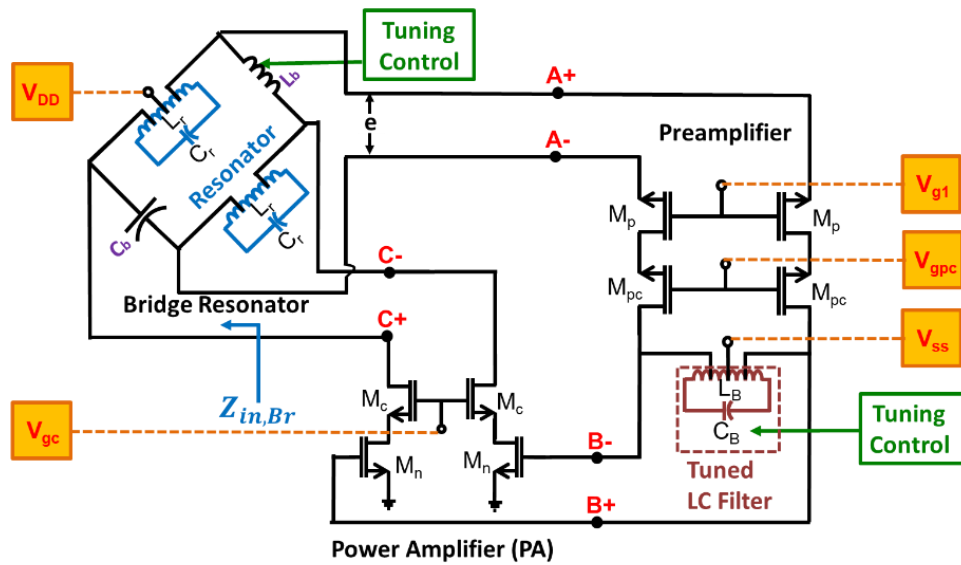


Fig. 7.9. Oscillator bias scheme

The advantage of this approach is that there is no need for extra biasing coils. The coils already used in the design are utilized, which conserves chip area. However, as the V_{DD} node creates an AC ground at the centre-tap of one coil of the bridge, the response of the bridge in the common-mode shifts, requiring re-balancing of the bridge. This effect may be treated as an advantage, as the imbalance created by the bridge bias increases the bridge gain by 10%. However, it comes with the cost of Q degradation by approximately the same amount. As the

phase noise depends both on the bridge gain and Q factor (eq. (6.12)), the overall phase-noise performance is unaffected.

7.3 Tuning Control Circuit

Frequency tuning ensures that the oscillator operates at the desired frequency of 8 GHz despite manufacturing variations. To achieve this, tuning control circuits are deployed in different stages of the oscillator circuit, as shown in Fig. 7.9. The purpose of the tuning circuits is to trim the gain and frequency of the oscillator. This could be realized by employing a MOS varactor or switching fixed value capacitors in the circuit under digital control. Switched-capacitor tuning is used for the low-noise oscillator in this work.

7.3.1 Switched Capacitor Network

A diagram of the proposed switched-capacitor tuning circuit is illustrated in Fig. 7.10. It consists of several capacitor branches in parallel. The capacitance values in each branch are a binary weighted multiple of unit capacitance C_u . An n-bit control circuit activates the switches. Each branch has a total capacitance $2^n C_u$, where n is the branch number. A switch in series with the capacitor is controlled by the voltage, V_{cn} . The equivalent impedance (Z_{TN}) seen at ports 1 and 2 of the circuit is varied by selecting the combination of the branches that are switched on. In this way a variable capacitor of tunable value, C_{TN} , is realized between port 1 and port 2. The maximum achievable C_{TN} when all the switches are activated is $(2^{n+1} - 1)C_u$,

$$C_{TN_{Full-Range}} = (2^{n+1} - 1)C_u . \quad (7.12)$$

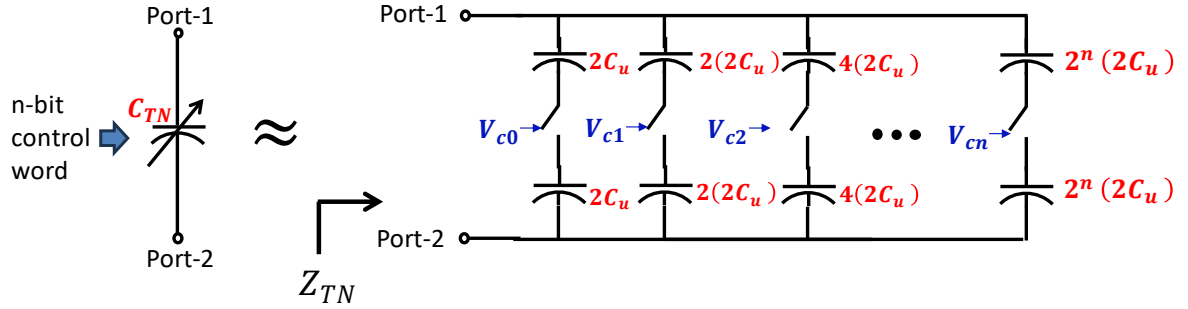


Fig. 7.10. Tuning-control circuit

The 22-nm SOI-CMOS PDK offers a range of metal-oxide-metal (MOM) capacitors. For capacitors below 1 pF, PDK capacitors are used. Custom physical layouts are designed for high-Q performance capacitors above 1 pF in value. The C_{TN} range is first determined for each tuning control circuit (ref. Fig. 7.9) from corner simulations of the circuit to control the worst-case process variation. The PDK offers substrate files for minimum and maximum resistance and capacitance variations. Post-layout simulations with these two substrate files define the minimum and maximum parameter ranges anticipated.

The switch is designed using a single NMOS transistor for simplicity. As the tuning circuits are connected to high-voltage-swing nodes of the oscillator, they must endure large AC voltage swings across them. Therefore, the 1.8-V EGSLVT NFET is used as the switch transistor. The width of the transistor is chosen to be 10 μm as a trade-off between on-resistance (R_{ON}) and parasitic capacitance (C_{ON}).

7.3.2 Tuning Range

Two major tuning control circuits are deployed in the oscillator prototype. One is placed across the bridge balancing component (L_b in Fig. 7.9) to vary the gain of the bridge, and hence the overall loop gain. The required range of $C_{TN,Lb}$ is approximately 300 fF, which is determined from simulation for a 25% change in bridge gain. A 3-bit control circuit is designed, which has unit capacitors (C_u) of 43 fF, as calculated from eq. (7.12). This is called the coarse tuning bank. A medium tuning bank that covers a range of 43 fF with unit capacitors of 6 fF, and a

fine tuning bank that covers the range of 6 fF with unit capacitance of 0.9 fF are also deployed, as shown in Fig. 7.11a across Z_{b1} .

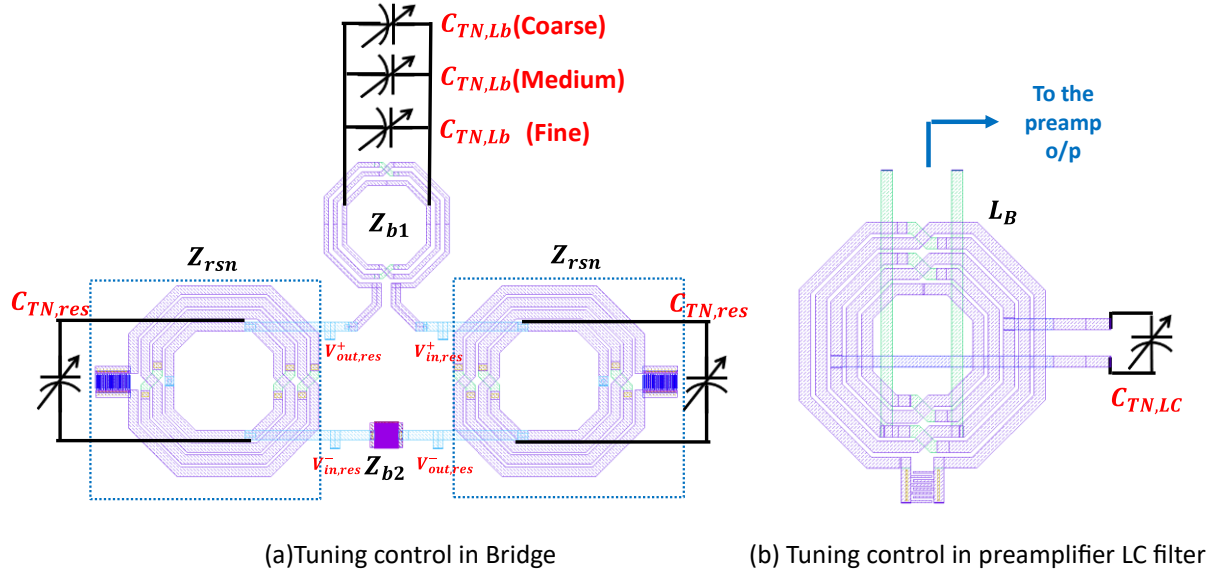


Fig. 7.11. Tuning control implementation

The tapping point, where the $C_{TN,Lb}$ tuning circuit is connected to the coil L_b , is determined to optimize routing in the physical layout and the required tuning capacitance range.

As the capacitor values are small (i.e., $< 1\text{pF}$), 10-V breakdown MOM PDK capacitors are used in the $C_{TN,Lb}(Coarse)$ and $C_{TN,Lb}(Medium)$ tuning circuits. As the unit capacitance for the fine-tuning circuit (0.9 fF) is in the atto-Farad range, layout parasitics between the capacitor metals are incorporated into the design, as shown in Fig. 7.12.

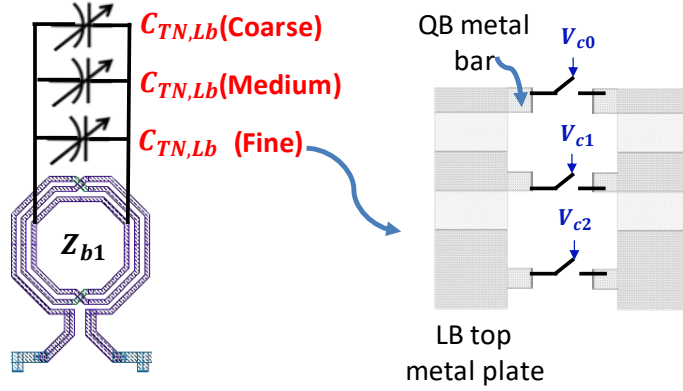


Fig. 7.12. Implementation of $C_{TN,Lb}(Fine)$ tuning circuit

Another 3-bit tuning circuit is designed to adjust the tuned load of the preamplifier that determines the peak in the loop gain (see Fig. 7.8). The required range of $C_{TN,LC}$ is determined in the same way as $C_{TN,Lb}$. A capacitance of 50 fF and a tuning range of 11% in f_{osc} is determined from corner simulations. This gives a tuning range of 7.6-8.5 GHz for the resonant frequency of the L-C filter to adjust the gain peak. With the shift in the peak gain of the preamplifier, the phase response of the oscillator also shifts. Therefore, $C_{TN,Lb}$ tuning enables f_{osc} tuning. This is used as the primary tuning control for oscillation frequency. The $C_{TN,LC}$ is placed across the L-C load as shown in Fig. 7.11b.

A third tuning control ($C_{TN,res}$) is used to control the frequency of the resonator placed at the input of Z_{rsn} , as shown in Fig. 7.11a. A range of 160 fF for $C_{TN,res}$ enables a 2% change in f_{osc} . It is used as an auxiliary tuning control for tuning f_{osc} .

7.4 Output-stage Buffer and the Full Prototype

The final RF output from the oscillator loop is taken from the preamplifier output node through a buffer, as shown in Fig. 7.13. The digital control voltages for the three tuning-control circuits are stored in a 16-bit shift register (serial in parallel out or SIPO). The register takes serial input data (from a bond pad) and converts it to a 16-bit parallel output control word, as illustrated in

Fig. 7.13. Among the 16 bits, 15 bits are gate voltages used to control the switches. The remaining bit is output for verification.

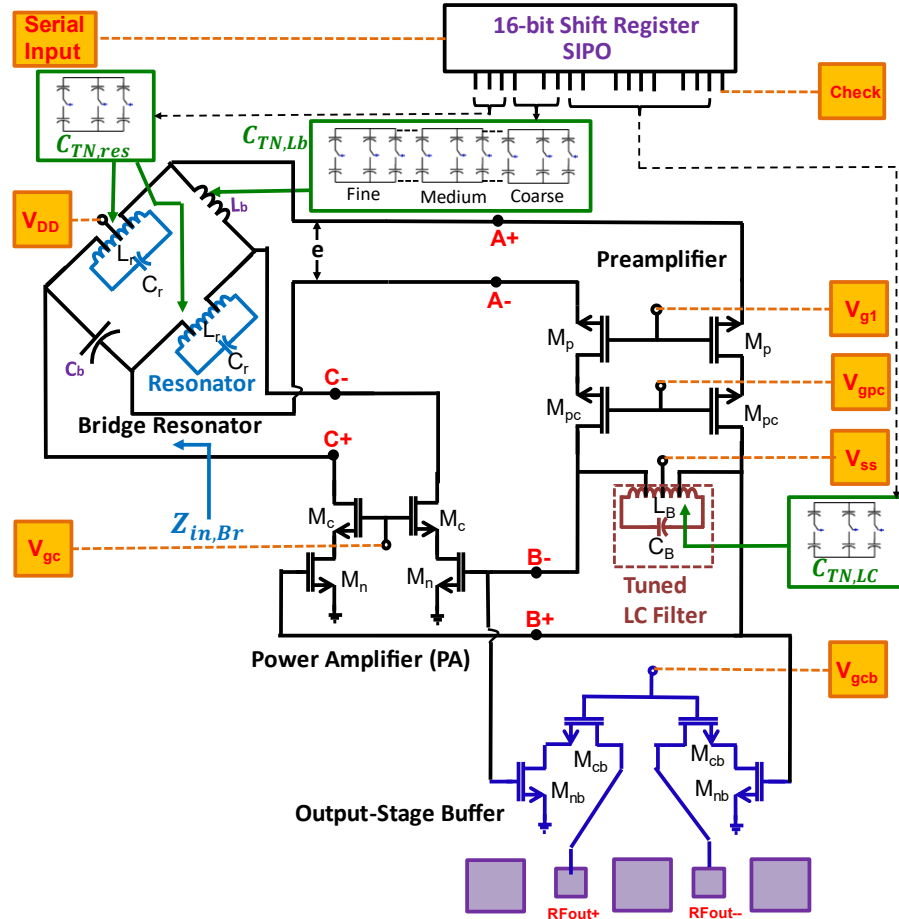


Fig. 7.13. Schematic of the complete oscillator prototype

The layout of the bridge oscillator prototype designed in the 22-nm FD-SOI CMOS technology is shown in Fig. 7.14. The total chip area is $0.48 \times 0.35 \text{ mm}^2$, and the active chip area is $0.28 \times 0.18 \text{ mm}^2$. Two P-G-P-P-G-P-P-G pad sets each having five power (P) pads and three ground (G) pads are used for applying the DC bias voltages and digital control signals for the tuning circuits.

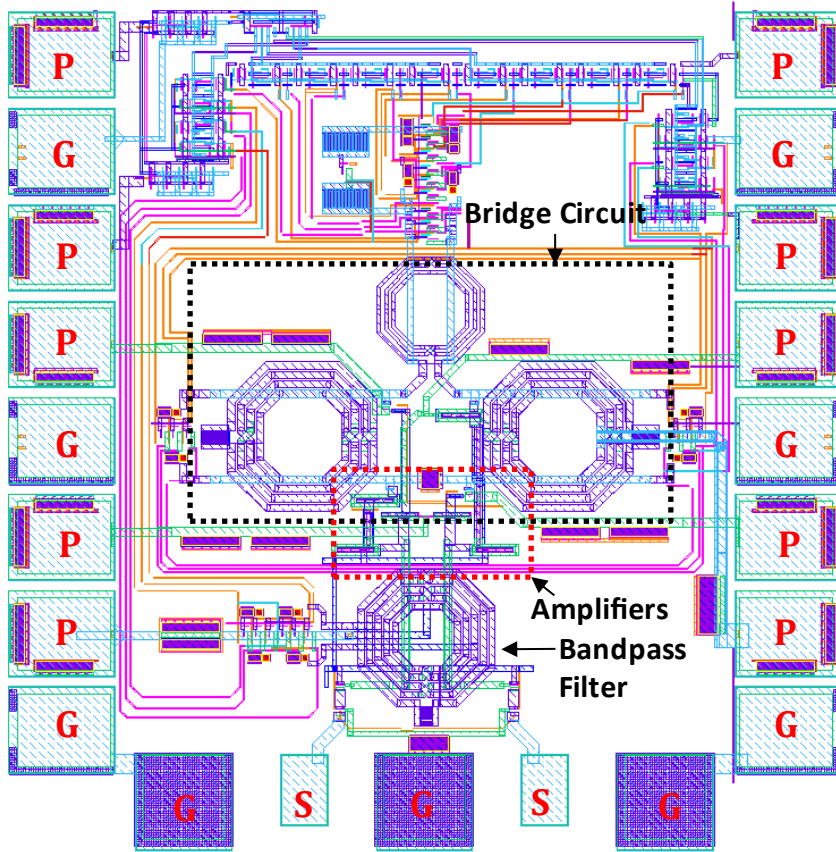


Fig. 7.14. Layout of the bridge oscillator (without metal pattern density filling)

7.5 Post-layout Simulations of the Oscillator

Final post-layout simulation results are shown in Fig. 7.15 to Fig. 7.17. The differential RF output voltage build up from a cold start (i.e., gradually turning on each transistor in the active circuits) is illustrated in Fig. 7.15. An output voltage swing of $2.49\text{-V}_{\text{peak}}$ is achieved from simulation. Fig. 7.15b illustrates the stable oscillation output across a shorter time scale. The loop gain and phase response are plotted in Fig. 7.16. As expected, the loop gain is 4 with a phase shift of 360° at 8 GHz.

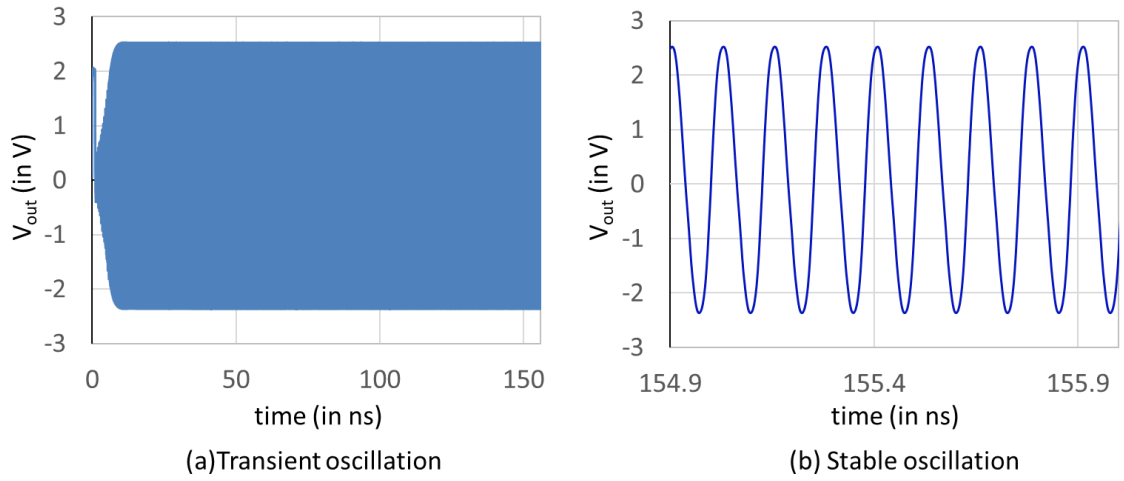


Fig. 7.15. Output voltage oscillation

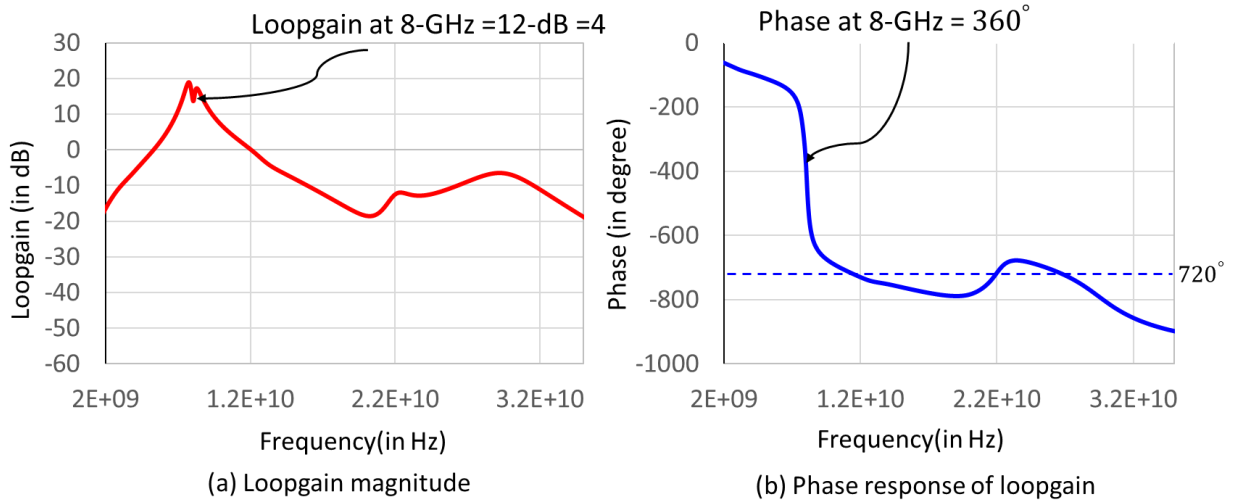


Fig. 7.16. Loop gain and phase response

Fig. 7.17 illustrates the phase-noise simulation result. A phase noise of -131.613 dBc/Hz at a frequency offset of 1 MHz is achieved for an 8-GHz carrier frequency. The corner frequency between the $1/f^2$ region and the thermal noise floor is 110 MHz, which gives an effective bridge Q-factor of 36 (from Leeson's formula, corner frequency is $\frac{f_0}{2Q_{br}}$).

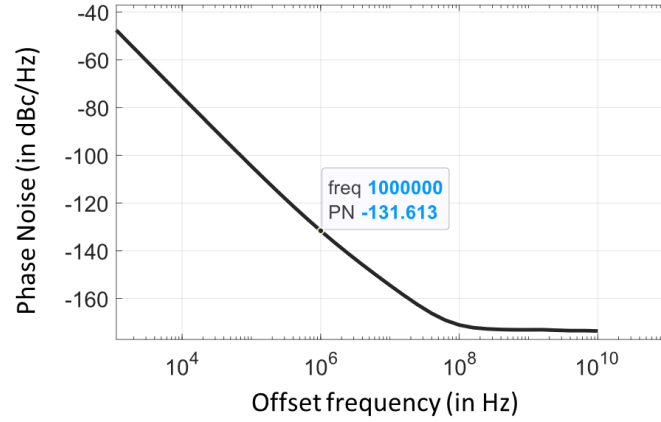


Fig. 7.17. Phase noise performance

7.6 Summary

The main objective of this work is improving upon the phase-noise performance of state-of-the-art on-chip RF oscillators by leveraging the high-Q bridge resonator circuit and passive components designed and explained in the previous chapters. The phase noise target, (-130 dBc/Hz at 1-MHz offset) is achieved in simulation with ~ 1.5 dB margin for an 8-GHz oscillation. High-Q passive and novel on-chip high-Q bridge resonator circuits demonstrated in this work are utilized to design the low-phase-noise oscillator. Robustness is improved by equipping the circuit with multiple tuning networks to adjust the loop gain and frequency. Post layout simulations predict a phase noise of -131.6 dBc/Hz at 1 MHz offset and 8-GHz carrier frequency.

Chapter 8

Conclusions and Future Work

This thesis has focused on the analysis, design, and validation of an integrated, high-Q on-chip bridge resonator and passive components. These elements are used to design a low-phase-noise RF oscillator (< -130 dBc/Hz at 1 MHz offset and 8 GHz carrier frequency) suitable for portable wireless and wireline applications. The main building blocks developed for the bridge oscillator include: 1) passive components, 2) a bridge circuit, 3) a preamplifier, 4) a tapped L-C filter, and 5) a power amplifier (PA). All circuits are fully-differential for ease of integration onto a single silicon chip. The circuit prototypes are simulated in GlobalFoundries 22-nm RF SOI-CMOS using BEOL stack option 19.

The success of this design comes from the utilization of high-Q passive components, including capacitors, and inductors, which have been optimized and implemented in a production 22-nm SOI-CMOS technology. Custom-designed inductors, with inductances of 1 nH and 2 nH, achieve Q factors exceeding 30 at 10 GHz. These inductors are realized through BEOL Stack 11 and Stack 19 configurations with varying shielding patterns, demonstrating remarkable performance. Additionally, high-Q capacitors, surpassing Q factors of 500 at 10 GHz, are demonstrated. Balanced transmission lines with Q factors exceeding 150 at 25 GHz are also successfully designed and implemented.

An on-chip bridge resonator, drawing inspiration from Meacham's seminal low-frequency discrete bridge circuit introduced in 1934, is realized by utilizing these high-Q passive components. Experimental results validate a Q-factor exceeding 50 at 8.5 GHz. Moreover, the potential of this high-Q bridge resonator in facilitating the design of a low-phase-noise RF oscillator is demonstrated, with post-layout simulations predicting a phase noise below -131 dBc/Hz at a 1 MHz offset for a 8-GHz carrier frequency.

8.1 Future Work

Several challenges and ideas for future work raised during the design, implementation, and measurement phases of this thesis.

1. Addressing the need for proper on-chip loop gain control and frequency tuning circuitry is crucial for mitigating the impact of process variation on oscillator performance. Future work could explore several avenues for further improvement and innovation. Investigating methods to optimize on-chip loop gain control to ensure robust and stable oscillation across process variations is an area for future work. This could involve exploring adaptive biasing for gain control.
2. There is scope for implementing more range with the tuning circuits given the nature of high sensitivity of the high-Q circuit to the accuracy of simulator tool, process, and environmental variations. Other tuning mechanisms that offer low parasitic effect in the layout and therefore minimally affecting the core circuit performance can be explored. Investigating innovative approaches which involve the development of self-calibration techniques or adaptive control algorithms capable of dynamically adjusting oscillator parameters to optimize performance in the presence of process variations is another potential research topic.
3. On-chip calibration mechanisms can be implemented to enable real-time monitoring and adjustment of critical parameters in response to any type of variations. This may involve the incorporation of built-in self-test (BIST) or self-correction mechanisms to ensure consistent and reliable performance under varying conditions.
4. The number of components in the bridge circuit can be reduced to reduce the complexity of the circuit. This can help with implementation and layout design and reduce parasitics.
5. Further research could focus on developing capacitors and switches capable of operating beyond 10 V breakdown without compromising performance. Custom-designed components for specific voltage requirements can be explored.
6. Techniques to lower supply voltages by optimizing the design and performance of the amplifier stages can be explored further. This could involve exploring different circuit

topologies, transistor configurations, number of stages, or biasing schemes to minimize supply voltages while minimizing phase noise.

7. The noise of the preamplifier stage is critical for the phase noise performance of the oscillator. An area of research could be optimizing the preamplifier design to reduce the noise further.
8. The transmission line resonator designed in this work could be used in a VCO. Future work can include demonstrating an oscillator with this type of transmission line resonator. The Q factor of the inductors can be raised beyond 30 by using the concepts demonstrated for transmission line resonator.
9. Area for future exploration includes a thorough examination of the common-mode and differential-mode behaviours within the bridge oscillator loop. This investigation has the potential to unveil new avenues for enhancing phase noise performance even further.
10. The phase noise formula derived in eq. (6.25) can be further investigated by sweeping the individual design parameters to assess its accuracy and effectiveness as a practical design tool.

By addressing these areas of future work, further advance in bridge oscillator circuit design and performance may be achieved and contribute to the development of more efficient, high-performance electronic systems for various RF applications.

References

- [1] A. S. Delke, M. S. O. Alink, A. J. Annema, Y. Jin, J. Verlinden and B. Nauta, *Frequency reference generator*, Google Patents, 2021.
- [2] J. A. McNeill and D. Ricketts, *The designer's guide to jitter in ring oscillators*, Springer Science & Business Media, 2009.
- [3] J. Lee and Y. S. Byun, "Analysis of clutter cancellation capability considering radar system phase noise effects," in *IEEE Antennas and Propagation Society International Symposium 1997. Digest*, 1997.
- [4] R. M. Narayanan and M. Dawood, "Doppler estimation using a coherent ultrawide-band random noise radar," *IEEE Transactions on Antennas and Propagation*, vol. 48, p. 868–878, 2000.
- [5] W. P. Robins, *Phase noise in signal sources: theory and applications*, vol. 9, IET, 1984.
- [6] R. J. Matthys, "Crystal oscillator circuits," *New York*, 1983.
- [7] L. A. Meacham, "The bridge stabilized oscillator," *Bell System Technical Journal*, vol. 17, p. 574–591, 1938.
- [8] W. R. Sooy, F. L. Vernon and J. Munushian, "A Microwave Meacham Bridge Oscillator," *Proceedings of the IRE*, vol. 48, pp. 1297-1306, 1960.
- [9] J. Williams and F. An, "Bridge Circuits Marrying Gain and Balance," 1990.
- [10] "22nm FD-SOI technology," [Online]. Available: <https://www.globalfoundries.com/sites/default/>.
- [11] "Cisco Visual Networking Index: Forecast and Trends, 2017–2022 White Paper," 2019.
- [12] T. S. Rappaport, S. Sun, R. Mayzus, H. Zhao, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. Samimi and F. Gutierrez, "Millimeter Wave Mobile Communications for 5G Cellular: It Will Work!," *IEEE Access*, vol. 1, p. 335–349, 2013.

- [13] X. Li, A. Gani, R. Salleh and O. Zakaria, "The future of mobile wireless communication networks," in *2009 International Conference on Communication Software and Networks*, 2009.
- [14] L. Cheng, M. Zhu, M. M. U. Gul, X. Ma and G.-K. Chang, "Adaptive photonics-aided coordinated multipoint transmissions for next-generation mobile fronthaul," *Journal of Lightwave Technology*, vol. 32, pp. 1907-1914, 2014.
- [15] J. R. Vig and T. R. Meeker, "The aging of bulk acoustic wave resonators, filters and oscillators," in *Proceedings of the 45th Annual Symposium on Frequency Control 1991*, 1991.
- [16] E. Rubiola, *Phase noise and frequency stability in oscillators*, Cambridge University Press, 2008.
- [17] S. Voinigescu, *High-frequency integrated circuits*, Cambridge University Press, 2013.
- [18] D. B. Lesson, "A simple model of feedback oscillator noise spectrum," *proc. IEEE*, vol. 54, p. 329–330, 1966.
- [19] P. Andreani and A. Fard, "More on the More on the $1/f^2$ Phase Noise Performance of CMOS Differential-Pair LC-Tank Oscillators Phase Noise Performance of CMOS Differential-Pair LC-Tank Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 41, p. 2703–2712, 2006.
- [20] B. Razavi, *RF Microelectronics*, 2nd ed., Prentice Hall, 2012.
- [21] E. V. Kulagin, V. P. Sokolov, A. I. Pikhitelev and B. P. Fateev, "Technical fluctuations in a quartz crystal oscillator with automatic gain control," *Radiophysics and Quantum Electronics*, vol. 21, p. 1234–1238, 1978.
- [22] T. Urgan, X. Le Polozec, W. Walker and L. Reindl, "RF energy harvesting design using high Q resonators," in *2009 IEEE MTT-S International Microwave Workshop on Wireless Sensing, Local Positioning, and RFID*, 2009.
- [23] B. Razavi, *Design of analog CMOS integrated circuits*, 2005.

- [24] U. L. Rohde, A. K. Poddar and G. Böck, The design of modern microwave oscillators for wireless applications: theory and optimization, John Wiley & Sons, 2005.
- [25] C. Weyers, P. Mayr, J. W. Kunze and U. Langmann, "A 22.3dB Voltage Gain 6.1dB NF 60GHz LNA in 65nm CMOS with Differential Output," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2008.
- [26] M. Fahimnia, M. Mohammad-Taheri, B. Biglarbeigian and S. Safavi-Naeini, "Characterization of a high-Q on-chip transmission line for CMOS MMIC applications," in *2011 19th Iranian Conference on Electrical Engineering*, 2011.
- [27] J. J. Lee and C. S. Park, "A slow-wave microstrip line with a high-Q and a high dielectric constant for millimeter-wave CMOS application," *IEEE Microwave and Wireless Components Letters*, vol. 20, p. 381–383, 2010.
- [28] H. Veenstra and M. G. M. Notten, "60GHz VCOs with transmission line resonator in a 0.25 μ m SiGe BiCMOS technology," in *2008 IEEE Radio Frequency Integrated Circuits Symposium*, 2008.
- [29] B. Krauter and S. Mehrotra, "Layout Based Frequency Dependent Inductance and Resistance Extraction for On-Chip Interconnect Timing Analysis," in *Proceedings of the 35th Annual Design Automation Conference*, New York, NY, USA, 1998.
- [30] S. Kim and D. P. Neikirk, "Compact equivalent circuit model for the skin effect," in *1996 IEEE MTT-S International Microwave Symposium Digest*, 1996.
- [31] S.-P. Sim, C. Chao, S. Krishnan, D. M. Petranovic, N. D. Arora, K. Lee and C. Y. Yang, "An effective loop inductance model for general non-orthogonal interconnect with random capacitive coupling," in *Digest. International Electron Devices Meeting*, 2002.
- [32] C.-S. Yen, Z. Fazarinc and R. L. Wheeler, "Time-domain skin-effect model for transient analysis of lossy transmission lines," *Proceedings of the IEEE*, vol. 70, pp. 750-757, 7 1982.

- [33] J. Zheng, Y.-C. Hahm, V. K. Tripathi and A. Weisshaar, "CAD-oriented equivalent-circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp. 1443-1451, 9 2000.
- [34] K. Yang, W. Yin and J. Mao, "Wideband Lumped Element Model for On-Chip (A)symmetrical Coupled Interconnects on Lossy Silicon Substrate," in *2007 Asia-Pacific Microwave Conference*, 2007.
- [35] K. Kang, L. Nan, S. C. Rustagi, K. Mouthaan, J. Shi, R. Kumar, W. Yin and L. Li, "A Wideband Scalable and SPICE-Compatible Model for On-Chip Interconnects Up to 110 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, pp. 942-951, 4 2008.
- [36] I. M. Kang, S.-J. Jung, T.-H. Choi, J.-H. Jung, C. Chung, H.-S. Kim, K. Park, H. Oh, H.-W. Lee, G. Jo, Y.-K. Kim, H.-G. Kim and K.-M. Choi, "RF Model of BEOL Vertical Natural Capacitor (VNCAP) Fabricated by 45-nm RF CMOS Technology and Its Verification," vol. 30, pp. 538-540, 2009.
- [37] J. Shi, A. Sidelnicov, K. W. J. Chew, M. S. Chin, C. Schippel, J. M. M. dos Santos, F. Schlaphof, L. Meinshausen, J. R. Long and D. L. Hareme, *Evolution and Optimization of BEOL MOM Capacitors Across Advanced CMOS Nodes*, 2018.
- [38] "22nm FD-SOI technology.," [Online]. Available: <https://www.globalfoundries.com/sites/default/>.
- [39] I. Chlis, D. Pepe and D. Zito, *A novel differential Hartley CMOS oscillator circuit topology*, 2016.
- [40] A. Fard and P. Andreani, "An Analysis of $1/f^2$ Phase Noise in Bipolar Colpitts Oscillators (With a Digression on Bipolar Differential-Pair LC Oscillators)," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 374-384, 2007.
- [41] I. Chlis, D. Pepe and D. Zito, "Phase noise analysis in CMOS differential Armstrong oscillator topology," *Int. J. Circuit Theory Appl.*, vol. 44, p. 1697–1705, 2016.

- [42] J. K. Clapp, "An Inductance-Capacitance Oscillator of Unusual Frequency Stability," vol. 36, pp. 356-358, 1948.
- [43] P. Andreani, X. Wang, L. Vandi and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1107-1118, 2005.
- [44] P. J. Fish, *Electronic noise and low noise design*, Springer, 1993.
- [45] R. Lacoste, 12 11 2013. [Online]. Available: <https://circuitcellar.com/research-design-hub/amplifier-classes-from-a-to-h/>.
- [46] A. Pini, 31 10 2018.[Online]. Available: <https://www.digikey.com/en/articles/simplify-portable-low-power-audio-circuit-design-class-d-amplifiers>.
- [47] S. Cripps, *RF Power Amplifiers for Wireless Communications*, 2006.
- [48] E. Hegazi, H. Sjoland and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1921-1930, 2001.
- [49] F. Hong, H. Zhang and D. Zhao, "An X -Band CMOS VCO Using Ultra-Wideband Dual Common-Mode Resonance Technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1-12, 2022.
- [50] Y.-K. Cho, J.-W. Nam and S.-W. Lee, "A Low-Power Class-C Voltage-Controlled Oscillator With Robust Start-Up and Compact High-Q Capacitor Array," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, pp. 819-823, 2022.
- [51] E. Ebrahimi and S. Naseh, "A CMOS low-noise low-power quadrature LC oscillator," in *2009 IEEE International Symposium on Circuits and Systems*, 2009.
- [52] M. Garampazzi, P. M. Mendes, N. Codega, D. Manstretta and R. Castello, "Analysis and Design of a 195.6 dBc/Hz Peak FoM P-N Class-B Oscillator With Transformer-Based Tail Filtering," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 1657-1668, 2015.

- [53] D. Murphy, H. Darabi and H. Wu, "Implicit common-mode resonance in LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 52, p. 812–821, 2017.
- [54] O. Esmaeeli, S. Lightbody, A. H. M. Shirazi, H. Djahanshahi, R. Zavari, S. Mirabbasi and S. Shekhar, "A Transformer-Based Technique to Improve Tuning Range and Phase Noise of a 20-28-GHz LC-VCO and a 51-62-GHz Self-Mixing LC-VCO," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022.
- [55] F. Hong, T. Ding and D. Zhao, "A 196.5 dBc/Hz FOMT 16.8–21.6-GHz Class-F23 CMOS VCO With Transformer-Based Optimal Q-Factor Tank," vol. 5, pp. 62-65, 2022.
- [56] H. S. Lee, D. M. Kang, S. J. Cho, C. W. Byeon and C. S. Park, "Low-Power, Low-Phase-Noise Gm-Boosted 10-GHz VCO With Center-Tap Transformer and Stacked Transistor," vol. 67, pp. 1710-1714, 2020.
- [57] O. El-Aassar and G. M. Rebeiz, "A stacked-complementary 5 GHz oscillator with even-only differential harmonic shaping achieving- 150 dBc/Hz phase noise at 10-MHz offset using body-biased thin-oxide 22-nm FDSOI," *IEEE Solid-State Circuits Letters*, vol. 3, p. 98–101, 2020.
- [58] A. Visweswaran, R. B. Staszewski and J. R. Long, "A low phase noise oscillator principled on transformer-coupled hard limiting," *IEEE Journal of Solid-State Circuits*, vol. 49, p. 373–383, 2014.
- [59] M. Babaie and R. B. Staszewski, "A Class-F CMOS Oscillator," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 3120-3133, 2013.
- [60] A. El-Gouhary and N. M. Neihart, "An analysis of phase noise in transformer-based dual-tank oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, p. 2098–2109, 2014.
- [61] M. Babaie and R. B. Staszewski, "An ultra-low phase noise class-F 2 CMOS oscillator with 191 dBc/Hz FoM and long-term reliability," *IEEE Journal of Solid-State Circuits*, vol. 50, p. 679–692, 2015.

- [62] H. Jian, Z. Tang, J. He and H. Min, "Analysis of self-resonant frequency for differential-driven symmetric and single-ended inductors," in *Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, 2004.*, 2004.
- [63] O. El-Aassar and G. M. Rebeiz, "Octave-tuning dual-core folded VCO leveraging a triple-mode switch-less tertiary magnetic loop," *IEEE Journal of Solid-State Circuits*, vol. 56, p. 1475–1486, 2021.
- [64] J. M. Miller, *Piezo-electric oscillation generator*, Google Patents, 1930.
- [65] G. W. Pierce, *Electrical system*, Google Patents, 1938.
- [66] S. Sabaroff, "A voltage stabilized high-frequency crystal oscillator circuit," *Proceedings of the Institute of Radio Engineers*, vol. 25, p. 623–629, 1937.
- [67] P.-C. Huang, M.-D. Tsai, G. D. Vendelin, H. Wang, C.-H. Chen and C.-S. Chang, "A Low-Power 114-GHz Push–Push CMOS VCO Using LC Source Degeneration," vol. 42, pp. 1230-1239, 2007.
- [68] P. Salzenstein, "Frequency and temperature control for complex system engineering in optoelectronics and electronics: an overview," *International Journal for Simulation and Multidisciplinary Design Optimization*, vol. 11, p. 7, 2020.
- [69] W. A. Edson, W. Clary, J. C. Hogg JR and F. Monlouth, *High Frequency Crystal-Controlled Oscillator Circuits*, Georgia Institute of Technology, State Engineering Experiment Station, 1948.
- [70] W. A. Edson, "Vacuum-tube oscillators," (*No Title*), 1953.
- [71] D. Firth, *Quartz crystal oscillator circuits design handbook*, US Army Electronics Laboratories, US Army Electronics Command, 1965.
- [72] V. Papez and S. Papezova, "Bridge symmetric crystal oscillator," in *2011 10th International Conference on Telecommunication in Modern Satellite Cable and Broadcasting Services (TELSIKS)*, 2011.

- [73] K. K. O, "Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1249-1252, 1998.
- [74] S. Amakawa, N. Ishihara and K. Masu, "A thru-only de-embedding method for on-wafer characterization of," *parameters*, vol. 28, p. 57–62.
- [75] "Specifying Calibration Standards and Kits for Keysight Vector Network Analyzers," [Online]. Available: <https://www.keysight.com/us/en/assets/7018-01375/application-notes/5989-4840.pdf>.
- [76] J. R. Long, "Passive Components for RFIC Design," *IEEE RFIC Virtual Journal*, no. 3, 2013.
- [77] J. R. Long, "Passive Components for RFIC Design," *IEEE RFIC Virtual Journal*, no. 18, 2020.
- [78] C. Weyers, P. Mayr, J. W. Kunze and U. Langmann, "A 22.3 dB voltage gain 6.1 dB NF 60GHz LNA in 65nm CMOS with differential output," in *2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*, 2008.
- [79] A. M. Mangan, Millimetre-wave device characterization for nano-CMOS IC design, University of Toronto Master's Thesis, 2005.
- [80] D. M. Pozar, *Microwave engineering*, John wiley & sons, 2011.
- [81] T. S. D. Cheung and J. R. Long, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," *IEEE Journal of Solid-state circuits*, vol. 41, pp. 1183-1200, 2006.
- [82] H. Hasegawa, M. Furukawa and H. Yanai, "Properties of Microstrip Line on Si-SiO₂ System," *IEEE Transactions on Microwave Theory and Techniques*, vol. 19, pp. 869-881, 11 1971.
- [83] H. A. Wheeler, "Formulas for the Skin Effect," *Proceedings of the IRE*, vol. 30, pp. 412-424, 9 1942.

- [84] J. R. Long and M. Danesh, "A uniform compact model for planar RF/MMIC interconnect, inductors and transformers," in *Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting (Cat. No. 01CH37212)*, 2001.
- [85] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, pp. 483-490, 8 1992.

APPENDICES

Appendix A

Phase Noise Fundamentals

Phase noise is the short-term instability of the oscillator output caused by phase modulation. An oscillator produces a sinusoidal output of the form

$$V_o(t) = A_{osc} \cos(\omega_{osc}t + \varphi_{osc}), \quad (\text{A.1})$$

where A_{osc} and ω_{osc} are the oscillation amplitude and its angular frequency, respectively. Ideally, they are constant over time. In this situation, the zero crossings of $V_o(t)$ occur at exact integer multiples of the period (i.e., $T = 1/f_{osc}$). Due to unavoidable physical noise sources, these quantities are modulated in a real circuit, and are thus time-varying. Modulations can be classified generally as amplitude and frequency/phase modulation [5].

In case of amplitude modulation (AM), the oscillator output voltage becomes

$$V_{oAM}(t) = A_{osc}[1 + a \cos(\omega_a t)] \cdot \cos(\omega_{osc}t), \quad (\text{A.2})$$

where, the first term (i.e., $A_{osc}[1 + a \cos(\omega_a t)]$) represents the random amplitude variation as a function of time. Typically, a is significantly smaller than unity, and ω_a is smaller than ω_{osc} . In the frequency domain, eq. (A.2) transforms to a Dirac delta function at ω_{osc} , along with sidetones at frequencies $(\omega_{osc} \pm \omega_a)$. The resulting output voltage can be expressed as [5]

$$V_{oAM}(t) = A_{osc} \sin(\omega_{osc}t) + \frac{aA_{osc}}{2} [\cos((\omega_{osc} - \omega_a)t) - \cos((\omega_{osc} + \omega_a)t)], \quad (\text{A.3})$$

where, the $(\omega_{osc} - \omega_a)$ frequency component represents the lower sideband, and $(\omega_{osc} + \omega_a)$ represents the upper sideband.

Frequency modulation is explained in terms of phase modulation (PM), as phase is the integral of frequency. The time-dependent phase term, $\varphi_{PM}(t)$ models phase modulation of the output voltage

$$V_{oPM}(t) = A_{osc} \cos(\omega_{osc}t + \varphi_{PM}(t)), \quad (A.4)$$

$$\varphi_{PM}(t) = \varphi_p \sin(\omega_p t). \quad (A.5)$$

The phase modulation index (φ_p) can be represented as the ratio of frequency variation ($\Delta\omega_{osc}$) divided by the phase modulation rate (ω_p). If φ_p is much lower than one radian, which is the case of small-angle modulation (i.e., narrow-band frequency modulation), the output signal $V_{oPM}(t)$ can be approximated as

$$\begin{aligned} V_{oPM}(t) &\cong A_{osc} \cos(\omega_{osc}t) \\ &+ \frac{A_{osc}\varphi_p}{2} \left[\cos((\omega_{osc} - \omega_p)t) - \cos((\omega_{osc} + \omega_p)t) \right]. \end{aligned} \quad (A.6)$$

Similar to the AM case, PM also generates two sidebands in the frequency domain, as can be seen from eq. (A.6). It shows that the oscillator signal is comprised of three frequency components: one at ω_{osc} , representing the power of the oscillator fundamental signal (or carrier power), and two sidebands of equal amplitude $\frac{A_{osc}\varphi_p}{2}$, at $(\omega_{osc} + \omega_p)$ and at $(\omega_{osc} - \omega_p)$. From eq. (A.6), the single-sideband phase noise, $L(\omega_p)$, can be defined as the ratio between the root-mean-square (RMS) power of either sideband and the RMS power of the carrier as [5]

$$L(\omega_p) = \frac{\frac{1}{2} \left(\frac{A_{osc}\varphi_p}{2} \right)^2}{\frac{1}{2} (A_{osc})^2} = \left(\frac{\varphi_p}{2} \right)^2. \quad (A.7)$$

The factor of $\frac{1}{2}$ in both numerator and denominator of eq. (A.7) is due to the RMS form of power. Limiting of the signal by the active devices introduces a coherence between the upper and the lower sideband known as ‘conformability’ [5]. Two signals are conformable when their mean frequency ($\omega/2\pi$) is large compared with their maximum frequency difference, their amplitudes are equal at the same frequency offset with respect to the mean frequency, and their phases are equal and opposite. Also, noise from higher harmonics is mixed up (or down) to the oscillation frequency by the non-linear behaviour of the active devices in the oscillator. For simplicity, these two phenomena are not considered in this section.

AM and PM are illustrated using the phasor diagram of Fig. A.1 for better understanding. The oscillation signal can be thought of as a carrier (phasor A_{osc}) with a small perturbation due to PM/AM rotating at its tip.

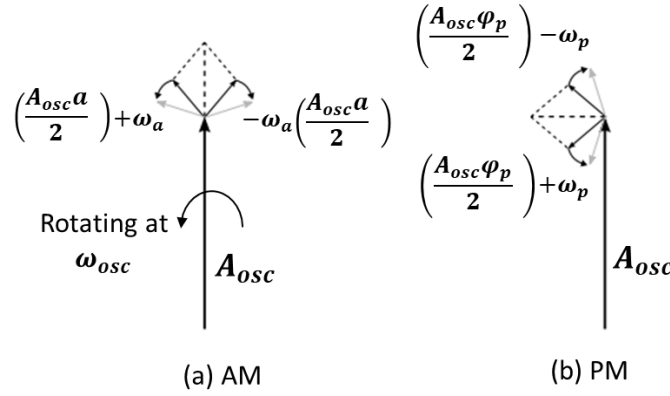


Fig. A.1. Phasor diagram for amplitude and phase modulation [5]

There are two phasors rotating in opposite directions, one for the upper and one for the lower sideband. The sum of these two sideband phasors model AM and PM of the carrier A_{osc} . The component along the axis of the carrier vector being AM noise and the component orthogonal to the carrier vector being phase noise. As seen from eq. (A.6), $\cos\left((\omega_{osc} + \omega_p)t\right)$ is approximated by $\cos(\omega_{osc}t)$, when ω_p is much lower than ω_{osc} . Therefore, PM can be thought of as a linear modulation as long as the phase deviation (i.e., $\omega_p t$) is considerably less than 0.1 rad. With limiting of the oscillator amplitude at large signal, the amplitude variation becomes negligible, as it gets fixed to a certain value. The AM component can therefore be removed, and PM dominates. Therefore, phase noise is typically the most important parameter characterizing the performance of oscillators.

Appendix B

System-Level Simulation

The ADS schematic circuit for oscillator system-level simulation is shown in Fig. B. 1. The resonators in the bridge circuit are formed with EM simulation data for a $100\ \Omega$ resonator. The rest of the components (i.e., tuning capacitor, L_b , and C_b) in the bridge circuit are modelled with lumped elements with ohmic losses modelled by resistors. The values are chosen to achieve a gain of 0.1 V/V from the bridge.

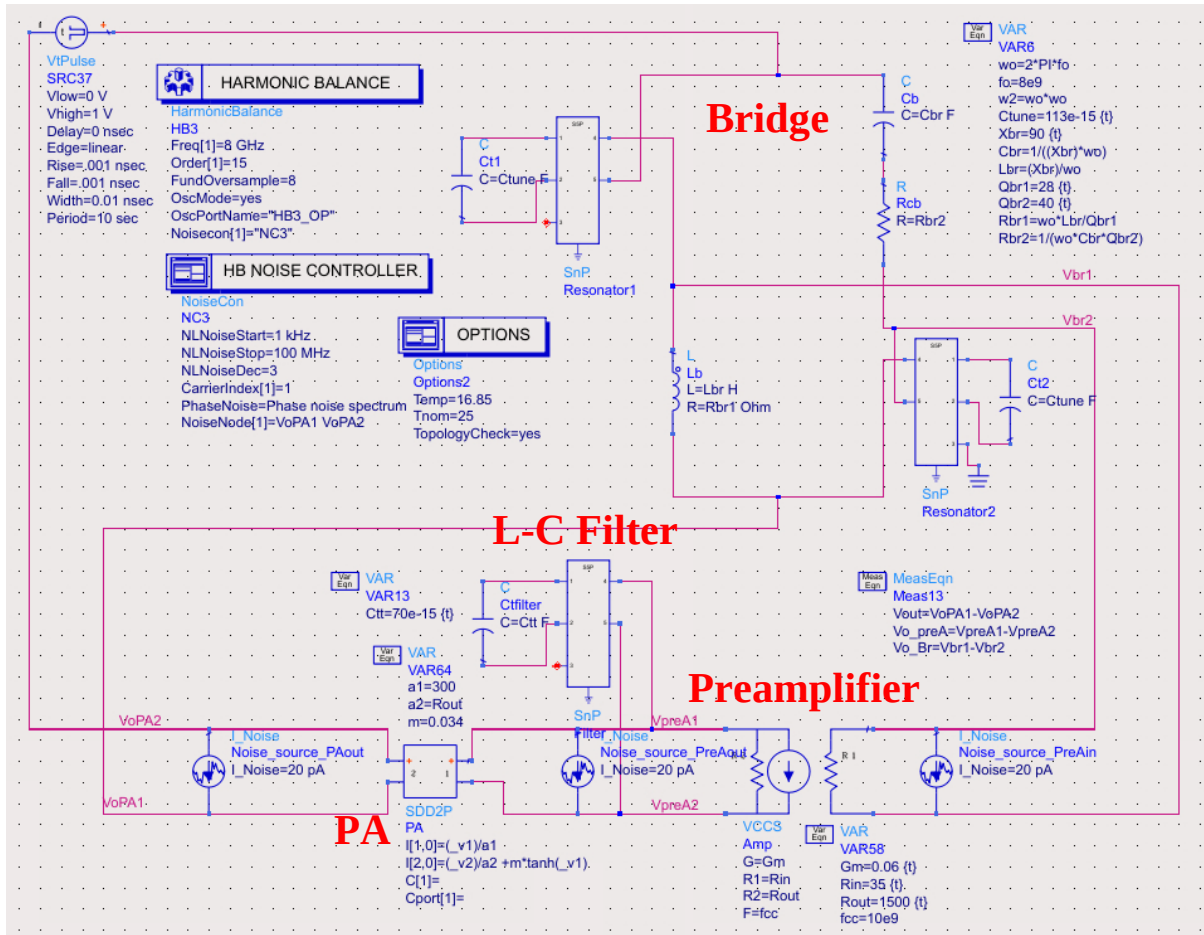


Fig. B. 1. ADS Schematic diagram for the oscillator

The L-C filter is similarly formed with EM simulation data block with a lumped-element tuning capacitor (C_{tt}).

The preamplifier is modelled with its small-signal model. The PA limiter block is modelled with a behavioural simulation block from ADS. It limits the output voltage of the oscillator providing the loop-gain. A limiter circuit was developed using the functional block from ADS which limits the output to 3 V. The block implements voltage limiting by using a hyperbolic tangent function. Usually, a MOS differential pair limits its output current following a hyperbolic relationship with the input voltage. The active circuits including the preamplifier and PA gives a total voltage gain of 42 V/V (preamplifier ~ 10 V/V and PA ~ 4 V/V) which is similar to the requirements set in the design section of Chapter 6.

The amplifiers are modelled to be noise-free. Therefore, the noise generated by the real amplifiers are modelled with three noise current sources ‘Noise_source_PreAin’, Noise_source_PreAout’, and ‘Noise-source_PAout’ (following the model described in Fig. 6.11 on page 101). The noise current value is set to 20 pA which is in the range of expected noise at the input of PMOS preamplifier designed in 22-nm SOI CMOS technology. To compare the weight of contributions for each noise current source to the total noise, all three noise current values are taken to be 20 pA.

The simulation results of the oscillator system-level circuit are shown in Fig. B. 2. The phase noise is -136.7 dBc/Hz. The output voltage has a peak swing of 3.6 V.

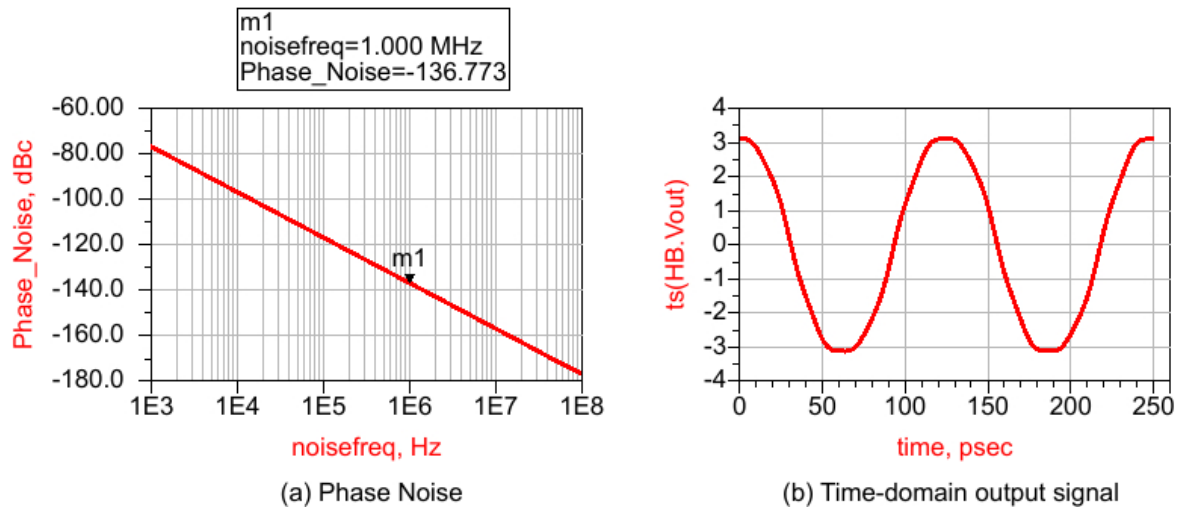


Fig. B. 2. System-level simulation results

Fig. B. 3 illustrates the contribution list of all the components to the total noise of the oscillator.

index	name	var("type")	vnc	NC3.noisefreq
0	total	total	-136.8 dBc	1.000 MHz
1	Noise_source_PreAin	I_Source	-140.4 dBc	
2	Noise_source_PreAout	I_Source	-141.7 dBc	
3	Resonator1	subckt	-146.0 dBc	
4	Resonator2	subckt	-147.9 dBc	
5	Noise_source_PAout	I_Source	-152.7 dBc	
6	Filter	subckt	-155.8 dBc	
7	Lb	L	-162.9 dBc	

Fig. B. 3. Contributions of the circuit blocks to the total oscillator phase noise

Fig. B. 3 shows that the noise at the preamplifier input has higher contribution than the noise at the PA output.