A Novel Computational Framework for Negative Capacitance Devices: From Ferroelectric-based Capacitors to Negative Capacitance Field-Effect Transistors

by

Hyunjae Lee

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Examining Committee Membership

The following served on the Examining Committee for this thesis. The decision of the Examining Committee is by majority vote.

External Examiner:	Dr. Mathieu Luisier Professor, Dept. of Information Technology and Electrical Engineering ETH Zurich
Supervisor:	Dr. Youngki Yoon Associate Professor, Dept. of Electrical and Computer Engineering University of Waterloo
Internal Member:	Dr. William Wong Professor, Dept. of Electrical and Computer Engineering University of Waterloo
Internal Member:	Dr. Guo-Xing Miao Associate Professor, Dept. of Electrical and Computer Engineering University of Waterloo
Internal-External Member:	Dr. Adam Wei Tsen Assistant Professor, Dept. of Chemistry University of Waterloo

Author's Declaration

This thesis consists of material all of which I authored or co-authored: see Statement of Contributions included in the thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Statement of Contributions

The following publications and preprints, of which I am the primary author, have been adapted into material for Chapters 3, 4, 5 and 6 respectively of this thesis:

- H. Lee, and Y. Yoon, "Modeling of Hysteretic Jump Points in Ferroelectric MOS Capacitors," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 3093-3098, 2019, doi: 10.1109/ted.2019.2915084 [100].

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- H. Lee, M. Sritharan, and Y. Yoon, "A Computational Framework for Gradually Switching Ferroelectric-Based Negative Capacitance Field-Effect Transistors," *IEEE Trans. Electron Devices*, 2022, doi: 10.1109/TED.2022.3197387 (accepted) [120].

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Abstract

Negative capacitance (NC) devices generally manifest hysteresis originating from the ferroelectric materials (FE) with nonlinear hysteretic responses of spontaneous polarization (P) to the applied electric field, while hysteresis should be suppressed for logic devices. The significant nonlinearity of P behavior in the FE entangles the manipulation and prediction of not only performance but also hysteresis in the NC-based devices when multiple materials are considered simultaneously within the device.

Here, hysteretic jump points (HJPs) are modelled by exploring the energy landscape based on the Gibbs free energy with the Landau approach in a metal-FE-oxide-semiconductor capacitor. With the aid of HJPs, the hysteresis response to the key design parameters in the NC device can be described for various ferroelectric materials, which can contribute to the hysteresis engineering.

While the Landau approach can provide insights into the polarization behavior of FE with a so-called "S-curve" of polarization versus electric field across the FE ($P - E_{\mathrm{FE}}$) characteristics, the Miller model (MM) is more suitable for a gradual transition of polarization switching for the stand-alone FE in steady states, since it can precisely capture the overall hysteresis loop including the polarization switching transition region. Firstly, the static NC characteristics in a ferroelectric-dielectric (FE-DE) capacitor are presented with significant internal voltage amplification using MM. Notably, the effect of different transitions of polarization switching that the S-curve from Landau approach cannot handle is explored.

After that, the FE-DE capacitor can be further extended to more advanced device such as a NC field-effect transistors (NCFETs), established on the understanding of NC characteristics with MM. Especially, NCFETs composed of FE exhibiting gradual switching transitions are demonstrated in steady-states using a novel computational framework. By iteratively solving three modules: (i) non-equilibrium Green's function (NEGF) for carrier transport, (ii) Poisson's equation for electrostatics, and (iii) the Miller model for the polarization behavior in FE, steep switching with hysteresis-free characteristics of NCFET can be achieved. Besides, various materials and device parameters are engineered to understand their effects on the device performance, which enables performance optimization as required for different target applications.

Although the demonstrated NCFET model provides in-depth understanding of NC in the device, an upgraded model including a more realistic behavior of FE that the $P - E_{\mathrm{FE}}$ could be varied by the

maximum electric field applied due to a property called a partially polarized FE (PPFE) can present more precise prediction of the NCFET. For the PPFE, the MM-based FE minor loop model has been used to describe its switching behavior. By elucidating the difference between the NCFET considering PPFE and ideal behavior of FE, the overestimated subthreshold swing for a NCFET under the ideal FE behavior is observed as compared to the PPFE. Furthermore, with the understanding of PPFE, a drain-induced barrier lowering (DIBL) in the PPFE-NCFET is investigated in comparison to the FPFE-NCFET.

This dissertation can provide not only a novel computational framework for NCFET simulation from FE-based capacitor to transistor but also irreplaceable physical insight into the NCFET behavior.

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Chapter 1
Introduction

1.1 Scaling and Power Challenges in Complementary Metal-Oxide-Semiconductor (CMOS)

Moore's law predicted that the transistors' count in a dense semiconductor integrated circuit (IC) would double approximately every two years by G. Moore in 1965 [1]. Following the Moore's law in the past few decades, CMOS logic technologies have been successfully developed by scaling down the feature size (see **Fig. 1.1**). However, the miniaturization of transistors becomes increasingly challenging and hampered by short channel effects in submicron CMOS technology. As shown in **Fig. 1.2**, semiconductor industries provide solutions of (a) strain engineering (for 90 nm logic technology node [2]), (b) high-k / metal gate transistor (for 45 nm logic technology node [3]), and (c) FinFET (for 22 nm logic technology node [4]). Moreover, extreme ultraviolet lithography (EUV) has been introduced for the 7 nm logic technology node [5] and gate-all-around (GAA) FETs (e.g., nanosheet and nanowire FETs) have been proposed for the beyond 7 nm technology node (see **Fig. 1.3** [6]).

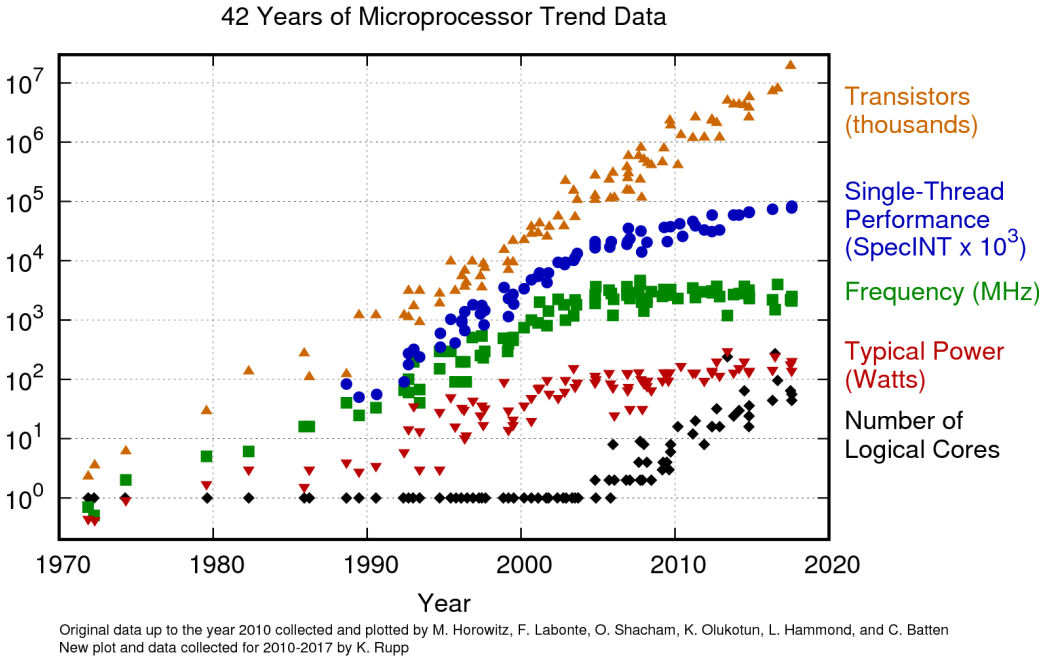
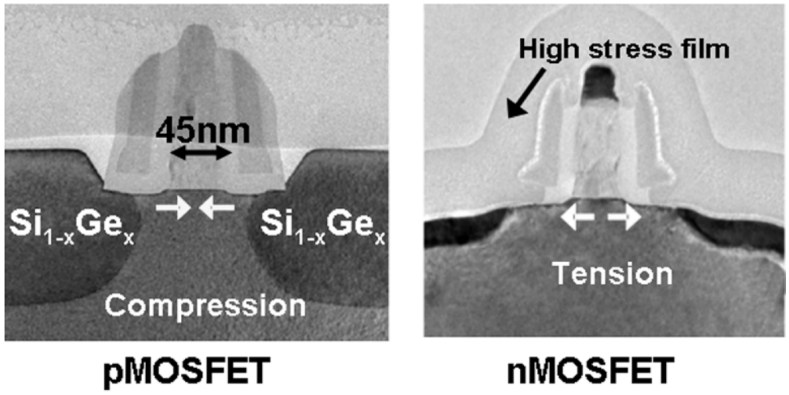
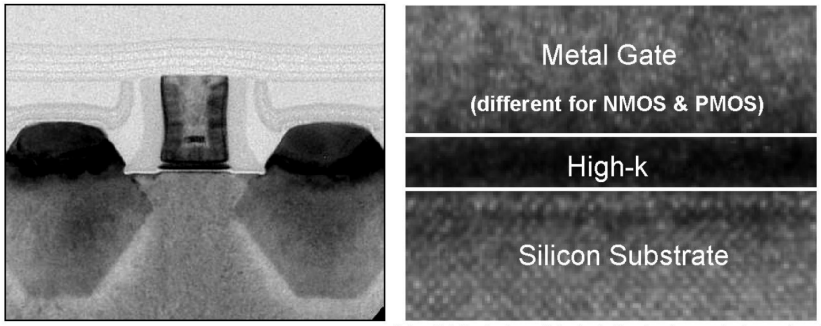


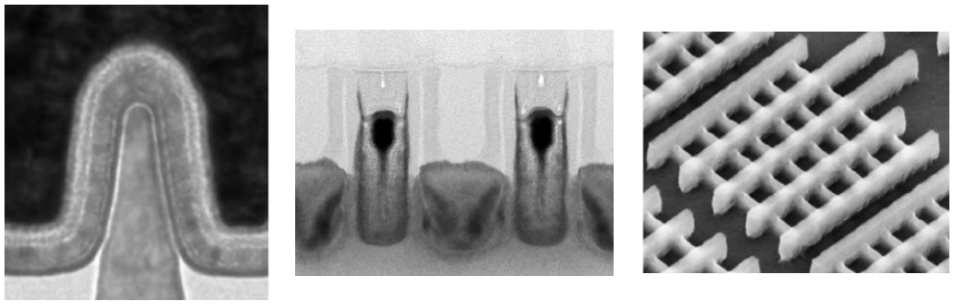
Fig. 1.1. Microprocessor trend data collected and plotted by [7].



(a)

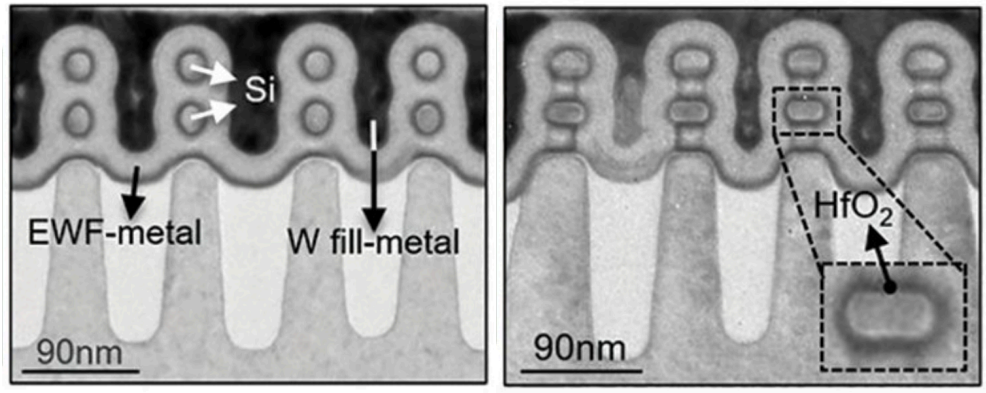


(b)



(c)

Fig. 1.2. Transmission electron microscopy (TEM) micrograph of (a) p-type and n-type MOSFET featuring strained-silicon [2], (b) high-k metal gate p-type MOSFET and the gate stack [3], and (c) fin-cut (left) and gate-cut (center) of FinFET and tilted scanning electron microscope (SEM) image of logic gate (right) [4].

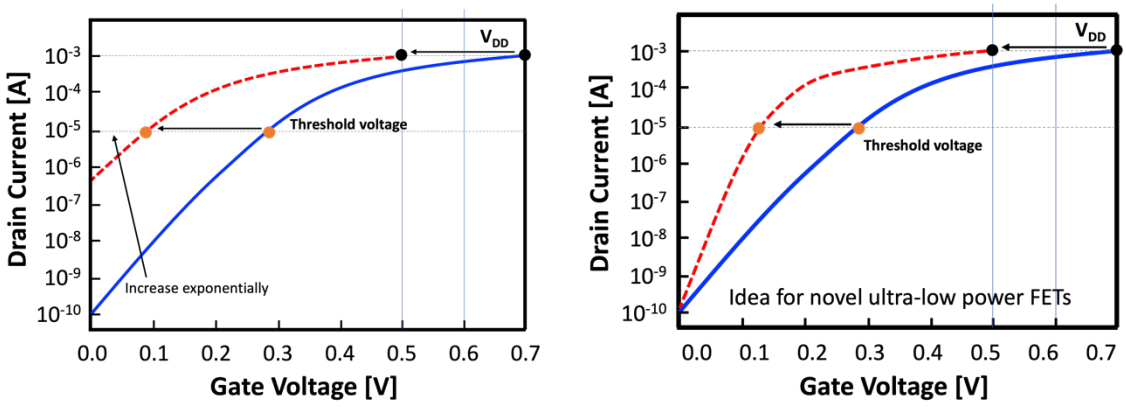


(a) (b)

Fig. 1.3. TEM images for cross-sectional views of vertically stacked (a) gate-all-around and (b) nanosheet FETs [8].

Although the density of transistors has continued to increase, as shown in **Fig. 1.1**, the clock frequency has been settled around from 3 to 4 GHz in the microprocessor, which originates from the limitation of further scaling the power density of transistors, determined by power supplied voltage (V_{DD}). Because of the restraint of further scaling down, V_{DD} undesirably provides the huge power dissipation in the microprocessor when the faster clock speed is pursued, which can result in preventing development towards the higher frequency.

Why is the issue of V_{DD} scaling raised? To reduce the V_{DD} without losing the performance of the transistor, the threshold voltage (V_{TH}) should be simultaneously reduced by the same amount of variation in V_{DD} not to lose the performance of transistor (i.e., ON-STATE drain current (I_{ON})) as shown in **Fig. 1.4(a)**. Subsequently, it is inevitable that the OFF-STATE drain current (I_{OFF}) becomes exponentially increased due to the physical limit of subthreshold swing (SS) in the drain current (I_{DS})–gate voltage (V_{GS}) characteristics for the metal-oxide-semiconductor field-effect transistors (MOSFETs), resulting in soaring the standby power dissipation. Note that the steepness of transfer characteristics ($I_{\mathrm{DS}} - V_{\mathrm{GS}}$) in the subthreshold region is distinguished by SS. The physical limit of SS originates from the thermionic transport over the energy barrier of the channel region due to the tail of the Boltzmann distribution of charge carriers in the source region. Hence at least 60 mV is needed to increase I_{DS} by ten times in the subthreshold region, leading to the physical limit of SS (i.e., 60 mV/decade) at room temperature. The inevitable restraints on I_{OFF}, V_{TH}, and V_{DD} scaling has become the major obstacle to delivering reasonable performance for the next generation of CMOS technology.



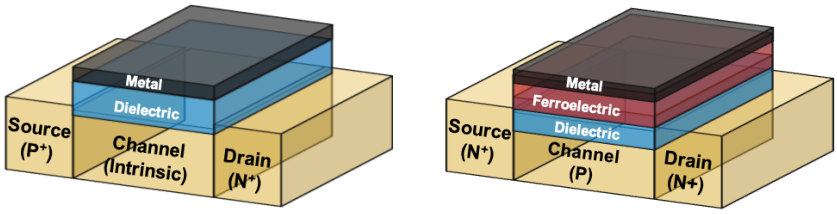
(a) (b)

Fig. 1.4. Schematic of transfer characteristics ($I_{DS} - V_{GS}$) for (a) conventional MOSFET and (b) steep switching FET.

1.2 Steep Switching FETs

Notwithstanding all efforts to continue scaling down the CMOS device, Moore's law appears to eventually reach the end of the line due to ever-increasing power dissipation. To keep developing CMOS technology, alternate transistors exhibiting better energy efficiency beyond the conventional CMOS devices are necessary. **Fig. 1.4(b)** shows a desirable $I_{DS} - V_{GS}$ of the alternate transistors. Even though the V_{DD} is reduced without sacrificing the performance (I_{ON}) for the next technology node, the OFF-state drain current can maintain the same level as the previous node due to scalable SS beyond 60 mV/dec at room temperature. The transistors which can offer sub-60 mV/dec SS at room temperature are called steep-switching FETs.

The steep switching FETs have received much attention as next-generation devices. Among steep switching devices, negative capacitance field-effect transistors (NCFETs) and tunnel field-effect transistors (TFETs) are the two most popular steep switching devices, as shown in **Fig. 1.5**.



(a) (b)

Fig. 1.5. Three-dimensional structure of (a) tunnel FET (TFET) and (b) negative capacitance FET (NCFET).

Fig. 1.5(a) shows the structure of TFET. The source/channel/drain configuration of TFET is simply a heavily doped p-type/intrinsic/heavily doped n-type semiconductor. It works with an alternative transport mechanism which is carrier injection by band-to-band tunneling from the source-to-channel region, resulting in surmounting the 60 mV/dec SS of the switching limit. The main mechanism for n-type TFET is as follows: Electrons can tunnel from the valence band of the heavily doped p-type source region to the conduction band of the intrinsic channel region as soon as those two energy bands are aligned. However, due to the insufficient I_{ON} caused of the limited band-to-band tunneling rate, the performances of TFETs are difficult to be acceptable for low-power applications [9]. Therefore, many studies have tried to improve both I_{ON} and SS by engineering a bandgap of the source region, adapting a heterojunction structure composed of materials such as Ge or III–V semiconductors [9]–[11] to enhance the tunneling probability. Although different bandgap materials have been exploited, satisfying the performance requirements for low-power applications is still challenging.

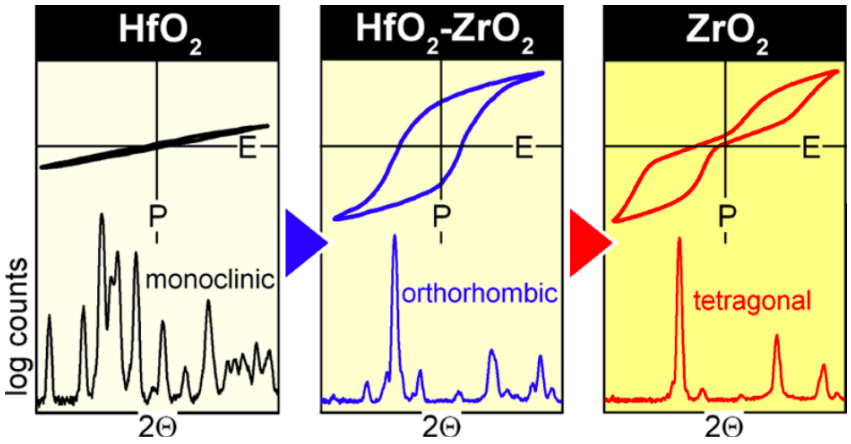
Unlike the TFET, NCFETs have advantages compared to other competing low-power technologies. A transport mechanism of conventional MOSFET can be implemented by simply replacing the gate oxide with ferroelectric (FE)/dielectric (DE) layers, which is a basic structure of NCFET as shown in **Fig. 1.5(b)**. In the NCFET, the channel potential can be amplified with the aid of the FE layer. Therefore, the physical limit of subthreshold swing in the conventional MOSFET can be overcome. This potential amplification is explained by the NC concept [12]. By inserting an FE capacitor (with negative capacitance) on a DE capacitor (FE-DE connected in series), the series capacitance of FE-DE becomes greater than the capacitance of DE only. Details will be discussed later in 1.3.2.

1.3 Negative Capacitance (NC) FETs

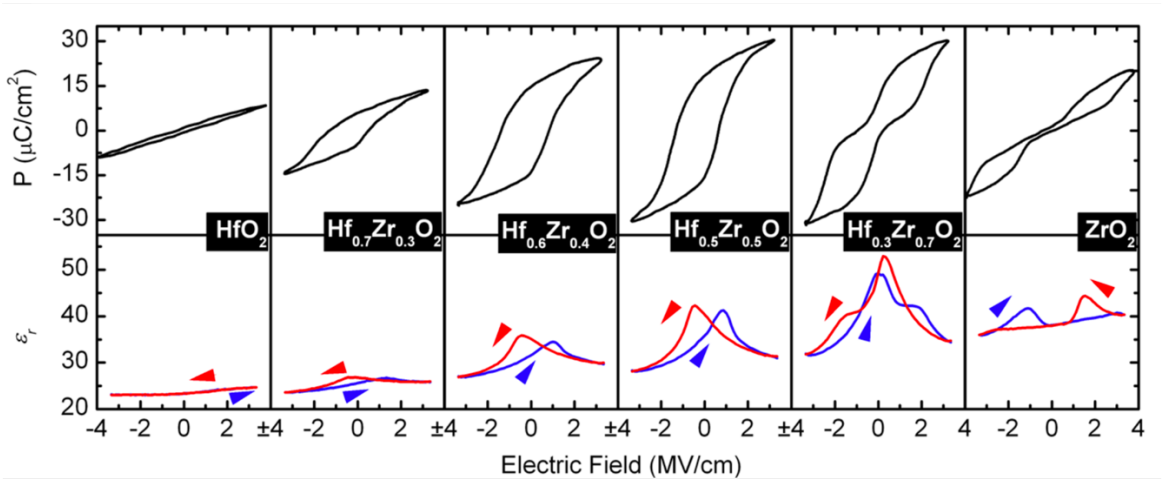
1.3.1 Ferroelectric (FE) Materials

Before discussing the NCFET, FE materials are investigated in this section first since FE is a key material for the NCFET. The FE materials show nonlinear hysteretic behavior of spontaneous polarization (P) under the applied electric field across the FE (E_{FE}) and it has been studied for the past hundred years [13]. The perovskite structure of $Pb[Zr_XTi_{1-X}]O_3$ ($0 \leq x \leq 1$) (PZT) or $BaTiO_3$ (BTO) is well-known as a conventional FE material. The FE material manifests hysteresis behavior, thereby exploiting FE as memory devices.

Recently, since a negative capacitance (NC) concept from FE material was proposed [12], the FE-based FETs are used as steep switching devices for low-power applications. Many experimental and theoretical works using the classical FE materials are reported to support the possibility that shows steep switching characteristics of the NCFETs [14]–[23]. It is noteworthy that NCFETs generally exhibit hysteresis originating from the hysteretic response of the FEs, which is necessary for memory devices, while hysteresis should be suppressed for logic devices. Even though the previous results show the steep switching characteristics, there are critical issues regarding the fabrication of the conventional FE. The fundamental scaling issue is that the thickness of conventional perovskite-structure FEs is limited to around 50 nm to obtain robust ferroelectricity [24]. Besides, such films deposited using the conventional perovskite-structure FEs are not acceptable for mass manufacturing due to the lack of CMOS compatibility [25]–[28]. Hence, it is very challenging to utilize the state-of-the-art logic technology node.



(a)



(b)

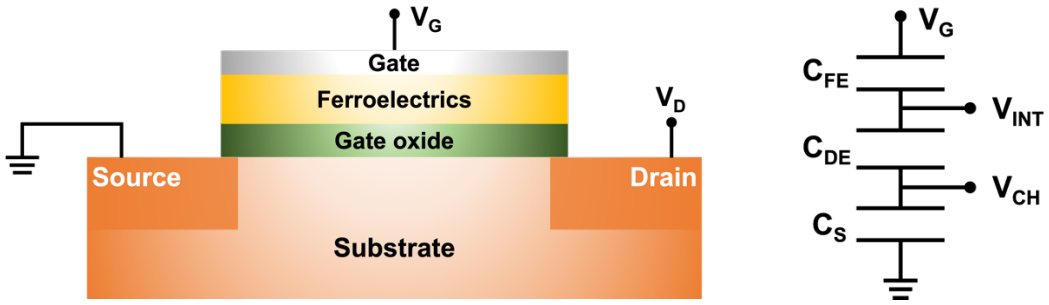
Fig. 1.6. Polarization vs. the electric field (a) with phase transitions and (b) with permittivity from 9-nm thin HfO_2-ZrO_2-based capacitors. Permittivity is calculated from the small-signal capacitance as a function of the electric field [29].

Since 2011, however, hafnium-based FE materials have made a major breakthrough by providing a solution to the aforementioned issues. First, J. Muller et al. [29] reported the ferroelectric properties of the Zr-doped HfO_2 (HZO) capacitor, as shown in **Fig. 1.6**. It appears that the mixed HfO_2 and ZrO_2 oxides manifest ferroelectricity attributed to a tetragonal to orthorhombic transformation during cooling with the aid of a TiN electrode, which can result in a noncentrosymmetric, orthorhombic phase.

Subsequently, several reports have revealed that the hafnium-based FE material can be successfully implemented in the NCFET exhibiting steep switching characteristics with hysteresis and hysteresis-free condition [14]–[20]. Therefore, due to the CMOS compatibility, the scalable hafnium-based FE becomes one of mainstream FE materials in the NCFET field.

1.3.2 NCFET using NC Phenomenon in FE

NCFET is one of the most promising steep switching devices exhibiting sub-60 mV/decade SS at room temperature by exploiting an NC phenomenon, which can be observed when FE is incorporated into the MOSFET.



(a) (b)

Fig. 1.7. (a) Cross-sectional view of NCFET and (b) its simplified equivalent capacitor network model.

Fig. 1.7 shows a structure of an NCFET, including a FE material on the gate oxide in the gate stack and its simplified equivalent capacitor network. C_{FE}, C_{DE}, and C_{S} are capacitances in the FE, DE, and semiconductor, respectively. In order to understand how the sub-60 mV/dec SS can be attained, the equation of SS for NCFET is required. It can be expressed as follows:

$$SS = \frac{\partial V_{\mathrm{GS}}}{\partial V_{\mathrm{INT}}} \times \frac{\partial V_{\mathrm{INT}}}{\partial \psi_{\mathrm{CH}}} \times \frac{\partial \psi_{\mathrm{CH}}}{\partial log(I_{\mathrm{DS}})} \tag{1}$$

where V_{GS} and V_{INT} are a gate-to-source voltage and potential at the interface between the FE and DE, respectively. Note that the potential difference across the FE is denoted by V_{FE} which is equal to $V_{GS} - V_{INT}$. The inverse of the first term on the right-hand side (RHS) is the voltage gain defined as $A_V = \partial V_{INT}/\partial V_{GS}$ and the rest part represents the SS equation for the base FET. $\partial \psi_{CH}/\partial log(I_{DS})$ is fixed as $ln(10) \times kT/q$, where kT/q is thermal voltage, resulting in gaining 60 mV at room temperature. The ideal case of the base FET could entirely project the internal voltage into the channel region without any loss of potential (i.e., $\partial V_{INT}/\partial \psi_{CH} = 1$), which yields 60 mV/dec at 300 K. Therefore, the limitation of SS could be sub-60 mV/dec as long as the voltage gain (A_V) is larger than 1.

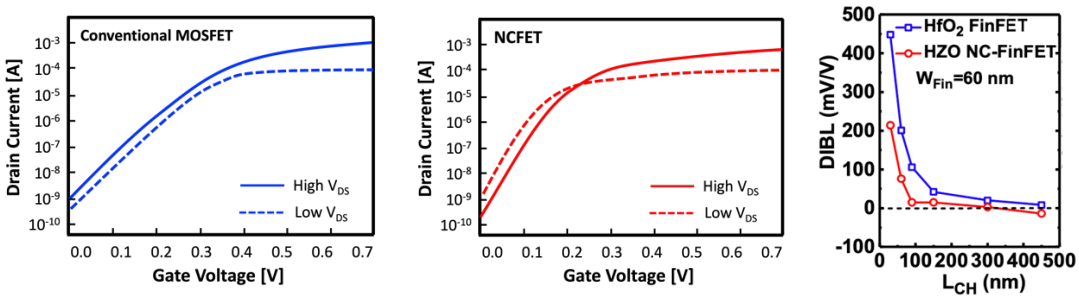
Now the question becomes how we can achieve $A_V > 1$. From the voltage divider rule in series-connected capacitors, the relation between V_{GS} and V_{INT} is given by

$$V_{INT} = \frac{C_{FE}}{C_{MOS}+C_{FE}} V_{GS} \tag{2}$$

where C_{DE} and C_S connected in series are grouped as C_{MOS} (${C_{MOS}}^{-1} = {C_{DE}}^{-1} + {C_S}^{-1}$). According to Eq. (2), $A_V = \partial V_{INT}/\partial V_{GS} = C_{FE}/(C_{FE} + C_{MOS})$ and the requirements for $A_V > 1$ are 1) $C_{FE} < 0$ and 2) $|C_{MOS}| < |C_{FE}|$. Note that as C_{MOS} is reached to C_{FE}, the voltage gain becomes maximized. Consequently, the steep switching characteristics can be attained when C_{FE} is negative and the transistors using the concept of NC are called NCFETs.

1.3.3 Negative DIBL and Negative Differential Resistance in NCFET

Drain-induced barrier lowering (DIBL) is a short channel effect in the ultra-scaled CMOS devices, resulting in a reduction of V_{TH} at higher drain voltages. A schematic of transfer curves for (a) the conventional MOSFET and (b) NCFET at different V_{DS} are illustrated in **Fig. 1.8** to show DIBL. Especially, in the case of NCFET, the short channel effect can be suppressed and even the V_{TH} at low V_{DS} is smaller than the V_{TH} at high V_{DS}, which gives a negative value of DIBL (see **Fig. 1.8(c)**). The negative DIBL is mainly caused by the capacitance coupling from the drain to the interface between FE and DE [30]–[32].



(a) (b) (c)

Fig. 1.8. Schematic of $I_{DS} - V_{GS}$ curves for (a) conventional MOSFET and (b) NCFET at high and low V_{DS} to represent DIBL. (c) Measured DIBL vs. channel length curve for FinFET and NC-FinFET [31].

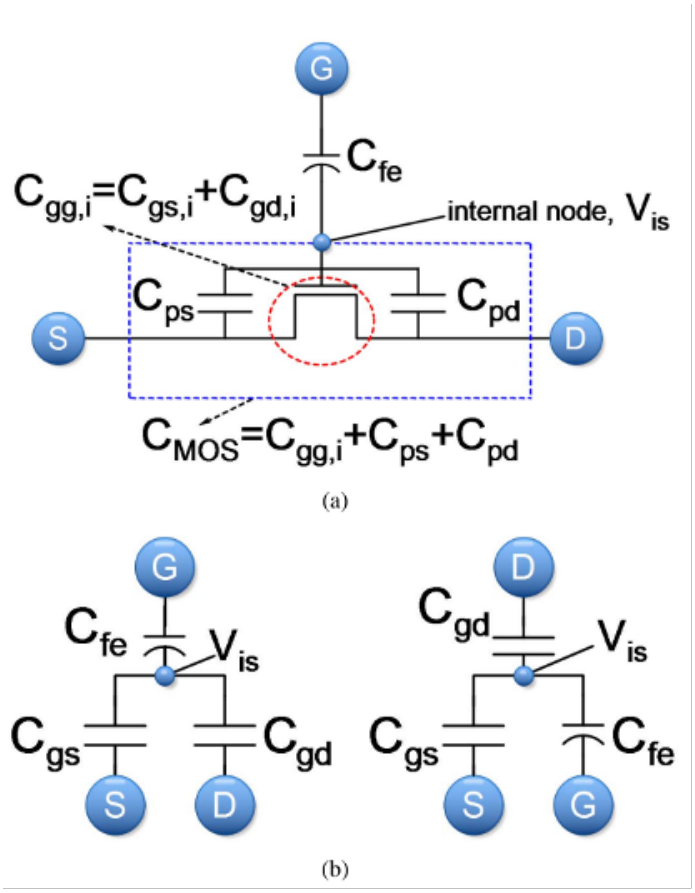


Fig. 1.9. (a) Equivalent circuit model for NCFET and (b) simplified circuit with gate-/drain-side point of view ($C_{gd} = C_{gd,i} + C_{pd}$ and $C_{gs} = C_{gs,i} + C_{ps}$) [30].

Another interesting feature caused by NC is a negative differential resistance (NDR). In the $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristics of NCFETs, we have been able to observe that the drain current is decreased as V_{DS} increases, which can result in negative slope of $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ curve called the NDR. The NDR effect can be explained using Eq. (3) and (4). **Fig 1.9(a)** shows the equivalent circuit model for NCFET. The capacitance of FE layer and baseline FET are labelled as C_{FE} and C_{MOS}. Note that the sum of intrinsic capacitance ($C_{\mathrm{gg,i}}$) and parasitic capacitances (C_{ps} and C_{pd}) is C_{MOS} as shown in **Fig. 1.9(a)**. **Fig. 1.9(b)** illustrates simplified circuits (with the relation of $C_{\mathrm{gd}} = C_{\mathrm{gd,i}} + C_{\mathrm{pd}}$ and $C_{\mathrm{gs}} = C_{\mathrm{gs,i}} + C_{\mathrm{ps}}$) in gate-side (left) and drain-side (right) point of view. The slope of $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ is given as

$$\frac{dI_{\mathrm{DS}}}{dV_{\mathrm{DS}}} = \frac{dI_{\mathrm{DS}}}{dV_{\mathrm{INT}}} \times \frac{dV_{\mathrm{INT}}}{dV_{\mathrm{DS}}} \tag{3}$$

where

$$\frac{dV_{\mathrm{INT}}}{dV_{\mathrm{DS}}} = \frac{C_{\mathrm{gd}}}{C_{\mathrm{FE}}+C_{\mathrm{gs}}+C_{\mathrm{gd}}} = \frac{C_{\mathrm{gd}}}{C_{\mathrm{FE}}+C_{\mathrm{MOS}}}. \tag{4}$$

Note that both V_{INT} and V_{is} are internal node potential. According to the aforementioned requirement of 1) $C_{\mathrm{FE}} < 0$ and 2) $|C_{\mathrm{MOS}}| < |C_{\mathrm{FE}}|$ for $A_{\mathrm{V}} > 1$, $dV_{\mathrm{INT}}/dV_{\mathrm{DS}}$ can be negative, so that we can obtain the negative slope of $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ $(dI_{\mathrm{DS}}/dV_{\mathrm{DS}} < 0)$. The negative DIBL and NDR effects can be confirmed and observed by experiments as shown in **Fig. 1.10**.

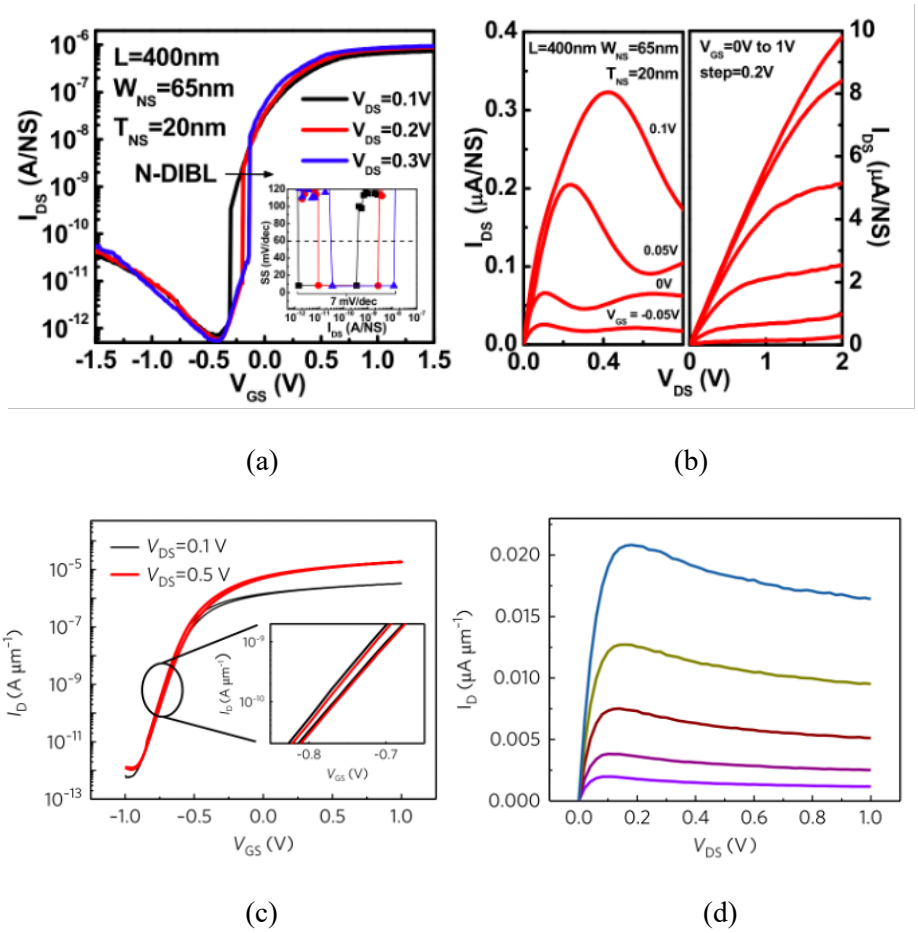


Fig. 1.10. Experimental results for the negative DIBL ((a) and (c)) and NDR ((b) and (d)) [16], [19].

1.3.4 Experimental Observation of NCFET

After the concept of NC was proposed in 2008 [12], the first NCFET was demonstrated by Ruso et al. using FE of P(VDF-TrFE) in 2010 [33]. Note that the early phase of experimental works focused on the steep switching characteristics despite presenting significant hysteresis [34]–[36]. However, recent studies have mainly demonstrated steep switching and hysteresis-free transfer behaviors for low-power CMOS devices by controlling drain voltage or the thickness of the ferroelectric layer [14]–[18]. After the first demonstration, the NCFETs with traditional FE (e.g., P(VDF-TrFE) [15], [33], [34] / $BiFeO_3$ (BFO) [35]/ PZT [36]) were extensively investigated to achieve sub-60 mV/decade SS for steep-switching CMOS transistors (see **Fig. 1.11**). However, as mentioned in 1.3.1, the thin film from

traditional FEs is not acceptable to implement into an NCFET due to the weakness of its ferroelectricity, which is not suitable for scaled CMOS technologies.

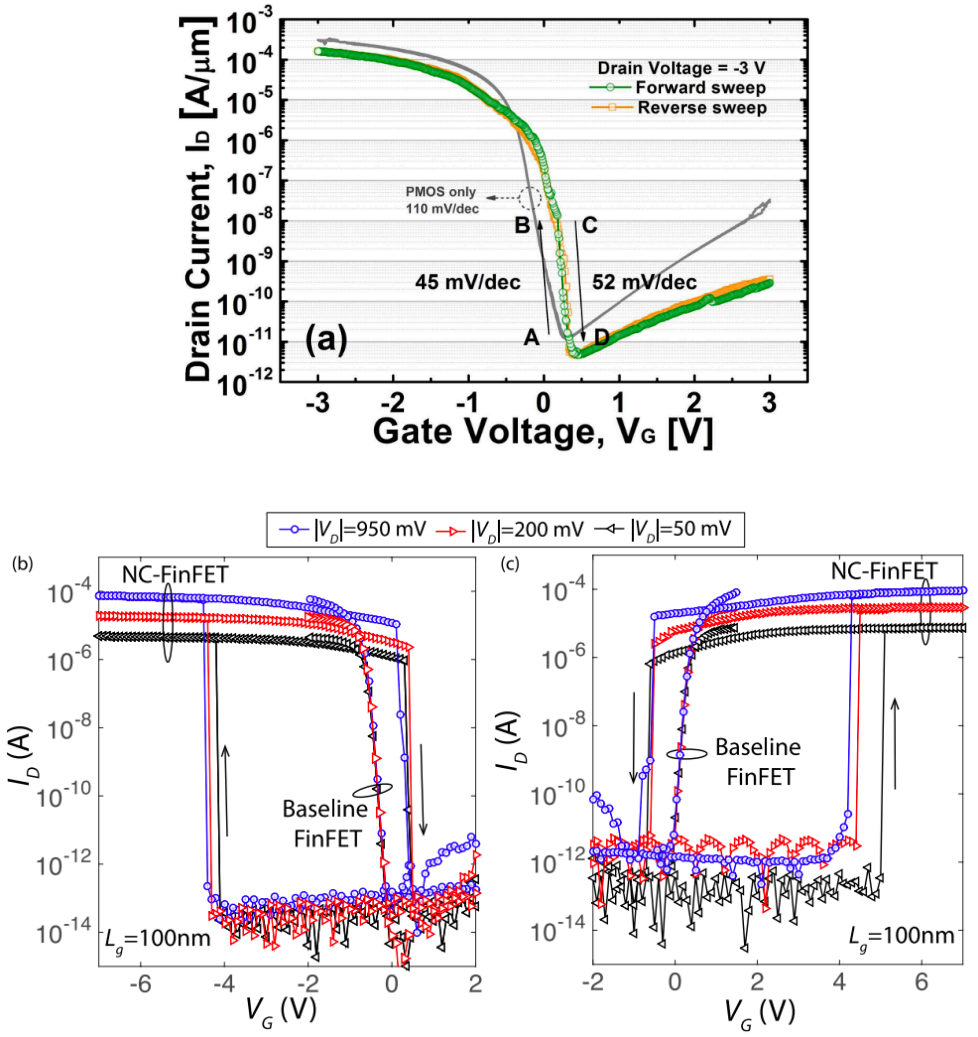


Fig. 1.11. Measured $I_D - V_G$ (a) for p-type MOSFET with 16-nm-thick P($VDF_{0.75}$-$TrFE_{0.25}$) FE exhibiting steep switching SS and hysteresis-free [15] and (b) and (c) for FinFET with 250-nm-thick $BiFeO_3$ FE showing hysteresis and sub-60 mV/dec [35].

Since 2012, the scenario for NCFET development has been changed due to the breakthrough discovery of HZO as an FE material [29]. Existing processes in the current commercial production can be used to integrate the FE into the gate stack, and it has been made possible by the compatibility of state-of-the-art CMOS technology. Thanks to this discovery, a large number of HZO-based NCFETs experimental works showing steep switching characteristics have been reported [14], [17]–[20].

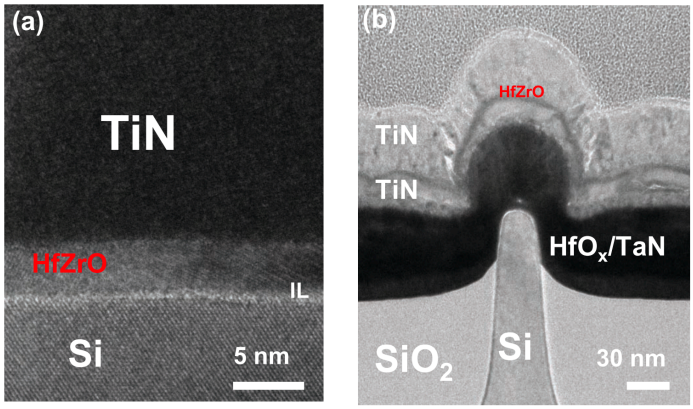
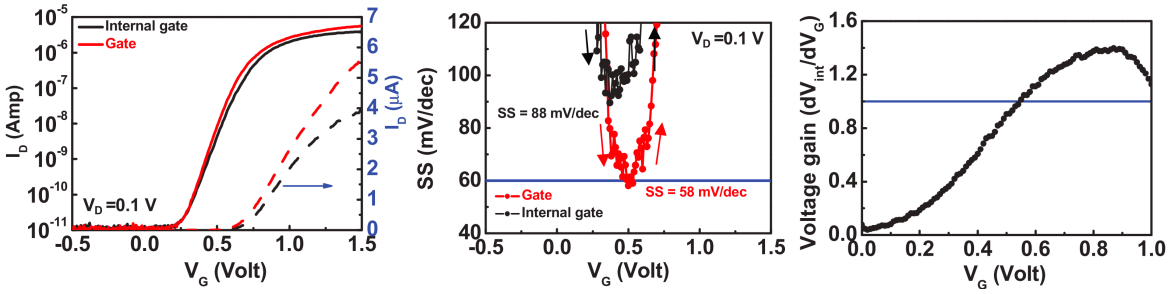


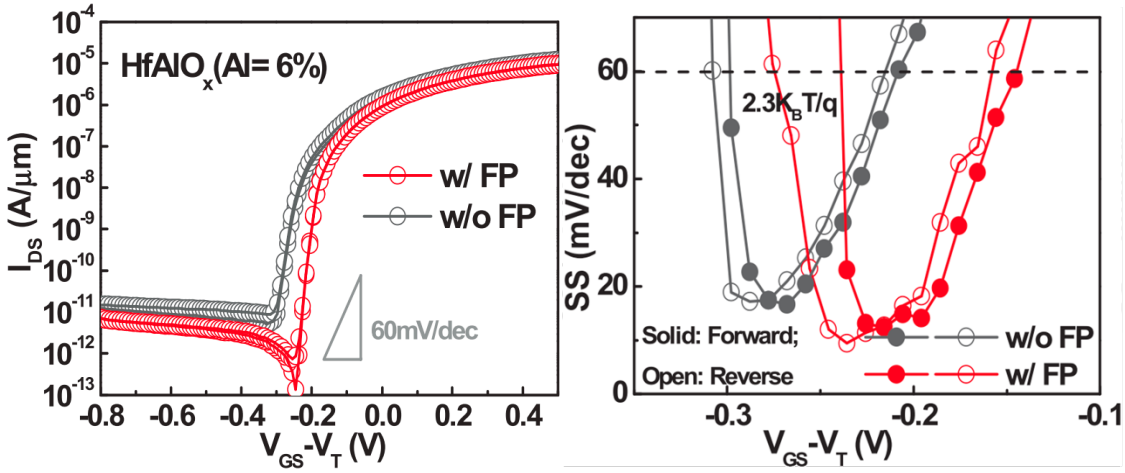
Fig. 1.12. TEM image of (a) a $Hf_{0.42}Zr_{0.58}O_2$ capacitor and (b) NC-FinFET with 5-nm-thick $Hf_{0.42}Zr_{0.58}O_2$ film [17].



(a) (b) (c)

Fig. 1.13. Measured (a) $I_D - V_G$, (b) $SS - V_G$, and (c) $dV_{INT}/dV_G - V_G$ plot at $V_D = 0.1$ V for the structure shown in Fig. 1. 12. The black curves in (a) and (b) represent the drain current and its SS as a function of V_{INT} (the potential at the internal gate, which is the gate of base FinFET). Note that the voltage gain is denoted by dV_{INT}/dV_G in (c) [17].

Fig. 1.12 shows the first HZO-based NC device demonstrated by Li et al., which was built on a FinFET with 30 nm channel length (L_{CH}) and 5 nm FE thickness (T_{FE}) [17]. The measured $I_D - V_G$ of NC-FinFET exhibits steep switching SS and hysteresis-free as shown in **Fig. 1.13(a) and (b)**. We can confirm that the voltage gain denoted by dV_{INT}/dV_G can be larger than 1 with the aid of FE in **Fig. 1.13(c)**, which is the requirement of steep SS as discussed in 1.3.2. Subsequently, Lee et al. reported NCFETs using an ultra-thin HZO of 1.5-nm T_{FE} and Krivokapic et al. demonstrated complementary NCFET on 14 nm FinFET technology [14], [18]. Furthermore, the GAA structure of NCFETs is experimentally presented with extremely steep switching [19].

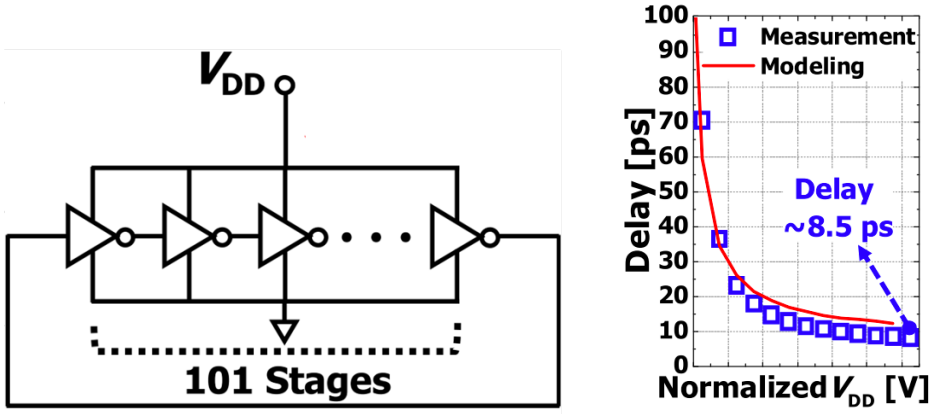


(a) (b)

Fig. 1.14. (a) $I_{DS} - V_{GS}$ and (b) SS characteristics of NCFET using 2.5-nm-thick $HfAlO_X$ FE with and without fluorine treatment for defect passivation (FP) [37].

Here, the important questions raised in the device community about NCFETs are as follows: 1) defects on the FE surface and 2) switching speed and response time. The performance degradation caused by defects is a huge concern for device reliability. **Fig. 1.14** shows the transfer characteristics of $HfAlO_X$-based NCFET with and without defect passivation using fluorine [37]. It is beneficial for switching characteristics by utilizing fluorine passivation (FP) treatment on the FE surface so that the

leakage current is suppressed by at least one-order of magnitude and the SS is improved by 50 %. Next, to answer the second question, Chatterjee et al. demonstrated that the intrinsic speed limit of NCFETs with doped hafnium oxides is only 270 fs, which is shorter than the general intrinsic delay for logic circuits (~1 ps) [38], [39]. Subsequently, as shown in **Fig. 1.15**, Kwon et al. reported on the measurement of a 101-stage ring oscillator (RO) based on state-of-the-art 14 nm FinFET technology with an FE layer [40]. It shows that no slowdown is associated with the NCFET at the highest speed tested-per-stage delay (~8.5 ps). Lastly, Li et al. reported that the measured cut-off frequency (f_T) of NC-FinFET can be 23.1 GHz, which was 23% higher than that of control FinFET [41].



(a) (b)

Fig. 1.15. (a) Schematics of the 101-stage ring oscillator (RO) based on state-of-the-art 14 nm NC-FinFET and its (b) measured delay plot for 2-fin NC-FinFET RO. Note that the stage delay can be as small as 8.5 ps [40].

1.3.5 Theoretical Efforts for NCFET

Theoretical works have made efforts to provide insights and support performance enhancement caused by NC in the experimental results by modeling the FE material as well as NCFET. Moreover, simulation tools are essential to optimize the performance of NCFETs, since the device engineering by only experiments will be costly, time-consuming, and complicated.

D. Jimenez et al. reported the first model for the NCFET in 2010 [42], in which the authors evaluated the opportunity of NCFETs for low power switching applications under various assumptions, including a single domain picture within the FE material. Similarly, Chen et al. developed a drain-current model in 2011 by coupling Pao-Sah double integral with the FE model [43]. Subsequently, Ota et al. provided a fully coupled three-dimensional technology computer-aided design (TCAD) tool along with the Landau-Khalatnikov equation for the FE model [44]. In addition, NCFET models, in which the FE model was solved with the standard BSIM model, were presented to support experimental results shown in **Fig. 1.16** [45]–[47]. After discovering HZO, Kobayashi et al. provided device design guidelines for HZO-based NCFETs in terms of operation speed, material requirements, and energy efficiency [48].

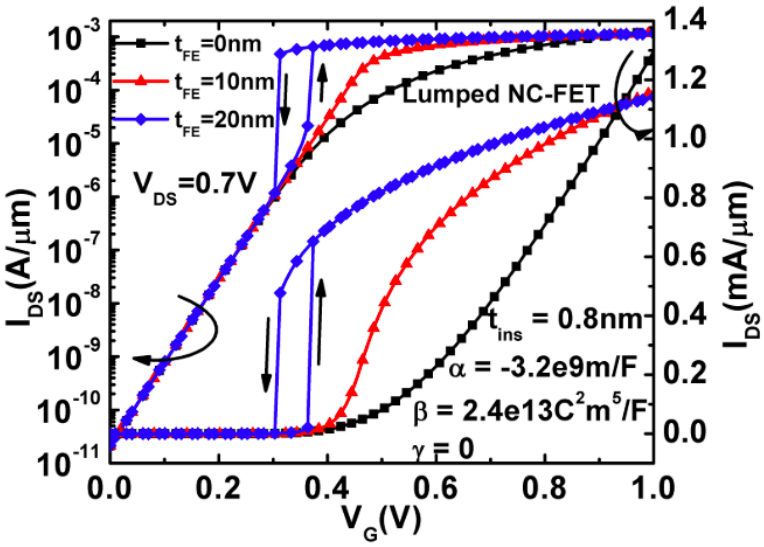
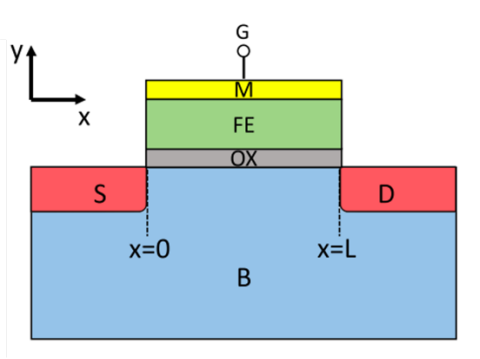
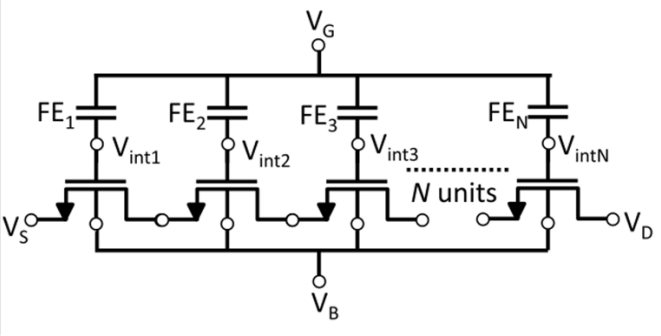


Fig. 1.16. Simulated $I_D - V_G$ for NCFET using a compact model, in which the FE model was solved with the standard BSIM model [47].

Up to this point, however, the theoretical studies of NCFET have been biased toward the single-domain picture, which assumes homogeneous polarization within the ferroelectric layer. Undoubtedly, this is a simplified approach compared to the real picture of ferroelectric behavior, leading to inaccurately evaluating device performance. Therefore, to handle more realistic domain, each domain is modelled as a separate FE capacitor connected in parallel to describe multi-domain picture by Hoffmann et al. [49]. In addition, **Fig. 1.17** shows the concept of a parallel capacitor network for FE employed by Pahwa et al. to investigate two different configurations of NCFET (i.e., with and without an intermetal layer between FE and dielectric layer) [50]. Although this circuit model tried to mimic a multi-domain FE, it failed to capture the realistic multi-domain properties such as polarization interactions.



(a)



(b)

Fig. 1.17. (a) Schematics of NCFET with metal-FE-oxide-semiconductor configurations and (b) its equivalent circuit proposed by [50].

However, Saha et al. presented a multi-domain FE-based (see **Fig. 1.18**) NCFET model by self-consistently solving Poisson's equation, a transport equation for carriers and Landau-based model with consideration of the polarization interaction [51]–[54].

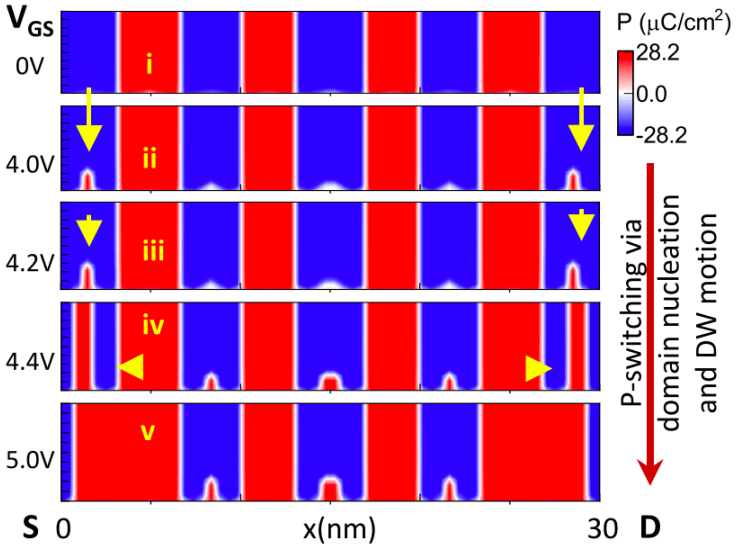


Fig. 1.18. Polarization profile in multi-domain FE exhibiting domain wall propagation based on polarization switching [52].

1.4 Thesis Overview

In this thesis, a novel computational framework for FE-based devices by means of negative capacitance is proposed. Through the proposed model, numerical simulations are carried out not only to assess the performance but also to provide insights behind the FE devices from ferroelectric-based capacitors to NCFETs.

In **chapter 2**, methodologies of device simulation are introduced. First, behaviors of polarization in FE with respect to electric field are explained using two approaches: Landau and Miller model. Next, the electrostatics of the entire device are described by discretized Poisson's equation. Finally, non-

equilibrium Green's function is introduced to represent the quantum transport of the carriers in the black phosphorus channel region.

In **chapter 3**, hysteretic jump points (HJPs) are modeled and how hysteresis responds to different parameters used is described. First, the energy landscape of FE-MOS capacitor is explored based on the Gibbs free energy, considering forward and backward sweep of gate voltage, to identify the HJPs. It should be noted that simulations in this chapter are carried out by calculating an analytic model for FE-MOS capacitor describing changes of Gibbs free energy, whereas fully numerical simulations considering spatial information of structure are used from chapter 4 to 6. The simulation result shows that the surface potential of HJP has a logarithmic relation to the doping concentration of the semiconductor while FE thickness (T_{FE}) and gate oxide thickness (EOT) shift the value of the surface potential up or down. Based on the developed model, hysteresis width and height to evaluate the extent of hysteresis and the amplification of potential is quantitatively introduced. Results also show that hysteresis width is a strong function of EOT and T_{FE} but the potential amplification is limited, especially when EOT is thin. In addition, the effect of doping concentration on the hysteresis window is minimal, particularly with thick FE layer. The proposed model provides a useful tool to directly investigate hysteresis, which makes it possible to modify the hysteresis window by engineering parameters for different target applications.

In **chapter 4**, NC characteristics of a ferroelectric-dielectric (FE-DE) capacitor by means of a fully numerical, self-consistent simulation based on the Miller model (MM) and Poisson's equation are demonstrated. Over the years, the Landau model (LM) has been widely used, which fits experimental data of spontaneous polarization vs. electric field ($P - E_{\mathrm{FE}}$) characteristics using a so-called 'S-curve'; however, it cannot capture different transitions of polarization switching and can also fail to properly represent the material properties of certain ferroelectrics. To overcome such limitations of the LM, I have used the MM to simulate an FE-DE capacitor. Even though the MM seemingly fails to show steep switching characteristics due to the absence of the negative slope in the $P - E_{\mathrm{FE}}$ curve unlike the LM, the simulation result exhibits the NC characteristics of FE-DE capacitors with significant internal voltage amplification. Notably, the effect of different transitions of polarization switching is investigated by varying the coercive field of FE within the MM, and it exhibits that greater NC characteristics can be achieved with a ferroelectric having more abrupt switching transition. I have also investigated the impact of other material parameters of FE, such as saturation and remnant polarization, on the NC characteristics of FE-DE capacitors. The results provide comprehensive insight into the

mechanism of the negative capacitors, suggesting sophisticated engineering of material and device parameters to seek desired performance of NC devices.

In **chapter 5**, I demonstrate a new computational framework for gradually switching FE-based NCFETs in steady-states. In particular, three modules are iteratively solved: (i) non-equilibrium Green's function (NEGF) for carrier transport, (ii) Poisson's equation for electrostatics, and (iii) the Miller model for $P - E_{\mathrm{FE}}$. Unlike the FE-DE capacitor, polarization varies along the device position due to the applied field across the device, and hence, polarization interactions are taken into account. This simulation result exhibits hysteresis-free, steep-switching characteristics of the NCFET even with the 'positive slope' in the $P - E_{\mathrm{FE}}$ curve originating from the MM. I have also explicated the physical origin of the experimentally demonstrated critical ferroelectric thickness, at which minimum subthreshold swing can be achieved, using two competing mechanisms. Finally, FE parameters (i.e., saturation polarization, remnant polarization, and coercive field) within the MM are varied to investigate their effects on the characteristics of the NCFET. This work not only suggests a novel computational framework for the simulation of the NCFET based particularly on gradually switching FE, but also provides irreplaceable physical insight into the optimization of the NCFET by tuning material and device parameters.

In **chapter 6**, NCFETs exhibiting a partially polarized ferroelectric (PPFE) are demonstrated by means of a novel approach under the quasi-static gate voltage sweep. For the PPFE, the MM-based FE minor loop model has been used to describe its switching behavior. By performing a fully numerical device simulation including NEGF, Poisson's equation, and FE module for PPFE along with a proposed process, I present the difference between the NCFET assuming a fully-polarized FE (FPFE-NCFET) and NCFET considering PPFE (PPFE-NCFET). Simulation results exhibit that when the FPFE is assumed, the subthreshold swing for a NCFET is overestimated compared to the PPFE case. Also, the drain-induced barrier lowering (DIBL) for both FPFE-/PPFE-NCFET is examined and the negative DIBL is observed. Lastly, the effect of the channel length (L_{CH}) and FE thickness (T_{FE}) on the performance of PPFE-NCFET are investigated. The proposed novel approach for the simulation and its discussion would be helpful in understanding of not only FE behavior but also NCFET comprised of PPFE.

In **chapter 7**, contributions and conclusions of this dissertation are summarized and suggestions for future works are discussed.

Chapter 2
Simulation Methods

2.1 Polarization Behavior in FE

2.1.1 Landau-Khalatnikov Equation

The Landau-Khalatnikov equation is most widely used model to describe the spontaneous polarization (P) with respect to the applied electric field across the FE (E_{FE}). For the Landau approach of FE, Gibbs free energy (G) modelled by adopting even power series expression of P is used under an E_{FE}

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - E_{FE}P, \tag{1}$$

where α, β, and γ are material parameters to determine the polarization behavior. Particularly, α is a function of temperature (T) as a form of $\alpha_0(T - T_C)$, where α_0 is a material dependent constant (positive value), T_C is Curie temperature of the FE material. α becomes negative when a material is in the ferroelectric phase ($T < T_C$). Whereas the material loses its ferroelectricity under the condition of $T > T_C$, resulting in the positive α. In the Eq. (1), the FE is assumed to be a single domain which results in responding all polarizations as one polarization under an applied field. Besides, the polarization direction of uniaxial axis perpendicular to the electrode is considered. **Fig. 2.1(a)** shows the energy landscape of FE (G vs. P plot) from Eq. (1) at E_{FE} = 0. The double well energy plot implies that there are two possible polarizations at a given electric field.

To model time evolution of polarization with Gibbs free energy, the Landau-Khalatnikov equation is given as [55]

$$\frac{\partial G}{\partial P} = -\rho \frac{\partial P}{\partial t}, \tag{2}$$

where t is time and ρ is viscosity coefficient that it can characterize the relaxation time of FE. Note that the Landau-Khalatnikov equation is abbreviated to Landau equation for simplicity in this whole dissertation. By using Eq. (1) and (2), we can achieve the behavior of P with respect to E as

$$E_{\mathrm{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5. \tag{3}$$

From Eq. (3), the $P - E_{FE}$ curve can be obtained in steady states ($\partial P/\partial t = 0$) as shown in **Fig. 2.1(b)**. Polarizations located at the minimum energy states in (a) are corresponding to polarizations at the zero electric field in (b).

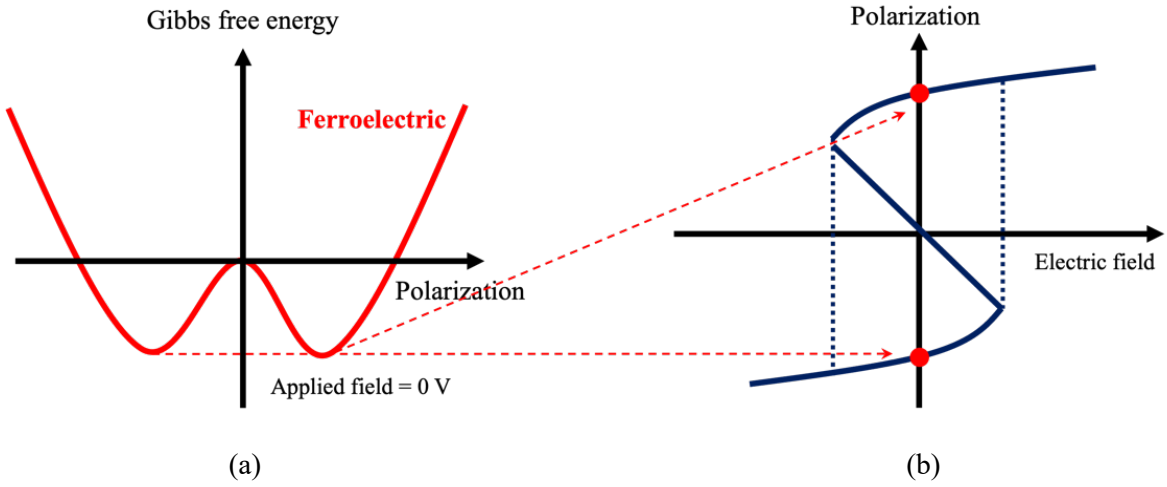


Fig. 2.1. Schematics of (a) energy landscape and (b) polarization vs. electric field curve of a stand-alone FE capacitor. Polarizations located at the minimum energy states in (a) are corresponding to polarizations at the zero electric field in (b).

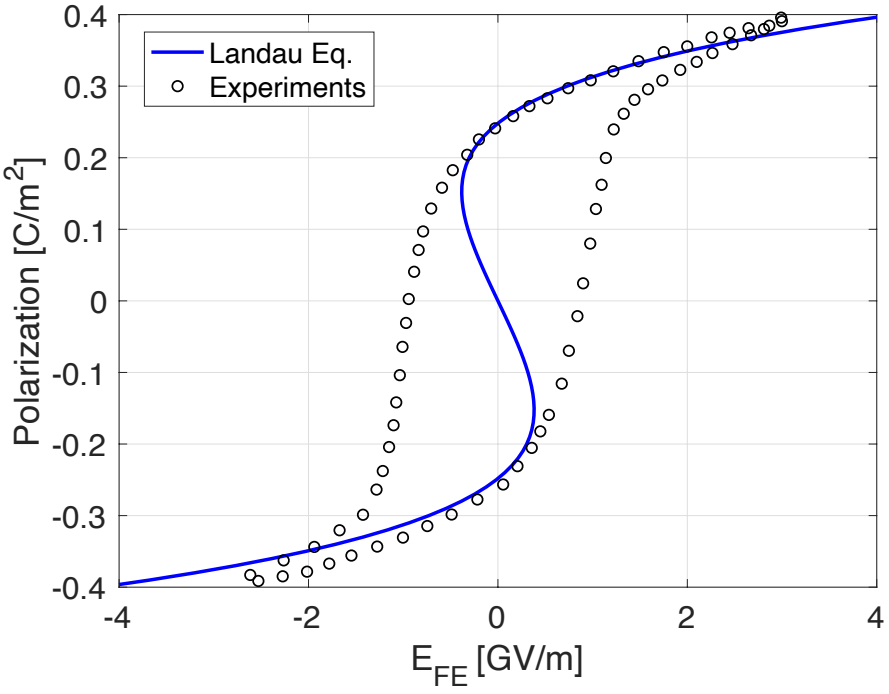


Fig. 2.2. Measured and simulated $P - E_{FE}$ curve for a stand-alone FE in steady states [56].

Fig. 2.2 shows the experiment (black dots) [56] and simulation using Eq. (3) (blue solid lines) results of $P - E_{FE}$ curve for a stand-alone FE in steady states. To fit the simulation results in experiments, the α, β, and γ (material parameters) of $-1.8 \times 10^9\ mF^{-1}$, $1.0 \times 10^{10}\ m^5F^{-1}C^{-2}$, and $5 \times 10^{10}\ m^9F^{-1}C^{-4}$ have been manually chosen and an NC region can be seen in so-called 'S-curve'. Note that α should be a negative since the FE phase is considered.

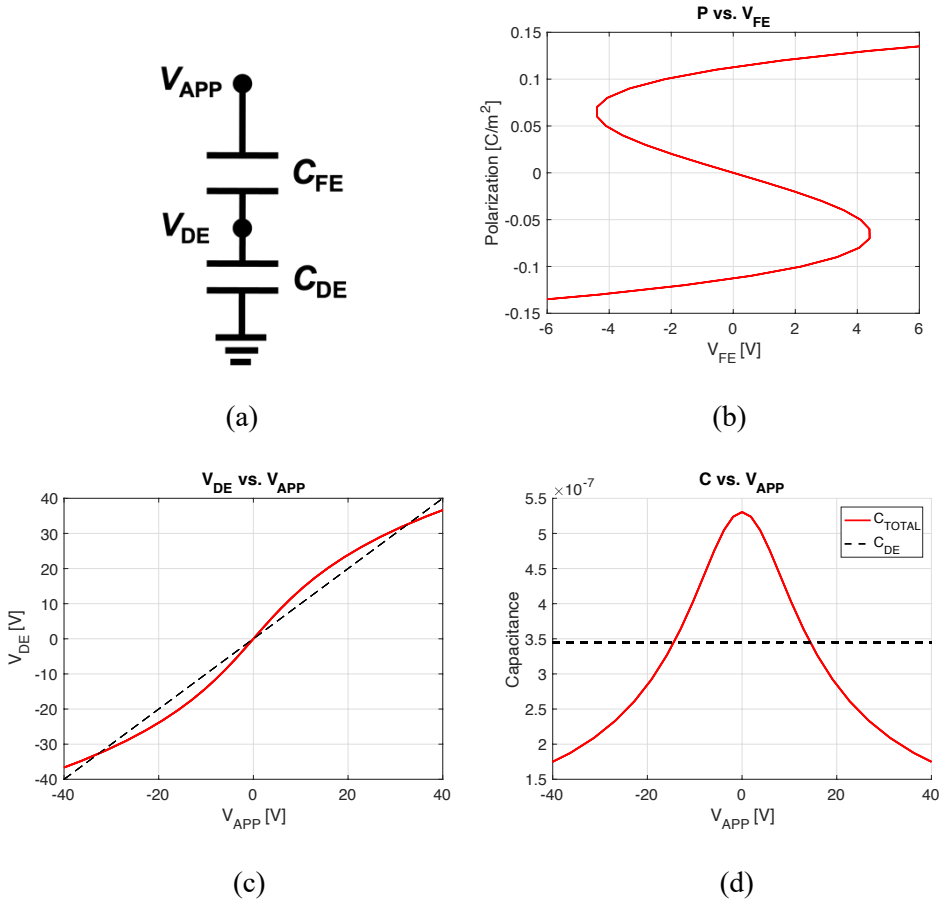


Fig. 2.3. (a) Capacitor network circuit, (b) $P - V_{\mathrm{FE}}$, (c) $V_{\mathrm{DE}} - V_{\mathrm{APP}}$, and (d) $C - V_{\mathrm{APP}}$ curve for the FE-DE capacitor.

In the perspective of the simulation process, here, the way to implement the FE into FE-based device is introduced by adopting the structure of a simple FE-dielectric (DE) capacitor in steady states. **Fig. 2.3(a)** shows the capacitor network of the FE-DE capacitor. The potential difference across the FE (V_{FE}) is given as

$$V_{\mathrm{FE}} = V_{\mathrm{APP}} - V_{\mathrm{DE}} = 2\alpha T_{\mathrm{FE}} P + 4\beta T_{\mathrm{FE}} P^3 + 6\gamma T_{\mathrm{FE}} P^5, \tag{4}$$

where the material parameters of FE are chosen for this simulation: $\alpha = -5.1 \times 10^9\ mF^{-1}$, $\beta = 2.0 \times 10^{11}\ m^5F^{-1}C^{-2}$, $\gamma = 1 \times 10^7\ m^9F^{-1}C^{-4}$, and T_{FE} (ferroelectric thickness) = 10 nm (see **Fig. 2.3(b)**). By rearranging Eq. (4), we can obtain the relation between V_{FE} and polarization as follows.

$$V_{\mathrm{APP}} = \frac{T_{\mathrm{DE}}P}{\varepsilon_{\mathrm{DE}}} + 2\alpha T_{\mathrm{FE}}P + 4\beta T_{\mathrm{FE}}P^3 + 6\gamma T_{\mathrm{FE}}P^5, \quad (5)$$

in which $V_{\mathrm{DE}} = Q/C_{\mathrm{DE}} = (P \times Area)/\left({}^{\varepsilon_{\mathrm{DE}} \times Area}/_{T_{\mathrm{DE}}}\right)$, where Q and $Area$ are a charge on the electrode and electrode size of the FE-DE capacitor. Note that $Q = P \times Area$ is assumed. For the DE, $\varepsilon_{\mathrm{DE}} = 3.9$ and $T_{\mathrm{DE}} = 10$ nm are used, respectively. **Fig. 2.3(c)** shows $V_{\mathrm{DE}} - V_{\mathrm{APP}}$ curve to estimate an internal potential (V_{DE}) variation against V_{APP}, which can result in observing voltage amplification ($dV_{\mathrm{DE}}/dV_{\mathrm{APP}} > 1$). To understand the origin of voltage amplification, the total capacitance (red solid line) and dielectric capacitance (black dashed line) as a function of V_{APP} are plotted as shown in **Fig. 2.3(d)**. The total capacitance can be larger than the DE capacitor in the series FE-DE capacitor and it is only the case when the FE capacitor has a negative value. Besides, the range of $dV_{\mathrm{DE}}/dV_{\mathrm{APP}} > 1$ is matched with that of $C_{\mathrm{TOTAL}} > C_{\mathrm{DE}}$. Consequently, the voltage amplification is originating from the NC in the FE according to the results.

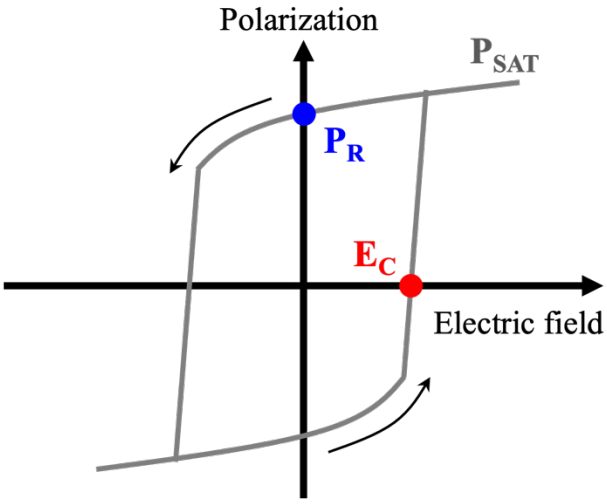


Fig. 2.4. Schematic of hysteresis loop plot ($P - E_{FE}$). Note that the saturated polarization, remnant polarization, and coercive field are denoted by P_{SAT}, P_{R}, and E_{C}, respectively.

2.1.2 Miller Equation

Miller model is a mathematical model to more focus on representing the shape of the $P - E_{FE}$ plot described as shown in **Fig. 2.4**. When the strong enough electric field is applied, the polarization in FE material becomes saturated and that is called saturated polarization denoted by P_{SAT}. Next, the FE has non-zero polarization value at zero electric field called the remnant polarization (P_{R}). Lastly, the FE shows a distinguishing feature that the polarization can be reversed over a coercive field (E_{C}) in the opposite orientation so that it yields a hysteresis loop. Note that this model reasonably assumes that the polarization curves from forward and reverse bias sweep are symmetric, which is expressed by $P_{\mathrm{FOR}}(E_{\mathrm{FE}}) = -P_{\mathrm{REV}}(-E_{\mathrm{FE}})$. By utilizing a convenient mathematical function that satisfies the requirements of polarization behavior, the polarization switching properties as a function of the applied electric field can be predicted. The hyperbolic tangent function is chosen since the reproduced switching behavior using the function is consistent with experimental data. The equation called Miller equation is as follows [57]:

$$P_{\mathrm{FE}} = P_{\mathrm{SAT}} tanh\left(\frac{E_{\mathrm{FE}} \mp E_C}{2\delta}\right) + \varepsilon_0 \varepsilon_{\mathrm{FE}} E_{\mathrm{FE}}, \tag{6}$$

where $\delta = E_{\mathrm{C}}\left[log_{10}\left(\frac{1+P_{\mathrm{R}}/P_{\mathrm{SAT}}}{1-P_{\mathrm{R}}/P_{\mathrm{SAT}}}\right)\right]^{-1}$ and ε_0 and $\varepsilon_{\mathrm{FE}}$ are permittivity of vacuum and background permittivity of FE [58], respectively. The negative sign between E_{FE} and E_{C} is used for the forward bias, whereas $E_{\mathrm{FE}} + E_{\mathrm{C}}$ is for the reverse bias. The P_{FE} is the total polarization and the first term in RHS represents the spontaneous polarization induced by the ferroelectricity in FE and the second term in RHS is the rest of contributions to the total polarization called the background polarization [58]. Note that the $\varepsilon_{\mathrm{FE}}$ can be modified in accordance with the slope of nearby P_{SAT} regions in the experimental data. Therefore, for a stand-alone FE in steady states, the $P - E_{FE}$ curve from experiment results (black dots) [56] can be fitted by that from the Miller model (using Eq. (6)) (red solid lines) as compared with Landau model results (blue solid line) as shown in **Fig. 2.5**. The experiments are well-matched with both models.

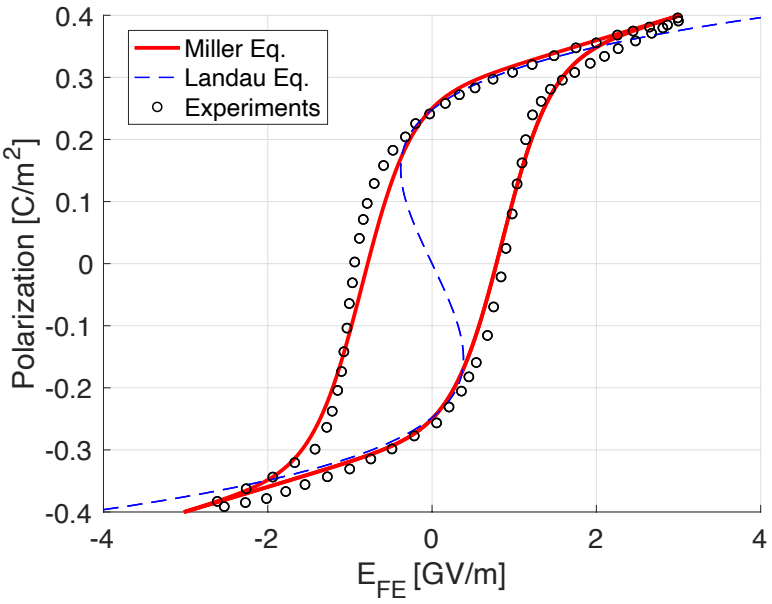


Fig. 2.5. Measured (black symbols) and simulated $P - E_{FE}$ curve using Miller (red solid line) and Landau equation (blue dashed line) for a stand-alone FE in steady states [56].

2.2 Electrostatics

2.2.1 Calculations Overview

Fig. 2.6 shows the discretized device structure of NCFET with uniformly spaced grid points. The finite-difference method (FDM) is used to calculate the electrostatic of the device. By starting with the differential form of Gauss's law, it can be written as:

$$\nabla \cdot D = \rho \tag{7}$$

, where D is the displacement field and ρ is the charge density. Since $D = \varepsilon_0 \varepsilon_r E$, in which ε_r and E are respectively a relative permittivity and electric field, Eq. (7) can be $\varepsilon_0 \varepsilon_r \nabla \cdot E = \rho$. The Poisson's equation is given as

$$-\varepsilon_0 \varepsilon_r \nabla^2 \cdot V = \rho, \tag{8}$$

due to $E = \nabla \cdot V$.

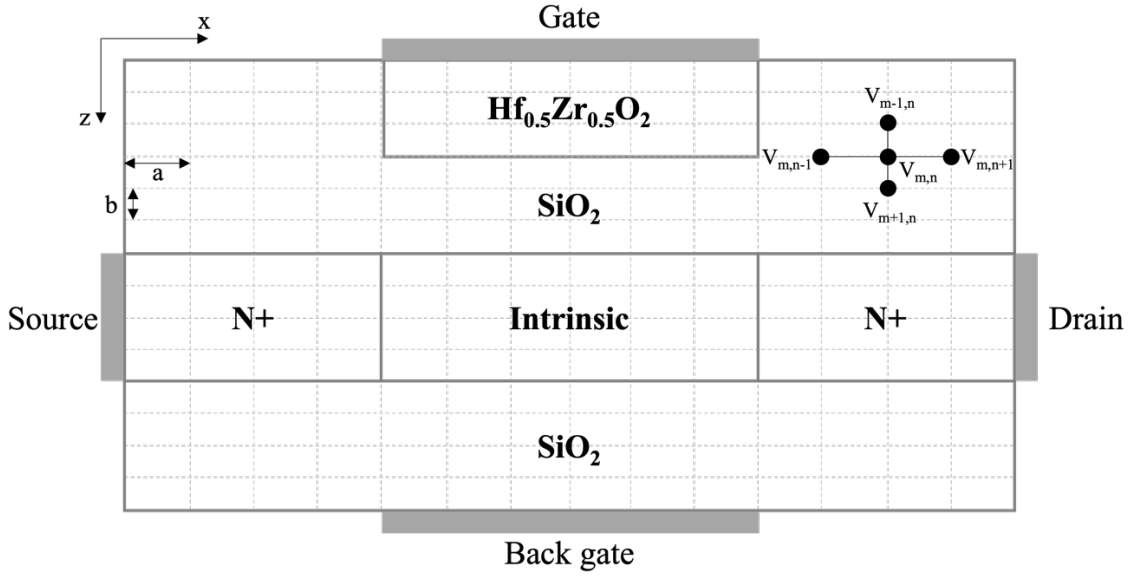


Fig. 2.6. A schematic of two-dimensional NCFET structure. The grid points are uniformly distributed along x and z direction with spacing of a and b, respectively. On the right-side, the potential at grid [m, n] and its adjacent potentials are labelled as $V_{\mathrm{m,n}}$ and $V_{\mathrm{m\pm1,n\pm1}}$ [59].

Before numerically calculating the Poisson's equation, various parameters have been defined as shown in **Fig. 2.6**. $V_{\mathrm{m,n}}$ represents a potential at grid point of (m, n) and $V_{\mathrm{m-1,n}}$, $V_{\mathrm{m,n-1}}$, $V_{\mathrm{m+1,n}}$, and $V_{\mathrm{m,n+1}}$ are adjacent potential values, respectively. To solve Poisson's equation numerically, we rewrite Eq. (8) to a discretized form:

$$\frac{\partial^2 V_{\mathrm{m,n}}}{\partial x^2} + \frac{\partial^2 V_{\mathrm{m,n}}}{\partial z^2} = -\frac{\rho_{\mathrm{m,n}}}{\varepsilon_0 \varepsilon_r}, \tag{9}$$

where $\rho_{\mathrm{m,n}}$ is a charge density at the grid point of (m, n). By using FDM, Eq. (9) becomes

$$\frac{V_{\mathrm{m,n+1}}+V_{\mathrm{m,n-1}}-2V_{\mathrm{m,n}}}{a^2}+\frac{V_{\mathrm{m+1,n}}+V_{\mathrm{m-1,n}}-2V_{\mathrm{m,n}}}{b^2}=-\frac{q(p-n+N_{\mathrm{D}}-N_{\mathrm{A}})_{\mathrm{m,n}}}{\varepsilon_0\varepsilon_{\mathrm{r}}}. \tag{10}$$

Note that a and b are the spacing of the mesh along x and z directions (see **Fig. 2.6**). Also, q is the elementary charge, n, p, N_{D}, and N_{A} are the concentration of electron, hole, donor, and acceptor, respectively. Therefore, the discretized Poisson's equation can be obtained by rearranging Eq. (10) as

$$\begin{aligned}\frac{a}{b}\varepsilon_{\mathrm{r}}V_{\mathrm{m-1,n}}+\frac{b}{a}\varepsilon_{\mathrm{r}}V_{\mathrm{m,n-1}}+\frac{a}{b}\varepsilon_{\mathrm{r}}V_{\mathrm{m+1,n}}+\frac{b}{a}\varepsilon_{\mathrm{r}}V_{\mathrm{m,n+1}}-2\left(\frac{a}{b}+\frac{b}{a}\right)\varepsilon_{\mathrm{r}}V_{\mathrm{m,n}}\\ =\frac{ab}{\varepsilon_0}q(p-n+N_{\mathrm{D}}-N_{\mathrm{A}})_{\mathrm{m,n}}.\end{aligned} \tag{11}$$

Next, let us consider the interface and boundary conditions in the discretized Poisson's equation. Since the dielectric constant of gate oxide ($\varepsilon_{\mathrm{OX}}$) and semiconductor ($\varepsilon_{\mathrm{SC}}$) are different, the discontinuity of dielectric constant should be considered. When the grid point is located within the semiconductor or gate oxide material, the ε_{r} depends on the corresponding material such as $\varepsilon_{\mathrm{OX}}$ or $\varepsilon_{\mathrm{SC}}$ in Eq. (11). However, at the interface between gate oxide and semiconductor, the equation is given by

$$\begin{aligned}\frac{a}{b}\varepsilon_{\mathrm{Top}}V_{\mathrm{m-1,n}}+\frac{b}{a}\left(\frac{\varepsilon_{\mathrm{Top}}+\varepsilon_{\mathrm{Bot}}}{2}\right)V_{\mathrm{m,n-1}}+\frac{a}{b}\varepsilon_{\mathrm{Bot}}V_{\mathrm{m+1,n}}+\frac{b}{a}\left(\frac{\varepsilon_{\mathrm{Top}}+\varepsilon_{\mathrm{Bot}}}{2}\right)V_{\mathrm{m,n+1}}\\ -2\left(\frac{a}{b}+\frac{b}{a}\right)\left(\frac{\varepsilon_{\mathrm{Top}}+\varepsilon_{\mathrm{Bot}}}{2}\right)V_{\mathrm{m,n}}=\frac{ab}{\varepsilon_0}q(p-n+N_{\mathrm{D}}-N_{\mathrm{A}})_{\mathrm{m,n}},\end{aligned} \tag{12}$$

in which $\varepsilon_{\mathrm{Top}}$ and $\varepsilon_{\mathrm{Bot}}$ represent material dielectric constants of the above and below the interface, respectively. Dirichlet boundary conditions have been chosen at the interface between an electrode and material, where $V_{\mathrm{m,n}} = V_{\mathrm{G}}$, V_{D}, and V_{S}. Neumann boundary conditions of $\boldsymbol{n}\cdot\nabla V=0$, where $\boldsymbol{n}$ denotes

the normal direction to the boundary are used for the rest of outer boundaries. To implement the boundary conditions into the discrete Poisson's equation, we have utilized the conditions as follows:

1) top and bottom edges (except for the gate electrode): $V_{\mathrm{m,n}} - V_{\mathrm{m}\pm1,\mathrm{n}} = 0$

2) left and right edges (except for the source/drain electrode): $V_{\mathrm{m,n}} - V_{\mathrm{m,n}\pm1} = 0$

3) left and right upper corner: $2V_{\mathrm{m,n}} - \left(V_{\mathrm{m+1,n}} - V_{\mathrm{m,n}\pm1}\right) = 0$

4) left and right lower corner: $2V_{\mathrm{m,n}} - \left(V_{\mathrm{m-1,n}} - V_{\mathrm{m,n}\pm1}\right) = 0$

2.2.2 Electrostatics in FE

Once the FE is considered, the Poisson's equation in Eq. (7) can be extended as

$$\nabla \cdot D = \nabla \cdot \left(\varepsilon_0 \varepsilon_{\mathrm{FE}} E + P_{\mathrm{Sp}}\right) = 0, \tag{13}$$

where P_{Sp} is a spontaneous polarization induced by the ferroelectricity and ρ becomes zero due to no free charge in FE like DE. As a consequence, Eq. (13) can be rewritten as

$$\nabla \cdot (\varepsilon_0 \varepsilon_{\mathrm{FE}} E) + \nabla \cdot \left(P_{\mathrm{Sp}}\right) = -\varepsilon_0 \varepsilon_{\mathrm{r}} \nabla^2 \cdot V + \nabla \cdot \left(P_{\mathrm{Sp}}\right) = 0. \tag{14}$$

Fig. 2.7(a) shows the one-dimensional grid points for a FE-DE bilayer to observe the effect of P_{Sp} on the potential. In FE, Eq. (14) of extended Poisson's equation is calculated to evaluate the potential given polarization value at a certain grid point, whereas no ferroelectricity exists in DE, leading to the original Poisson's equation with $P_{\mathrm{Sp}} = 0$ in Eq. (14).

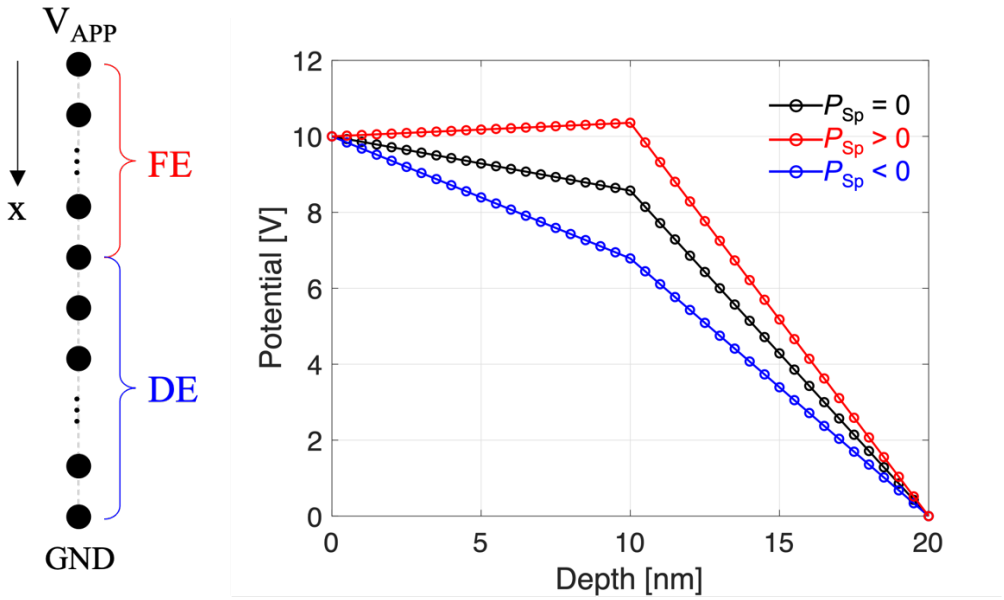


Fig. 2.7. (a) A schematic of one-dimensional FE-DE bilayer structure with uniform spacing. (b) Potential curve along with x direction.

The potential vs. position curves are shown in **Fig. 2.7(b)**. For this test, both of FE and DE thickness are 10 nm and those permittivities ($\varepsilon_{\mathrm{FE}} = 24$ and $\varepsilon_{\mathrm{DE}} = 4$) are chosen. Note that the grid spacing is 0.5 nm. The black line can be evaluated under the applied voltage (V_{APP}) of 10 V without considering P_{Sp}. This result is the same as the result of a capacitor with bilayer dielectrics having aforementioned dielectric constants. However, once P_{Sp} is considered, we can observe either red or blue line depending on the sign of P_{Sp}. When P_{Sp} is negative, the electric field induced by the P_{Sp} in FE (called depolarization field) strengthens the electric field from the applied voltage, which can result in increasing the effective electric field across the FE, since the direction of depolarization field is identical to that of applied field. As a result, more voltage drop through the FE can be observed. In contrast, when P_{Sp} is a positive value, the applied field and depolarization field are in the opposite direction. Therefore, the effective field across the FE could be weaker than the applied field or even could be opposite to the applied field, resulting in obtaining less voltage drop or voltage amplification. Details will be discussed later in this dissertation (chapter 4).

2.3 Two-dimensional Materials: Black Phosphorus (BP)

2.3.1 Density Functional Theory

Density functional theory (DFT) is a widely used computational modeling method to investigate electronic properties of the many-body system. The equation for DFT is derived from the many-body time-independent Schrödinger equation given by

$$\widehat{H}\Psi(r_1, \dots, r_N) = \left[\sum_{i=1}^{N}\left(-\frac{\hbar^2}{2m_i}\nabla_i^2\right) + \sum_{i=1}^{N} V(r_i) + \sum_{i<j}^{N} U(r_i, r_j)\right]\Psi(r_1, \dots, r_N)$$

$$= \mathrm{E}\Psi(r_1, \dots, r_N), \tag{15}$$

where, for the N-electron system, H is the Hamiltonian, which can describe the electronic properties of the material used, E is the total energy, V is the potential energy from the external field, and U is the electron-electron interactions energy. However, the problem of using this method is to require huge computational resources, which makes it virtually impossible to solve them for the complex system containing many atoms. For the practical device simulations, we need a more effective approach to calculate the material properties such as a tight-binding approximation.

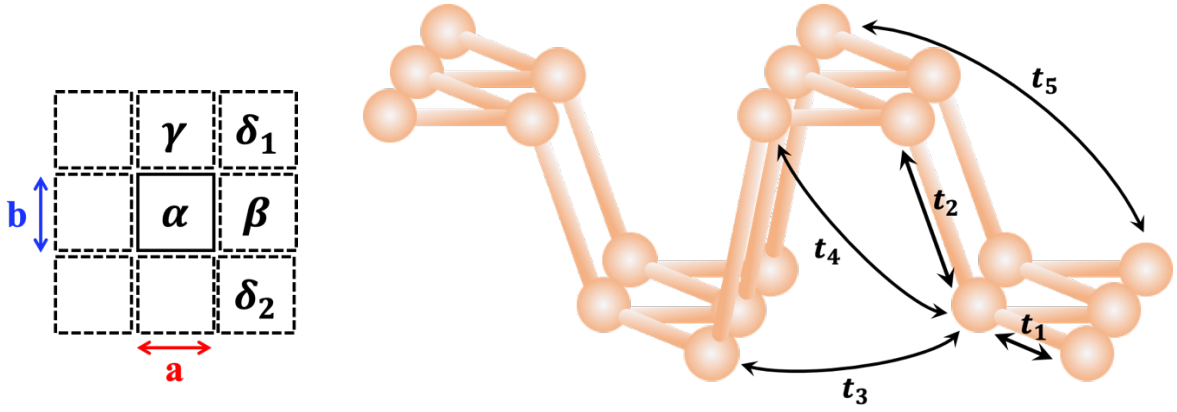
2.3.2 Tight-binding (TB) Approximation

A tight-binding method is an approximate approach to calculate the electronic band structure based on the superposition of wave functions for the isolated atoms. The matrix form of Hamiltonian for monolayer BP including the interaction between cells can be written as

$$\boldsymbol{H} = \boldsymbol{\alpha} + \boldsymbol{\beta}e^{i\vec{k}\cdot(a,0)} + \boldsymbol{\gamma}e^{i\vec{k}\cdot(0,b)} + \boldsymbol{\delta_1}e^{i\vec{k}\cdot(a,b)} + \boldsymbol{\delta_2}e^{i\vec{k}\cdot(a,-b)}$$

$$\left[\boldsymbol{\beta}e^{i\vec{k}\cdot(a,0)} + \boldsymbol{\gamma}e^{i\vec{k}\cdot(0,b)} + \boldsymbol{\delta_1}e^{i\vec{k}\cdot(a,b)} + \boldsymbol{\delta_2}e^{i\vec{k}\cdot(a,-b)}\right]^{\dagger}, \tag{16}$$

where from $\boldsymbol{\alpha}$ to $\boldsymbol{\delta_2}$ are the centered unit cell (4 × 4 matrix) and its nearest neighbor cells as shown in **Fig. 2.8(a)**. Note that a and b are 4.43 Å and 3.27 Å, respectively.



(a) (b)

Fig. 2.8. (a) The matrix form of Hamiltonian for monolayer BP with adjacent unit cells and (b) inlayer hopping parameters for monolayer TB model.

In order to utilize the TB method for the monolayer BP, the TB parameters of BP are obtained from GW approximation [60] as listed in **Table 1**, which is described by five in layer hopping parameters of t_i (i = 1, 2, …, 5) between sites (see **Fig. 2.10(b)**). By considering the interactions of each site, the Hamiltonian matrix of the interaction between the unit cell and its neighbor cells are given as follows.

$$\boldsymbol{\alpha} = \begin{bmatrix} 0 & t_1 & t_4 & t_5 \\ t_1 & 0 & t_2 & t_4 \\ t_4 & t_2 & 0 & t_1 \\ t_5 & t_4 & t_1 & 0 \end{bmatrix} \quad \boldsymbol{\beta} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ t_3 & 0 & 0 & 0 \\ t_4 & t_5 & 0 & 0 \\ t_2 & t_4 & t_3 & 0 \end{bmatrix} \quad \boldsymbol{\gamma} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ t_1 & 0 & 0 & t_4 \\ t_4 & 0 & 0 & t_1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\boldsymbol{\delta_1} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ t_3 & 0 & 0 & 0 \\ t_4 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad \boldsymbol{\delta_2} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & t_4 & t_3 & 0 \end{bmatrix}$$

	Inlayer	
No.	t (eV)	d (Å)
1	-1.220	2.22
2	3.665	2.24
3	-0.205	3.34
4	-0.105	3.47
5	-0.055	4.23

Table 1. Inlayer hopping parameters (t) of monolayer BP obtained in terms of TB from [60]. The distance between interacting lattice sites shown in Fig. 2. 10(b) is denoted by d.

Fig 2.9 shows band structures from original GW bands in comparison with the calculation by using the TB parameters. Although energy dispersions from the TB method are incomparable with the original GW bands along most of the high symmetry points, it is well-matched at the gamma point where the conduction band minimum and valence band maximum occur, which results in good accuracy for large-scale device simulations.

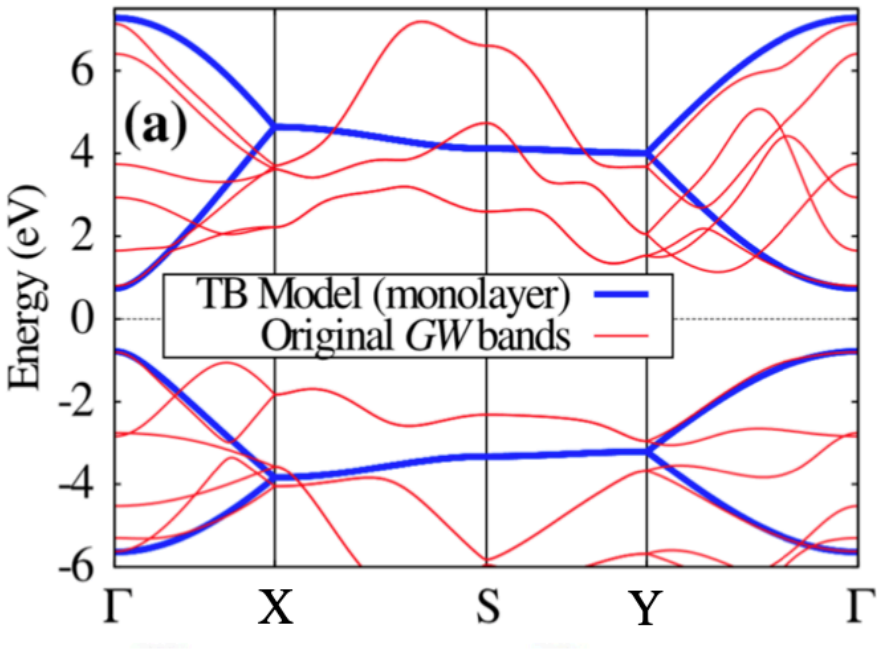


Fig. 2.9. Calculated band structures using the TB parameters (blue) compared to the original GW bands (red) for a monolayer BP [60].

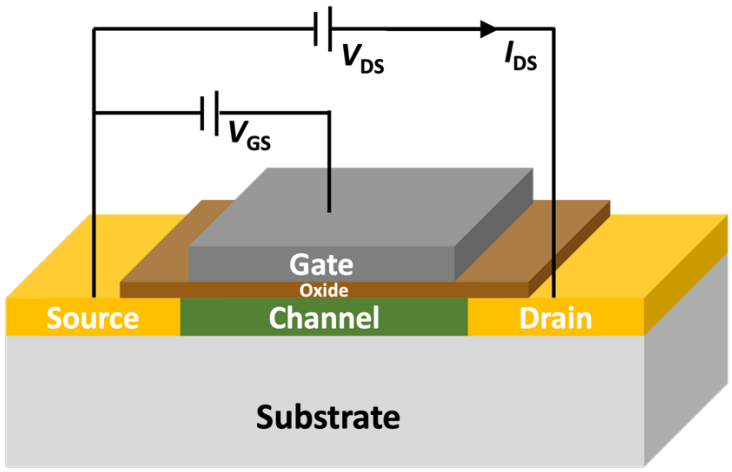


Fig. 2.10. A schematic of nanotransistor under the non-equilibrium bias.

2.4 Quantum Transport: Non-equilibrium Green's Function

For nano-scale devices, the non-equilibrium Green's function (NEGF) formalism provides a powerful computational framework to accurately predict and explore quantum transport of carriers [61]. In this chapter, the NEGF is introduced using generalized forms of Green's functions under the non-equilibrium bias in a nanotransistor. **Fig. 2.10** shows the basic structure of the nanotransistor. The channel is connected to the source and drain with distinct Fermi-Dirac distribution function, $f_{\mathrm{S}}(\mathrm{E})$ and $f_{\mathrm{D}}(\mathrm{E})$:

$$f_{\mathrm{S/D}}(E) = \frac{1}{exp[(E-\mu_{\mathrm{S/D}})/k_{\mathrm{B}}T]+1} \tag{17}$$

To evaluate transfer characteristics of the nanotransistor, we calculate the Green's function [61] at a given energy as

$$G(\mathrm{E}) = [(\mathrm{E} + i0^{+})\mathrm{I} - H - \Sigma_{\mathrm{S}} - \Sigma_{\mathrm{D}}]^{-1} \tag{18}$$

, where E, I, and 0^{+} are energy, the identity matrix, and infinitesimal positive value, respectively. H is the Hamiltonian obtained from TB approximation as explained in the previous chapter. Self-energy matrices are used to describe the coupling between the channel and source/drain contact denoted by Σ_{S} and Σ_{D}. Under the non-equilibrium bias condition of the channel region, the current flows and it is determined by differences between electrochemical potential at source and drain (μ_{S} and μ_{D}), resulting in gaining the relation of $qV_{\mathrm{DS}} = \mu_{\mathrm{S}} - \mu_{\mathrm{D}}$. Next, the matrix of electron density can be written as

$$[\rho] = \int_{-\infty}^{+\infty} \frac{1}{2\pi} [G^{n}(\mathrm{E})] d\mathrm{E}, \tag{19}$$

where $G^{n}(\mathrm{E})$ is the electron correlation function. It means the matrix form of the electron density per unit energy, and it can be given by (with dropping the argument E for clarity)

$$[G^{n}] = [A_{\mathrm{S}}] f_{\mathrm{S}} + [A_{\mathrm{D}}] f_{\mathrm{D}}. \tag{20}$$

Note that $[A_{\mathrm{S/D}}] = G\Gamma_{\mathrm{S/D}}G^{\dagger}$, where $[A_{\mathrm{S/D}}]$ is a fraction of the spectral function for source/drain, which represents the matrix version of the density of states per unit energy, so that the total spectral function is achieved by adding up two fractions of the spectral functions: $[A] \equiv i[G - G^{\dagger}] = [A_{\mathrm{S}}] + [A_{\mathrm{D}}]$. Also, $\Gamma_{\mathrm{S/D}}$ is broadening matrices, which equals to $i\left(\Sigma_{\mathrm{S/D}} - \Sigma_{\mathrm{S/D}}^{\dagger}\right)$. Subsequently, the current at the terminal can be written in the form as

$$I_{S/D} = -(q/h)\int_{-\infty}^{+\infty} \tilde{I}_{S/D}\, dE \tag{21}$$

with

$$\tilde{I}_{S/D} = Trace\left[\Gamma_{S/D}A\right]f_{S/D} - Trace\left[\Gamma_{S/D}G^{n}\right], \tag{22}$$

where h is Planck's constant. In the simulations for the nanoelectronics, NEGF provides the charge density, ρ to the Poisson's equation to calculate an updated potential in Poisson's equation. Details of self-consistent simulation will be discussed in 2.5.

2.5 Self-consistent Simulation

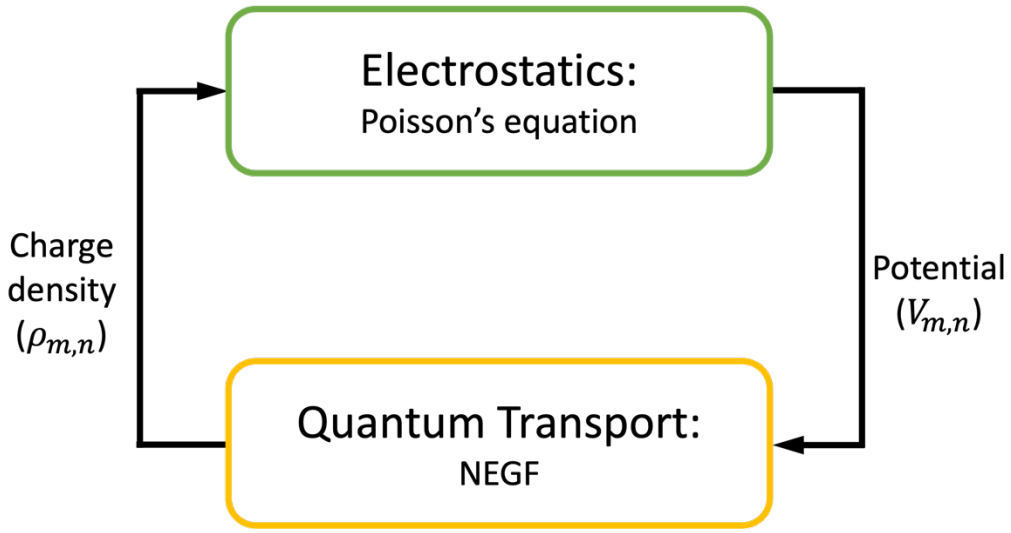


Fig. 2.11. Schematic of self-consistent simulation process between electrostatics and quantum transport.

Fig. 2. 11 shows the self-consistent simulation process between Poisson's equation and NEGF. Note that FE module can be included depending on the structure simulated. Parameters (potential and charge density) calculated in each module are iteratively exchanged throughout the self-consistent simulation. After calculating the Poisson's equation with the initial guess of a charge density, the potential at a certain position (for example, $V_{m,n}$) is given for the input of next NEGF calculation. By employing the

given potential, charge density (i.e., $\rho_{\mathrm{m,n}}$) can be estimated using the NEGF process, which can be an updated input for the next calculation of Poisson's equation. Here, Poisson's equation provides another potential value along with the updated charge density, denoted by $V_{\mathrm{m,n}}^{NEW}$. Note that the previous potential can be $V_{\mathrm{m,n}}^{OLD}$. This self-consistent simulation (see **Fig. 2. 11**) continues until an error of $\left|V_{\mathrm{m,n}}^{NEW} - V_{\mathrm{m,n}}^{OLD}\right|$ becomes converged to small enough value (e.g., 1 mV).

Chapter 3
Modeling of Hysteretic Jump Points in Ferroelectric MOS Capacitors

3.1 Introduction

Ever-increasing power density issue in the nanoscale complementary metal–oxide–semiconductor (CMOS) technology has been in existence for over a decade. It originates from the inherent attribute of "thermally activated" conventional MOS field-effect transistors (FETs), resulting in inevitable constraint on OFF-state current, threshold voltage, and power supply voltage (V_{DD}) scaling. To overcome this, various steep-switching devices have been proposed [12], [62], [63]. Unlike others, negative capacitance (NC) devices based on ferroelectric (FE) materials do not introduce any new device physics but give a new life to the CMOS technology by integrating an FE layer with the conventional MOSFET [14], [15]. The underlying concept is to amplify the gate voltage using the NC effect of the FE layer, leading to small subthreshold swing below the classical limit of 60 mV/dec at room temperature, large ON-state current, and low-power operation [12]. Since the idea was conceptualized in 2008, various NC devices have been proposed for next-generation electronics [14], [64], [65].

In order to properly design both logic and memory devices, understanding the exact hysteresis behavior of NC device is critical. For low-power logic devices, suppressing hysteresis while keeping steep-switching characteristics is important; in contrast, knowing the exact hysteresis window is the key for memory devices to capitalize on it. Thus, it is equally crucial for both applications to describe hysteresis based on material and device parameters used. Recently, NC has been studied to integrate an FE layer with various functional devices [66]–[75]. In particular, hysteresis behaviors in different devices are investigated based on transfer characteristics, both experimentally and theoretically [76]–[79]. Although the hysteresis behavior is based on the energy landscape, the trend of hysteresis and capacitance matching have been studied previously [72], [73], [78]–[80] and models describing the direct relation between device design parameters and hysteresis response are currently missing from the field.

In this paper, we model hysteretic jump point (HJP) of an FE-MOS capacitor—the basic structure that needs to be understood first before investigating more complicated FET— using three key design

parameters of FE layer thickness (T_{FE}), gate dielectric thickness (EOT), and semiconductor doping concentration (N_{SC}). First, we explore how the hysteresis varies with T_{FE}, EOT, and N_{SC} by investigating the energy landscape of the FE-MOS capacitor, considering semiconductor, gate dielectric, and battery, as well as the FE layer to capture the nonlinear nature of the total capacitance. HJP, the point at which the surface potential changes abruptly, is identified while sweeping the gate voltage by tracking the charges that make the system stable for a given device structure. After that, a detailed relation between the HJP and the device parameters is described with our model by carefully investigating the response of HJP to the variation of T_{FE}, EOT, and N_{SC}. Our model not only provides useful insight into the FE-MOS capacitors but also makes it possible to directly investigate hysteresis, thereby enabling the engineering of hysteresis through various design parameters for different target applications.

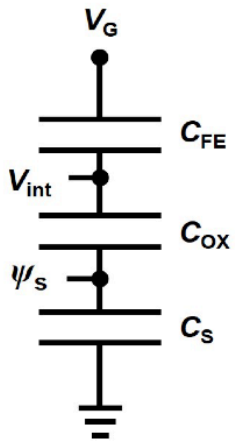


Fig. 3.1. Equivalent capacitor circuit model for FE-MOS capacitor. C_{FE}, C_{OX}, and C_S represent the capacitance of FE layer, gate oxide, and semiconductor (*i.e.*, silicon), respectively. For the nominal device, the following parameters are used: T_{FE} = 350 nm, N_{SC} = 10^{16} cm^{-3}, and EOT = 1 nm. V_G, V_{int} and ψ_s are gate voltage, internal voltage, and surface potential, respectively.

3.2 Hysteresis Analysis

Fig. 3.1 illustrates an equivalent capacitor circuit model for FE-MOS capacitor. Here we use $Pb[Zr_{0.48}Ti_{0.52}]O_3$ (PZT) [81] for the FE layer of the nominal device, but the method presented in this study can be extended to other FE materials. Single domain is assumed for the FE material, and we do not consider depolarization field and leakage through FE. It is worth mentioning that, due to these assumptions, metal–FE– dielectric–semiconductor structure can be treated the same as the one considered in this work.

In this paper, we use MATLAB for numerical simulations, as commercial tools are still very limited for the simulation of NC devices. First, the total Gibbs free energy (G_{TOTAL}) of the entire system is calculated by considering the energies of the FE layer (U_{FE}), gate dielectric (U_{OX}), semiconductor (U_{SC}), and battery (U_{B}) as [82]

$$G_{\mathrm{TOTAL}} = \alpha T_{\mathrm{FE}} Q^2 + \beta T_{\mathrm{FE}} Q^4 + \gamma T_{\mathrm{FE}} Q^6 + \frac{Q^2}{2C_{\mathrm{OX}}} + \int_0^Q \psi_{\mathrm{S}}(Q')dQ' - QV_{\mathrm{G}} \tag{1}$$

where α, β, and γ are -5.2×10^7 $\mathrm{mF^{-1}}$, 5.8×10^7 $\mathrm{m^5F^{-1}C^{-2}}$, and 1.5×10^8 $\mathrm{m^9F^{-1}C^{-4}}$, respectively, for PZT [81]. It should be noted that this Gibbs free energy method can be used to calibrate Landau parameters against experiments [83]. The charge Q must be matched at each node to integrate FE, gate dielectric, and semiconductor in the FE-MOS capacitor. For the semiconductor, the following nonlinear relation between the surface potential (ψ_{S}) and charge is used, assuming zero flat band voltage [84]:

$$Q = \sqrt{2\varepsilon_{\mathrm{Si}} k_{\mathrm{B}} T N_{\mathrm{SC}}} \left[\left(e^{-q\psi_{\mathrm{S}}/k_{\mathrm{B}}T} + \frac{q\psi_{\mathrm{S}}}{k_{\mathrm{B}}T} - 1 \right) + \frac{{n_{\mathrm{i}}}^2}{{N_{\mathrm{SC}}}^2} \left(e^{q\psi_{\mathrm{S}}/k_{\mathrm{B}}T} - \frac{q\psi_{\mathrm{S}}}{k_{\mathrm{B}}T} - 1 \right) \right]^{1/2} \tag{2}$$

where $\varepsilon_{\mathrm{Si}}$ is the silicon permittivity, k_{B} is Boltzmann's constant, T is the temperature, q is the elementary charge, and n_{i} is the intrinsic carrier concentration of silicon. **Fig. 3.2(a)** shows the energy landscape of the FE-MOS capacitor at the gate voltage of 0.8 V. There are two energy minima, representing bistable states [the zoomed plot of each point is shown in **Fig. 3.2(b)** and **(c)**, respectively].

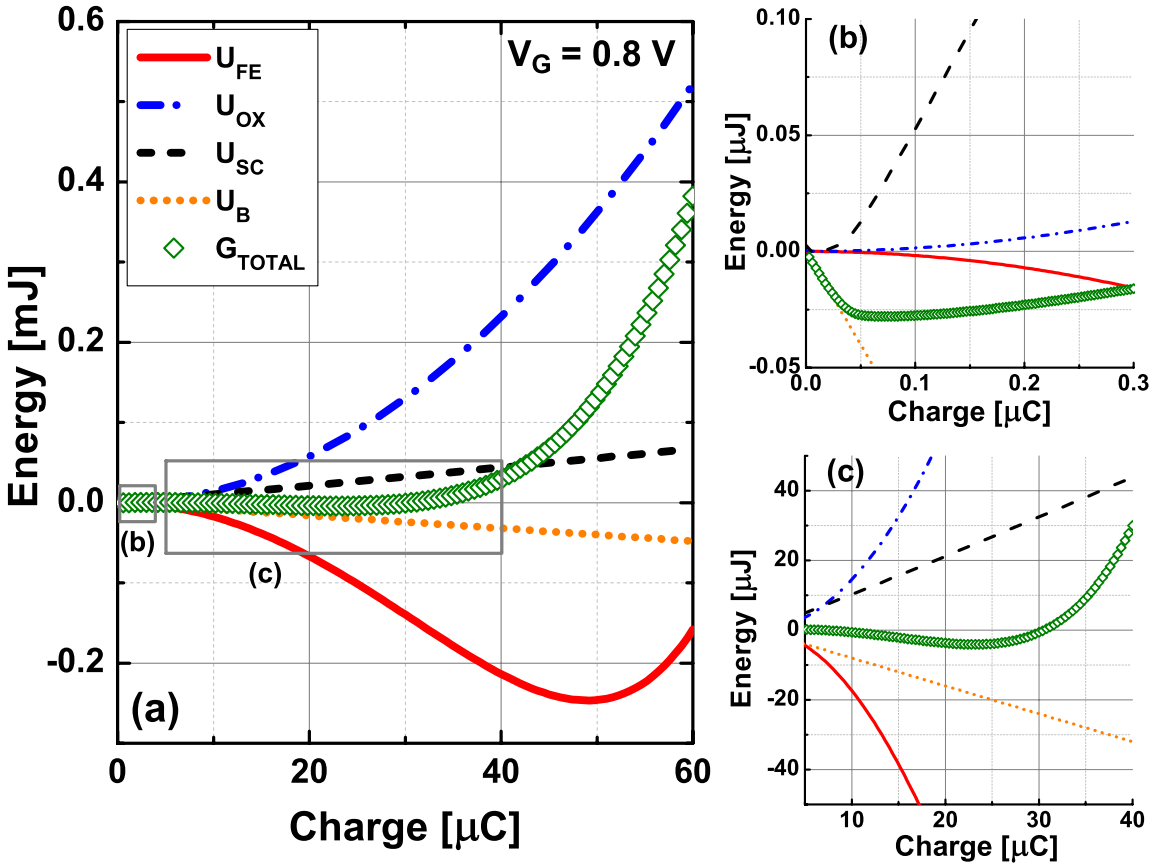


Fig. 3.2. (a) Total Gibbs free energy (G_{TOTAL}) as a function of charge for the FE-MOS capacitor (diamond symbol) at V_{G} = 0.8 V. The energies of FE layer (U_{FE}), gate dielectric (U_{OX}), semiconductor (U_{SC}) and battery (U_{B}) are also shown. The zoomed plots for two local energy minima are shown in (b) and (c).

This indicates that the charge can have different values based on the previous state of the system: 0.072 μC/cm^2 for the forward sweep of gate voltage and 23 μC/cm^2 for the backward sweep. It is noteworthy that we can also find a local maximum (Q = 3.9 μC/cm^2), representing an unstable state of NC. We have used $\partial G_{\mathrm{TOTAL}}/\partial Q = 0$ with $\partial^2 G_{\mathrm{TOTAL}}/\partial Q^2 > 0$ and $\partial G_{\mathrm{TOTAL}}/\partial Q = 0$ with $\partial^2 G_{\mathrm{TOTAL}}/\partial Q^2 < 0$ for the local minima and the local maximum, respectively. In contrast, if an applied voltage is out of the hysteresis region (i.e., $V_{\mathrm{G}} < 0.45$ V or > 0.9 V with the given device structure), only one local minimum can be observed.

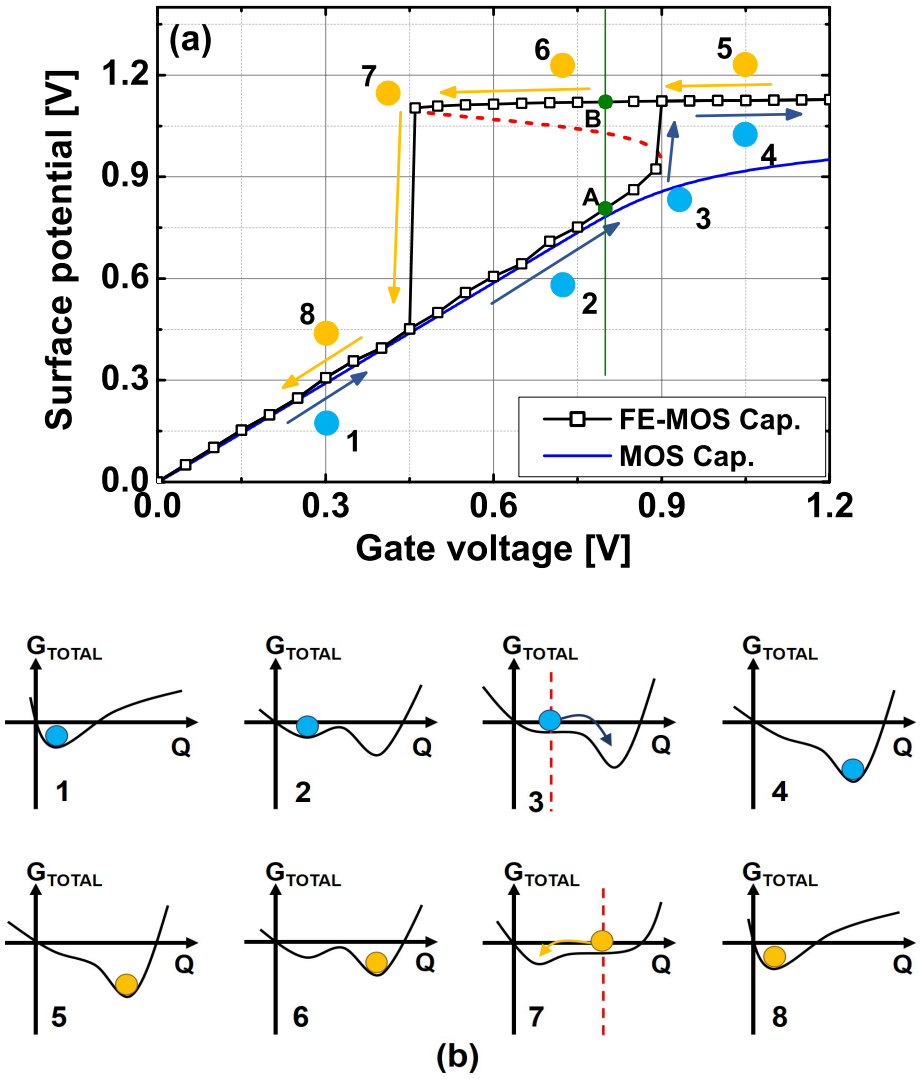


Fig. 3.3. (a) Surface potential (ψ_s) vs. gate voltage (V_G) for the FE-MOS capacitor (symbols) and the reference MOS capacitor (solid line). (b) Energy landscape (lines) and charge (circles) of the FE-MOS capacitor for the points 1-8 shown in (a).

Once the charge making the entire system stable is achieved, the corresponding surface potential is numerically obtained using (2). For example, at V_G = 0.8 V, the corresponding surface potentials for the two stable states with 0.072 and 23 μC/cm^2 are 0.81 and 1.12 V, respectively [A and B in **Fig. 3.3(a)**]. Similarly, by sweeping the gate voltage between 0 and 1.2 V, the surface potential at different gate voltages can be obtained as plotted in **Fig. 3.3(a)** with symbols. The $\psi_S - V_G$ plot for a regular MOS capacitor is also shown in **Fig. 3.3(a)** as a reference. In order to illustrate the hysteresis behavior of the FE-MOS capacitor, we have plotted the energy landscape of the device in **Fig. 3.3(b)** for the eight different points shown in **Fig. 3.3(a)**. In **Fig. 3.3(b)**, the circles represent the charge in the stable state at each point, which is determined by a given gate voltage along with the previous state of the device. The variation of the charge for the forward (points $1-4$) and backward (points $5-8$) V_G sweep can be explained as follows.

1) *At Small Gate Voltages (Point 1)*: There is only one minimum in the energy landscape, and the charge remains small, resulting in small surface potential. The minimum energy state is mainly determined by the MOS capacitor as the contribution of the FE layer ($U_{FE} = \alpha T_{FE} Q^2 + \beta T_{FE} Q^4 + \gamma T_{FE} Q^6$) is negligible, and therefore, the surface potential of the FE-MOS capacitor is almost the same as that of the MOS capacitor

2) *In the Moderate V_G Region (Point 2)*: If the gate voltage is gradually increased from points 1 to 2, another local minimum is developed and there exist two local minima. However, the charge still remains at the lower value due to the potential barrier between the two. The dominant state is still determined by the MOS capacitor rather than the FE layer [as it can be seen in **Fig. 3.2(b)**], and the surface potential of the FE-MOS capacitor is mainly determined by that of the MOS capacitor, as was the case for the point 1. The red dashed line in **Fig. 3.3(a)** is plotted for the local maximum of energy.

3) *At a Hysteretic Jump Point (Point 3)*: If the gate voltage is further increased, the satellite valley is developed more but the original valley diminishes, resulting in only a single minimum energy state available with an increased charge value. This is an HJP where the amplification of the surface potential can be observed.

4) *At High Gate Voltages (Point 4)*: Beyond the HJP, there exists only one energy minimum with an enhanced charge and potential. Unlike points 1 and 2, here the FE layer largely contributes to G_{TOTAL} along with the MOS capacitor, and therefore, the surface potential of the FE-MOS capacitor exhibits significant amplification as compared to the reference ψ_{S} of the MOS capacitor.

5) *For the Backward V_{G} Sweep (Points 5–8)*: The $\psi_{\mathrm{S}} - V_{\mathrm{G}}$ curve for the backward sweep can also be understood in a similar manner as the forward sweep case. Point 5 is identical to the point 4. As the gate voltage is gradually reduced, point 6 can be reached, which is equivalent to point 2. However, unlike the forward sweep case, the charge remains large due to the barrier between the two local minima, thereby maintaining the enhanced surface potential. Point 7 is the HJP for the backward V_{G} sweep, where the charge and the potential drop significantly. Point 8 is identical to the point 1.

Based on the above observation, we focus on two HJPs at points 3 and 7; we call the former the lower HJP (HJP-low) and the later the upper HJP (HJP-up). Both HJPs satisfy $(\partial G_{\mathrm{TOTAL}}/\partial Q) = (\partial^2 G_{\mathrm{TOTAL}}/\partial Q^2) = 0$ and the corresponding points are shown by the red dashed line for the points 3 and 7 in **Fig. 3.3(b)**. It is worth mentioning that our model is developed for steady-state conditions as it can be seen from $(\partial G_{\mathrm{TOTAL}}/\partial Q) = -\rho(\partial Q/\partial t) = 0$, where t is the time and ρ is the viscosity coefficient. Using those HJPs, we can obtain two important pieces of information: hysteresis width and hysteresis height. The former is the difference of gate voltages at HJP-up and HJP-low, and it quantifies the extent of hysteresis. If hysteresis width is zero, it means there is no hysteresis. On the other hand, hysteresis height is the difference of the surface potential of the two HJPs, which is proportional to the potential amplification. For low-power logic devices, large hysteresis height with narrow hysteresis width will be preferred. However, the preferred requirement for the hysteresis window could be altered for different target applications.

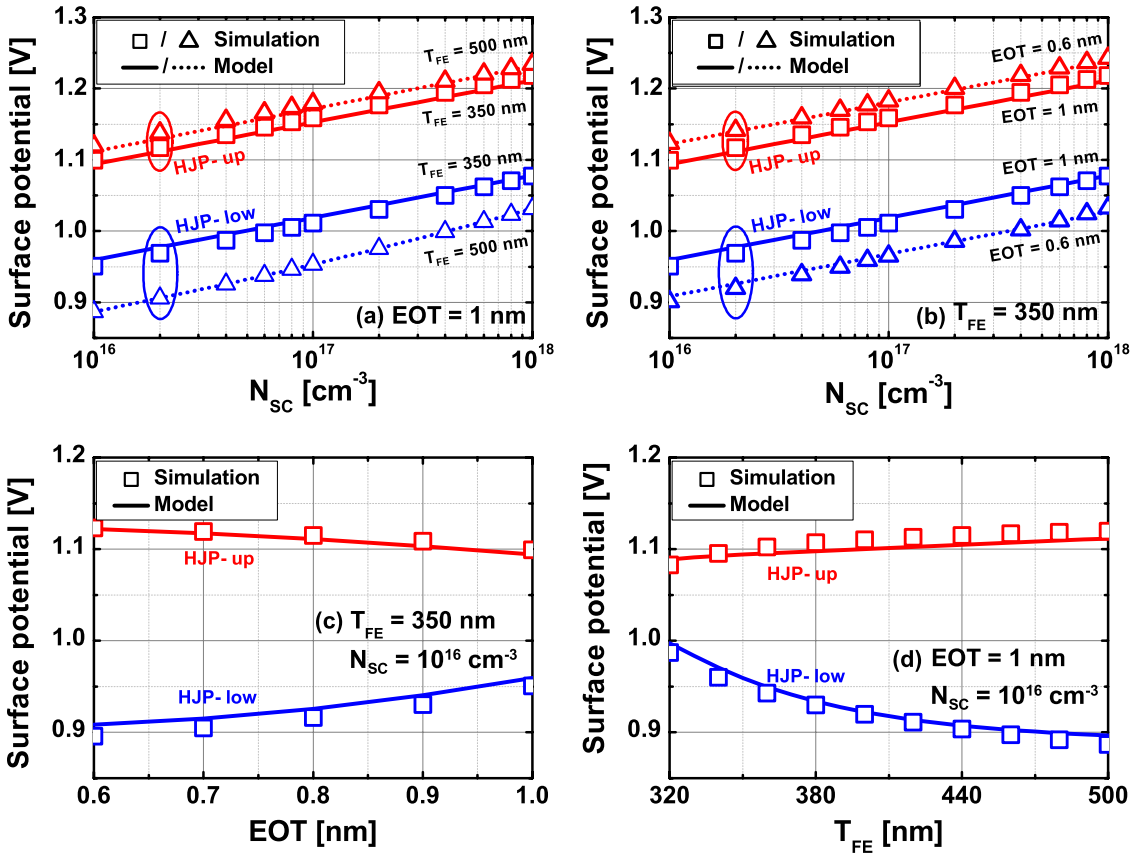


Fig. 3.4. The surface potential at the HJPs as a function of N_{SC} (a) with T_{FE} of 350 nm and 500 nm (at EOT = 1 nm) and (b) with EOT of 0.6 nm and 1 nm (at T_{FE} = 350 nm). The surface potential at the HJPs as a function of (c) EOT (at fixed N_{SC} and T_{FE}) and (d) T_{FE} (at fixed N_{SC} and EOT).

3.3 Modeling of Hysteretic Jump Points

Although the $\psi_S - V_G$ plot and the hysteresis window are fixed for a given set of parameters as demonstrated in **Fig. 3.3**, each HJP can be tuned with material and device parameters. **Fig. 3.4** shows the variation of the surface potential for each HJP (red symbols for HJP-up; blue symbols for HJP-low) with different parameters. In **Fig. 3.4(a)**, N_{SC} is varied from 10^{16} to 10^{18} cm^{-3} with T_{FE} of 350 and 500 nm at a fixed EOT = 1 nm. In **Fig. 3.4(b)**, N_{SC} is varied within the same range with EOT of 0.6 and 1 nm at a fixed T_{FE} = 350 nm. **Fig. 3.4(c)** and **(d)** shows ψ_S of each HJP as a function of EOT and T_{FE}, respectively. Our simulation results show that the surface potential at the HJPs can be modified by tuning parameters, and the response of HJPs to the variation of T_{FE}, EOT, and N_{SC} is used for modeling of the HJPs in the following.

We model the HJPs by carefully investigating our physics-based simulation data in **Fig. 3.4** since the direct measurement of the surface potential is practically impossible. It can be observed in **Fig. 3.4(a)** and **(b)** that the surface potential of HJP is a logarithmic function of N_{SC}. The slope is more sensitive to T_{FE} than to EOT although the difference is insignificant. On the other hand, the y-intercept is largely affected by T_{FE} and EOT. Hence, the basic form of the model can be given by

$$\psi_{S,HJP} = f_1(T_{FE}) \cdot \left\{ log_{10}\left(\frac{N_{SC}}{n_0}\right)\right\} + f_2(T_{FE}, \text{EOT}), \tag{3}$$

in which

$$f_1(T_{FE}) = A'\{(T_{FE} - T_0)/l_0\}^{B'} + C' \tag{4}$$

where T_0 is the reference thickness of FE to observe hysteresis, which has been obtained with EOT = 1 nm and N_{SC} = 10^{16} cm^{-3} in our simulation. Also, n_0 and l_0 are 1 cm^{-3} and 1 nm, respectively. Finally, by varying EOT with fixed N_{SC} and T_{FE}, f_2 can be determined as

$$\begin{aligned} f_2(T_{FE}, EOT) = {} & \{D'[(EOT - EOT_{MIN})/l_0]^2 + E'\}e^{F' \cdot T_{FE}} + \\ & \{G'[(EOT - EOT_{MAX})/l_0]^2 + H'\}e^{I' \cdot T_{FE}}, \end{aligned} \tag{5}$$

where EOT_{MIN} and EOT_{MAX} are the lower and upper limit of EOT. In this work, EOT_{MIN} = 0.6 nm and EOT_{MAX} = 1.0 nm are used. The upper limit of 1.0 nm is taken considering the first high-k/metal gate 45-nm technology [3], whereas different values can be chosen for the lower limit as technology matures. Note that the Eq. (3) is constructed by careful analysis of physics-based simulation results. In comparison, Eqs. (4) and (5) are written empirically. f_1 represents how sensitive the surface potential is with respective to the change in doping concentration, which is a function of T_{FE}. On the other hand, f_2 sets a reference point for $\psi_{S,\mathrm{HJP}}$, which is a function of both T_{FE} and EOT. $A' - I'$ in Eqs. (4) and (5) are fitting parameters, which depends on the ferroelectric material used (the values are given in Table 2). Both HJP-up and HJP-low can be described by the same Eqs. (3) - (5) using different sets of parameters (Table 2). Notably, our model (lines) reproduces the simulation results (symbols) accurately as shown in **Fig. 3.4**. Moreover, our model can also be used for FE-MOS capacitors based on different FE. The model has also been tested and confirmed with $BaTiO_3$ (BTO) (α = -3.3 × 10^7 mF^{-1}, β = -6.3 × 10^8 $m^5F^{-1}C^{-2}$, γ = 4.3 × 10^9 $m^9F^{-1}C^{-4}$) [81] and hafnium zirconium oxide (HZO) (α = -3.3 × 10^7 mF^{-1}, β = -6.3 × 10^8 $m^5F^{-1}C^{-2}$, γ = 4.3 × 10^9 $m^9F^{-1}C^{-4}$) which can have thin FE thickness [85]. The parameters used for BTO and HZO are also shown in Table 2.

Using Eq. (3), the hysteresis height can be determined as $\psi_{S,\mathrm{HJP-up}} - \psi_{S,\mathrm{HJP-low}}$. On the other hand, the hysteresis width can be calculated by $V_{G,\mathrm{HJP-low}} - V_{G,\mathrm{HJP-up}}$, where the gate voltage for HJP-low and HJP-up can be obtained by considering the voltage drop through each capacitor $\left(V_G = V_{FE}(\psi_s) + \frac{Q(\psi_s)}{C_{OX}} + \psi_s\right)$ and $V_{FE} = 2\alpha T_{FE} Q + 4\beta T_{FE} Q^3 + 6\gamma T_{FE} Q^5$ along with Eqs. (2) and (3) at the HJPs.

	PZT		BTO		HZO	
	HJP-up	HJP-low	HJP-up	HJP-low	HJP-up	HJP-low
A' [V]	3.7×10^{-4}	3.7×10^{-4}	5×10^{-4}	5×10^{-4}	0.01	1.8×10^{-3}
B'	0.4	0.4	0.4	0.4	0.4	0.4
C' [V]	0.057	0.057	0.06	0.06	0.06	0.055
D' [V]	-124	50	-0.136	0.598	0.718	-0.097
E' [V]	28	7.7	0.312	0.575	1.28	0.12
F' [nm^{-1}]	-0.02	-0.015	-5×10^{-3}	-0.01	-0.4	-0.08
G' [V]	0.04	-0.04	-0.82×10^{-3}	-0.02	-0.089	-0.011
H' [V]	0.143	-0.05	1.74×10^{-3}	2×10^{-4}	-0.35	2.7×10^{-3}
I' [nm^{-1}]	10^{-4}	0.01	0.01	0.01	0.03	0.08
T_0 [nm]	310		165		4	

Table 2. Parameters used in this study

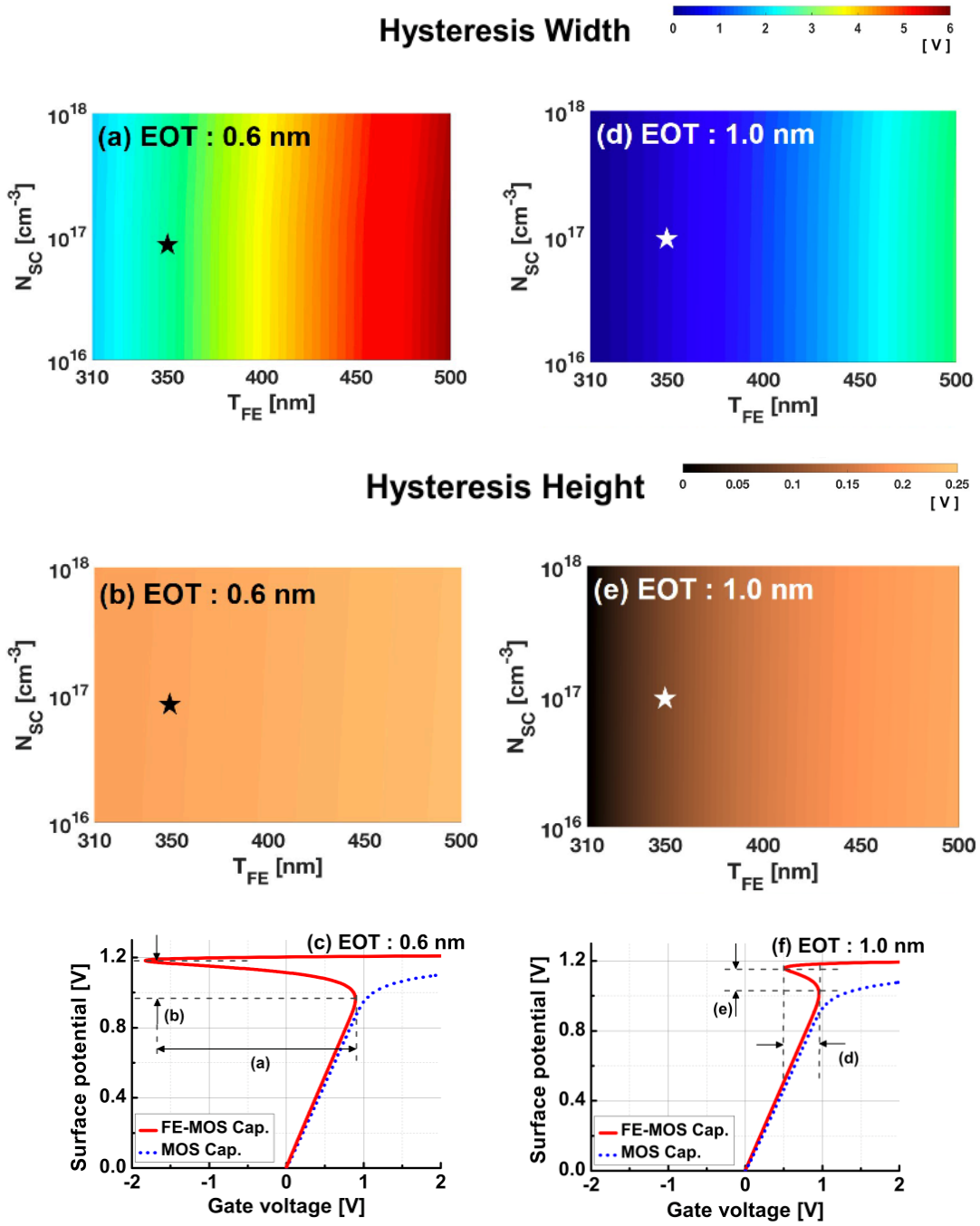


Fig. 3.5. Color map of hysteresis width [(a) and (d)] and hysteresis height [(b) and (e)] for different N_{SC} and T_{FE} with fixed EOT = 0.6 nm [(a) and (b)] and EOT = 1.0 nm [(d) and (e)] with PZT for the FE layer. The ψ_s–V_G plots with $N_{SC} = 10^{17}$ cm^{-3} and $T_{FE} = 350$ nm are shown for EOT = 0.6 nm and 1.0 nm in (c) and (f), respectively.

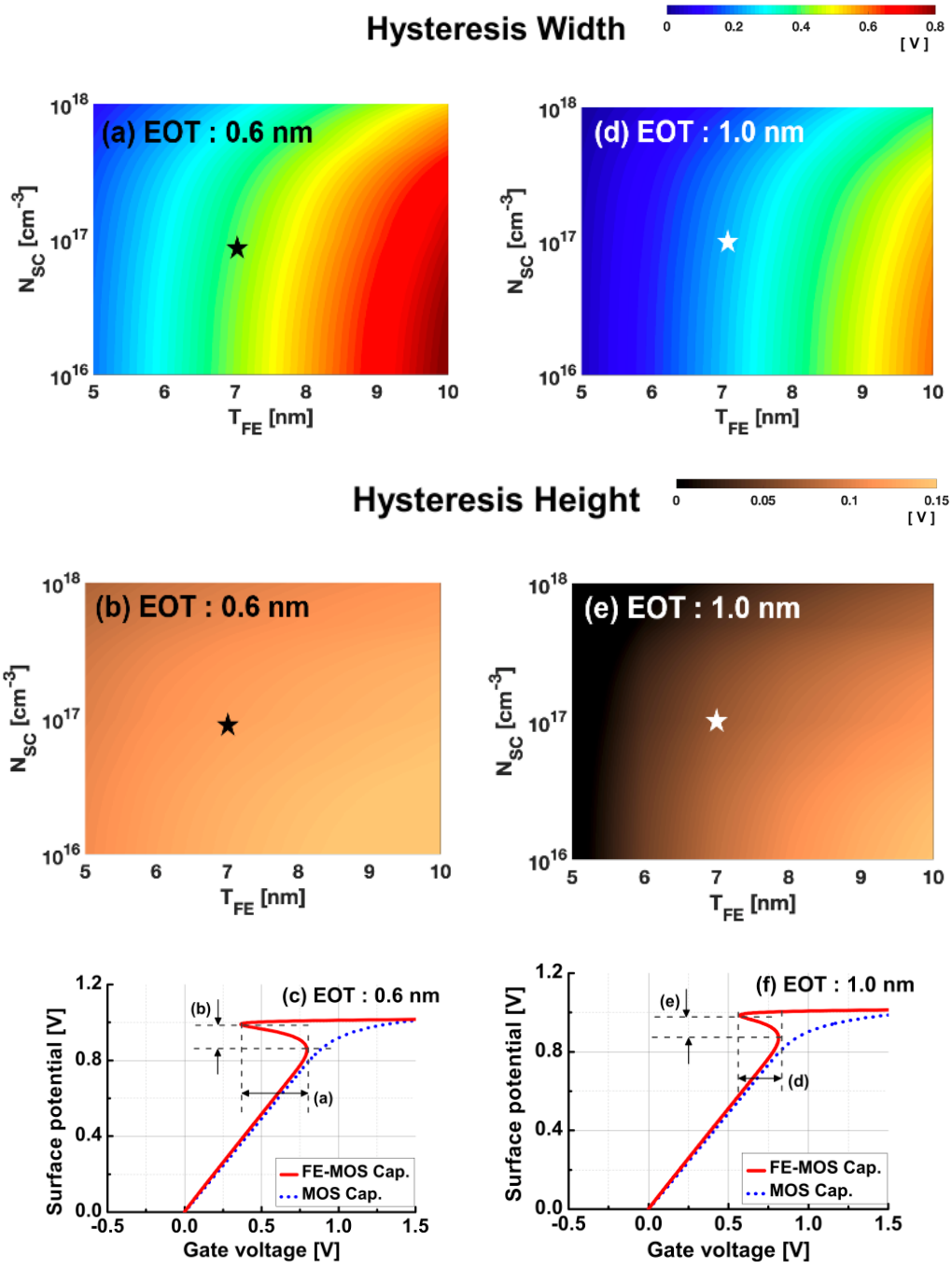


Fig. 3.6. Color map of hysteresis width [(a) and (d)] and hysteresis height [(b) and (e)] for different N_{SC} and T_{FE} with fixed EOT = 0.6 nm [(a) and (b)] and EOT = 1.0 nm [(d) and (e)] with HZO for the FE layer. The ψ_s–V_G plots with N_{SC} = 10^{17} cm^{-3} and T_{FE} = 7 nm are shown for EOT = 0.6 nm and 1.0 nm in (c) and (f), respectively.

Figures 3.5(a) and **3.5(b)** show color maps of hysteresis width and hysteresis height, respectively, determined by our model for different N_{SC} and T_{FE} at EOT = 0.6 nm. **Figure 3.5(c)** shows the ψ_s–V_G plot with T_{FE} = 350 nm and N_{SC} = 10^{17} cm^{-3} (marked with a star in **Figs. 3.5(a)** and **5(b)**). **Figures 3.5(d) – 3.5(f)** are the equivalent plots to **Figs. 3.5(a) – 3.5(c)** with EOT = 1.0 nm. It can be seen that hysteresis width is a strong function of EOT and T_{FE} as shown in **Fig. 3.5(a)** and **3.5(d)**. On the other hand, hysteresis height increases from 0.13 to 0.22 V by varying EOT from 1.0 to 0.6 nm at the marked point; however, it is less susceptible to T_{FE} compared to hysteresis width, especially when EOT is thin, as observed in **Figs. 3.5(b)** and **3.5(e)**. N_{SC} has the minimal impact on tuning hysteresis window for PZT, which can also be confirmed with **Figs. 3.4(a)** and **3.4(b)**. We have also plotted the equivalent figures for HZO in **Fig. 3.6** using significantly thinner T_{FE} of 5–10 nm. Overall, it shows the similar trend as PZT; however, hysteresis window is more susceptible to N_{SC} as shown in **Fig. 3.6**, which can also be seen from different A' and C' values for HJP-up and HJP-low in case of HZO, unlike other two materials.

3.4 Conclusion

In summary, the hysteresis window of FE-MOS capacitor is modeled. First, ψ_s–V_G relation was characterized based on the Gibbs free energy of the entire device. Simulation results show that hysteretic jump points can be tuned by varying parameters such as T_{FE}, EOT and N_{SC}. In particular, the surface potential of HJP exhibits a logarithmic function of N_{SC}, while the slope and the y-intercept can be affected by other parameters. Based on the simulation data, the surface potential of HJP was modeled, and the strategy to engineer the hysteresis window was discussed. It turned out that both hysteresis height and width can be modified effectively with T_{FE} and EOT. They can also be tuned by N_{SC} for thin HZO, but less susceptible when thick FE layer is used. The proposed model is expected to provide a powerful tool to tune the hysteresis window by engineering material and device parameters in order to satisfy the hysteresis requirement for different target applications. Although I have only focused on the impact of most important design parameters of T_{FE}, EOT and N_{SC} through modeling and simulation, this model could be further improved if other measurable data would also be considered, which is beyond the scope of this study and thereby suggested for future work.

Chapter 4
Simulation of Negative Capacitance Based on the Miller Model: Beyond the Limitation of the Landau Model

4.1 Introduction

Ferroelectric (FE) materials exhibit nonlinear hysteretic responses of spontaneous polarization (P) to the applied electric field. Although ferroelectricity was studied for the past hundred years [13], it has been only a decade since a concept of the negative capacitance (NC) based on FE was adopted by the electronics community for low-power steep-switching devices [12]. Over the years, FE materials have been integrated within various device structures such as planar metal-oxide-semiconductor (MOS) field-effect transistor (FET), FinFET, two-dimensional material FET, and tunnel FET [14]–[18], [86]–[88]. Furthermore, the concept of NC has been proven experimentally by the enhancement of a total capacitance with ferroelectric-dielectric (FE-DE) bilayer or the direct measurement of an FE capacitor with an external resistor [89]–[92].

Many theoretical works have also predicted and supported steep-switching characteristics of NC devices [30], [50], [51], [93], [94]. Most theoretical studies are based on the Landau model (LM) and describe the characteristic of FE using a so-called 'S-curve', which fits experimental data of $P - E_{FE}$ (spontaneous polarization vs. electric field) characteristics [30], [47], [50], [51], [93], [94]. Although different extent of hysteresis could be observed based on transient simulations using the LM [69], the LM cannot capture the gradual transition of polarization switching in steady states, as shown in **Fig. 4.1(a)**. Moreover, the LM becomes impractical for certain situations that $P - E_{FE}$ curves have small hysteresis with a gradual transition of polarization switching [e.g., see an inset of **Fig. 4.3(b)**]. In addition, most previous theoretical studies have used an analytical charge-based capacitor model [30], [47], [94], which treats FE as a dielectric material where background permittivity and spontaneous polarization are not individually considered. Notably, a simple charge-based capacitor model using a single grid point for the entire system cannot provide the spatial information of charge and polarization inside the device, while such details become important particularly for non-equilibrium conditions.

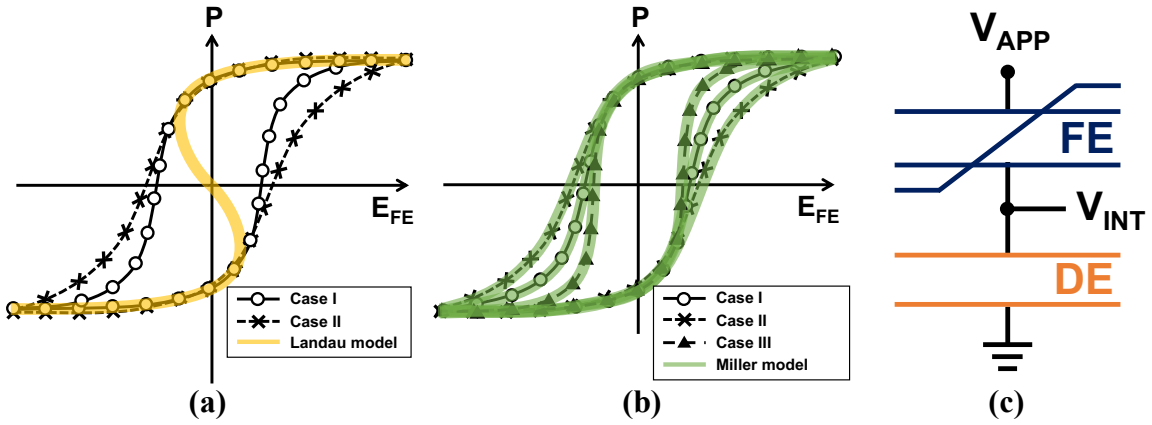


Fig. 4.1. (a) Schematics of $P - E_{FE}$ curves in steady states exhibiting two different transition cases of polarization switching for a stand-alone ferroelectric (FE) (solid line with circles and dashed line with asterisks). A single S-curve is used to fit these two cases based on the Landau model (LM) (yellow curve). (b) Schematics of $P - E_{FE}$ curves in steady states with three different transitions of polarization switching (black lines with symbols), each of which can be individually fitted by the Miller model (MM) (green curves). (c) Equivalent circuit model for an FE-DE capacitor used in this work.

To overcome the aforementioned limitations, in this study, we use the Miller model (MM) [57] as it can precisely represent the overall polarization switching including the transition region in steady states as depicted in **Fig. 4.1(b)**, which is inherently impossible with the S-curve using the LM. However, the MM seemingly fails to show steep switching with internal voltage (V_{INT}) amplification in an FE-DE capacitor [**Fig. 4.1(c)**] due to the monotonic increase of P with E_{FE} (i.e., 'positive slope' in the $P - E_{FE}$ curves) if a charge-based capacitor model is assumed; in comparison, the LM inherently implies the NC characteristic with the negative slope of the 'S-curve' [see the yellow curve in **Fig. 4.1(a)**]. Previous studies showed that *transient* NC characteristics can be observed by introducing a delay coefficient with the MM [69], [95], [96]. Unlike the previous studies, however, here we demonstrate NC characteristics, for the first time, even in *steady states* by performing a fully numerical device simulation on the FE-DE structure [**Fig. 4.2(a)**] based on the MM and Poisson's equation. Namely, the metrics of the NC characteristics in this study are internal voltage amplification with respect to the

change in applied voltage (dV_{INT}/dV_{APP}), the negative slope in the $P - V_{FE}$ curves extracted from the device simulation (in contrast to the positive slope in the $P - E_{FE}$ curves for stand-alone FE), and the total capacitance enhancement for the FE-DE capacitor.

We elucidate how the NC characteristic can be achieved even with the 'positive slope' in the MM. In particular, we demonstrate how the aforementioned two limitations of the LM can be overcome with the MM, using the FE whose $P - E_{FE}$ curve cannot be properly represented by the LM and those with different polarization switching transitions. Finally, we examine how hysteresis and voltage amplification are affected by the material parameters of FE, such as saturation polarization (P_{SAT}), remnant polarization (P_R), and coercive field (E_C).

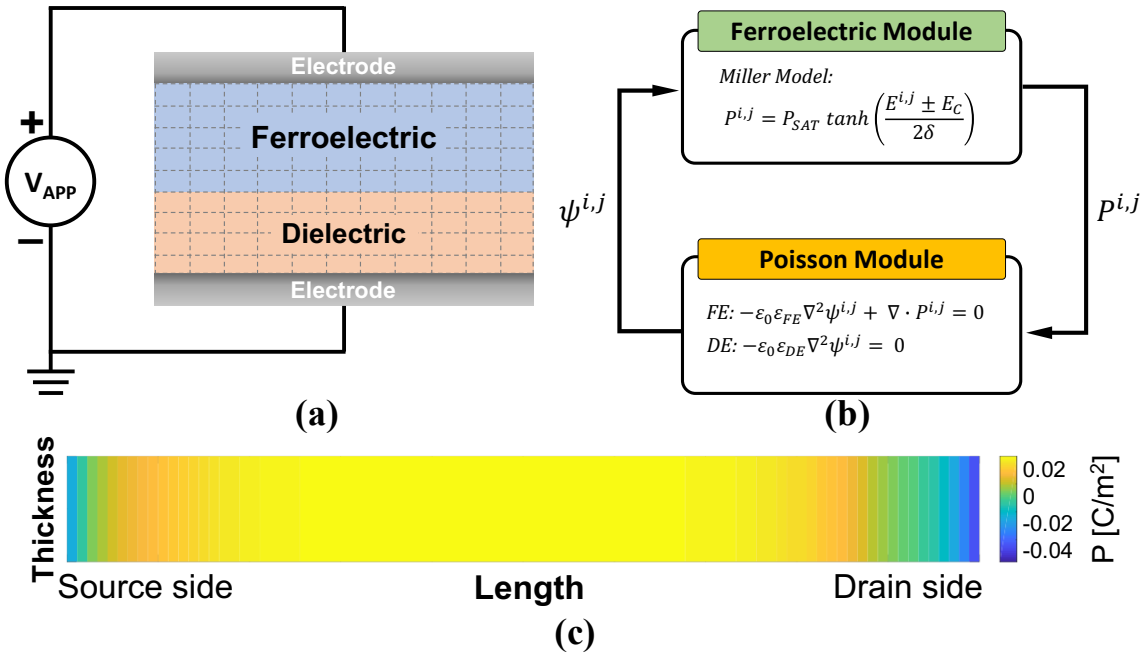


Fig. 4.2. (a) Schematic of an FE-DE capacitor used for simulations. (b) Flowchart for a fully numerical, self-consistent simulation between the ferroelectric module and the Poisson module. The superscripts of i, j represent the spatial information (i.e., different nodes within the device). (c) Two-dimensional plot of polarization within the FE layer in an NCFET.

4.2 Methods

Figure 4.2(a) shows the FE-DE structure simulated in this work, where grid points inside the device are evenly distributed. The thicknesses of FE and DE are varied, and the length of the capacitor is 15 nm and the spacing between two adjacent grid points is 0.25 nm. Dirichlet boundary condition is used at the top/bottom interface with electrodes and Neumann boundary condition is used on the sides for Poisson's equation. Unlike the case with a simple single-point charge-based capacitor model [30], [47], we evaluate the polarization and potential at each node inside the device using the MM and Poisson's equation, respectively. This makes it possible to evaluate the local average polarization value around each grid point, which can vary spatially with non-uniform electric field within a device. In particular, polarization variation within an FE is expected for NCFETs [97] as shown in **Fig. 4.2(c)**. Therefore, the proposed model developed in this study can be further extended to the simulation of NCFETs, which is suggested for future studies. In this work, multi-domains do not appear due to the nearly uniform electric field within the FE for the considered FE-DE structure, and hence, coupling between different domains is ignored. For the suggested future studies on NCFETs, however, domain interactions [21], [51] should also be considered along with this proposed model to achieve reliable results.

Figure 4.2(b) shows an iterative process along with the input/output parameters between the FE module and the Poisson module for self-consistent simulations. In the FE module, the MM is given by [57]

$$P^{i,j} = P_{SAT}\ tanh\left(\frac{E^{i,j} \pm E_C}{2\delta}\right), \tag{1}$$

in which $P^{i,j}$ and $E^{i,j}$ are polarization and electric field at the (i, j) node, respectively, and

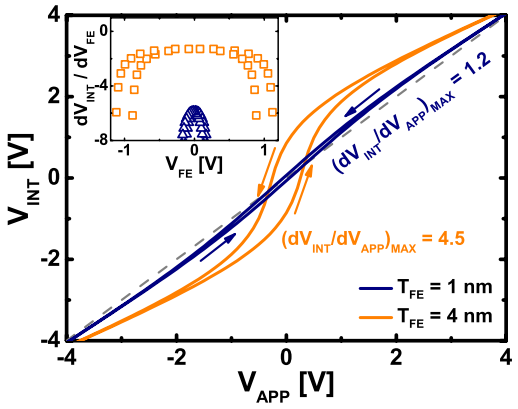
$$\delta = E_C \left[log\left(\frac{1+P_R/P_{SAT}}{1-P_R/P_{SAT}}\right)\right]^{-1}. \tag{2}$$

In the Poisson module, ε_0, ε_{FE}, and ε_{DE} are the permittivity of vacuum and the background FE/DE permittivity, respectively (ε_{FE} = 21 and ε_{DE} = 4 are used [51]). The FE module generates the spatial

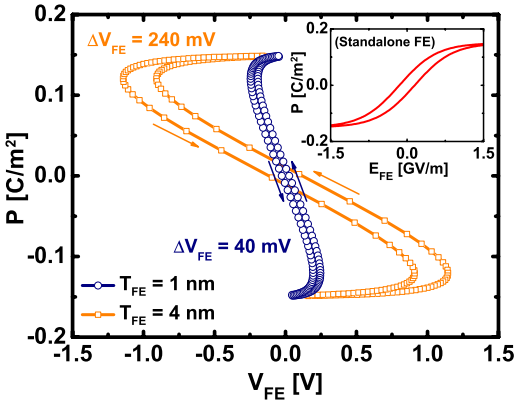
information of $P^{i,j}$ from $E^{i,j}$, which can be given by the potential ($\psi^{i,j}$) profile from the Poisson module. Then, the divergence of P ($\nabla \cdot P^{i,j}$) is calculated to achieve the potential within the FE, which naturally incorporates depolarization field – the origin of the NC effect demonstrated in this study (details will be discussed later in **Fig. 4.3**) – through the self-consistent simulation. This iterative process continues until $\psi^{i,j}$ is converged. The condition for the FE/DE interface is given by $(D_{DE} - D_{FE}) \cdot n_{FE-DE} = 0$, where $D_{DE(FE)}$ is electric displacement field for DE (FE) and n_{FE-DE} is the normal vector from FE to DE, resulting in

$$\varepsilon_0 \varepsilon_{FE} \frac{V_{FE}}{T_{FE}} + P = \varepsilon_0 \varepsilon_{DE} \frac{V_{INT}}{T_{DE}}, \tag{3}$$

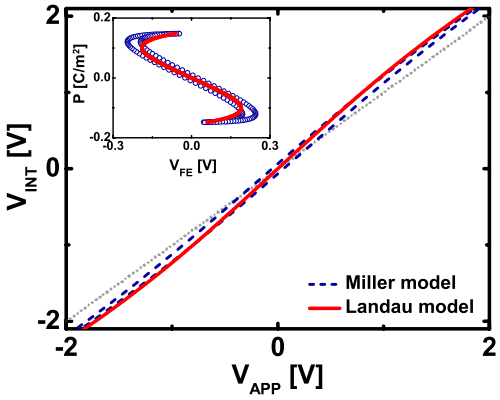
where $V_{FE} = V_{APP} - V_{INT}$ is voltage across FE, V_{APP} is applied voltage across the FE-DE capacitor, T_{FE} and T_{DE} are the thickness of FE and DE, respectively.


V_INT [V]
V_APP [V]
dV_INT / dV_FE
V_FE [V]
(dV_INT/dV_APP)_MAX = 1.2
(dV_INT/dV_APP)_MAX = 4.5
T_FE = 1 nm
T_FE = 4 nm

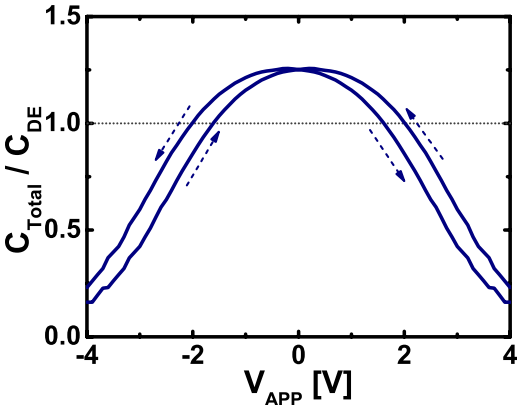
(a)


ΔV_FE = 240 mV
ΔV_FE = 40 mV
P [C/m²]
V_FE [V]
(Standalone FE)
E_FE [GV/m]
T_FE = 1 nm
T_FE = 4 nm

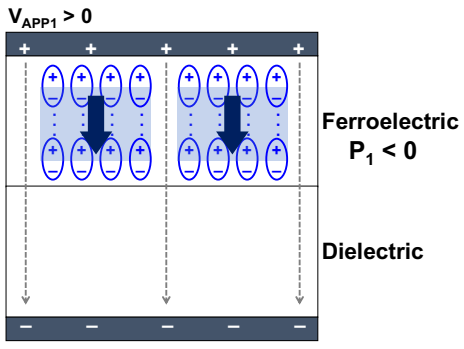
(b)


V_INT [V]
V_APP [V]
P [C/m²]
V_FE [V]
Miller model
Landau model

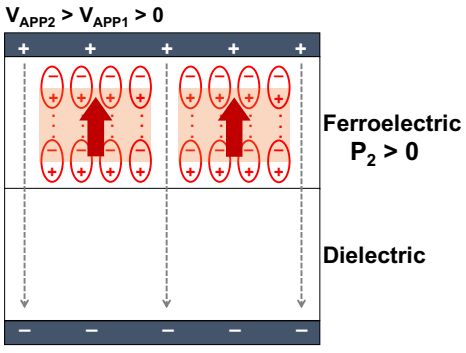
(c)


C_Total / C_DE
V_APP [V]

(d)


V_APP1 > 0
Ferroelectric
P_1 < 0
Dielectric

(e)


V_APP2 > V_APP1 > 0
Ferroelectric
P_2 > 0
Dielectric

(f)

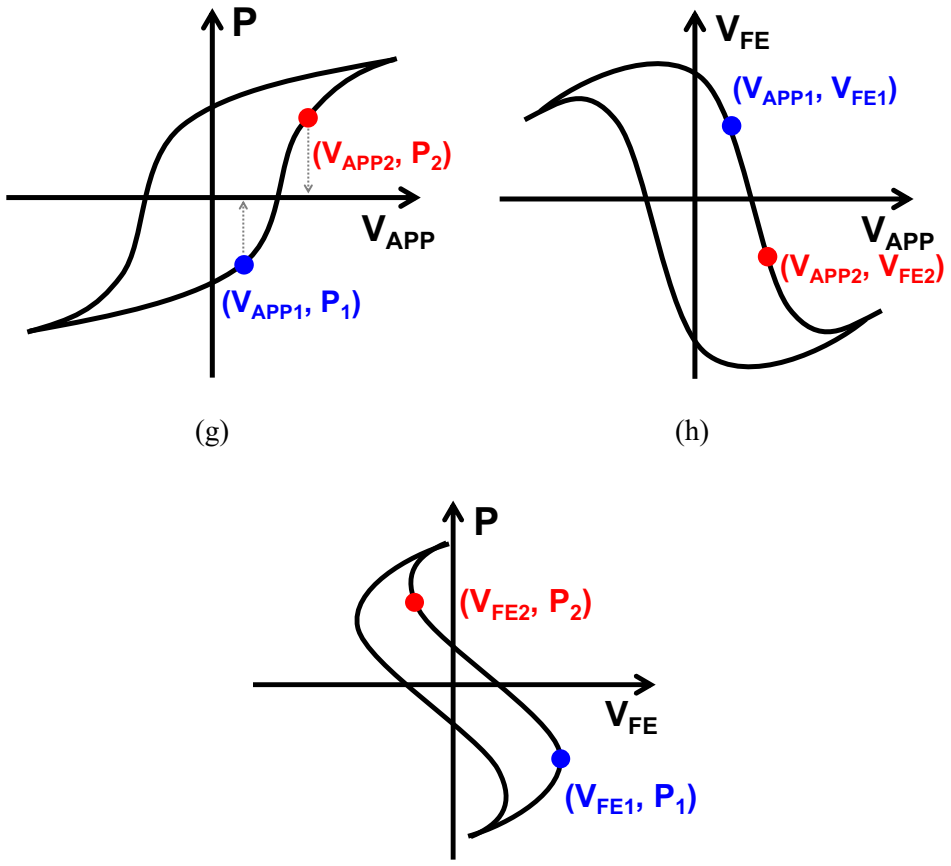


Fig. 4.3. (a) $V_{INT} - V_{APP}$ and (b) $P - V_{FE}$ plots for the FE-DE capacitor with different FE thickness (T_{FE}) of 1 nm and 4 nm and a fixed DE thickness (T_{DE}) of 1 nm. Insets: (a) dV_{INT}/dV_{FE} as a function of V_{FE} for two different T_{FE}'s and (b) $P - E_{FE}$ curve for the FE used in the FE-DE capacitor. Material parameters of FE: P_{SAT} = 0.15 C/m^2, P_R= 0.03 C/m^2 and E_C = 1.5 × 10^8 V/m. Both cases show the maximum dV_{INT}/dV_{APP} greater than 1 (i.e., voltage amplification). The hysteresis window for T_{FE} = 1 and 4 nm are 40 and 240 mV, respectively. (c) $V_{INT} - V_{APP}$ plot based on the MM and the LM for T_{FE} = 1. Insets: $P - V_{FE}$ plots showing the corresponding NC regions (navy for the MM; red for the LM). (d) Total capacitance (C_{Total}) to dielectric capacitance (C_{DE}) ratio as a function of applied voltage for the FE-DE capacitor with $T_{FE} = T_{DE}$ = 1 nm. (e, f) Schematics of the FE-DE capacitor showing the direction of electric field resulted from the applied voltage and the spontaneous polarization. (g) $P - V_{APP}$, (h) $V_{FE} - V_{APP}$, and (i) $P - V_{FE}$ plots showing two points at V_{APP1} and V_{APP2}, which represent the cases in (e) and (f).

4.3 Results and Discussion

Firstly, we show the NC effect in an FE-DE capacitor using the MM. Here we use the FE exhibiting gently inclined $P - E_{FE}$ curves with narrow hysteresis, as shown in the inset of **Fig. 4.3(b)**, which cannot be modelled properly by the LM using the 'S-curve'. **Figure 4.3(a)** shows V_{INT} as a function of V_{APP} for the FE-DE capacitor for T_{FE} of 1 nm and 4 nm. The NC effect can be seen by examining dV_{INT}/dV_{APP}, as it shows the amplification of V_{INT} with respect to the change in V_{APP}. The internal voltage amplification is confirmed with $dV_{INT}/dV_{APP} > 1$ for both cases. As the T_{FE} increases, both maximum dV_{INT}/dV_{APP} and hysteresis become greater. Compared with the case of T_{FE} = 1 nm, which exhibits nearly hysteresis-free characteristics (ΔV_{FE} = 40 mV) with $(dV_{INT}/dV_{APP})_{MAX}$ = 1.2, the FE with T_{FE} = 4 nm shows notable hysteresis of ΔV_{FE} = 240 mV and $(dV_{INT}/dV_{APP})_{MAX}$ = 4.5. **Figure 4.3(b)** shows the $P - V_{FE}$ characteristics extracted from our self-consistent result for the FE (with P_{SAT} = 0.15 C/m^2, P_R= 0.03 C/m^2, and E_C = 1.5 × 10^8 V/m [20]) of the capacitor simulated in **Fig. 4.3(a)**. The extracted P is calculated by taking the average of $P^{i,j}$ for all grid points. It should be noted that even though we have used the MM that exhibits the increase of P with E_{FE} implying the positive capacitance for the stand-alone FE (as an input of simulation), 'S-curves' representing the NC effects are observed for both T_{FE}'s in the $P - V_{FE}$ curves extracted from the output of simulation data. It is worth pointing out that, if this NC region is fitted with the LM (e.g., α, β and γ are -2.5 × 10^9 m·F^{-1}, 3 × 10^{10} m^{5}F^{-1}C^{-2} and 3 × 10^{12} m^{9}F^{-1}C^{-4}, respectively, for T_{FE} = 1 nm; see the inset of **Fig. 4.3(c)**), the $V_{INT} - V_{APP}$ curves from the LM and MM can be well matched each other as shown in **Fig. 4.3(c)**. **Figure 4.3(d)** shows the total capacitance (C_{Total}) enhancement in the FE-DE structure (with T_{FE} = 1 nm) at -2 V < V_{APP} < 2 V, compared to the dielectric capacitance C_{DE}, which exhibits the same trend as the reported experimental results [90], [91].

Physics behind the observation above can be understood from **Fig. 4.3(e)-(i)**. **Figures 4.3(e)** and **4.3(f)** are the FE-DE structure showing the direction of electric field resulted from applied voltage (thin dashed arrows) and that of depolarization field induced by spontaneous polarization (thick solid arrows). **Figures 4.3(g)-(i)** show $P - V_{APP}$, $V_{FE} - V_{APP}$, and $P - V_{FE}$ characteristics based on simulation results. The orientation of P changes as the applied voltage increases from V_{APP1} to V_{APP2} [**Fig. 4.3(g)**]. P_1, which is polarization at V_{APP1}, increases the total field across the FE since the direction of depolarization field induced by P_1 is same as that by the applied voltage, as illustrated in **Fig. 4.3(e)**. Consequently, V_{FE1} at V_{APP1} becomes enhanced. On the other hand, P_2 decreases the total field across

the FE due to the opposite direction of depolarization field induced by P_2 as compared to that by the applied voltage [see **Fig. 4.3(f)**]. In this case, V_{FE2} at V_{APP2} becomes a negative value [**Fig. 4.3(h)**] as the depolarization field induced by the spontaneous polarization overpowers that by the applied voltage [**Fig. 4.3(f)**]. This change in depolarization field direction caused by the spontaneous polarization switching is the main mechanism for the NC effect observed in **Fig. 4.3(a)**, **4.3(b)** and **4.3(d)**. Finally, **Fig. 4.3(i)** shows the intrinsic NC behavior of FE, which can be achieved from **Figs. 4.3(g)** and **4.3(h)** by eliminating V_{APP}. It should be pointed out that the polarization switching is not a requirement to obtain NC behavior, but it originates from polarization changes.

The slope in the NC region can be evaluated by dP/dV_{FE}. Along with the **Eq. (3)**, it gives rise to the condition for the inherent NC as

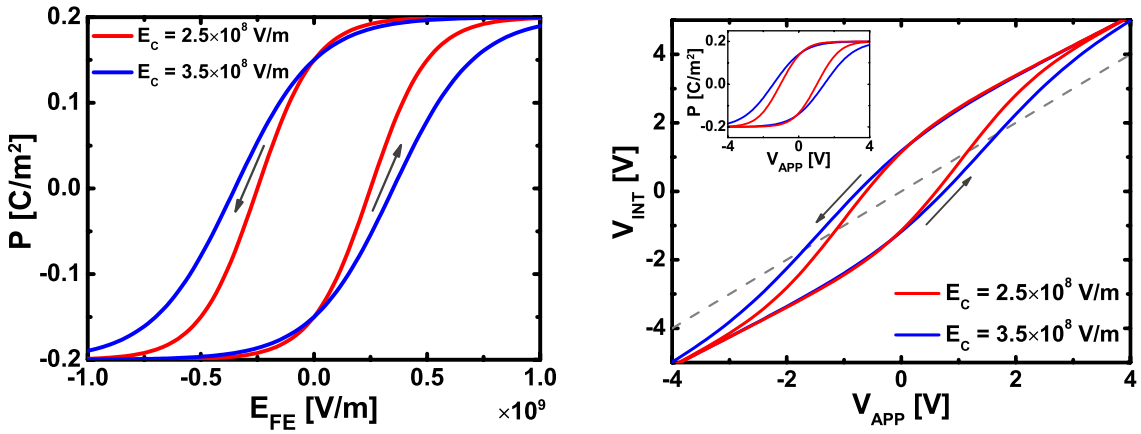
$$\frac{dP}{dV_{FE}} = \frac{\varepsilon_0\varepsilon_{DE}}{T_{DE}}\frac{dV_{INT}}{dV_{FE}} - \frac{\varepsilon_0\varepsilon_{FE}}{T_{FE}} < 0. \tag{4}$$

The negative slope in the $P - V_{FE}$ plot is steeper with T_{FE} = 1 nm as compared to the case with T_{FE} = 4 nm [see **Fig. 4.3(b)**]. This is because dV_{INT}/dV_{FE} [see the inset of **Fig. 4.3(a)**] and $-\varepsilon_0\varepsilon_{FE}/T_{FE}$ become more negative with thinner FE.

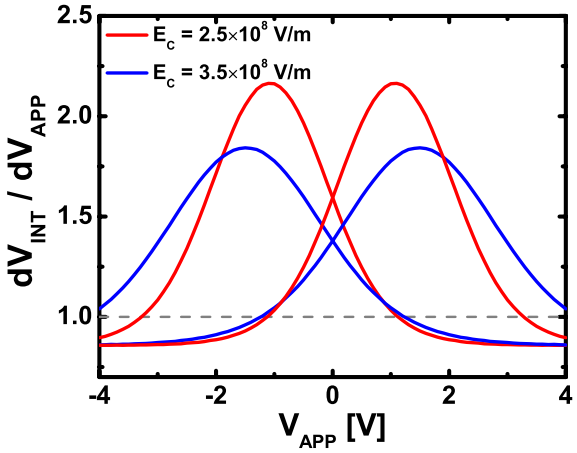
As mentioned earlier, the MM can handle different transitions of polarization switching, unlike the LM. Here we created such two different cases of FE by varying E_C (with P_{SAT} = 0.2 C/m^2 and P_R = 0.15 C/m^2 unchanged) as shown in **Fig. 4.4(a)**. Note that, if the LM were adopted, these two $P - E_{FE}$ curves were fitted by a single 'S-curve' and no distinction could be made. Using these two different inputs of $P - E_{FE}$ curves for the FE, we simulated the FE-DE capacitor ($T_{FE} = T_{DE}$ = 2 nm) to examine how V_{INT} is affected by the applied voltage across the device. **Figure 4.4(b)** shows that two $V_{INT} - V_{APP}$ curves with different hysteresis are achieved, which would not be possible if the LM were used. The maximum internal voltage amplification is greater with $E_C = 2.5 \times 10^8$ V/m by 22% as compared to the case with $E_C = 3.5 \times 10^8$ V/m [**Fig. 4.4(c)**].

The effect of different polarization switching region can be understood with the inset of **Fig. 4.4(b)** (P vs. V_{APP}) along with **Eq. (5)**, which is derived from **Eq. (3)**:

$$\left(\frac{\varepsilon_0\varepsilon_{DE}}{T_{DE}}+\frac{\varepsilon_0\varepsilon_{FE}}{T_{FE}}\right)\frac{dV_{INT}}{dV_{APP}}=\frac{dP}{dV_{APP}}+\frac{\varepsilon_0\varepsilon_{FE}}{T_{FE}}. \quad (5)$$



(a) (b)

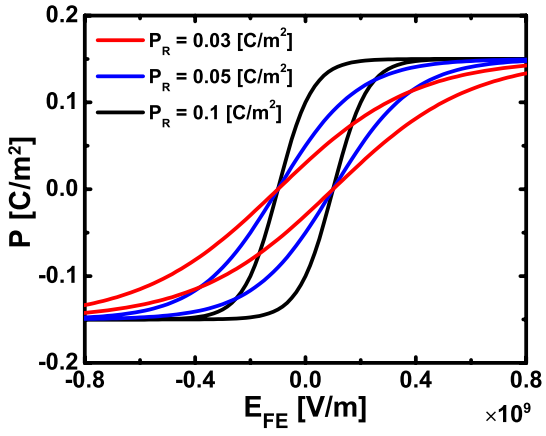


(c)

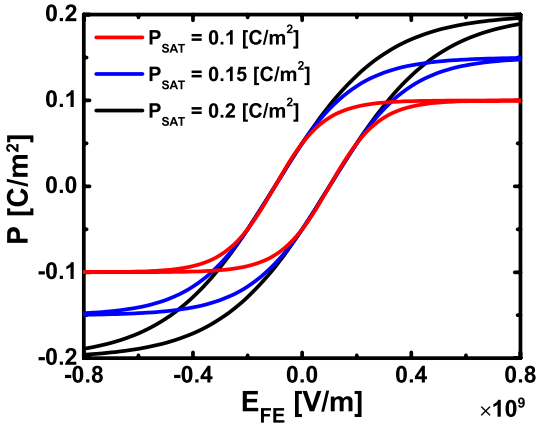
Fig. 4.4. (a) $P-E_{FE}$ characteristics of a ferroelectric, (b) $V_{INT}-V_{APP}$ (inset: $P-V_{APP}$), and (c) $dV_{INT}/dV_{APP}-V_{APP}$ plots for the FE-DE capacitor with two different E_C = 2.5 × 10^8 V/m and 3.5 × 10^8 V/m. The hysteresis windows are 1.2 V and 1.5 V for E_C of 2.5 × 10^8 V/m and 3.5 × 10^8 V/m, respectively. The following parameters are used in Fig. 4: T_{FE} = T_{DE} = 2 nm, P_{SAT} = 0.2 C/m^2 and P_R = 0.15 C/m^2.

Our simulation result shows that spontaneous polarization switches more abruptly with a smaller E_C as V_{APP} increases [see the inset of **Fig. 4.4(b)**], resulting in steeper slope of dP/dV_{APP} in the transition region. On the other hand, the internal voltage amplification dV_{INT}/dV_{APP} is directly proportional to dP/dV_{APP} according to **Eq. (5)**. Therefore, the internal voltage amplification in the transition region becomes more significant under lower E_C as it can be seen in **Fig. 4.4(c)**.

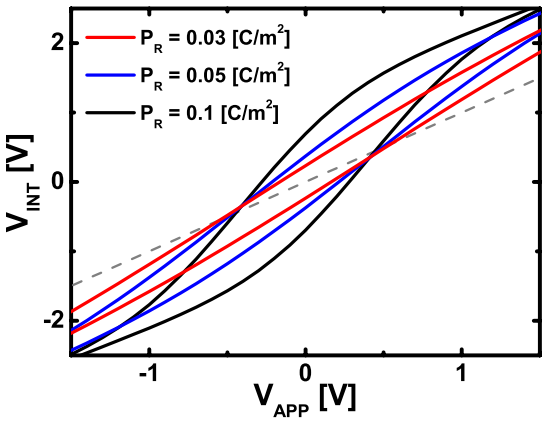
So far, we have varied only E_C to investigate the effect of polarization switching transition of FE in **Fig. 4.4**. However, there are other parameters describing the behavior of FE that can be modified within the MM. Here we simulate by varying P_R (with P_{SAT} and E_C unchanged) and P_{SAT} (with fixed P_R and E_C), which, along with the result from **Fig. 4.4**, will provide useful insight into how the material parameters of FE can affect the overall performance of the device. **Figures 4.5(a)** and **4.5(d)** show $P - E_{FE}$ characteristics of the stand-alone FE materials with (a) P_R = 0.03, 0.05, and 0.1 C/m^2 (P_{SAT} = 0.15 C/m^2) and (d) P_{SAT} = 0.1, 0.15, and 0.2 C/m^2 (P_R = 0.05 C/m^2), commonly with $E_C = 1 \times 10^8$ V/m and $T_{FE} = T_{DE} = 2$ nm. We have plotted V_{INT} and dV_{INT}/dV_{APP} as a function of V_{APP} [see **Figs. 4.5(b)**, **4.5(c)** for varying P_R; **Figs. 4.5(e), 4.5(f)** for varying P_{SAT}]. Our results indicate that small E_C and P_R are needed to achieve small hysteresis [see **Figs. 4.4(b)** and **4.5(b)**], but P_{SAT} has a negligible effect on hysteresis [**Fig. 4.5(e)**]. On the other hand, **Fig. 4.5(c)** shows that greater internal voltage amplification can be achieved with larger P_R, while higher P_{SAT} can provide a wider range of V_{APP} for the voltage amplification ($dV_{INT}/dV_{APP} > 1$ can be achieved at -3.2 V < V_{APP} < 3.2 V with P_{SAT} = 0.2 C/m^2) with minor impacts on $(dV_{INT}/dV_{APP})_{MAX}$ [see **Fig. 4.5(f)**].


P_R = 0.03 [C/m^2]
P_R = 0.05 [C/m^2]
P_R = 0.1 [C/m^2]
P [C/m^2]
E_FE [V/m]
×10^9

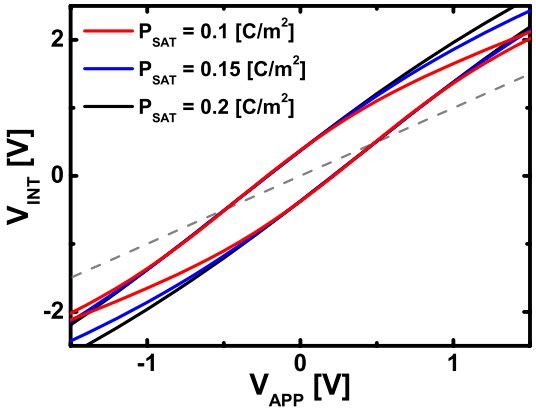
(a)


P_SAT = 0.1 [C/m^2]
P_SAT = 0.15 [C/m^2]
P_SAT = 0.2 [C/m^2]
P [C/m^2]
E_FE [V/m]
×10^9

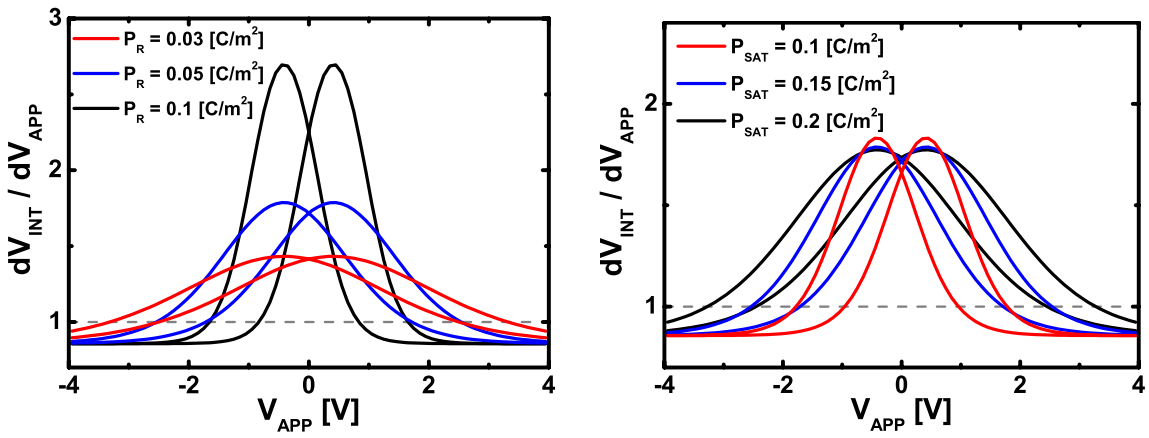
(d)


P_R = 0.03 [C/m^2]
P_R = 0.05 [C/m^2]
P_R = 0.1 [C/m^2]
V_INT [V]
V_APP [V]

(b)


P_SAT = 0.1 [C/m^2]
P_SAT = 0.15 [C/m^2]
P_SAT = 0.2 [C/m^2]
V_INT [V]
V_APP [V]

(e)



(c) (f)

Fig. 4.5. $P - E_{FE}$ (for a stand-alone FE), $V_{INT} - V_{APP}$ and dV_{INT}/dV_{APP} (for an FE-DE capacitor) as a function of V_{APP} for various P_R (0.03, 0.05, and 0.1 C/m^2) with fixed P_{SAT} and E_C [(a) – (c)]; and for various P_{SAT} (0.1, 0.15, and 0.2 C/m^2) with fixed P_R and E_C [(d) – (f)]. Hysteresis values are 0.28 V, 0.38 V, and 0.56 V for P_R = 0.03, 0.05, and 0.1 C/m^2, respectively, in (b) and 0.4 V for all P_{SAT} values in (e). The following parameters are used: $T_{FE} = T_{DE}$ = 2 nm and E_C = 1 × 10^8 V/m. P_{SAT} of 0.15 C/m^2 for (a) – (c); P_R of 0.05 C/m^2 for (d) – (f).

4.4 Conclusion

In conclusion, an FE-DE capacitor using the MM with Poisson's equation is simulated. I have employed the MM as it can accurately describe polarization switching behaviors particularly in the transition region to overcome the limitation of the LM. Self-consistent simulation results exhibited the steady-state NC characteristics even with a 'positive slope' in the $P - E_{FE}$ curve using the MM. I have elucidated the origin of the NC effect by investigating the changes in spontaneous polarization, electric field and voltage across the FE as the applied voltage increases. It was seen that thicker T_{FE} could result in a greater NC effect with larger hysteresis. I have also demonstrated that FE materials with different transitions of polarization switching can be simulated by modifying E_C with the MM, and the NC effect can be boosted if the FE having more abrupt transition is used within the FE-DE capacitor. Finally, I have varied other material parameters of FE as well to investigate the general impact of FE properties on the NC effect. The results show that greater internal voltage amplification is expected when FE has

larger P_R. On the other hand, when higher P_{SAT} is used, the NC effect can be achieved for a wider range of V_{APP} with a negligible effect on the magnitude of voltage amplification. When it comes to the hysteresis, small E_C and P_R are required to reduce hysteresis but P_{SAT} has only a negligible impact on hysteresis. This study creates a novel computational framework based on the MM to explore an FE-DE capacitor, and it is suggested to apply our approach to investigate more complicated NCFET structures for a future work.

Chapter 5
A Computational Framework for Gradually Switching Ferroelectric-Based Negative Capacitance Field-Effect Transistors

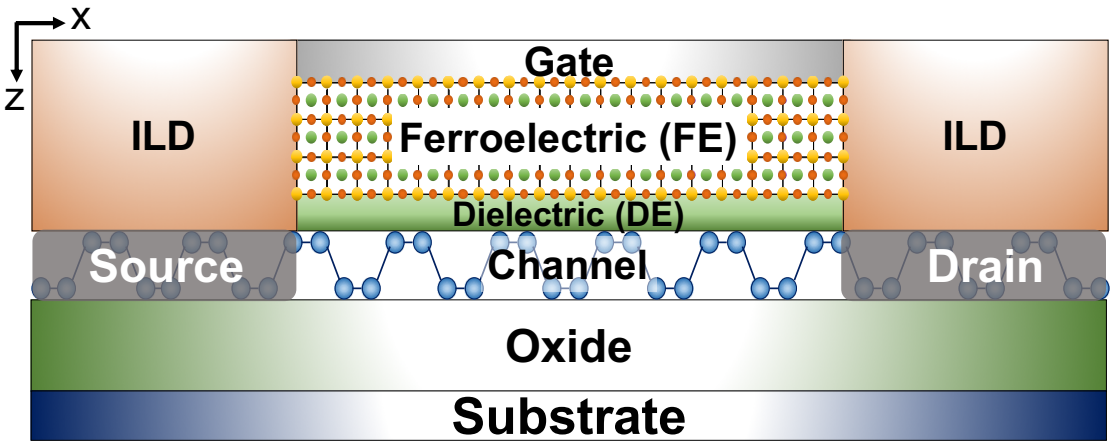
5.1 Introduction

Negative capacitance field-effect transistors (NCFETs) are one of the promising front-runners for future low-power electronic devices [14]–[16], [35], [41], [98]. Recent studies have demonstrated that a ferroelectric (FE) material in an NCFET can improve the performance of base FETs, such as planar MOSFETs, FinFETs, and tunnel FETs, beyond the classical limit [14]–[20], [88], [99].

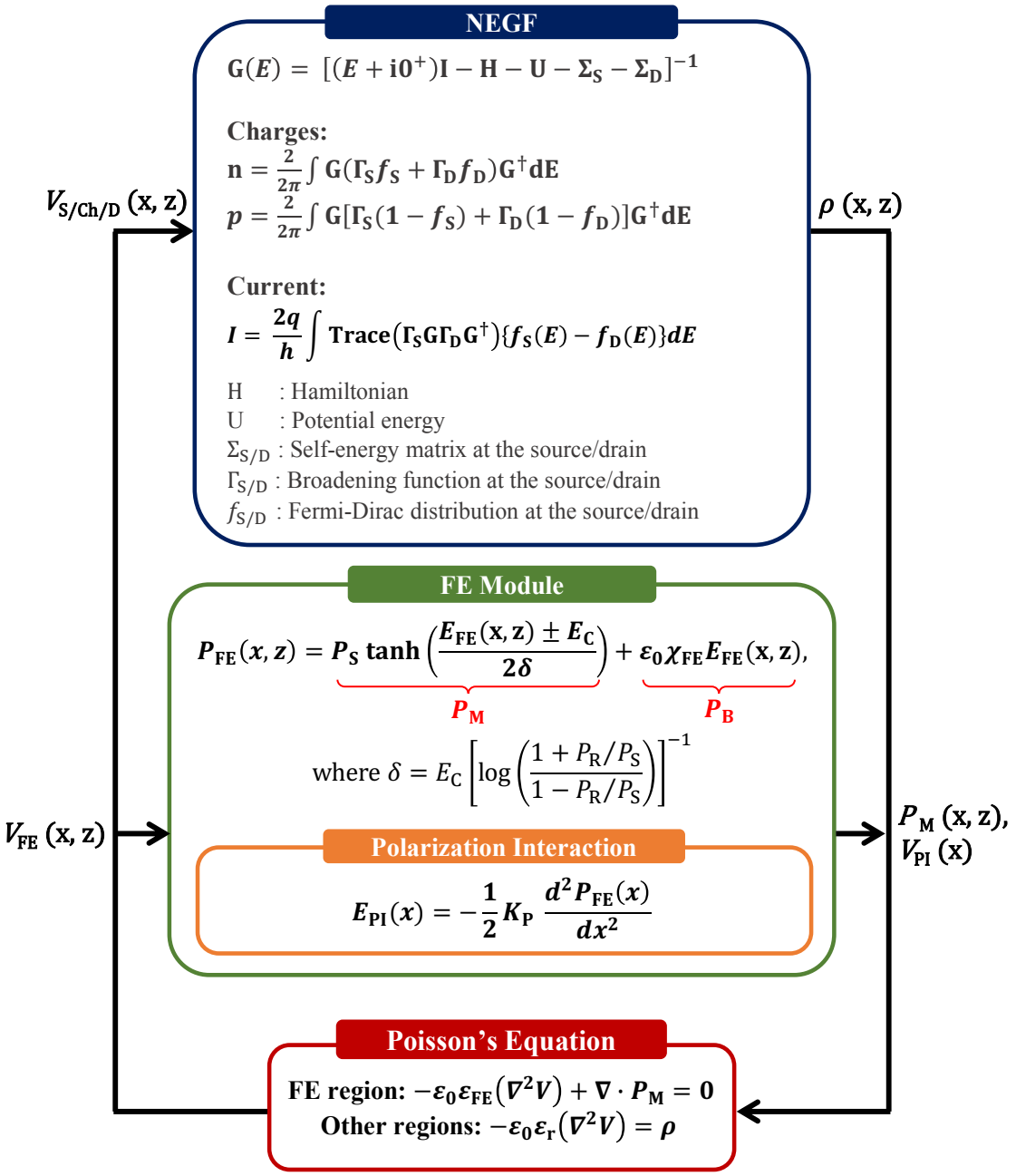
The steep switching characteristic of the NCFET has been explained by means of theory and simulation [30], [47]–[51], [94]. Most simulation studies are based on the Landau model (LM), where spontaneous polarization (P) as a function of electric field across the FE layer (E_{FE}) is fitted for a stand-alone FE using the so-called 'S-curve' [30], [47]–[51], [94], [100]. However, a recent study has shown that the LM can fail to accurately describe certain cases such as the gradual transition of polarization switching in steady states, and proposed that the Miller model (MM) can circumvent such limitations [101]. Although the previous study demonstrated that the NC effect can be achieved even with the monotonic increase of P with E_{FE} in the MM (i.e., 'positive slope' in the $P - E_{\mathrm{FE}}$ curve unlike with the LM) when divergence of polarization within Poisson's equation is evaluated properly by means of the self-consistent simulation, it was shown only for an ferroelectric-dielectric (FE-DE) capacitor in steady states [101]. On the other hand, other previous studies investigated 'transient NC' characteristics in the NCFET by employing a delay coefficient with the MM [95], [102]–[104]. Hence, a fully numerical simulation study of steady-state NC characteristics for the NCFET based on the MM has not been demonstrated yet, despite the high demands for such rigorous simulation that explore technical insight into the NCFET beyond the limitation of the Landau picture. Moreover, polarization interactions within the FE should be considered for the NCFET as polarization can vary significantly along the device position, which was not the case with the previous study for the FE-DE structure [101].

In this work, we simulate steady-state NC characteristics of the NCFET, for the first time, by performing a fully numerical self-consistent device simulation based on non-equilibrium Green's function (NEGF) formalism, the MM considering polarization interactions, and Poisson's equation. Since our model can accurately capture the gradual transition of polarization switching within the FE

layer, the characteristics of practical NCFETs can be investigated accurately through material and device parameters engineering. Thus, we have investigated the impact of FE on the performance of NCFETs by varying FE thickness (T_{FE}) and its material parameters [i.e., saturation polarization (P_S), remnant polarization (P_R), and coercive field (E_C)]. By using our rigorous simulation tool, we have also reproduced T_{FE} dependence of the NC effect as previously observed in experiments and elucidate the origin of the critical T_{FE} for which the NC effect can be maximized.



(a)



(b)

Fig. 5.1. (a) Schematic of the NCFET used for simulations. (b) Flowchart of the self-consistent simulation process consisting of three modules: the NEGF, the FE module including polarization interactions, and Poisson's equation. The (x, z) represents different nodes within the device.

5.2 Simulation Process

Fig. 5.1(a) shows the schematic of an NCFET simulated in this work. We have adopted monolayer black phosphorus (BP) for the channel material, $Hf_{0.5}Zr_{0.5}O_2$ (HZO) for the FE, and SiO_2 for the DE layer. It should be noted that we have chosen the BP as a channel material for computational efficiency, however, silicon or other two-dimensional materials could be a candidate for channel material. By using the same simulation procedure as shown in **Fig. 5.1(b)** with the proper Hamiltonian of given channel material, an NCFET using different channel material can be evaluated. The channel length (L_{CH}), source/drain extension length ($L_{\mathrm{S/D}}$), equivalent oxide thickness (EOT), and source/drain doping concentration ($N_{\mathrm{S/D}}$) are 20 nm, 20 nm, 0.5 nm, and 2.6×10^{13} cm^{-2}, respectively. T_{FE}, P_{S}, P_{R}, and E_{C} of the FE will be varied to examine their effects on the device performance. Low-κ (κ = 2) inter-layer dielectric (ILD) is used for spacers [105].

The simulation processes along with the detailed equations for the carrier transport, the MM, polarization interactions, and the electrostatics are shown in **Fig. 5.1(b)**. Parameters calculated in each module are exchanged through the iterative process. Ballistic transport is simulated using the NEGF method [61] under the tight-binding approximation [106], [107]. In the FE region, total polarization within FE (P_{FE}) is determined as $P_{\mathrm{FE}} = P_{\mathrm{M}} + P_{\mathrm{B}}$, where P_{M} is the spontaneous polarization of the ferroelectric and P_{B} is the background polarization which is the rest of contributions to the P_{FE}, calculated as $P_{\mathrm{B}} = \varepsilon_0 \chi_{\mathrm{FE}} E_{\mathrm{FE}}$, where ε_0 and χ_{FE} are the permittivity of vacuum and the background susceptibility of FE, respectively [58]. For P_{M}, we have adopted the MM to describe the polarization switching under an electric field as [57]

$$P_{\mathrm{M}}(x,z) = P_{\mathrm{S}} \tanh\left(\frac{E_{FE}(x,z) \pm E_C}{2\delta}\right), \tag{1}$$

where

$$\delta = E_{\mathrm{C}} \left[\log\left(\frac{1+P_{\mathrm{R}}/P_{\mathrm{S}}}{1-P_{\mathrm{R}}/P_{\mathrm{S}}}\right)\right]^{-1}. \tag{2}$$

The Miller model generates the spatial information of polarization at a given node, $P_{\mathrm{M}}(x,z)$, within the FE based on the electric field, $E_{FE}(x,z)$ that is calculated from Poisson's equation. It should be noted that the polarization mentioned in this work represents the local average polarization at each node (x,z)

[101]. We then introduce the effect of polarization interaction using the average P_{FE} within the FE thickness along the x direction [$P_{\mathrm{FE}}(x)$] as [51]

$$E_{\mathrm{PI}}(x) = -\frac{1}{2} K_{\mathrm{P}} \frac{d^2 P_{\mathrm{FE}}(x)}{dx^2}, \tag{3}$$

where E_{PI} and K_{P} are the electric field induced by the polarization interactions and the interaction coefficient, respectively. We assume that the polarization interaction along the z direction is insignificant due to the thin FE considered. The polarization interaction effect captured by E_{PI} is integrated in our simulation process by updating the interface condition between FE and DE in the Poisson module to $V_{\mathrm{INT}} + V_{\mathrm{PI}}$, where V_{INT} is the internal voltage (i.e., the potential at the interface between FE and DE) and $V_{\mathrm{PI}} = E_{\mathrm{PI}} \times T_{\mathrm{FE}}$.

In the Poisson module, $-\varepsilon_0 \varepsilon_{\mathrm{FE}}(\nabla^2 V) + \nabla \cdot P_{\mathrm{M}} = 0$ is used within the FE region, where $\varepsilon_{\mathrm{FE}}$ (equal to χ_{FE} + 1) is the permittivity of the background FE. For other regions, the above equation can be simplified to $-\varepsilon_0 \varepsilon_{\mathrm{r}}(\nabla^2 V) = \rho$, where ε_{r} and ρ are relative permittivity and charge density, respectively. Note that ρ becomes zero except for the semiconductor region.

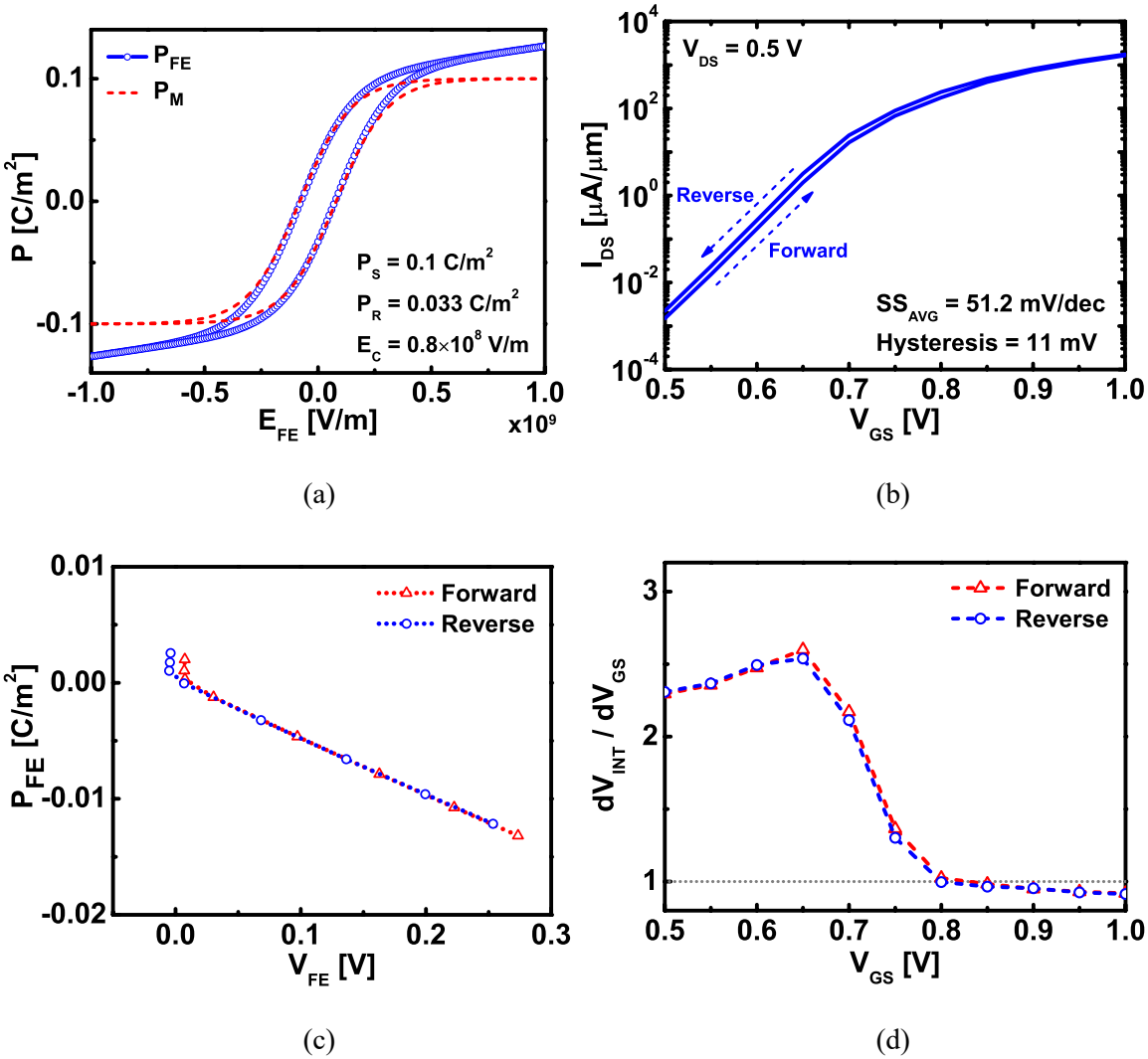


Fig. 5.2. (a) P_{FE} and P_M vs. E_{FE} curves for the FE (P_S = 0.1 C/m^2, P_R = 0.033 C/m^2, and E_C = 0.8×10^8 V/m) used for the NCFET. (b) $I_{DS} - V_{GS}$ plots of forward and reverse bias sweep for the NCFET with the T_{FE} = 1 nm and K_P = 1 × 10^{-7} m^3/F. Both sweep directions show the steep switching characteristics (average SS = 51.2 mV/dec) and the transfer characteristics show a hysteresis-free condition (i.e., hysteresis window is as narrow as 11 mV). (c) $P_{FE} - V_{FE}$ plots extracted from the NCFET simulation for both sweep directions showing NC characteristics (i.e., negative slope). (d) dV_{INT}/dV_{GS} vs. V_{GS} curves for the NCFET exhibiting $dV_{INT}/dV_{GS} > 1$ (i.e., internal voltage amplification).

5.3 Results and Discussion

Fig. 5.2(a) shows P_{FE} and P_M as a function of E_{FE} for the stand-alone FE with P_S = 0.1 C/m^2, P_R = 0.033 C/m^2, and $E_C = 0.8\times10^8$ V/m. To illustrate the benefit of using the MM, we have chosen an FE having a $P - E_{FE}$ curve such that narrow hysteresis with a gradual change in polarization switching can be observed, as it cannot be accurately described by the LM, by considering a reasonable range of material parameters for HZO from experiments [20]. The slope close to the saturated polarization region in P_{FE} is attributed to the P_B term which varies with χ_{FE}. The value of χ_{FE} can be determined from experimentally measured $P - E_{FE}$ curves, and we have used χ_{FE} = 3 in this study.

We have simulated characteristics of the NCFET based on the FE in **Fig. 5.2(a)**. Drain current (I_{DS}) vs. gate voltage (V_{GS}) curves for the NCFET are shown in **Fig. 5.2(b)** for both sweep directions at a drain voltage (V_{DS}) of 0.5 V with T_{FE} = 1 nm, where steep-switching and hysteresis-free characteristics are clearly demonstrated. We have achieved an average subthreshold swing of SS = 51.2 mV/dec (measured from V_{GS} of 0.5 V to the threshold voltage, V_{TH}) at room temperature. The hysteresis (defined as ΔV_{TH} between the forward and reverse bias directions) is as low as 11 mV, and hence it can be considered as hysteresis-free. The interactions between adjacent polarizations were considered in all our simulations (details of the polarization interactions will be discussed later in **Fig. 5.3**) with K_P = 1 × 10^{-7} m^3/F [51] for **Fig. 5.2**.

Fig. 5.2(c) shows the P_{FE} as a function of V_{FE} (voltage across the FE) extracted from the simulation results. The NC effect is evidenced by the negative slope in the $P_{FE} - V_{FE}$ curves, which results in the observed steep switching characteristics in **Fig. 5.2(b)**. To evaluate how much the internal voltage ($V_{INT} = V_{GS} - V_{FE}$) can be amplified due to the NC effect by varying V_{GS}, we present the derivative of V_{INT} with respect to V_{GS} (dV_{INT}/dV_{GS}) as a function of V_{GS} in **Fig. 5.2(d)**. It shows $dV_{INT}/dV_{GS} > 1$ at V_{GS} < 0.8 V which is the requirement for SS improvement (i.e., sub-60 mV/dec at room temperature) according to the following equation

$$SS = \frac{dV_{GS}}{dV_{INT}} \times \frac{dV_{INT}}{d\psi_{CH}} \times \frac{d\psi_{CH}}{d(logI_{DS})}, \quad (4)$$

where the ψ_{CH} is the channel potential. The minimum value of $\frac{dV_{\mathrm{INT}}}{d\psi_{\mathrm{CH}}} \times \frac{d\psi_{\mathrm{CH}}}{d(logI_{\mathrm{DS}})}$, which is the physical limit of SS for the conventional MOSFET, is 60 mV/dec at room temperature. Since the voltage amplification ($dV_{\mathrm{INT}}/dV_{\mathrm{GS}} > 1$) was observed at V_{GS} < 0.8 V, SS smaller than 60 mV/dec could be achieved.

Next, we have investigated the effect of polarization interactions within FE on the characteristics of the NCFET by varying the K_{P} value in **Eq. (3)**. **Fig. 5.3(a)** shows polarization variation within the FE along the *x* position with two different K_{P} values (2.5×10^{-8} m^3/F for weak polarization interaction; 2.5×10^{-7} m^3/F for strong polarization interaction). Due to the non-equilibrium condition across the device from applied V_{GS} and V_{DS}, the potential fluctuation is expected, which results in the polarization variation within the FE as shown in **Fig. 5.3(a)**. To investigate how the performance of the NCFET is affected by polarization interactions, we have varied K_{P} in **Eq. (3)**. **Fig. 5.3(b)** shows $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curves with strong and weak polarization interactions. Average SS with different values of K_{P} is summarized in the Table in the inset of **Fig. 5.3(b)**. We can see from **Fig. 5.3(b)** that the polarization interactions have a negligible impact on the ON current. On the other hand, the polarization interactions can affect the subthreshold characteristics significantly. According to **Eq. (3)**, as K_{P} increases, $E_{\mathrm{PI}}(x)$ becomes a more negative value due to the positive $d^2P_{\mathrm{FE}}(x)/dx^2$ in the mid-channel region (where the top of the barrier is located) as shown in **Fig. 5.3(a)**, which, in turn, results in a larger negative value of $V_{\mathrm{PI}}(x)$. Consequently, the new internal voltage considering the polarization interactions ($V_{\mathrm{INT}} + V_{\mathrm{PI}}$) becomes smaller, suppressing the subthreshold current at a given voltage. Therefore, the SS can be improved as K_{P} increases, which is consistent with a previous study [51].

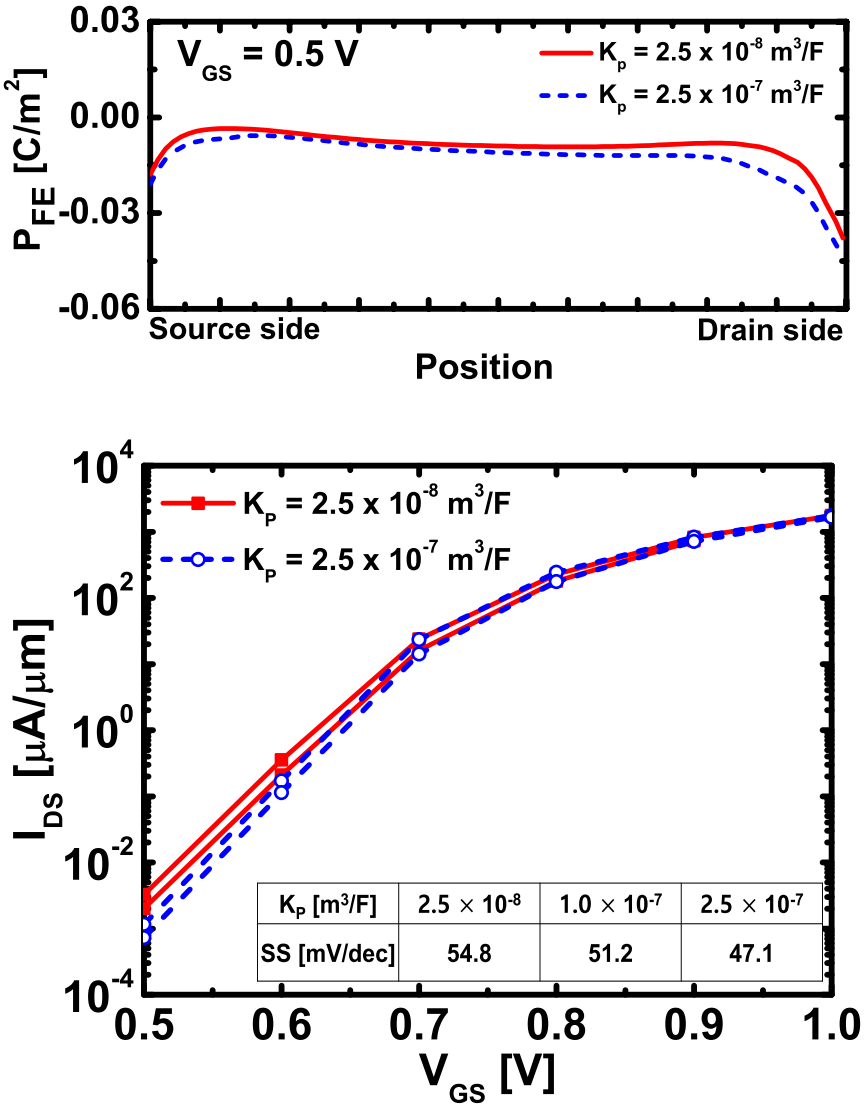


Fig. 5.3. (a) Extracted P_{FE} as a function of the position along the device within FE, where the variation of the polarization is observed. (b) $I_{DS} - V_{GS}$ characteristics of the NCFET with two different K_P values of 2.5×10^{-8} m^3/F and 2.5×10^{-7} m^3/F. Insets in (b): SS with different K_P values.

Ferroelectric thickness is one of the key parameters that can determine the overall performance of the NCFET as it significantly impacts both hysteresis and SS. Here we present two cases with different FE parameters to investigate the effect of T_{FE}: (Case 1) P_S = 0.1 C/m^2, P_R = 0.033 C/m^2, and E_C = 0.8 × 10^8 V/m for **Fig. 5.4(a)** and **5.4(b)**; (Case 2) P_S = 0.1 C/m^2, P_R = 0.075 C/m^2, and E_C = 1 × 10^8 V/m for **Fig. 5.4(c)** and **5.4(d)**. The $I_{DS} - V_{GS}$ characteristics for Case 1 and Case 2, are presented in **Fig. 5.4(a)** and **5.4(c)** respectively, with different T_{FE}. For Case 1, as T_{FE} increases, both SS and hysteresis become larger as shown in **Fig. 5.4(b)**. For case 2, the same trend in hysteresis is observed in **Fig. 5.4(d)**; however, for SS, there is a critical T_{FE} of 2 nm where SS becomes a minimum. Since SS monotonically increases with T_{FE} in Case 1 (see **Fig. 5.4(b)**), its critical T_{FE} is the thinnest T_{FE} considered, i.e., 1 nm. The existence of critical T_{FE} has already been confirmed by experiments [18], [41], [108] and can be attributed to two competing mechanisms affecting SS. As T_{FE} increases, the NC effect is enhanced, which can result in smaller SS and improved switching characteristics, as demonstrated in previous studies [77], [85], [109]. However, increasing T_{FE} also weakens the gate controllability as gate capacitance reduces, leading to an increase in SS. For Case 1, the loss in gate control overwhelms the gain in the NC effect with the increased T_{FE}, thereby increasing the SS monotonically. Nonetheless, the steep switching characteristics with sub-60 mV/dec are observed for Case 1 at $T_{FE} \leq 4$ nm. However, in Case 2, the two competing mechanisms explained above leads to a minimum SS of 27.6 mV/dec at a critical T_{FE} of 2 nm. In this case, as T_{FE} increases, the intensification of the NC effect engulfs the penalty in gate control until the critical T_{FE} is reached, after which the loss in gate control dominates. When it comes to the hysteresis, as T_{FE} increases, the hysteresis becomes larger since the coercive voltage in the stand-alone FE becomes greater.

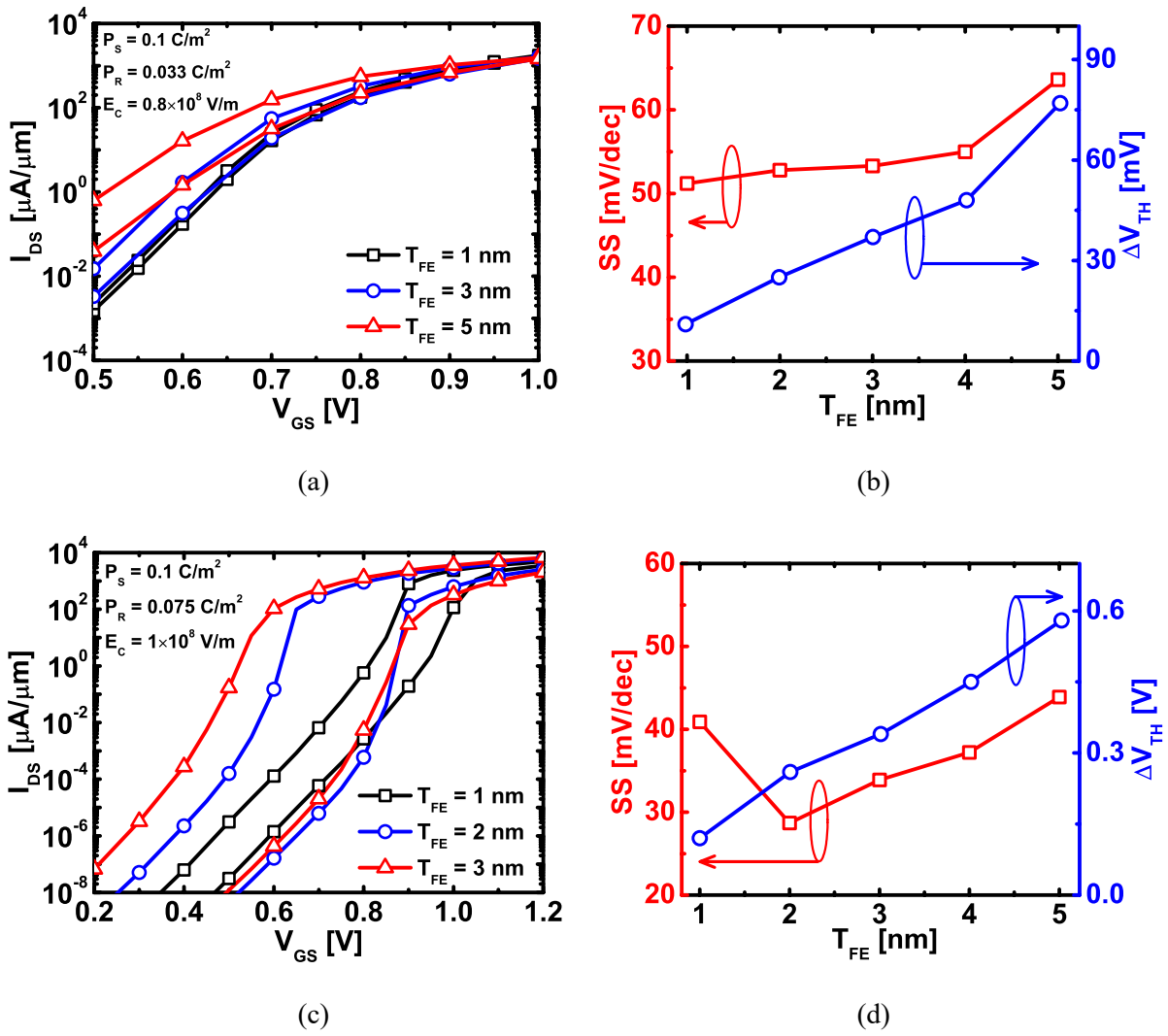
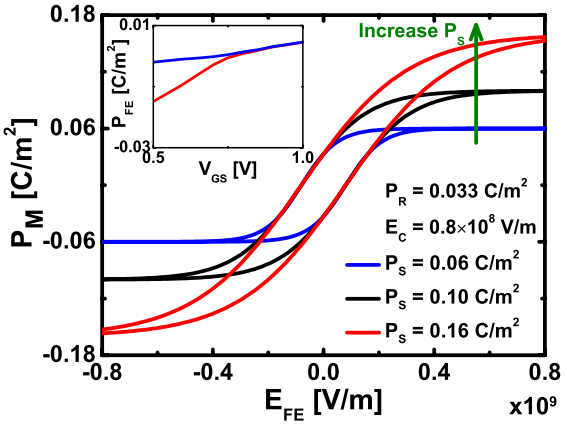
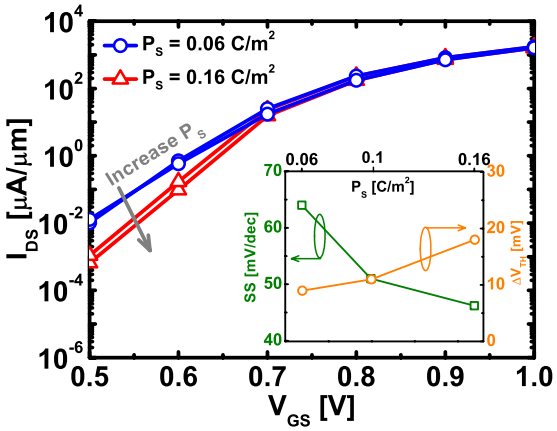


Fig. 5.4. $I_{DS} - V_{GS}$ characteristics for various T_{FE} with different FE parameters: (a) P_S = 0.1 C/m^2, P_R = 0.033 C/m^2, and E_C = 0.8×10^8 V/m with T_{FE} = 1, 3, and 5 nm and (c) P_S = 0.1 C/m^2, P_R = 0.075 C/m^2, and E_C = 1.0×10^8 V/m with T_{FE} = 1, 2, and 3 nm. (b), (d) SS and ΔV_{TH} vs. T_{FE} for (a) and (c). The critical T_{FE} of (b) 1 nm and (d) 2 nm are obtained where the NC effect is maximized for each device.

So far, we have demonstrated our model to simulate the characteristics of the NCFET (**Fig. 5.2**), discussed the effect of polarization interactions (**Fig. 5.3**), investigated the T_{FE} dependences and exhibited a critical T_{FE} for the minimum SS (**Fig. 5.4**). Aside from the T_{FE}, understanding the effect of FE parameters (i.e., P_S, P_R, and E_C) on the overall performance of the NCFET will be of great importance to properly design an NCFET using a ferroelectric layer. Therefore, we investigate the device performance by varying one material parameter within the MM at a time. **Fig. 5.5(a)–(c)** show $P_M - E_{FE}$ of the stand-alone FE with (a) P_S = 0.06, 0.1, and 0.16 C/m^2 (P_R = 0.033 C/m^2 and E_C = 0.8 × 10^8 V/m are unchanged), (b) P_R = 0.023, 0.033, and 0.043 C/m^2 (with fixed P_S = 0.1 C/m^2 and E_C = 0.8 × 10^8 V/m), and (c) E_C = 0.6 × 10^8, 0.8 × 10^8, and 1.0 × 10^8 V/m (with fixed P_S = 0.1 C/m^2 and P_R = 0.033 C/m^2) at T_{FE} = 1 nm. Highest and lowest values of the materials parameters were used to plot $I_{DS} - V_{GS}$ curves in **Fig. 5.5(d)–(f)** [(d) P_S = 0.06 and 0.16 C/m^2, (e) P_R = 0.023 and 0.043 C/m^2, and (f) E_C = 0.6×10^8 and 1.0×10^8 V/m]. The SS and hysteresis are also shown in the inset of **Fig. 5.5(d)–(f)** for each case.



(a)



(d)

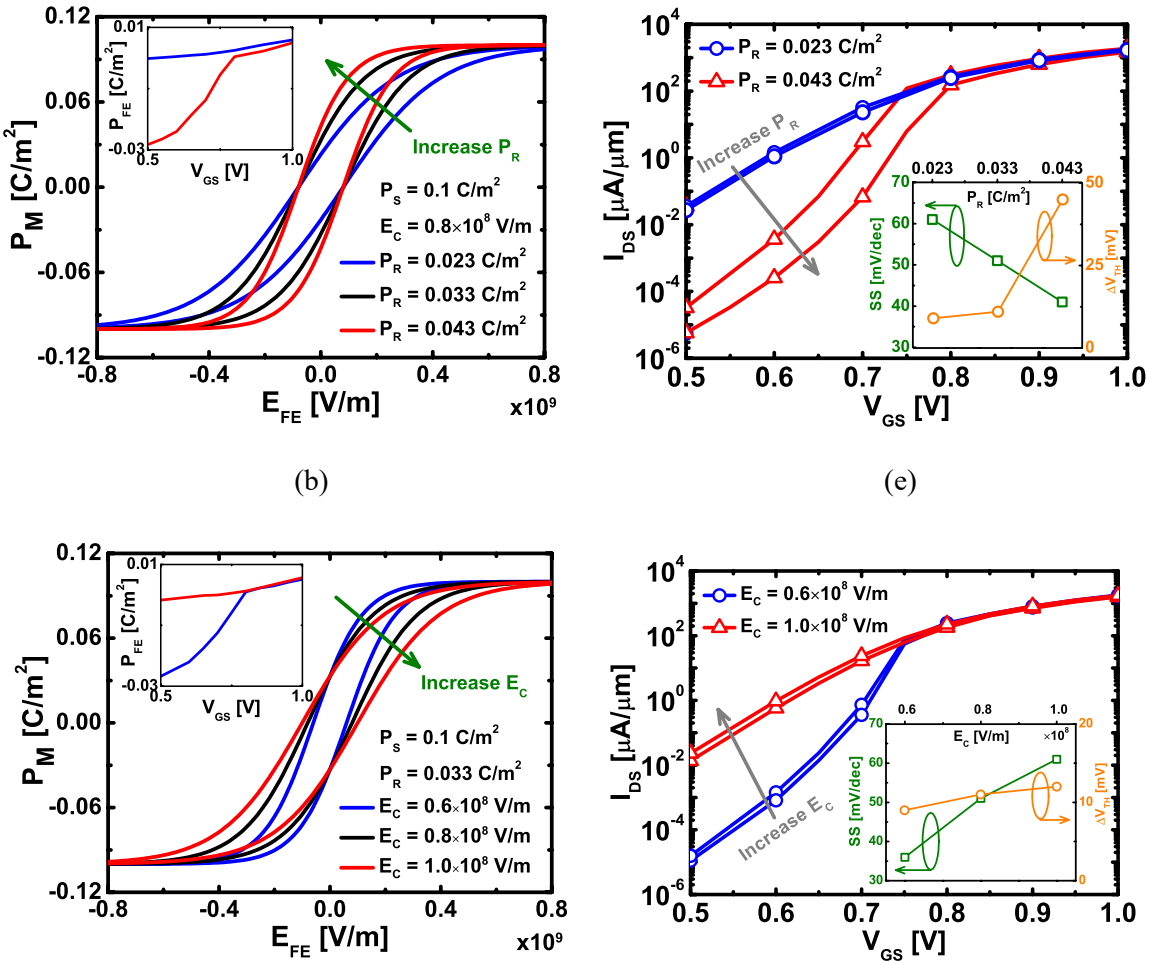


Fig. 5.5. (a)–(c) $P_{\mathrm{M}} - E_{\mathrm{FE}}$ plots for a stand-alone FE and (d)–(f) the corresponding $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ characteristics for the NCFET based on the FE shown in (a)–(c). Insets: $P_{\mathrm{FE}} - V_{\mathrm{GS}}$ plots (forward bias only) for (a) P_{S} = 0.06 C/m^2 (blue) and 0.1 C/m^2 (red), (b) P_{R} = 0.023 C/m^2 (blue) and 0.043 C/m^2 (red), and (c) E_{C} = 0.6 × 10^8 V/m (blue) and 1.0 × 10^8 V/m (red), and (d)–(f) SS and ΔV_{TH} for the $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curves shown in the main panel of (d)–(f). The following parameters are used: T_{FE} = 1 nm with (a) P_{S} = 0.06, 0.10, and 0.16 C/m^2 and (d) P_{S} = 0.06 and 0.16 C/m^2 with fixed P_{R} = 0.033 C/m^2 and E_{C} = 0.8 × 10^8 V/m; (b) P_{R} = 0.023, 0.033, and 0.043 C/m^2 and (e) P_{R} = 0.023 and 0.043 C/m^2 with fixed P_{S} = 0.1 C/m^2 and E_{C} = 0.8 × 10^8 V/m; (c) E_{C} = 0.6 × 10^8, 0.8 × 10^8, and 1.0 × 10^8 V/m and (f) E_{C} = 0.6 × 10^8 and 1.0 × 10^8 V/m with fixed P_{S} = 0.1 C/m^2 and P_{R} = 0.033 C/m^2.

To interpret the observed effect of the FE parameters on the device performance, we need to understand the internal voltage amplification at the FE/DE interface. The normal components of electric displacement for FE and DE (D_{FE} and D_{DE}) are continuous at the interface, resulting in

$$P_{\mathrm{FE}} + \varepsilon_0 \frac{V_{\mathrm{FE}}}{T_{\mathrm{FE}}} = \varepsilon_{\mathrm{DE}} \varepsilon_0 \frac{V_{\mathrm{DE}}}{T_{\mathrm{DE}}}, \tag{5}$$

where the left- and right-hand side of **Eq. (5)** represent D_{FE} and D_{DE}, respectively. By rearranging **Eq. (5)** and taking the derivative with respect to V_{GS}, we can obtain the following relation

$$\left\{\frac{\varepsilon_0}{T_{FE}} + \frac{\varepsilon_0 \varepsilon_{\mathrm{DE}}}{T_{\mathrm{DE}}}\left(1 - \frac{d\psi_{\mathrm{CH}}}{dV_{\mathrm{INT}}}\right)\right\} \frac{dV_{\mathrm{INT}}}{dV_{\mathrm{GS}}} = \frac{dP_{\mathrm{FE}}}{dV_{\mathrm{GS}}} + \frac{\varepsilon_0}{T_{\mathrm{FE}}}. \tag{6}$$

As we discussed earlier in **Eq. (4)**, steeper subthreshold slope can be achieved with larger $dV_{\mathrm{INT}}/dV_{\mathrm{GS}}$. We can see from **Eq. (6)** that $dV_{\mathrm{INT}}/dV_{\mathrm{GS}}$ monotonically increases with $dP_{\mathrm{FE}}/dV_{\mathrm{GS}}$, as the other terms are fixed for a particular FE. It should be noted that $d\psi_{\mathrm{CH}}/dV_{\mathrm{INT}}$ is also unchanged since the same base transistor is used. Therefore, the subthreshold characteristics are a strong function of $dP_{\mathrm{FE}}/dV_{\mathrm{GS}}$, which can be seen from the slope of $P_{\mathrm{FE}} - V_{\mathrm{GS}}$ curves in the inset of **Fig. 5.5(a)–(c)**. Our results show that SS becomes smaller with increasing P_{S} and P_{R} (see the inset in **Fig. 5.5(d)** and **(e)**), or decreasing E_{C} (the inset in **Fig. 5.5(f)**), as $dP_{\mathrm{FE}}/dV_{\mathrm{GS}}$ increases (the inset in **Fig. 5.5(a)–(c)**). It is also shown in the inset of **Fig. 5.5(d)–(f)** that the hysteresis of the NCFET can be suppressed with smaller values of P_{S}, P_{R}, and E_{C}, due to the smaller discrepancy in the spontaneous polarization between the forward and the reverse bias under the same electric field.

5.4 Conclusion

In this study, hysteresis-free, steep-switching characteristics of the NCFET in steady states by using the NEGF, Poisson's equation, and the MM with polarization interactions are demonstrated. In particular, I have used the MM, instead of the LM, to not only capture different transitions of polarization switching within the FE but to also capture the behavior of certain ferroelectrics that have small hysteresis and gradual polarization switching. I have also considered the polarization interactions caused by polarization variation along the device position to evaluate realistic NCFET characteristics. Simulation results show that SS is improved with stronger polarization interactions due to the suppressed internal voltage. Using the developed simulation tool, we have shown critical T_{FE} for the minimum SS and investigated its physical origin. Lastly, NCFETs by varying P_{S}, P_{R}, and E_{C} in the

MM are simulated. I have observed that the SS can be improved with larger P_S and P_R, but degrades with greater E_C. When it comes to hysteresis, smaller FE parameters are preferred to suppress the hysteresis window. This study introduces a new computational framework for gradually switching FE-based NCFETs, which enables to engineer material and device design parameters of the NCFET for performance optimization as required for different target applications.

Chapter 6
Simulation of a Partially Polarized Ferroelectric-Based Negative Capacitance FETs

6.1 Introduction

Since negative capacitance (NC) concept was conceptualized in 2008 [12], many recent experimental and theoretical studies have shown that negative capacitance (NC) can improve the subthreshold swing (SS) beyond the classical limit (i.e., SS = 60 mV/decade at room temperature) by integrating a ferroelectric layer (FE) into the base field-effect transistors (FETs) [14]–[23]. In particular, theoretical works have made an effort to support performance enhancement caused by NC of the experimental results, by modeling not only FE but NCFET [42]–[47], [49]–[51]. Even though rigid models of FE are used for NCFET simulation, it could fail to precisely predict the performance of NCFET without properly implementing the FE model into NCFET. This is mainly because the polarization (P) behavior becomes different depending on the maximum electric field applied as shown in **Fig. 6.1** originating from the partially polarized property of FE (PPFE).

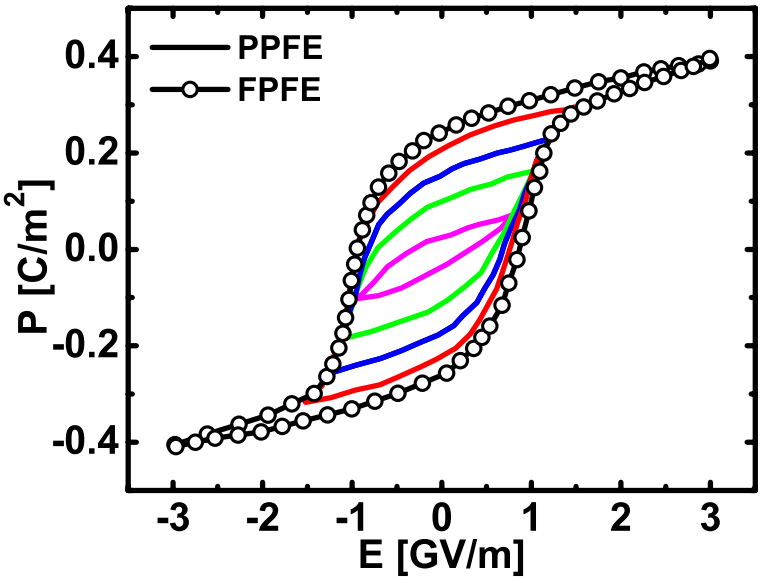


Fig. 6.1. Experimental results of polarization vs. electric field across the FE for various applied electric field bias ranges extracted from [56]. Line with symbol and solid line show the FE with assuming a fully polarized polarization (FPFE) and considering partially polarized (PPFE).

Most theoretical works assume a fully polarized FE (FPFE) that the behavior of polarization against electric field is unchanged under the different maximum electric field across the FE (E_{FE}). In other words, once the FE material is chosen, the same $P - E_{\mathrm{FE}}$ curve of FPFE (see **Fig. 6.1**) is always used regardless of the applied electric field range. However, that is far from the case when the range of electric field applied is small as shown in **Fig. 6.1**. Besides, it is reasonably ratiocinated that the polarization behavior along the direction from source to drain should be dealt with the different $P - E_{\mathrm{FE}}$, since the maximum potential differences across the FE (V_{FE}) determined by the range of applied electric field are varied by the position under the non-equilibrium bias. Therefore, different $P - E_{\mathrm{FE}}$ curves with careful consideration of the maximum applied field along the channel direction are required in the FE. Notwithstanding the importance of PPFE, the study of NCFET along with PPFE including evaluation of spatial information in steady states is missing in this field.

In this work, for the first time, we demonstrate an NCFET for PPFE by utilizing a novel approach of simulation under quasi-static gate voltage (V_{GS}) sweep. By performing a fully numerical device simulation including Poisson's equation, non-equilibrium Green's function (NEGF), and FE minor loop model with a proposed process, the differences between the NCFET assuming FPFE (FPFE-NCFET) and the NCFET considering PPFE (PPFE-NCFET) are elucidated. With the aid of the understanding of PPFE, a drain-induced barrier lowering (DIBL) in the PPFE-NCFET is investigated by comparing with the FPFE-NCFET. Lastly, the changes of DIBL are investigated under the different channel lengths (L_{CH}) and FE thickness (T_{FE}).

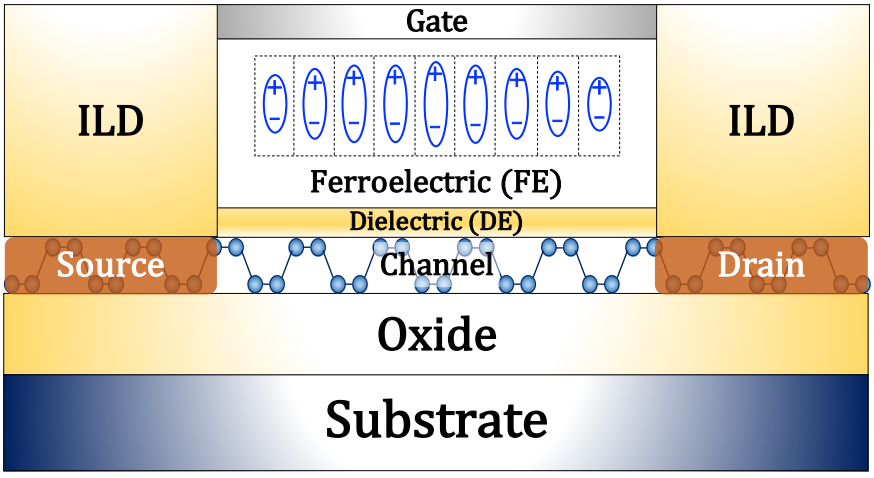
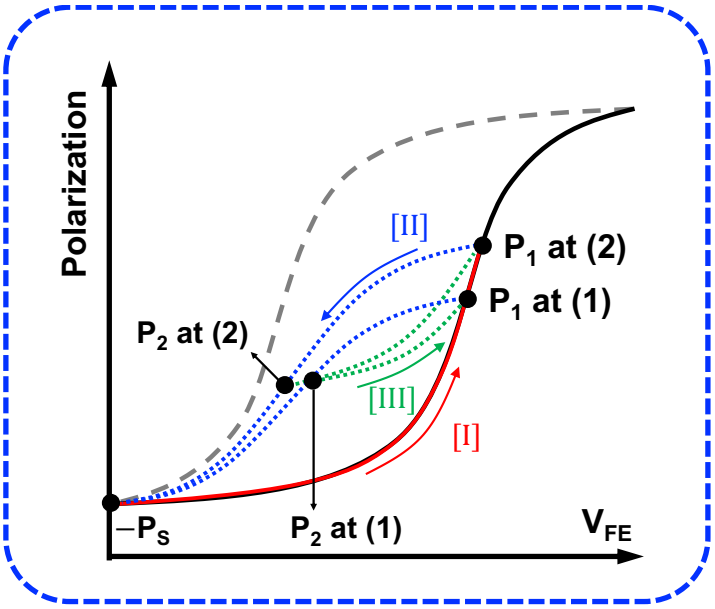


Fig. 6.2. Schematic of an NCFET used for simulations. The monolayer black phosphorus, $Hf_{0.5}Zr_{0.5}O_2$, and SiO_2 are utilized for the channel material, FE, and DE, respectively.

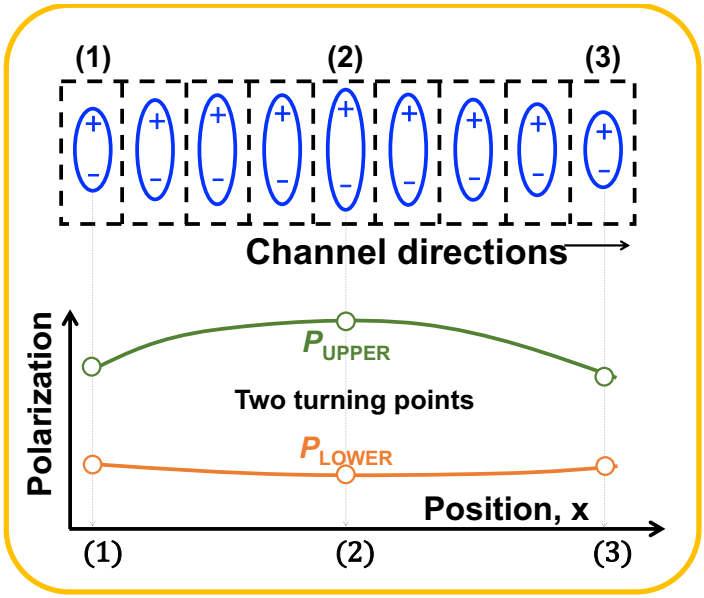
6.2 Simulation Process

Fig. 6.2 shows the schematic of NCFET simulated in this work. We have adopted monolayer black phosphorus (BP), $Hf_{0.5}Zr_{0.5}O_2$ (HZO), and SiO_2 for the channel material, FE, and dielectric layer (DE), respectively. T_{FE} and L_{CH} are 1 nm and 20 nm, respectively, unless otherwise stated. The inter-layer dielectric (ILD) is used with low-κ (κ = 2) value [105]. The source/drain length ($L_{S/D}$) and doping concentration ($N_{S/D}$) are 20 nm, and 2.6×10^{13} cm^{-2} respectively. Note that 0.5 nm of equivalent oxide thickness (EOT) is used. The FE material parameters [saturation polarization (P_{SAT}), remnant polarization (P_R), and coercive field (E_C)] can be adjusted by the maximum applied electric field calculated. Before explaining detailed simulation method, entire simulation approach is discussed.

To demonstrate PPFE-NCFET, we have reasonably assumed that the initial polarization is $-P_{SAT}$ in FPFE, so that it is able to start the simulation with the known $P - V_{FE}$ curve for FPFE as an initial guess. The entire steps are as follows.



(a)



(b)

Fig. 6.3. (a) Schematic of P vs. V_{FE} curves of the stand-alone FE to explain the process of PPFE-NCFET simulation. (b) Illustrated polarization within FE (upper) and two turning points along the x-direction (lower). $-P_{\mathrm{SAT}}$, P_1, and P_2 are turning points at a certain position within the FE [(1) and (2) shown in (b)].

STEP 1) Forward V_{GS} bias sweep from 0 V to 1.5 V (initial guess using FPFE): After initial calculation of the NCFET based on FPFE under V_{GS} range from 0 V to 1.5 V using our in-house simulation tool (details will be discussed later), the maximum value of polarization at V_{GS} of 1.5 V labeled as P_1 can be obtained through the line of [I] as shown in **Fig. 6.3(a)**. Since, in the NCFET, the polarization becomes varied along with the channel direction (x direction) due to the existence of V_G and V_D, P_1 located at (1), (2), and (3) (i.e., $P_1(x$ = (1), (2) and (3)) could be different (see **Fig. 6.3(b)**). Note that there are only P_1 at (1) and (2) in **Fig. 6.3(b)** for clarity. In this step, we have used $-P_{SAT}$ as an initial value, so that it becomes the minimum value of polarization.

From the next step, the important property of memorizing polarization history for FE should be considered. FE material can remember previous maximum and minimum value of polarization called turning points [110]. Therefore, here, $P_1(x)$ is the upper turning point denoted by $P_{UPPER}(x)$ and the lower turning point denoted by $P_{LOWER}(x)$ becomes $-P_{SAT}$. Again, it should be noted that the turning points could be varied along the x direction as shown in lower **Fig. 6.3(b)**.

STEP 2) Reverse V_{GS} bias sweep from 1.5 V to 0 V (PPFE): The range of polarization in the previous step is from $-P_{SAT}$ to $P_1(x)$. In other words, this FE can memorize $-P_{SAT}$ and $P_1(x)$ as two turning points of $P_{LOWER}(x)$ and $P_{UPPER}(x)$, respectively. In order to attain a new $P - V_{FE}$ curve for this bias sweep, an FE minor loop model considering two turning points is used as shown in **Fig. 6.4** [110]. Based on the equations in **Fig. 6.4**, new $P - V_{FE}$ plots for this step, which are different depending on the x position in FE are acquired (see the line of [II]). By separately considering the different $P - V_{FE}$ curves along the x position, the drain current and corresponding polarization can be evaluated at a given V_{GS}. Therefore, under the reverse bias sweep of V_{GS}, the polarization can move from $P_1(x)$ to $P_2(x)$ obtained at V_{GS} = 0 V through the $P - V_{FE}$ plot calculated (i.e., [II]).

STEP 3) Forward V_{GS} bias sweep from 0 V to 1.5 V (PPFE): In this step, the lower turning point that the FE layer remembers is updated to $P_2(x)$ instead of $-P_{SAT}$, since polarizations at V_{GS} = 0 V start to increase with forward bias sweep from $P_2(x)$. In the same manner, the updated $P - V_{FE}$ plots can be decided based on two turning points ($P_2(x)$ and $P_1(x)$), thereby enabling the extracted polarization to start progress toward P_1 as V_{GS} increases (see the line of [III]).

STEP 4) Repeat STEP 2 and STEP 3 until P_{UPPER} and P_{LOWER} are converged (PPFE): Through this step, the final $P - V_{FE}$ curves can be attained by repeating the forward and reverse V_{GS} bias sweep until the difference between previous and current $P - V_{FE}$ curve becomes negligible. Note that, in this work, the negligible difference is observed between STEP 2/STEP 3 and STEP 4.

To implement the proposed steps, the process of a fully numerical simulation along with the detailed equations of (i) non-equilibrium Green's function (NEGF), (ii) FE module including a FE minor loop model and polarization model with polarization interactions, and (iii) Poisson's equation are introduced as illustrated in **Fig. 6.4**. Parameters evaluated from NEGF, FE model, and Poisson's equation are self-consistently calculated throughout the proposed simulation. In particular, the FE model for PPFE that accounts for the history of turning points, minor loop trajectories, and spatial information in FE is used as described above.

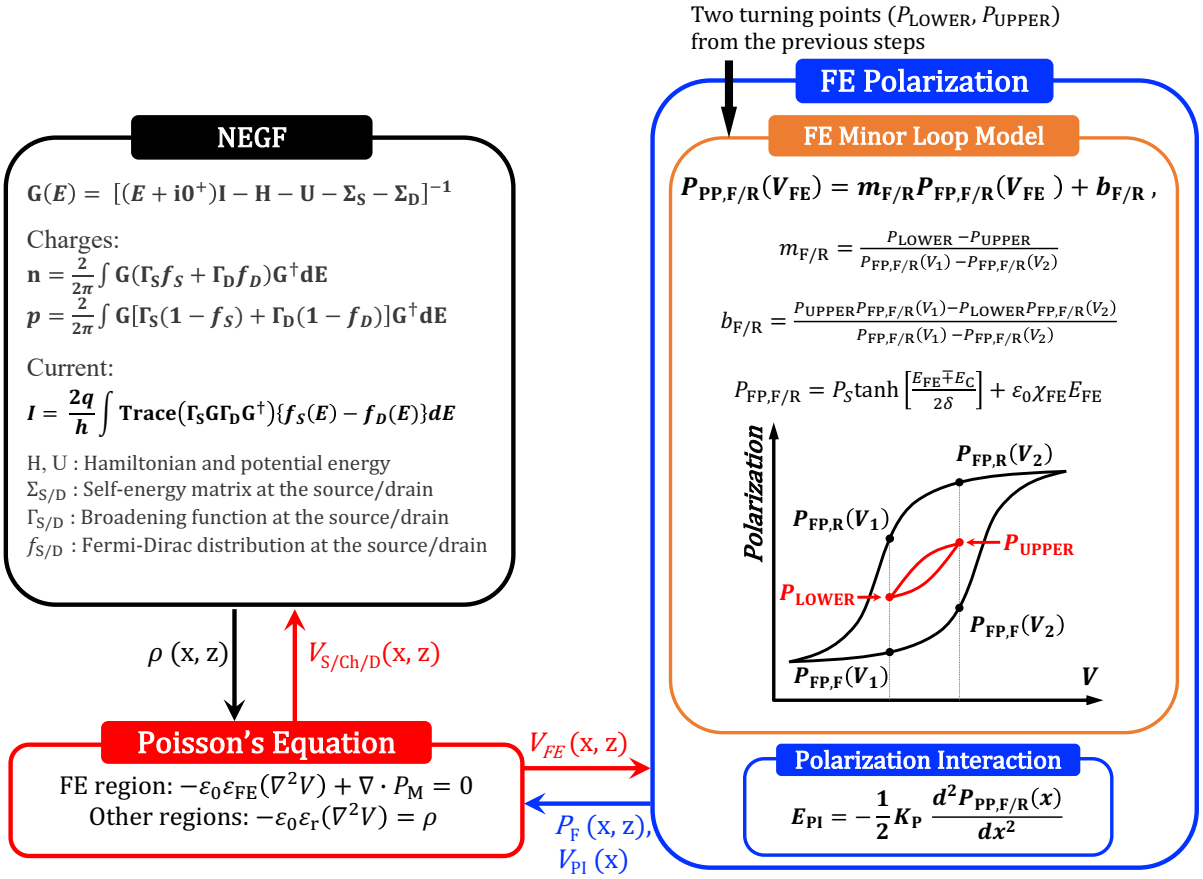


Fig. 6.4. Flowchart of the self-consistent simulation process with three modules: (i) the FE module including FE minor loop model, FE polarization model, and polarization interactions, (ii) Poisson's equation, and (iii) the NEGF. The (x, z) indicates different nodes within the device.

There are two parts of the FE module. The first part of the FE module named as the FE minor loop model [110] in **Fig. 6.4** is to update the $P - V_{\mathrm{FE}}$ depending on the aforementioned STEPs. Note that since the FPFE-NCFET is considered only for the initial calculation in STEP 1, the positive and negative P_{SAT} become $P_{\mathrm{UPPER}}(x)$ and $P_{\mathrm{LOWER}}(x)$ as inputs, respectively, to perform the FPFE simulation using FE minor loop model. For other STEPs, the inputs of $P_{\mathrm{UPPER}}(x)$ and $P_{\mathrm{LOWER}}(x)$ are determined by two turning points (STEP2: $-P_{\mathrm{SAT}}$ and $P_1(x)$, STEP3: $P_2(x)$ and $P_1(x)$). As mentioned before, two turning points are varied depending on the position of FE, since the V_{FE} is not constant under a non-equilibrium condition as shown in **Fig. 6.3(b)**. As a consequence of having different turning points along the x-direction of FE, the same number of different $P - V_{\mathrm{FE}}$ plots as the number of grid points along the position x are generated.

Using the $P_{\mathrm{UPPER}}(x)$ and $P_{\mathrm{LOWER}}(x)$, new $P - V_{\mathrm{FE}}$ curves varied by the position of x are generated. Firstly, at a certain location in the channel region, for example $x = x_0$, where x_0 can be (1) or (2) or (3) in **Fig. 6.3(b)**, let $P_{\mathrm{FP,F/R}}$ denotes the forward and reverse bias of polarization for the FPFE given by

$$P_{\mathrm{FP,F/R}}(x,z) = P_{\mathrm{SAT}} \tanh\left(\frac{E_{\mathrm{FE}}(x,z) \mp E_{\mathrm{C}}}{2\delta}\right) + \varepsilon_0 \chi_{\mathrm{FE}} E_{\mathrm{FE}}(x,z), \quad (1)$$

where $\delta = E_{\mathrm{C}}\left[\log[(1 + P_{\mathrm{R}}/P_{\mathrm{SAT}})/(1 - P_{\mathrm{R}}/P_{\mathrm{SAT}})]\right]^{-1}$. ε_0 and χ_{FE} are the permittivity of vacuum and the background susceptibility of FE [58], respectively. Note that the first term in the RHS indicates the spontaneous polarization of FE and the second term is called the background polarization meaning the rest of contributions to the total polarization ($P_{\mathrm{FP,F/R}}$). Since the PPFE along the thickness shares the turning points which is a function of x position only, $P_{\mathrm{PP,F/R}}$ within the thickness along the x-direction ($P_{\mathrm{PP,F/R}}(x)$) is calculated with the average $P_{\mathrm{FP,F/R}}$ along the thickness ($P_{\mathrm{FP,F/R}}(x)$). Here, the assumption of using average $P_{\mathrm{FP,F/R}}$ is reasonable due to the thin FE layer considered. We then introduce the equation for PPFE (see **Fig. 6.4**) as

$$P_{\mathrm{PP,F/R}}(v_{\mathrm{FE}}) = m_{\mathrm{F/R}} \times P_{\mathrm{FP,F/R}}(v_{\mathrm{FE}}) + b_{\mathrm{F/R}}, \quad (2)$$

where

$$m_{\mathrm{F/R}} = \frac{P_{\mathrm{LOWER}} - P_{\mathrm{UPPER}}}{P_{\mathrm{FP,F/R}}(V_1) - P_{\mathrm{FP,F/R}}(V_2)} \tag{3}$$

and

$$b_{\mathrm{F/R}} = \frac{P_{\mathrm{UPPER}} P_{\mathrm{FP,F/R}}(V_1) - P_{\mathrm{LOWER}} P_{\mathrm{FP,F/R}}(V_2)}{P_{\mathrm{FP,F/R}}(V_1) - P_{\mathrm{FP,F/R}}(V_2)}. \tag{4}$$

The v_{FE} here denotes the range of V_{FE} used for the FE minor loop model (from V_1 to V_2, where V_1 and V_2 are the potential at the two turning points). Based on **Eq. 2**, the updated $P - v_{\mathrm{FE}}$ are generated as an output of the FE minor loop model, thereby attaining different $P - v_{\mathrm{FE}}$ curves determined by the STEP. The second part of the PPFE module is the FE polarization model. The main role of the FE polarization model is to find P under a given potential within the FE calculated from Poisson's equation by taking the $P - v_{\mathrm{FE}}$ curves generated from the FE minor loop model. After evaluating the polarization, the electric field induced by the interaction between adjacent polarizations is estimated by the equation as [51]

$$E_{\mathrm{PI}}(x) = -\frac{1}{2} K_{\mathrm{P}} \frac{d^2 P_{\mathrm{PP,F/R}}(x)}{dx^2},$$

where K_{P} is the interaction coefficient. The effect of polarization interaction is incorporated with the proposed simulation process by accepting V_{PI} (i.e., $V_{\mathrm{PI}} = E_{\mathrm{PI}} \times T_{\mathrm{FE}}$) in the Poisson module. After which the interface condition between FE and DE in the Poisson module is updated to $V_{\mathrm{INT}} + V_{\mathrm{PI}}$, where V_{INT} is the potential at the interface between FE and DE.

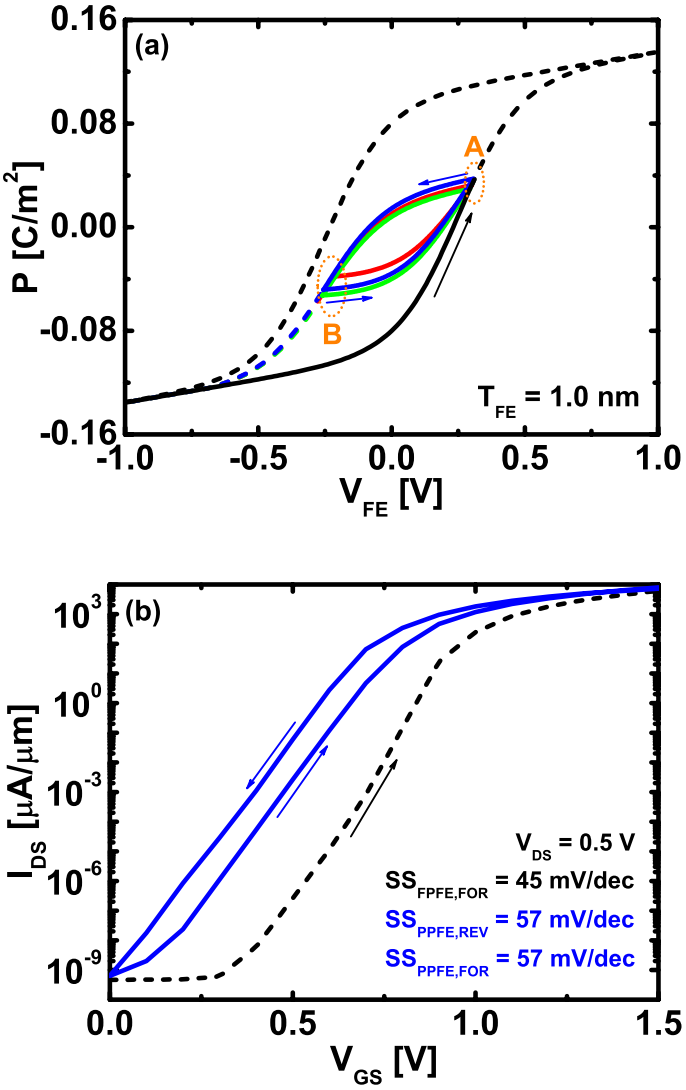


Fig. 6.5. (a) Simulated P vs. V_{FE} curves for the FE of FPFE (P_{SAT} = 0.1 C/m^2, P_R = 0.033 C/m^2, and E_C = 0.8×10^8 V/m) and PPFE. The point A and B denotes the turning points used during the simulation steps. (b) Simulated $I_{DS} - V_{GS}$ plots of forward bias sweep for the FPFE-NCFET and forward and reverse bias sweeps for the PPFE-NCFET with the T_{FE} = 1 nm. Both sweep directions show the steep switching characteristics.

Through the Poisson's equation, the potential profile in the FE can be evaluated by using $-\varepsilon_0\varepsilon_{\mathrm{FE}}(\nabla^2 V) + \nabla \cdot P_{\mathrm{M}} = 0$, where $P_{\mathrm{M}} = P_{\mathrm{PP,F/R}} - \varepsilon_0\chi_{\mathrm{FE}}E_{\mathrm{FE}}$ and $\varepsilon_{\mathrm{FE}} = \chi_{\mathrm{FE}} + 1$ (meaning the permittivity of the background FE). For other regions, we have used $-\varepsilon_0\varepsilon_{\mathrm{r}}(\nabla^2 V) = \rho$, where ε_{r} and ρ are relative permittivity and charge density, respectively. Only the semiconductor region has non-zero value of ρ. Lastly, in the BP channel region, ballistic transports are calculated through the NEGF method [61] with a tight-binding approximation [60].

6.3 Results and Discussion

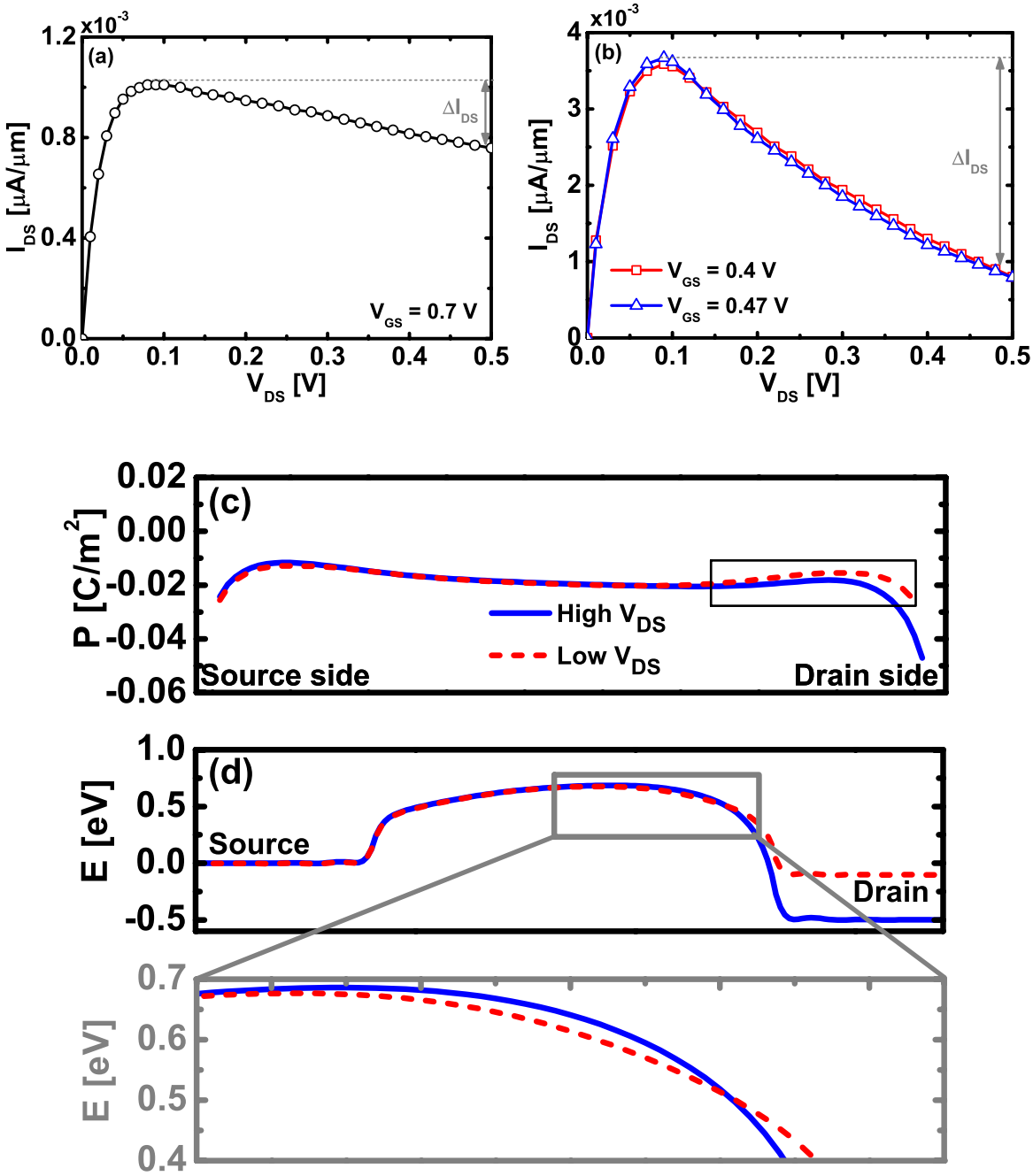
Fig. 6.5(a) shows the simulated polarization as a function of V_{FE} for the stand-alone FE of FPFE (black solid and dashed lines) and PPFE (colored solid and dashed line). For the FPFE-NCFET used in this work, the material parameters (i.e., P_{SAT}, P_{R}, and E_{C}) have been chosen based on reasonable range of material parameters from the experimental results as follows: P_{SAT} = 0.1 C/m^2, P_{R} = 0.08 C/m^2, and E_{C} = 2.5 × 10^8 V/m [20]. Note that K_{P} is 1 × 10^{-7} m^3/F [51].

By adopting the $P - V_{\mathrm{FE}}$ for the FPFE (see the black lines in **Fig. 6.5(a)**), the black dashed line of simulated drain current (I_{DS}) – gate voltage (V_{GS}) from the initial forward gate bias sweep (V_{GS} = 0 V to 1.5 V) is shown in **Fig. 6.5(b)**. Once the first gate bias sweep approaches 1.5 V, the polarization reaches the maximum value on the solid black line, labelled as A in **Fig. 6.5(a)**, which becomes the first $P_{\mathrm{UPPER}}(x)$. Note that, as already mentioned, the maximum value could be different depending on the position in FE along the x-direction (i.e., A(x)).

Once the reverse bias sweep (V_{GS} = 1.5 V to 0 V) is applied, the polarization can start moving from the first $P_{\mathrm{UPPER}}(x)$ in **Fig. 6.5(a)**. Since the A(x) and $-P_{\mathrm{SAT}}$ are memorized as two turning points, the colored lines for the reverse bias are generated by calculating the equations in the FE minor loop model. Different colored lines represent $P - V_{\mathrm{FE}}$ curves for the different position. We have employed the reverse bias of $P - V_{\mathrm{FE}}$ curves to obtain its transfer characteristics as shown the blue solid line with the reverse bias sweep direction in **Fig. 6.5(b)**. In this step, as the V_{GS} decreases until V_{GS} is reached at V_{GS} = 0 V, the polarization proceeds up to a certain polarization value where the minimum value denoted as B in **Fig. 6.5(a)** is attained through the reverse bias.

Based on the results of the previous reverse bias sweep, two turning points that FE layer remembers become $\mathrm{B}(x)$ and $\mathrm{A}(x)$, which corresponds to $P_{\mathrm{LOWER}}(x)$ and $P_{\mathrm{UPPER}}(x)$. In the same manner as explained in the simulation process, the updated P vs. V_{FE} curve can be attained as shown in **Fig. 6.5(a)** (forward bias of colored line), resulting in obtaining the $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curve calculated using the updated $P - V_{\mathrm{FE}}$ curve (forward bias of blue curve in Fig. **6.5(b)**). Note that in spite of carrying out more forward and reverse bias sweep of simulation, the negligible difference is observed, resulting in gaining the complete set of simulation for PPFE. The minimum SS from FPFE- and two PPFE-NCFETs (reverse and forward bias) are 45 mV/dec, 57 mV/dec, and 57 mV/dec, respectively. The discrepancy of SS between FPFE and PPFE is originating from a given $P - V_{\mathrm{FE}}$ curve used. According to the previous work [101], SS can be improved with a steeper slope of polarization switching so that the FPFE-NCFET shows steeper SS.

Both FPFE and PPFE-NCFET manifest steep switching characteristics emanated from NC. The NC operation can be identified by observing the negative DIBL (FPFE: ~ -16 mV/V and PPFE: ~ -71 mV/V). Here, there is a huge disagreement between two negative DIBL values. To elucidate negative DIBL effect, energy barrier heights between high V_{DS} and low V_{DS} at the same V_{GS} can be generally examined. Since the energy barrier height can determine the amount of I_{DS} at a given condition, I_{DS} varied with different V_{DS} at a given V_{GS} is investigated to understand and compare the negative DIBL between FPFE- and PPFE-NCFET in **Fig. 6.6**. We have repeatedly simulated $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curve with different V_{DS} values (from 0 V to 0.5 V) and taken corresponding I_{DS} values to obtain $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ at a certain V_{GS}. This method is acceptable when the negative DIBL is investigated. It should be noted that in order to study a negative differential resistance (NDR), an $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ with new $P - V_{\mathrm{FE}}$ considering drain bias sweep is required, which is suggested for future studies. Therefore, study of negative DIBL is only carried out in this work.


x10^-3
(a)
ΔI_DS
V_GS = 0.7 V
I_DS [μA/μm]
V_DS [V]
x10^-3
(b)
ΔI_DS
V_GS = 0.4 V
V_GS = 0.47 V
I_DS [μA/μm]
V_DS [V]
(c)
High V_DS
Low V_DS
Source side
Drain side
P [C/m^2]
(d)
Source
Drain
E [eV]
E [eV]

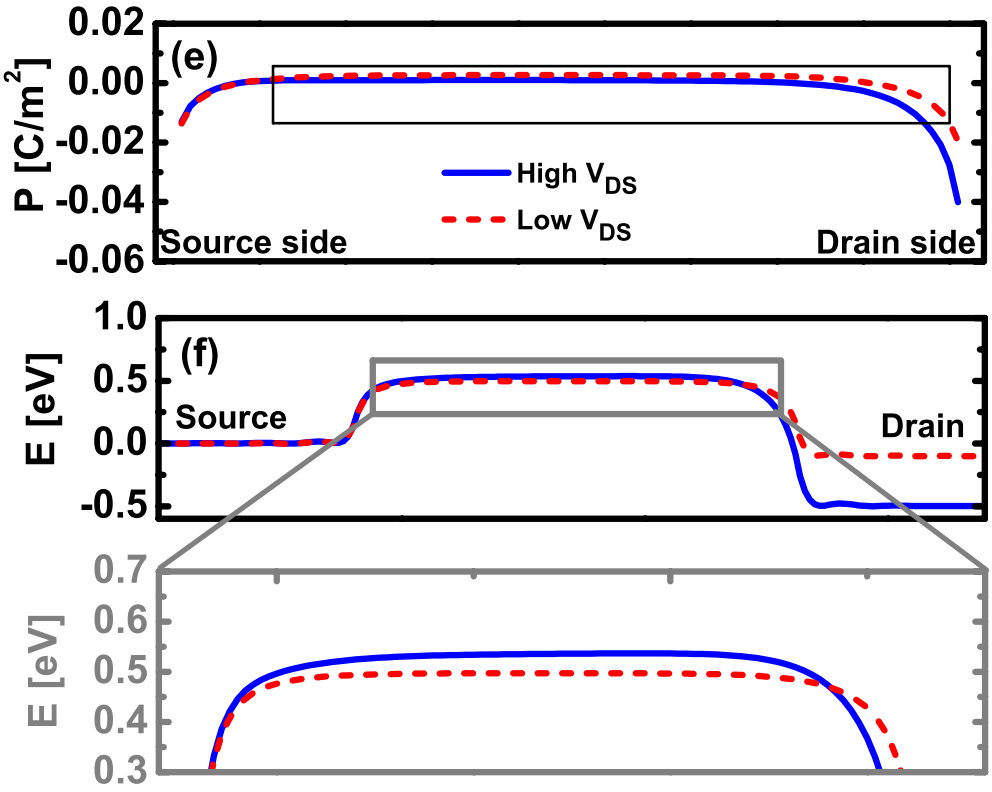


Fig. 6.6. I_{DS} as a function of V_{DS} for the (a) FPFE-NCFET and (b) PPFE-NCFET (blue: forward bias sweep and red: reverse bias sweep), which is measured at (a) V_{GS} = 0.7 V and (b) V_{GS} = 0.47 V (forward) and V_{GS} = 0.4 V (reverse), respectively. Note that those V_{GS}s are the gate voltage where I_{DS} is 1 × 10^{-3} μA/μm. P and E (conduction band edge) vs. x-direction with V_{DS} = 0.5 V (high V_{DS}) and V_{DS} = 0.1 V (low V_{DS}) for (c, d) FPFE and (e, f) PPFE (reverse only).

Fig. 6.6(a) and **6.6(b)** show the I_{DS} as a function of V_{DS} at a V_{GS} where I_{DS} = 1 × 10^{-3} μA/μm (i.e., V_{GS} = 0.7 V for FPFE and V_{GS} = 0.4V/0.47 V for PPFE (reverse/forward bias) in **Fig. 6.5(b)**. The negative DIBL can be observed in both FPFE and PPFE, which is caused by the NC effect. To understand the impact of drain voltage on both FPFE and PPFE, ΔI_{DS} is defined as the current difference between the maximum value of I_{DS} and I_{DS} at V_{DS} of 0.5 V, which implies that ΔI_{DS} is

directly proportional to the energy barrier height differences in energy band diagram. In the case of FPFE, the I_{DS} is reduced by ~ 20 %, when V_{DS} is varied from 0.1 V (low V_{DS}) to 0.5 V (high V_{DS}). Whereas we have observed a huge decrease of I_{DS} between V_{DS} = 0.1 V and 0.5 V (reduced by ~ 72 %) for the PPFE.

To elucidate the reason why the negative DIBL from PPFE-NCFET becomes severe compared to that from FPFE-NCFET, the polarization (**Fig. 6.6(c)** and **6.6(e)**) and the conduction band edge (E) (**Fig. 6.6(d)** and **6.6(f)**) as a function of position along the channel direction for FPFE and PPFE (reverse bias only) are examined. Note that the blue solid line and red dashed line represent high and low V_{DS}. As the V_{DS} increases, the attribute of the drain voltage on the channel region is greater, leading to a negatively increase of the polarization. **Fig. 6.5(a)** manifests that the magnitude of P in FPFE is larger than that in PPFE. Since a larger polarization value from the FPFE-NCFET, which tends to more suppress or amplify the voltage caused by NC, assists the gate to control the channel [101], the energy barrier of the channel in the FPFE-NCFET is more governed by the gate than that in the PPFE-NCFET. Hence, the E in the FPFE-NCFET can be modified only at the channel close to the drain-side (see **Fig. 6.6(d)** with a zoomed plot), when the drain voltage is varied. Unlike the FPFE-NCFET, however, the E in the PPFE-NCFET is likely to shift in the entire channel region due to the lack of the impact of polarization on the channel as shown in **Fig. 6.6(f)** with a zoomed plot. Consequently, PPFE-NCFET is more vulnerable to the variation of drain voltage, which results in the larger negative DIBL.

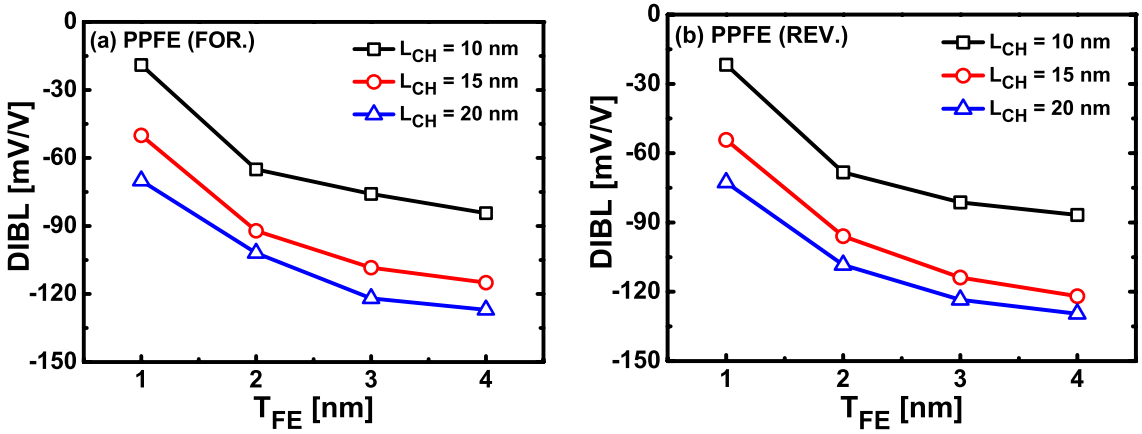


Fig. 6.7. DIBL vs. T_{FE} curves in the (a) forward bias and (b) reverse bias PPFE-NCFET for L_{CH} = 10 nm (black), 15 nm (red), and 20 nm (blue). Both results show the negative DIBL.

Fig. 6.7 shows the DIBL in the **(a)** forward- and **(b)** reverse-biased PPFE-NCFET as a function of T_{FE} for various L_{CH}. For both V_{GS} sweep directions, as L_{CH} shrinks, the short channel effect overpowers the negative DIBL effect. On the other hand, when T_{FE} becomes thicker, the NC effect is enhanced, resulting in gaining more negative DIBL. However, increasing T_{FE} also weakens the gate controllability due to worsening the gate capacitance, which leads to push towards the positive DIBL. In conclusion, the loss in gate controllability originating from thick T_{FE} suppresses the growth rate of the negative DIBL.

6.4 Conclusion

PPFE-NCFET using the novel approach is demonstrated with the proposed steps under the quasi-static V_{GS} sweep. By calculating three modules including NEGF, Poisson's equation, and MM-based FE minor loop model, the difference between the FPFE-NCFET and PPFE-NCFET is investigated. I have observed that the SS of PPFE-NCFET is less steep than FPFE-NCFET due to gently varied polarization transition. Besides, the DIBL from the PPFE-NCFET shows more negative value than that from the FPFE-NCFET, since PPFE-NCFET is more vulnerable to the drain voltage changes, caused by smaller value of polarization. Finally, L_{CH} and T_{FE} in the PPFE-NCFET are varied to investigate their effects on DIBL. Simulation results show that short L_{CH} suppresses the negative DIBL due to the short channel effect. On the other hand, even though thick T_{FE} can strengthen the negative DIBL effect, the growth rate become decreased by losing gate controllability.

Chapter 7
Summary and Future Works

7.1 Summary

In this dissertation, firstly, the hysteretic jump point of FE-MOS capacitor is modeled using LM to engineer the hysteresis by examining ψ_s–V_{G} curve based on the Gibbs free energy of the entire device. This simulation result shows that hysteretic jump points can be varied by modifying design parameters (e.g., T_{FE}, EOT and N_{SC}). Both hysteresis height and width can be effectively tuned by T_{FE} and EOT but N_{SC} is less susceptible. For thin HZO, however, they can also be influenced by N_{SC}. It is anticipated that this proposed hysteretic jump point model can provide a useful engineering tool to adjust hysteresis to satisfy the requirement of hysteresis window depending on the target applications.

Next, the MM is employed to surmount the limitation of the LM when a so-called "S-curve" is used to fit $P - E_{\mathrm{FE}}$ curve, since the MM can precisely describe the transition of polarization switching. By self-consistently simulating an FE-DE capacitor, the static NC characteristics are demonstrated using the MM nevertheless the $P - E_{\mathrm{FE}}$ curve showing a 'positive slope'. The origin of NC effect caused by depolarization field is explored by elucidating the variation of spontaneous polarization, electric field and voltage across the FE under different applied voltages. It was observed that a greater NC effect with larger hysteresis can be obtained as T_{FE} becomes thicker. Besides, FE materials with different transitions of polarization switching are simulated by adjusting material parameters of FE with the MM to investigate the impact of FE material on the NC effect. The result shows that using FE, exhibiting more abrupt switching transition, within the FE-DE capacitor can enhance the NC effect. Especially, as P_{R} becomes larger, greater internal voltage amplification can be attained. In the case when FE has larger P_{SAT}, the NC effect is observed for a wider range of V_{APP}. When it comes to the hysteresis, P_{SAT} shows a minor impact on hysteresis but smaller P_R and E_C are preferred to suppress the hysteresis. It is suggested that more complicated NCFET structure can be investigated by applying the proposed novel computational framework established on the MM.

Therefore, in the next chapter, NCFETs employing the novel computational framework are demonstrated by means of a fully numerical, self-consistent simulation based on the NEGF, Poisson's equation, and the MM with polarization interactions, resulting in gaining hysteresis-free and steep switching characteristics in steady states. In contrast to the LM, MM is used to capture the FE

manifesting different polarization switching transition as well as small hysteresis with gradual polarization switching. In the FE module, the polarization interactions originating from the variation of polarization along the device are considered to evaluate the performance of NCFET more precisely. The simulation result related the polarization interaction shows that better SS characteristics are shown with stronger interactions due to the suppressed internal voltage. Throughout the developed simulation tool, the critical T_{FE} where SS becomes a minimum is observed, which is confirmed by experiments. Subsequently, I have simulated NCFETs for different material parameters so that SS becomes steeper with greater P_{S} and P_{R}, while greater E_{C} can deteriorate SS. With regard to hysteresis, the requirement of narrow hysteresis is to reduce FE material parameters. A new computational framework for NCFET enables to tune design parameters of material and device for performance optimization as required for target applications.

Lastly, a more realistic behavior of FE that could be varied by the maximum applied electric field due to a PPFE is considered by adopting a new approach in this chapter. Three main modules including NEGF, Poisson's equation, and MM-based FE minor loop model are self-consistently calculated to compare the difference between the FPFE-NCFET and PPFE-NCFET. The SS of FPFE-NCFET is overestimated as compared with that of PPFE-NCFET, caused by steeper polarization switching transition. Also, the result shows that the PPFE-NCFET is more susceptible to the changes from drain voltage, which can result in more negative DIBL observed in PPFE-NCFET than FPFE-NCFET. Subsequently, the effects of L_{CH} and T_{FE} in the PPFE-NCFET on DIBL are investigated, so that the negative DIBL can be strengthened with thicker T_{FE}, but its growth rate is declined by losing gate controllability. The study in this chapter establishes a new approach for PPFE-NCFET, leading to predict and support experiments more accurately.

7.2 Suggested Future Works

7.2.1 Modeling of Polycrystalline FE

In this dissertation, ferroelectric HZO is mainly used to demonstrate and investigate FE-based devices from a FE-DE capacitor to NCFET. A single crystal FE is assumed in entire work, since a model to accurately implement FE into the base device is needed to understand how FE-based device can be affected by NC effect first. However, the polycrystalline nature of HZO is confirmed through

various experiments [111]–[113], so that the FE with multiple grains should be considered for the next advanced model. Besides, it is possible for the polycrystalline FE material to contain multiple phases including DE which shows non-FE property [114], [115]. Consequently, the polycrystalline FE model can be further extended by implementing the mixture of FE and DE property within FE layer.

7.2.2 FE Model Considering Defects

FE layers used in this dissertation are treated as a defect-free. However, defects within the FE could affect the potential profile, resulting in obtaining different behaviors of polarization. For example, the voltage amplification in a FE-DE capacitor device could be varied by not only the number of defects but also its position. In addition, when it comes to NCFET, the position of defect is important to determine the performance of NCFET, since the defect within FE could modify the channel potential. Therefore, different performance could be expected between defect positions located (at the center and side of FE). Theoretical modeling of defect effects on the FE-device could provide in-depth understanding to predict its performance.

7.2.3 Modeling of Negative Capacitance in Antiferroelectric Material

An antiferroelectric material contains spontaneous polarization oriented in antiparallel directions between adjacent polarizations, which can result in zero net polarization measured at zero applied field as shown in **Fig. 7.1**. Interestingly, there are two possible NC regions located separately at $P \neq 0$ unlike FE (see **Fig. 7.2**). Double hysteresis can be utilized for memory applications and the NC region can be employed for low-power logic applications by achieving sub-60 mV/dec SS at room temperature. Moreover, the reported studies indicate that higher endurance can be observed in AFE [116], [117].

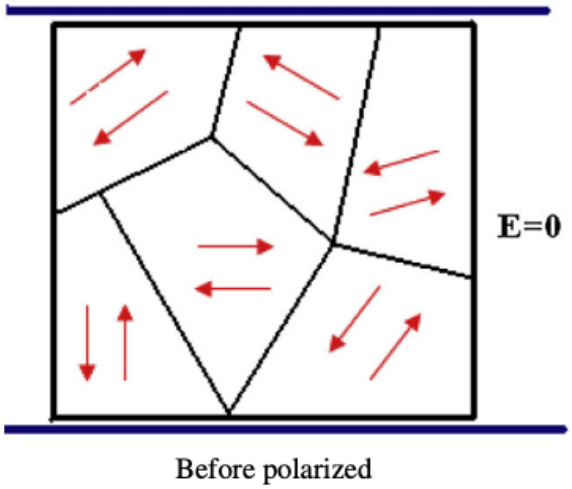


Fig. 7.1. The schematic of polarization orientation of AFEs [118].

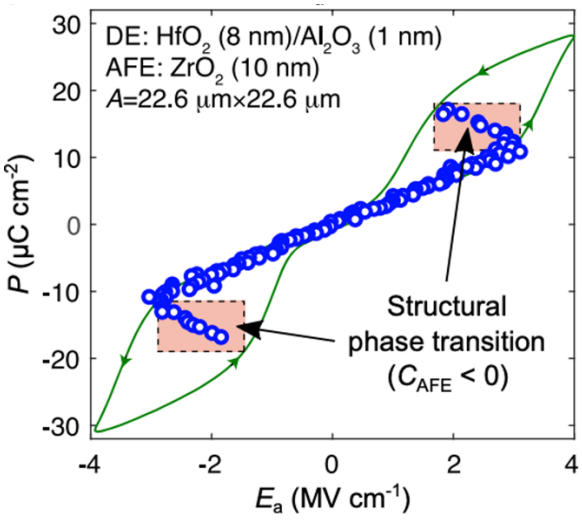


Fig. 7.2. Measured polarization as a function of extracted electric field across the AFE in a DE-AFE capacitor [119].

For the future work, firstly, a study of AFE switching dynamics could reveal the transient NC effect from domain nucleation and propagation mechanism using phase-field modeling. Besides, the AFE switching dynamics could be altered by different DE materials in AFE-DE heterostructures. Hence, the transient AFE modeling could attribute to providing more insights for the understanding of AFE. Next,

a static NC from AFE, which is the main mechanism of potential amplification is needed to explore by investigating 1) AFE-DE capacitors and 2) AFE-based NCFETs for the low-power logic application. Demonstration of the proposed devices would be helpful to understand the physics behind it and to support the experimental works.

References

[1] G. E. Moore, “Cramming more components onto integrated circuits,” *Electronics*, vol. 38, no. 8, 1965, doi: 10.1109/n-ssc.2006.4785860.

[2] S. E. Thompson *et al.*, “A 90-nm Logic Technology Featuring Strained-Silicon,” *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, Nov. 2004, doi: 10.1109/TED.2004.836648.

[3] K. Mistry *et al.*, “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging,” in *2007 IEEE International Electron Devices Meeting*, Dec. 2007, pp. 247–250, doi: 10.1109/IEDM.2007.4418914.

[4] C.-H. Jan *et al.*, “A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications,” in *2012 International Electron Devices Meeting*, Dec. 2012, pp. 3.1.1-3.1.4, doi: 10.1109/IEDM.2012.6478969.

[5] R. Xie *et al.*, “A 7nm FinFET technology featuring EUV patterning and dual strained high mobility channels,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, vol. 12, no. c, pp. 2.7.1-2.7.4, doi: 10.1109/IEDM.2016.7838334.

[6] N. Loubet *et al.*, “Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET,” in *2017 Symposium on VLSI Technology*, Jun. 2017, vol. 5, no. 1, pp. T230–T231, doi: 10.23919/VLSIT.2017.7998183.

[7] K. Rupp, “42 Years of Microprocessor Trend Data.” https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/.

[8] S.-H. Chen, “Next to FinFET, How Will ESD Suffer?” https://incompliancemag.com/article/next-to-finfet-how-will-esd-suffer/.

[9] C. Convertino, C. B. Zota, H. Schmid, A. M. Ionescu, and K. E. Moselund, “III–V heterostructure tunnel field-effect transistor,” *J. Phys. Condens. Matter*, vol. 30, no. 26, p. 264005, Jul. 2018, doi: 10.1088/1361-648X/aac5b4.

[10] C. Convertino *et al.*, “A hybrid III–V tunnel FET and MOSFET technology platform integrated on silicon,” *Nat. Electron.*, vol. 4, no. 2, pp. 162–170, Feb. 2021, doi:

10.1038/s41928-020-00531-3.

[11] H. K. Sung, H. Kam, C. Hu, and T. J. K. Liu, “Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF},” *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 178–179, 2009.

[12] S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices,” *Nano Lett.*, vol. 8, no. 2, pp. 405–410, Feb. 2008, doi: 10.1021/nl071804g.

[13] “A century of ferroelectricity,” *Nat. Mater.*, vol. 19, no. 2, pp. 129–129, Feb. 2020, doi: 10.1038/s41563-020-0611-1.

[14] Z. Krivokapic *et al.*, “14nm Ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, pp. 15.1.1-15.1.4, doi: 10.1109/IEDM.2017.8268393.

[15] J. Jo and C. Shin, “Negative capacitance field effect transistor with hysteresis-free sub-60-mV/decade switching,” *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 245–248, 2016, doi: 10.1109/LED.2016.2523681.

[16] M. Si *et al.*, “Steep-slope hysteresis-free negative capacitance MoS2 transistors,” *Nat. Nanotechnol.*, vol. 13, no. 1, pp. 24–28, Jan. 2018, doi: 10.1038/s41565-017-0010-1.

[17] K.-S. Li *et al.*, “Sub-60mV-swing negative-capacitance FinFET without hysteresis,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2015, pp. 22.6.1-22.6.4, doi: 10.1109/IEDM.2015.7409760.

[18] M. H. Lee *et al.*, “Physical thickness 1.x nm ferroelectric HfZrOx negative capacitance FETs,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, pp. 12.1.1-12.1.4, doi: 10.1109/IEDM.2016.7838400.

[19] M. H. Lee *et al.*, “Extremely Steep Switch of Negative-Capacitance Nanosheet GAA-FETs and FinFETs,” in *2018 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2018, pp. 31.8.1-31.8.4, doi: 10.1109/IEDM.2018.8614510.

[20] M. H. Lee *et al.*, “Prospects for ferroelectric HfZrOx FETs with experimentally CET=0.98nm, SSfor=42mV/dec, SSrev=28mV/dec, switch-off 0.2V, and hysteresis-free strategies,” in *2015*

IEEE International Electron Devices Meeting (IEDM), Dec. 2015, pp. 22.5.1-22.5.4, doi: 10.1109/IEDM.2015.7409759.

[21] M.-Y. Kao, G. Pahwa, A. Dasgupta, S. Salahuddin, and C. Hu, "Analysis and Modeling of Polarization Gradient Effect on Negative Capacitance FET," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4521–4525, Oct. 2020, doi: 10.1109/TED.2020.3013569.

[22] Y.-H. Liao, D. Kwon, Y.-K. Lin, A. J. Tan, C. Hu, and S. Salahuddin, "Anomalously Beneficial Gate-Length Scaling Trend of Negative Capacitance Transistors," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1860–1863, Nov. 2019, doi: 10.1109/LED.2019.2940715.

[23] Y.-K. Lin *et al.*, "Spacer Engineering in Negative Capacitance FinFETs," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 1009–1012, Jun. 2019, doi: 10.1109/LED.2019.2911104.

[24] J. F. Ihlefeld, D. T. Harris, R. Keech, J. L. Jones, J.-P. Maria, and S. Trolier-McKinstry, "Scaling Effects in Perovskite Ferroelectrics: Fundamental Limits and Process-Structure-Property Relations," *J. Am. Ceram. Soc.*, vol. 99, no. 8, pp. 2537–2557, Aug. 2016, doi: 10.1111/jace.14387.

[25] T. Tybell, C. H. Ahn, and J.-M. Triscone, "Ferroelectricity in thin perovskite films," *Appl. Phys. Lett.*, vol. 75, no. 6, pp. 856–858, Aug. 1999, doi: 10.1063/1.124536.

[26] J. Junquera and P. Ghosez, "Critical thickness for ferroelectricity in perovskite ultrathin films," *Nature*, vol. 422, no. 6931, pp. 506–509, Apr. 2003, doi: 10.1038/nature01501.

[27] D. D. Fong *et al.*, "Ferroelectricity in Ultrathin Perovskite Films," *Science*, vol. 304, no. 5677, pp. 1650–1653, Jun. 2004, doi: 10.1126/science.1098252.

[28] N. Sai, A. M. Kolpak, and A. M. Rappe, "Ferroelectricity in ultrathin perovskite films," *Phys. Rev. B*, vol. 72, no. 2, p. 020101, Jul. 2005, doi: 10.1103/PhysRevB.72.020101.

[29] J. Müller *et al.*, "Ferroelectricity in simple binary ZrO2 and HfO2," *Nano Lett.*, vol. 12, no. 8, pp. 4318–4323, 2012, doi: 10.1021/nl302049k.

[30] H. Agarwal *et al.*, "Engineering Negative Differential Resistance in NCFETs for Analog Applications," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 2033–2039, May 2018, doi: 10.1109/TED.2018.2817238.

[31] H. Zhou *et al.*, "Negative Capacitance, n-Channel, Si FinFETs: Bi-directional Sub-60 mV/dec,

Negative DIBL, Negative Differential Resistance and Improved Short Channel Effect," in *2018 IEEE Symposium on VLSI Technology*, Jun. 2018, pp. 53–54, doi: 10.1109/VLSIT.2018.8510691.

[32] T. Yu, W. Lü, Z. Zhao, P. Si, and K. Zhang, "Negative drain-induced barrier lowering and negative differential resistance effects in negative-capacitance transistors," *Microelectronics J.*, vol. 108, no. May 2020, p. 104981, Feb. 2021, doi: 10.1016/j.mejo.2020.104981.

[33] A. Rusu, G. A. Salvatore, D. Jimenez, and A. M. Ionescu, "Metal-Ferroelectric-Meta-Oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification," in *2010 International Electron Devices Meeting*, Dec. 2010, pp. 16.3.1-16.3.4, doi: 10.1109/IEDM.2010.5703374.

[34] J. Jo, W. Y. Choi, J. D. Park, J. W. Shim, H. Y. Yu, and C. Shin, "Negative Capacitance in Organic/Ferroelectric Capacitor to Implement Steep Switching MOS Devices," *Nano Lett.*, vol. 15, no. 7, pp. 4553–4556, 2015, doi: 10.1021/acs.nanolett.5b01130.

[35] A. I. Khan *et al.*, "Negative Capacitance in Short-Channel FinFETs Externally Connected to an Epitaxial Ferroelectric Capacitor," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 111–114, Jan. 2016, doi: 10.1109/LED.2015.2501319.

[36] S. Dasgupta *et al.*, "Sub-kT/q Switching in Strong Inversion in $PbZr_{0.52}Ti_{0.48}O_3$ Gated Negative Capacitance FETs," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, no. April, pp. 43–48, 2015, doi: 10.1109/jxcdc.2015.2448414.

[37] C. Liu, H.-H. Chen, C.-C. Hsu, C.-C. Fan, H.-H. Hsu, and C.-H. Cheng, "Negative Capacitance CMOS Field-Effect Transistors with Non-Hysteretic Steep Sub-60mV/dec Swing and Defect-Passivated Multidomain Switching," in *2019 Symposium on VLSI Technology*, Jun. 2019, vol. 2019-June, pp. T224–T225, doi: 10.23919/VLSIT.2019.8776482.

[38] K. Chatterjee, A. J. Rosner, and S. Salahuddin, "Intrinsic speed limit of negative capacitance transistors," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1328–1330, Sep. 2017, doi: 10.1109/LED.2017.2731343.

[39] Bin Yu *et al.*, "FinFET scaling to 10 nm gate length," in *Digest. International Electron Devices Meeting,* 2002, vol. 00, no. 100, pp. 251–254, doi: 10.1109/IEDM.2002.1175825.

[40] D. Kwon *et al.*, "Response Speed of Negative Capacitance FinFETs," in *2018 IEEE*

Symposium on VLSI Technology, Jun. 2018, pp. 49–50, doi: 10.1109/VLSIT.2018.8510626.

[41] K.-S. Li *et al.*, "Negative-Capacitance FinFET Inverter, Ring Oscillator, SRAM Cell, and Ft," in *2018 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2018, pp. 31.7.1-31.7.4, doi: 10.1109/IEDM.2018.8614521.

[42] D. Jimenez, E. Miranda, and A. Godoy, "Analytic Model for the Surface Potential and Drain Current in Negative Capacitance Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2405–2409, Oct. 2010, doi: 10.1109/TED.2010.2062188.

[43] H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur, "Modeling and Design of Ferroelectric MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2401–2405, Aug. 2011, doi: 10.1109/TED.2011.2155067.

[44] H. Ota, T. Ikegami, J. Hattori, K. Fukuda, S. Migita, and A. Toriumi, "Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, pp. 12.4.1-12.4.4, doi: 10.1109/IEDM.2016.7838403.

[45] G. Pahwa *et al.*, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance—Part I: Model Description," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4981–4985, Dec. 2016, doi: 10.1109/TED.2016.2614432.

[46] G. Pahwa *et al.*, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance—Part II: Model Validation," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4986–4992, Dec. 2016, doi: 10.1109/TED.2016.2614436.

[47] S. Khandelwal, J. P. Duarte, A. I. Khan, S. Salahuddin, and C. Hu, "Impact of parasitic capacitance and ferroelectric parameters on negative capacitance FinFET characteristics," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 142–144, 2017, doi: 10.1109/LED.2016.2628349.

[48] M. Kobayashi and T. Hiramoto, "Device design guideline for steep slope ferroelectric FET using negative capacitance in sub-0.2V operation: Operation speed, material requirement and energy efficiency," in *2015 Symposium on VLSI Technology (VLSI Technology)*, Jun. 2015,

pp. T212–T213, doi: 10.1109/VLSIT.2015.7223678.

[49] M. Hoffmann, M. Pesic, S. Slesazeck, U. Schroeder, T. Mikolajick, and T. Mikolajick, "Modeling and design considerations for negative capacitance field-effect transistors," in *2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, Apr. 2017, vol. 2, pp. 1–4, doi: 10.1109/ULIS.2017.7962577.

[50] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Nonhysteresis and Hysteresis Regimes: MFMIS Versus MFIS Structures," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 867–873, 2018, doi: 10.1109/TED.2018.2794499.

[51] A. K. Saha, P. Sharma, I. Dabo, S. Datta, and S. K. Gupta, "Ferroelectric transistor model based on self-consistent solution of 2D Poisson's, non-equilibrium Green's function and multi-domain Landau Khalatnikov equations," in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, pp. 13.5.1-13.5.4, doi: 10.1109/IEDM.2017.8268385.

[52] A. K. Saha, M. Si, K. Ni, S. Datta, P. D. Ye, and S. K. Gupta, "Ferroelectric Thickness Dependent Domain Interactions in FEFETs for Memory and Logic: A Phase-field Model based Analysis," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, pp. 4.3.1-4.3.4, doi: 10.1109/IEDM13553.2020.9372099.

[53] A. K. Saha and S. K. Gupta, "Negative capacitance effects in ferroelectric heterostructures: A theoretical perspective," *J. Appl. Phys.*, vol. 129, no. 8, p. 080901, Feb. 2021, doi: 10.1063/5.0038971.

[54] A. K. Saha and S. K. Gupta, "Multi-Domain Ferroelectric FETs with Negative and Enhanced Positive Capacitance for Logic Applications," in *2021 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2021, pp. 77–80, doi: 10.1109/SISPAD54002.2021.9592573.

[55] L. Landau and I. Khalatnikov, "On the anomalous absorption of sound near a second order phase transition point," *Dokl. Akad. Nawk SSSR*, vol. 96, pp. 469–472, 1954.

[56] A. K. Saha, K. Ni, S. Dutta, S. Datta, and S. Gupta, "Phase field modeling of domain dynamics and polarization accumulation in ferroelectric HZO," *Appl. Phys. Lett.*, vol. 114, no.

20, p. 202903, May 2019, doi: 10.1063/1.5092707.

[57] S. L. Miller, R. D. Nasby, J. R. Schwank, M. S. Rodgers, and P. V. Dressendorfer, “Device modeling of ferroelectric capacitors,” *J. Appl. Phys.*, vol. 68, no. 12, pp. 6463–6471, Dec. 1990, doi: 10.1063/1.346845.

[58] A. P. Levanyuk, B. A. Strukov, and A. Cano, “Background dielectric permittivity: Material constant or fitting parameter?,” *Ferroelectrics*, vol. 503, no. 1, pp. 94–103, Oct. 2016, doi: 10.1080/00150193.2016.1218245.

[59] Z. Ren, “Nanoscale MOSFETs: Physics, simulation, and design,” Purdue University, 2001.

[60] A. N. Rudenko and M. I. Katsnelson, “Quasiparticle band structure and tight-binding model for single and bilayer black phosphorus,” *Phys. Rev. B*, vol. 89, no. 20, p. 201408, May 2014, doi: 10.1103/PhysRevB.89.201408.

[61] S. Datta, *Quantum Transport: Atom to Transistor*. Cambridge: Cambridge University Press, 2005.

[62] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, “Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors,” *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196805, Nov. 2004, doi: 10.1103/PhysRevLett.93.196805.

[63] H. Kam, T.-J. K. Liu, V. Stojanović, D. Markovic, and E. Alon, “Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic,” *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 236–250, Jan. 2011, doi: 10.1109/TED.2010.2082545.

[64] A. Sharma and K. Roy, “1T Non-Volatile Memory Design Using Sub-10nm Ferroelectric FETs,” *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 359–362, Mar. 2018, doi: 10.1109/LED.2018.2797887.

[65] X. Li *et al.*, “Enabling Energy-Efficient Nonvolatile Computing With Negative Capacitance FET,” *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3452–3458, 2017, doi: 10.1109/TED.2017.2716338.

[66] Z. Wang *et al.*, “Experimental Demonstration of Ferroelectric Spiking Neurons for Unsupervised Clustering,” in *2018 IEEE International Electron Devices Meeting (IEDM)*, 2018, pp. 13.3.1-13.3.4, doi: 10.1109/IEDM.2018.8614586.

[67] G. Pahwa, A. Agarwal, and Y. S. Chauhan, “Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior,” *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5130–5136, Nov. 2018, doi: 10.1109/TED.2018.2870519.

[68] X. Zhang, X. Gong, and G. Liang, “Effects of scalability and floating metal on NCFETs based on a real-space atomic model,” *Semicond. Sci. Technol.*, vol. 33, no. 8, p. 08LT01, Jul. 2018, doi: 10.1088/1361-6641/aace45.

[69] A. K. Saha, S. Datta, and S. K. Gupta, “‘Negative capacitance’ in resistor-ferroelectric and ferroelectric-dielectric networks: Apparent or intrinsic?,” *J. Appl. Phys.*, vol. 123, no. 10, p. 105102, Mar. 2018, doi: 10.1063/1.5016152.

[70] Z. Dong and J. Guo, “A Simple Model of Negative Capacitance FET With Electrostatic Short Channel Effects,” *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2927–2934, 2017, doi: 10.1109/TED.2017.2706182.

[71] J. Zhou *et al.*, “Ferroelectric HfZrOx Ge and GeSn PMOSFETs with Sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved Ids,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 12.2.1-12.2.4, doi: 10.1109/IEDM.2016.7838401.

[72] J. Zhou *et al.*, “Comparative Study of Negative Capacitance Ge pFETs With HfZrOx Partially and Fully Covering Gate Region,” *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4838–4843, 2017, doi: 10.1109/TED.2017.2762926.

[73] J. Zhou *et al.*, “Hysteresis Reduction in Negative Capacitance Ge PFETs Enabled by Modulating Ferroelectric Properties in $HfZrO_X$,” *IEEE J. Electron Devices Soc.*, vol. 6, pp. 41–48, 2018, doi: 10.1109/JEDS.2017.2764678.

[74] M. Kumar and S. Jit, “A Novel Four-Terminal Ferroelectric Tunnel FET for Quasi-Ideal Switch,” *IEEE Trans. Nanotechnol.*, vol. 14, no. 4, pp. 600–602, 2015, doi: 10.1109/TNANO.2015.2427195.

[75] M. Kumar and S. Jit, “Effects of Electrostatically Doped Source/Drain and Ferroelectric Gate Oxide on Subthreshold Swing and Impact Ionization Rate of Strained-Si-on-Insulator Tunnel Field-Effect Transistors,” *IEEE Trans. Nanotechnol.*, vol. 14, no. 4, pp. 597–599, 2015, doi:

10.1109/TNANO.2015.2426316.

[76] W. Chung, M. Si, and P. D. Ye, “Hysteresis-free negative capacitance germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, pp. 15.3.1-15.3.4, doi: 10.1109/IEDM.2017.8268395.

[77] H. Lee, Y. Yoon, and C. Shin, “Current-Voltage Model for Negative Capacitance Field-Effect Transistors,” *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 669–672, 2017, doi: 10.1109/LED.2017.2679102.

[78] A. I. Khan, C. W. Yeung, Chenming Hu, and S. Salahuddin, “Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation,” in *2011 International Electron Devices Meeting*, Dec. 2011, pp. 11.3.1-11.3.4, doi: 10.1109/IEDM.2011.6131532.

[79] S.-C. Chang, U. E. Avci, D. E. Nikonov, and I. A. Young, “A Thermodynamic Perspective of Negative-Capacitance Field-Effect Transistors,” *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 3, pp. 56–64, 2017, doi: 10.1109/JXCDC.2017.2750108.

[80] C.-I. Lin, A. I. Khan, S. Salahuddin, and C. Hu, “Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics,” *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2197–2199, 2016, doi: 10.1109/TED.2016.2514783.

[81] K. Majumdar, S. Datta, and S. P. Rao, “Revisiting the Theory of Ferroelectric Negative Capacitance,” *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2043–2049, 2016, doi: 10.1109/TED.2016.2544813.

[82] T. Rollo and D. Esseni, “Energy Minimization and Kirchhoff’s Laws in Negative Capacitance Ferroelectric Capacitors and MOSFETs,” *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 814–817, 2017, doi: 10.1109/LED.2017.2691002.

[83] A. Saeidi, F. Jazaeri, I. Stolichnov, and A. M. Ionescu, “Double-Gate Negative-Capacitance MOSFET With PZT Gate-Stack on Ultra Thin Body SOI: An Experimentally Calibrated Simulation Study of Device Performance,” *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4678–4684, 2016, doi: 10.1109/TED.2016.2616035.

[84] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. Cambridge University Press, 2009.

[85] A. Sharma and K. Roy, “Design Space Exploration of Hysteresis-Free HfZrOx -Based Negative Capacitance FETs,” *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1165–1167, Aug. 2017, doi: 10.1109/LED.2017.2714659.

[86] M. Si *et al.*, “Sub-60 mV/dec ferroelectric HZO MoS_2 negative capacitance field-effect transistor with internal metal gate: The role of parasitic capacitance,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, vol. 6, pp. 23.5.1-23.5.4, doi: 10.1109/IEDM.2017.8268447.

[87] Z. Yu *et al.*, “Negative capacitance 2D MoS_2 transistors with sub-60mV/dec subthreshold swing over 6 orders, 250 μA/μm current density, and nearly-hysteresis-free,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, vol. 17, no. 8, pp. 23.6.1-23.6.4, doi: 10.1109/IEDM.2017.8268448.

[88] M. H. Lee *et al.*, “Ferroelectric negative capacitance hetero-tunnel field-effect-transistors with internal voltage amplification,” in *2013 IEEE International Electron Devices Meeting*, Dec. 2013, pp. 4.5.1-4.5.4, doi: 10.1109/IEDM.2013.6724561.

[89] A. I. Khan *et al.*, “Negative capacitance in a ferroelectric capacitor,” *Nat. Mater.*, vol. 14, no. 2, pp. 182–186, Feb. 2015, doi: 10.1038/nmat4148.

[90] A. Islam Khan *et al.*, “Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures,” *Appl. Phys. Lett.*, vol. 99, no. 11, p. 113501, Sep. 2011, doi: 10.1063/1.3634072.

[91] W. Gao *et al.*, “Room-Temperature Negative Capacitance in a Ferroelectric–Dielectric Superlattice Heterostructure,” *Nano Lett.*, vol. 14, no. 10, pp. 5814–5819, Oct. 2014, doi: 10.1021/nl502691u.

[92] D. J. R. Appleby *et al.*, “Experimental Observation of Negative Capacitance in Ferroelectrics at Room Temperature,” *Nano Lett.*, vol. 14, no. 7, pp. 3864–3868, Jul. 2014, doi: 10.1021/nl5017255.

[93] G. Pahwa, A. Agarwal, and Y. S. Chauhan, “Numerical investigation of short-channel effects in negative capacitance MFIS and MFMIS transistors: Above-threshold behavior,” *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1591–1598, 2019, doi: 10.1109/TED.2019.2892186.

[94] J. P. Duarte *et al.*, “Compact models of negative-capacitance FinFETs: Lumped and distributed charge models,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, vol. 5, no. 2, pp. 30.5.1-30.5.4, doi: 10.1109/IEDM.2016.7838514.

[95] B. Obradovic, T. Rakshit, R. Hatcher, J. A. Kittl, and M. S. Rodder, “Modeling Transient Negative Capacitance in Steep-Slope FeFETs,” *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5157–5164, Nov. 2018, doi: 10.1109/TED.2018.2868479.

[96] C. Jin, T. Saraya, T. Hiramoto, and M. Kobayashi, “Transient Negative Capacitance as Cause of Reverse Drain-induced Barrier Lowering and Negative Differential Resistance in Ferroelectric FETs,” in *2019 Symposium on VLSI Technology*, Jun. 2019, vol. 2019-June, pp. T220–T221, doi: 10.23919/VLSIT.2019.8776583.

[97] Y.-K. Lin *et al.*, “Analysis and Modeling of Inner Fringing Field Effect on Negative Capacitance FinFETs,” *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2023–2027, Apr. 2019, doi: 10.1109/TED.2019.2899810.

[98] J. C. Wong and S. Salahuddin, “Negative Capacitance Transistors,” *Proc. IEEE*, vol. 107, no. 1, pp. 49–62, 2019, doi: 10.1109/JPROC.2018.2884518.

[99] E. Ko, H. Lee, Y. Goh, S. Jeon, and C. Shin, “Sub-60-mV/decade Negative Capacitance FinFET With Sub-10-nm Hafnium-Based Ferroelectric Capacitor,” *IEEE J. Electron Devices Soc.*, vol. 5, no. 5, pp. 306–309, Sep. 2017, doi: 10.1109/JEDS.2017.2731401.

[100] H. Lee and Y. Yoon, “Modeling of Hysteretic Jump Points in Ferroelectric MOS Capacitors,” *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 3093–3098, 2019, doi: 10.1109/ted.2019.2915084.

[101] H. Lee and Y. Yoon, “Simulation of Negative Capacitance Based on the Miller Model: Beyond the Limitation of the Landau Model,” *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 237–241, Jan. 2022, doi: 10.1109/TED.2021.3124475.

[102] P. Sharma *et al.*, “Impact of total and partial dipole switching on the switching slope of gate-last negative capacitance FETs with ferroelectric hafnium zirconium oxide gate stack,” in *2017 Symposium on VLSI Technology*, Jun. 2017, no. Il, pp. T154–T155, doi: 10.23919/VLSIT.2017.7998160.

[103] C. Jin, T. Saraya, T. Hiramoto, and M. Kobayashi, “On the Physical Mechanism of Transient

Negative Capacitance Effect in Deep Subthreshold Region," *IEEE J. Electron Devices Soc.*, vol. 7, no. December 2018, pp. 368–374, 2019, doi: 10.1109/JEDS.2019.2899727.

[104] B. Obradovic, T. Rakshit, R. Hatcher, J. A. Kittl, and M. S. Rodder, "Ferroelectric Switching Delay as Cause of Negative Capacitance and the Implications to NCFETs," in *2018 IEEE Symposium on VLSI Technology*, Jun. 2018, vol. 2018-June, no. 272, pp. 51–52, doi: 10.1109/VLSIT.2018.8510628.

[105] *More Moore White Paper-International Roadmap for Devices and Systems*, 2016, http://irds.ieee.org/reports.

[106] A. N. Rudenko, S. Yuan, and M. I. Katsnelson, "Toward a realistic description of multilayer black phosphorus: From GW approximation to large-scale tight-binding simulations," *Phys. Rev. B*, vol. 92, no. 8, p. 085419, Aug. 2015, doi: 10.1103/PhysRevB.92.085419.

[107] D. Yin and Y. Yoon, "Design strategy of two-dimensional material field-effect transistors: Engineering the number of layers in phosphorene FETs," *J. Appl. Phys.*, vol. 119, no. 21, p. 214312, Jun. 2016, doi: 10.1063/1.4953256.

[108] X. Liu *et al.*, "MoS2 Negative-Capacitance Field-Effect Transistors with Subthreshold Swing below the Physics Limit," *Adv. Mater.*, vol. 30, no. 28, p. 1800932, Jul. 2018, doi: 10.1002/adma.201800932.

[109] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Compact model for ferroelectric negative capacitance transistor with MFIS structure," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1366–1374, 2017, doi: 10.1109/TED.2017.2654066.

[110] B. Jiang, P. Zurcher, R. E. Jones, S. J. Gillespie, and J. C. Lee, "Computationally efficient ferroelectric capacitor model for circuit simulation," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 141–142, 1997, doi: 10.1109/vlsit.1997.623738.

[111] M. H. Lee *et al.*, "Steep Slope and Near Non-Hysteresis of FETs With Antiferroelectric-Like HfZrO for Low-Power Electronics," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 294–296, Apr. 2015, doi: 10.1109/LED.2015.2402517.

[112] C.-Y. Liao *et al.*, "Multibit Ferroelectric FET Based on Nonidentical Double HfZrO2 for High-Density Nonvolatile Memory," *IEEE Electron Device Lett.*, vol. 42, no. 4, pp. 617–620, Apr. 2021, doi: 10.1109/LED.2021.3060589.

[113] W.-C. Chen *et al.*, “Performance Improvement by Modifying Deposition Temperature in HfZrOx Ferroelectric Memory,” *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 3838–3842, Aug. 2021, doi: 10.1109/TED.2021.3093256.

[114] Y.-T. Tang *et al.*, “A Comprehensive Study of Polymorphic Phase Distribution of Ferroelectric-Dielectrics and Interfacial Layer Effects on Negative Capacitance FETs for Sub-5 nm Node,” in *2018 IEEE Symposium on VLSI Technology*, Jun. 2018, vol. 2018-June, no. 9, pp. 45–46, doi: 10.1109/VLSIT.2018.8510696.

[115] M. H. Park *et al.*, “Ferroelectricity and Antiferroelectricity of Doped Thin HfO2-Based Films,” *Adv. Mater.*, vol. 27, no. 11, pp. 1811–1831, Mar. 2015, doi: 10.1002/adma.201404531.

[116] M. Pesic, U. Schroeder, S. Slesazeck, and T. Mikolajick, “Comparative study of reliability of ferroelectric and anti-ferroelectric memories,” *IEEE Trans. Device Mater. Reliab.*, vol. 18, no. 2, pp. 154–162, 2018, doi: 10.1109/TDMR.2018.2829112.

[117] M. Pesic *et al.*, “Anti-ferroelectric ZrO2, an enabler for low power non-volatile 1T-1C and 1T random access memories,” *Eur. Solid-State Device Res. Conf.*, pp. 160–163, 2017, doi: 10.1109/ESSDERC.2017.8066616.

[118] X. Hao, J. Zhai, L. B. Kong, and Z. Xu, “A comprehensive review on the progress of lead zirconate-based antiferroelectric materials,” *Prog. Mater. Sci.*, vol. 63, pp. 1–57, 2014, doi: https://doi.org/10.1016/j.pmatsci.2014.01.002.

[119] M. Hoffmann *et al.*, “Antiferroelectric negative capacitance from a structural phase transition in zirconia,” *Nat. Commun.*, vol. 13, no. 1, p. 1228, Dec. 2022, doi: 10.1038/s41467-022-28860-1.

[120] H. Lee, M. Sritharan, and Y. Yoon, “A Computational Framework for Gradually Switching Ferroelectric-Based Negative Capacitance Field-Effect Transistors,” *IEEE Trans. Electron Devices*, 2022, doi: 10.1109/TED.2022.3197387 (accepted).