# Monolithic Amorphous-Selenium/CMOS Small-Pixel-Effect-Enhanced Single-Photon-Counting Imagers for Dedicated Breast Computed Tomography

by

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## Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

## Abstract

Breast cancer is the most common cause of cancer-related death in women in the world. However, early and reliable detection of breast cancer can reduce its high fatality rate. Diagnosis hinges on medical X-ray imaging techniques like screen-film mammography and digital mammography, which are burdened by false positives, increased radiation exposure, and patient discomfort due to breast compression. Conversely, three-dimensional (3-D) imaging modalities, like magnetic resonance imaging and digital breast tomosynthesis, aim to reduce false positives but have several limitations, including high cost, patient discomfort, and difficulties imaging dense breast tissue.

Alternatively, dedicated breast computed tomography (DBCT) with a single-photon-counting (SPC) detector offers 3-D imaging without breast compression and lower radiation exposure, but faces challenges related to the fabrication of the X-ray sensor. Commonly-used X-ray-sensor materials for SPC detectors are silicon (Si), cadmium zinc telluride (CZT), and cadmium telluride (CdTe). However, Si has low detection efficiency and poly-crystalline CZT and CdTe face yield issues due to the bump-bonding process needed for integration with a complementary metal-oxide-semiconductor (CMOS) readout integrated circuit (ROIC).

An alternative to these materials for monolithic X-ray SPC imagers is amorphous selenium (a-Se), a well-established X-ray-sensitive material. While the use of an a-Se sensor is more cost-effective for large-area deposition, the major drawbacks of a-Se are its limited temporal and energy resolution, preventing its use in detectors for DBCT.

In this thesis, we tackle the intrinsic limitations of a-Se and demonstrate, for the first time, the potential of a monolithic a-Se/CMOS X-ray imager to meet the demanding DBCT requirements. First, we demonstrate single-photon counting with an a-Se sensor, monolithically integrated on a CMOS ROIC, for the first time. We report the electrical characterization of a previously-designed CMOS SPC imager (Chip 1) and outline the limitations in achieving the electrical performance necessary for photon counting. Subsequently, we present circuit simulations and measurements that identify these limitations and suggest methods for overcoming the associated electrical barriers. Additionally, we discuss the technical challenges hindering the integration of a-Se on Chip 1 and propose our solution to address these issues.

Next, we present the first measured transient X-ray response from a monolithic a-Se/CMOS imager and the first measured pulse-height spectroscopy results using our designed CMOS ROIC (Chip 2). We also experimentally demonstrate the small-pixel effect

(SPE) with an a-Se/CMOS detector for the first time and show its potential to dramatically improve energy resolution and temporal response. Additionally, with device-level simulations, we analyze the impact of carrier movement in an a-Se sensor on SPE.

We then demonstrate, for the first time, photon-counting results using new a-Se/CMOS pixel (Chip 3), which is able to meet the stringent DBCT requirements. To achieve this, we design and verify a novel large-area scalable 92 $\times$ 92 $\mu$m$^2$ pixel having a sub-pixel SPE-enhancement technique. We also present a novel area-efficient foreground calibration circuit for SPC pixels, which employs a new area-efficient current-steering calibration digital-to-analog converter.

Finally, we demonstrate a photon-counting pixel (Chip 4) that features a new adaptive common-mode leakage-compensation circuit with offset correction to further improve the maximum pixel count rate for medical imaging.

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## Dedication

This dissertation is dedicated to my parents and my wife Narges ♡.

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# List of Abbreviations

**$^{241}$Am** Americium-241 42, 51, 54, 57, 77, 123

**2-D** two-dimensional 1, 2, 13, 27, 28

**3-D** three-dimensional 2–4, 27, 28, 58, 82, 86

**6T** six-transistor 99, 109, 110

**a-Se** amorphous selenium xv, 4–7, 26, 27, 29, 31–39, 41–44, 47, 50, 51, 54–64, 67, 71, 75–80, 82–86, 98, 113, 114, 117, 118, 122–125, 135, 139, 140

**BW** bandwidth 98

**CCD** charge-coupled device 13

**CDF** cumulative distribution function 40, 43

**CDS** correlated-double-sampling 127, 129

**CdTe** cadmium telluride 4, 5, 26–30, 41, 67

**CMOS** complementary metal-oxide-semiconductor xv, 3–8, 13, 14, 26, 29, 31, 35–37, 41–43, 51, 54, 56–58, 61, 67, 70, 77–79, 82–86, 113, 134, 139, 140

**CS3B** cold-solder-ball/ball bonding 115

**CSA** charge-sensitive amplifier 19, 58, 61, 67, 68, 70, 74, 75, 78, 79, 87, 91, 97, 98, 101, 103, 110, 117, 118, 122, 126–131, 133–137

**CT** computed tomography 2, 3, 27, 28, 34

**CZT** cadmium zinc telluride 4, 5, 26–30, 41, 67

**DAC** digital-to-analog converter 7, 44, 85, 86, 88, 90–96, 98, 99, 101, 104–106, 110, 117–119, 125, 140, 141

**DBCT** dedicated breast computed tomography 3–8, 27–29, 31–34, 36–38, 41, 57, 67, 75, 82–86, 88, 97, 124, 125, 139, 140

**DBT** digital breast tomosynthesis 1, 2

**DFF** D flip-flop 100

**DM** digital mammography 1–3, 27

**EHP** electron-hole pair 16, 20, 21, 32, 34, 58, 61

**EID** energy-integrating detector 3, 14, 28, 29

**ER** error rate 36, 40, 43, 44, 67

**FDA** Food and Drug Administration 3, 28, 29

**FF** fast-fast 107

**FPGA** field-programmable gate array 73

**FS** fast-slow 107

**FWHM** full-width half-maximum 24, 80, 82, 83

**GBW** gain-bandwidth product 67, 98

**$HgI_2$** mercury (II) iodide 26

**HV** high voltage 15, 16, 32, 58, 59, 64, 66, 114, 115

**I/O** input-output 100, 101

**IR** infrared radiation 48, 49

**LDO** low drop-out 73

**LSB** least-significant bit 96, 101, 105, 107, 110, 117–120

**MIMCAP** metal-insulator-metal capacitor 43

**MOSFET** metal-oxide-semiconductor field-effect transistor 19

**MRI** magnetic resonance imaging 1, 2

**MSB** most-significant bit 94–96, 101, 104–107, 110, 118–120

**MTF** modulation transfer function 22, 23, 35, 140

**NMOS** n-channel metal-oxide semiconductor 67

**OTA** operational transconductance amplifier 19, 58, 67, 68, 98, 127, 132, 135

**PC** personal computer 73

**PCB** printed-circuit board 43, 48, 49, 52, 73, 117

**PHS** pulse-height spectroscopy 5, 7, 24, 57, 79, 83, 122, 123, 139

**PSD** power spectral density 75

**PWL** piecewise linear 95, 96, 104, 110, 119

**QE** quantum efficiency 22, 26, 32, 44, 55

**RMS** root mean square 36, 46

**ROIC** readout integrated circuit 4–7, 14, 26, 29, 31, 37, 38, 41, 42, 47, 51, 54, 56, 57, 67, 79, 82–85, 87, 125, 139, 140

**Si** silicon 4, 25–27, 30, 41

**SNM** static noise margin 109

**SNR** signal-to-noise ratio 4, 27, 80

**SPC** single-photon counting 18

**SPC** single-photon counting 3–8, 13, 14, 18, 19, 26–29, 31, 34, 36, 41, 57, 59–61, 63, 64, 67, 82, 84–86, 88, 90–92, 125–129, 139–141

**SPE** "small-pixel effect" 5–7, 31, 36–38, 41, 57, 58, 60–68, 71, 77–88, 92, 93, 97, 102, 114, 122–125, 139, 140

**SRAM** static random access memory 91, 92, 99, 101, 109, 110

**SS** slow-slow 106

**TC** transfer characteristic 92, 95, 96, 104, 105, 119, 120

**TCAD** technology computer-aided design 7

**TFT** thin-film transistor 3, 13

**TSMC** Taiwan Semiconductor Manufacturing Company 43

**TT** typical-typical 106

**USB** universal serial bus 73

# Chapter 1

# Introduction

## 1.1 Motivation

Breast cancer is a leading cause of cancer-related death among women globally, with an estimated 2.3 million cases diagnosed in 2020 alone, resulting in about 685,000 deaths worldwide [1]. However, early and reliable detection is critical to improving treatment outcomes and reducing mortality rates [2] [3] [4]. Recognizing the critical importance of early detection, breast cancer screening recommendations and policies have recently undergone revisions. For example, in a newly-published update on May 9, 2023, the United States Preventive Services Task Force implemented a revision to their recommendations, now suggesting women undergo screening every other year starting at age forty, which signifies a substantial departure from the previous guideline of starting at age fifty [5] [6].

Early and accurate diagnosis of breast cancer depends on several critical factors, including the identification of soft-tissue lesions and the shape, size, and morphology of microcalcifications [3] [7]. Identification of these factors is made possible by medical X-ray imaging. Optimizing X-ray detector design is essential to achieving better breast cancer screening results, while balancing minimum-feature-size imaging capability, image contrast between different tissues, and the X-ray radiation dose absorbed by the patient.

Breast imaging technologies in clinical use include screen-film mammography, digital mammography (DM), digital breast tomosynthesis (DBT) [8], and magnetic resonance imaging (MRI) [9] [10]. Screen-film mammography and, more recently, DM are the most frequently-used clinical techniques in screening asymptomatic breasts, commonly known as "screening mammography", which provide a two-dimensional (2-D) breast image. The

spatial resolution of screen-film mammography, a measure of minimum-feature-size imaging capability, is at least two times better than that of DM [11]. However, DM provides higher detection efficiency, a measure of the ability of an imager to absorb X-ray photons with limited radiation dose [12] [13].

Although DM is considered the gold standard in breast cancer screening and diagnosis [12] [13], it suffers from two significant drawbacks. The first is its high false-positive rate and relatively high false-negative rate. False negatives miss cancer, which increases the death rate, while false positives affect patients' mental and physical well-being due to calls for additional imaging or biopsy ("callbacks"). Breast density affects the true detection rate of conventional mammography to detect cancer [14] [15] [16]. DM fails to differentiate between dense breast tissue and tumors due to their superposition, potentially resulting in both false positives and false negatives [17]. Medical cost and time are also important factors. In general, for every US$100 spent on screening mammography, an additional cost of US$33 is required to evaluate false positives [15].

The second drawback of DM is its high radiation exposure. In screening mammography, low radiation dose is critical because exposure to X-rays could cause cancer, especially for high-risk patients with familial cancer history [15] [16]. For young women with dense breasts, this poses a greater challenge since considerably higher radiation dose is required to reduce the false-detection rate [16]. In addition to these two primary drawbacks, DM requires breast compression, which often results in an uncomfortable experience for patients [14] [15].

A high false-positive rate due to the superposition of structures in 2-D images with DM can be greatly reduced by three-dimensional (3-D) imaging modalities like MRI and DBT. Although DBT reduces callback rates compared to DM, it still has low performance in imaging of dense breasts, limited 3-D spatial resolution, and has not yet been proven to show better performance over DM for clinical use [16]. Despite the comprehensive 3-D imaging of breast tissue that contrast-enhanced MRI provides and its effectiveness in detecting and diagnosing breast cancer, the prolonged duration of each scan is a significant barrier to its widespread use. Patients often experience inconvenience and discomfort when undergoing MRI scans. Moreover, the limited availability and high purchase costs of MRI machines (averaging US$1M-$3M per machine), combined with its slow imaging speed of only ten to twenty images per day for 24-hour non-stop use, make MRI less accessible to many individuals, even in affluent and developed countries [18]. Additionally, MRI is not appropriate for patients with pacemakers, implantable devices, or claustrophobia [19].

X-ray computed tomography (CT) scanners for breast cancer detection have emerged as another imaging modality to quickly provide 3-D images of the breast without breast

compression. Although conventional CT can provide full 3-D breast images, it applies high radiation dose. To address this issue, General Electric developed a dedicated breast computed tomography (DBCT) system in 1976-1981 and studied its clinical feasibility on over 1500 human breasts [20] [16]. To avoid unnecessary radiation, the system contained a hole designed to hold the breast, and the imager was rotated around it. Despite achieving encouraging results, such as 20% improvement in true-detection rates compared to DM, as well as suppressing unnecessary X-ray exposure to the patient's chest, the system could not meet the dose and spatial-resolution requirements for breast imaging [20] [16]. Two decades later, with developments in technology and image-reconstruction techniques, DBCT has gained researchers' interest again to improve further dose efficiency and spatial resolution [21] [4].

DBCT using a conventional flat-panel energy-integrating detector (EID), in either thin-film transistor (TFT) or CMOS technology, has been investigated to meet the minimum X-ray exposure requirements [22] [23] [24] [25] [26] [27] [28]. Initial clinical investigations have shown improvement in visualization of soft-tissue masses compared to screening mammography. However, a clinical product based on this technology, introduced by Koning, was approved by the U.S. Food and Drug Administration (FDA) in 2014 for only diagnostic mammography, and not screening mammography, due to its high radiation dose compared to DM. Since screening mammography should look for cancer in asymptomatic breasts, the allowed radiation dose is strictly limited. On the other hand, diagnostic mammography is used when cancer is suspected. Therefore, the radiation dose of diagnostic mammography can be higher than screening mammography because more detailed images are required. Nevertheless, two main challenges remain for DBCT systems with EIDs. The first is the low dose efficiency of DBCT due to its higher noise levels, and the second is that DBCT provides low-contrast images due to its limited material separation ability.

Single-photon counting (SPC) imagers are emerging technologies capable of detecting single photons and measuring their energies, which could potentially overcome the limitations of EIDs. SPC detectors use an energy threshold to eliminate electronic noise and low-energy scattering, leading to lower radiation-dose requirements compared to EIDs. In addition, energy-discriminating functionality enables differentiation of the contribution of low-energy photons from those with higher energies. Therefore, better differentiation of soft and hard tissue is achievable. Moreover, multiple energy-windowed images (i.e., spectral imaging) can be performed simultaneously during a single scan [29] [30]. The combination of DBCT and energy-discriminating SPC detectors provides an opportunity for separation of soft-tissue lesions and tumours, especially for dense breasts, in 3-D at a low radiation dose close to that of screening mammography. These are not possible at the same time using the techniques mentioned earlier. Moreover, contrast-enhanced SPC is a potential

enabling technology to achieve better contrast images with lower dose requirements for diagnostic mammography [31].

Research is currently underway to advance DBCT systems that utilize SPC detectors. However, these systems face two significant challenges. First, the performance and manufacturing yield limitations of current X-ray sensor materials make it difficult to scale up monolithic SPCs for large-area imaging, although a few commercially-available small-area monolithic SPCs exist [17] [32][3]. Commonly-used X-ray-sensitive materials, such as silicon (Si), cadmium zinc telluride (CZT), and cadmium telluride (CdTe), are integrated with a CMOS pixel-array readout integrated circuit (ROIC) to form monolithic SPCs. However, Si has low detection efficiency, leading to poor detector signal-to-noise ratio (SNR), and polycrystalline sensors, such as CZT and CdTe, face yield issues with the bump-bonding process needed for CMOS ROIC integration.

The second challenge is that the nominal spatial resolution of existing SPC detectors for DBCT is greater than 100 $\mu$m, which falls short of the required level of detail necessary for imaging microcalcifications. While a nominal spatial resolution of 100 $\mu$m is the highest reported for DBCT using SPC detectors, imaging microcalcifications with diameters less than 100 $\mu$m requires a pixel pitch (i.e., a center-to-center spacing between two adjacent pixels) below 100 $\mu$m. This is crucial for cancer detection and has the potential to reduce false positives in screening mammography [17] [32][3] [7] [30] [4] [33].

In summary, DBCT with SPC detectors has the potential to revolutionize breast imaging by making it possible to detect soft-tissue lesions and microcalcifications in 3-D while keeping radiation exposure low. However, challenges related to large-scale and cost-effective manufacturing and limited spatial resolution need to be addressed for SPC detectors to deliver their full benefits for DBCT.

## 1.2 Thesis Overview and Organization

In this thesis, we aim to tackle the challenges associated with using a-Se, a well-established X-ray-sensitive material, as an alternative to employing Si and polycrystalline-based sensors for SPC detectors. In addition, we endeavour to demonstrate the potential of using monolithic a-Se/CMOS SPC detectors to meet the requirements of DBCT and introduce these detectors as a potentially game-changing development, taking advantage of a-Se's status as an affordable gold-standard X-ray sensor for mammography in flat-panel detectors [34].

The primary obstacles to building a monolithic a-Se/CMOS SPC detector for DBCT

are related to the physical properties of a-Se. While the use of a-Se is more cost effective for large-area deposition, the major drawback of a-Se is that it exhibits lower temporal and energy resolution compared to other materials. Temporal resolution determines photon-processing time, while energy resolution dictates how well the detector can discriminate photons based on their energy. Unlike CZT and CdTe sensors, which require mechanical bump bonding, a-Se can be deposited over a large-area CMOS ROIC using a low-cost thermal-evaporation process [35] [36]. Consequently, manufacturing yield can be improved since a mechanical sensor-attachment process is not required. On the other hand, a-Se exhibits low electron mobility $\mu_n$, which limits its temporal resolution for use in SPC detectors. In addition, random trapping and de-trapping of electrons in a-Se degrade its energy resolution [37][38]. One way to overcome the limited temporal and energy resolution of a-Se is to exploit a phenomenon called the "small-pixel effect" (SPE), which mitigates the impact of slow carriers [39] [40] [41].

We must accomplish the following experimental milestones, ***all for the first time***, to realize a monolithic a-Se/CMOS SPC detector for DBCT:

1. **Photon-counting feasibility**: We aim to demonstrate the ability to perform photon counting using a-Se integrated on a CMOS ROIC.

2. **Transient response**: We will demonstrate the transient response of a-Se monolithically integrated on a CMOS ROIC. This demonstration confirms the feasibility of achieving proper transient charge induction in a-Se when integrated with CMOS. Furthermore, it shows the respective contributions of electrons and holes to the transient response and the total induced charge.

3. **Pulse-height spectroscopy**: We will perform pulse-height spectroscopy (PHS) with a-Se monolithically integrated on a CMOS ROIC. These results will enable us to report the intrinsic energy resolution of a-Se more precisely, which is also the first time when integrated on a CMOS chip. We also need to achieve energy resolution less than 7.3-keV to meet the DBCT energy-resolution requirement.

4. **SPE and its impact**: We aim to demonstrate SPE and use it to enhance the performance of monolithic a-Se/CMOS X-ray detectors.

5. **Photon counting with energy discrimination**: We will demonstrate an a-Se/CMOS X-ray detector capable of discriminating single photons based on their energy.

6. **Large-area scalable spectral SPE-enhanced energy-discriminating SPC pixel**: We will design and validate an a-Se/CMOS photon-counting pixel, which can also benefit from SPE. The pixel must be large-area scalable with two energy bins, possess sub-100-$\mu$m pitch, and achieve a count-rate density of 20 Mcps/mm$^2$ photons to satisfy DBCT requirements.

7. **High-speed pixel design**: We endeavor to design a high-speed SPC pixel that can meet the rigorous requirements of DBCT. This requires a combination of the aforementioned steps along with the ability of the pixel to quickly recover and be ready for the next photon after resolving an X-ray photon.

This thesis is organized as follows:

In Chapter 2, we provide an overview of different X-ray imaging modalities. We introduce X-ray generation, interaction with matter, detection, and digital X-ray imagers. We also discuss direct and indirect-conversion X-ray imagers, sensor materials for direct-conversion X-ray imaging, and charge-integrating versus SPC X-ray imagers. Additionally, we provide a detailed discussion of SPC DBCT systems. Lastly, we present limitations associated with existing SPC DBCT systems and underscore the importance of developing large-area detectors, which remains a challenge with existing technology.

In Chapter 3, we presenet monolithic a-Se/CMOS X-ray imager and discuss their potential use in SPC DBCT imaging. We begin by detailing monolithic integration of a-Se with CMOS and compare properties of a-Se and those of other available materials, highlighting the advantages and limitations of a-Se. Then, we lay out the design requirements for DBCT, including spatial, temporal, and energy resolution. We also assess the feasibility of using a-Se as an X-ray sensor for SPC DBCT and highlight the limiting factors of a-Se in meeting the DBCT requirements. Next, we discuss SPE, which could potentially mitigate the limitations of a-Se and make it a viable alternative material. Finally, we outline the design specifications for SPC DBCT using an a-Se/CMOS imager.

In Chapter 4, we present, for the first time, experimental results that show single-photon-counting feasibility with a-Se monolithically integrated on a CMOS ROIC. We detail the electrical characterization of a previously-designed CMOS chip (Chip 1) and explain the barriers that have hindered photon-counting performance. Subsequently, we present simulated and measured results that identify limitations and suggest methods for resolving these electrical barriers. Despite overcoming electrical restrictions, we highlight the remaining obstacles that further prevent photon counting. We also explain technical limitations preventing the integration of a-Se onto Chip 1. We continue by detailing the proposed steps we took to overcome the challenges, ultimately leading to successful photon

counting with a-Se combined with CMOS. Finally, we present the first demonstration of photon counting with a-Se integrated on CMOS and compare our results to theoretical predictions.

In Chapter 5, we present the first experimental demonstration of SPE with an a-Se sensor integrated on a CMOS pixel-array ROIC (Chip 2). We begin with device-level statistical simulations using technology computer-aided design (TCAD) software to demonstrate the contribution of electrons and holes of a-Se to SPE performance enhancement. Furthermore, we present the front-end pixel and chip design, layout, and fabrication, and explain the chip post-processing and fabrication of shadow masks for a-Se deposition. Our experimental results demonstrate up to 70× reduction in transient-response duration compared to the non-SPE response. This is the first experimental demonstration of SPE-enhanced transient response of an a-Se X-ray sensor on CMOS. These results are also the first demonstration of transient response for a-Se integrated on CMOS, with and without SPE. Furthermore, we report an approximately 2× improvement in energy resolution and demonstrate the first reported PHS results from a monolithic a-Se/CMOS X-ray detector.

In Chapter 6, we present a CMOS ROIC that incorporates the first a-Se/CMOS SPC pixel (Chip 3) and use it to demonstrate SPE-enhanced energy-discriminating photon-counting for the first time. Our novel large-area-scalable pixel uses SPE for dual-X-ray-energy photon counting for the first time, leading to improved temporal and energy resolution. Chip 3 is also the first large-area-scalable a-Se/CMOS single-photon-counting detector. In addition, we present details of our (1) area-efficient SPE-enhanced sub-pixels with shared counters, and (2) a novel partially-shared foreground input-offset-correction circuit employing (3) a new area-efficient current-steering calibration digital-to-analog converter (DAC). Moreover, we present the imager design and fabrication, including its pixel and chip design, layout, simulation, and fabrication, along with shadow mask design for post-processing. Our experimental results satisfy demanding medical-imaging requirements, particularly for DBCT, while offering low-cost large-area scalability.

In Chapter 7, we present a photon-counting pixel (Chip 4) that incorporates a novel adaptive common-mode leakage-compensation circuit with front-end offset correction to further improve pixel count rate. Our simulated and measured results demonstrate the effectiveness of the proposed technique.

Finally, Chapter 8 summarizes our main findings and conclusions. We also highlight our key achievements and contributions, and suggest future work.

# Chapter 2

# Background and Review

In this chapter, we provide an introductory overview of digital X-ray-imaging systems and the fundamental principles underlying X-ray generation, interaction between X-rays and matter, and the detection process. Additionally, we explore and compare different types of imagers. Among these imagers, we focus on detailing direct-conversion SPC CMOS X-ray imagers, which is the main focus of this thesis. Furthermore, we discuss X-ray sensors suitable for direct-conversion imagers, categorizing them based on material type, while highlighting their advantages and disadvantages. Additionally, we emphasize the significance of SPC detectors and DBCT systems and provide an overview of available imagers.

## 2.1 X-Ray-Imaging Principles

### 2.1.1 Basic Digital X-Ray-Imaging System

Figure 2.1 illustrates a basic digital X-ray-imaging system, which includes an X-ray source; a digital X-ray imager, which is composed of an array of pixels containing an X-ray sensor and electronic readout circuits to sense incoming photons passing through the specimen (a female breast in this figure); and an image-processing and display unit to reconstruct the image. We next discuss how X-rays are generated by the source and interact with the specimen, before exploring digital X-ray imagers in more detail.

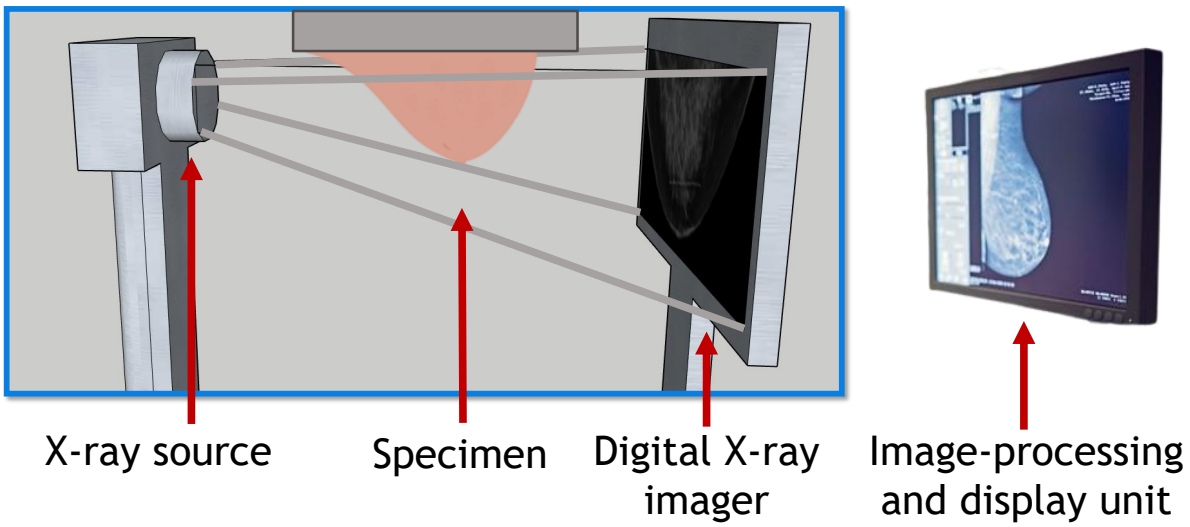



Figure 2.1: A basic digital X-ray-imaging system.

### 2.1.2 X-Ray Generation

In medical X-ray-imaging applications, X-rays are generated using cathodic tubes. As shown in Figure 2.2(a), a heated filament generates thermally-excited electrons which are accelerated under an electric field created by applying a high voltage between an anode and a cathode. The accelerated electrons strike the target material in the anode (positive polarity), which is often made of tungsten, and interact with its atoms through two dominant processes that produce X-ray photons: (1) Bremsstrahlung radiation and (2) characteristic radiation. In (1), incoming electrons release X-ray photons as they decelerate in the target by interacting with the nuclei of anode atoms. X-ray photons are generated with energies ranging from nearly zero up to the kinetic energy of the electrons. In (2), an incoming electron collides with a target atom and kicks out an electron, leaving a vacancy in one of the atom's electron shells. Another electron fills the vacancy and releases X-ray photons of a specific energy unique to each atom [42] [43]. Figure 2.2(b) shows an example of an X-ray spectrum with characteristic and Bremsstrahlung radiation.

The photon-energy range and intensity depend on the application. For instance, the energy spectrum commonly used in mammography falls between 10 keV and 50 keV. In this context, 1 eV is defined as the kinetic energy an individual electron gains when it accelerates from rest when a 1-V potential difference is applied between an anode and cathode in a vacuum. When quantified as an energy unit, 1 eV is equivalent to approximately $1.6 \times 10^{-19}$

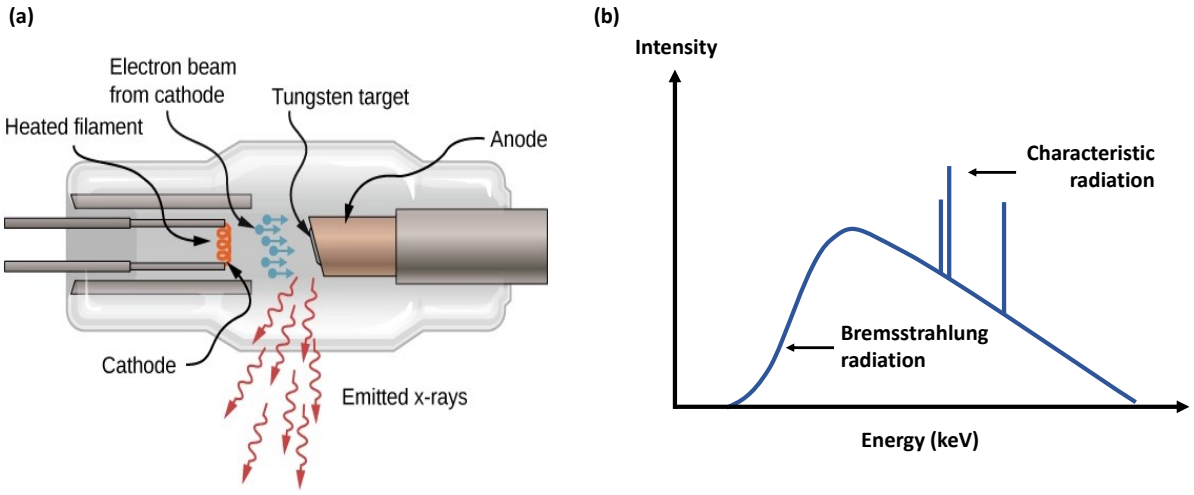



Figure 2.2: (a) An X-ray tube. (b) A typical X-ray spectrum generated by the tube in (a) [43].

J. In addition, intensity is often measured in "milliampere-seconds" (mAs), which is the product of the tube current (mA) and exposure time (s). The photon intensity defines the photon flux, which is the number of photons passing through a unit area per unit time. In mammography, the photon flux typically remains below 20 million counts per second per square millimeter (Mcps/mm$^2$) [44] [45] [46].

### 2.1.3 X-Ray Interaction with Matter

When an X-ray photon strikes a material, this interaction can result in energy deposition or production of a secondary X-ray photon. X-ray interactions in medical imaging include photoelectric absorption and Compton scattering.

In photoelectric interaction, shown in Figure 2.3(a), the incident X-ray with energy $E_0$ interacts with an electron $e^-$ in the medium by ejecting the electron from its orbital. The incident X-ray is completely absorbed, and all its energy is transferred to the electron. If the energy of the incident X-ray is less than the electron's binding energy, the photoelectric interaction does not occur. K-shell electrons are bound more tightly to the atom than outer-shell (e.g., L shell, etc.) electrons. Therefore, if a photoelectric interaction is energetically not possible with K-shell electrons, an interaction may still occur with an outer-shell electron. The photoelectric interaction occurs when the energy of the X-ray photon is slightly higher than the binding energy of the ejected electron [42] [43].

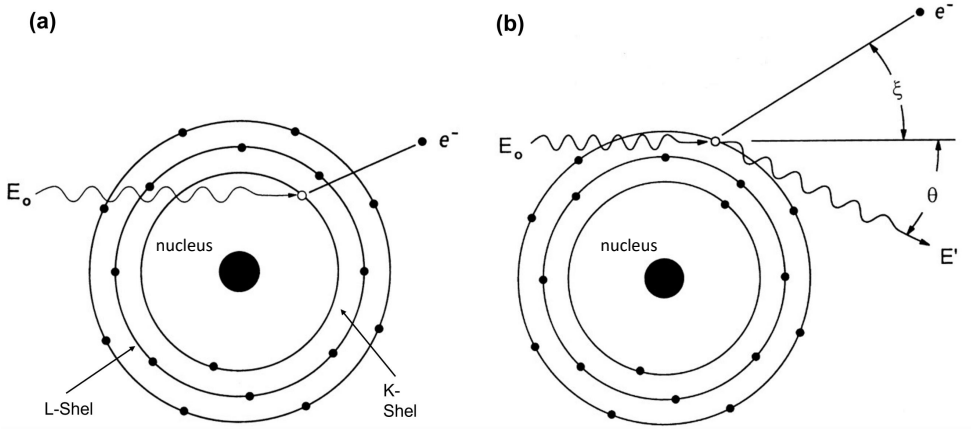



Figure 2.3: Atoms of a medium exposed to X-ray: (a) Photoelectric effect, and (b) Compton scattering [42].

Compton scattering, shown in Figure 2.3(b), occurs at X-ray-photon energies much higher than the binding energy of the electron. In the Compton effect, the incident X-ray with energy $E_0$ interaction produces an scattered X-ray-photon with lower energy $E'$, an ejected electron $e^-$, and an ionized atom [42] [43].

The interaction mechanisms discussed above combine to attenuate the incident photon beam as it passes through matter by absorption or scattering events. There is an exponential relationship between the incident photon fluence $N_0$ and transmitted photon fluence (photons/mm$^2$) $N_x$ after the photon passes through a total material thickness $x$. This relationship is given by:

$$N_x = N_0 e^{-\alpha x}, \tag{2.1}$$

where $\alpha$ is the attenuation coefficient of the material. Materials can be differentiated by measuring their specific attenuation coefficients. This is done by quantifying the emitted photons and assessing the number of photons received from those emitted photons after passing through a known thickness of each material.

## 2.2 Digital X-Ray Imagers

A digital X-ray imager comprises an X-ray sensor, an array of pixels, controlling electronics, and a readout circuit. These imagers are differentiated based on (1) photon-to-electronic signal conversion mechanism, (2): circuit-implementation technology, and (3)

photon-processing principle, as discussed below.

1. **Photon-to-electronic-signal conversion mechanism**

   This refers to the method by which the X-ray sensor converts absorbed X-ray photons into an electronic signal. There are two categories:

   - **Indirect conversion:** In an indirect-conversion imager, shown in Figure 2.4(a), a sensor material called a "scintillator" absorbs incoming X-ray photons and generates visible-light photons. In this process, incoming X-ray-photon energy excites an electron from the scintillator's valence band to its conduction band. This transition leaves a vacancy in the valence band, and when the excited electron returns to the valence band to fill the vacancy, it releases its extra energy by emitting a visible-light photon. The resulting light is then converted to charge $Q_{IN}$ by a visible-light sensor. Readout electronics then convert $Q_{IN}$ to an electronic signal before further processing.
   - **Direct conversion:** In a typical direct-conversion imager, shown in Figure 2.4(b), incoming photons interact with the X-ray sensor by the photoelectric effect and generate $Q_{IN}$. Similar to indirect conversion, readout electronics convert $Q_{IN}$ to an electronic signal.

   Direct-conversion imagers have higher X-ray-to-charge efficiency and higher spatial resolution compared to indirect-conversion imagers. Therefore, the former is a better candidate for low-dose and high-quality medical imaging such as breast imaging [47] [48]. Our focus in this thesis is on direct-conversion imagers.

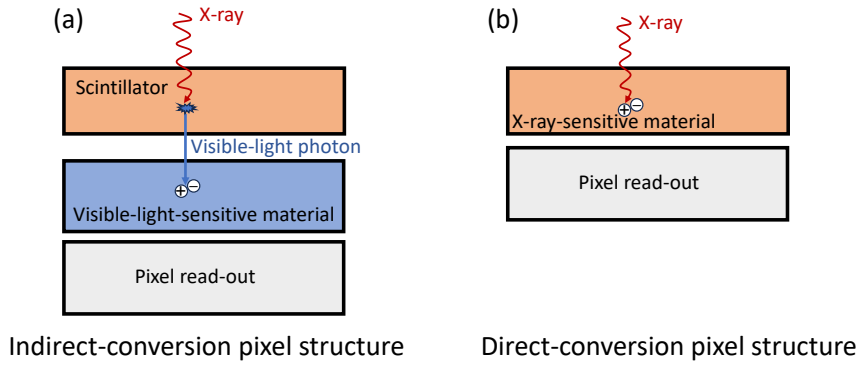



Figure 2.4: General structure of a pixel with an (a) indirect-conversion X-ray sensor, and (b) direct-conversion X-ray sensor.

2. **Circuit-implementation technology**

   This category is based on the technology used to implement the detector pixel and readout electronics. The most popular technologies include:

   - **Charge-coupled device (CCD):** CCDs operate by accumulating and transferring X-ray-induced charges. These charges, which reflect the X-ray energy, are sequentially shifted through rows of pixels and then processed to produce an image.
   - **TFT:** TFTs are field-effect transistors primarily fabricated by amorphous-silicon thin films. Notably, TFTs are designed for large-area substrates, allowing for individual addressing of pixels in a 2-D array. TFTs function as switching elements, facilitating the retrieval of signals from each pixel.
   - **CMOS:** In a CMOS X-ray imager, an X-ray sensor is attached to or deposited on a CMOS chip, and the pixel array and readout circuits are made using CMOS technology.

   While CCDs and TFTs have been prominent for several decades, our focus is on CMOS imagers since they outperform both CCDs and TFTs in several aspects. In general, CMOS imagers are more economical for mass production, dissipate less power, achieve faster image captures, and exhibit reduced readout noise [49] [50] [51] [52] [53] [54].

3. **Photon-processing principle**

   This pertains to the strategy by which pixels process the incoming X-ray-generated electronic signal. The categories are:

   - **Energy-integrating detection:** In digital X-ray imagers built using TFT, CCD, and CMOS technology, energy-integrating detection is a well-established method. When X-ray photons hit the sensor, the generated charge is continuously collected and converted to a voltage over an "integration" period. The converted signal, which is proportional to the energy and number of X-rays absorbed by the sensor during the integration period, is then used to reconstruct the image.
   - **Single-photon-counting detection:** SPC imagers detect the energy of individual photons. With each photon interaction, an electronic signal, having an amplitude linearly proportional to the energy of the detected photon, is generated.

Our focus is on SPC detectors given their superior performance compared to EIDs. One disadvantage of EIDs is that the charges generated by photons with different energies are summed (integrated) without distinction. For example, two 20-keV photons striking the sensor during the integration period could produce the same signal as one 40-keV photon. This diminishes the detector's ability to differentiate tissues, since low-energy-photon detectablity plays a critical role in image contrast.

Another disadvantage is that noise of the EID will be added during the energy-integration period, which could increase radiation dose requirements to achieve higher-quality images [50] [55]. On the other hand, the discrete nature of photon detection in SPC imagers leads to a significant reduction in sensitivity to noise [29] [30].

Based on the categories discussed above, we will investigate direct-conversion SPC CMOS X-ray imagers, which we present in the next section.

## 2.3 Direct-Conversion Single-Photon-Counting CMOS X-Ray Imagers

### 2.3.1 General Architecture

The general architecture of a direct-conversion SPC CMOS X-ray imager is illustrated in Figure 2.5. The imager incorporates an array of SPC pixels, controlling electronics, and a readout circuit, all fabricated using CMOS technology. It also integrates a direct-conversion X-ray sensor on top of the pixel array. The X-ray sensor is often bump-bonded to pixels, as depicted in the figure. Each pixel is designed to capture the generated charge from individual photons at a specific location, subsequently converting the captured photon energy into an electronic signal. Pixels are also linked to output buses, facilitating the transfer of signals to the readout circuit. Once processed, these signals are then sent to an image reconstruction unit via dedicated external (off-chip) acquisition electronics.

### 2.3.2 Signal Formation

We now present the process by which the electronic signal is formed in a direct-conversion X-ray imager. Figure 2.6 shows a pixel with an X-ray sensor sandwiched between two rectangular electrodes with dimension $d$, with its pixel ROIC block. The mobilities of

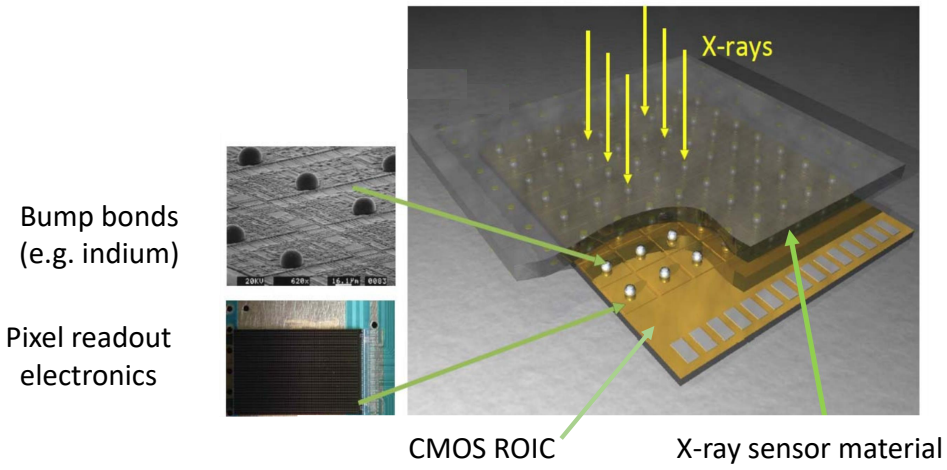



Figure 2.5: General architecture of a direct-conversion SPC CMOS X-ray imager (adapted from [56]).

X-ray-generated charge carriers in the sensor have a significant impact on the transient response of X-ray imagers. We use the Shockley-Ramo theorem to calculate $Q_{ind}$ for a direct-conversion X-ray imager, under the assumption that the generated charge density changes slowly so that quasi-static conditions are satisfied [39] [57] [58] [59] [60]. This approach is more computationally efficient compared to solving Maxwell's equations, which involves accounting for interactions between instantaneous electric and magnetic fields associated with a "cloud" of moving charge [39] [40] [57].

To illustrate the Shockley-Remo theorem, we consider how X-ray induced charge $Q_{ind}$ is formed, assuming only a single charge $Q_{ph} = q$, shown in Figure 2.6, is generated in a biased X-ray sensor material with thickness $L$, following absorption of an X-ray photon. The high voltage (HV) electrode is shown on the left and a collection electrode on the right. We also assume that $q$ is generated on a horizontal line that intersects the pixel center. When $q$ drifts along lateral dimension $x$, starting from position $x = a$ and ending at its final position $x = b$, then $Q_{ind}$ is given by

$$Q_{ind} = q \times [\Phi_\omega(b) - \Phi_\omega(a)], \tag{2.2}$$

where $\Phi_\omega(b)$ - $\Phi_\omega(a)$ is the difference in the weighting potential $\Phi_\omega$ at positions $a$ and $b$. Weighting potential $\Phi_\omega$ is a dimensionless quantity that represents the normalized electric potential gradient across the semiconductor when the pixel sensing electrode has a weight normalized to unity, and the bias electrode is set to a weight of zero. In Figure 2.6, the

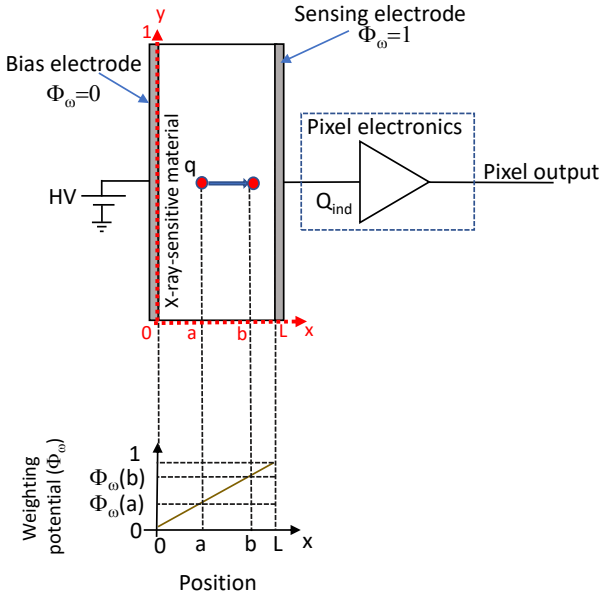



Figure 2.6: Direct-conversion pixel model with its weighting potential across the X-ray sensor.

pixel and HV bias electrodes are equally-sized, $L/d \ll 1$, and $\Phi_\omega$ increases linearly along $x$, from $x = 0$ to $x = L$, for any vertical position $y$, where $y$ is normalized such that $0 \leq y \leq 1$. Consequently, when $q$ is generated at $x = L/2$ in the sensor, where $\Phi_\omega(a) = 0.5$, and drifts all the way to $x = L$, where $\Phi_\omega(b) = 1$, then $Q_{ind} = Q_{ph}/2 = q/2$, as calculated from (1). Therefore, $Q_{ind}$ is only 50% of $Q_{ph}$.

However, when a positive HV is applied at the bias electrode relative to the pixel electrode, both holes and electrons are generated by single X-ray photon absorbed by the X-ray sensor. These charge carriers will drift toward the pixel electrode and the bias electrode, respectively. The number of generated electron-hole pairs (EHPs) $N$ is given by $N = E_{ph}/E_{ion}$, where $E_{ph}$ is the photon energy and $E_{ion}$ is the sensor material ionization energy, which is the energy required to generate one EHP. The generated carriers induce a time-varying charge signal $Q_{ind}$ on the pixel electrode, which is detected by a readout circuit.

To describe the contribution of the carriers to the transient response, which defines the maximum count-rate of the detector, we assume, for simplicity, that a photon interaction generates a single EHP, and each carrier drifts laterally to its respective electrode from the center of the sensor. We also do not consider the impact of charge sharing due to cloud

diffusion, Compton scattering, or any electrical coupling between pixels. In a conventional detector with two large parallel-plate electrodes for which $L/d \ll 1$, shown in Figure 2.7, both electrons and holes contribute to $Q_{ind}$. Typically, electrons move faster than holes, and we assume for our given sensor, the election mobility is $2\times$ the hole mobility for simplicity. The horizontal axis is normalized such that the duration required for the slow carrier to travel from the center to its respective electrode is unity. The figure also displays the normalized hole-induced charge $Q_{ind,h}$ and electron-induced charge $Q_{ind,e}$, as each carrier drifts to its respective electrode. In this case, with $Q_{ph} = q$, then $Q_{ind,h} = |Q_{ind,e}| = q/2$, since each carrier travels a distance of $L/2$ and the $\Phi_\omega$ gradient is linear. Therefore, the total induced charge $Q_{ind} = Q_{ind,e} + Q_{ind,h} = q$ once both carriers reach their respective electrodes, and the signals rise linearly with time.

Figure 2.7 also shows that the settling time of $Q_{ind}$ is mainly determined by the settling time of $Q_{ind,h}$. As a result, the slower carriers are responsible for reducing the temporal resolution of the detector.

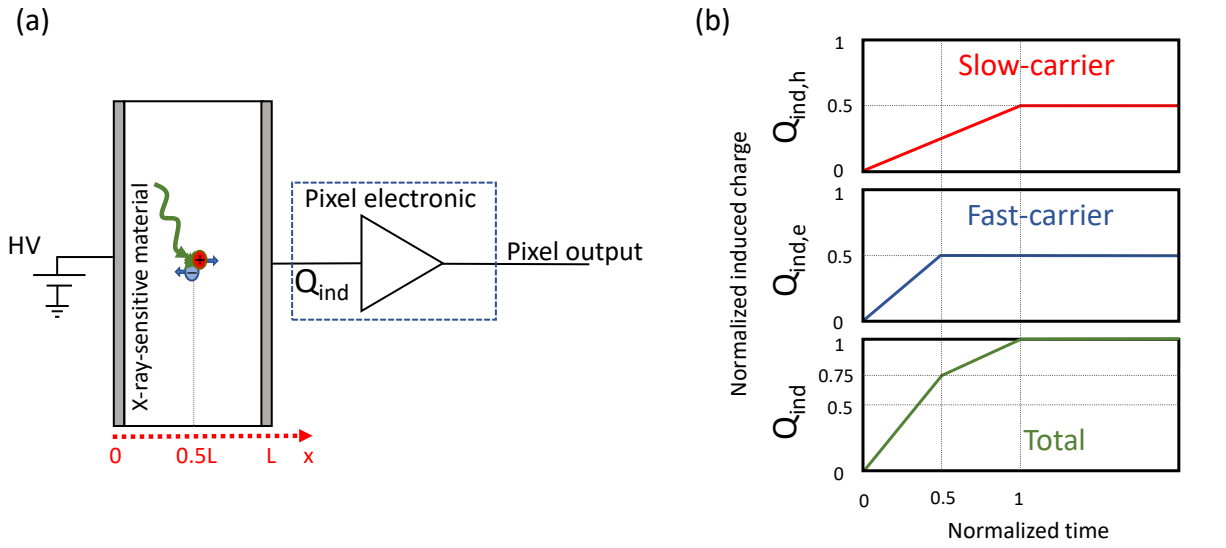



Figure 2.7: Normalized transient response of the induced charge by X-ray-generated carrier drift illustrating the contribution of each carrier for a material where electron mobility is higher than hole mobility.

### 2.3.3 Energy Discrimination in Single-Photon Counting Imagers

In this section, we emphasize the benefits of energy discrimination using SPC imagers. Figure 2.8 conceptually illustrates SPC pixel operation. In an SPC pixel, photons absorbed by the sensor are categorized (binned) according to their energy and counted. Figure 2.8 shows an analogy for SPC pixel operation with 2 energy bins, which is our target number of bins. The circles represent individual photons, and the diameter of each circle represents the photon energy. Based on their size, each circle will be either ignored or fall into two bins corresponding to the energy bins of an single-photon counting (SPC) pixel. The three openings correspond to the three levels of comparison. Opening 1 sets the limit where circles with undesirably small diameters will be ignored. This corresponds to photons with energy less than our desired level. Openings 2 and 3 correspond to two desired energy levels, where we finally count the number of circles separately.

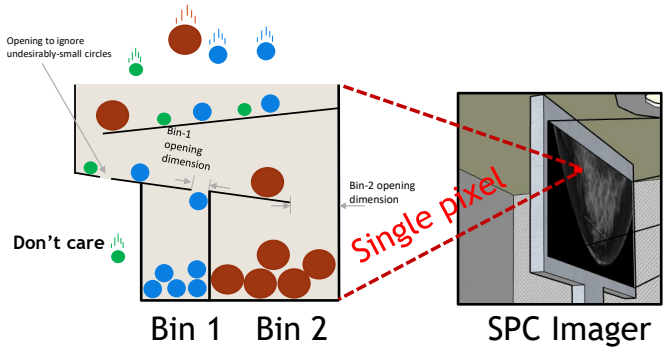



Figure 2.8: Concept of energy-discriminating single-photon-counting imager pixel.

Using two energy bins will improve the differentiation of soft and hard tissues with improved radiation dose exposure. For instance, we consider the mapping of counted high and low energy photons for three materials with different densities and thicknesses, as illustrated in Figure 2.9. With two bins, photon counts with low (but above a certain limit), and high energies can be separately mapped into x and y axes when X-rays pass through a given material. In Figure 2.9 when imaging is performed solely using low-energy X-rays, Materials 1 and 2 cannot be distinguished since the number of counted photons are the same. Conversely, when imaging is conducted using only high-energy X-ray photos, the count of photons passing through Materials 1 and 2 differ significantly. However, in this case, Materials 1 and 3 cannot be discriminated in the final image. Therefore, by performing imaging twice with two different energy levels, which is called conventional dual-energy imaging, or by separately counting high-energy and low-energy photons using

SPC with two energy bins when a range of X-ray energies are applied with a single exposure, these materials can be accurately differentiated, as demonstrated in Figure 2.9. However, the SPC pixel will result in a lower radiation exposure to the patient since both images will be simultaneously captured with a single exposure.

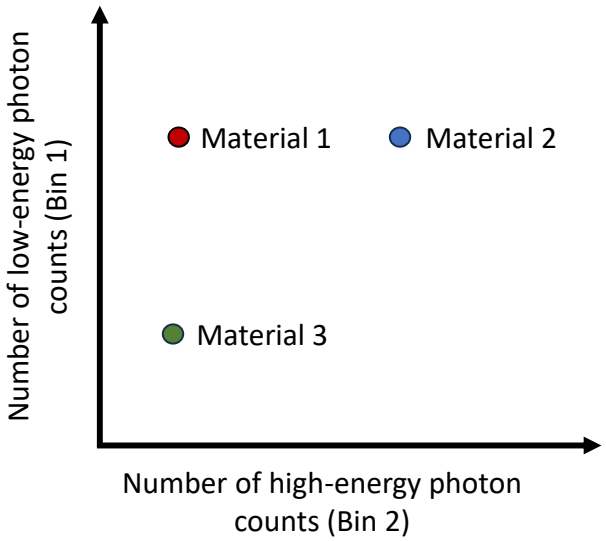



Figure 2.9: Example of material separation using SPC pixel with two energy bins.

### 2.3.4 Simplified SPC Pixel and its Operation

Figure 2.10 depicts a simplified circuit architecture of an SPC pixel with two energy-discriminating bins. In the figure, pixel operation using three photons of different energies is shown as an example. For each X-ray photon absorbed by the sensor, the induced charge pulse is collected and amplified by a charge-sensitive amplifier (CSA) containing an operational transconductance amplifier (OTA) and integration capacitor $C_f$. A resistive path, in parallel with $C_f$, using a metal-oxide-semiconductor field-effect transistor (MOSFET) operated in triode, discharges $C_f$ before the next charge packet arrives and provides dc feedback around the OTA. Each pulse is compared to two threshold voltages $Vth_1$ and $Vth_2$ using two comparators, where $Vth_1 < Vth_2$. The threshold voltages are defined based on the expected photon-energy levels set by the application. Each comparator is followed by a counter, which increments when the corresponding comparator output transitions from low (logic '0') to high (logic '1'). The value of each counter represents the total number of counted photons with energy above the defined photon-energy level. Finally, the data

collected from all pixels is utilized to generate two separate images, each corresponding to a specific range of energy levels.

In Figure 2.10(a), a low-energy X-ray photon is absorbed by the sensor, resulting in a small number of generated EHPs and a signal below $Vth_1$ and $Vth_2$. As a result, no counters increment, and the final images remain unaffected.

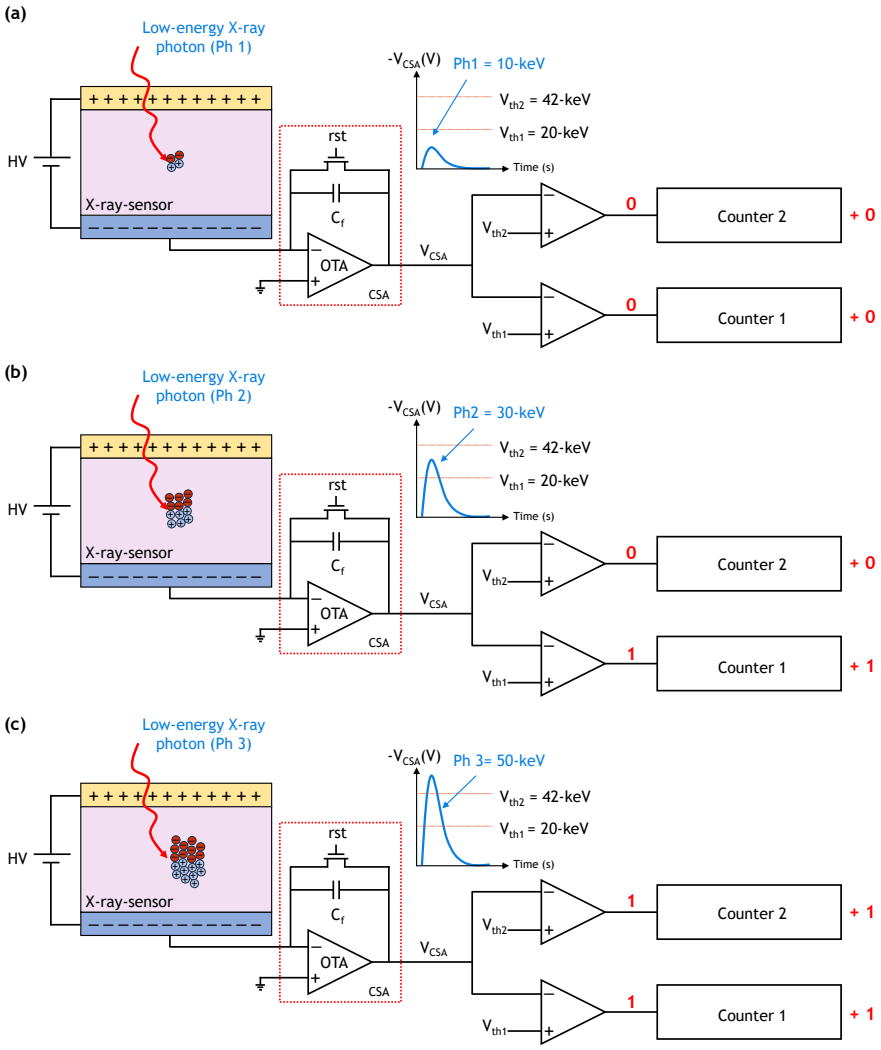



Figure 2.10: Example operation of an SPC pixel with an absorbed (a) low-energy photon, (b) medium-energy photon, and (c) high-energy photon.

Figure 2.10(b) depicts the interaction of a medium-energy photon, producing a larger number of generated EHPs and a signal that falls between $Vth_1$ and $Vth_2$. This causes Counter 1 to incerement, and forms the final soft-tissue image.

Lastly, in Figure 2.10(c), a high-energy photon interacts, generating a significantly larger number of generated EHPs and a signal surpassing both threshold levels. This causes both counters to increment, resulting in the formation of a final hard-tissue image from Counter 2 outputs.

Using a mammography example, the hard-tissue image containing microcalcifications is generated using a matrix that holds the count values for all pixels from Counter 2, as shown in Figure 2.11(a). The black regions correspond to areas where a majority of the photons are detected by the pixels, while the white regions indicate areas where photons are predominantly absorbed by the sensor. This image effectively highlights the presence of microcalcifications, which can potentially serve as indicators of malignancy. The image in Figure 2.11(b) represents soft-tissue lesions, which are also indicative of cancer. This particular image is formed through the collected data from both counters in each pixel. Each cell value in the matrix represents the count of low-energy photon events, obtained by subtracting the value from Counter 2 from the value of Counter 1 [61] [62] [63] [55] [64] [61] [62] [63] [55] [64].

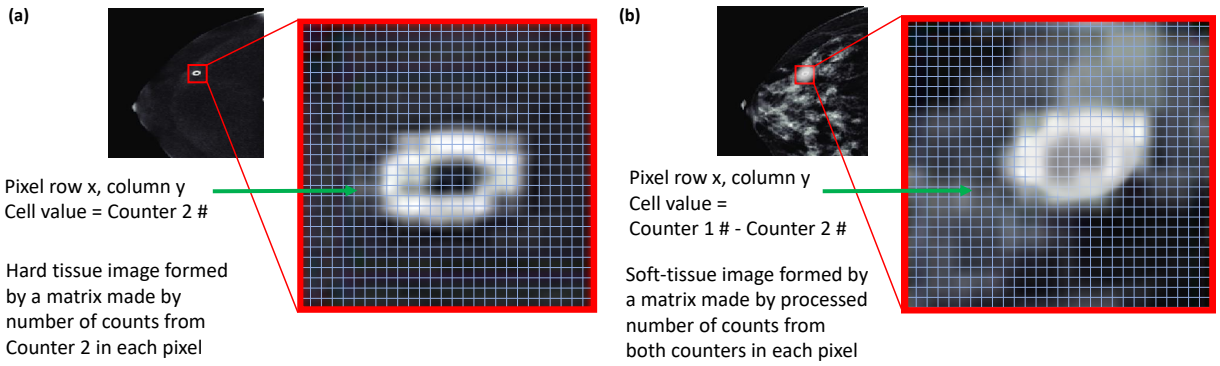



Figure 2.11: Example of hard- and soft-tissue images of a breast formed through dual-energy imaging.

### 2.3.5 X-ray-Sensor-Performance Measures

In this section we introduce several measures to evaluate the performance of X-ray sensors.

### Quantum efficiency

Quantum efficiency (QE) represents the percentage of incident photons that are absorbed by the sensor and converted into charge. The attenuation coefficient, which defines a sensor's ability to stop photons, is illustrated in Figure 2.12 for different materials based on the energy of incident X-ray photons. The formula to calculate QE is as follows:

$$QE = 1 - e^{-\alpha(E,Z,d)}, \tag{2.3}$$

where $d$ denotes the sensor thickness, $Z$ defines the atomic number, $E$ is the energy of the incoming photon, and $\alpha$ is the attenuation coefficient. An effective atomic number $z_{eff}$ can be defined for alloys based on the number of atoms in the alloy and the percentage of each material [65].

### Spatial resolution

Spatial resolution defines the minimum feature size that can be imaged. The modulation transfer function (MTF) is a measure of the effective spatial resolution of imagers. Figure 2.13 illustrates the concept behind MTF. If the imaged object consists of line pairs defined as ideal black and white bars in the spatial domain, the input of the imager is a square wave

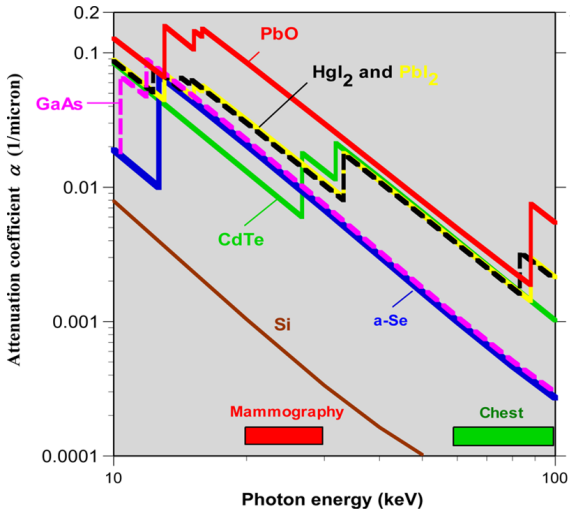



Figure 2.12: Attenuation coefficient versus photon energy for different sensor materials [35].

with full contrast (100%) between two phases. An ideal system has the same contrast at the output. However, real imagers exhibit lower contrast (90% in this example) depending on the effective resolution of the imager. As lines get closer to each other (i.e., higher number of line pairs per unit distance), the image contrast becomes lower [66]. The effective spatial resolution is defined as the number of lines per millimeter (lp/mm) where the MTF is 50%.

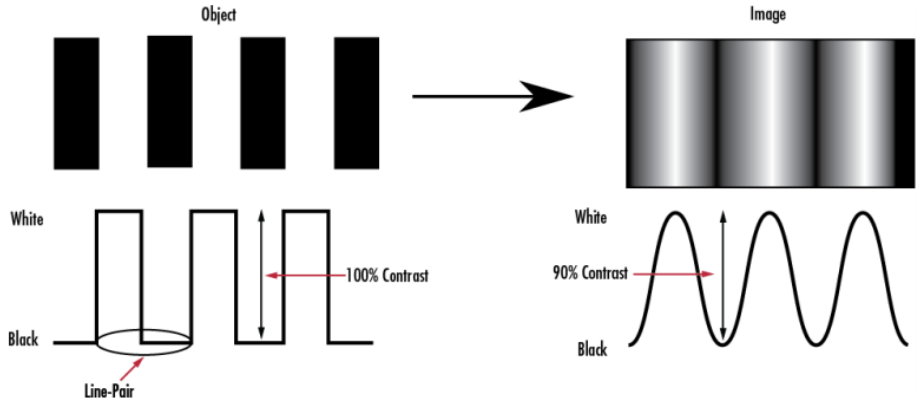



Figure 2.13: MTF conceptual illustration (adapted from[66]).

### Temporal resolution

The temporal resolution of a detector signifies how quickly it processes an absorbed photon and becomes ready again for the arrival of the next photon. A commonly-used metric to assess temporal resolution is the count rate of the detector. Assuming an ideal readout circuit, this is primarily governed by the X-ray sensor's properties like carrier mobility. We can express the count rate $CR$ as follows:

The velocity of carriers $\nu$ (in cm/s) in the sensor is given by

$$\nu = \mu E, \tag{2.4}$$

where $E$ is the applied electric field and $\mu$ is the carrier mobility. The maximum time $t_{max}$ required for a generated carrier to traverse the sensor is dictated by its slow carrier's mobility, which is often the hole mobility $\mu_h$, and is defined by

$$t_{max} = \frac{L}{\nu_h}, \tag{2.5}$$

where $L$ is the sensor thickness and $\nu_h$ is the hole velocity. The pixel $CR$ is therefore given by

$$CR = \frac{1}{t}. \tag{2.6}$$

### Energy resolution

The energy resolution of an X-ray detector refers to its ability to effectively differentiate between the energies of incoming photons. A widely-used measure for assessing energy resolution is full-width half-maximum (FWHM) from PHS diagram. PHS is generated by constructing a histogram of measured pulse heights from the detector's outputs and then converting these values into corresponding photon energies, as illustrated in Figure 2.14. The FWHM quantifies the width of the pulse-height or energy peak of PHS diagram at the point where its intensity is half of the maximum number, represented as $N_{max}$. Smaller FWHM values indicate a higher energy resolution. The FWHM is approximately 2.3 times the standard deviation of a fitted Gaussian distribution. The energy resolution is affected by carrier mobility, carrier lifetime $\tau$, and random trapping and de-trapping of charge carriers.

X-ray sensors for digital X-ray imagers are distinguished by their atomic structures, falling into three primary categories: crystalline, poly-crystalline, and amorphous. In this

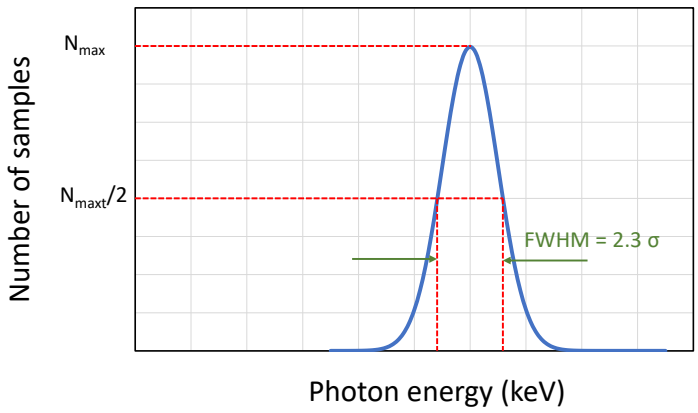



Figure 2.14: A pulse-height spectrum demonstrating FWHM energy resolution.

section, we outline prominent materials within each category and discuss their inherent properties, advantages, and disadvantages.

### 2.3.6 X-Ray-Sensor Materials

X-ray-sensitive materials for digital X-ray imagers are distinguished by their atomic structures, falling into three primary categories: crystalline, poly-crystalline, and amorphous. In this section, we outline prominent materials within each category and discuss their inherent properties, advantages, and disadvantages.

#### Crystalline Materials

Crystalline direct-conversion X-ray-imaging materials have several unique advantages. One of their foremost merits is their superior thermal stability compared to amorphous structures. This ensures they function reliably across a wide range of temperatures. Furthermore, their structured atomic layout allows for high spatial resolution and leads to reduced electronic interference in the final image, primarily because of the efficient movement of generated charge carriers. This not only ensures a fast response, but also improves the overall image quality.

However, while these materials present considerable benefits, they also have their challenges. Fabrication of high-quality single crystals can be both expensive and technically demanding. These challenges have prompted interest in polycrystalline and amorphous materials for X-ray imaging [67] [68] [69] [34] [35].

Silicon is a well-known crystalline X-ray-sensitive material. Despite its unique advantages, the low attenuation coefficient of Si at high energies for mammography, shown in Figure 2.12, makes it a less efficient candidate for this application [35].

#### Polycrystaline Materials

Polycrystalline materials are more commonly used in X-ray imaging systems compared to crystalline sensors. Polycrystalline sensors are generally more cost-effective and simpler to fabricate compared to single-crystal materials. Their granular nature allows for varied grain sizes which can be customized for specific applications. However, due to grain boundaries, there can be inconsistencies in charge transport, leading to delayed response times. The main challenge with polycrystalline detectors is the need for bump-bonding attachment to

a CMOS ROIC, a process that often has a low yield, increasing both costs and production complexity [34] [35] [70] [71] [49] [72] [73] [30].

Well-known examples of polycrystalline materials for X-ray imaging are CdTe, CZT, and mercury (II) iodide ($HgI_2$). Although $HgI_2$ has a high $\alpha$, it is a highly toxic material which makes it less practical to work with [74]. CdTe and CZT are the most common materials for SPCs. However, despite their higher $\alpha$ than Si, they suffer from low yield and require an expensive bump-bonding process for CMOS integration [73]. Moreover, $HgI_2$ and CdTe, and similarly CZT, suffer from characteristic X-rays for energies above the K-edge of Cd and Te, causing fluorescence X-rays, which includes the mammography range. Fluorescence X-rays are X-ray-photons generated due to the photoelectric effect, which could be detected by neighboring pixels, limiting the spatial resolution of the imager [73] [30] [75].

### Amorphous Materials

Amorphous materials are also widely used as direct-conversion X-ray sensors. Their primary advantage is that they can be processed more easily and at a lower cost than their crystalline counterparts. Owing to their non-crystalline nature, they lack the grain boundaries that can complicate the performance of polycrystalline materials. Nevertheless, their lack of a structured atomic arrangement can result in less efficient charge transport, potentially leading to a slower response and, thus, limited temporal resolution. Moreover, the absence of a uniform atomic structure might also cause varied electronic properties due to random trapping and de-trapping of charge carriers, ultimately reducing the energy resolution of the imager.

A-Se is a well-established amorphous X-ray sensor and is considered the gold standard for large-area flat-panel detectors in mammography. A primary advantage of a-Se is its manufacturability on a large scale using a straightforward thermal-evaporation process. Additionally, the high atomic number of a-Se contributes to a comparable with polycrystalline sensors, making a-Se suitable for mammography. The attenuation coefficient of a-Se falls within a comparable range to CdTe, and $HgI_2$, and significantly exceeds that of Si for photon energies ranging from 15 keV to 60 keV, as shown in Figure 2.12(a). It is worth noting that $\alpha$ of a-Se decreases significantly for higher energies. However, since mammography typically operates within the energy range of 15 keV to 50-keV, a-Se demonstrates satisfactory QE for this application. Although the challenge of low $\alpha$ for high-energy photons remains, compared to other commonly used materials, it lies beyond the intended scope of our target application [35].

Despite its unique manufacturability advantage, a-Se has certain limitations as a photon-counting sensor when compared to Si, CdTe, and CZT. The first limitation is its slow carrier response, which is approximately ten times slower than that of CdTe. This slower response, along with the limited carrier lifetime of a-Se, significantly impacts the temporal and energy resolution of the a-Se-based imager. Additionally, a-Se has high ionization energy, typically 50 eV, in contrast to the 4.4 eV of CdTe. This means that photons striking a CdTe sensor will generate an output signal that is more than ten times greater in amplitude than that generated by a-Se. This results in a lower pixel SNR for an imager with a-Se, ultimately limiting the energy resolution.

Table 2.1 provides carrier mobility and lifetime values for the different materials we have discussed, which highlights the significant differences between a-Se and its counterparts.

Table 2.1: Material properties of a-Se compared to other common X-ray sensors.

| | a-Se | CdTe | CZT | Si |
|---|---|---|---|---|
| $\mu_e$ ($cm^2/Vs$) | 0.003 | 1100 | 1900 | 1400 |
| $\mu_h$ ($cm^2/Vs$) | 0.14 | 100 | 110 | 480 |
| $\tau_e$ ($\mu s$) | 1 | 3 | 2.7 | 1000 |
| $\tau_h$ ($\mu s$) | 1 | 3 | 1.6 | 3000 |

## 2.4 Dedicated Breast Computed Tomography Using SPC

Recent advances in DBCT systems incorporating SPCs have shown promise for breast cancer detection, indicating the potential to replace conventional X-ray imaging systems. A DBCT scanner is illustrated in Figure 2.15. CT scanners exploit mathematically-processed combinations of several X-ray images taken from different angles to generate cross-sectional images of a specimen. Geometry-processing algorithms, which are beyond the focus of this thesis, are used to generate a 3-D volume image of the object from 2-D images. A DBCT imager is a CT imager designed specifically for breast scanning. As shown in the figure, the patient lies on the bed, and only the breast, placed through a dedicated opening, is exposed to X-rays. Another advantage of DBCT imaging is its avoidance of breast compression, a discomforting experience commonly associated with conventional DM. During image acquisition, the X-ray source and imager rotate around the breast to take several images from different angles. The total time required to scan the whole breast

is the "scan time". The "number of projections" is the number of X-ray measurements during the scan needed to produce a 3-D image. The "frame time" is the time needed to acquire one 2-D tomographic image from a single projection.

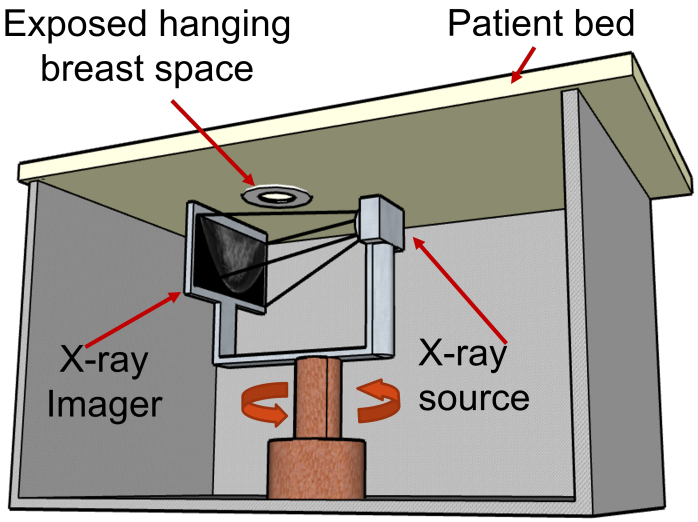



Figure 2.15: A DBCT scanner.

Significant advances have been made in the field of CT imaging with the integration of SPC technology in recent years. Industry leaders such as Canon (through their acquisition of Redlen Inc.) and Siemens Healthcare have been driving this progress. The integration of Redlen's expertise in CZT material growth, wafer processing, and sensor fabrication, along with Canon's CT manufacturing capabilities, have resulted in notable advancements in the development of SPC CTs [76] [77] [78] [79]. On the other hand, the NAEOTOM Alpha CT detectors, manufactured by Siemens, are equipped with SPC technology, utilizing CdTe as the sensor material. Notably, this product was the first CT scanner with SPC technology to receive clearance from the FDA (but not for breast imaging), in September 2021 [80] [31] [81] [80].

Since the above-mentioned scanners are designed as conventional CT scanners, they require exposing the entire chest, rather than focusing solely on the breast, to X-ray radiation. Consequently, they are not authorized for use in DBCT purposes. The previously-mentioned advantages of detecting soft-tissue lesions and microcalcifications in 3-D, while maintaining a low radiation dose comparable to the range used in screening mammography, cannot be simultaneously achieved with either DBCT imagers using conventional EIDs or SPCs in conjunction with traditional CT systems. To achieve this superior performance,

a combination of SPC technology and DBCT imaging is required.

Two research groups, one from the Friedrich Alexander University Erlangen-Nuremberg (FAU) and the other from the University of California, Irvine (UCI), are actively engaged in the development of DBCT systems utilizing SPCs. In 2010, Willi Kalender from FAU proposed the concept and demonstrated the feasibility of photon-counting DBCT at a dose level of only 5 mGy, comparable to the limit in screening mammography [32] [82] [83] [84]. The prototype system employed a CdTe sensor with a pixel pitch of 100 $\mu$m, enabling scanning of the entire breast in 10 s. It is worth noting that the scan duration should be less than 20 s to allow the patient to hold their breath, thereby minimizing motion artifacts caused by respiration [32] [17] [83] [84].

A spin-off company from FAU, founded in 2008, introduced the AB-CT system in 2014 as the sole commercially available DBCT system incorporating an SPC. However, this product is still awaiting approval from the FDA for clinical use [32] [17] [82] [83].

A research group at UCI is also developing DBCT with SPC for screening mammography [85]. In 2010, this group demonstrated the feasibility of an SPC in combination with a fan-beam X-ray source (i.e., a collimated beam of X-rays emitted in a fan-like pattern), resulting in 50% reduction in the required dose compared to flat-panel EID, while maintaining image quality [29]. The system from UCI incorporates a CZT sensor with a pixel pitch of 800 $\mu$m. The reported count-rate requirement is approximately 1.2 Mcps/mm$^2$, operating at 20 frames per second (50-ms frame time), and utilizing 204-1229 projections [86] [87] [29] [88].

The group at UCI later reported the development of a second-generation imager featuring a silicon sensor with a detector pixel pitch of 100 $\mu$m. They investigated the feasibility of detecting microcalcifications, a vital aspect in mammography [89] [30]. The detector count-rate density achieved was 100 Mcps/mm$^2$, with linear operation up to 40 Mcps/mm$^2$ and an adjustable frame time ranging from 1 ms to 2000 ms. Table 3.1 provides a summary of the reported DBCT systems using SPCs.

Current DBCT systems are constrained by the challenges associated with the low yield and high manufacturing costs of (poly)crystalline sensor materials. In our research, we examine the potential of monolithically integrating a-Se with a CMOS ROIC for DBCT as an affordable and more practical approach.

Table 2.2: Performance of recently-reported SPC-based DBCT systems.

| | **Group** | **FAU** | **UC Irvine** | |
|---|---|---|---|---|
| | **References** | [32] [17] [82] [83] | [86] [88] | [87] [29] [30] |
| Detector | **Sensor** | CdTe | CZT | Si |
| | **Pixel pitch ($\mu$m)** | 100 | 800 | 100 |
| | **No. of energy bins** | 2 | 5 | 4 |
| | **Count rate (Mcps/mm$^2$)** | 100 | 1.2 | 100 |
| DBCT scanner | **Scan time (s)** | 7-12 | - | 20 |
| | **No. of projections** | 2000 | 204-1229 | 462-1300 |
| | **Frame rate (frames/s)** | 1000 | 20 | 20 |
| | **Application** | Screening | - | Screening |
| | **Dose (mGy)** | 5 | - | 6 |

# Chapter 3

# Feasiblity of a Monolithic A-Se/CMOS Single-Photon-Counting X-Ray Imager for DBCT

In this chapter, we explore monolithic integration of a-Se with a CMOS ROIC and the use of a-Se in SPC detector for DBCT. First, we present the structure of a monolithic a-Se/CMOS imager. Next, we investigate the advantages and limitations of a-Se compared to other sensor materials commonly employed for DBCT. Furthermore, we discuss the potential of SPE to mitigate the inherent limitations of a-Se. Finally, we outline design specifications for a SPC detector for DBCT using a-Se/CMOS integration, encompassing aspects such as pixel area, noise, and bandwidth, and a-Se sensor thickness.

## 3.1 Structure of a Monolithic A-Se/CMOS Imager

Figure 3.1 shows a simplified cross-section of a monolithic a-Se/CMOS X-ray imager. The CMOS ROIC chip incorporates the pixel array and is integrated with the a-Se X-ray sensor. The top metal of the CMOS process, metal-6 (M6) in this figure, serves as the sensing electrode for the pixels. During CMOS fabrication, an opening is created above the bottom electrode by etching the passivation layer situated above M6. This opening facilitates the electrical connection between the a-Se sensor and the ROIC pixel input. The deposition of a-Se onto the chip surface is accomplished using a simple thermal-evaporation process. Another round of thermal evaporation is used to form the top contact, which involves depositing a thin layer of gold.

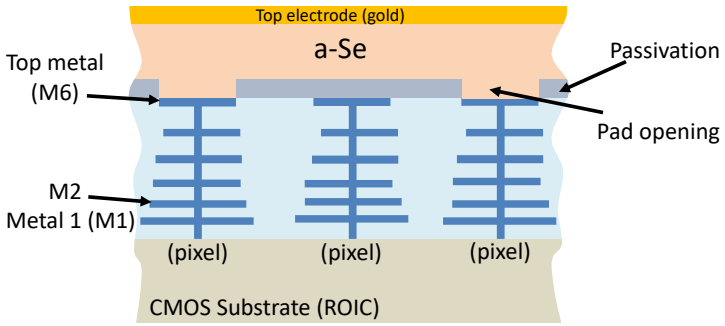



Figure 3.1: Simplified cross-section of a-Se/CMOS X-ray imager.

To cause electrons and holes, generated by X-ray-photon absorption, to drift toward the top contact and bottom electrode, respectively, a positive HV is applied to the top contact relative to the bottom electrode. The number of EHPs generated $N$ is calculated using $N = E_{ph}/E_{ion}$, where $E_{ph}$ is the photon energy and $E_{ion}$ is the a-Se ionization energy. The generated carriers create a time-varying charge signal $Q_{ind}$ on the pixel electrode. A front-end circuit subsequently detects this signal, as previously explained in Section 2.3 for direct-conversion imagers. However, the difference here is that holes are collected at the pixel bottom electrode since these carriers have greater mobility than electrons in a-Se.

## 3.2 Feasibility of using a-Se in an SPC detector for DBCT

### 3.2.1 Sensor Thickness

The thickness of a-Se, $L$, must be carefully chosen to achieve acceptable QE for DBCT, where photons in the 20-kev to 50-keV range are relevant. Figure 3.2 presents $\alpha$ of a-Se as a function of thickness for photons with energies of 20 keV, 50 keV, and 100 keV [90].

A typical configuration for achieving acceptable QE for mammography is using 200-$\mu$m-thick a-Se with an applied electric field of 10 V/$\mu$m. As shown in Figure 3.2, approximately 95% of 20-keV photons are absorbed. For 50-keV photons, 65% of these are absorbed and QEs are considered acceptable [91] [34] [35].

It is important to note that implementing a-Se thickness exceeding 200 $\mu$m with consistent uniformity poses a fabrication challenge. Consequently, there is a limitation on the

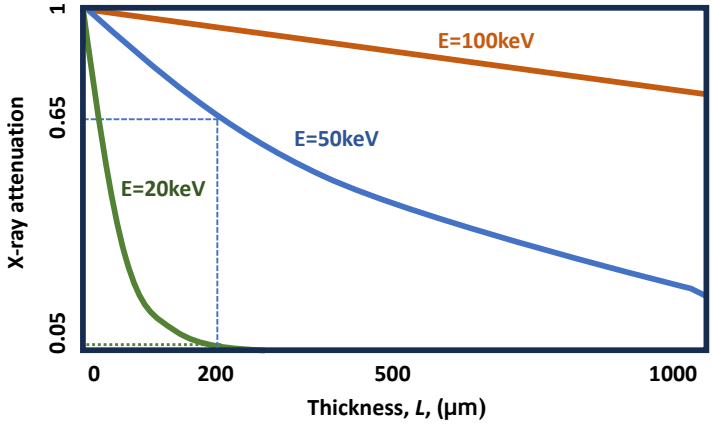



Figure 3.2: X-ray attenuation of a-Se for three photon energies under a constant electric field (adapted from [90]).

achievable thickness, which is why the a-Se thickness typically reported in the literature does not exceed 200 $\mu$m [34] [35].

### 3.2.2 Spatial and Temporal Resolution

The pixel size spcecification, which is determined by the minimum required feature size to be imaged, affects both the spatial resolution and temporal resolution of the imager. The 100-$\mu$m spatial resolution reported for DBCT sets the upper limit for square pixel dimension. Moreover, the imager should be able to handle the photon count-rate requirement for DBCT, which sets another upper limit for pixel size to avoid pileup.

Pileup is a phenomenon that occurs when more than one photon hits the pixel during the photon-processing time. A pixel exhibits pileup when the incoming photon flux is higher than the maximum count rate that the pixel is able to process. To implement an imager capable of handling higher photon flux, the pixel area must be reduced for a given pixel count rate, leading to higher pixel density. Reduction in pixel size enables the imager to capture and process more incoming photons in a given time period, effectively enhancing the temporal resolution of the imager. This means the count-rate requirement also impacts pixel size.

The imager count-rate requirements are impacted by radiation dose level in terms of photon flux to the imager. Scan time for DBCT should be short enough to avoid motion

artifacts due to patient breathing. The typical number of CT projection reported in the literature is between 300 and 500 for 360-degree rotation [87] [88] [92]. A 10-s scan time is typical to avoid motion artifacts. Using 500 projections per image, the necessary frame rate is 20 frames per second [93]. For screening mammography (6 mGy dose level), the true photon flux at the detector is reported to be as low as 2 Mcps/mm$^2$ [30]. The range of reported count-rate requirements for this application is around 10-20 Mcps/mm$^2$ [87] [88] [30]. A detector with a maximum count rate of 100 Mcps/mm$^2$ is also presented, which exceeds the requirements. However, this detector is linear only up to 40 Mcps/mm$^2$, which is still above the reported requirements [94]. Thus, it becomes imperative for the DBCT application incorporating SPC to have the ability to accommodate a photon flux of 20 Mcps/mm$^2$ to ensure it can handle the required photon detection rate with some margin.

Assuming 100% fill factor, where fill factor is the ratio of the X-ray-sensitive area of the imager to the total imager area, and a maximum pixel count rate of 20 Mcps/mm$^2$, the required pixel size can be calculated as follows. The pixel density should be high enough to handle the photon flux defined by the application. The upper limit for square pixel dimension $d_{max}$ (in $\mu$m) is given by

$$d_{max} = \sqrt{(10^6 \times CR)/\phi_q}\,, \tag{3.1}$$

where $\phi_q$ is the incoming photon flux and $CR$ is calculated using (2.5). The transient response of the induced charge depends on $\mu_n$ and $\mu_p$, and for a-Se (as opposed to other conventional X-ray sensor material), it is dominated by the slow electron response. Figure 3.3 shows a typical normalized transient response of charge induced on a pixel electrode due to the movement of EHPs generated by a photon absorbed at the center of a 200-$\mu$m-thick a-Se sensor.

The waveform from the first part of the transient response (up to 1 $\mu$s) is from both electron and hole movement. The second part of the waveforms (after 1 $\mu$s) is due to electrons only, since a-Se's holes have higher mobility and reach the electrode sooner.

To handle the photon flux needed by DBCT, different pixel sizes will be required depending on a-Se thickness and applied electric field, assuming the transient response is dominated by electrons. For 200-$\mu$m-thick a-Se under a 10-V/$\mu$m electric field, the pixel count rate is calculated as 15 kcps. The upper limit for pixel size can be calculated as 27×27 $\mu$m$^2$ to handle 20 Mcps/mm$^2$. However, conservative design and practical measurement considerations suggest a pixel size of approximately 15.8 $\mu$m would be required [96].

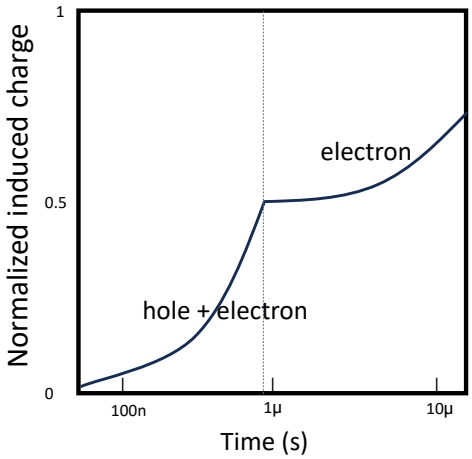



Figure 3.3: Normalized transient collected charge induced by holes and electrons in a 200-$\mu$m-thick a-Se X-ray sensor (adapted from [95]).

The lower bound of pixel size is another design consideration that is defined by the inherent spatial resolution of a-Se. Designing a pixel smaller than this intrinsic spatial resolution is not useful. The measured MTF of a-Se on a CMOS chip is shown in Figure 3.4. The 50% MTF is reported to occur at 32 lp/mm, corresponding to a 16-$\mu$m effective object size [97]. Although this reported imager is not a single-photon-counting detector, it illustrates that spatial resolution well below our target is achievable using an a-Se sensor.

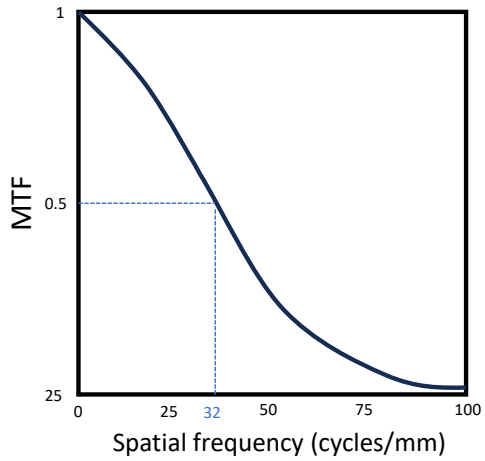



Figure 3.4: Measured MTF from a previously-reported hybrid a-Se/CMOS X-ray imager (adapted from [97]).

Although the requirement for spatial resolution in an SPC detector using an a-Se sensor is easily achievable, thanks to the high intrinsic spatial resolution of a-Se, the low $\mu_n$ of a-Se imposes strict constraints on the spatial resolution since it requires high pixel density to meet the temporal resolution of DBCT.

### 3.2.3 Energy Resolution

The energy resolution of a-Se is another limitation in meeting the DBCT requirements. In dual-energy mammography, optimal energy thresholds have been reported as 20 keV and 42 keV [92]. Therefore, for an SPC detector for DBCT, two threshold discriminating levels, corresponding to 42-keV and 20-keV energies, are required. Discriminating 20-keV and 42-keV photons with $6\sigma$ separation, as an ideal design case, gives 0.13% error rate (ER). This translates to a root mean square (RMS) energy uncertainty of 3.6 keV. However, targeting $3\sigma$ separation, as a more practical limit which reduce its energy resolution, translates to an rms uncertainty of 7.3 keV, or 6.6% ER. The main limitations of a-Se are its low $\mu_n$ relative to $\mu_p$, random trapping and de-trapping of electrons, and its high ionization energy [37] [38]. The reported energy resolution of a-Se is approximately 14.3 keV, achievable without additional fabrication complexity, which is a desirable characteristic for monolithically integrating a-Se with CMOS technology [98]. This resolution leads to around 50% ER, which is far below the requirements presented.

Therefore, despite its valuable low-cost, high-yield, and large-area scalable manufacturability, a-Se appears to be unsuitable for an SPC detector for DBCT due to its poor energy and temporal resolution. However, there is potential for overcoming these limitations, as explained next.

### 3.2.4 Small-Pixel Effect Potential Impact

The SPE has the potential to significantly enhance the temporal and energy resolution of an a-Se X-ray sensor, utilizing the near-field effect. When the ratio of the sensor thickness $L$ to square-pixel electrode dimension $d$ exceeds unity, the photon-generated charge carriers that drift relatively close to the pixel-electrode surface contribute to the output signal. This reduction in the deteriorating impact of slow-moving carriers on both temporal and energy resolution results in improved performance. The transient response with SPE will show a sharp change when fast carriers manage to reach certain proximity of the pixel (i.e., near-field region). The impact of this near-field effect, known as SPE in monolithic

direct-conversion CMOS imagers with pixellated small electrodes, can enhance the temporal and energy resolution of these imagers [40] [99] [95]. Figure 3.5 shows a simplified comparison between a normalized conventional transient response of a detector and the response obtained with SPE. In the transient response of a conventional pixel the fast hole-dominated segment is clearly observable, as is the slow electron-dominated segment. This transient time is mainly dominated by slow electrons. On the other hand, the transient response with SPE demonstrates that the observed transient response is not affected by slow electron transport but rather shows a sharp response. However, the influence of SPE on a-Se/CMOS has not been previously demonstrated.

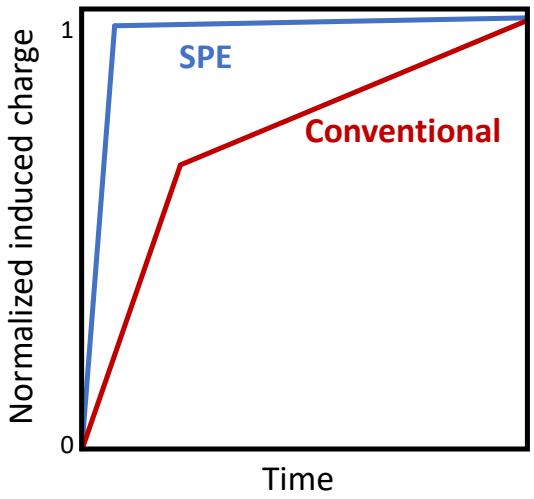



Figure 3.5: Conventional and SPE-enhanced transient response comparison.

## 3.3 ROIC Pixel Design Requirements

Our primary objective is to design a ROIC with pixels that meet the spatial-, temporal-, and energy-resolution requirements of DBCT. We aim to do this by exploiting the potential benefits of SPE.

Choosing the ROIC pixel dimension involves careful consideration of several factors. Meeting the spatial-resolution requirements of DBCT necessitates a pixel area smaller than $100 \times 100\ \mu m^2$. Additionally, to leverage the benefits of SPE, it is desirable to have smaller pixel sizes. However, since SPE has not been demonstrated on an a-Se/CMOS detector

before, precise information on the ideal pixel dimensions to exploit SPE remains uncertain. Hence, our objective is to explore various pixel dimensions and ultimately propose a design that not only meets the spatial-resolution requirements, but also exploits the benefits of SPE to enhance the energy and temporal resolution of the pixel.

In one aspect, the count-rate density requirement of DBCT can result in different ROIC pixel bandwidth requirements, depending on the chosen pixel dimension. In order to ensure that the ROIC can exploit the benefits of SPE and meet the demanding DBCT requirements, and considering the absence of published data, we opt for a conservative approach when defining the ROIC bandwidth limit. This involves setting the ROIC bandwidth while considering the DBCT count-rate density requirements, different possible implemented pixel dimensions, and potential improvement from SPE.

We first assume the X-ray sensor is ideal and then define the required pixel count rate to ensure meeting the DBCT requirements. In the worst-case scenario, where the pixel dimension is 100 $\mu$m, the upper-limit dictated by the application, and assuming an ideal temporal response from a-Se, the count-rate requirement is 200 kcps/pixel. This represents the highest pixel count-rate requirement to fulfill the 20 Mcps/mm$^2$ DBCT requirement. If the implemented pixel dimension is smaller, this count-rate requirement would be less demanding. Therefore, designing the pixel to achieve 200 kcps ensures that the pixel response will not be the limiting factor in meeting the temporal resolution requirement of DBCT.

The second consideration when choosing the pixel count-rate involves accommodating the impact of SPE. Assuming a conventional response (without SPE), a pixel equipped with an a-Se sensor can handle a count rate up to 15 kcps. To account for the uncertain impact of SPE on temporal response, we conservatively aim to design a pixel with a 1.5-Mcps count rate. This ensures that the pixel can handle a 100× potential increase in a-Se temporal response due to SPE. By targeting a count rate of 1.5 Mcps, we accommodate a significantly higher temporal response due to SPE, and meet the required worst-case DBCT pixel count rate of 200 kcps.

Discriminating photons with acceptable resolution is another specification which sets the pixel noise requirements. To explain how the noise requirement is derived, we consider the ideal pixel model shown in Figure 3.6(a). The charge induced by generated electron-hole pair movements is stored in capacitor $C_{int}$, creating voltage signal $V_{int}$, which is proportional to the photon energy. Voltage $V_{int}$ is compared to two threshold levels corresponding to 20-keV and 42-keV photons and generates a two-bit digital output.

Comparison of the ideal responses gives deterministic results, meaning that if the photon energy is less than 20 keV, the two-bit digital output generated by two comparators will

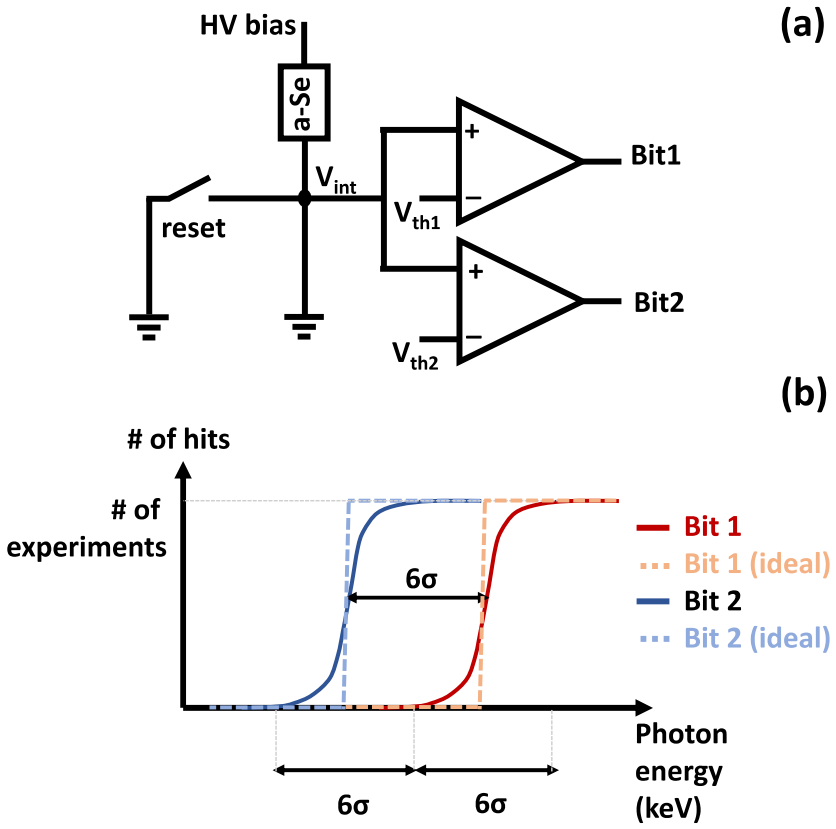



Figure 3.6: (a) Ideal pixel model. (b) Number of photon hits versus photon energy.

be '00', as shown in figure 3.6(a). For photon energies between 20 keV and 42 keV, and higher than 42 keV the output will be '01' and '11', respectively, with 100% certainty. However, a practical pixel circuit suffers from two main non-idealities, which introduce uncertainty to the comparator output. The first is input-referred random offset $V_{os}$ due to device mismatch during the fabrication process non-ideality. The second is input-referred noise $V_n$ produced by devices in the pixel. Another source of uncertainty is a-Se sensor shot noise charge $Q_{sh}$.

Voltage $V_{ind}$ in Figure 3.7 calculated as follows. For a 20-keV photon hitting a-Se under a 10-V/$\mu$m field, the ionization energy of a-Se needs to be estimated. Figure 3.7 shows a-Se ionization energy as a function of applied electric field for different photon energies. With the typical thickness and applied electric field, the ionization energy can be estimated as 48 eV. Therefore, a 20-keV photon generates 416 electron-hole pairs [100]. Assuming the

generated charge will be stored in a $C_{int}$ of 10 fF, then $V_{int}$ will be 6.7 mV. This voltage can be defined as a threshold voltage corresponding to 20-keV photon energy.

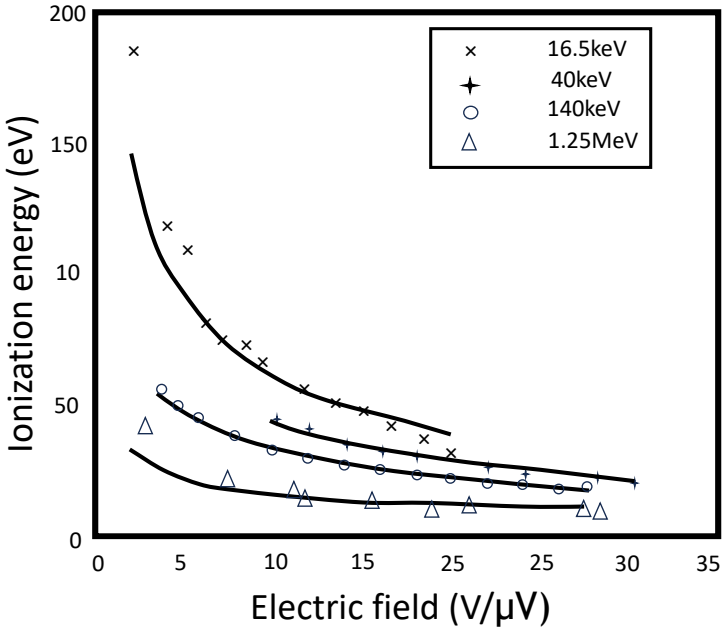



Figure 3.7: A-Se ionization energy vs electric field (adapted from [101]).

We assume the noise source referred to the comparator input follows a Gaussian distribution. Repeated measurements give the probability of getting logic "1" at the pixel output as a function of photon energy. This can be fit to the cumulative distribution function (CDF) of a Gaussian distribution, which is also shown in Figure 3.6(b) [102]. Discriminating 20-keV and 42-keV photons with $6\sigma$ separation, as a typical design constraint, gives 3.6-keV$_{rms}$ uncertainty, which is equivalent to 76 $e^-{}_{rms}$ [100]. By assuming the main sources of noise are thermal noise $Q_n$ and shot noise $Q_{shot}$ and they are uncorrelated, each noise contributor should be less than 43 $e^-{}_{rms}$ to achieve the desired ER. Shot noise for 20-keV and 42-keV photons is calculated as 20 and 30 $e^-{}_{rms}$, respectively, which are below the desired limit. Note that, for a given photon energy, shot noise is the variation in the number of electron-hole pairs which can be estimated as the square root of the number of generated electron-hole pairs [100]. In addition, assuming thermal noise on $C_{int}$ is the main source of noise at the pixel input, it is proportional to $C_{int}$ value. The noise $Q_n = (kTC_{int})^{0.5}/q_{rms}$ where $T$ is the absolute temperature and $K$ is Boltzmann's constant. For $C_{ind} = 10$ fF, $Q_n = 40$ $e^-{}_{rms}$ at room temperature.

Finally, Table 3.1 presents our derived imager requirements and compares them with currently-available systems. Before designing an SPC imager for DBCT, the first step is to experimentally demonstrate the feasibility of photon counting with a-Se monolithically integrated on CMOS ROIC, which is the focus of the next chapter.

Table 3.1: Summary of imager requirements and comparison.

| **References** | **FAU** | **UCI** | | **Our requirements** |
|---|---|---|---|---|
| | [32][17][82][83] | [86][88] | [87][29][30] | |
| **Pixel pitch ($\mu$m)** | 100 | 800 | 100 | $< 100$ |
| **Sensor** | CdTe | CZT | Si | A-Se |
| **No. of energy bins** | 2 | 5 | 4 | 2 |
| **Count-rate density (Mcps/mm$^2$)** | 100 | 1.2 | 100 | $> 20$ |

## 3.4 Summary

We discussed monolithic a-Se/CMOS image sensors and presented their potential use as SPC for DBCT imaging. We detailed monolithic integration of a-Se with CMOS and laid out the design requirements for DBCT. We also assessed the feasibility of using a-Se as an X-ray sensor for SPC DBCT and highlighted the limiting factors of a-Se in meeting the DBCT requirements. Next, we explained SPE and outlined the design specifications for SPC DBCT using a-Se/CMOS.

# Chapter 4

# Experimental Demonstration of Single-Photon Counting Using a Monolithic A-Se/CMOS X-Ray Imager (Chip 1)

## 4.1 Introduction

In this chapter, we demonstrate the feasibility of using a-Se as an X-ray-photon-counting sensor by providing an initial experimental demonstration of single-photon counting with a-Se monolithically integrated on CMOS ROIC. Our results are the first demonstration of single-photon counting with a-Se on a CMOS ROIC. The ROIC (Chip 1) was previously designed [103], and post-processed, wirebonded, and packaged by three other graduate students at the University of Waterloo. First, we discuss our electronic characterization of the chip, its limitations, and the challenges we encountered in integrating a-Se with the ROIC. We also present the chip architecture and its operation to explain our contributions and results. Next, we present our solutions to fix several experimental issues that initially prevented us from demonstrating single-photon counting. Finally, using a low-flux monoenergetic Americium-241 ($^{241}$Am) gamma source, we show single-photon counting results with an a-Se sensor on a CMOS integrated circuit, for the first time.

## 4.2 Architecture and Operation

Chip 1 is fabricated in a Taiwan Semiconductor Manufacturing Company (TSMC) 180-nm analog/mixed-signal CMOS technology, and the die occupies a $3 \times 4$ mm$^2$ area. The chip consists of two arrays of $26 \times 196$ pixels. Two counter arrays neighbor the two pixel arrays where we have one counter per pixel. The pixel circuit, with its timing diagram, is illustrated in Figure 4.1. The pixel consists of a top-metal pad covered by a-Se, an integration capacitor $C_i$ (formed from transistor gate capacitance), two preamplifiers, and a latch. Two metal-insulator-metal capacitors (MIMCAPs) $C_{os}$ have been used as offset storage to correct pixel offset voltage. Each pixel stores the generated charge on $C_i$, and the generated voltage across this capacitor is then compared to a defined threshold voltage $V_{th}$ using preamplifier PA1. Voltage $V_{th}$ is defined by the desired photon energy, as explained in Chapter 2. Finally, the latch outputs a logic one or zero: a zero means that no photon has been absorbed by sensor, or its energy is less than the corresponding $V_{th}$; and one means that a photon with energy higher than the corresponding $V_{th}$ has been absorbed by the sensor [103].

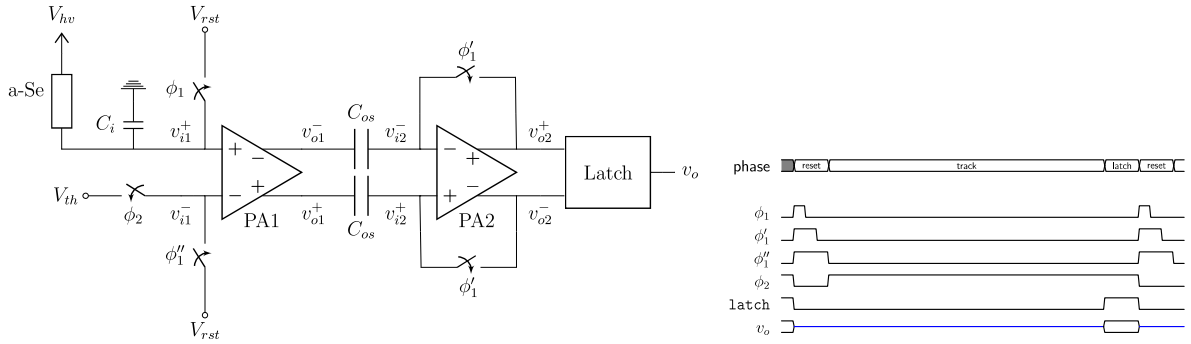



Figure 4.1: Chip 1 pixel circuit and its timing diagram [103].

## 4.3 Electronic Characterization

We first quantify the minimum detectable photon energy used for electronic characterization of Chip 1. Our custom printed-circuit board (PCB) is shown in Figure 4.2. CDF plots, introduced in Chapter 3, enable noise characterization of the chip, which is required to define the ER of photon detection. The probability transfer characteristic plots resemble CDF plots obtained by sweeping $V_{th}$, without an X-ray source present.

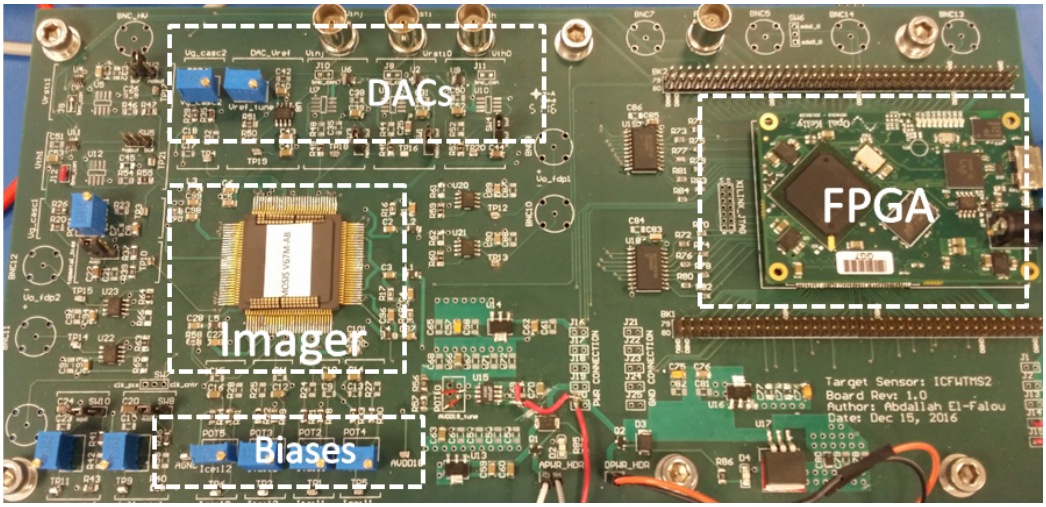



Figure 4.2: PCB for electronic characterization of Chip 1.

The preliminary response of all pixels in one array is shown in Figure 4.3(a). The measured input-referred noise of 6.7 $mV_{rms}$ is close to 10× higher than the expected noise level. This noise translates to a 116-keV minimum detectable photon energy. Detecting 116-keV photons is almost impossible due to the extremely low QE of the a-Se sensor for high-energy photons, as discussed in Chapter 3. In addition, this energy range is far above our target application. More importantly, at this noise level, the required minimum photon energy to achieve acceptable ER will saturate the pixel preamplifiers. Upon examining the response, we discovered unexpected interference causing small undesired peaks in the probability transfer characteristics for all pixels, as shown in Figure 4.3(a), and Figure 4.3(b) for one pixel. This interference critically limits the overall performance of the imager and prevents its photon-counting capability.

After system-level modifications, such as board-level noise performance improvements, off-chip DAC output buffering to set the threshold voltages, grounding improvements, impedance matching for critical input signals, and timing optimizations, the noise results are improved to 5.9 $mV_{rms}$, as shown in Figure 4.3(c). Powering down one array out of two arrays reduces the uncertainty to only 4.6 $mV_{rms}$, as shown in Figure 4.3 (d). However, the undesired peaks in pixel probability transfer characteristics are still present.

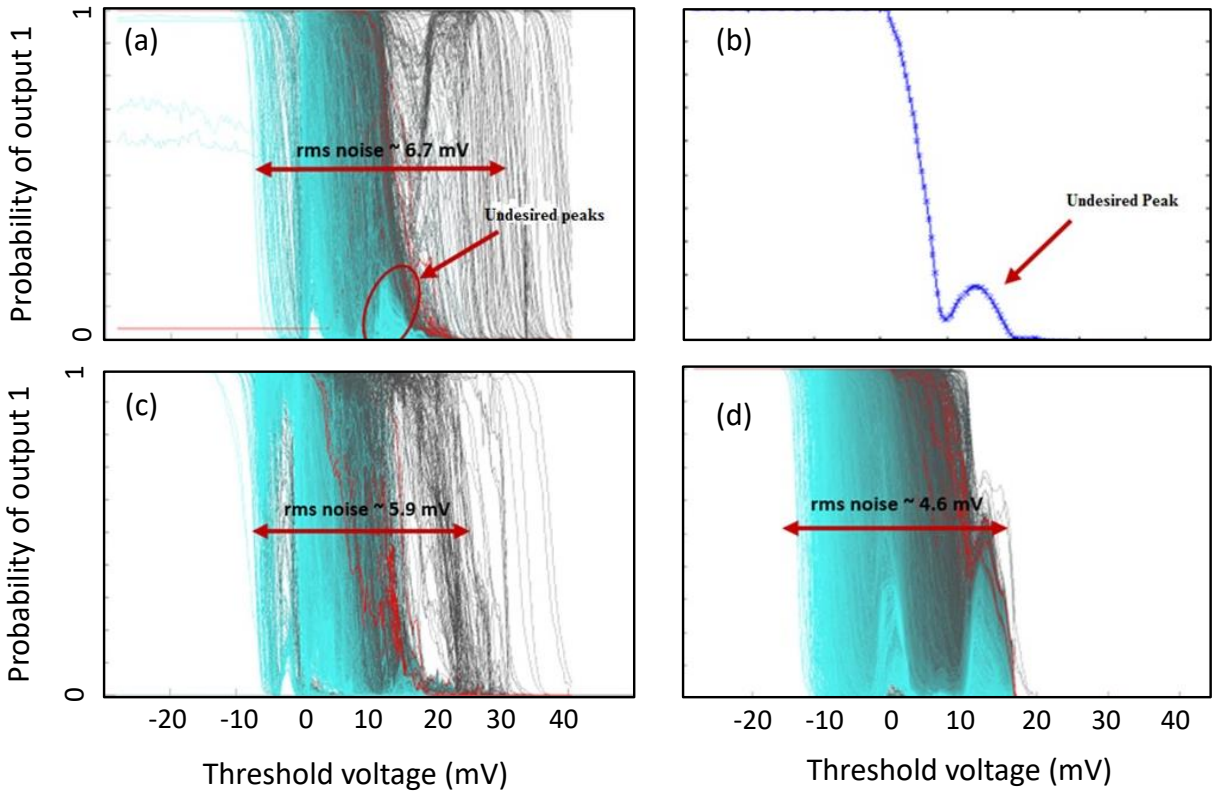



Figure 4.3: Measured probability transfer characteristics. (a) Preliminary results, (b) results from one pixel, (c) results after performance modifications, and (d) results after bypassing one array.

## 4.4 Simulation and Functional Modifications

After conducting extensive circuit simulations of the pixel and the array, we identify parasitic capacitance coupling between digital nodes and the high-impedance node at the pixel input as the main causes of the performance issues. This effect could manifest as either inter-pixel kickback, occurring between internal nodes of a single pixel, or cross-talk between neighboring pixels.

To illustrate the issue, we model inter-pixel kickback, as depicted in Figure 4.4(a), which involves the coupling capacitance $C_c$ between the pixel output and integration node. This coupling gives rise to two significant issues. First, the previous state of the pixel output has a notable impact on the leakage current into $C_i$. This could potentially affect the

voltage developed at $C_i$ during the integration period, leading to undesirable peaks in the probability transfer characteristic plot. Second, due to the nature of sharing an output bus column-wise, when a pixel toggles in another row, it can couple charge into $C_i$ of the pixel that is operating in its integration phase. As a result, approximately +/- 586$e^-$ could be coupled into $C_i$ for each toggle. Considering there are 26 rows, each row could potentially couple in an interfering signal corresponding to a 28-keV photon. The accumulation of these interfering signals could cause significant deviations from proper pixel functionality.

To address these issues, we operate the chip as a line scanner by enabling only one row at a time, with other rows not being reset at all. This forces the comparator output to a known state after each integration period to mitigate the memory effect caused by leakage. These measures result in considerable improvement, as demonstrated by the electrical characterization results for all 196 pixels in a row shown in Figure 4.4(b). The RMS noise, including the offset distribution, measured at only 1.69 $\text{mV}_{rms}$ and corresponding to a minimum detectable signal of 33-keV, is a notable improvement. This enables us to proceed with photon-counting experiments. However, the offset is not entirely removed, as shown in Figure 4.4(b), where the offset distribution over the row remains higher than the expected value of 0.7 $\text{mV}_{rms}$. This discrepancy is attributed to the preamplifiers operating in their non-linear region when the input signal voltage is large, ultimately restricting proper offset correction [103].

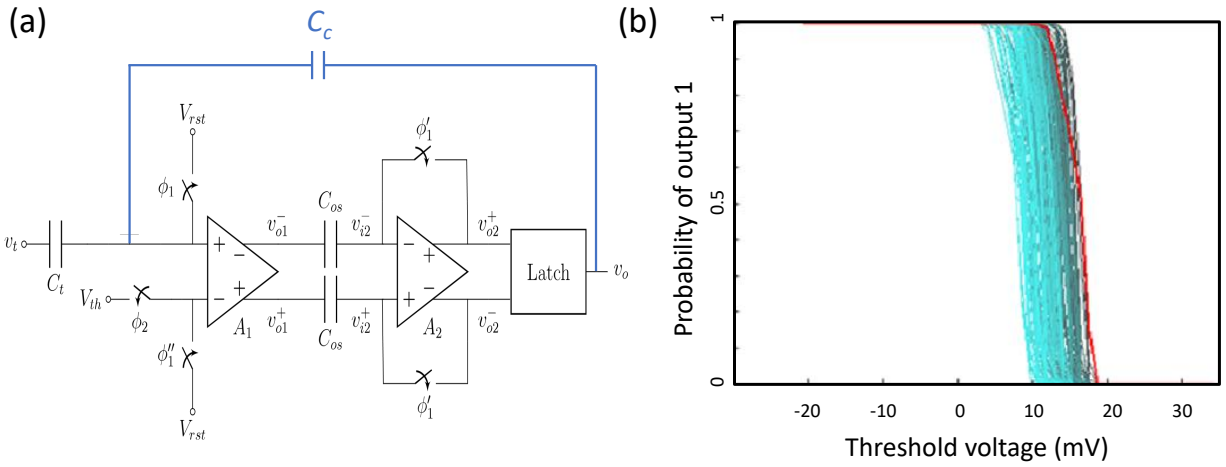



Figure 4.4: (a) Pixel schematic with coupling capacitance modelled between output and input. (b) Measured probability transfer characteristics of pixels from one row after fixing memory and cross-talk effects.

## 4.5 Monolithic Integration of an A-Se X-Ray Sensor

This section outlines the challenges and our solutions during the integration of the a-Se sensor with Chip 1. This integration is vital to achieving our photon-counting objective.

As shown in Figure 4.5, a 70-$\mu$m-thick a-Se sensing layer is deposited via thermal evaporation on Chip 1, and a high-voltage connection is manually attached to a 15-nm-thick gold bias electrode. After this, the chip is wirebonded.

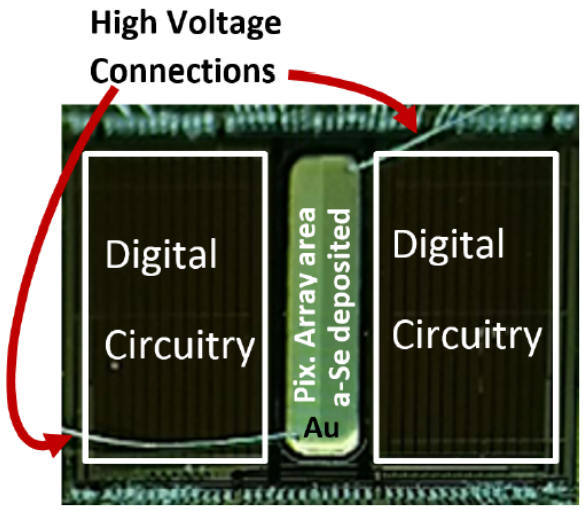



Figure 4.5: Post-processed Chip 1 with a-Se sensor, gold bias electrode, and high-voltage bias connections.

### 4.5.1 A-Se Sensor Delamination due to Thermal Effects

We initially observed a-Se delamination from the chip surface after powering the chip. As shown in Figure 4.6(a), the a-Se layer with gold has delaminated and rolled over to the left side of the active area. We speculate that a high temperature at the chip surface under the a-Se layer could be the main reason for this delamination. Therefore, to reduce the temperature, we reduce the pixel preamplifier biases by 25% while maintaining acceptable offset correction. Nevertheless, as shown in Figure 4.6(b), we observe delamination again. However, under the presented conditions, the a-Se sensor has maintained its shape but has lifted up from the ROIC surface. Therefore, we identify the rise in temperature as the

primary cause of delamination. We then further reduce the bias current from 820 mA to 430 mA. However, reducing the bias current and installing a heat sink on the back side of the PCB does not prevent delamination, as shown in Figure 4.6(c) and (d), but reduces its deteriorating impact.

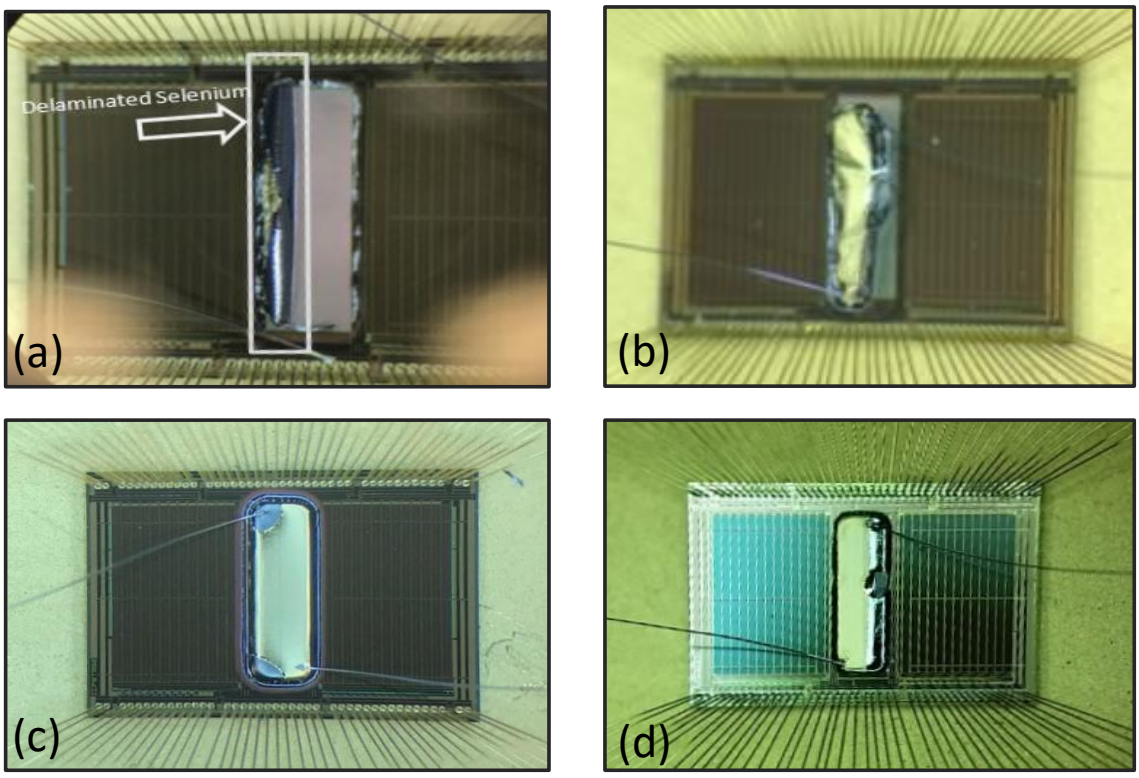



Figure 4.6: A-Se sensor delimitation from Chip 1 (a) under normal operation conditions, (b) with 25% reduced chip bias current, and (c) and (d) with the minimum possible chip bias current (i.e., 430 mA).

Based on the results above, we speculate that the two critical factors causing sensor delamination are the rate of temperature increase and the final temperature value. To assess these factors, we utilize an infrared radiation (IR) thermometer (FLIR TG165) to monitor the chip surface temperature under different experimental conditions. Using the measurements and thermal conductivity calculations for each material, we implement a cooling system to control both the rate of temperature increase on the chip and the steady-state temperature. Figure 4.7 shows the cross-section of the system. The cooling system involves drilling a hole in the PCB to access the backside of the package and attaching a

high-thermal-conductivity pad, which extends through the hole. We also connect a suitable Peltier cooler to the thermal pad on the back of the PCB. Another thermal pad is used to adhere the Peltier cooler to heat pipes, which efficiently transfer heat to a heat sink. We secure the heat sink to the heat pipes using a copper clamp. Lastly, we include a fan to enhance the thermal dissipation of the system.

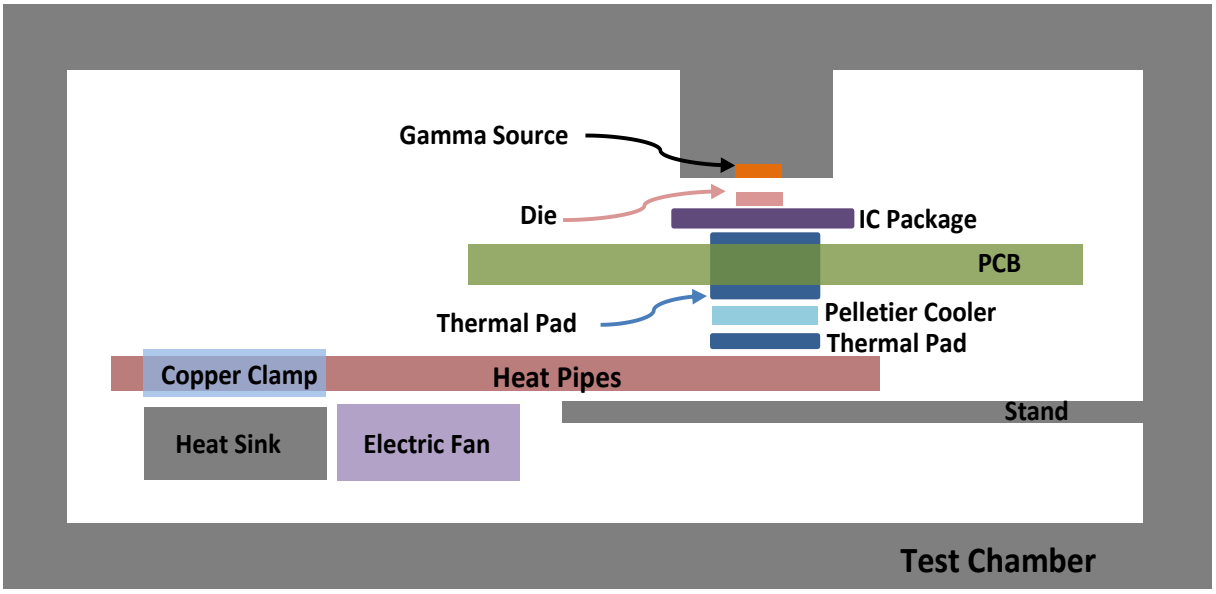



Figure 4.7: Cross-section of the cooling system designed to prevent a-Se sensor delamination on Chip 1.

Figure 4.8 illustrates the temperature variation of the chip over time, as measured using an IR thermometer, both before and after implementation of our temperature control measures. Prior to temperature control implementation, the average temperature of the chip and package exhibits a rapid increase at a rate of 7°C per minute during the initial three minutes. However, after the temperature control system is in place, the rate of temperature increase is reduced to 0.3°C per minute for the same initial three minutes. Additionally, the steady-state temperature is decreased from 42°C to 25°C while keeping the current at 430 mA.

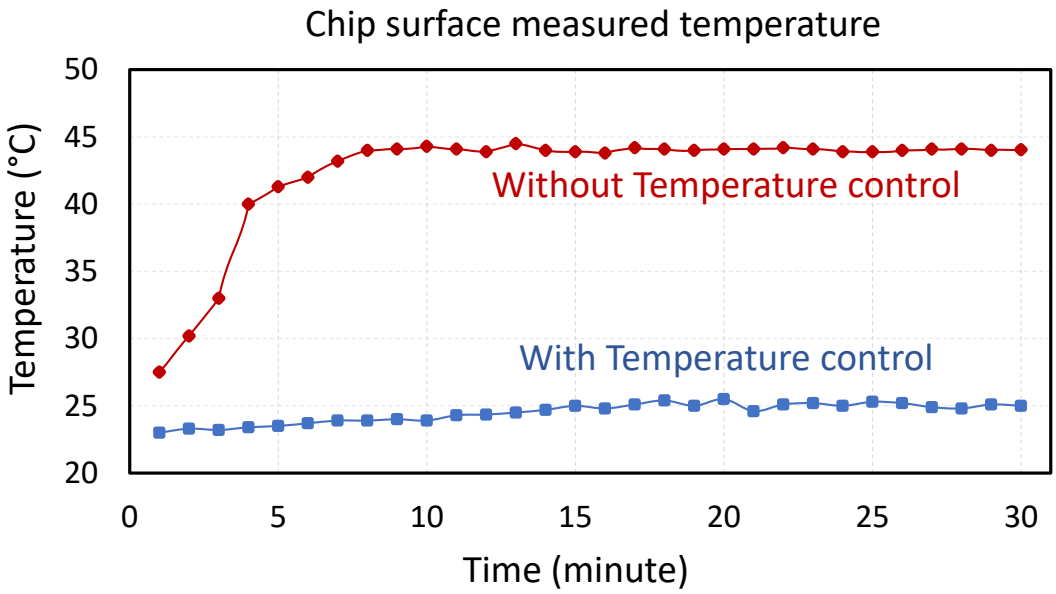



Figure 4.8: Measured temperature over time of Chip 1 with and without the temperature control system.

### 4.5.2 Failure due to High-Voltage Biasing

After resolving the a-Se delamination issue caused by high temperature, the next step is to bias the a-Se sensor with a high voltage to generate the necessary electric field. However, this process introduces new issues such as electric breakdown, a-Se crystallization, and shorted connections, shown in Figure 4.9.

Different cases of a-Se crystallization, shown in Figure 4.9(a) and (b), occur during the high-voltage bring-up process. Furthermore, with the next two chips, local defects on the a-Se/Au surface are also observed, as shown in Figure 4.9(c) and (d). In the case demonstrated by Figure 4.9(d), a defect is scattered onto the wirebonds, eventually leading to a short circuit in the chip, causing an electrical failure.

Given the unpredictability of breakdown occurrences, extensive chip characterization, testing, and optimization are essential before applying the high-voltage bias. This is made possible by the temperature control system, which prevents a-Se delamination throughout the bring-up process, as previously observed right after powering the imager without the cooling system.

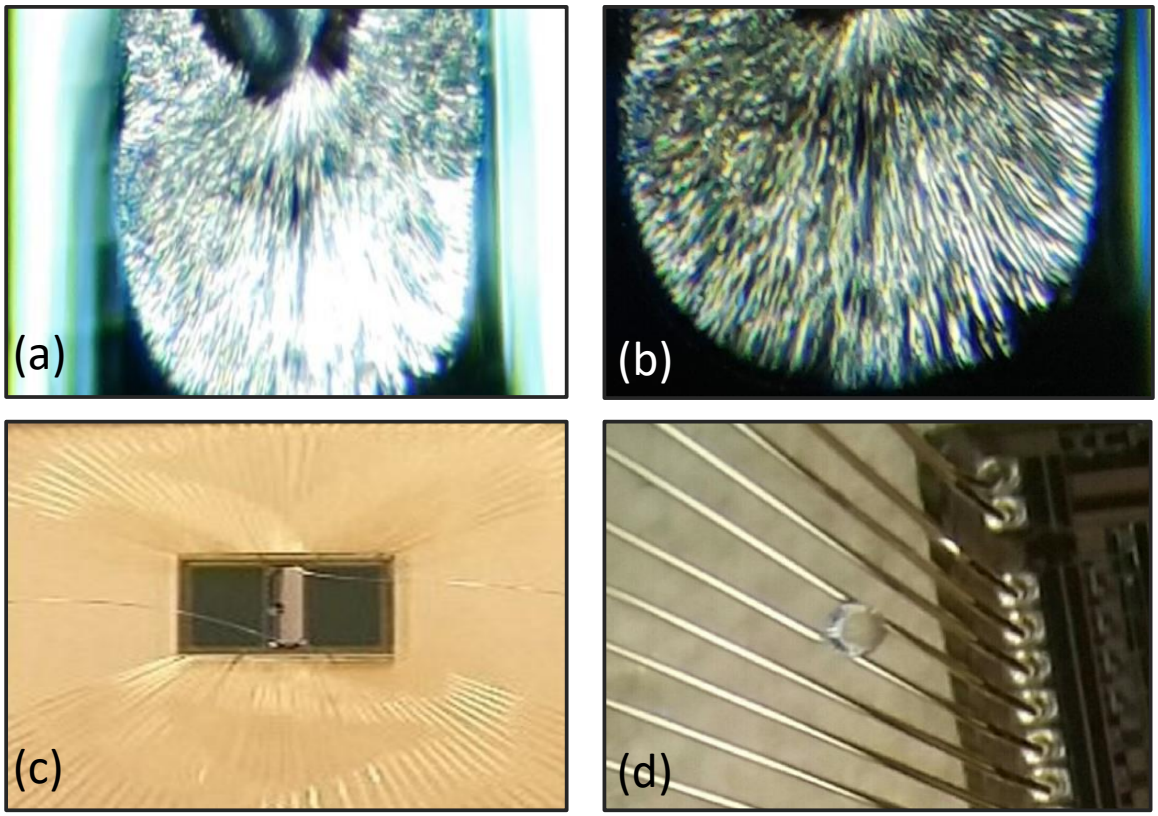



Figure 4.9: Electric-breakdown impact, where (a) and (b) show two incidents of a-Se crystallisation, (c) shows a-Se local delamination, and (d) displays shorted wirebonds.

However, high-voltage breakdown incidents cause all the chips to become completely nonfunctional. To overcome these challenges, we take a systematic approach by increasing the high voltage in 50-V steps, with fine 5-V increments per minute, while closely monitoring the chip's response to an $^{241}$Am gamma source. Notably, starting with an applied voltage of 300 V leads to a successful outcome, as explained in the next section.

## 4.6 Experimental Results

We now present the measured results of single-photon counting with an a-Se sensor monolithically integrated with the CMOS ROIC using a low-flux (10-$\mu$Ci activity) mono-energetic 60-keV $^{241}$Am source. The $^{241}$Am gamma source is positioned a distance of 6.5 mm above

the chip surface, as illustrated in Figure 4.10.

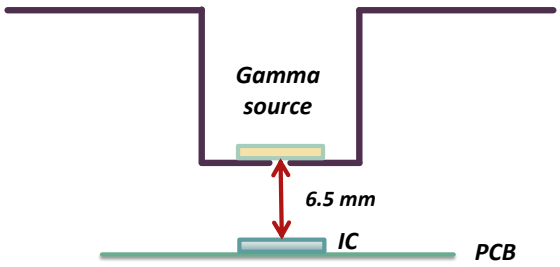



Figure 4.10: Gamma source positioning relative to Chip 1.

Our complete experimental setup is shown in Figure 4.11, where Chip 1, thermometric cooler, and the PCB are visible.

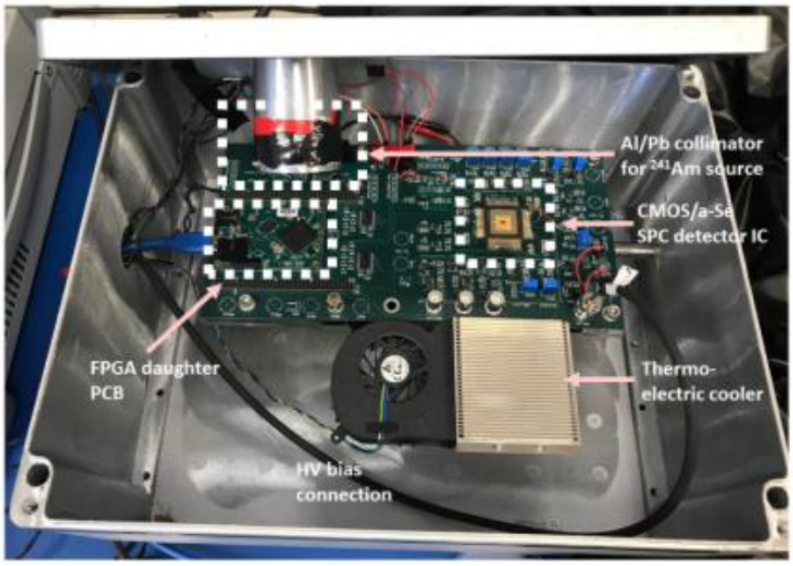



Figure 4.11: Single-photon counting experimental setup.

Electronic pixel verification results are shown in Figure 4.12. This characterization is performed before starting the single-photon-counting measurements. Figure 4.12(a) displays the photon hit probability versus the estimated charge at the input to one pixel in the row, revealing an input-referred noise of 190 $e^-_{\text{rms}}$. Additionally, Figure 4.12(b) shows the histogram of the threshold distribution for the row of pixels in our measurement.

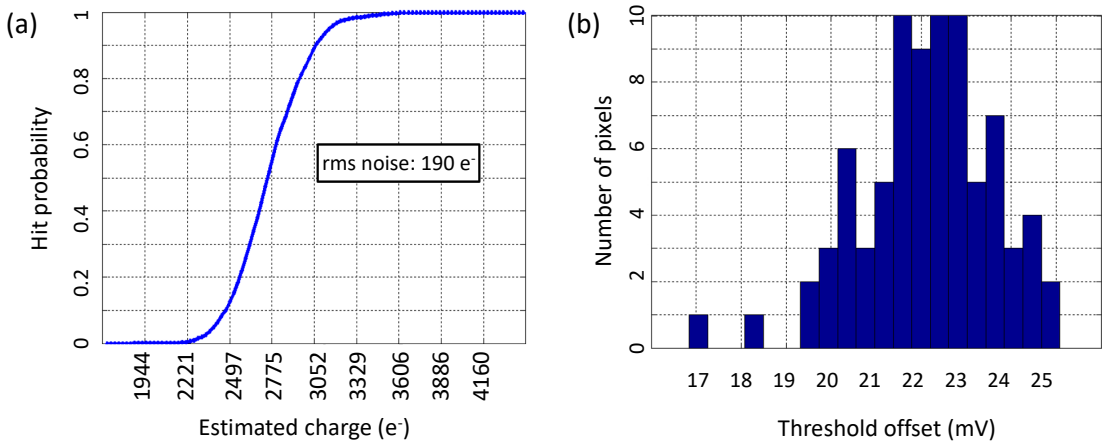



Figure 4.12: Electronic characterization of pixel performance. (a) Photon hit probability versus estimated charge at the input to one pixel. (b) Histogram of the threshold distribution for one row of pixels.

Figure 4.13 displays our single-photon-counting results from 80 adjacent pixels in one row of the imager, and with a 20-$\mu$s integration time, which is conducted both with and

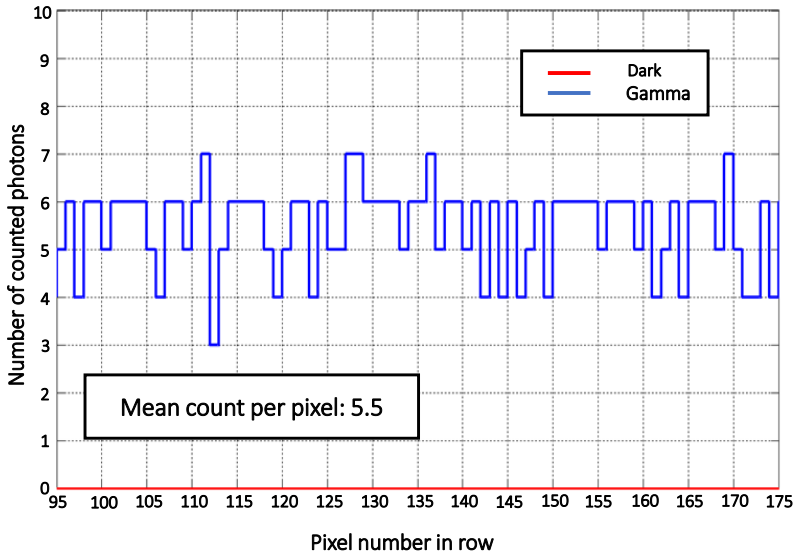



Figure 4.13: Measured single-photon-counting results.

without the $^{241}$Am source present. For this experiment, an applied voltage of 300 V, equivalent to 4.3 V/$\mu$m, is used. Notably, an average of 5.5 counts per pixel is recorded over the course of a 120-min experiment. No counts are observed when the $^{241}$Am source is absent. The histogram of counts is displayed in Figure 4.14.

These results demonstrate the feasibility of single-photon counting with a-Se monolithically integrated on a CMOS ROIC. However, due to chip performance limitations such as having access to the digital output of the pixels only, reduced bandwidth, and cross-talk restrictions, several questions remain unanswered. We therefore aim to investigate these in the imager designs presented in the upcoming chapters. Among these uncertain aspects, we particularly highlight the unknown accuracy of the measured number of counts, the sensor's quantum efficiency, the actual pixel response time for a single photon, the influence of the small-pixel effect, the impact of charge sharing between pixels on our counted number, and the potential effect of temperature.

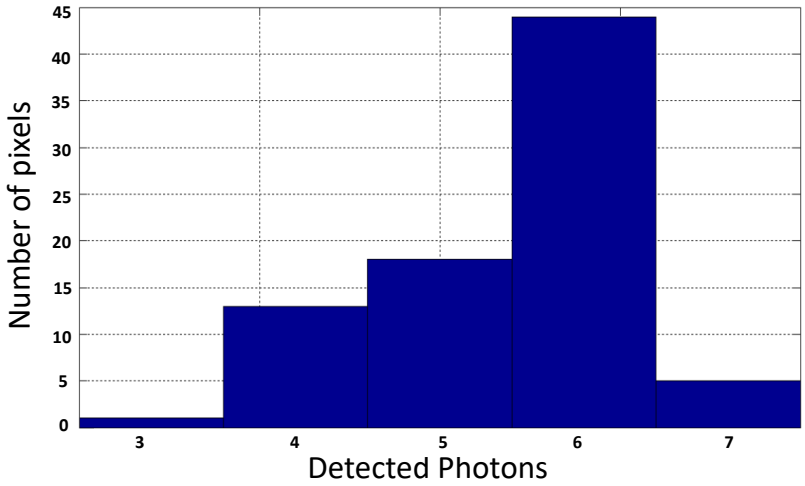



Figure 4.14: Measured histogram of counted photons.

We compare our measured results to theoretical values. The expected counted photon number is estimated by first assuming that the source is a point source and by determining the active area of the pixels. Figure 4.15 illustrates our estimation, where the chip is being exposed to a point source. We also show the chip's active area where photons can be detected. Since we are operating only one array, which consists of 196 $\times$ 26 pixels, the active area is 2.3 $\times$ 0.3 mm$^2$. With its 10-$\mu$Ci activity, the $^{241}$Am source emits 370 $\times$ $10^3$ photons/s. The sphere area shown in the figure is $4\pi r^2$, where $r$ is the sphere radius (source to die distance) of 6.5 mm. The photon flux incident on the chip's active

area is the emitted flux from the source multiplied by the ratio of the active area to the area of sphere. Consequently, the number of photons striking the active area is approximately $4 \times 10^3$ photons/s. This translates to 659 photons/pixel during our 120-min experiment.

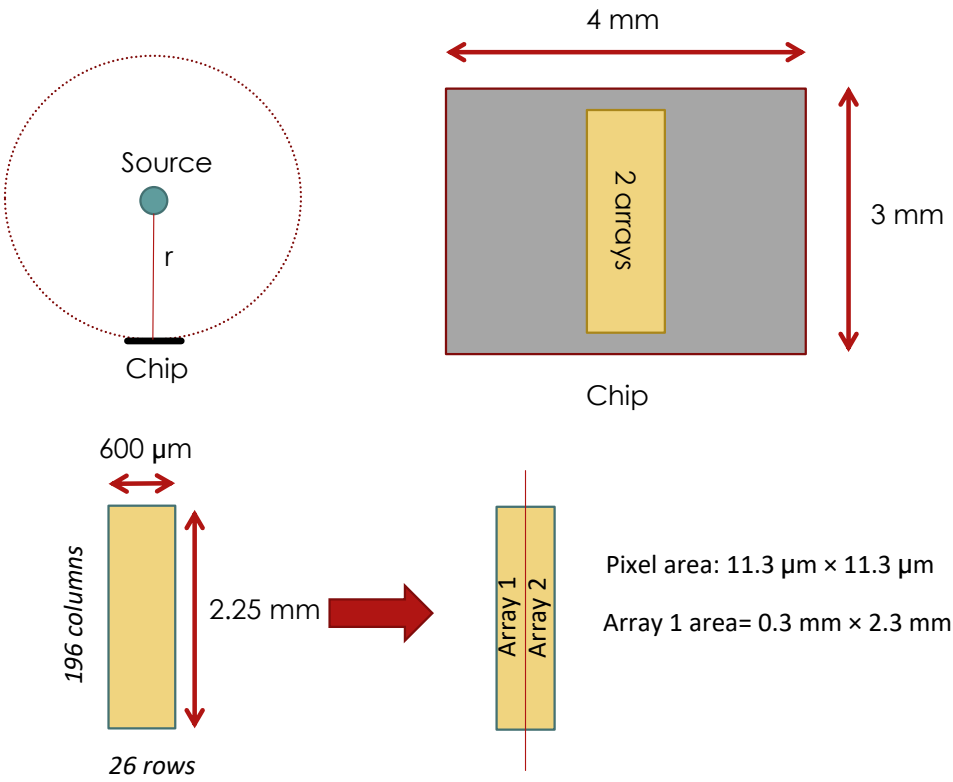



Figure 4.15: Chip 1 active area being exposed to a point gamma source

We estimate the QE of the a-Se sensor at around 3-5% at the applied electric field, a-Se thickness, and photon energy range based on [90]. Therefore, the number of photons being absorbed is about 19 to 33 photons per pixel. However, our counted photons are approximately 4 to 6 times less than the expected numbers. We attribute this discrepancy to the short 20-$\mu$s integration time, causing some absorbed photons to not be completely detected as we reset the integration capacitor.

Even if we achieve the precise number of photons to be detected with our current settings, the comparison may still lack reliability due to uncertainties related to cross-talk and temperature. The high sensitivity of the pixels to coupling with neighbouring pixels,

along with the small pixel area, contribute to charge sharing, making it challenging to determine the percentage of counted photons. Furthermore, variations in temperature can also impact the counted numbers by altering the threshold voltages.

## 4.7 Summary

We presented the feasibility of employing an a-Se sensor for X-ray photon counting through experimental demonstrations. This was achieved by monolithically integrating an a-Se sensor onto a CMOS ROIC. Our results are the first demonstration of single-photon counting using an a-Se sensor on a CMOS integrated circuit. Although this marks an important milestone, we will address several uncertainties and investigate our other research objectives in the upcoming chapters.

# Chapter 5

# Experimental Demonstration of the Small-Pixel Effect (Chip 2)

## 5.1 Introduction

After the successful demonstration of single-photon counting with a-Se monolithically integrated on a CMOS ROIC from Chapter 4, we now need to tackle the intrinsic limitations of a-Se, which prevent us from meeting our application requirements. In this Chapter, we report the first experimental demonstration of SPE with a-Se integrated on a CMOS ROIC (Chip 2). Our results highlight the untapped potential of SPE in dramatically improving the temporal resolution of an a-Se X-ray sensor. We demonstrate this improvement by measuring, for the first time, the intrinsic transient response of a-Se combined with a CMOS ROIC pixel. Our CMOS ROIC also leverages the lowest electronic noise reported for a-Se photon detection to demonstrate the first CMOS-integrated a-Se PHS results. We also report up to 2× and 5× improvement in energy resolution and photon detection error rate, respectively, by exploiting SPE.

Additionally, we provide device-level statistical simulations to elaborate on the detailed contribution of SPE to improving the energy and temporal resolution of an a-Se sensor for photon counting. These simulations underscore potentially greater performance enhancement of SPE for a-Se compared to that of other crystalline or polycrystalline sensor materials. Our simulated and measured results using a 59.6-keV mono-energetic $^{241}$Am gamma source reveals the overlooked potential of monolithic a-Se/CMOS to expedite the development of SPC detectors for DBCT.

## 5.2 Signal Formation in a-Se/CMOS Pixels and Small-Pixel Effect Impact

### 5.2.1 Signal Formation

In this section, we describe signal formation and SPE in our monolithic a-Se/CMOS imager. Figure 5.1 shows a simplified 3-D cross section of a monolithic a-Se/CMOS imager, with a single pixel slice and pixel electronics shown. The opening above the collection electrode allows the a-Se sensor, deposited using thermal evaporation, to be electrically connected to the pixel input. A second thermal evaporation is used to deposit the Au HV bias electrode. When a positive HV is applied to this electrode relative to the bottom (pixel) electrode, holes and electrons generated by a single X-ray photon absorbed by the a-Se sensor, drift towards the sensing electrode and bias electrode, respectively. The number of generated EHPs $N$ is given by $N = E_{ph}/E_{ion}$, where $E_{ph}$ is the photon energy and $E_{ion}$ is the a-Se ionization energy [104]. The generated carriers induce a time-varying charge signal $Q_{ind}$ on the pixel electrode, which is detected by a CSA in the pixel. The CSA, which is composed of an OTA and a resettable feedback capacitor $C_f$, linearly converts $Q_{ind}$ to an output voltage $V_{CSA}$, where $V_{CSA} = -Q_{ind}/C_f$. Voltage $V_{CSA}$ must normally be further processed in the pixel to threshold (bin) the energy of the incident photon. However, we do not implement or require on-chip energy binning in this chapter to study SPE.

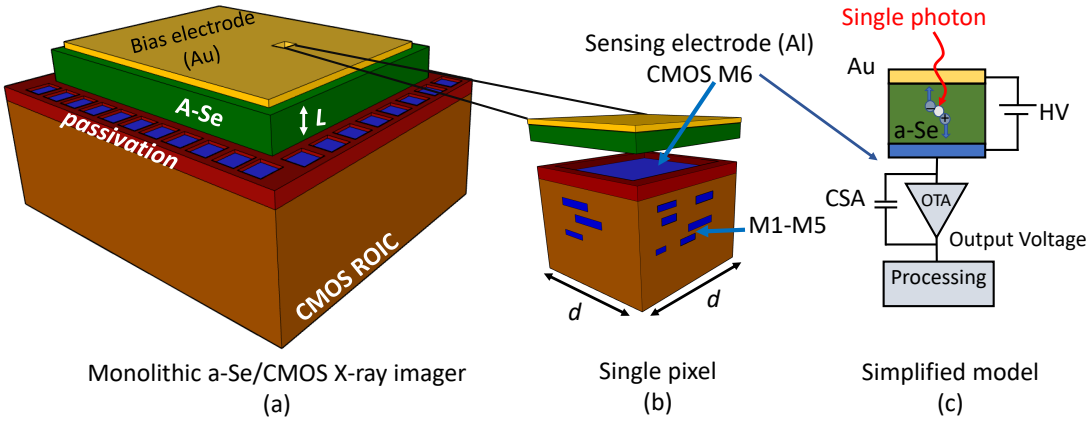



Figure 5.1: Overview of the proposed monolithic a-Se/CMOS imager. (a) 3-D cross-section of imager. (b) 3-D cross-section of a pixel "slice". (c) Simplified model of the material stack and pixel electronics.

The mobilities of X-ray-generated charge carriers in a semiconductor sensor have a significant impact on the energy resolution of an SPC imager. In a detector exhibiting high energy resolution, the difference between photon-generated charge $Q_{ph}$ and $Q_{ind}$, for a given $E_{ph}$, is relatively small. However, the energy resolution of an X-ray detector is reduced and mainly dominated by slow carriers when there is a considerable difference between $\mu_n$ and $\mu_p$, as with a-Se, for which $\mu_n = 0.003$ cm$^2$/Vs and $\mu_p = 0.15$ cm$^2$/Vs [35]. Therefore, we first numerically simulate the movement of charges to better understand the energy-resolution limitations of an a-Se sensor.

We use the Shockley-Ramo theorem to calculate $Q_{ind}$ in an SPC detector with an a-Se sensor, under the assumption that the generated charge density changes slowly so that quasi-static conditions are satisfied [39] [57] [58] [59] [60]. This approach is more computationally efficient compared to solving Maxwell's equations, which involves accounting for interactions between instantaneous electric and magnetic fields associated with a "cloud" of moving charge [39] [40] [57]. To illustrate the Shockley-Remo theorem, we consider how $Q_{ind}$ is formed, assuming only a single charge $Q_{ph} = q$, shown in Figure 5.2(a), is generated in a biased a-Se sensor with thickness $L$, following absorption of an X-ray photon. The a-Se sensor is sandwiched between two parallel electrodes: an HV electrode on the left and a collection (pixel) electrode on the right. We also assume that $q$ is generated on a horizontal line that intersects the pixel center. When $q$ drifts along lateral dimension $x$, starting from position $x = a$, to its final position $x = b$, then $Q_{ind}$ is given by

$$Q_{\text{ind}} = q \times [\Phi_\omega(b) - \Phi_\omega(a)], \tag{5.1}$$

where $\Phi_\omega(b)$ - $\Phi_\omega(a)$ is the difference in the weighting potential $\Phi_\omega$ at positions $a$ and $b$. Potential $\Phi_\omega$ is a dimensionless quantity that represents the normalized electric potential gradient across the semiconductor when the pixel sensing electrode has a weight normalized to unity, and the bias electrode is set to a weight of zero. For pixelated arrays, $\Phi_\omega$ is again the normalized electric potential gradient across the semiconductor when the target pixel electrode, at which $Q_{ph}$ is generated with the same vertical position of its center but with lateral distance of $L/2$, is set to unity. For example, in Figure 5.2(b) photon is absorbed at $x = L/2$ and $y = 0.5$, and the target electrode is the one at the middle with its center at $y = 0.5$. The bias electrode, as well as the other pixel electrodes, are defined to have a weight of zero.

For the sensor in Figure 5.2(a), where the pixel and HV-bias electrodes are equally sized and $L/d \ll 1$, $\Phi_\omega$ increases linearly along $x$, from $x = 0$ to $x = L$, for any vertical position $y$, where $y$ is normalized such that $0 \leq y \leq 1$. Consequently, when $q$ is generated at $x = L/2$ in the sensor, where $\Phi_\omega(\text{a}) = 0.5$, and drifts all the way to $x = L$, where $\Phi_\omega(b) = 1$, then $Q_{ind} = Q_{ph}/2 = q/2$, as calculated from (1). Therefore, $Q_{ind}$, found from measuring

$V_{CSA}$, is only 50% of $Q_{ph}$. As is evident, $Q_{ind}$ varies depending on the distance the charge travels within the sensor. Consequently, $Q_{ind}$ for a given $Q_{ph}$ can vary based on where $Q_{ph}$ is generated in the a-Se sensor and the distance it travels. This variation is random and, therefore, contributes to the reduction in energy resolution of the SPC detector.

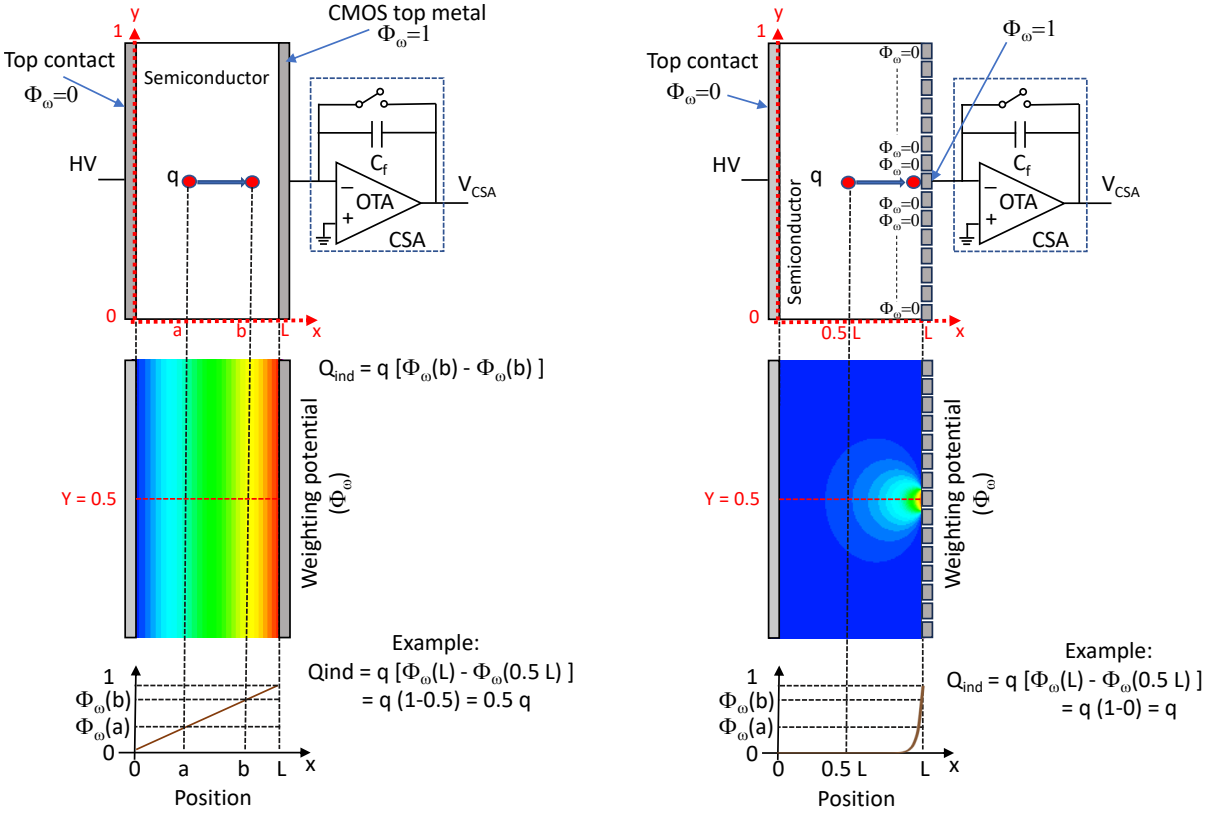



Figure 5.2: Signal formation with and without SPE using TCAD Sentaurus simulation. (a) Induced charge amount and weighting potential for a conventional sensor with parallel plates. (b) Weighting potential for pixelated small electrodes and an example, where the scaling has been adjusted for clarity and does not reflect actual dimensions.

### 5.2.2 Impact of SPE on Energy Resolution

The small-pixel effect is observed using an array of pixel electrodes with $L/d \gg 1$, as shown in Figure 5.2(b). As a consequence of SPE, $\Phi_\omega$ is no longer a linear function of $x$. Rather, $\Phi_\omega$ is negligible everywhere except in the vicinity of the pixel electrode, where it

exhibits a sharp non-linear increase for increased $L/d$ ratio. In this near-field shaping of $\Phi_\omega$, $Q_{ind}$ is influenced more by charges in close proximity to the pixel-electrode surface. In Figure 5.2(b), the CSA monitors $Q_{ind}$ at the center electrode and all adjacent pixel electrodes are biased at the same potential. We use finite-element-modeling CAD software (Sentaurus) to compute $\Phi_\omega$ in two dimensions for the center pixel electrode only, where $L = 120$ $\mu$m and $d = 7.5$ $\mu$m [with a pixel center-to-center spacing (pitch) of 8.5 $\mu$m], so that $L/d = 16$. Charge $Q_{ph} = q$, generated at a position with coordinates $x = L/2$ and $y = 0.5$, and drifting along a horizontal path to its final position at $x = L$, produces $Q_{ind}$ of approximately $q$, and not $q/2$, as was the case for a linear $\Phi_\omega$. This result demonstrates how SPE reduces the deviation in $Q_{ind}$ for photons with the same $Q_{ph}$, but absorbed at different locations within the sensor. As a result, we can exploit SPE to improve the energy discrimination of a monolithic a-Se/CMOS SPC detector.

The impact of SPE becomes more significant as $L/d$ exceeds unity. Figure 5.3(a) shows $\Phi_\omega$ in a sensor with $L = 120$ $\mu$m for $d$ ranging from $L$ down to 7.5 $\mu$m. As $L/d$ increases from one to sixteen, the region of highest $\Phi_\omega$ shrinks while a greater portion of the sensor area exhibits $\Phi_\omega$ of nearly zero. Figure 5.3(b) shows $\Phi_\omega$, at position $y = 0.5$, plotted against $L$ for the same $d$ values included in Figure 5.3(a). The rate of change of $\Phi_\omega$ with $x$ is maximized for the smallest $d$ we consider, as $x$ approaches $L$. Figures 5.3(a) and (b) illustrate this by showing the modeled weighting gradient and function as the lateral position of the sensor, respectively, for pixel dimensions 120 $\mu$m to 7.5 $\mu$m with 120-$\mu$m-thick a-Se.

## 5.3 Impact of SPE on Temporal Resolution

The temporal resolution of an SPC detector, which defines the maximum count rate, is also impacted by the slow-moving electrons of the a-Se sensor. To explain this relationship, we assume, for simplicity, that a photon interaction generates a single EHP, and each carrier drifts laterally to its respective electrode from the center of the sensor. We also do not consider the impact of charge sharing due to cloud diffusion, Compton scattering, or any electrical coupling between pixels. In a conventional a-Se detector with two large parallel-plate electrodes for which $L/d \ll 1$, shown in Figure 5.4(a), both electrons and holes contribute to $Q_{ind}$. Figure 5.4(a) also displays the normalized hole-induced charge $Q_{ind,h}$ and electron-induced charge $Q_{ind,e}$, as each carrier drifts to its respective electrode. In this case, with $Q_{ph} = q$, then $Q_{ind,h} = |Q_{ind,e}| = q/2$, since each carrier travels a distance of $L/2$ and the $\Phi_\omega$ gradient is linear. Therefore, the total induced charge $Q_{ind} = Q_{ind,e} + Q_{ind,h} = q$ once both carriers reach their respective electrodes, and the signals increase linearly

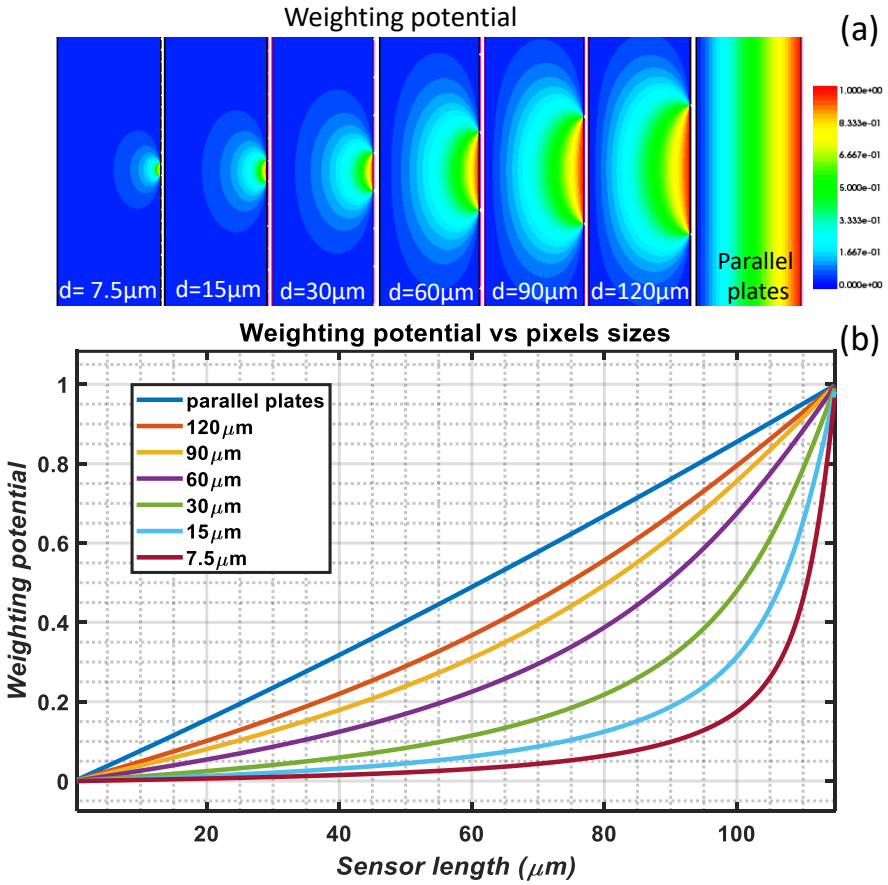



Figure 5.3: TCAD Sentaurus modeling for a 115-$\mu$m-thick a-Se sensor with different sensing electrode sizes. (a) Weighting potential gradient. (b) Weighting potential as a function of pixel dimension (sensor length $L$).

with time. Figure 5.4(a) also shows that the settling time of $Q_{ind}$ is mainly determined by the settling time of $Q_{ind,e}$. As a result, the slower electrons in a-Se are responsible for reducing the temporal resolution of the detector.

Conversely, if we consider the temporal resolution of the pixel-array detector in Figure 5.4(b), where $L/d = 16$, SPE now comes into play and improves the temporal resolution by attenuating the dependence of electron drift on $Q_{ind}$, compared to the detector in Figure 5.4(a). Applying the same assumptions to the detector in Figure 5.4(b) as we did for that in Figure 5.4(a), we see that $Q_{ind,e} \approx 0$ due to the negligible $\Phi_\omega$ far from the pixel electrode. On the other hand, when the hole drifts toward the pixel electrode, the

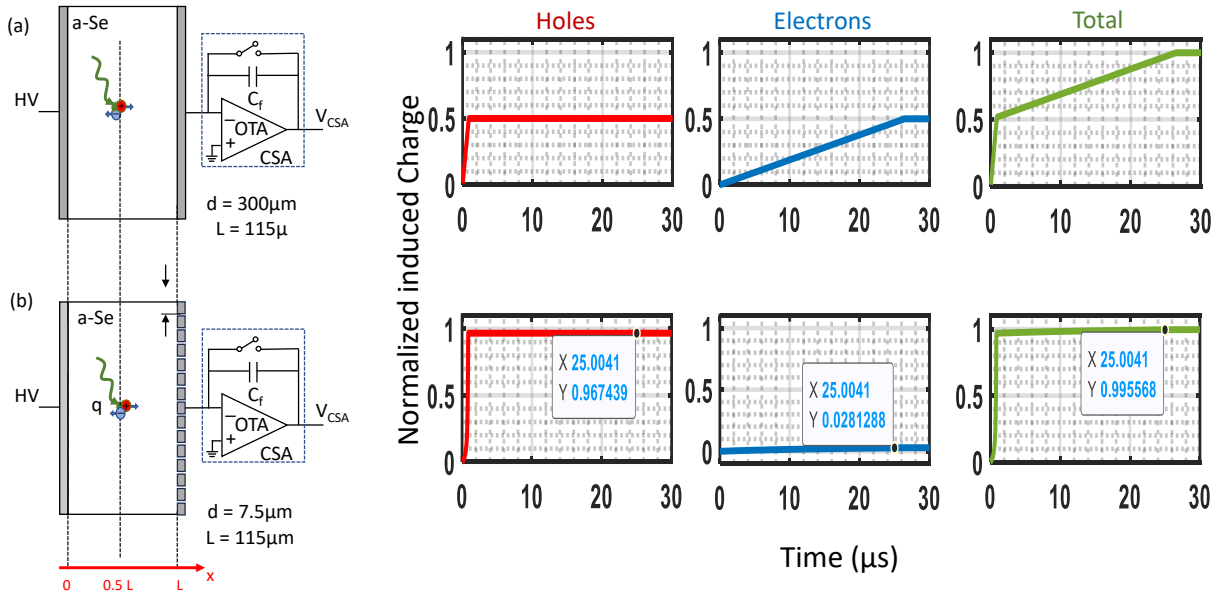



Figure 5.4: Signal formation, with and without SPE enhancement, using TCAD Sentaurus modeling. (a) Conventional transient response for a 115-$\mu$m-thick a-Se sensor with parallel plate electrodes. (b) Transient response for 115-$\mu$m-thick a-Se with 7.5-$\mu$m sensing electrodes demonstrating the impact of SPE.

hole will not induce any charge until it is in close proximity to this electrode, where $\Phi_\omega$ in non-negligible. Consequently, $Q_{ind,h}$ will reach a steady-state value of approximately $q$ in a relatively short period of time once the hole enters the near-field region of the pixel electrode. Therefore, $Q_{ind} \approx Q_{ind,h}$ and the settling time of $Q_{ind}$ is much shorter compared to the detector in Figure 5.4(a), significantly improving the detector temporal resolution. We note that SPE results in a two-fold enhancement in temporal resolution by two processes: first by eliminating the slow-electron contribution, and second by further reducing the settling time of $Q_{ind,h}$.

## 5.4 Impact of Charge Trapping

Next, we investigate how random trapping and de-trapping of generated carriers diminishes the energy and temporal resolution of an a-Se-based SPC detector, and how these limitations could be overcome by exploiting SPE. Due to the amorphous structure of a-Se, charge

carriers have a higher probability of being trapped compared to carriers in polycrystalline or crystalline materials. Furthermore, since the carrier lifetime of holes $\tau_h$ and electrons $\tau_e$ in a-Se are approximately 1 $\mu$s, and $\mu_p$ is about 50$\times$ greater than $\mu_n$, the likelihood of electrons being trapped is about 50$\times$ higher than for holes. Therefore, the energy- and temporal-resolution limitations due to electron trapping and de-trapping are also greater by the same factor compared to that of holes. Table 2.1 summarizes the electronic properties of a-Se in comparison to other commonly-used $x$-ray-sensitive materials.

Figure 5.5(a) shows two sets of modeling conditions, where we statistically model the SPC detector energy- and temporal-resolution dependence on (1) the lateral position where the photon is absorbed (absorption depth), and (2) the variation in the period between the time when an electron is generated and the time when it is trapped, for both a conventional and SPE-enhanced detector. First, we examine the effect of absorption depth by considering Simulation 1 in Figure 5.5(b), in which a photon is absorbed at three different $x$ values, and the electron is trapped after traveling a distance of $0.2L$ towards the HV electrode. The top row of graphs in Figure 5.5(b) shows how the photon interaction depth degrades the energy and temporal resolution of a conventional a-Se detector, for which $L/d = 0.38$. Since the electron travels only 0.2 $L$ before being trapped, its contribution to the total normalized induced charge magnitude $Q_n$, where $Q_n = \left|\frac{Q_{ind}}{q}\right|$, is less than 0.5 in steady state. In addition, the generated hole travels a distance of $L - x$ (where we have assumed the hole is not trapped), and, therefore, the hole contributes a greater proportion of $Q_n$ compared to the electron. Consequently, the steady-state $Q_n$ is different for each $x$ value, even though the photon energy remains constant. This, in turn, limits the energy resolution of the SPC detector. Moreover, the rise time $t_r$, which is established mainly by the slow electrons, also varies with $x$, limiting the temporal resolution.

When the detector is designed to take advantage of SPE, as shown in the second row of graphs in Figure 5.5(b) where $L/d = 4.2$, the effect of photon interaction depth on $Q_n$ is mitigated dramatically. This is because the contribution of the electron to $Q_n$ can be neglected since $\Phi_\omega$ is very small over the distance the electron travels. In addition, the energy-resolution reduction caused by hole movement is less significant because most of the distance $L - x$ lies outside the near-field region of the pixel electrode. As a result, for each value of $x$, the hole moves through the near-field region, contributing a similar amount of charge in each case, which leads to better energy resolution. Moreover, SPE improves the temporal resolution of the SPC detector because the contribution of the slow electron to $t_r$ is reduced while the hole passes through the near-field region.

The bottom row of graphs in Figure 5.5(b) displays statistical analysis results from Simulation 1, where steady-state $Q_n$ PHS and rise time spectrum (RTS), resulting from

$10^4$ random photon interaction depths, uniformly distributed over $L$, are provided for a conventional detector and one exhibiting SPE. The histograms show that when interaction depth is the only source of uncertainty in the detector, then SPE improves the mean steady-state $Q_n$ ($\mu_{Q_n}$) and mean $t_r$ ($\mu_{t_r}$) by factors of approximately 6× and 7×, respectively. Furthermore, the standard deviations of steady-state $Q_n$ and $t_r$ (denoted $\sigma_{Qn}$ and $\sigma_{t_r}$, respectively), are both 18× smaller with SPE than for the conventional detector.

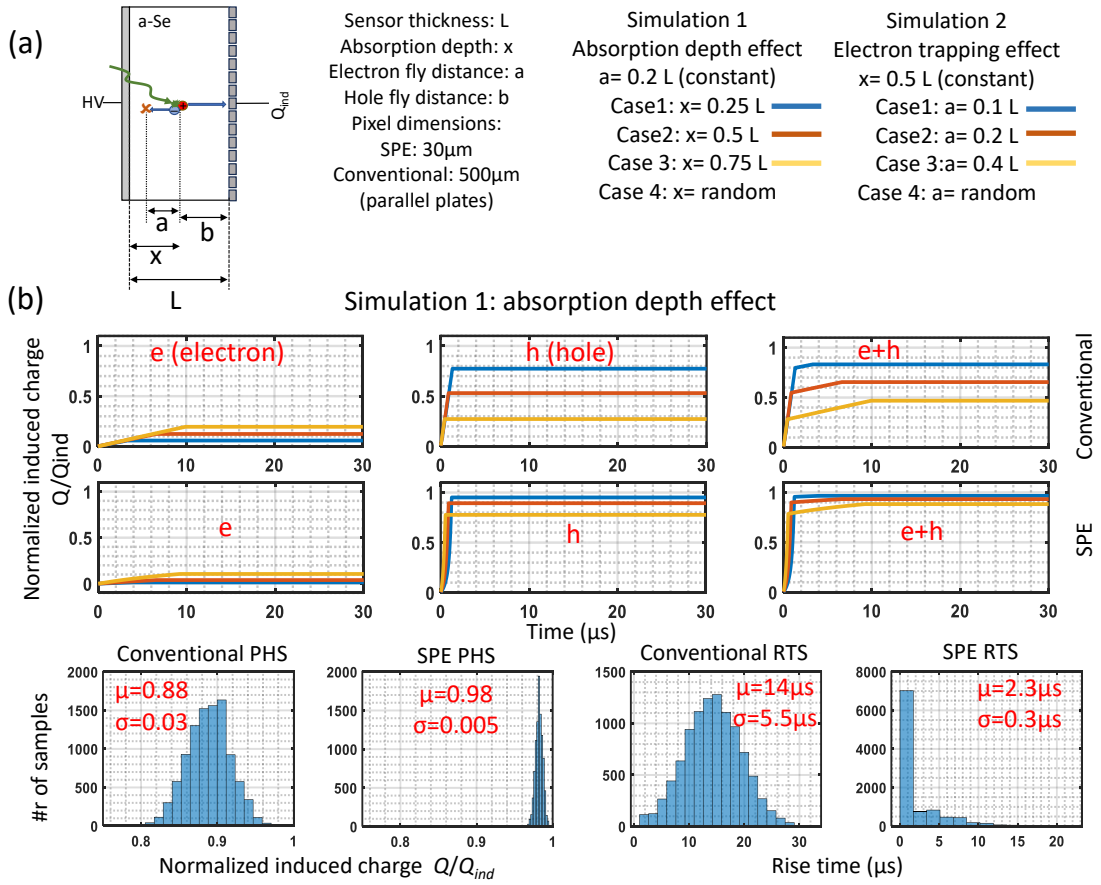



Figure 5.5: Improved temporal and energy resolution with SPE based on statistical simulation with TCAD Sentaurus. (a) Defining the parameters with simulation specifications for absorption-depth effect and electron random-trapping effect. (b) Simulating the absorption-depth effect for three different depths and with statistical analysis showing the electron, hole, and total-induced charge, PHS, and rise-time spectrum (RTS) for SPE-enhanced and conventional structures.

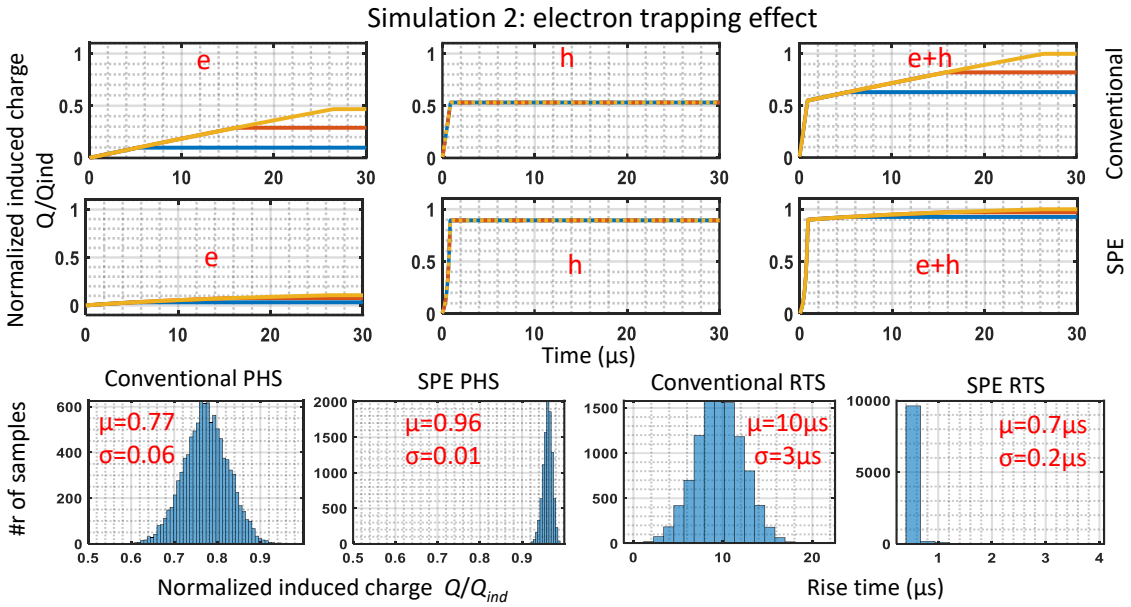



Figure 5.6: Simulating the electron random-trapping effect for three different trapping distances and with statistical analysis showing the electron, hole, and total-induced charge, PHS, and RTS for SPE-enhanced and conventional structures.

In Simulation 2, shown in Figure 5.6, we examine the energy and temporal resolution for both a conventional and SPE-enhanced detector for the case where the incident photon is absorbed at the center of the detector (i.e., where $x = 0.5\ L$), but the electron is trapped after traveling different distances towards the HV electrode. The top row in Figure 5.6 displays the effect of variations in how far the electron travels before being trapped in a conventional detector for three different trapping distances. Since the photon is absorbed at the center, the hole travels the same distance in each case and, therefore, its contribution to $Q_n$ in steady state is 0.5. However, because the electron travels different distances, over which $\Phi_\omega$ is linear, energy and temporal resolution will be reduced for the same reasons we presented in our discussion of Simulation 1. Conversely, energy and temporal resolution are improved in an SPE-enhanced detector, as shown in the middle row of graphs in Figure 5.6. The results from statistical analysis, displayed in the bottom row of graphs in Figure 5.6, demonstrate improvements of 6× and 14× in $\mu_{Qn}$ *and* $\mu_{t_r}$, respectively, for an SPE-enhanced detector compared to a conventional one.

When examining the effect of random trapping and photon interaction depth on detector resolution, it becomes evident that the slower carrier limits the resolution, particularly

in materials like a-Se, with substantial disparities in electron and hole mobility. Our modeling demonstrates how SPE improves the energy- and temporal resolution by mitigating the effect of sluggish electrons in a-Se. Consequently, the influence of SPE is anticipated to be more substantial in a-Se than in materials like CZT and CdTe, which possess less significant variations in electron and hole mobility. Although the SPE-enhanced energy- and temporal-resolution of an a-Se sensor still lag behind those of CZT and CdTe, the performance of a-Se is adequate to meet demanding application requirements for commercially-available detectors. Our modeling and analysis suggest that monolithic integration of an a-Se sensor with CMOS, and appropriate pixel sizing to leverage SPE, could surmount significant challenges in achieving large-area scalable SPC detectors.

## 5.5 Chip Design

To experimentally demonstrate SPE and its potential in improving the intrinsic limitations of an a-Se sensor, we design Chip 2. Here, we present the design, simulation, and fabrication details of this Chip.

### 5.5.1 Pixel Front-End CSA

In Section 3.3, we established the pixel ROIC specifications required to satisfy both the rigorous demands of DBCT and our quest to explore potential enhancements through SPE. In Chip 2, we design the analog input stage of our pixels, featuring a CSA with a 10-fF integration capacitor $C_f$ and with an n-channel metal-oxide semiconductor (NMOS) transistor for the feedback/resistive discharge pathway, as depicted in Figure 5.7. Here, we proceed to determine the specifications required for the OTA in this design.

The target pixel count rate of 1.5 Mcps translates to a photon-processing time of 660 ns. We target the minimum $t_r$ of 330 ns, which is half the photon-processing time. With our ideal target ER of 0.13%, $t_r$ will be equal to 6.6 $\tau$. Therefore, with $\tau$ = 50 ns, which translates to a required OTA gain-bandwidth product (GBW) of 3.2 MHz. However, we design for 3.5 MHz to maintain extra margin. In our design, we consider the CSA load capacitance $C_o$, which contains the output capacitance of the OTA and input capacitances from the two comparators needed to design a complete SPC pixel. We estimate $C_o$ to be 200 fF. We assume a maximum voltage step resulting from photon impact to be 50 mV, with a substantial 5-fold margin, which translates to a slew rate of 3.5 V/$\mu$s. In addition, while a 0.13 % error rate corresponds to a dc gain of approximately 800 V/V, we aim

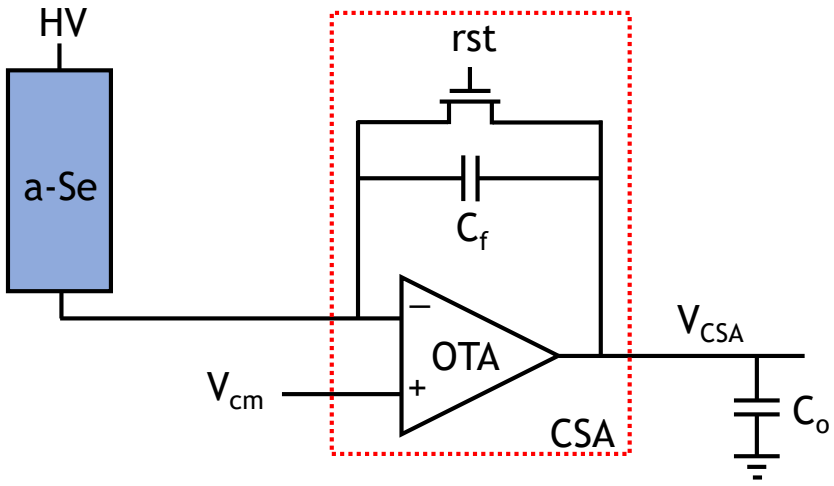



Figure 5.7: Chip 2 pixel charge-sensitive amplifier.

for a dc gain of 1000 V/V (60 dB) to provide margin. Moreover, to maintain low power consumption and avoid chip overheating while meeting speed, noise, and gain requirements, we have opted for the telescopic-cascode OTA architecture, illustrated in Figure 5.8.

We design the CSA with a reset-control multiplexer and a transmission gate at the output to choose the desired pixel within the array. Figure 5.9(a) shows the implemented CSA and Figure 5.9(b) shows the layout of the pixel with 30-$\mu$m pitch.

### 5.5.2 Array Design and Chip Architecture

We design the chip with five arrays, each featuring different pixel sizes, including pitches of 30, 60, 90, and 120 $\mu$m, as shown in Figure 5.10. Array 1 comprises 12 $\times$ 11 square pixels, each with dimensions of 27 $\mu$m with 30-$\mu$m pitch. Array 2 consists of 8 $\times$ 10 square pixels, each measuring 57 $\mu$m in dimension and with a pitch of 60 $\mu$m. Array 3 features 6 $\times$ 10 square pixels, each with a dimension of 87 $\mu$m and a pitch of 90 $\mu$m. Array 4 comprises 8 $\times$ 7 square pixels, each measuring 117 $\mu$m in dimension and with a pitch of 120 $\mu$m. This difference in sizing of pixels enables us to thoroughly investigate the effects of SPE on performance. The pixels share an output bus in a column-wise fashion, with the transmission gate at the output of the pixel's CSA activated when a specific row is selected. To facilitate the selection of four pixels from each row, an analog multiplexer

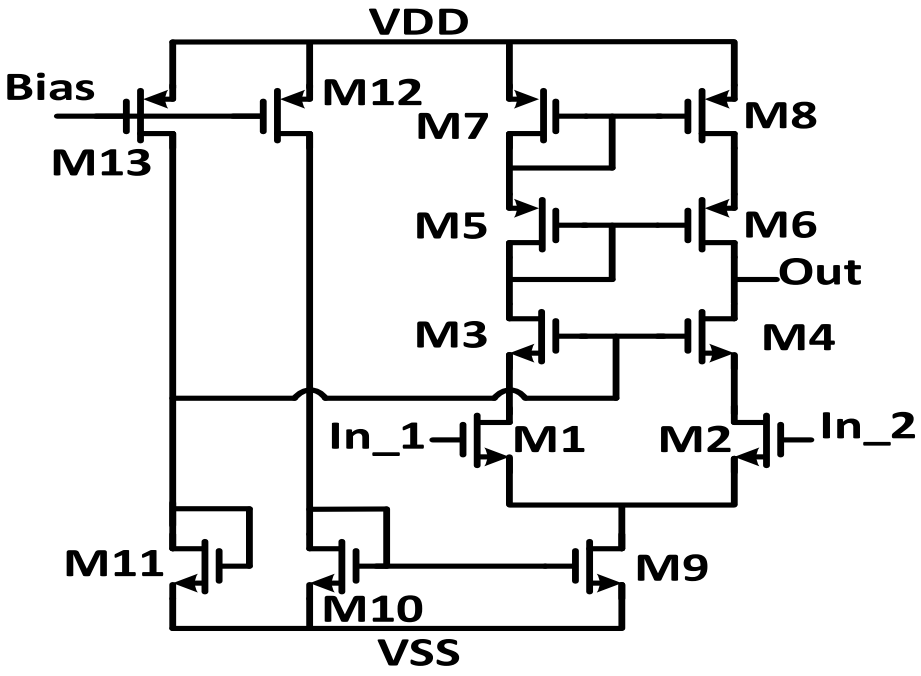



Figure 5.8: Telescopic-cascode OTA designed for the Chip 2 pixel.

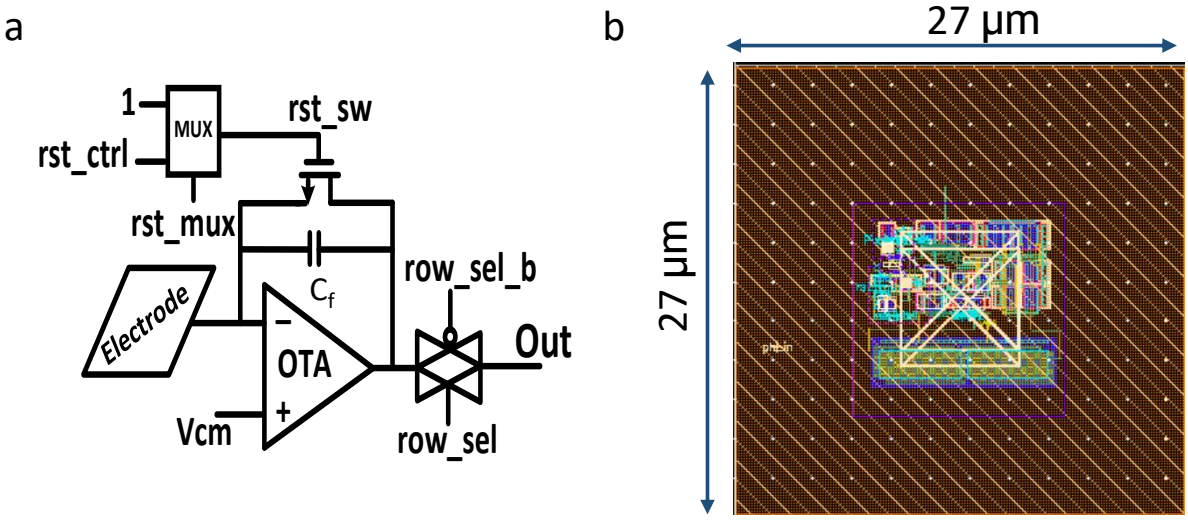



Figure 5.9: Chip 2 pixel: (a) Implemented CSA and (b) pixel layout.

is positioned at the output of a row of pixels. Subsequently, the output from the CSA is connected to an analog buffer, which is linked to an analog output pad. Additionally, for the purpose of characterization, two larger pixels with a 300-$\mu$m pitch are included.

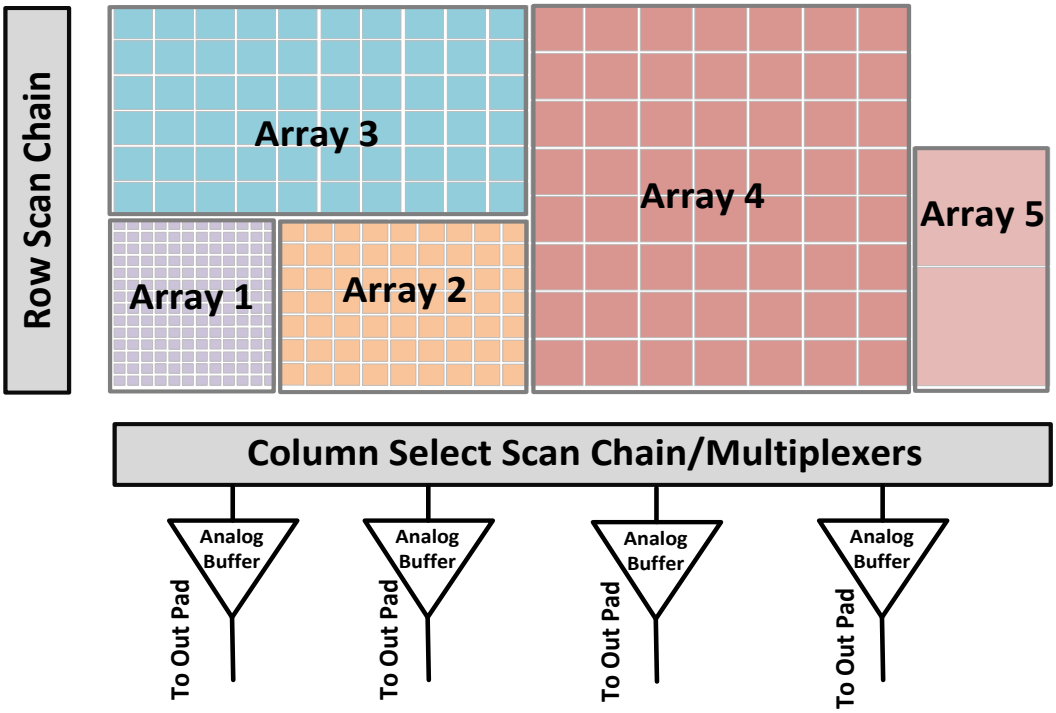



Figure 5.10: Chip 2 architecture.

## 5.6 Fabrication and Post-Processing

### 5.6.1 Chip Fabrication

The chip is fabricated in a 0.18-$\mu$m analog/mixed-signal one-poly six-metal (1P6M) mixed-signal CMOS process. Figure 5.11 shows the fabricated chip micro-graph with its floor-plan. The chip occupies an area of 1.5 $\times$ 2.5 mm$^2$, and it contains 5 arrays of different pixel sizes. Each pixel consumes 11 µW from a 1.8-V supply.

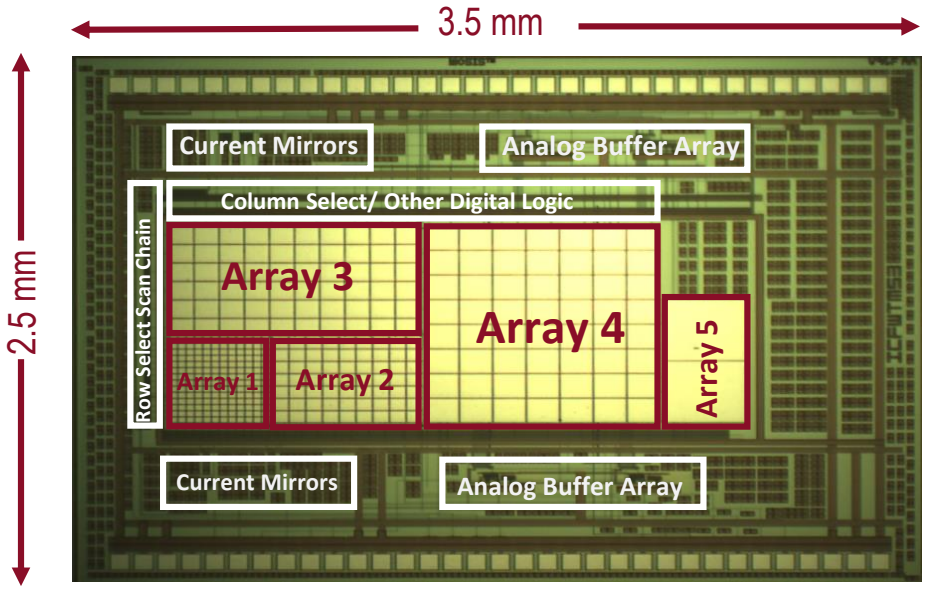



Figure 5.11: Fabricated Chip 2 micrograph.

### 5.6.2 Shadow Masks for a-Se/Au Post-Processing

We designed two shadow masks for a-Se and Au deposition on Chip 2. The masks contain five different arrays shown in Figure 5.12. Each array has slightly different opening sizes, around 2.5 mm $\times$ 2 mm, to ensure the chips fit and accommodate the 30-$\mu$m machining tolerance. We fabricate our shadow masks using 2.5-mm-thick 7075 aluminum. Figure 5.12 shows the fabricated masks for a-Se sensor deposition and the chip exposed area before processing.

### 5.6.3 Wirebonding and Packaging

Figure 5.13 shows a micrograph of our post-processed, wirebonded, and high-voltage connected chip. To increase the SPE enhancement factor, we increase the a-Se sensor thickness as much as can be reliably processed. The thermally-evaporated 115-µm-thick a-Se sensor is covered with a 50-nm-thick Au electrode. We also make the high-voltage connection to the bias electrode manually using silver epoxy.

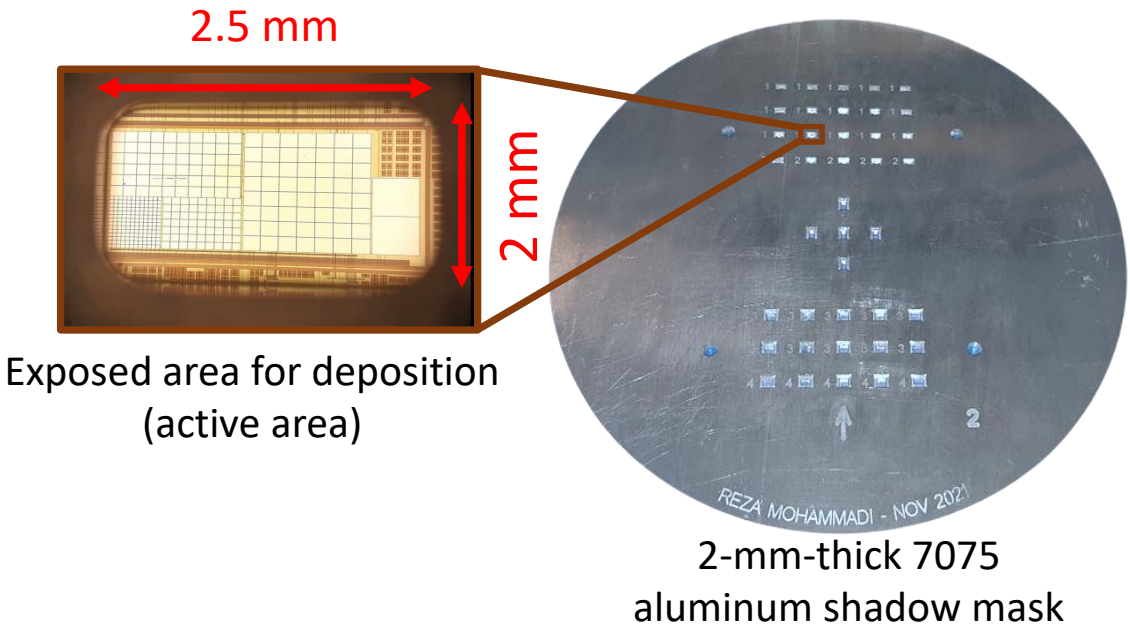



Figure 5.12: Fabricated shadow masks for Chip 2 post-processing.

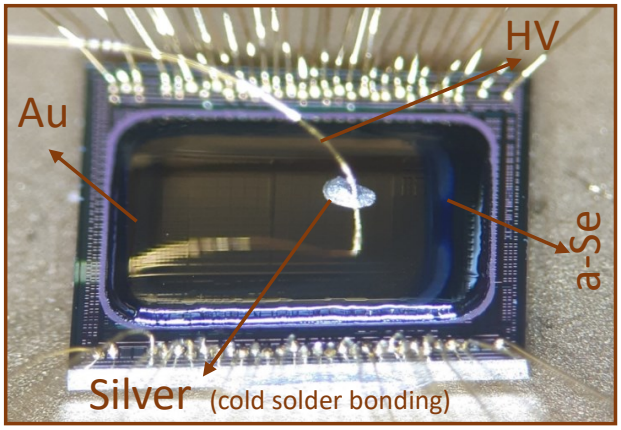



Figure 5.13: Micrograpf of Chip 2 after post-processing.

Following chip post-processing, we conduct in-house wirebonding of Chip 2. Our wirebonder has a nominal resolution of 120 $\mu$m, which presents a challenge given our pad

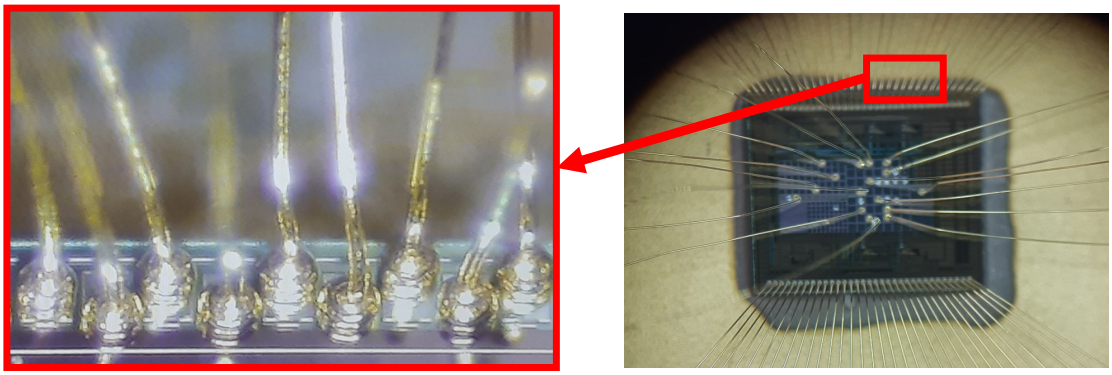


Figure 5.14: Chip 2 after wirebonding.

pitch of 75 $\mu$m. To address this, we employ a staggered bonding technique, as depicted in Figure 5.14. We also wirebond a few pixel pads in each array on, un-processed chips. As a result, we can apply current pulses directly to the pads, allowing more precise pixel characterization.

## 5.7 Experimental Results

In this section, we provide an overview of our custom test PCB and its key blocks, along with the PC interfacing modules. We then present the results of electronic characterization of Chip 2.

### 5.7.1 PCB Design

We design a custom four-layer PCB for the electronic characterization of Chip 2, as illustrated in Figure 5.15. The 30 cm $\times$ 22 cm PCB serves multiple functions, including biasing the analog voltage and current inputs of the IC, generating digital signals to operate selected pixels, and transferring the chip outputs to a personal computer (PC) for processing. Additionally, the PCB distributes power throughout the system while maintaining analog/digital isolation. The analog/mixed-signal power domain contains the imager, biasing circuits, and data converters. The digital power domain comprises a field-programmable gate array (FPGA) on a separate board, powered by low drop-out (LDO) regulators, that generate digital control signals and acquire serial data, followed by a universal serial bus (USB) bridge to interface with a PC.

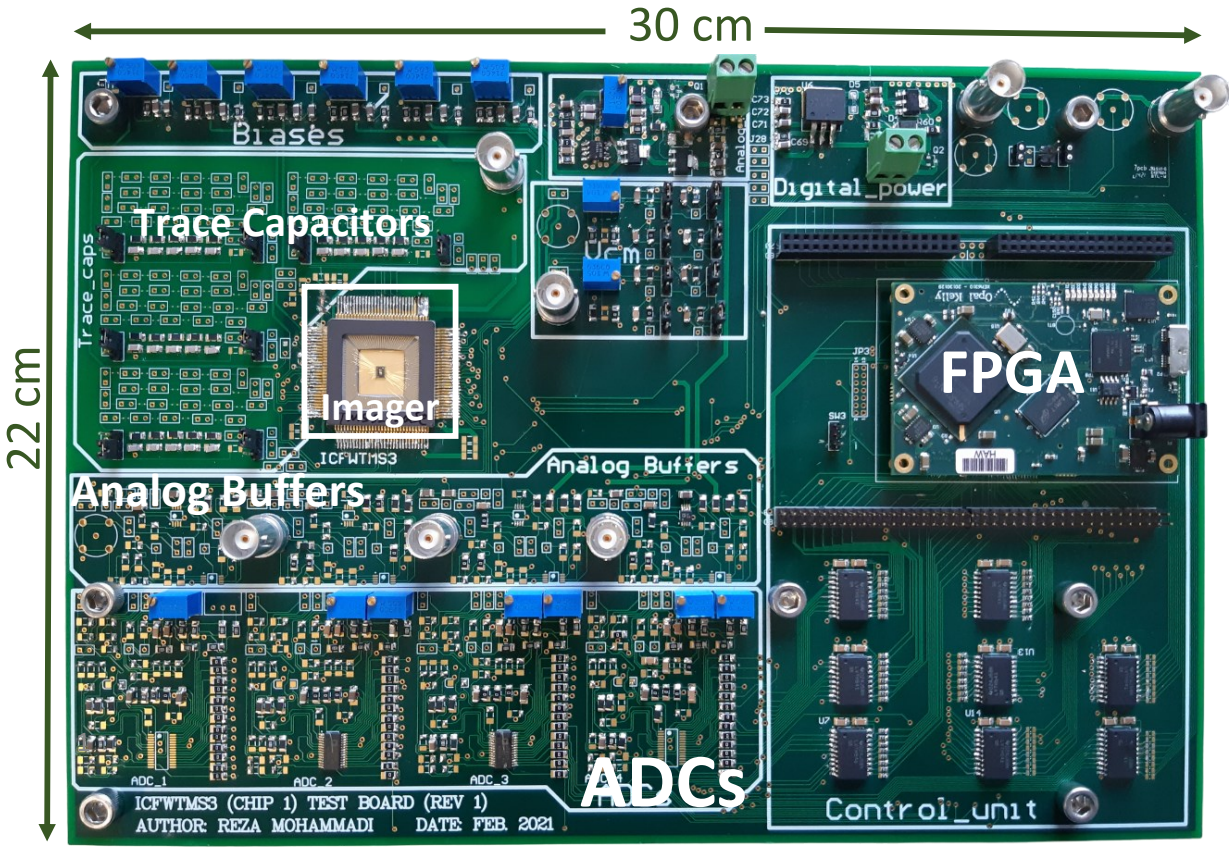



Figure 5.15: Four-layer PCB designed for Chip 2 electronic characterization and photon-counting experiments.

### 5.7.2 Electronic Characterization Results

We now present electronic characterization results from Chip 2. Figure 5.16 shows the measured response of one of the pixel CSAs configured in unity feedback with a 3.3-MHz sinusoidal input. Since the measured output amplitude is around 0.707× the input, the unity-gain frequency of the CSA is 3.3 MHz.

Figure 5.17 shows the step response of the CSA to a rectangular input pulse train with 50% duty cycle. The measured slew rate of the CSA is 2.5 V/$\mu$s with our estimated 200 fF capacitance at the CSA output.

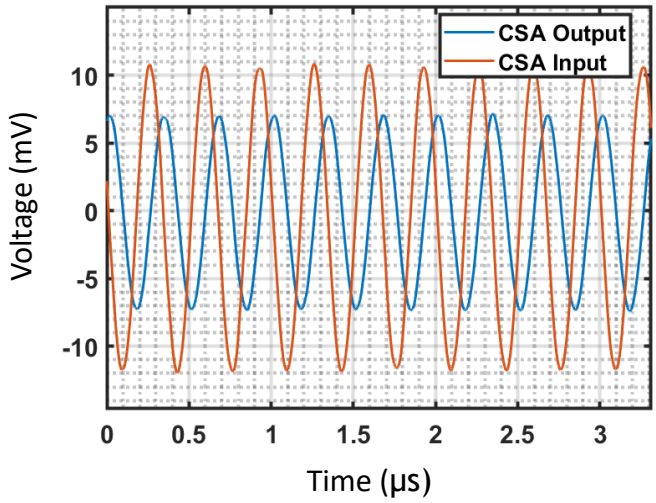



Figure 5.16: Sinusoidal steady-state response of the CSA in unity feedback.

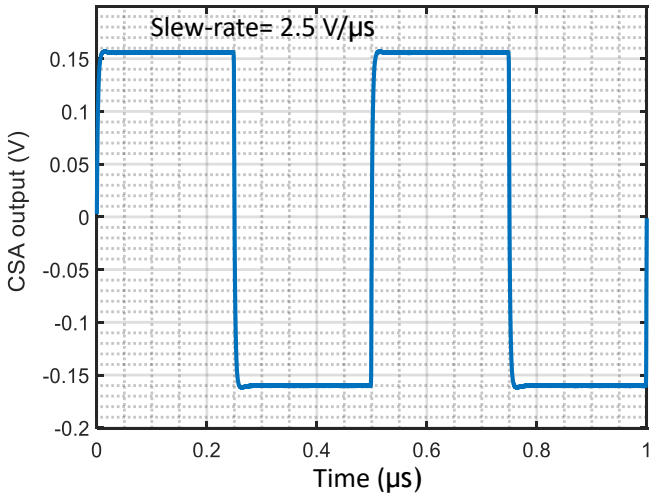



Figure 5.17: Measured CSA step response.

The measured output noise power spectral density (PSD) of the CSA, biased in unity feedback, with an applied 1-MHz sinusoidal input, is shown in Figure 5.18. The rms noise over the entire bandwidth shown is 27 $\mu$V, which is 10$\times$ less than the DBCT requirement.

The measured noise PSD in dark conditions, when a-Se is biased at an 8-V/$\mu$m electric field, is shown in Figure 5.19. This presents the total output noise of the pixel, including

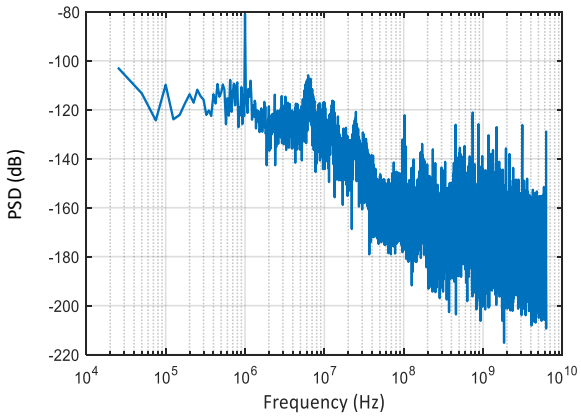



Figure 5.18: Noise PSD of the CSA output with an unbiased a-Se sensor.

its electronic noise and a-Se dark-current noise. The measured rms noise over the entire bandwidth shown is 301 $\mu$V, well below the specified limit of $\sim$ 700 $\mu$V from the application. This shows that the dark-current noise from the a-Se sensor dominates the pixel noise, as intended. With a 10-fF $C_f$, this translates to 15 $e^-_{rms}$ at the input to the pixel.

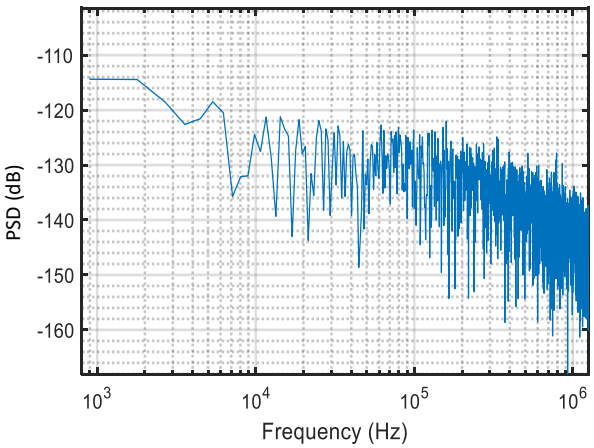



Figure 5.19: Output noise PSD of the CSA with a high-voltage-biased a-Se sensor in dark conditions.

Finally, Table 5.1 summarizes the pixel performance by comparing our simulated and measured results under the same conditions.

Table 5.1: Simulated and measured CSA electronic performance.

| Parameter | Simulated | Measured |
|---|---|---|
| GBW (MHz) | 4.5 | 3.33 |
| Output swing (mV) | 300 | 280 |
| Slew rate (V/µs) | 3.5 | 2.5 |
| Input-referred noise ($e_{rms}$) | 9 | 15 |

### 5.7.3 First Experimental Demonstration of SPE using an a-Se/CMOS X-ray Imager

Figure 5.20 shows the experimental setup we use to measure the energy and temporal resolution of our a-Se/CMOS sensor. Our photon source is a monoenergetic 60-keV $^{241}$Am gamma source with 10-$\mu$Ci (3.7 $\times 10^{10}$-photons/s) activity. As shown in Figure 5.20(b) and (c), we place the gamma source in a small chamber 5 mm above the a-Se/CMOS chip surface.

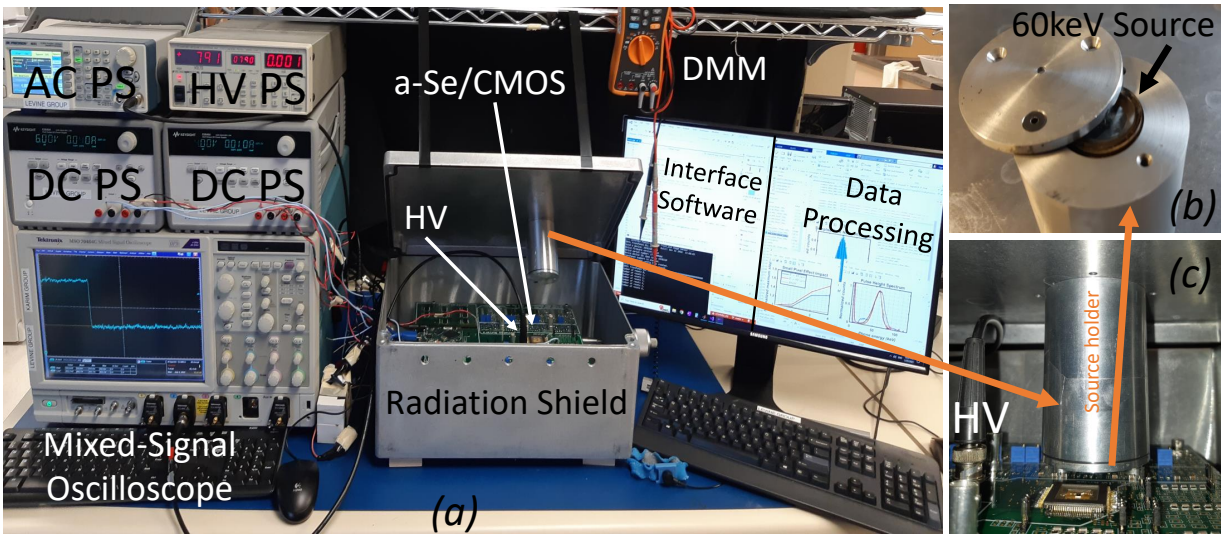



Figure 5.20: Our experimental setup for performing photon-counting measurements.

We first measure the transient response of our detector when operated with $L/d \ll 1$ so that SPE is not expected to impact the response. Figure 5.21(a) shows $V_{CSA}$ from a pixel with $d = 300$ $\mu$m, where $L/d = 0.4$, and with an 8-V/$\mu$m applied electric field $E_{HV}$. In this response, the fast hole-dominated segment is clearly observable, as is the slow electron-

dominated segment, which exhibits a 40-$\mu$s fall time. This is the first demonstration of the transient single X-ray photon response from a monolithic a-Se/CMOS pixel.

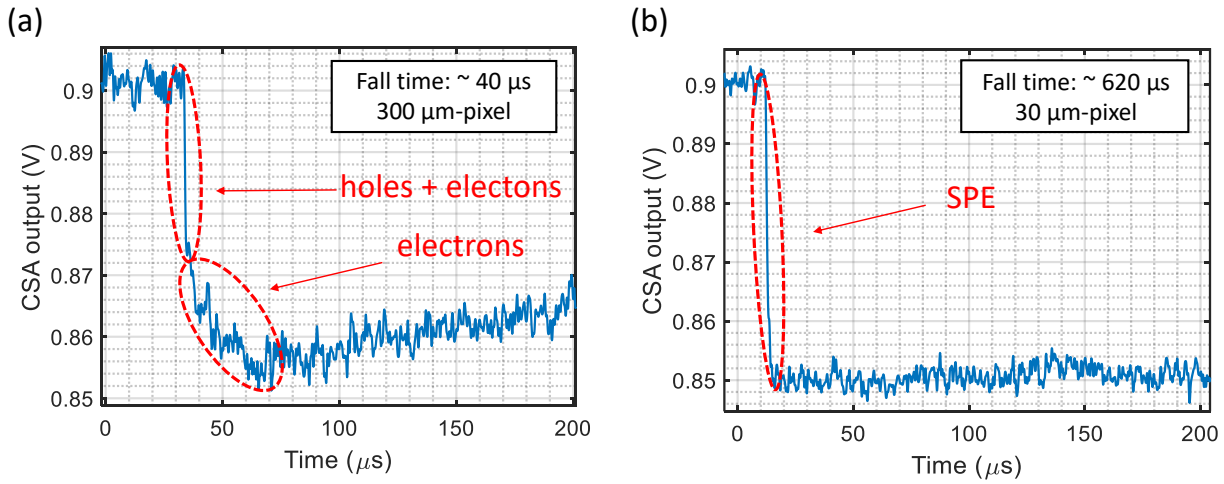



Figure 5.21: (a) Measured transient response of a single-X-ray-photon from our a-Se/CMOS pixel without SPE enhancement. (b) Transient response of an a-Se/CMOS pixel with SPE enhancement.

To demonstrate improved temporal response from SPE, we observe the fall time $t_f$ of $V_{CSA}$ from a pixel in Array 1, where the pixel pitch is 30 $\mu$m. Figure 5.21(b) demonstrates that the observed transient response is not affected by slow electron transport, where $t_f$ is measured at 620 ns with $E_{HV} = 8$ V/$\mu$m This is more than a 70$\times$ improvement in temporal resolution compared to the response without SPE. This result is also the first demonstration of SPE using a monolithic a-Se/CMOS X-ray detector.

We also measure the impact of SPE on settling time. Figure 5.22 displays the normalized slope of $t_f$ for different pixel sizes, with $E_{HV} = 4$ V/$\mu$m and 8 V/$\mu$m, as well as the normalized CSA slew rate by applying a large input current pulse directly to the pixel electrode. Our slew-rate measurement confirms that the transient response improvement for smaller pixels is not attributed to smaller capacitive parasitics associated with these pixels. Rather, these results demonstrate a trend of improving temporal response with decreasing pixel size for a given a-Se sensor thickness, consistent with our modeling. Settling-time improvements also become even greater with higher $E_{HV}$.

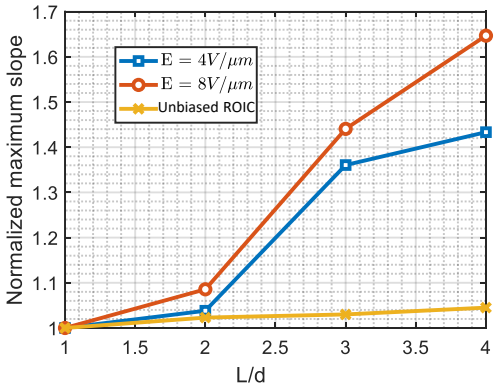



Figure 5.22: Normalized X-ray response maximum slope versus pixel size demonstrating the total measured impact of SPE on temporal response.

We demonstrate the impact of SPE on the energy resolution of our detector by measuring PHS from pixels with $L/d > 1$. Figure 5.23(a) shows the normalized PHS, where the peak at 60-keV energy is normalized to one, obtained by monitoring the CSA output from approximately 2,000 recorded photon hits, for four pixels located at the center of Arrays 1-4, with $E_{HV} = 4$ V/$\mu$m. Figure 5.23(b) shows PHS measurements for the same pixels, but with $E_{HV} = 8$ V/$\mu$m. These results are also the first demonstration of PHS with an a-Se sensor monolithically integrated on a CMOS ROIC.

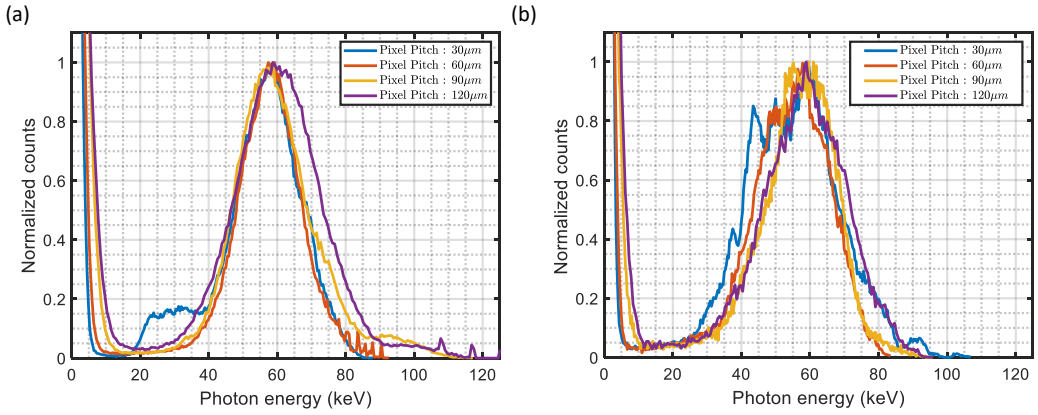



Figure 5.23: Measured PHS results from a monolithic a-Se/CMOS X-ray detector, showing the total impact of SPE on energy resolution. (a) Measured PHS for different pixel dimensions with a 4-V/$\mu$m bias, and (b) with an 8-V/$\mu$m bias.

FWHM energy resolution from the Gaussian-fitted curve is shown in Figure 5.24(a) for different pixels under two different applied electric fields. We achieve the lowest FWHM of 13.9 keV from our 57-$\mu$m pixel with $E_{HV} = 4$ V/$\mu$m. In addition, with $E_{HV} = 8$ V/$\mu$m, we observe an FWHM of 16 keV. Furthermore, the observed trend indicates better SPE-enhanced energy resolution with decreasing pixel dimensions, in line with the anticipated impact of smaller pixel sizes from our simulations. Our highest measured energy resolution in FWHM, 13.9-keV, is more than a 2-fold improvement compared to the well-known energy resolution reported for an a-Se X-ray sensor with an FWHM of 33 keV [98].

Our measured results also indicate that SPE leads to an increase in average induced signal amplitude with smaller pixels, which is consistent with our modeling results from Figure 5.6. Figure 5.24(b) demonstrates the average normalized pulse height for pixels with different sizes and with 4-V/$\mu$m and 8-V/$\mu$m bias. This shows that shrinking down the near-field region will help holes to contribute similarly, independent of the absorption depth, and induce a normalized charge of close to 1, consistent with the argument in Figure 5.5. Improved signal amplitude achieved with SPE is an additional advantage, complementing other improvements presented, that enhances the energy resolution by improving SNR through higher signal levels attained.

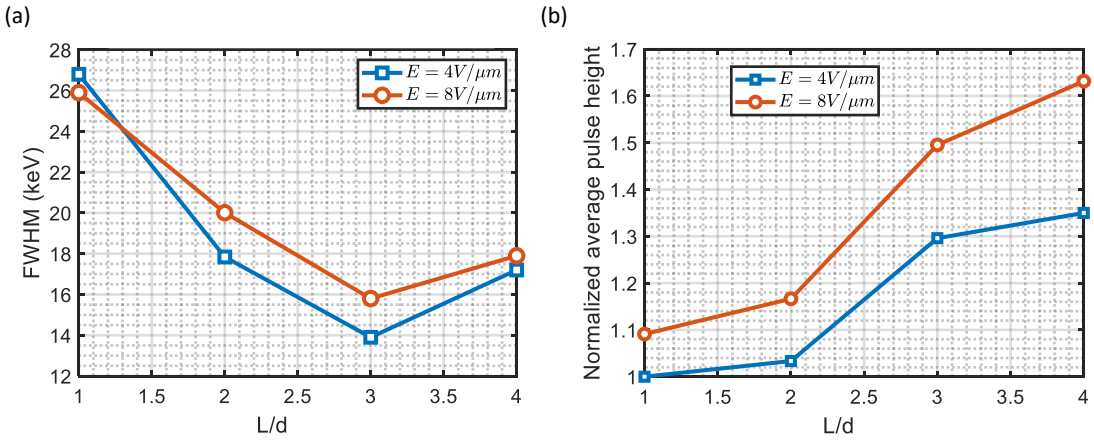



Figure 5.24: (a) Measure SPE impact on energy resolution. (b) Measured SPE impact on pulse height.

### 5.7.4 Potential Impact of Charge-Sharing

Despite the trend of improved performance by employing smaller pixel dimensions, charge sharing between neighboring pixels ultimately limits the benefits from SPE. Our findings indicate that the trend of achieving better energy resolution by reducing pixel size persists up to our second largest pixel. This holds true for both applied electric fields in Figure 5.23(a) and (b). In both cases, we observe that the energy resolution for a 60 $\mu$m-pitch pixel is slightly better than that of 30 $\mu$m-pitch pixel. This stands in contrast to the anticipated outcome of SPE, which suggests that smaller pixels would result in enhanced energy resolution. Because of the reduction in pixel size, it is more likely that a fraction of the charge is appearing at adjacent pixels due to lateral charge diffusion while the charges are drifting vertically. Consequently, while SPE strives to enhance energy resolution through smaller pixels, charge diffusion poses a counteractive impact.

Evidence highlighting the impact of charge sharing is the improved energy resolution observed in our results, achieved through a lower $E_{HV}$. The results shown in Figure 5.23(a) and (b) with $E_{HV}$ of 4 V/$\mu$m and 8 V/$\mu$m, respectively, illustrate that each pixel exhibits improved energy resolution with lower $E_{HV}$. To clarify, higher $E_{HV}$ leads to lower ionization energy, resulting in larger charge clouds for a given photon energy [101]. This increase in charge cloud size subsequently enhances the likelihood of charge sharing between neighboring pixels, aligned with our observed results.

The presence of Compton scattering between adjacent pixels also supports the theory that charge sharing is responsible for the slight energy resolution degradation observed in our smallest pixel. Compton scattering involves low-energy photons emitted in different directions generated after high-energy photon absorption. Notably, discernible small peaks in the spectra can be seen in Figure 5.23(a) and (b), particularly within the energy range of 20-keV to 40-keV for the 30-$\mu$m-pitch pixel. This empirical observation supports the idea that the degradation in SPE improvement, resulting in reduced energy resolution, can be ascribed to charge sharing caused by Compton scattering originating from neighboring pixels.

We also emphasize that while the energy resolution is degrated by charge sharing, this decline is not substantial compared to improvement gained from SPE. Furthermore, the impact of charge sharing on decreasing energy resolution becomes even less significant when working with lower photon energies, particularly in breast imaging, where photon energies below 45 keV are commonly utilized. However, we anticipate that charge sharing will have a more noticeable impact compared to the improvement from SPE for pixels with dimensions well below 30 $\mu$m when reaching the reported 16-$\mu$m spatial resolution [97].

### 5.7.5 Performance Benefits of SPE

Furthermore, it is crucial to emphasize that substantial benefits from SPE are achieved using a thermally evaporated a-Se sensor on a CMOS ROIC. Additional improvements in performance can be made by incorporating supplementary techniques, including the integration of extra layers like hole-blocking layers or the utilization of Frisch grids, among others. However, we note that integrating these methods with CMOS fabrication technology may present certain challenges [95] [105] [106]. Nonetheless, the essence of our work lies in our ability to maintain a streamlined, cost-effective, and high-yield process while delivering significantly improved results.

Finally, our measured results suggest that a monolithic a-Se/CMOS X-ray detector exploiting SPE could meet the stringent requirements for demanding bio-imaging applications like DBCT. A DBCT system employing an SPC detector would allow for simultaneous imaging of hard and soft tissues, reducing patient exposure to X-rays by avoiding multiple exposures and increasing reliability with 3-D imaging [107] [108]. DBCT requires energy discrimination between 20 keV and 40 keV, sub-100-$\mu$m spatial resolution, and a maximum flux-handling capability of 2-10 $\times 10^7$ photons/mm$^2$. Amorphous selenium's status as an affordable gold-standard sensor for mammography in flat-panel detectors makes meeting the DBCT requirements via SPE enhancement a potentially game-changing development [35] [49]. Given the high spatial resolution of a-Se, measured down to 16 $\mu$m, meeting the 100-$\mu$m spatial resolution requirement for DBCT is not a challenge [97]. To discriminate photons with 20-keV and 40-keV energies with $3\sigma$ separation, the uncertainty from all noise sources, including electronic noise and shot noise from a-Se, should not exceed FWHM of 15.5 keV$_{rms}$. Since our measured uncertainty is 13.9 keV$_{rms}$, which translates to a 10% error rate, a significant improvement compared to a 50% error for a conventional detector (FWHM= 33 keV) [98]. Assuming our SPC ROIC can reset with the same settling time as the photon-induced signal fall time, leveraging SPE could yield a count rate up to 400 Mph/s.mm$^2$ with an energy resolution FWHM of 13.9 keV, and a 60-$\mu$m pixel pitch, meets the DBCT requirements.

As a proof of concept, we have successfully demonstrated the first scalable monolithic a-Se/CMOS SPC detector, which effectively leverages the benefits of SPE [109]. This achievement is enabled by using a new pixel design with four subpixels, although the circuit details are beyond the focus of this chapter. However, our presented pixel is the first to meet DBCT requirements with an amorphous semiconductor, showcasing the early-stage utility of our work.

## 5.8 Summary

We have demonstrated, for the first time, that SPE can significantly enhance the temporal and energy resolution of an a-Se X-ray sensor through its monolithic integration with CMOS. Furthermore, using device-level statistical simulation, we have highlighted the intensified impact of SPE when there is a large difference between slow and fast carrier mobilities, as for a-Se. To emphasize the total impact of SPE, we designed and fabricated a CMOS ROIC, containing arrays of pixels with various dimensions, ranging from 30-300 $\mu$m. Our measured conventional and SPE-enhanced transient response measurements of a-Se integrated with a CMOS ROIC, both for the first time, show 70$\times$ improvement in SPE-enhanced settling time, measured down to 620 ns, compared to a conventional detector settling time of 40 $\mu$s. In addition, our results include the first PHS measurements from a monolithic a-Se/CMOS X-ray and report an energy resolution of 6.42 keV, more than a 2$\times$ improvement. The 60-$\mu$m-pitch pixel measured 13.9-keV FWHM energy resolution and 1.2-$\mu$s temporal resolution underscores the overlooked potential of monolithic a-Se/CMOS technology for large-area DBCT application, particularly given the established excellence of a-Se as the gold standard for mammography in flat panel detectors. More importantly, monolithic integration of an a-Se sensor with CMOS ROIC would not entail any additional fabrication complexity for these benefits.

# Chapter 6

# SPE-Enhanced Monolithic A-Se/CMOS Single-Photon-Counting X-Ray Imager (Chip 3)

## 6.1 Introduction

Fundamental challenges exist in designing a scalable a-Se/CMOS SPC pixel ROIC for the development of large-area image sensors for SPC DBCT. Addressing these obstacles is key to fully exploiting the promising potential we have demonstrated via (1) photon counting with a-Se monolithically integrated on CMOS, and (2) enhancement in a-Se temporal and energy resolution realized through SPE.

In Chapter 4, we presented, for the first time, the capability of a-Se monolithically integrated on CMOS to count single photons. Additionally, in Chapter 5, also for the first time, we demonstrated that the intrinsic performance issues of a-Se can be mitigated by leveraging SPE, leading to approximately 2× enhancement in energy resolution and up to 70× in temporal response.

However, designing a pixel capable of energy-discriminating single-photon counting, benefiting from SPE enhancement, and offering large-area scalability at the same time demands careful considerations and poses a significant area challenge. Based on our results from Chip 2 in Chapter 5, to enhance energy and temporal resolution through SPE, a pixel dimension $d < 45$ $\mu$m is needed for a typical $t_{sen}$ of 115 $\mu$m. Nonetheless, integrating typical pixel electronics, including charge-sensitive amplifiers, energy-thresholding comparators,

and counters, as well as calibration circuits, poses a significant challenge at this scale. For DBCT, with our targeted 20-s scan duration, 2000 projections per scan, 10 frames per projection at a 1-ms frame interval, and pixel count rate of 20 Mcps/mm$^2$, we will aim for at 200 photons/frame. To ensure proper counting, allocating at least 8 bits is essential, accommodating up to 256 photons/frame. This provides a safety margin, whereas a 7-bit counter would be insufficient.

This chapter introduces Chip 3, from which we present the experimental demonstration of the first dual-energy-discriminating SPC pixel. Our pixel integrates a-Se as the X-ray sensor with a novel CMOS ROIC. The proposed pixel features a large-area-scalable design, with a pixel area of $92 \times 92$ $\mu$m$^2$. Our design exploits SPE in an amorphous semiconductor for X-ray SPC for the first time. By exploiting SPE, our pixel achieves an energy resolution of 7.9 keV while handling 35-Mcps/mm$^2$ flux with an a-Se sensor, which is traditionally perceived as a slow and low-energy-resolution X-ray-sensitive material. Our design achieves this performance using (1) a novel area-efficient sub-pixel-SPE enhancement architecture, and (2) a partially-shared foreground input-offset-correction circuit employing (3) a new area-efficient current-steering calibration DAC.

## 6.2 Chip Design

In this section, we present the design of our proposed pixel circuits and their physical implementation on Chip 3. First, we present our proposed circuit architectures for SPE enhancement. This is followed by an explanation of the complete pixel design and the implementation of its associated sub-blocks. Lastly, we present the array design, along with the physical implementation of the pixel.

### 6.2.1 Proposed Sub-Pixel SPE-Enhanced Architecture

We now introduce the concept of sub-pixel SPE enhancement as an effective solution to significantly mitigate the area/performance trade-off in meeting DBCT requirements. As outlined in Chapter 3, the pixel dimension required to meet the spatial resolution requirements for DBCT differs from the dimension needed to achieve energy and temporal resolution requirements. DBCT spatial resolution necessitates a pixel dimension less than 100 $\mu$m, while our findings from the previous chapter indicate a need for a pixel dimension around 45 $\mu$m to meet the energy and temporal resolution specifications for DBCT. As a

result, we need to restrict our maximum pixel dimension to 45 $\mu$m to satisfy both requirements. However, implementing an SPC pixel at this dimension without compromising its performance poses a significant area-related challenge.

We present a novel approach to making these two requirements independent by decoupling the dimension needed for SPE enhancement from the overall pixel dimension required to meet the spatial resolution set by DBCT. We propose the concept of sub-pixel SPE enhancement to attain this objective. In particular, we suggest incorporating sub-pixels with independent analog front-ends that meet the dimension required for SPE enhancement. These sub-pixels share a digital backend and other circuit blocks, such as offset-calibration, with the main pixel that handles the photon-counting task. Through sharing area-intensive components, such as counters and DACs, we can avoid reducing the size of the main pixel while still harnessing the advantages of SPE. Our sub-pixel SPE enhancement approach is adaptable to a variety of other digital pixels. Various factors, such as the demands of the application, thickness of the X-ray-sensitive material, pixel functionality, and CMOS technology node, will shape the decisions on the number of sub-pixels and the selection of shared blocks. Figure 6.1 provides a 3-D cross-sectional view of our proposed single pixel with its sub-pixels.

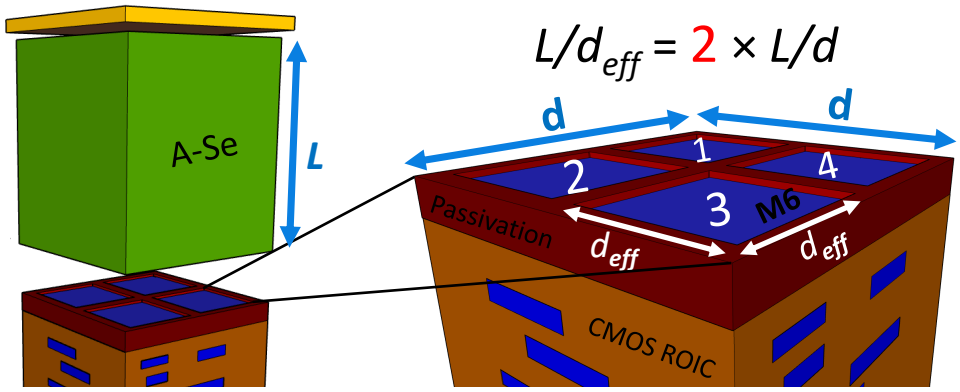



Figure 6.1: 3D cross-section of a sub-pixel SPE-enhanced monolithic a-Se/CMOS SPC single pixel with four sub-pixels.

To satisfy our specifications, we subdivide the pixel into four equal-sized square sub-pixels. Each sub-pixel has a dimension $d_{eff} \approx d/2$, facilitating the required dimensions for SPE enhancement. As shown in Figure 6.1, our pixel dimension is d=92 $\mu$m, and the whole pixel is covered by a-Se. It comprises four sub-pixels, each with $d_{eff}$= 45 $\mu$m. Each pixel incorporates four openings in the top metal layer, serving as the sensing electrode for the respective sub-pixel. Note that there is around 1-$\mu$m spacing between sub-pixels, and

that is why $d_{eff}$ is not equal to $d/2$ exactly.

Each sub-pixel features its own CSA and comparators while sharing a digital back-end, as depicted in Figure 6.2, and a partially-shared calibration circuit. To ensure each sub-pixel operates independently, the output from each comparator triggers an edge-detector circuit. This circuit, upon the comparator's rising edge, generates a short pulse, subsequently multiplexed to drive the clock signal of the asynchronous counters.

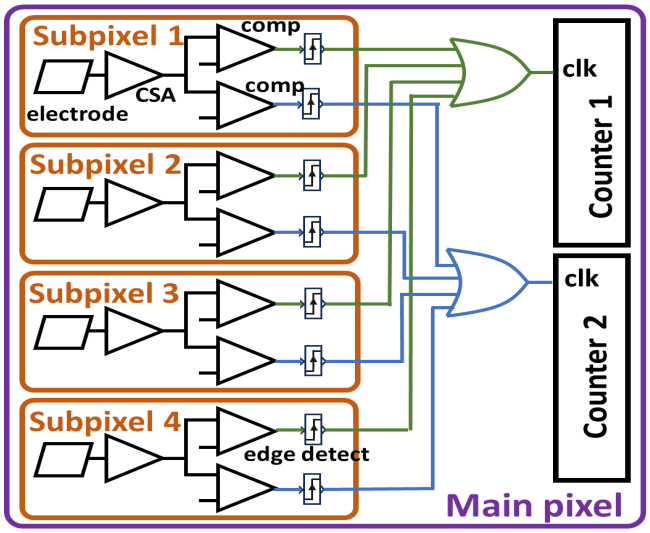



Figure 6.2: SPC pixel with four SPE-enhanced sub-pixels and shared digital back-end.

Therefore, implementing sub-pixel SPE enhancement increases the SPE-factor. We define the SPE-factor as the ratio between the sensor thickness and the SPE-effective dimension (sub-pixel dimension), represented as $t_{sen}/d_{eff}$. An increased SPE-factor signifies better performances as it provides enhanced energy and temporal resolution in each sub-pixel due to the use of SPE. However, pixel spatial resolution is still determined by $d$, allowing space for the required additional circuits.

Furthermore, our design using sub-pixel SPE enhancement leads to another factor in boosting the temporal resolution of the main pixel. Concurrently, the count rate of the main pixel is improved by the number of sub-pixels. To clarify, for a given pixel dimension, sensor response time, and front-end ROIC, a pixel integrated with four sub-pixels can accommodate a photon flux four times greater than a pixel that does not include sub-pixels.

To sum up, based on the findings detailed in Chapter 5 and by utilizing the proposed

sub-pixel-SPE-enhanced architecture, in conjunction with our application requirements, our objective is to leverage the capabilities of SPE to meet the demanding 20-Mcps/mm$^2$ DBCT requirement. We plan to design with $t_{sen}/d_{eff}$= 2.5 to aim for a targeted energy resolution of 7 keV and a rise time of 3 $\mu$s (ensuring the photon-processing time remains under 25 $\mu$s). Each pixel will possess two energy bits, necessitating two 8-bit counters.

### 6.2.2 Complete Pixel Architecture

Figure 6.3 shows the complete architecture of our designed pixel, which integrates our proposed circuits for implementing SPE enhancement and meeting the DBCT specifications. The pixel incorporates the four sub-pixels and includes a partially-shared input-offset foreground-calibration circuit for SPC pixels to correct random offset, one cause of energy-resolution degradation. The proposed foreground-calibration circuit automatically and simultaneously corrects the offset of all sub-pixel comparators by adjusting a dc bias current in the comparator. Moreover, we have proposed a dedicated 8-bit piece-wise linear current-steering DAC, with details to follow in section 6.2.4, to sweep the comparator current. In addition, all four sub-pixels utilize the two embedded counters during calibration mode, resulting in a reduced calibration DAC area for each sub-pixel, as detailed in section 6.2.3.

The pixel operates in two distinct modes: (1) calibration mode and (2) photon-counting mode. During calibration mode, all four sub-pixels share the two integrated counters, optimizing the calibration DAC area for each sub-pixel. In photon-counting mode, the counter's input is directly connected to the comparator's output via an edge-detection circuit. This circuit generates an asynchronous pulse lasting 250 ns, which then triggers the corresponding counter upon the arrival of a photon. Such a configuration facilitates independent sub-pixel operation, given that the counters solely interact with the multiplexed output from the edge detector of the sub-pixels. Additionally, $C_f$ is soft resetting using parallel MOSFET transistor $M_f$, which functions as a resistor when biased in the triode region. A pulse generator, controlled by the comparator's output, asynchronously triggers $M_f$ to discharge $C_f$ after detecting a photon. The following sections provide comprehensive details of each proposed circuit's operation separately and their integration with the main pixel.

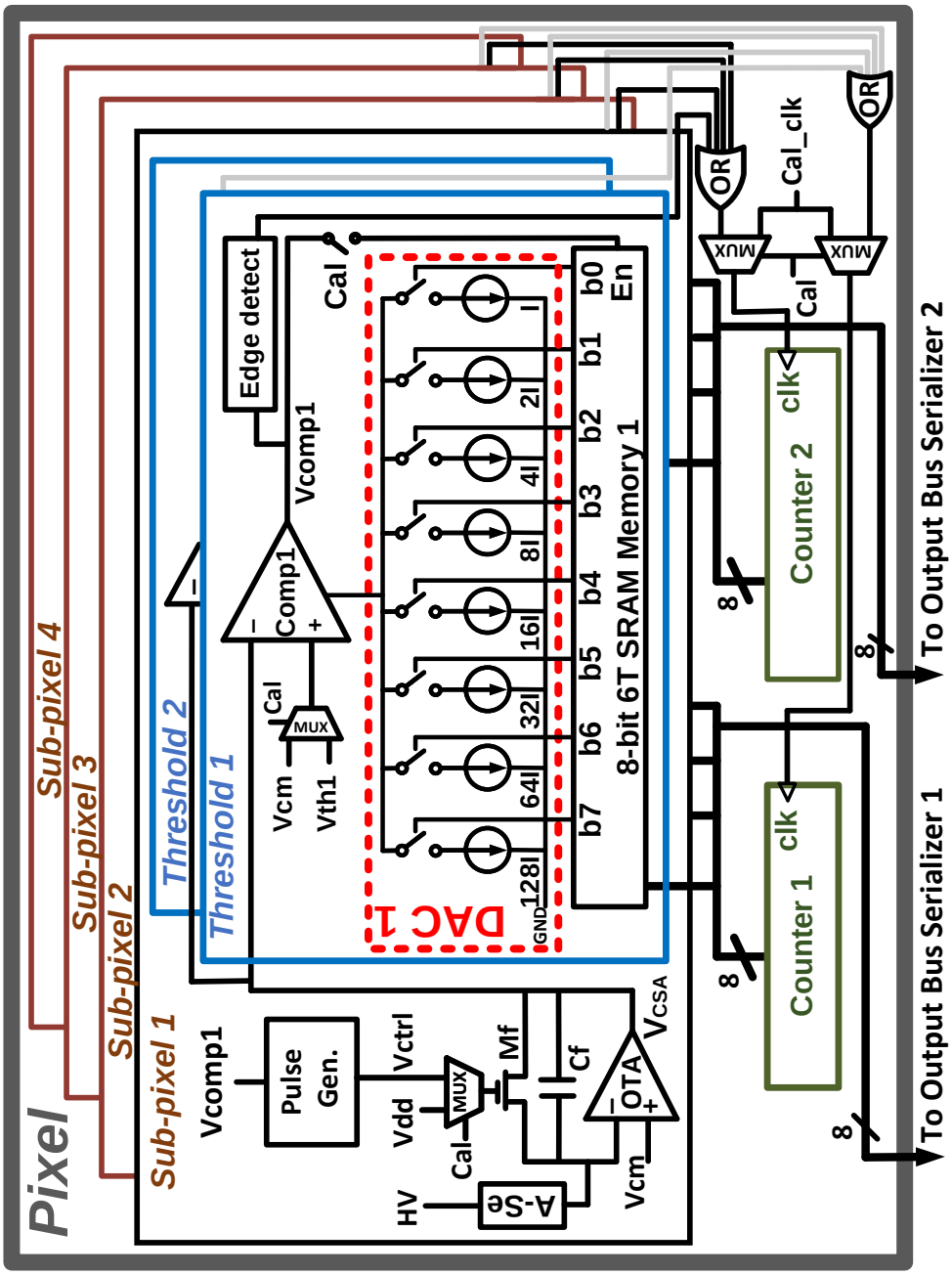



Figure 6.3: Complete SPE-enhanced SPC pixel implementation.

### 6.2.3 Foreground Input-Offset Calibration Circuit

Our proposed offset correction mechanism combines reconfigurable resolution with an area-efficient design. Figure 6.4(a) shows a simplified SPC pixel with one comparator, one counter (CNTR), and an offset-calibration circuit. The offset-calibration circuit comprises three major components: a current-steering DAC, a digital logic circuit to implement the DAC search algorithm, and memory to store the input required to correct the offset. We employ the SPC pixel counter to carry out a linear search within the offset-calibration circuit, as illustrated in Figure 6.4(b).

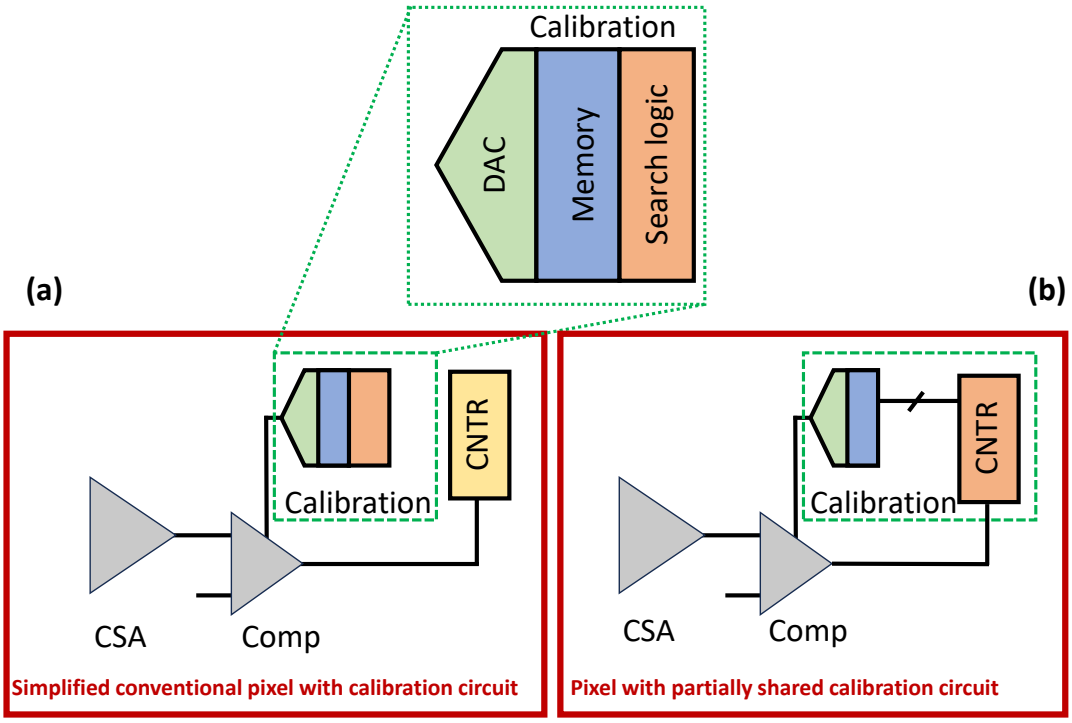



Figure 6.4: SPC pixel with foreground-calibration circuit. (a) Conventional calibration circuit. (b) Proposed dedicated partially-shared calibration circuit.

A simplified proposed SPC pixel in calibration mode and photon-counting mode is shown in Figure 6.5(a) and (b), respectively. The pixel first enters calibration mode, at which the counter functions as the digital-search logic circuit. The integrated memory array incorporates an 8-bit static random access memory (SRAM), and the DAC is realized using a current-steering topology. In calibration mode, the CSA operates with unity feedback, ensuring both comparator inputs maintain the common-mode voltage, shown as ground in Figure 6.5(a). The comparators require a large systematic dc input offset voltage, ensuring the output starts at logic '1' at the beginning of the correction cycle. This ensures the corresponding SRAM's write enable En is initially active, allowing for subsequent storage of the DAC code. An external clock is multiplexed as the counter input clock in this mode when the Cal signal is logic '1'. The counter increments the DAC digital input, and the comparator output $Vcomp$ toggles once $V_{os}$ is compensated. The DAC code is then saved in the SRAM and applied during photon-counting operation. The counter continues to increment up to 256 cycles, at which time the Cal signal becomes '0', marking the end of the calibration cycle.

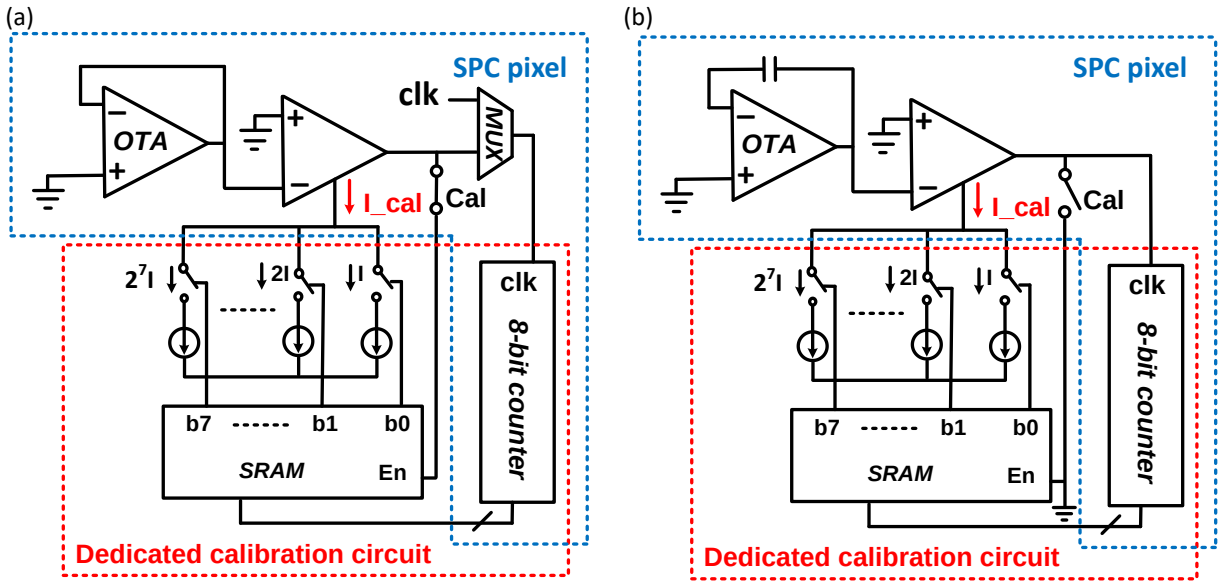



Figure 6.5: SPC pixel with proposed foreground-calibration circuit operating in (a) calibration mode, and (b) photon-counting mode.

Figure 6.6 illustrates the proposed calibration operation, highlighting the DAC current transfer characteristic (TC), comparator output $V_{comp}$ which also acts as the SRAM enable En, applied current during calibration $I_{cal}$, and the input-referred offset $V_{os}$ based on the DAC input code.

After calibration, the pixel enters photon-counting mode. In this mode, the counter is used exclusively for counting the number of absorbed photons. Its input connects to the comparator output through an edge-detection circuit. As a result, the counter is clocked upon detecting a photon, facilitating the normal operation of the photon-counting pixel. The SRAM enable is set to '0', preserving the stored data.

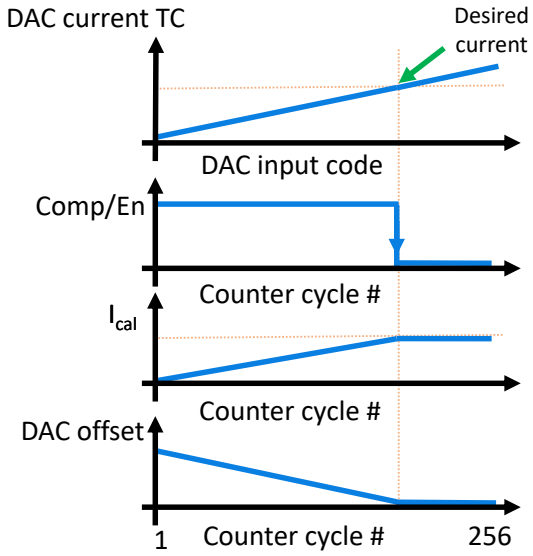



Figure 6.6: Proposed foreground-calibration circuit operation.

Integrating the proposed foreground-calibration with our sub-pixel SPE-enhanced SPC pixel leads to further improved area efficiency. As shown in Figure 6.7(a), the pixel encompasses two energy bins, four sub-pixels, two counters, and a calibration circuit for each comparator. By embedding our calibration circuit into the main pixel and sharing each of the two counters among the four calibration circuits, illustrated in Figure 6.7(b), we eliminate the necessity for logic circuits in all eight calibration circuits during the search algorithm execution. To maintain simplicity, the figure omits detailed connections and block specifics. As per our naming convention, 'calibration 1-1' denotes sub-pixel one, and comparator one, respectively. The detailed implementation is provided in Figure 6.3.

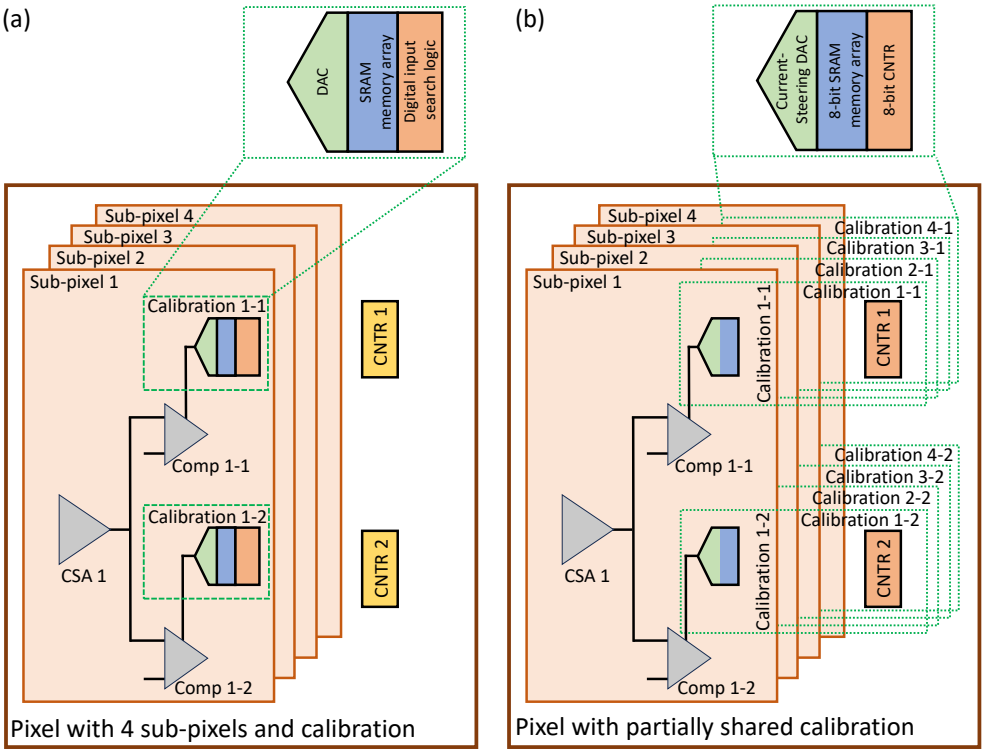



Figure 6.7: Proposed sub-pixel SPE-enhanced pixel with four sub-pixels with (a) a dedicated calibration circuit per comparator, and (b) a partially-shared calibration circuit.

### 6.2.4 Piecewise-Linear Current-Steering DAC

To meet the area requirements for sub-pixel SPE enhancement, we need an area-efficient calibration DAC implementation. At least 7-bit resolution is required to ensure the comparator offset is not a dominant factor in limiting the pixel energy resolution. Assuming 50-mV maximum i $V_{os}$ for the comparator, 7-bit resolution translates to $V_{os}$ of 400 $\mu$V, which is 5$\times$ less than the limit set by the energy resolution limit of 6.6 keV or 2.1 mV [110]. However, we aim to design the DAC for 8-bit resolution to include margin. In a conventional architecture, the current-steering DAC area doubles with each additional bit due to its binary-weighted implementation. Designing an 8-bit conventional current-steering DAC with 255 cells poses a challenge to meeting our pixel area requirements, even if implemented with minimum-feature-size unit-current cells [111].

To address this issue, we propose an area-efficient piece-wise linear current-steering DAC. By using the same-sized devices for most-significant bits (MSBs) b5-b7 as for bits b0-b2, depicted in Figure 6.8, the required number of DAC current cells drops to 38 which is 15% of a conventional DAC. While this method necessitates an additional bias line, it is not a critical area challenge. However, drawing large current with small cells makes the DAC highly sensitive to mismatch because even a small deviation in transistor threshold voltage $V_t$ could cause a significant deviation in the resulting current.

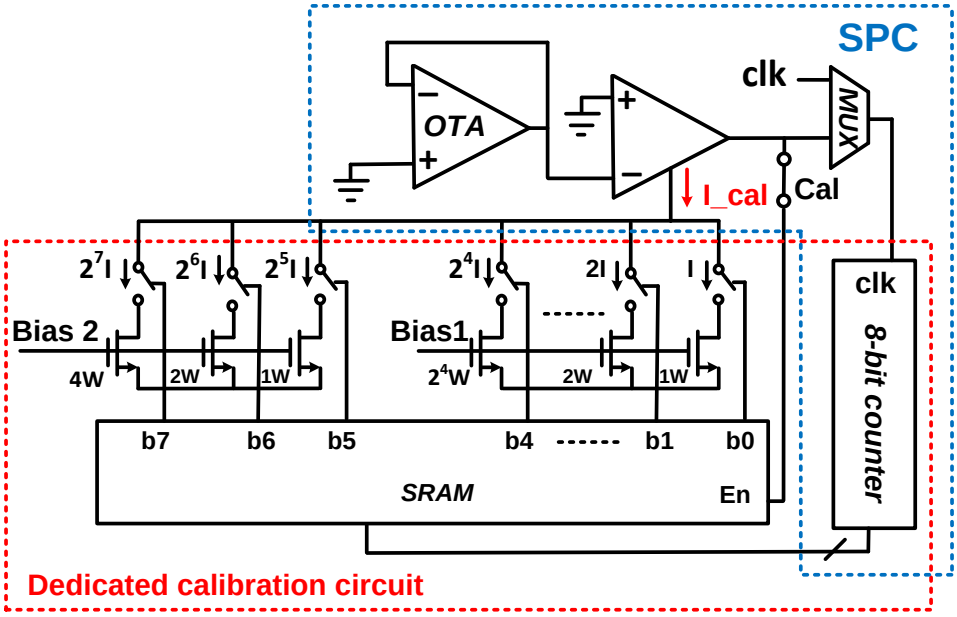



Figure 6.8: Proposed foreground-calibration circuit with a reduced-area current-steering DAC.

We show the impact of mismatch on the calibration algorithm in Figure 6.9. For simplicity, we assume only the MSBs are mismatched. In the figure, the blue line illustrates a scenario without mismatch, while the red line depicts extreme mismatch ($+3\sigma$). If the applied current exceeds that of the ideal DAC due to mismatch when the MSB toggles, then the calibration process will terminate the present cycle. Consequently, the stored offset will have a significant error.

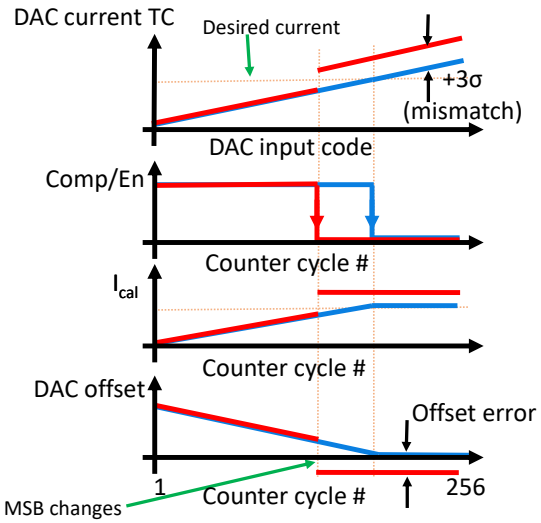



Figure 6.9: Impact of mismatch on the proposed foreground-calibration circuit operation with reduced-area DAC.

Implementing a piecewise linear (PWL) DAC, as depicted in Figure 6.10, significantly mitigates this mismatch impact. We bias b5-b7 current sources to provide DI= 40 nA less than their ideal binary-weighted values. DI is defined as 3× the current resulting from the standard deviation of $V_t$ mismatch. This ensures MSB mismatch does not introduce a large positive ($V_{os}$ to the DAC TC, which would cause significant error.

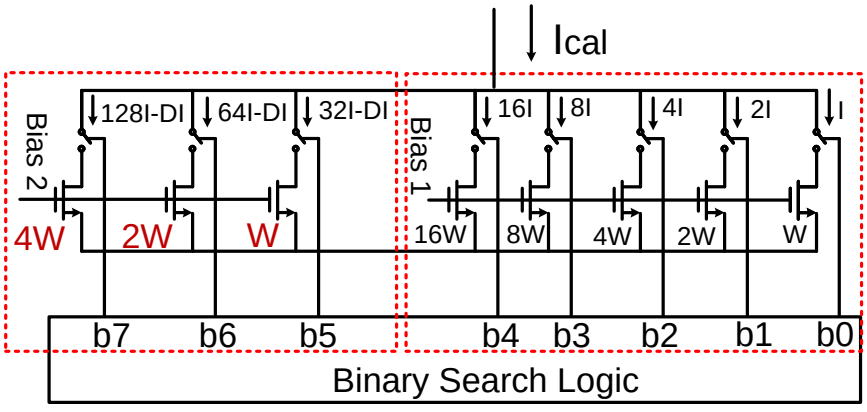



Figure 6.10: Proposed current-steering DAC implementation.

As shown in Figure 6.11, when the applied current becomes less than the expected current when the MSB toggles, the applied current will not terminate the calibration with a large error since the calibration continues until the offset is compensated with the ideal least-significant bit (LSB) resolution. By biasing b5-b7 in this manner, the DAC exhibits a PWL TC. In the figure, the gray line represents the operation of an ideal reduced-area DAC with linear TC, while the blue line represents an ideal reduced-area DAC with PWL biasing. As shown in Figure 6.11, both cases can successfully correct the offset. While the reduced-area PWL biasing decreases dynamic range by about 20% relative to a conventional DAC, our design brings the $V_{os}$ within the LSB limit using less chip area.

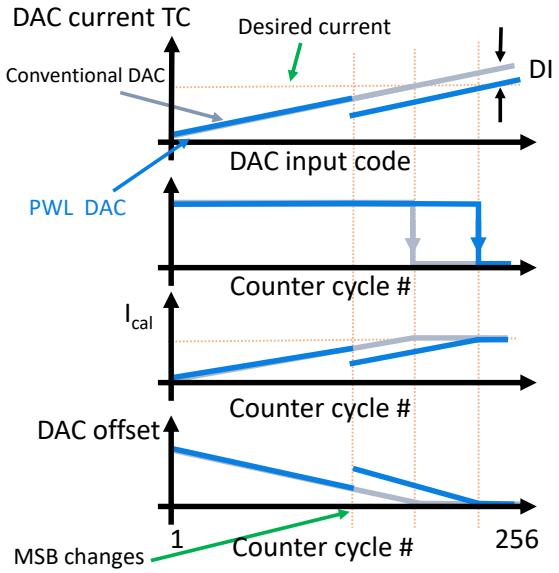



Figure 6.11: Proposed PWL DAC operation with optimized bias.

Figure 6.12 depicts the effect of mismatch on the functionality of our dedicated PWL DAC in the calibration circuit. In this figure, the blue line represents the TC for an ideal PWL DAC without mismatch, while the red line illustrates the case when mismatch is applied only to the MSBs. The TC indicates that the presence of mismatch does not terminate calibration, and correction of $V_{os}$ continues until it is compensated.

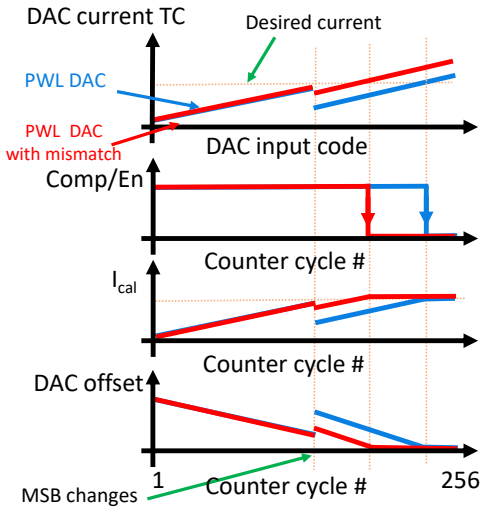



Figure 6.12: Impact of mismatch on the proposed PWL DAC operation with optimized bias.

### 6.2.5 Asynchronous Soft-Reset Scheme

Along with the reduction in signal-current rise time through SPE, a fast pixel reset is imperative to satisfy the stringent temporal resolution demands for DBCT. Conventional resistive discharge of $C_f$ through a large feedback resistor presents a trade-off between conversion gain and speed when choosing the feedback resistor value [64][55]. While hard resetting the capacitor using a switch is a possible solution for resetting the amplifier, it could introduce distortion to the output signal due to charge injection and clock feed-through. To mitigate this, we soft reset the capacitor, whereby the switch is not fully closed during the reset phase. Figure 6.13(a) illustrates two distinct resistances during the integration ($R_d$+$R_f$) and reset phase ($R_d$), governed by the pulse generated by the comparator. The reduced resistance facilitates a faster discharge of the $C_f$ compared to a conventional CSA with feedback resistor, allowing for faster pixel reset in preparation for the next photon. Figure 6.13(b) contrasts the CSA output between the conventional pixel transient response and the SPE-enhanced sensor with soft reset. When a photon is detected, the comparator toggles, and a short pulse, produced by an edge-detection circuit, adjusts the discharge resistance.

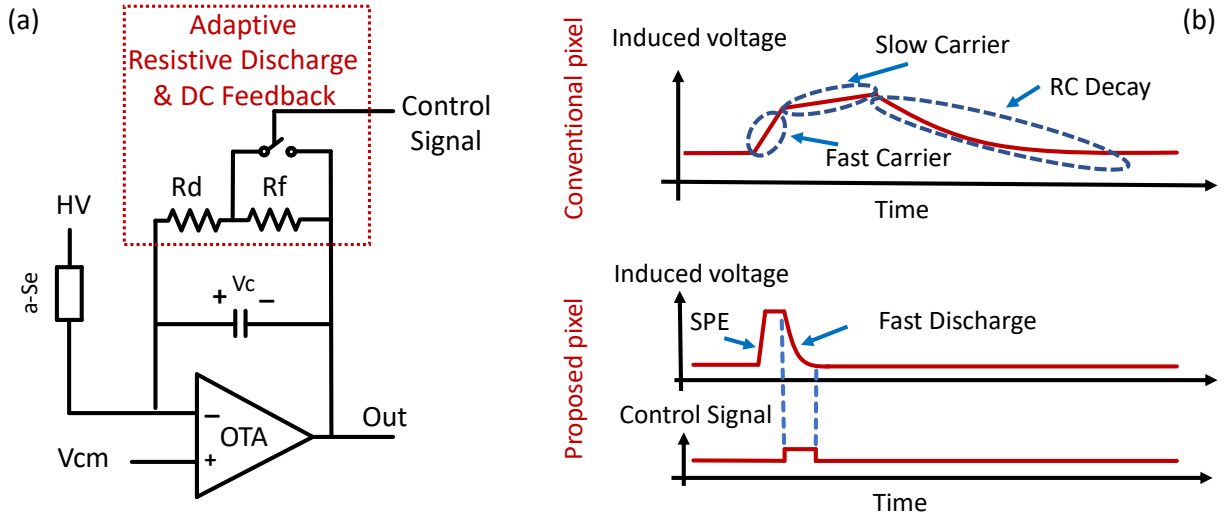



Figure 6.13: SPE-enhanced asynchronous soft reset.

### 6.2.6 CSA and Telescopic OTA

The sub-pixel CSA, built using a telescopic-cascode OTA from Chip 2 with 55-dB dc gain and 3.3-MHz GBW, and 8-fF $C_f$, is wired to a-Se via a distinct exposed 45×45-$\mu$m$^2$ top-metal (M6) pad. Two sub-pixel comparators provide dual-energy-band (30-60 keV and > 60 keV) discrimination, while two 8-bit ripple-carry counters, shared by sub-pixels, count photons in each energy band.

### 6.2.7 Comparator

Two sub-pixel comparators are implemented with an open-loop OTA, shown in Figure 6.14, followed by four inverters for additional gain. Each comparator is designed with a large 30-mV static offset for the proper start-up of the proposed calibration algorithm. The OTA provides 45-dB dc gain and 50-MHz 3-dB bandwidth (BW), and offers a linear adjusting capability of its systematic offset by sweeping $I_{cal}$ with its dedicated current-steering DAC.

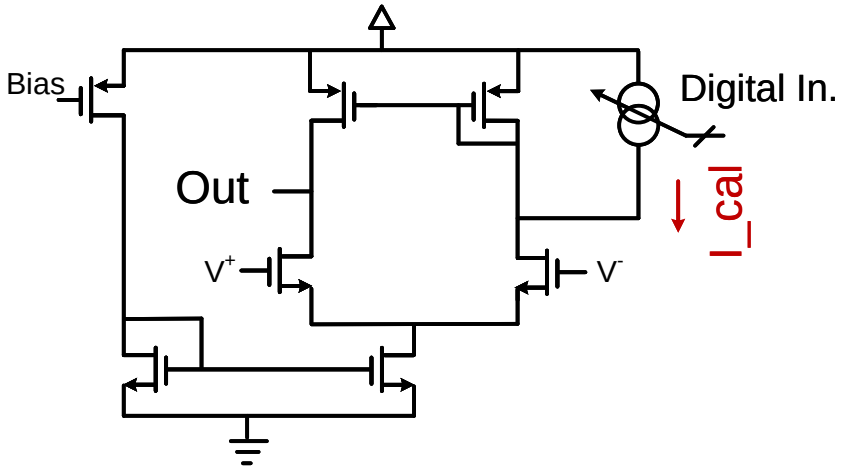



Figure 6.14: Comparator with adjustable offset.

### 6.2.8 8-Bit 6T SRAM

We implemented an 8-bit six-transistor (6T) SRAM to store the corrected offset digital input to the current-steering DAC after calibration. Our single-bit SRAM, shown in Figure 6.15, operates with a 1.8-V supply and occupies an area of 2.5×4 $\mu$m$^2$, with simulated write and read times of 0.9 ns and 1 ns, respectively.

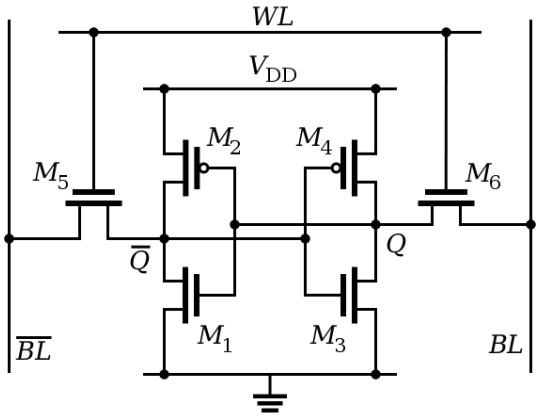



Figure 6.15: Signle-bit 6T SRAM.

### 6.2.9 Ripple-Carry Counter

Due to the asynchronous operation of our photon-counting pixel, we have designed an 8-bit ripple-carry counter, shown in Figure 6.16. The maximum simulated counter speet is 360 Mcounts/s, and it resets itself upon reaching its maximum value. The counter also utilizes an asynchronous reset to reset the counter when the pixel begins operation after calibration and during data transfer from all pixels to the input-output (I/O) shift registers.

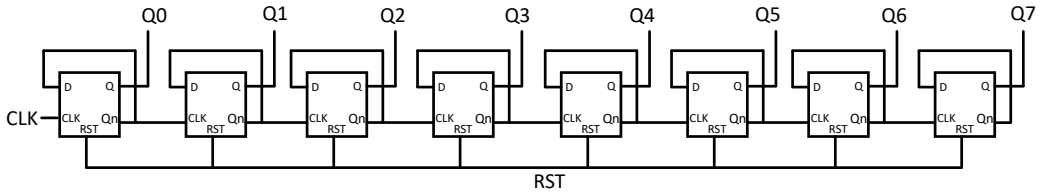



Figure 6.16: 8-bit asynchronous ripple-carry counter.

### 6.2.10 Shift Registers

The output shift register is made up of 136 D flip-flops (DFFs), which are loaded in parallel from a row of pixels. This supports eight pixels in each row, with a pair of 8-bit counters assigned to each pixel, along with four framing bits at the start and four framing bits at the end. The outputs of the corresponding row counters are activated and connected to column buses linked to the input of the output shift register. Figure 6.17 illustrates the shift register with its single element in the chain. The shift registers also operate with an asynchronous reset, RST.

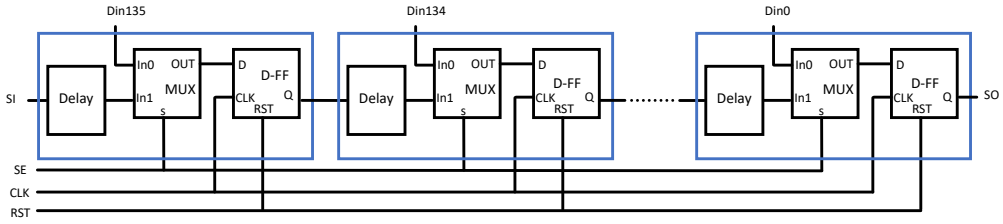



Figure 6.17: Output shift register.

### 6.2.11 Array Architecture

The architecture of Chip 3 is illustrated in Figure 6.18, which features an array of 5 × 8 pixels. We also include a row of test pixels, in which we have access to critical nodes within the pixel for validation purposes. Ten 16-to-1 multiplexers are used to gain access to sixteen nodes in each of the ten selected pixels through digital I/O pads. This design enables access to transient data from critical nodes, including direct output from sub-pixels, SRAM enable signal, SRAM MSB and LSBs, counter outputs and input, and the edge-detector output. Additionally, five analog buffers are employed to drive and access the outputs of the CSA and comparator in a single pixel through analog I/O pads. Three 136-bit parallel-to-serial shift registers are used to send serial data out from two counters as well as all sub-pixel outputs from sixteen selected pixels.

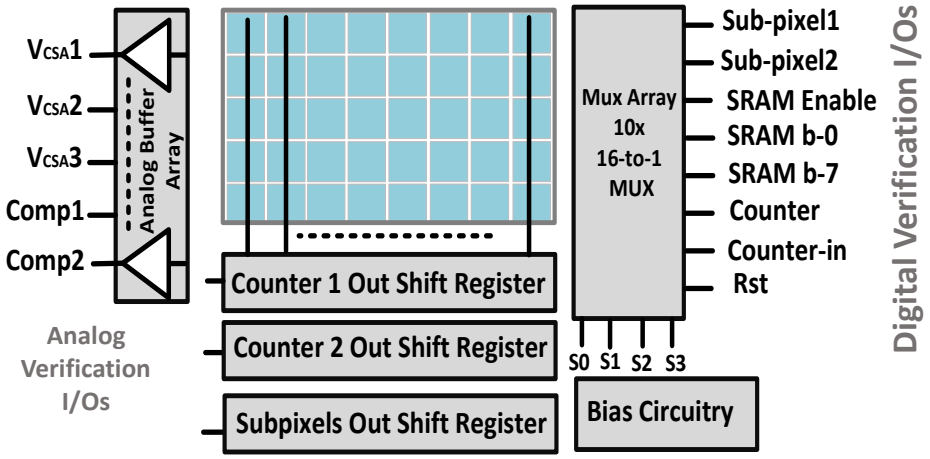



Figure 6.18: Chip 3 architecture.

### 6.2.12 Physical Implementation

Figure 6.19 shows the detailed layout of a pixel and one of its sub-pixels, along with the pixel area breakdown. Each sub-pixel occupies an area of 45 × 45 $\mu m^2$, and the entire pixel covers an area of 92 × 92 $\mu m^2$. Each sub-pixel DAC, comparator, and 8-bit SRAM occupies an area of 20 × 6 $\mu m^2$ , 20 × 9 $\mu m^2$ , and 6 × 22 $\mu m^2$ , respectively. The combined area of the two counters and digital multiplexers is around 780 $\mu m^2$. The CSA occupies 20 × 23 $\mu m^2$.The distribution of area across the entire pixel is also depicted in the

figure. The substantial portion occupied by the digital circuit underscores the significance of our sub-pixel SPE enhancement architecture, facilitating shared digital circuits among sub-pixels.

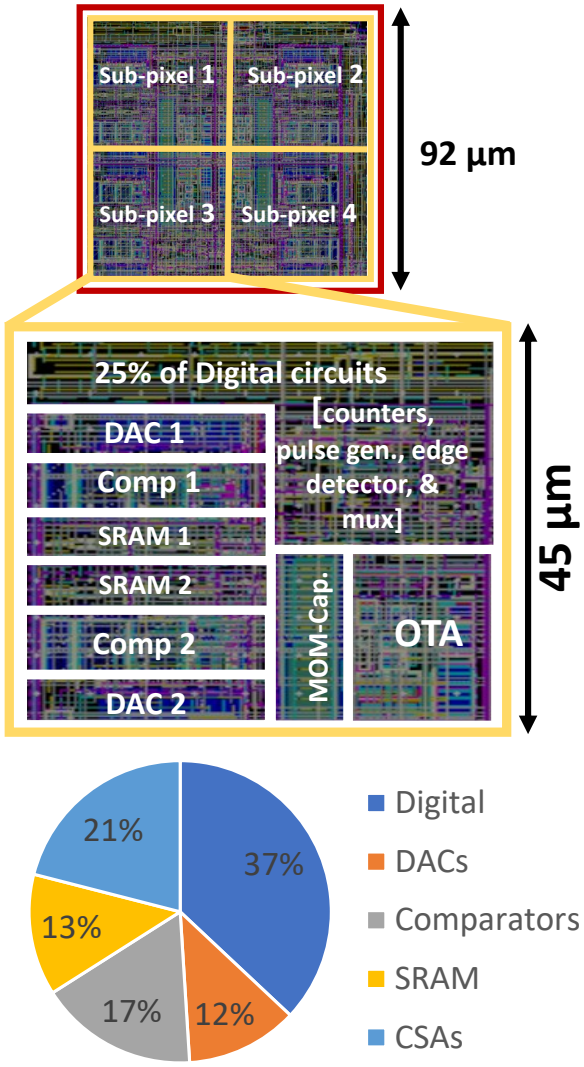



Figure 6.19: Pixel physical implementation and area breakdown.

## 6.3 Simulation Results

This section presents post-layout and Monte Carlo simulations of Chip 3 along with transistor-level functional-verification simulation results for critical blocks.

### 6.3.1 CSA

We use the CSA from Chip 2 in Chip 3. Simulated results of this CSA are presented in Chapter 5.

### 6.3.2 Comparator

The post-layout simulation results for the comparator indicate an average propagation delay of 89 ns and a slew rate of 9 V/ns with a preamplifier dc gain of 44.5 dB ($\Delta V_{out}/\Delta V_{in}$) in its linear region, as seen in Figure 6.20. The comparator also draws a dc current of 950 nA.

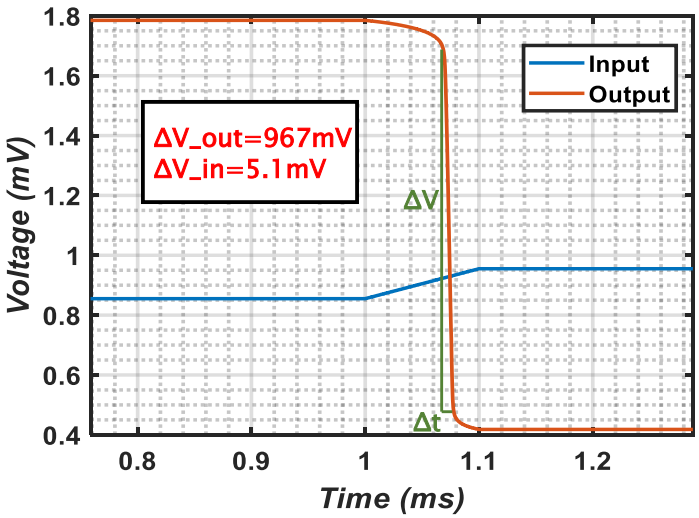



Figure 6.20: Post-layout simulation result of comparator propagation delay and slew rate.

The 1000-point simulated $V_{os}$ in all process and temperature corners, along with introduced mismatch on the post-layout extracted view, results in an average $V_{os}$ of 30 mV with

a large standard deviation $\sigma$ of 2.5 mV, as shown in Figure 6.21. These results suggest that while the propagation delay and slew rate are within acceptable limits, the $V_{os}$ may need correction to achieve a $\sigma$ of less than 0.7 mV.

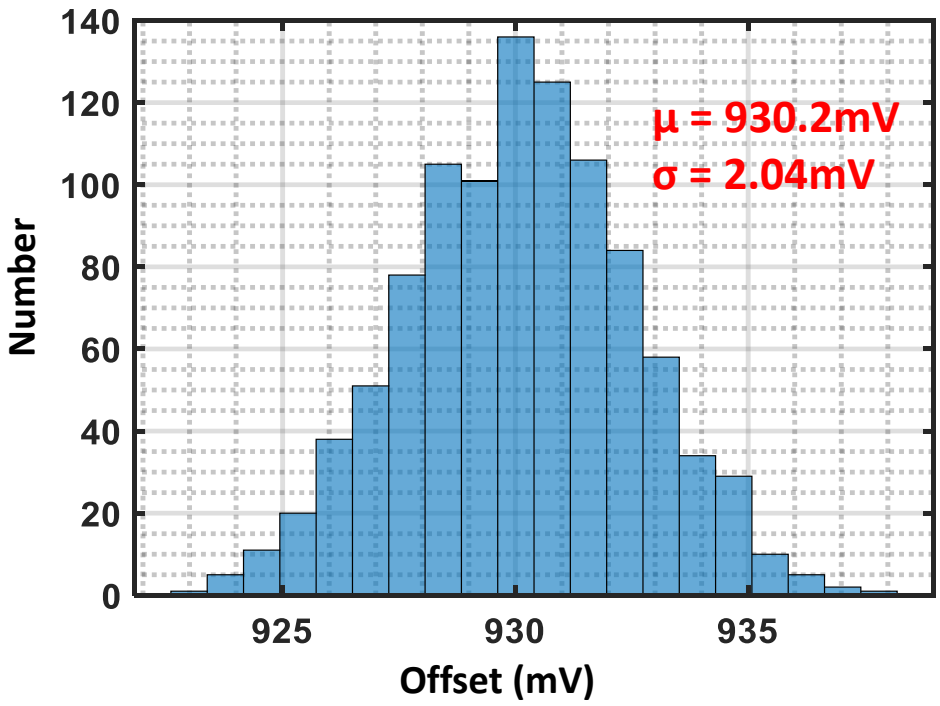



Figure 6.21: Monte Carlo simulation of results comparator input offset voltage distribution.

### 6.3.3 Current-Steering DAC

Here we examine the functionality of the proposed PWL current-steering offset-calibration DAC. First, we model the sensitivity of a reduced-area linear DAC to mismatch, where its simulated transfer function is shown in Figure 6.22. The figure displays a zoomed-in view of the DAC TC by showing the comparator input-referred offset by adjusting its current as explained in 6.2.4. We show the comparator offset for each DAC digital input point where the currents are biased such that internal offset becomes zero after the MSB toggles.

Next, we highlight the MSB mismatch impact by showing four different mismatch cases introduced only to the MSB, while keeping the other bits ideal. First, we show a zoomed-in view of the TC for the DAC without PWL biasing when the MSB toggles, in Figure

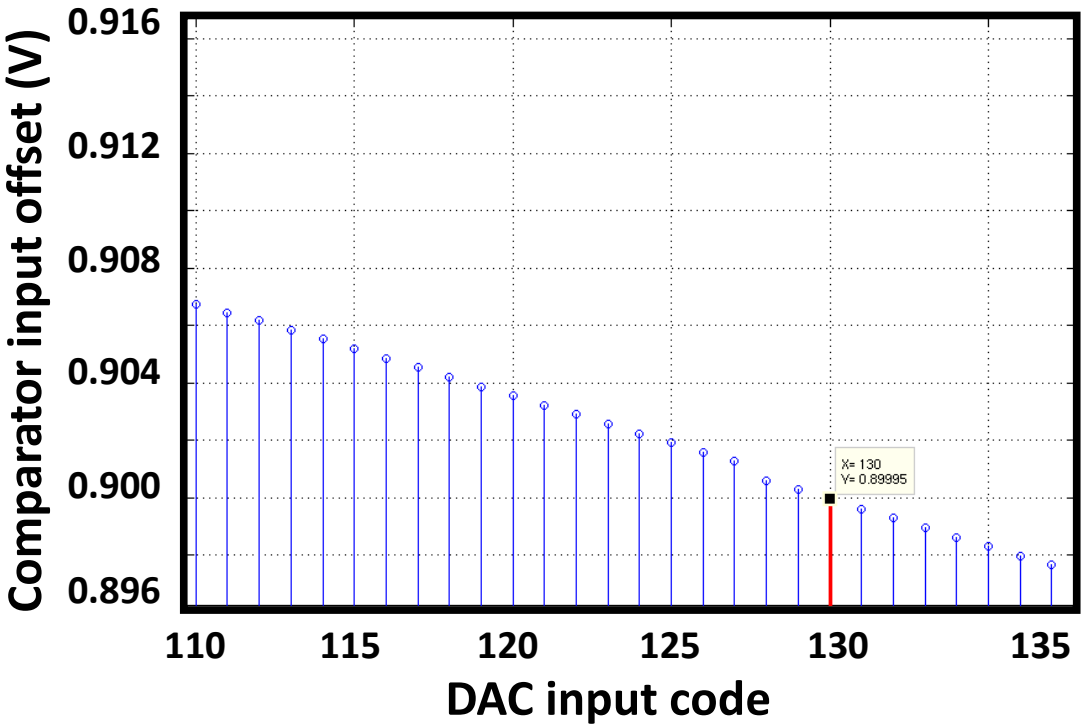



Figure 6.22: Simulated DAC transfer characteristic.

6.23. For simplicity, we bias the current cells such that $V_{os}$ becomes zero when the MSB toggles. Figure 6.23(a) and (c) shows the TC with mismatch on MSB current cells where the comparator offset changes by around $\pm 2$ mV from its ideal case when the MSB toggles. The calibration circuit is designed to end the correction process once the comparator offset becomes equal to or less than zero. We store the comparator offset when the calibration ends, and the error can be defined as the difference between the stored offset and the ideal (zero) offset. When the mismatch alters the offset from its ideal case, reducing it by $\sim 2$ mV as in Figure 6.23(a), this error will be stored as the compensated offset of the comparator as shown in Figure 6.23(b). However, when the comparator offset becomes larger than the ideal case due to mismatch, by around 2 mV, as in Figure 6.23(c), the calibration will not end when MSB toggles, but rather at a greater digital input when another bit toggles, as in Figure 6.23(d). Therefore, the error will be at our LSB scale, which in this specific simulation is around 110 $\mu$V for +2 mV applied mismatch.

Additionally, we run Monte Carlo simulation on our piecewise linear DAC by introducing mismatch on all three MSB devices (b5-b7), as previously shown in Figure 6.10.

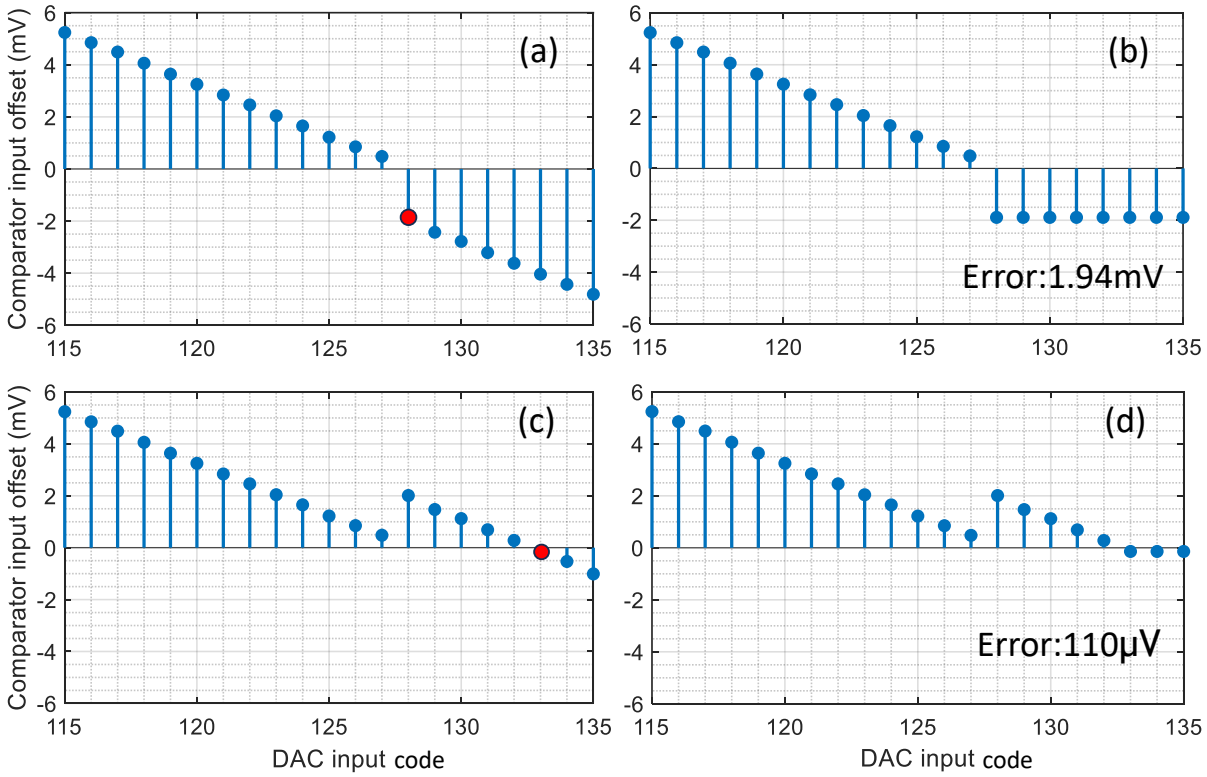



Figure 6.23: Simulated DAC TC and corrected offset with MSB mismatch. (a) DAC TC when MSB offset is shifted by -2 mV and (b) stored offset vs. digital input for this case. (c) DAC TC when offset at MSB, is shifted by +2 mV due to mismatch and (d) stored offset vs. digital input for this case.

The MSB bits are biased such that the comparator offset becomes larger than that of its previous digital input when they toggle, independent of how large the mismatch impact is, shown in Figure 6.24. To properly set the bias voltage for MSB devices, we find the standard deviation in comparator offset distribution imposed by $V_t$ mismatch after running Monte Carlo simulation, and we bias the MSB current cells such that the resulting offsets are $3\sigma$ greater than its ideal case when the MSBs change. This will ensure the MSB mismatch has no impact on the stored offset.

Finally, we perform post-layout Monte Carlo simulation in different process and temperature corners for the entire DAC with the comparator. We use a 30-point Monte Carlo simulation in each typical-typical (TT) corner at 25 °C, slow-slow (SS) corner at 0°C,

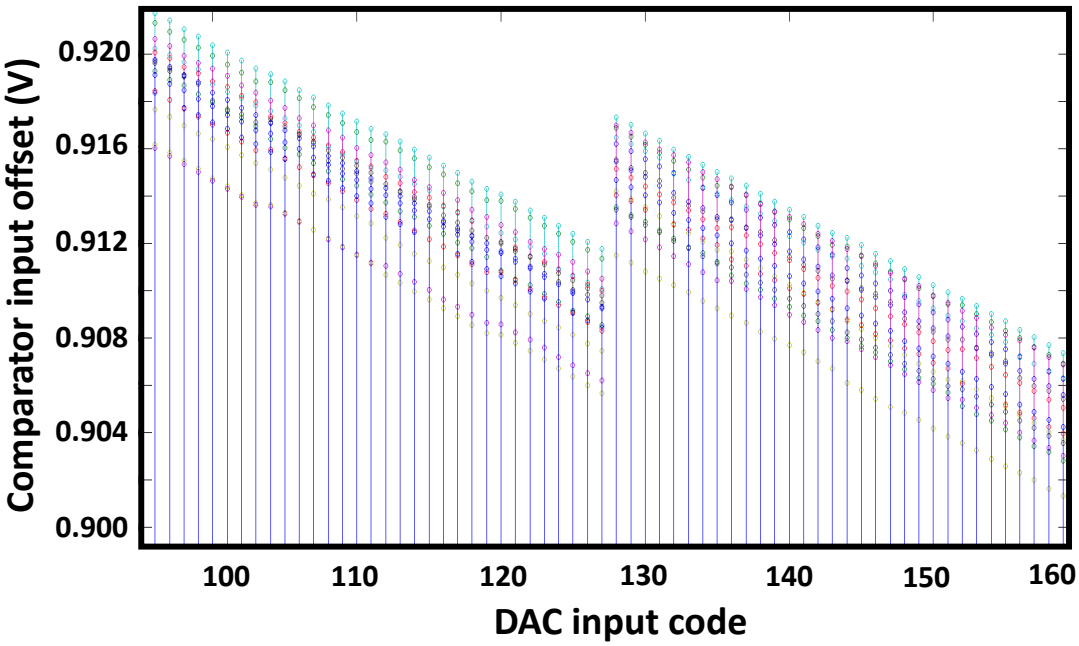



Figure 6.24: Monte Carlo simulation result where DAC mismatch is applied to only MSB.

fast-fast (FF) corner at 50°C, and fast-slow (FS) corner at 25°C. Figure 6.25 shows the histogram of change in the offset when we increment the input bits. We have plotted the histogram of step sizes for LSBs and MSBs separately in each corner. For MSBs, both the average and standard deviation are higher than 2.1 mV and 2.3 mV, respectively, in the worst case. On the other hand, the average and standard deviation of LSB steps is 412 $\mu$V and 114 $\mu$V, respectively, in the worst case. However, as stated earlier, the notable advantage is that our calibration resolution will be dictated by the average steps in LSBs, which is within our requirements.

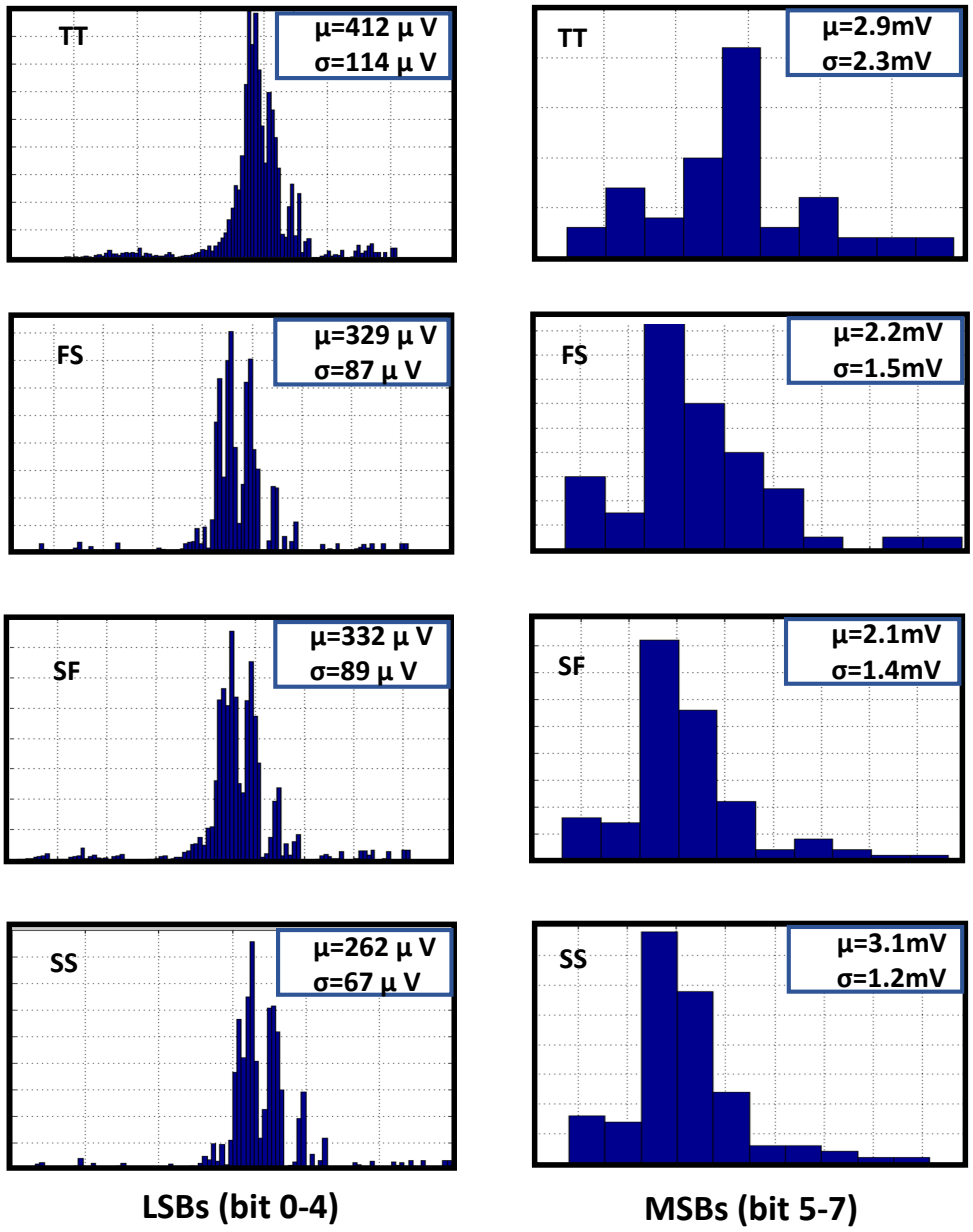



Figure 6.25: Simulated DAC Monte Carlo process and temperature corner results.

### 6.3.4 6T SRAM

We also provide post-layout 120-point Monte Carlo simulation results in all process and temperature corners for our 8-bit 6T SRAM. Based on these simulations, the single-bit 6T SRAM has a write and read access time of less than 0.9 ns in all corners, which enables a fast write frequency of approximately 1 GHz. This fast access time allows for a quick calibration phase, although the time taken for calibration is not a constraint because the calibration method is conducted in the foreground and only performed once before the start of the photon-counting mode and X-ray exposure.

The simulated butterfly curve is displayed in Figure 6.26. The static noise margin (SNM) of 507 mV is indicating strong stability of our designed cells. The SRAM single cell consumes 0.3-nW and 153-$\mu$W static and dynamic power, respectively, from a 1.8-V supply.

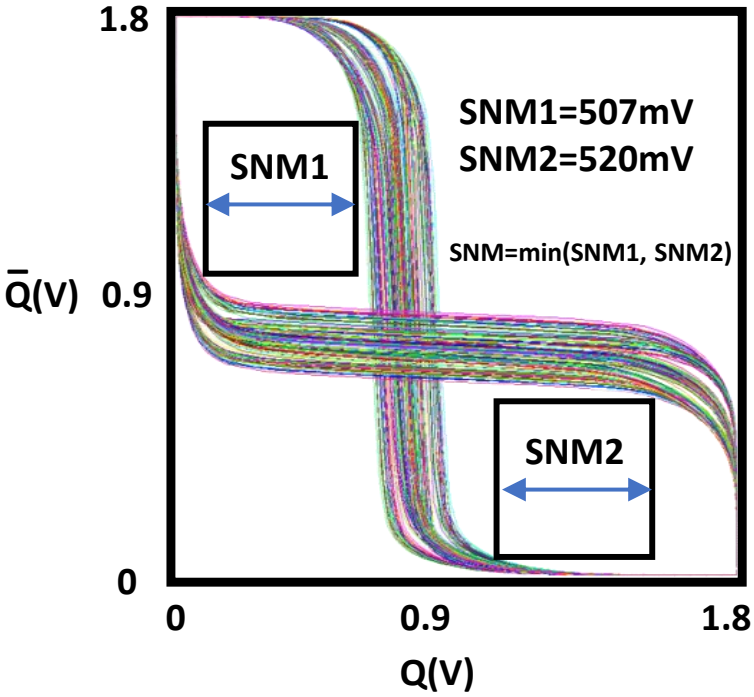



Figure 6.26: Simulated single SRAM cell butterfly curve.

### 6.3.5 Foreground Input-Offset Calibration

We simulate the entire foreground-calibration circuit to verify its functionality and reliability. The circuit comprises a CSA, comparator, 8-bit reduced-area PWL DAC, 8-bit 6T SRAM cell, and 8-bit counter, as illustrated in Figure 6.8. The complete calibration cycle and testing of the stored offset are shown in Figure 6.27, along with the corresponding signals. During calibration mode, when the calibration signal is enabled, and the entire circuit comes out of reset, the counter is multiplexed to an external clock used to sweep the DAC current. As depicted in the figure, due to an intentionally designed large systematic input offset, the comparator output is high, which sets the SRAM enable, SRAM_en, signal. This allows the SRAM to be written to, and as the counter is swept, the corresponding code is stored in the SRAM in each clock cycle. However, as the digital input is increased, the comparator offset changes, and at a specific point highlighted in the figure, it toggles, disabling the SRAM write signal. We also show the counter and SRAM's LSB and MSB outputs.

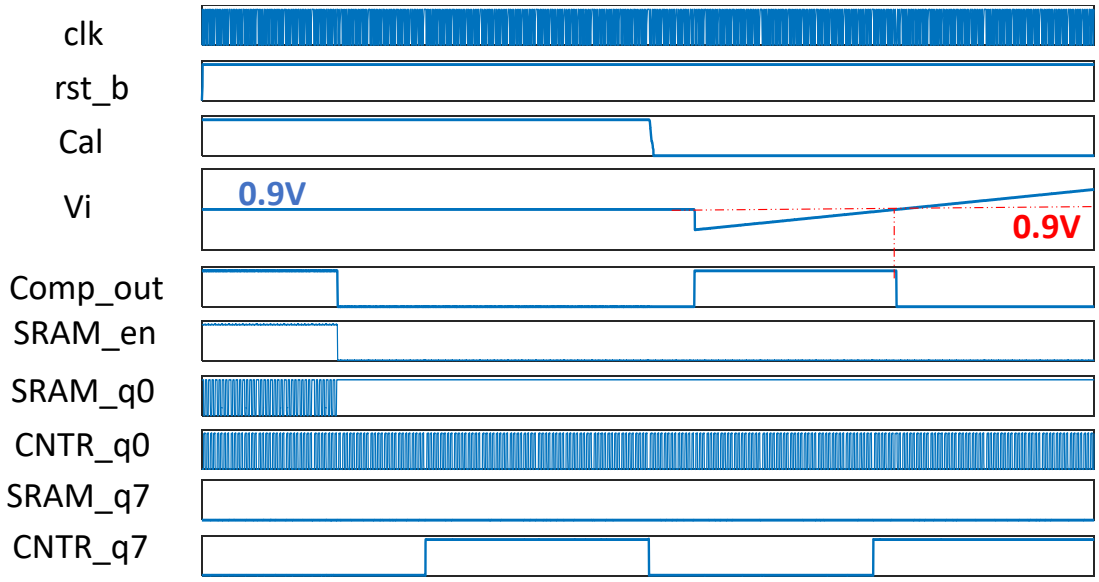



Figure 6.27: Foreground-calibration circuit post-layout simulation results.

After this point, the SRAM no longer changes its stored value, effectively storing the corrected offset. The counter-sweeping continues until the code reaches 256, at which point the calibration signal goes low. The reason for continuing the clocking is that the pixel is designed to calibrate all eight comparators at the same time and with the same counters,

each toggling at different points. After calibration, the comparator input signal is swept from 0.7 V to 1.1 V to verify the offset is corrected, as shown in the figure. The comparator toggles once both inputs are equal (i.e., 0.9 V and not 0.930 V as prior to calibration). This simulation verifies the functionality of our proposed background calibration scheme.

We next run a 400-point Monte Carlo simulation on the entire foreground-calibration circuit. The comparator offset is measured before and after calibration for each point to assess the circuit's performance. The simulation results shown in Figure 6.28 indicate that the standard deviation of the comparator offset before calibration is 2.3 mV, with an average of 30.7 mV. However, after calibration, the standard deviation significantly decreases to 280 $\mu$V, with an average offset of 97$\mu$V. This demonstrates the functionality and reliability of the proposed foreground-calibration circuit.

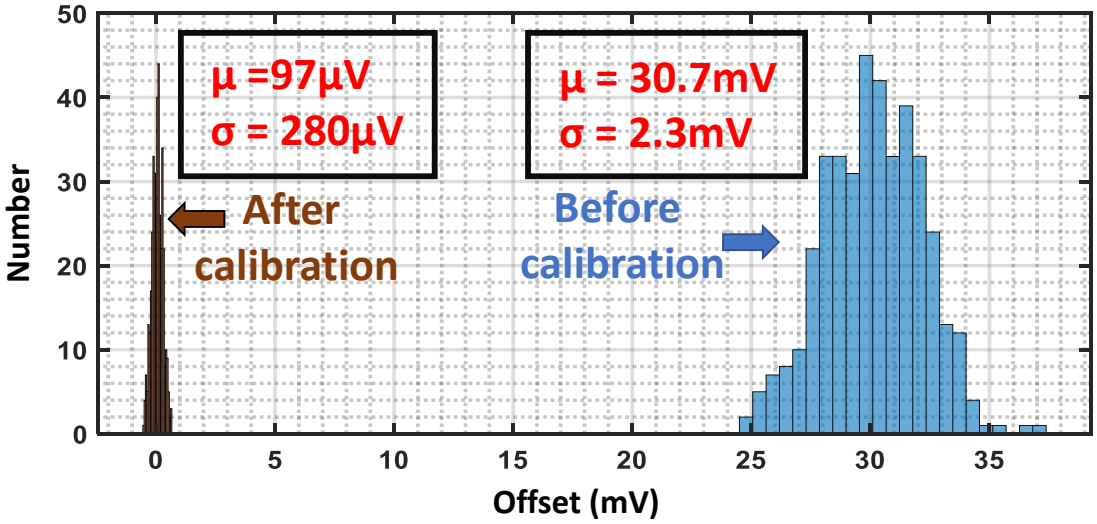



Figure 6.28: Comparator offset distribution from Monte Carlo simulation before and after calibration.

### 6.3.6 Complete Pixel Operation

We conduct pixel-level simulations to evaluate the complete pixel, including its foreground-calibration circuit and sub-pixels. Figure 6.29 shows the output of both sub-pixels and applied charge pulses modeling our desired photon energies of 20 keV and 40 keV. The

simulation results demonstrate successful photon detection and energy discrimination of the complete pixel.

For the 20-keV photons, only sub-pixel 1 is toggled, indicating accurate detection of low-energy photons. Conversely, for the 40-keV photons, both sub-pixel 1 and sub-pixel 2 toggle. Monte Carlo simulations, performed with 100 points on the complete pixel, detect and discriminate between these two photon-energy levels with 100% accuracy.

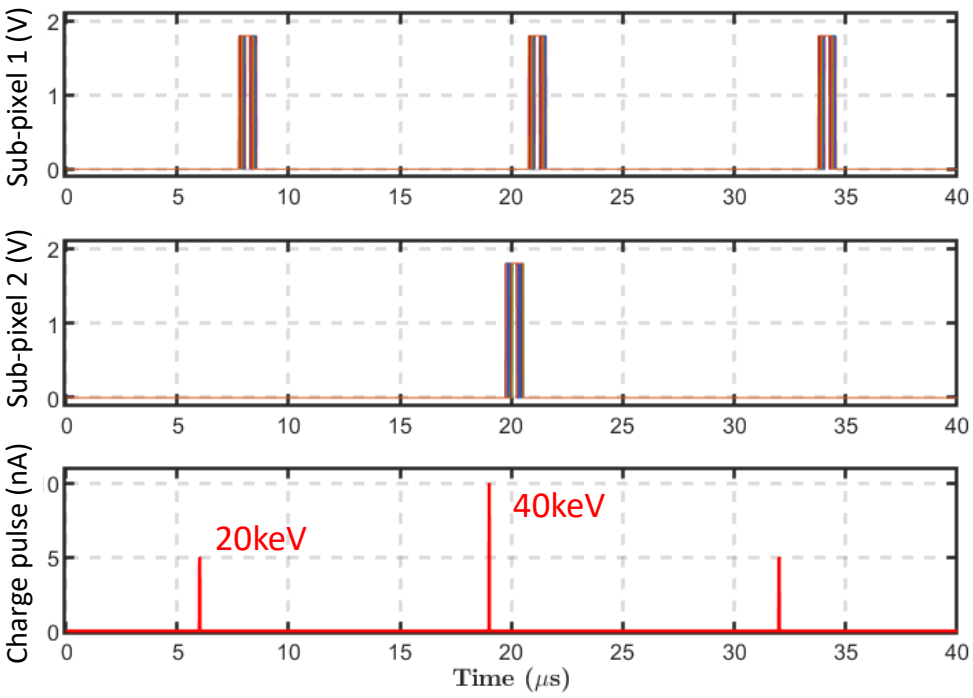



Figure 6.29: Simulated pixel functional operation.

## 6.4 Fabrication and Post-Processing

### 6.4.1 Chip Fabrication

We fabricated Chip 3 in a 0.18-$\mu$m analog/mixed-signal 1P6M CMOS process. Figure 6.30 shows the fabricated chip micrograph with its floor plan illustrating the pixel arrays, multiplexers, shift registers, and analog buffers. The chip area is 1.5 $\times$ 2.5 mm$^2$, and it contains an array of 5 $\times$ 8 pixels. Each pixel consumes 11 µW from a 1.8 V supply.

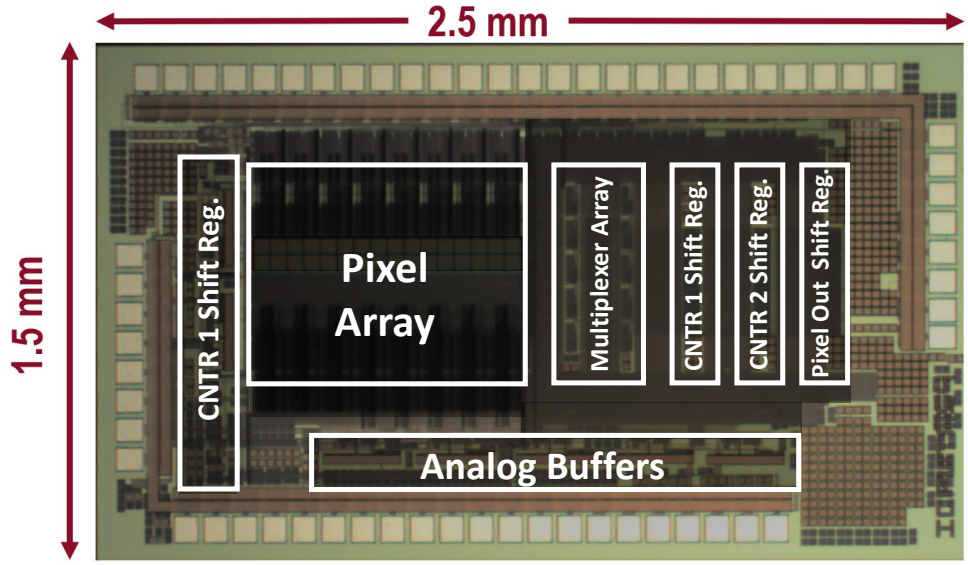



Figure 6.30: Micrograph of Chip 3.

### 6.4.2 Shadow Masks for a-Se/Au Post-Processing

We designed two shadow masks for a-Se and Au (gold) deposition. The masks contain two arrays of 3 $\times$ 5 and 4 $\times$ 5 pockets with slightly different opening sizes (around 1 mm

× 2 mm) to ensure that chips will fit properly. We made these shadow masks with 2.5-mm-thick 7075 aluminum. Figure 6.31 shows the fabricated masks for a-Se/Au deposition, chip exposed area before processing, and a micrograph of the fabricated pixel with four sub-pixel top-metal openings.

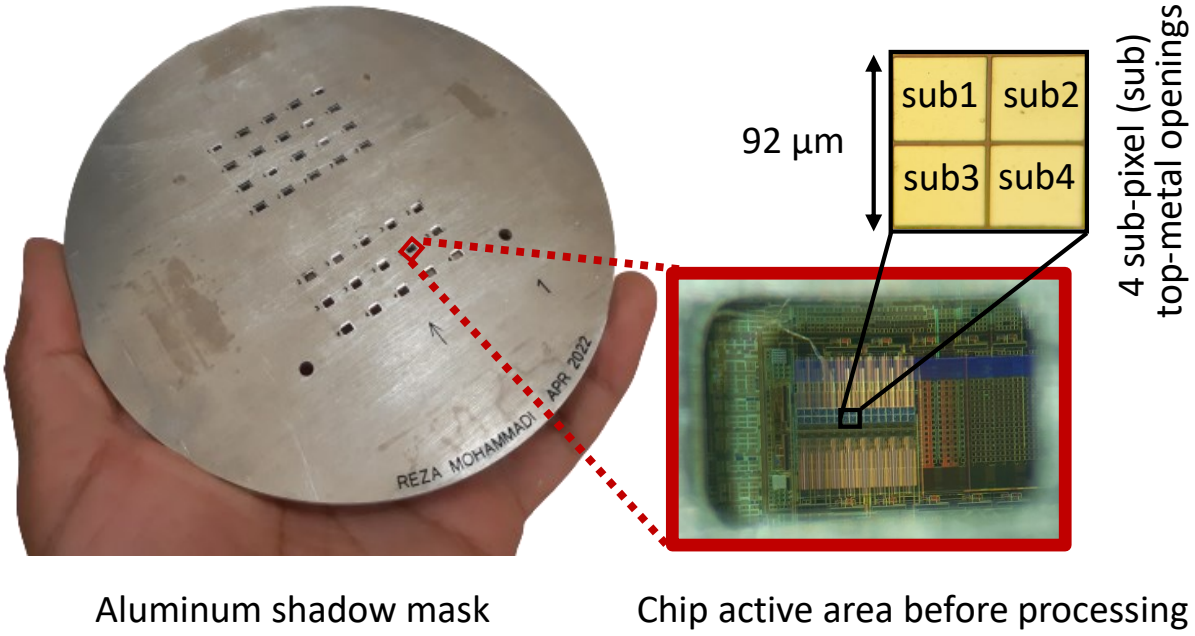



Figure 6.31: Mask for a-Se/Au deposition, chip exposed area before post-processing, and micrograph of the fabricated pixel with four sub-pixel top-metal openings.

Figure 6.32 shows a micrograph of our a-Se/Au processed chip. To benefit from SPE, we increased the a-Se thickness as much as it could reliably be processed. The thermally evaporated 115-µm-thick a-Se sensor is covered with a 50-nm-thick Au bias electrode.

### 6.4.3 Wirebonding and Packaging

We package and wirebond the chip, followed by making the HV bond connection in the same way as was done for Chip 2. While this process is mostly the same, we developed a new approach to form the HV connections to bias a-Se. Our new method not only improves

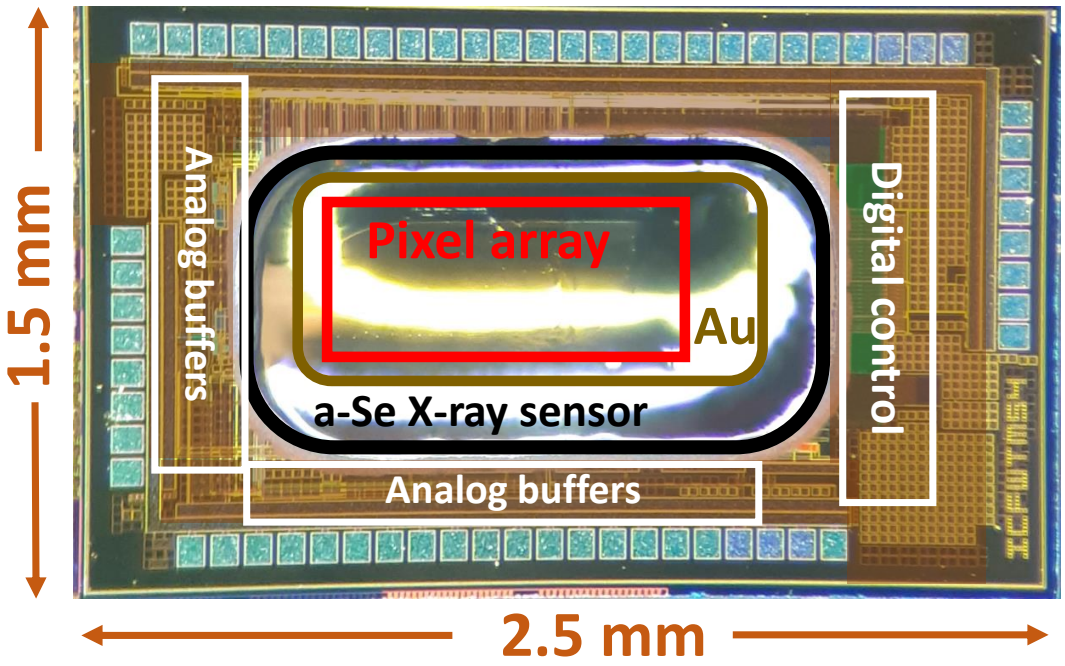



Figure 6.32: Micrograph of the a-Se/CMOS SPC imager.

precision and yield, but also reduces the requisite time to approximately half. The detailed steps are shown in Figure 6.33.

In forming the HV connection to the Au bias electrode, we leverage the capabilities of the manual wirebonder, instead of the manual process we used for Chip 1 and 2. The process begins with immersion of the wire in a specialized liquid silver paste, subsequently directing the capillary towards the chip, shown in Figure 6.33(a), (b), and (c). Once the capillary is positioned sufficiently close to the chip, we elevate the chip to establish contact with the wire, as in Figure 6.33(d), a maneuver executed with high precision using the position adjusting knobs. Following this, we leave the wirebonder untouched, allowing the silver to cure, which typically takes 24 hours. Finally, we make the second bond to the pad instantly as a normal ball bond rather than waiting another 24 hours, as shown in Figure 6.33(e). Our method, which we refer to as cold-solder-ball/ball bonding (CS3B), saves time and cost by offering a very-high-resolution HV connection with almost 100% yield compared to attaching the HV connection in a completely manual way. Figure 6.33(f) shows our processed, packaged, and wirebonded chip with its bonded HV connection.

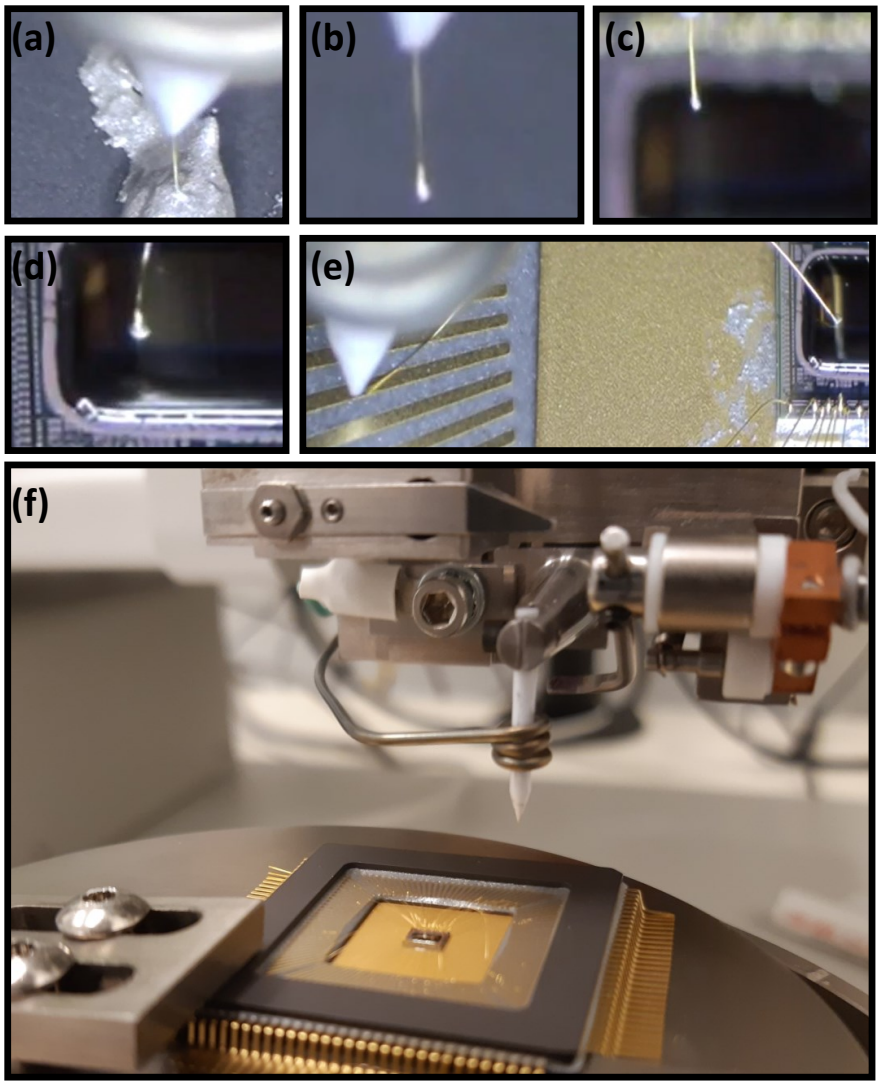



Figure 6.33: CS3B wirebonding process. (a) Immersion of the wire in a specialized liquid silver paste. (b) and (c) Directing the capillary toward the chip. (d) Elevating the chip to establish contact with the wire. (e) Making the second bond. (f) Wirebonded and HV-bonded Chip.

## 6.5 Experimental Results

### 6.5.1 PCB Design

To test Chip 3, we design the 30 cm × 17 cm four-layer PCB shown in Figure 6.34 with two outer routing layers and two inner power/ground layers. Two critical biases for Chip 3 are the pixel thresholds and reset voltages. We employ six low-noise 16-bit AD5662 DAC set to a 250-$\mu$V LSB, to generate all biases. These DACs enable semi-automatic characterization of the chip by sweeping the voltages with flexible and precise steps.

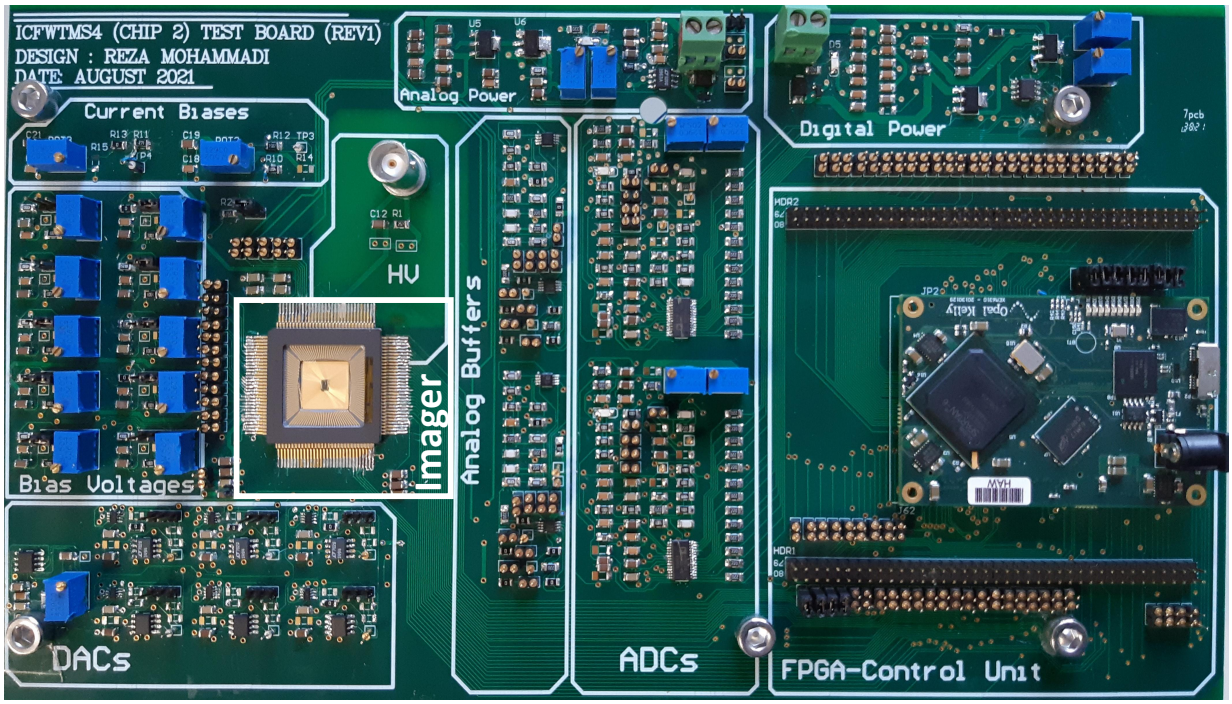



Figure 6.34: Custom-designed PCB used to characterize Chip 3.

### 6.5.2 Electronic Characterization Results

Figure 6.35 shows a measured histogram of the CSA output under dark conditions. Notably, the measured input-referred noise is 1.3 $mV_{rms}$, which equates to 83 $e^-{}_{rms}$, or 3.4 keV, given the ∼48-eV ionization energy of a-Se [35]. This histogram is mreasured

when a-Se is biased with a 8-V/$\mu$m field and incorporates all noise sources in the system, including CSA electronic noise and a-Se dark-current shot noise.

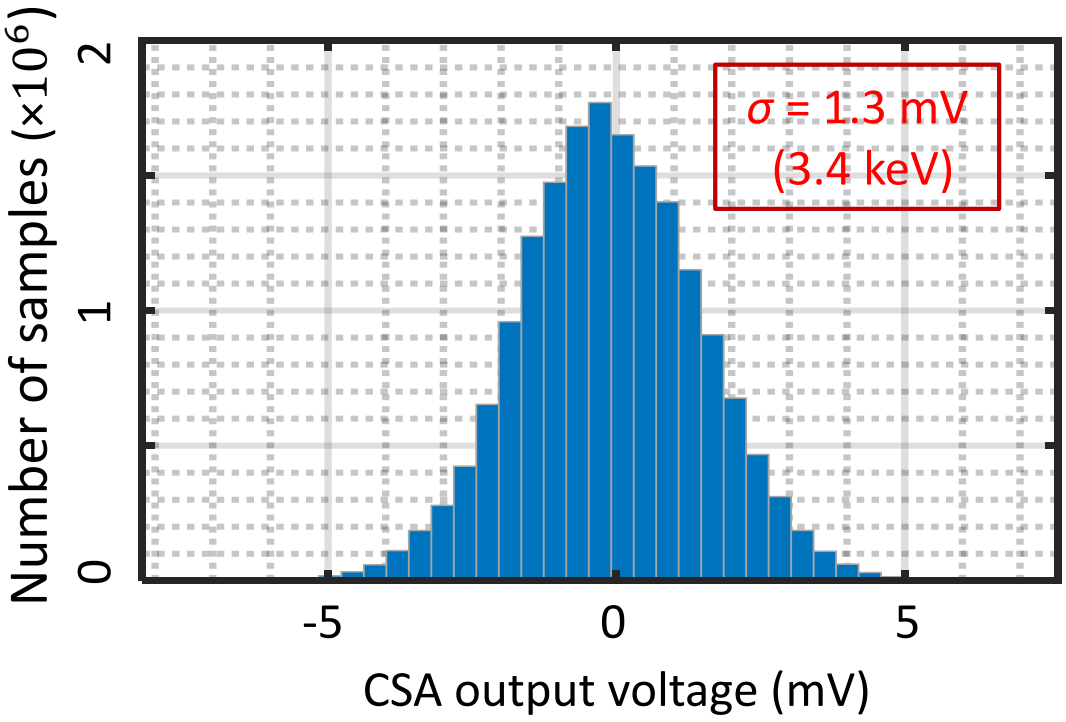



Figure 6.35: Measured histogram of CSA output voltage under dark conditions.

In order to assess the effectiveness of our offset-correction technique, we measure the comparator input offset as a function of DAC input code. Our results are presented in Figure 6.36. Systematic offset, $V_{os}$, is observed at code '0'. As the DAC code increments, the current $I_{cal}$ increases, leading to a reduction in $V_{os}$. The correction cycle ends when $V_{os}$ is approximately zero and $V_{comp}$ toggles. The mean step size for the MSBs is approximately 3 mV with a standard deviation of 1.6 mV, while for the LSBs the mean step size is 0.23 mV with a standard deviation of 0.22 mV.

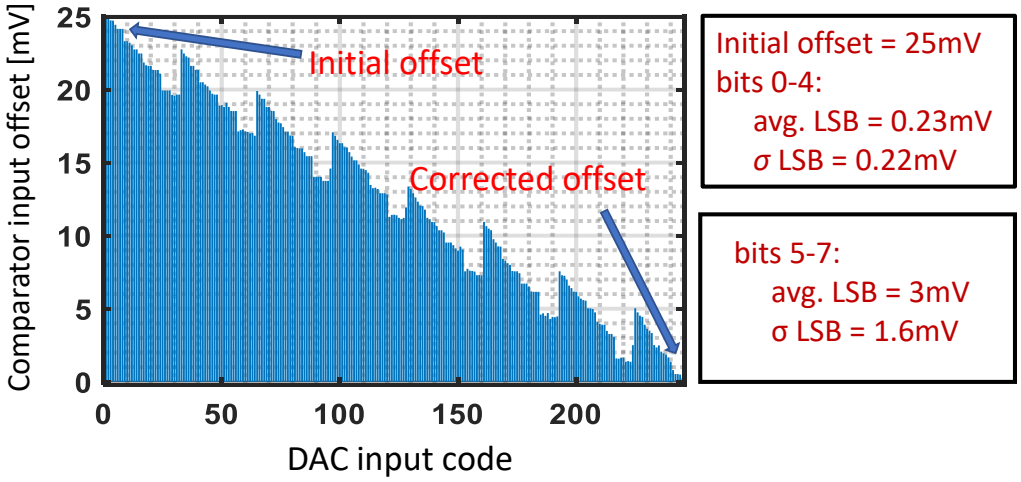



Figure 6.36: Measured transfer characteristic of sub-pixel DAC.

Although the DAC is PWL, the calibration circuit only stops when the offset is reduced compared to its previous value as the input increments. This can happen only when LSBs are changing since when MSBs toggle, the comparator offset becomes greater than its previous value. Therefore, the calibration will be impacted by negative steps and it will end when zero offset is passed. The steps that can effectively terminate the offset correction are given in Figure 6.37(a). By plotting these applied offset voltages, we show the effective TC in Figure 6.37(b), which is linear and its resolution is defined by the LSBs.

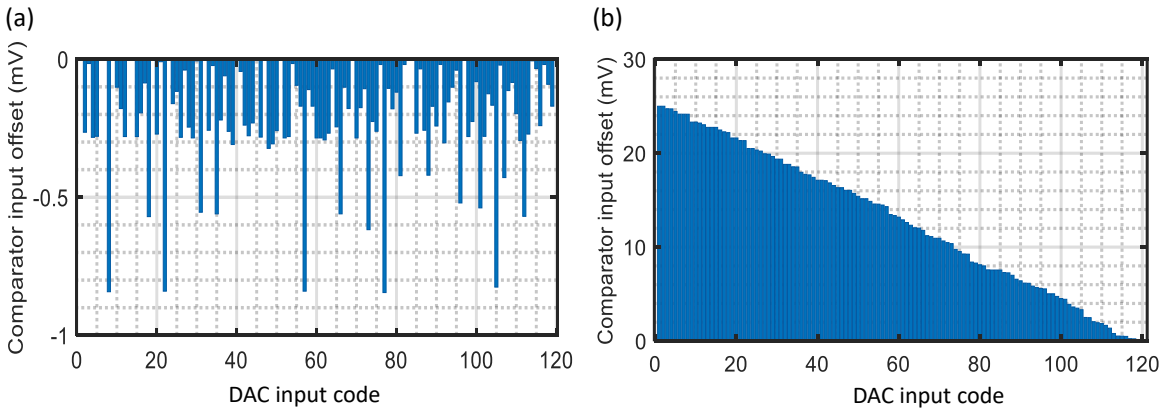



Figure 6.37: Measured effective (a) offset steps and (b) DAC TC.

The comparator TC is obtained by sweeping the threshold voltage and measuring the comparator output 1000 times at each threshold voltage for 32 comparators, as shown in Figure 6.38. Before correction, the mean offset is 29 mV, with a standard deviation of 2.1 mV. After correction, the offset is reduced to 0.05 mV, with a standard deviation of 0.42 mV. This is equivalent to a noise of 1.5 keV, or 21 $e^-_{rms}$.

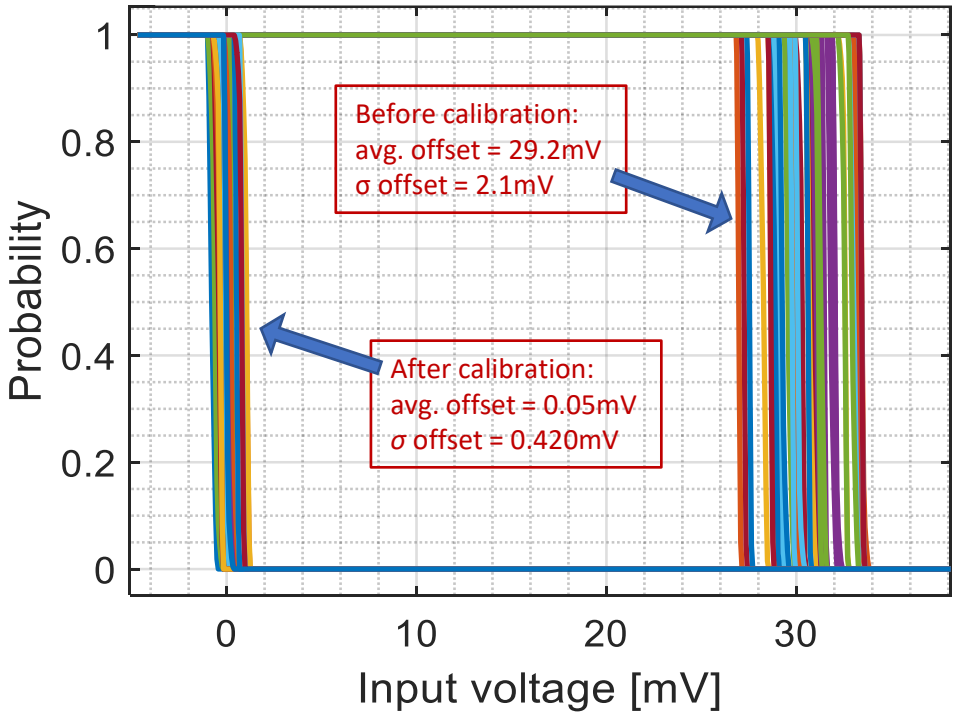



Figure 6.38: Measured foreground offset-calibration results showing comparator input-referred offset voltage before and after calibration.

Figure 6.39 shows the histogram of input-referred offset distribution before and after calibration for $32 \times 10^3$ measurements. These results confirm that the correction is performed at the LSB resolution and is not affected by high-mismatch-prone MSBs. Moreover, our results demonstrate that our correction scheme is accurate and meets our application requirements.

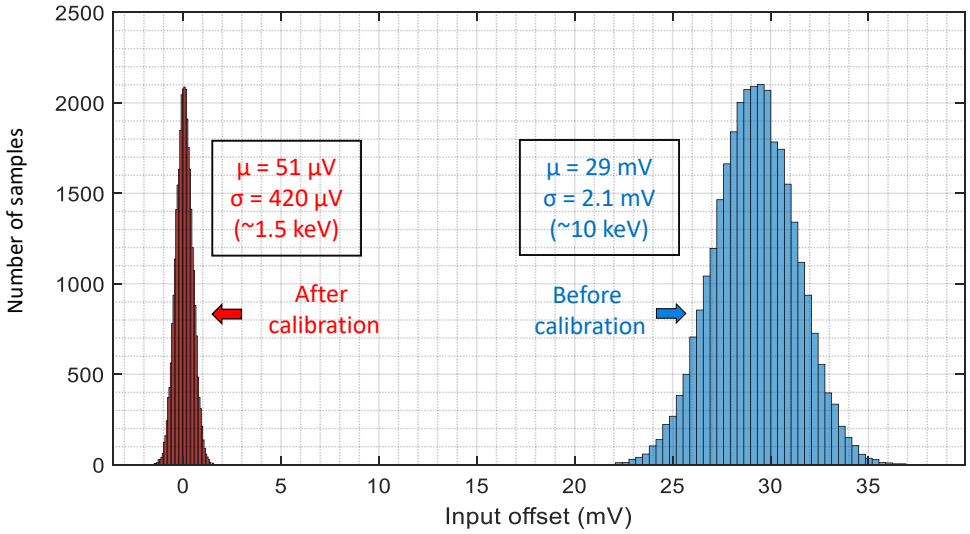



Figure 6.39: Measured histogram of comparator input offset before and after calibration.

### 6.5.3 Single-Photon-Counting Results

Figure 6.40 shows our experimental setup for photon-counting measurements and Figure 6.41 displays our measured results for 65-keV and 41-keV photons. This is the first demon-

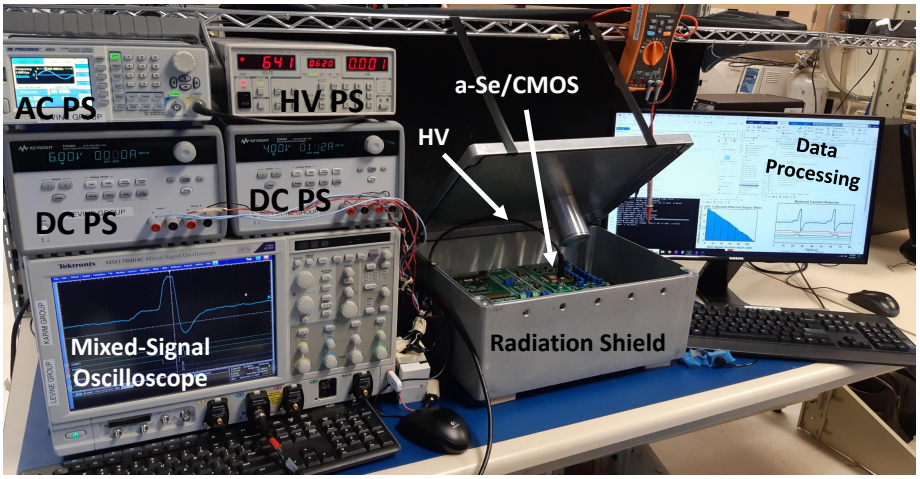



Figure 6.40: Experimental setup used to characterize the photon-counting performance of Chip 3.

stration of dual energy-discriminating photon-counting with an a-Se/CMOS X-ray-detector pixel. By leveraging SPE and adaptive RC discharge, we obtain a photon-processing time of about 13.8 $\mu$s This translates to 35 Mcps/mm$^2$ count-rate density, roughly 25× improvement compared to the conventional response with the same pixel size. The figure also shows that photons with two different energies are successfully discriminated. For a 41-keV photon, when the CSA output CSAout crosses Vth1, the output from comparator 1 Comp1Out toggles, triggering the control signal Vctrl to reset the capacitor and input clock to the counter 1 Cntr1clk only. This shows that only the low-energy photon counter is being clocked in response to the 41-keV photon, and for 65-keV photon, both comparators toggle and both counters are clocked.

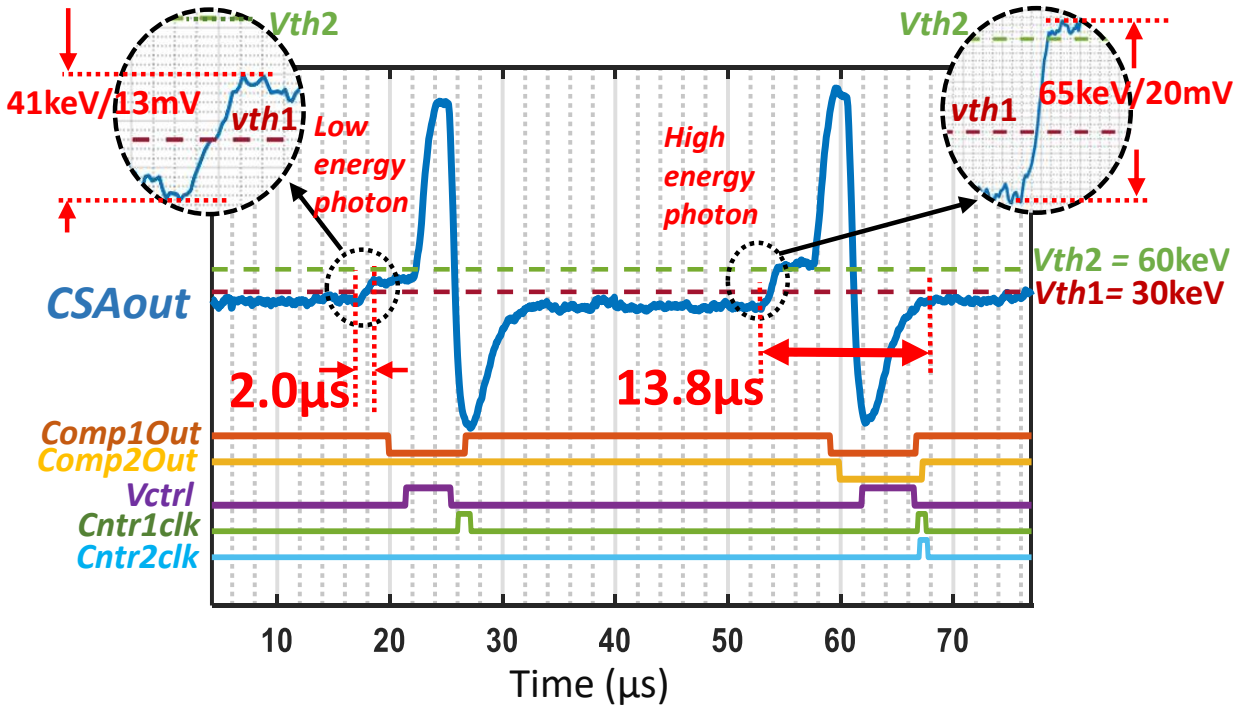



Figure 6.41: Pixel transient response showing the first demonstration of energy-discriminating single-photon-counting with an amorphous semiconductor monotonically-integrated on CMOS.

Our measured PHS results are shown in Figure 6.42, demonstrating that our pixel achieves an energy resolution of 7.9 keV, which is a significant improvement compared

to non-integrated detectors. This translates to a minimum-detectable input signal of 161 $e^-_{rms}$ for a 48-eV a-Se ionization energy, indicating the high sensitivity of our pixel. By exploiting SPE, we are able to achieve around 2× improvement in energy resolution compared to the conventional response.

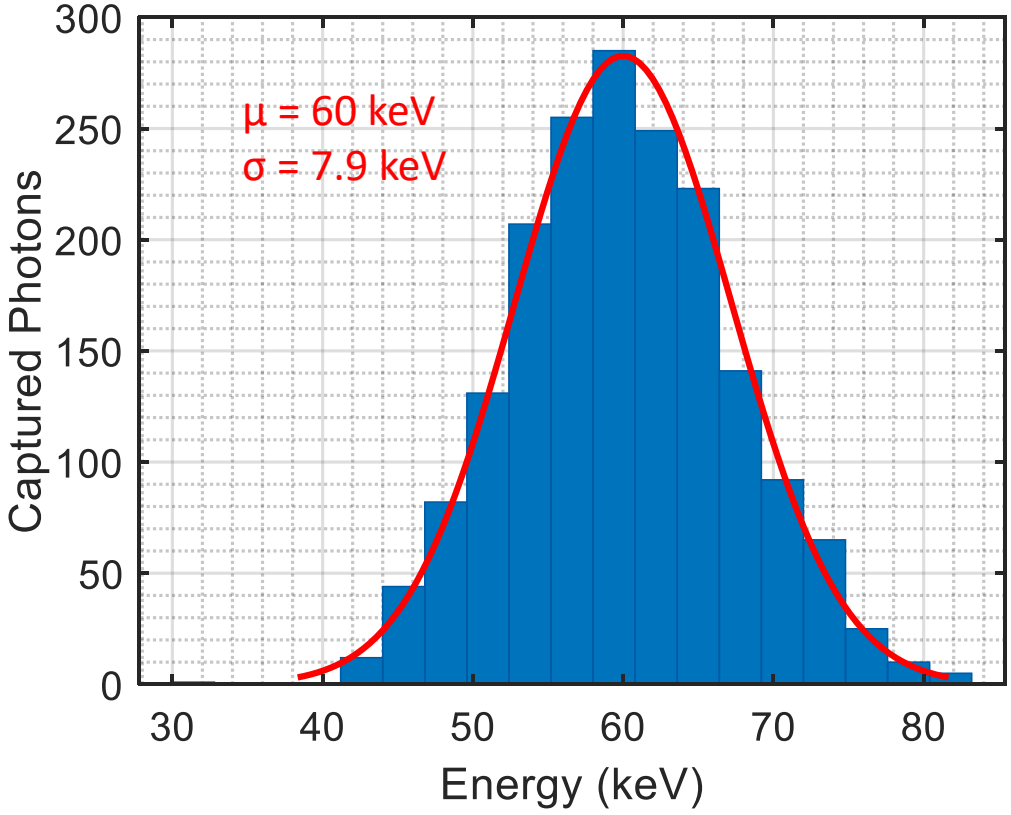



Figure 6.42: Measured pulse-height spectroscopy results from Chip 3.

In Figure 6.43, we show the number of detected photons for four sub-pixels, where the threshold voltages are set to 35 keV and 60 keV. The peak average energy for $^{241}$Am is 60 keV, with a 7.9-keV standard deviation from our PHS results. Therefore, approximately half the photons will have energy above 60 keV and the number of detected photons in our high energy bin would be around half the total number of detected photons. During two different measurements, M1 and M2, we count 2097 low-energy photons and 1190 high-energy photons, which is approximately double the high-energy photon numbers, demonstrating proper energy discrimination by our pixel.

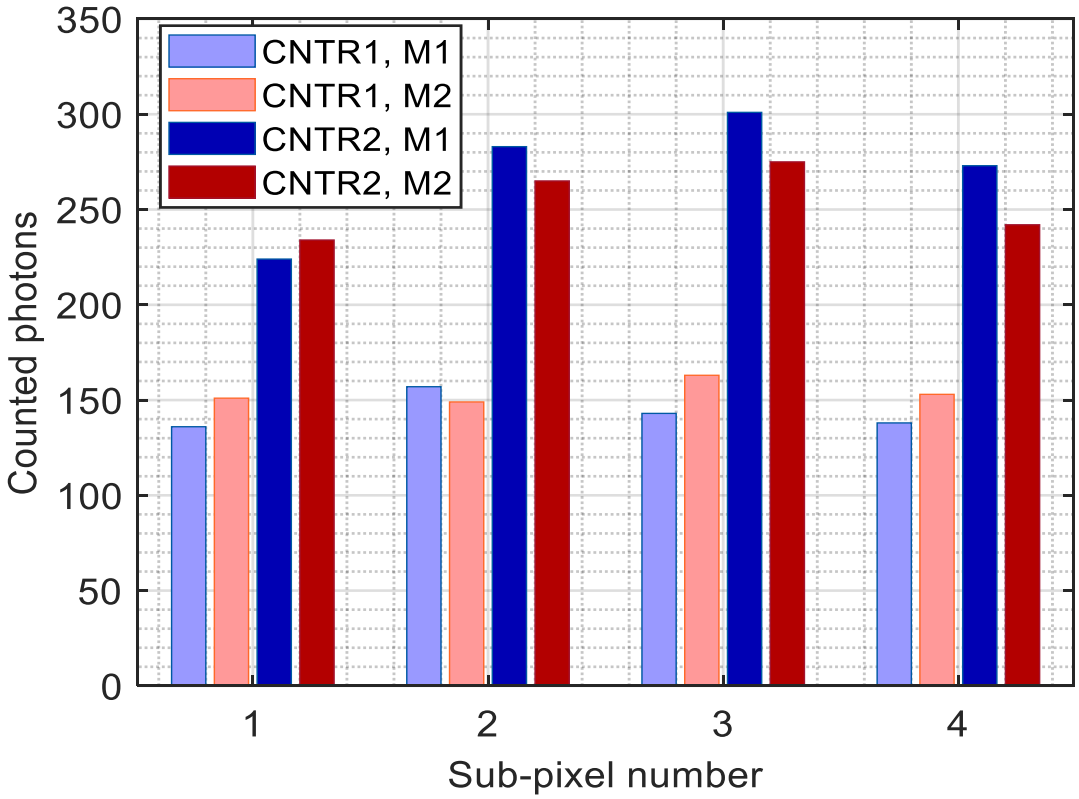



Figure 6.43: Energy-discriminating single-photon counting results from four sub-pixels from two different measurements.

Table 6.1 provides a comprehensive comparison of the performance of our pixel to other CMOS X-ray-detector pixels. The table shows that our pixel exhibits the highest energy resolution among the compared detectors while maintaining a comparable spatial resolution. This is due to the optimized design of our $45 \times 45$ $\mu$m$^2$ sub-pixel area, which allows for improved detection sensitivity and increased count-rate density. In the last two lines, for comparison purposes, we assume depositing a-Se on other chips and theoretically evaluate their performance compared to ours. Our imager achieves the highest SPE-factor and the shortest pixel rise time, assuming the rise time is linearly proportional to the SPE-factor. Moreover, the table highlights the unique advantage of our monolithic a-Se/CMOS pixel design, which enables a compact, low-power, and cost-effective solution for applications like DBCT, where high energy resolution is critical for detecting early-stage breast cancer.

Table 6.1: Comparison table.

| Parameter | Kim, ISSCC'12 | Kleczek, JSSC'18 | Kleczek, ESSIRC'19 | Rajendran, Radiol'22 | This work |
|---|---|---|---|---|---|
| **CMOS process [nm]** | 130 | 40 | 130 | 65 | 180 |
| **Sensor integration method** | Bump bond | Bump bond | Bump bond | Bump bond | Evaporation ☺ |
| **Pixel area ($d \times d$) [$\mu m^2$]** | 60 × 60 | 100 × 100 | 75 × 75 | 225 × 225 | 92 × 92 |
| **SPE-effective pixel area* ($d_{eff} \times d_{eff}$) [$\mu m^2$]** | Same as pixel area | | | | 45 × 45 ☺ |
| **Number of energy bins** | 3 | 1 | 2 | 2 | 2 |
| **X-ray sensor** | $HgI_2$ (polycrystal) | Si (single crystal) | Si (single crystal) | CdTe (polycrystal) | a-Se (amorphous) |
| **Pixel input-referred noise [$e^-_{rms}$]** | 68 (elec. only) | 212 (elec. only) | 60 (elec. only) | Not reported | 83 (w/ a-Se dark noise) |
| **RMS offset [$e^-_{rms}$]** | 164 | 7.5 | 9.4 | Not reported | 21 |
| **Min. detectable signal [$e^-_{rms}$]** | 290 | Not reported | Not reported | Not reported | 161 |
| **Power/pixel [µW]** | 4.6 | 45 | 37 | Not reported | 11 (2.75/sub) |
| **Count rate density [Mcps/$mm^2$]** | 138 (real photon) | 1200 (ROIC only) | 177 (ROIC only) | 50 (real photon) | 35 (real photon) |
| **SPE factor = $t_{sen}/d_{eff}$** | 2.0 | 1.2 | 1.6 | 0.53 | 2.6 |
| **SPE-enhanced rise time** [µs]** | 2.6 | 4.3 | 3.2 | 40 (no SPE) | 2.0 (measured) |

NOTE: Bottom two rows assume a-Se ($t_{sen}$=115µm) is deposited on the ROICs in other chips.
*For other chips in this table, $d_{eff} = d$ because these detectors do not employ sub-pixels.
**Predicted signal rise time, assuming rise time is linearly proportional to SPE factor.

## 6.6 Summary

We have demonstrated the first SPC pixel that uses an a-Se/CMOS ROIC. By exploiting SPE, we have achieved an energy resolution of 7.9 keV and a count-rate density of 35 Mcps/$mm^2$, making our pixel the first SPC detector that integrates an amorphous semiconductor sensor suitable for DBCT. To achieve these results, we designed a new area-efficient pixel architecture to employ SPE, which we call sub-pixel SPE enhancement, with a new partially-shared foreground input-offset-correction circuit. Our design also employs a new area-efficient current-steering calibration DAC. Our fabricated chip, designed using a 0.18 $\mu$m analog/mixed-signal CMOS process, contains two 5 × 8 pixel arrays. In conclusion, our design presents a promising approach for the development of advanced X-ray imaging systems with superior performance and functionality for DBCT.

# Chapter 7

# Asynchronous Sampling-Based Single-Photon-Counting Pixel with Adaptive-Leakage Compensation (Chip 4)

## 7.1 Introduction

In addition to the adaptive-resistive feedback SPC pixel, presented in Section 6.2.5, a sampling-based SPC pixel, proposed in [64], is another approach to address the trade-off between speed and charge-to-voltage efficiency in conventional pixels. In conventional pixels, a larger feedback resistor results in a higher charge-to-voltage ratio, but it also leads to a slower response time. However, the leakage current in SPC pixels decreases the energy resolution and may lead to saturation of the pixel. Leakage current originates from the dark current of the X-ray sensor, the resistive path between the sensing electrode and ground, and the off-current of the integration-capacitor reset switch.

In this chapter, we present a sampling-based SPC pixel with an adaptive-leakage-compensation circuit to mitigate the leakage current impact. In addition, we present an offset-cancellation circuit to correct the CSA offset and residue leakage impact. First, we present our adaptive-leakage compensation scheme and the proposed pixel architecture. Next, we show our simulation results to demonstrate the effectiveness of the proposed circuit in reducing the leakage current. Electronic verification results of the fabricated chip (Chip 4) confirm the functionality of the proposed pixel circuit.

## 7.2 Sampling-Based SPC Pixel

The sampling-based SPC pixel architecture proposed in [64] is shown in Figure 7.1(a). This architecture offers a solution to address the trade-off between charge-to-voltage gain and reset time in conventional pixels. Instead of utilizing a feedback resistor $R_f$ as in conventional pixels, shown in Figure 7.1(b), the CSA employs a switch SW1 to fully discharge integration capacitor $C_f$ (hard reset). Prior to sampling the charge packet, SW1 is momentarily closed to reset $C_f$. During the charge packet sampling phase, this switch is off, enabling the rapid conversion of the charge packet into output voltage without any loss. The output voltage remains at its peak value until it resets. Following the voltage pulse processing, SW1 is activated, initiating the reset period. This architecture also offers the feasibility of correlated-double-sampling (CDS) to the OTA offset prior to the start of photon detection. The timing diagram of hard reset with CDS is shown in Figure 7.1(c). The sampling-based pixel CSA output voltage for the pixel in [64] is compared to a conventional pixel with different $R_f$ values, highlighting the charge-to-voltage gain versus speed trade-off. The sampling-based pixel CSA response shows this trade-off does not impact the pixel.

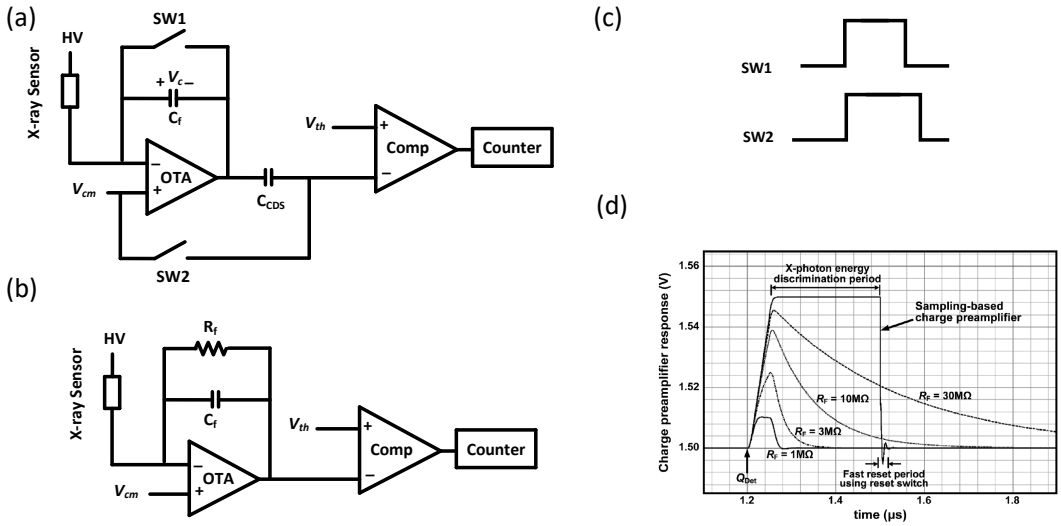



Figure 7.1: (a) Sampling-based SPC pixel with CDS offset cancellation. (b) Conventional SPC pixel. (c) The timing diagram of hard reset sampling-based SPC pixel. (d) Conventional pixel transient response vs. different $R_f$, along with the sampling-based pixel response. (adapted from [64]).

## 7.3 Leakage-Current Impact on Pixel Operation

Leakage current in sampling-based SPC pixels potentially decreases the energy resolution and may lead to saturation of the pixel. To explain this impact, we show a simplified SPC pixel in Figure 7.2(a), which incorporates a CSA, comparator, and digital counter. For simplicity, we assume an ideal sensor generates an impulse when a photon is absorbed by the pixel. If the only non-ideality in the pixel is a constant leakage current $I_{leak}$, as shown in Figure 7.2(b), $C_f$ voltage $V_c$ will increase linearly. Therefore, CSA output $V_{out}$ will increase with the same slope over time while the pixel is waiting for a photon. This will result in two main issues: (1) energy-resolution reduction and (2) CSA saturation.

The energy resolution of the pixel may be affected by the leakage current since the interpretation of photon-energy level by the comparator varies based on when the photon is absorbed. This variation arises because $V_{out}$ comprises both the photon-generated voltage

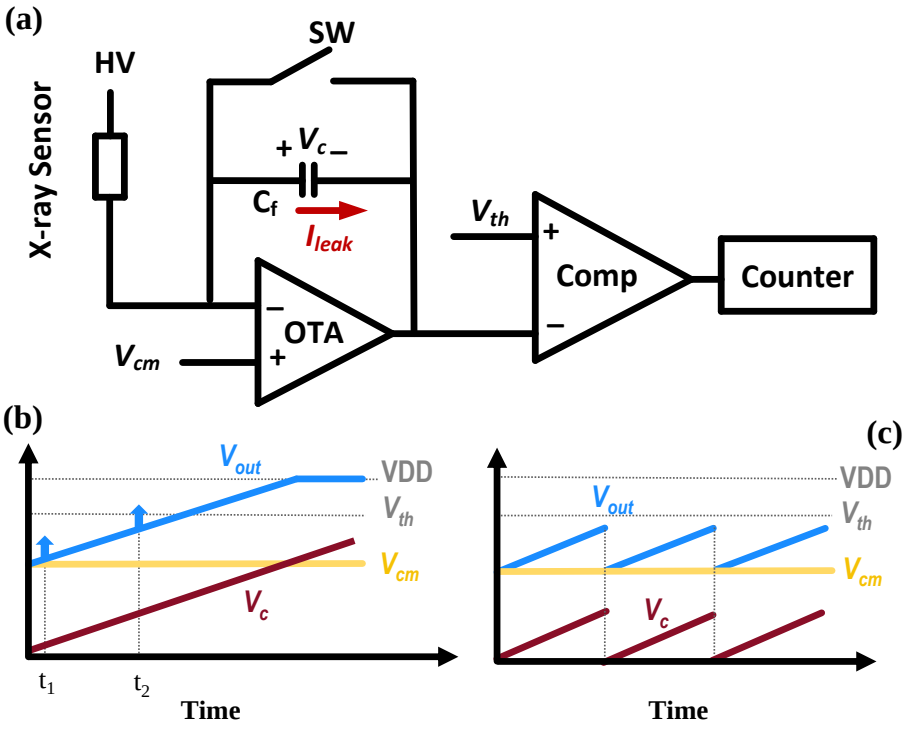



Figure 7.2: (a) SPC pixel circuit. (b) Leakage-current impact on asynchronous sampling-based SPC pixel. (c) Synchronous periodic resetting of the pixel used to overcome leakage-current impact.

and the CSA output dc voltage at the moment of photon arrival, as shown in Figure 7.2(b). If a low-energy photon generates a voltage less than $V_{th}$ when it hits the sensor at the time $t_1$, then the comparator will not toggle correctly because the voltage generated by the photon is less than $V_{th}$. However, when a photon with the same energy as the first one hits the sensor at $t_2$, it will toggle the comparator because of the additional charge stored on $C_f$ due to leakage. While the CSA saturation from the leakage current can be mitigated by periodically resetting $C_f$, as illustrated in 7.2(c), this approach does not address the degradation of energy resolution.

The leakage current is also an issue for conventional pixels. In conventional SPC pixels, the feedback resistor creates a path for the leakage current to flow. However, variations in the feedback resistor value lead to changes in the dc value of the CSA output across an array of pixels. An effective solution to compensate for the leakage impact has been proposed for use in conventional pixels, which employ a negative-feedback network to adjust the leakage current [112]. This technique has also been modified for use in conventional SPC X-ray imagers [113]. However, this method has its limitations that arise from adding extra parasitic capacitance and resistance to the integration node.

Compared to conventional pixels, the CDS offset-cancellation capability of the sampling-based architecture enables canceling any offset at the CSA output by leakage-current after resetting the capacitor upon photon arrival. Therefore, once pixel resets itself the leakage impact will be canceled out, as explained in [64]. However, this is ideal if photon hits the pixel again soon after reset, which is not always the case. Depending on when the photon arrives, the leakage impact at the CSA output will be different. In X-ray sensors with high dark current, this limits the pixel energy resolution, as explained above. We aim to investigate canceling this leakage-current impact by adaptively adjusting the common-mode voltage of the CSA, without loading the integration node, and implementing a dedicated CDS offset-cancellation technique, as presented next.

## 7.4 Chip Design

### 7.4.1 Leakage Compensation Scheme

To compensate for the effect of leakage current on sampling-based SPC pixel performance, we implement an adaptive-compensation technique. We aim to decrease the common-mode voltage $V_{cm\_new}$ at the same rate as leakage charges the integration capacitor, but with a negative slope. This way $V_{out}$ stays constant since it is equal to sum of $V_{cm\_new}$ and $V_c1$.

To implement adaptive common-mode adjustment, we add an auxiliary amplifier as shown in Figure 7.3.

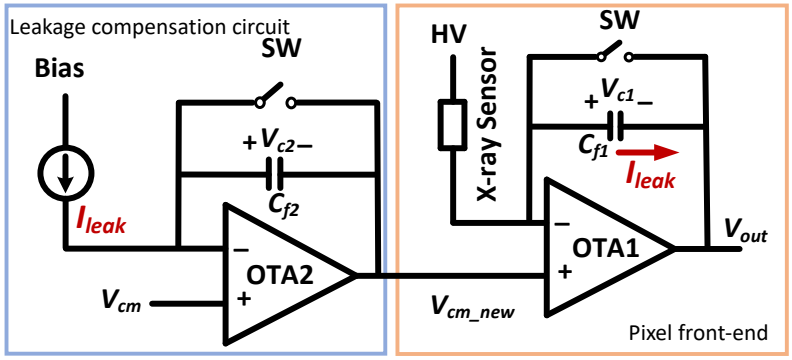



Figure 7.3: Simplified leakage-compensation circuit implementation.

To cancel out the leakage, we supply a constant current equal to $I_{leak}$ to the negative terminal of the OTA2, which charges the capacitor $C_{f2}$. As $C_{f2}$ charges, the output of the leakage-compensation circuit $V_{cm\_new}$ decreases compensating the increase in $V_{c1}$ due to $I_{leak}$, as shown in Figure 7.4.

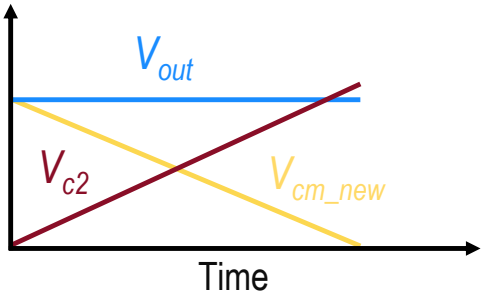



Figure 7.4: Adaptive-leakage compensation waveforms based on the circuit in Figure 7.3.

### 7.4.2 Input-Referred Offset-Cancellation Scheme

Input-referred offset also impacts the energy resolution of the pixel, as explained in the previous chapter. However, with adaptive-leakage-current compensation, the common-mode voltage of the CSA is changing over time. Therfore, in addition to input-referred offset, we must also take into account the differences between the common-mode voltage

generated by the leakage-compensation circuit $V_{cm\_new}$ at photon arrival time and the actual constant common-mode voltage $V_{cm}$ applied to the comparator. This arises when we reset the capacitor after processing the absorbed photon since the output becomes $V_{cm\_new}$, which is different than $V_{cm}$. Therefore, we implement a dedicated offset-cancellation scheme for our pixel, shown in Figure 7.5, that not only accounts for this difference, but also addresses random input offset of the CSA. The figure shows the implemented CSA, highlighting the two phases involved and the required non-overlapping switch control signals. Given the very short time required to complete these two phases, we ignore the leakage current. For simplicity, we do not include the representation of the X-ray sensor and its associated leakage. Additionally, we assume that no photo is absorbed by the sensor during the offset cancellation phase.

The input-referred offset also impacts the energy resolution of the pixel, as explained in the previous chapter. However, with adaptive-leakage-current compensation, the common-mode voltage of the CSA changes over time. Therefore, at photon arrival time, in addition to the input-referred offset, we must also take into account the differences between the common-mode voltage generated by the leakage-compensation circuit $V_{cm_new}$ and the actual constant common-mode voltage $V_{cm}$ applied to the comparator. This arises when we reset the capacitor after processing the absorbed photon since the output becomes $V_{cm\_new}$, which is different than $V_{cm}$. Consequently, we implement a dedicated offset-cancellation scheme for our pixel, depicted in Figure 7.5, that not only considers this difference but also addresses the random input offset of the CSA. The figure illustrates the implemented CSA, highlighting the two phases involved and the required non-overlapping switch control signals. Given the very short time required to complete these two phases, we ignore the leakage current during this time. For simplicity, we do not include the representation of the X-ray sensor and its associated leakage. Additionally, we assume that no photons are absorbed by the sensor during the offset cancellation phase.

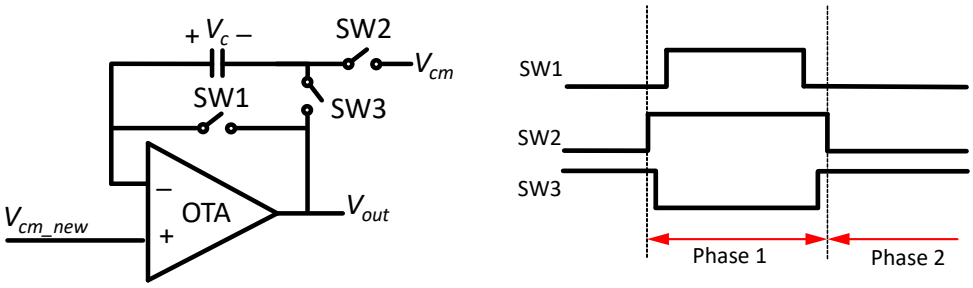



Figure 7.5: Offset-cancellation implementation.

Phase 1 is the sampling phase, where both the input-referred offset of the OTA and the difference between $V_{cm\_new}$ and $V_{cm}$ is stored in the integration capacitor to be corrected in the next phase. Figure 7.6(a) shows the switch configuration where SW1 and SW2 are closed and SW3 is open. Phase 2 is the integration phase, where the sampled voltage is subtracted at the output, ideally leading to $V_{out} = V_{cm}$. In this phase, the pixel is ready for photon arrival. Figure 7.6(a) shows the switch configuration in Phase 2 where SW1 and SW2 are open and SW3 is closed.

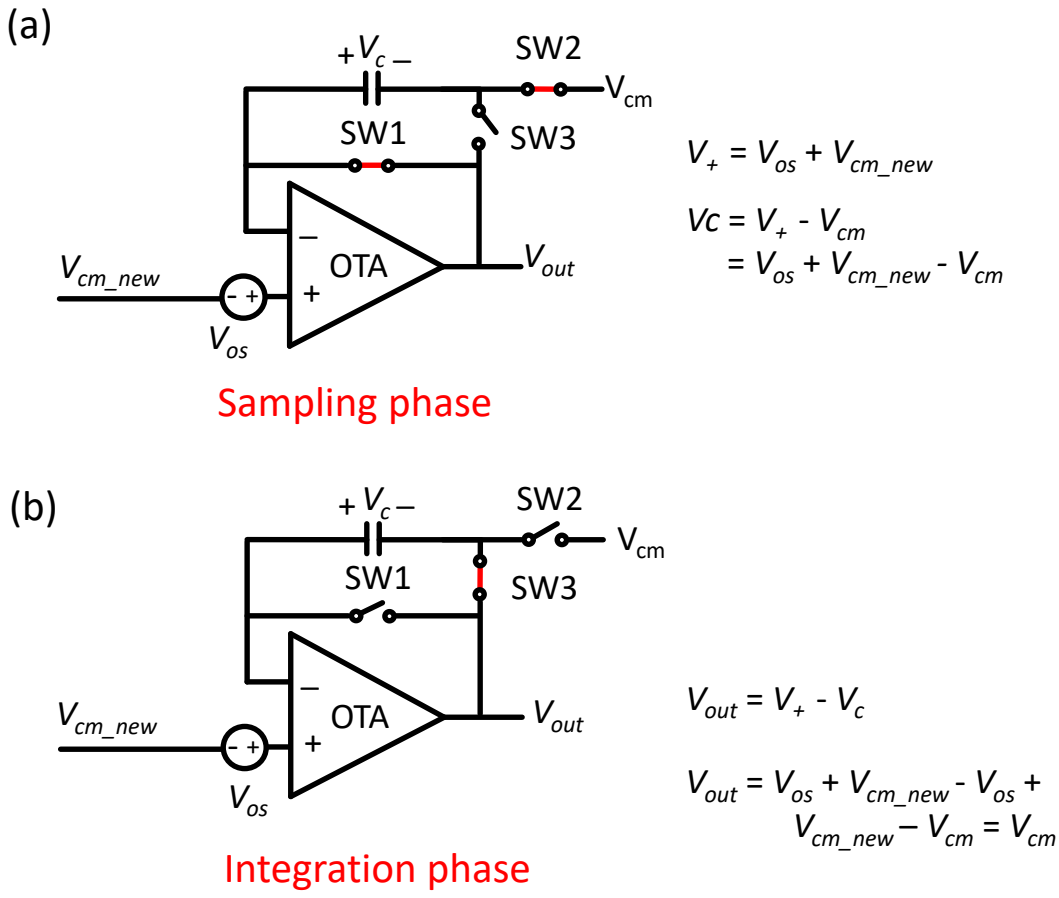



Figure 7.6: Offset-cancellation scheme: (a) Sampling phase. (b) Integration phase.

### 7.4.3 Pixel Design

We have designed and implemented a complete pixel incorporating the leakage-compensation and offset-correction circuit. Our design includes the CSA from Chip 2 and the comparator from Chip 3. Figure 7.7 shows the complete pixel circuit.

In order to generate the non-overlapping pulses required to implement our proposed offset-correction scheme, we incorporate a pulse-generation circuit that is activated either when a photon is absorbed or when the pixel is reset asynchronously. This pulse-generation block is implemented using a series of current-starved delay cells with configurable delay time. The detailed implementation of our pulse-generation circuit is also shown in Figure 7.7. The pulse-generation circuit outputs are SW1, SW2, and SW3 to configure the sampling and offset-correction/photon-integration phase.

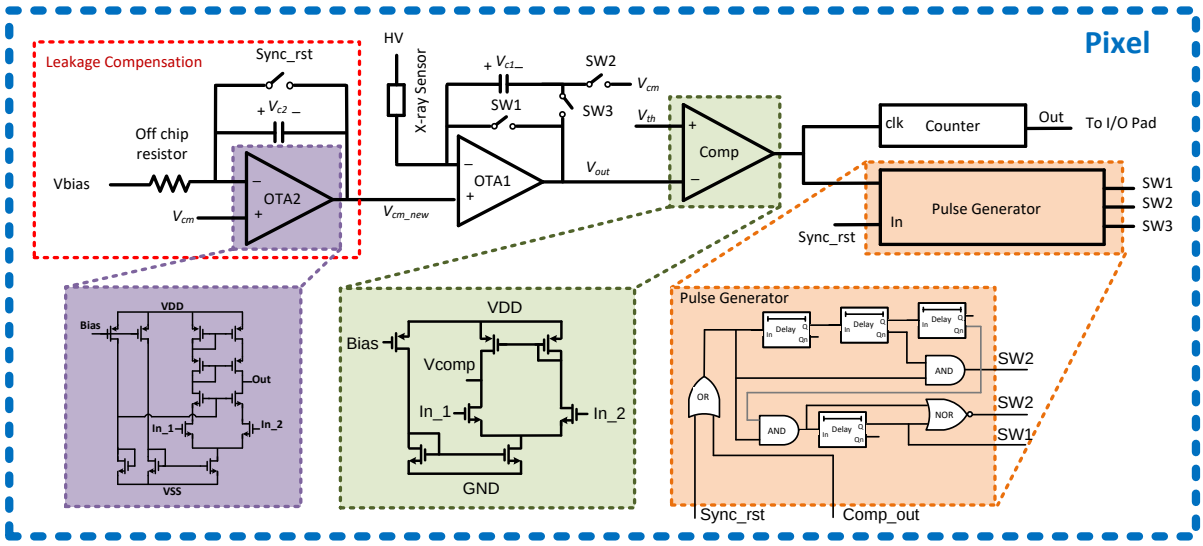



Figure 7.7: Proposed pixel circuit.

### 7.4.4 Physical Design and Fabrication

We now present physical implementation of the designed pixel, which is fabricated as part of Chip 4. The layout of each block and fabricated blocks with an array of 4 × 8 test pixels are shown in Figure 7.8. Figure 7.8(a) displays the layout of the analog buffer, which occupies a 112 × 250-$\mu$m$^2$ area. Figure 7.8(b) presents the layout of the comparator and

Figure 7.8(c) shows the CSA layout. The layout of the pulse-generation circuit is shown in Figure 7.8(d), which is a series of current-starved delay cells with delay control.

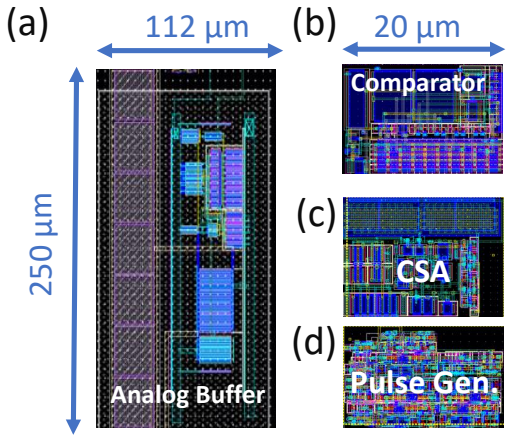



Figure 7.8: Layout of various pixel bloks: (a) analog buffer, (b) comparator, (c) CSA, and (d) pulse-generation circuit.

Chip 4 is designed using a 0.18-$\mu$m analog/mixed-signal one-poly six-metal CMOS process and occupies an area of 2 $\times$ 3 mm$^2$. Figure 7.9 shows a micrograph of the fabricated chip and highlights the area occupied by our sampling-based pixels with leakage-compensation circuits.

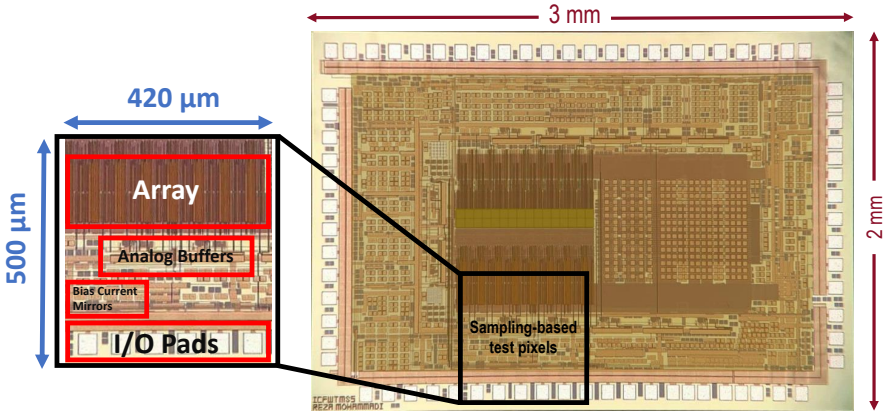



Figure 7.9: Micrograph of fabricated Chip 4 showing the 4 $\times$ 8 array of test pixels.

## 7.5 Simulated and Experimental Results

We now present post-layout simulation results along with measured electronic characterization results from our fabricated chip. Post-layout pixel operation is shown in Figure 7.10, where we apply a 10-pA leakage current from an a-Se sensor. The output of the CSA with and without the proposed leakage-cancellation technique is demonstrated in the figure. The CSA output in black represents the output with both leakage and OTA saturation issues. The red plot demonstrates the CSA output with the saturation resolved by implementing an asynchronous external reset. Finally, the blue plot shows the simulation results with the leakage effectively canceled and the CSA avoiding saturation with a pre-defined asynchronous reset. The output of the pixel stays constant with the leakage-compensation circuit.

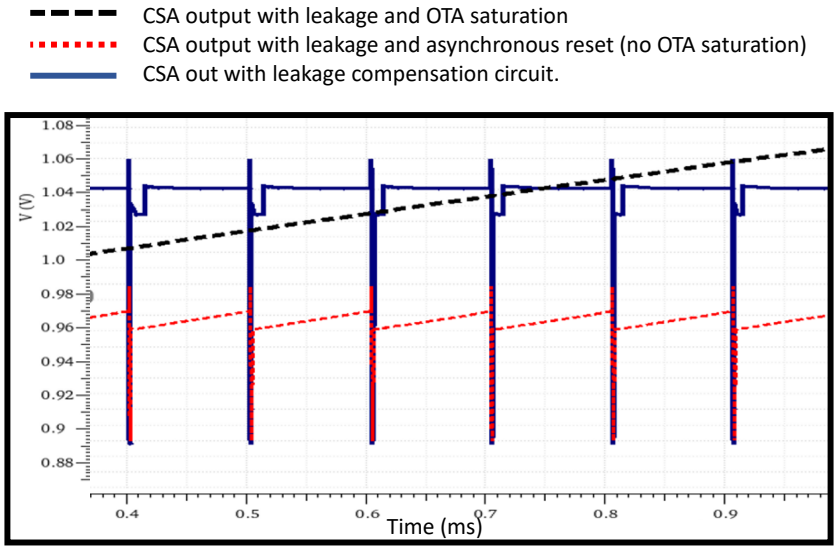
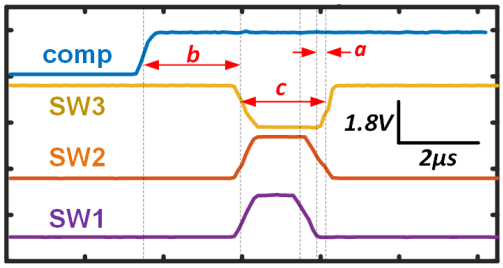



Figure 7.10: Simulated pixel output with and without leakage compensation.

Figure 7.11(a) displays the measured non-overlapping output signals from our pulse-generation circuit. We apply different bias voltages to the current-starved delay cells to control the pulse-width and non-overlapping times between the signals. The table in Figure 7.11(b) provides the maximum and minimum values for each phase pulse width and delay time between each phase, ensuring non-overlapping conditions. These values are measured for test and characterization purposes.

(a)




(b)

| | Min | Max |
|---|---|---|
| a | 72 ns | 3.96 µs |
| b | 270 ns | 78 µs |
| c | 1.9 µs | 18 ms |

Figure 7.11: (a) Measured non-overlapping pulses from pulse-generation circuit. (b) Maximum and minimum measured pulse width and delays while maintaining non-overlapping.

A normalized histogram of measured pixel CSA output voltage after being reset at the beginning of the integration phase, with offset correction applied, is shown in Figure 7.12. The measured mean and standard deviation of the output voltage is 906 mV and 2.1 mV, respectively.

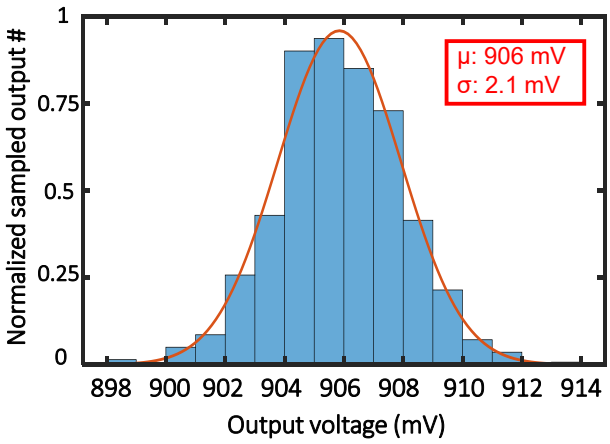



Figure 7.12: Measured CSA sampled output voltage histogram after offset correction.

We have also measured the CSA output slope to demonstrate the effectiveness of the leakage-compensation circuit, as shown in Figure 7.13 for 15 pixels. The average slope is 1.2 mV/$\mu$s with a 0.35-mV/$\mu$s standard deviation.

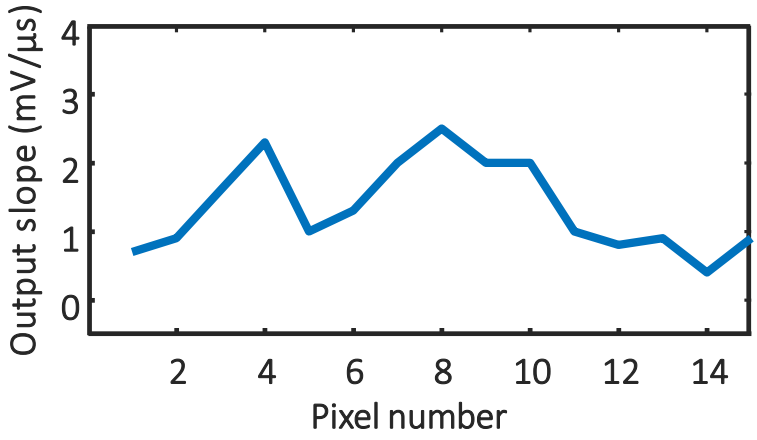



Figure 7.13: Measured CSA output slope after leakage compensation for 15 pixels.

Finally, Figure 7.14 shows the CSA transient response for leakage-compensated and non-compensated cases, along with simulated results. Without leakage compensation, the leakage current reduces the output with a large slope of 160 mV/$\mu$s. With the compensation circuit, the leakage can be completely corrected, leading to zero slope at the CSA output. However, the measured slope at the output is compensated to be around 0.8 mV/$\mu$s, which is a improvement of approximately 200×.

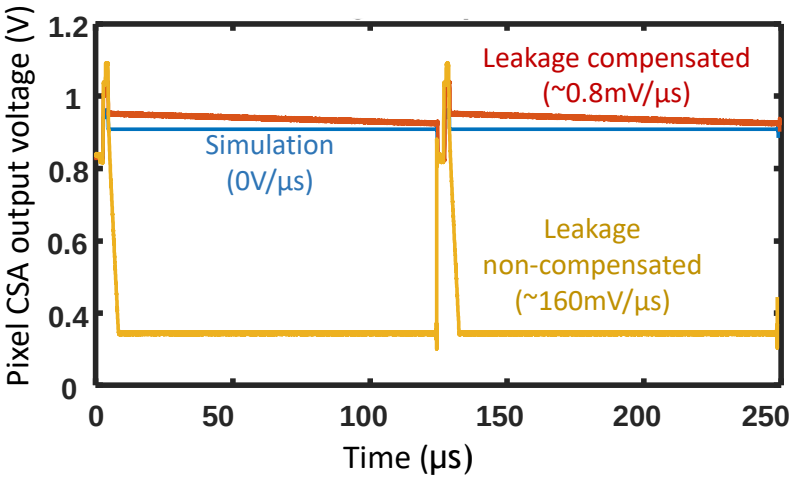



Figure 7.14: Measured pixel CSA output voltage transient response.

## 7.6 Summary

In this chapter, we presented a sampling-based photon-counting pixel (Chip 4) incorporating an adaptive common-mode leakage-compensation circuit and front-end offset correction to further improve pixel maximum count rate. Our simulation and measured results demonstrated the effectiveness of the proposed technique.

# Chapter 8

# Summary and Contributions

In this work, we investigated the feasibility of developing cost-effective large-area-scalable SPC imagers to meet the requirements for DBCT. By integrating a-Se, a well-established X-ray-sensitive amorphous material, of a-Se onto our custom-designed CMOS ROICs, and by tackling the inherent weaknesses, we provided a practical alternative to dominant polycrystalline-based sensors for SPCs. We achieved several experimental milestones and introduced new circuit designs to reach our objectives.

We presented the first X-ray SPC imager with an amorphous semiconductor as the X-ray sensor. This allows large-area scalability with a simple thermal-evaporation process, but without the need for expensive low-yield bump bonding. We experimentally demonstrated single-photon-counting feasibility using a-Se integrated on a CMOS ROIC as the first step to achieve our objectives. In our next step, we presented the first measured transient response and PHS results from a-Se monolithically integrated on a CMOS ROIC. We designed our Chip 2 for this purpose which was necessary to investigate the temporal and energy resolution of a-Se-based CMOS X-ray sensors and to study their limitations to meet DBCT requirements.

After demonstrating the limitations of conventional a-Se/CMOS SPC imagers, we experimentally demonstrated the impact of SPE on the performance of monolithic a-Se/CMOS detectors, for the first time. This was essential to demonstrating how SPE can dramatically enhance the intrinsic performance limitations of a-Se for DBCT.

In our next step, we designed Chip 3 with SPC pixels to meet demanding DBCT requirements. We experimentally presented the feasibility of energy-discriminating single-photon counting results with an a-Se/CMOS detector and showed that our imager can satisfy the requirements for DBCT.

At the circuit level, we designed a pixel ROIC with the lowest reported electronic noise and highest reported ROIC bandwidth for a-Se/CMOS imagers (Chip 2). Using our Chip 3, we introduced sub-pixel SPE-enhancement that enables large-area scalable SPC a-Se/CMOS pixel which can benefit from SPE. We also designed and fabricated an SPC pixel with a new re-configurable area-efficient foreground input-offset-correction circuit. In addition, we proposed a new reduced-area current-steering calibration DAC for foreground input-offset correction circuits in SPC pixels. Our imager has the lowest reported pixel size for DBCT application enabling better visualization of breast cancer.

Lastly, using our Chip 4, we proposed an SPC pixel with an adaptive leakage compensation circuit, to further improve the performance of SPC X-ray imagers by reducing the deteriorating impact of leakage on the energy resolution of the imager.

## 8.1 Future Work

The following advances could be investigated to fully realize the potential of achieving low-cost large-area-scalable SPC imagers for high-performance medical imaging applications:

1. Further experiments would be beneficial in studying the full potential of SPE and its impact on a-Se/CMOS imagers. The impact of charge sharing and cross-talk on SPE could be investigated with more extensive and detailed experiments.

2. Imagers with large arrays based on our proposed pixel can be designed and fabricated to perform real imaging of breast tissue samples using an X-ray source. Image performance metrics such as contrast, MTF, etc. could then be investigated.

3. Designing our sub-pixel SPE-enhancement technique with more advanced technologies would allow for a higher number of sub-pixels with smaller sub-pixel sizes. This would lead to better energy and temporal resolution due to the higher SPE-factor.

4. Implementing pixels with a greater a-Se sensor thickness could be investigated to achieve higher SPE-factor to further benefit from SPE.

5. Our sub-pixel SPE-enhancement technique can adapt to other digital pixel typologies. This architecture would be beneficial even when used with dominant polycrystalline sensors to help improve their performance. The number of sub-pixels and the sub-pixel size will be determined by the application, X-ray sensor material and its thickness, pixel functionality, and the CMOS technology node.

6. Our proposed reduced-area DAC and foreground input-offset calibration circuit is not limited to SPC pixels and could be employed in calibration circuits for other applications.

## 8.2 Publications

We published or are submitting for review the following articles based on this thesis:

1. R. Mohammadi, P. M. Levine, and K. S. Karim, " Near-Field-Effect Enables Monolithic-CMOS-Integrated Amorphous-Semiconductor to Realize Large-Area-Scalable X-Ray Quantum Sensor," *In preparation for submission.*

2. R. Mohammadi, P. M. Levine, and K. S. Karim, " Monolithically-Integrated Scalable Amorphous-Selenium/CMOS X-Ray-Energy-Discriminating Single-Photon-Counting Pixel with Sub-Pixel Small-Pixel-Effect-Enhancement," *In preparation for submission to IEEE Journal of Solid-State Circuits (JSSC).*

3. R. Mohammadi, P. M. Levine, and K. S. Karim, "A monolithic amorphousselenium/cmos small-pixel-effect-enhanced X-ray-energy-discriminating quantumcounting pixel for biomedical imaging," *in proceedings of the 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, pp. 1–2, 2023.

4. R. Mohammadi, P. M. Levine, and K. S. Karim, "Experimental demonstration of the small pixel effect in an amorphous photoconductor using a monolithic spectral single photon counting capable cmos-integrated amorphous-selenium sensor", *in proceedings of the 2022 International Electron Devices Meeting (IEDM)*, pp. 467–470, 2022.

5. A. El-Falou, A. Camilca, R. Mohammadi, P. M. Levine and K. S. Karim, "A Monolithic Amorphous-Selenium/CMOS Single-Photon-Counting X-Ray Detector," *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 1746-1752, April 2021, doi: 10.1109/TED.2021.3063073.

6. A. El-Falou, A. Camilca, R. Mohammadi, P. M. Levine, and K. S. Karim, "CMOS-Integrated Single-Photon Counting X-Ray Detector using an Amorphous-Selenium Photoconductor with $11 \times 11$ m$^2$ Pixels," *2018 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2018, pp. 32.5.1-32.5.4.

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