Improved Control and Stability Analysis of a Microgrid Connector Controller Under Unbalanced Network Conditions

Hanwen Gu, *Student Member, IEEE,* Behnam Tamimi, *Senior Member, IEEE,* and Claudio A. Cañizares, *Fellow, IEEE*

***Abstract*—The microgrid connector controller has been shown to be a more cost-effective alternative for a microgrid-grid interface than a back-to-back connector. This paper proposes an improved control system for this controller under unbalanced operation, as distribution feeder and microgrid loads are normally unbalanced. The controller regulates the utility interface while minimizing the impact of load unbalancing on both the utility feeder and the microgrid. An improved reference current generation strategy is designed to suppress the fluctuations of the dc link voltage, thereby preventing them from being introduced into the control system and affecting the controller operation. Furthermore, a four-stage start-up strategy is proposed to avoid an external dc source for charging the controller's dc link capacitor, making the interface more practical and cost-effective. The paper also presents a comprehensive investigation of the effects of the controller parameters and microgrid load unbalance on the small-perturbation stability of grid-connected microgrids. The performance of the presented controller is compared with its original controls, a back-to-back with existing unbalance control techniques, and a switch interface through detailed simulations in a benchmark test system. The results illustrate that the proposed controls can minimize the impact of feeder and microgrid unbalancing by eliminating the negative-sequence components and reducing the fluctuations in the transferred powers and dc link voltage, showing similar overall performance to a back-to-back interface.**

***Index Terms*—Active Distribution Network (ADN), Back-to-Back (B2B), grid interface, Microgrid Connector Controller (MGCC), small-perturbation stability, unbalanced grids.**

GLOSSARY

ADN	Active Distribution Network
B2B	Back-to-Back
BPSC	Balanced Positive-Sequence Control
DDSRF	Decoupled Double Synchronous Reference Frame
DG	Distributed Generator
IARC	Instantaneous Active-Reactive Control
MG	Microgrid
MGCC	Microgrid Connector Controller
PI	Proportional-Integral
PLL	Phase-Lock Loop
PNSC	Positive-Negative-Sequence Compensation
RCG	Reference Current Generation
SG	Synchronous Generator
SOGI	Second-Order Generalized Integrator
SRF	Synchronous Reference Frame
TDS	Time-Domain Simulation
VSC	Voltage Source Converter

H. W. Gu is with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: guhanwen@stu.xjtu.edu.cn).

B. Tamimi and C. A. Cañizares are with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada, N2L 3G1 (e-mail: behnam.tamimi@uwaterloo.ca; ccanizares@uwaterloo.ca).

I. INTRODUCTION

MICROGRIDS (MGs) are a group of Distributed Generators (DGs), energy storage systems, and controllable loads that act as a single controllable entity with respect to the grid [1]. MGs have both grid-connected and islanded modes [2]. A grid-connected MG should be capable of connecting and disconnecting from the main grid with a seamless transition, enabling it to operate grid-connected or intentionally islanded [3]. Thus, a flexible, cost-effective, and reliable interface for providing a controllable connection of MGs to the utility is essential in the context of modern Active Distribution Networks (ADNs).

Unlike conventional power systems, load imbalance is commonplace in ADNs and MGs, which can reach 100% difference in phase currents, causing significant negative and zero-sequence voltage and current components [4]. The grid-microgrid interface operating under such conditions may impact the power quality of the ADN and MG, as well as the system stability when transitioning between grid-connected and islanded modes [3]. Hence, unbalanced operation techniques are required to minimize the impact of the MG imbalance on the utility, and vice versa.

Different means for connecting two networks with controlled power transfer capability have been proposed and studied, in particular, Back-to-back (B2B) and Microgrid Connector Controller (MGCC) interfaces [5]. A B2B interconnection is considered the standard for grid-microgrid interfacing, as it can asynchronously connect the ADN and MG and control the transferred powers [6]. The effects of the pulse-width modulation carrier signal synchronization on the dc link current in the B2B interface is analyzed in [7], demonstrating the relevance of proper synchronization of the Voltage Source Converters' (VSCs') carrier signals. In [8], the authors present the analysis and control design of a B2B interface using a multivariable approach. Several common-mode voltage reduction strategies are presented in [9] and [10] for B2B unbalanced operations. However, a B2B connection requires a sizable capital investment due to the relative high voltage

ratings of its elements [11]. Hence, a flexible and economical alternative to the B2B interface is proposed in [12], namely the MGCC, which can provide similar overall performance to B2B but at a fraction of its capital cost. However, the unbalanced operation of the MGCC has not been considered, which is an issue in MGCC practical implementations. Furthermore, the initial charging process of the dc link is not discussed in [12], and a stability analysis of the MGCC system is missing, which are issues addressed in the present paper.

The technical literature on control strategies for VSCs operating under unbalanced network conditions is extensive, focusing on Phase-Lock Loop (PLL), current controller, and various Reference Current Generation (RCG) strategies, which are all considered in this paper and discussed in detail next. Regarding PLL-based approaches, since Synchronous Reference Frame (SRF) PLLs cannot achieve accurate phase-locking when grid voltages are distorted due to significant steady-state oscillations, a common strategy has been proposed to address this issue that involves adding a pre-filter at the front stage of the SRF PLL [13], such as Decoupled Double Synchronous Reference Frame (DDSRF) PLL, Second-Order Generalized Integrator (SOGI) PLL, delayed signal cancellation PLL, and a moving average filter PLL. The DDSRF PLL is considered a standard for unbalanced grid synchronization, as it accurately extracts positive and negative-sequence components through DDSRF transformations and a decoupling approach [14]. The SOGI PLL generates quadrature signals with a 90-degree phase angle difference, facilitating phase sequence separation and phase-locking. Enhancements such as incorporating a frequency-locked loop with frequency-adaptive links are introduced in [15] and [16] to improve dynamic responses during sudden frequency and phase changes. Delayed signal cancellation filters have also been proposed, offering rapid dynamic responses while eliminating harmonics; these filters are integrated in-loop components within PLLs, as proposed in [17], enhancing the performances of the single-phase and two-phase enhanced PLLs. In [18], the authors use an SOGI after the adaptive cascaded delayed signal cancellation unit to improve the transient profile of frequency response. Furthermore, moving average filters based on linear-phase finite-impulse-response filters have been suggested to effectively block harmonics generated by unbalancing [19]. Finally, a variable window size moving average filter, adaptable based on the dominant frequency of oscillations in the dq frame, is proposed in [20] to improve dynamic response when integrated with SRF PLLs.

Current control strategies to manage unbalancing operation are predominantly based on a Proportional-Integral (PI)-based unbalanced current controller in the SRF [21], or a proportional-resonant-based current controller in the stationary reference frame [22]. The performances of these controllers are compared and discussed in [23], demonstrating that PI-based unbalanced current controllers have a straightforward implementation and satisfactory response. On the other hand, a PLL-free current controller is proposed in [24], wherein synchronous signals are generated directly using two standard second-order bandpass filters, eliminating the need for a PLL. Comparative studies between PLL-based and PLL-free current controllers under distorted grid conditions are presented in [25], showing that the filters employed in PLL-free controllers introduce dynamics similar to those of PLLs; however, it is mentioned that a well-designed PLL-based current controller should be the preferred choice. In this context, integrating the PLL into the current control loop, as proposed in [26], has been shown to substantially enhance system performance under weak grid conditions [27]. Building on this concept, a robust PLL-integrated controller in the stationary frame is developed in [28] to improve VSC performance under unbalanced grid conditions.

For RCG strategies, the Instantaneous Active-Reactive Control (IARC) has been adopted in converters under balanced conditions [29]; however, negative-sequence components introduce high-order harmonics in the reference currents in this case. In this context, several RCG strategies more suitable for unbalanced operation are presented in [30], of which the two most widely adopted are Balanced Positive-Sequence Control (BPSC) and Positive-Negative-Sequence Compensation (PNSC). The BPSC implements a sinusoidal current injection using only the balanced positive-sequence currents, but it does not eliminate power oscillations; on the other hand, the PNSC eliminates the double-frequency fluctuations of the transferred active power. Based on the PNSC, a novel RCG strategy is presented in [31] for asymmetrical fault control, where a direct method is introduced to calculate power references and controller gains, ensuring compliance with converter current limitations while adhering to next-generation grid code requirements. Since the MGCC introduced in [12] does not consider unbalanced operation, improved controls based on both BPSC and PNSC techniques are proposed here for the MGCC to minimize the impact of ADN and MG unbalancing for grid-connected operation.

Small-perturbation stability studies for converter controls have been extensively discussed in the literature, mainly based on eigenvalue analyses of the system state-space model in the dq frame [32]. These models are limited to balanced network conditions with time-invariant operating points that can be transformed to the dq frame. However, unbalanced operation produces time-periodic equilibria that do not allow applying classical dq-based eigen-analysis techniques [33]. To address this, multiple-frequency models such as harmonic state-space and Floquet models, have been developed to capture frequency-coupling terms, making them more suitable for small-perturbation stability studies of unbalanced conditions [34]. However, these model-based approaches are dependent on the modeling details, which can be rather complex and unrealistic for practical ADN applications. In this context, several modal estimation approaches, particularly the Prony method and the Steiglitz-McBride iteration method [35], have been proposed to extract information on the system oscillatory modes based on Time-Domain Simulations (TDSs), which are effective for studying small-perturbation stability in MGs [3]. Hence, the Prony method is used here for the small-perturbation stability analysis of the MGCC system.

Based on the aforementioned discussion, the main contributions of the present work are:

- The design of a control system for the MGCC to improve

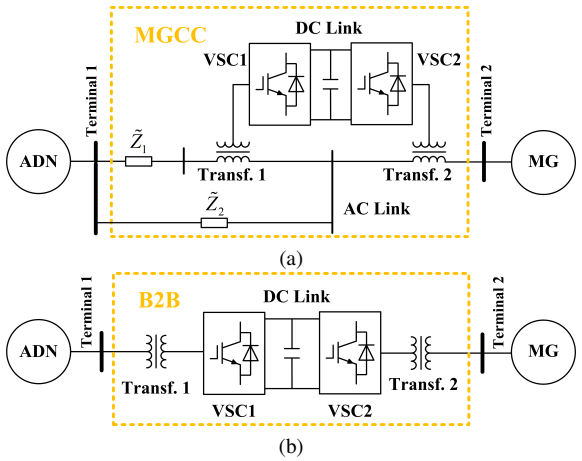


Fig. 1. Architecture of (a) MGCC and (b) B2B MG interfaces [12].

its operation under unbalanced ADN and MG conditions.
- An improved PNSC strategy for the MGCC to minimize oscillations of the dc link voltage.
- A practical four-stage start-up strategy without an external dc source for the MGCC.
- An investigation of the effects of MGCC control parameters and MG load unbalance based on small-perturbation stability studies using the Prony method.

The rest of the paper is organized as follows: Section II reviews the architecture, power flow analysis, and original controls of the MGCC. Section III presents the improved MGCC controls along with the proposed dc link start-up strategy, as well as the TDS models used to evaluate the performance and small-perturbation stability of the proposed controls. Section IV presents and discusses the results of applying the proposed start-up strategy and the improved MGCC controls to a benchmark test system. Finally, Section V highlights the contributions and conclusions of the paper.

II. Background

A. MGCC Architecture

Fig. 1 shows the circuit topologies of the MGCC and B2B used as ADN-MG interfaces [12]. Observe that the MGCC provides both ac and dc paths for the power to flow between the two terminals, while the B2B only has the DC Link. In addition, the low-value $\widetilde{Z_2}$ branch forces most of the power to flow through the AC Link instead of the DC Link, thus reducing the power ratings of the VSCs, transformers, and other passive elements. On the other hand, the converters' voltage ratings for a B2B are approximately the line voltage of the utility and MG. Hence, due to the series nature of the MGCC, the input voltages of the converters correspond approximately to the voltage difference between the two connection terminals which is a fraction of the line voltage. Consequently, the voltage ratings of the components in an MGCC are significantly lower than those in a B2B, making the former more economical, as discussed in detail in [12]. Furthermore, the reduced ratings translate into significantly smaller physical dimensions, making the deployment logistics simpler and cheaper. Finally, with the appropriate selection of components and control parameters, both interfaces could be readily scaled up or down to meet any voltage and power level requirement, as discussed in [36].

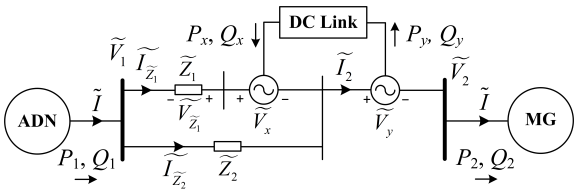


Fig. 2. Equivalent phasor circuit of the MGCC.

Observe that the MGCC topology, as discussed in detail in [12] and [36], employs a three-phase three-wire configuration on the two series-connected VSCs of the MGCC, and thus the neutrals of the grid and the microgrid are isolated. This design and its associated control strategies remain consistent regardless of whether the grid operates as a three-phase three-wire or a three-phase four-wire system. Hence, the proposed control strategy can be directly applied to three-phase four-wire systems without any modification.

B. MGCC Power Flow Analysis and Limitations

Fig. 2 shows the equivalent circuit of the MGCC, where the phasors $\widetilde{V_1}$ and $\widetilde{V_2}$ are the connection terminals' voltages, and P_1, Q_1, P_2, and Q_2 represent the powers flowing in and out of the MGCC, respectively. P_x and Q_x are the powers flowing out of the VSC1 from the DC Link, and P_y and Q_y are the powers injected into the VSC2. As discussed in [12], for the MGCC to work properly, $\widetilde{Z_2}$ should be small. Hence, $\widetilde{V_x} \approx \widetilde{V_{Z_1}}$, and thus the active power of $\widetilde{Z_1}$ is closed to P_x. The power balances of the MGCC can then be shown to be:

$$\begin{aligned} P_x &\approx P_{\widetilde{Z_1}} > 0 \\ P_y &\approx P_{loss_{VSCs}} + P_x \\ P_{loss_{MGCC}} &= P_1 - P_2 \approx P_y \end{aligned} \tag{1}$$

where $P_{loss_{MGCC}}$ stands for the power losses of the interface, which is the sum of $P_{\widetilde{Z_1}}$ and the $P_{loss_{VSCs}}$ representing the power losses of the converters along with their transformers. Accordingly, $P_y > P_{loss_{VSCs}} > 0$ is an operational limitation of the MGCC that requires the setpoints to be chosen appropriately based on the power flow calculation. Thus, $P_2 = Q_2 = 0$ is not feasible for this controller, unlike the case of a B2B.

It is important to add that inaccuracies in the power flow calculations can lead to the selection of setpoints that fail to meet the aforementioned MGCC's operational constraints, resulting in controller instability. These setpoints must be determined offline as part of the MGCC implementation and set up, and cannot be accomplished online by monitoring system variables in real time.

C. MGCC Controls Overview

The MGCC's overall control system is explained in detail in [12]. Thus, an SRF PLL is used to track the voltage of the utility terminal, with its output being an input for the dq transformations. A typical vector-current controller

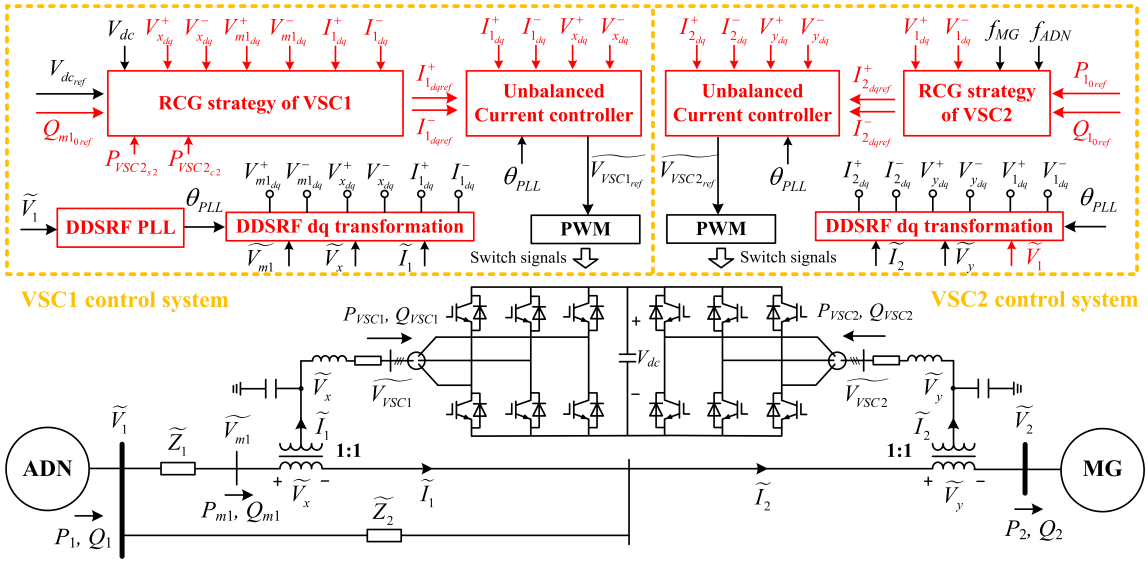


Fig. 3. Improved MGCC control system.

composed of the current controller and an RCG strategy is chosen for active and reactive power controls. The current controller is a closed-loop system in which PI controllers are used to generate the desired output voltages for the VSC pulse-width modulation control. For the RCG, VSC1 uses an IARC strategy with an additional PI-based dc voltage controller to provide a smooth DC Link voltage. Note that due to the direct connection of the two terminals through the AC Link, the MG frequency must be fast-synched with the ADN after any disturbance; thus, the IARC strategy with an auxiliary frequency control is chosen for the VSC2 to regulate the powers injected into the MG.

III. MGCC Improved Controls

Load imbalance is commonplace in MG operation, which is reflected on the ADN side through the MGCC AC Link, affecting power quality for the original controls proposed in [12], since negative-sequence voltages and currents introduce multi-frequency components into the transferred powers and DC Link voltage. Thus, a control system is proposed here to improve MGCC operation under unbalanced conditions, which compared to [12], controls the powers on the grid side instead of the MG side, which is more practical in the context of ADN operation. Furthermore, it is assumed in [12] that the DC Link is initialized by an external dc source, which would affect the reliability and cost efficiency of the MGCC in practice. Thus, a start-up strategy without an external source is proposed here for the initial charging of the DC Link capacitor.

Fig. 3 depicts the overall structure of the proposed MGCC control system, where the improvements compared with the original control are marked in red. The DDSRF PLL, unbalanced current controller, RCG strategies for the two converters, and the start-up procedure are discussed next.

A. DDSRF PLL

If the network voltage is unbalanced, the positive-sequence voltage detected using an SRF PLL is distorted due to the double-frequency component. Although this issue can be addressed by reducing the bandwidth of the SRF PLL, the dynamic response of the system is significantly affected. Thus, the DDSRF PLL from [14] is adopted here to eliminate the detection errors of the SRF PLL, with the positive and negative-sequence components being accurately extracted by the double synchronous frame transformations and a decoupling approach. A low-pass filter is used to remove the oscillations introduced by the harmonic components; however, the signal before filtering is used as the PLL input to improve its dynamic response.

B. Unbalanced Current Control

The unbalanced current controller from [21] is used here to control the unbalanced current vector consisting of positive and negative-sequence components, i.e., I_d^+, I_q^+, I_d^-, and I_q^-. Two decoupled closed-loop systems are used to regulate positive and negative currents, respectively. The differences between the references and measured values feed PI controllers to generate the desired output voltages. The time constant of the controller should be small enough to provide a fast current-control response, but not too small to ensure its reciprocal is smaller than the switching frequency [12].

C. Improved RCG Strategies

The RCG strategies are designed to provide the current references for the current controller. Under unbalanced conditions, the current references are commonly calculated based on the instantaneous powers at the PCC, as follows:

$$\begin{aligned} P &= P_0 + P_{s2}\sin(2\omega t) + P_{c2}\cos(2\omega t) \\ Q &= Q_0 + Q_{s2}\sin(2\omega t) + Q_{c2}\cos(2\omega t) \end{aligned} \tag{2}$$

where subscripts 0, $s2$, and $c2$ denote the steady-state and sine and cosine double-frequency components of the powers,

respectively, which can be expressed as:

$$\begin{bmatrix} P_0 \\ Q_0 \\ P_{s2} \\ P_{c2} \\ Q_{s2} \\ Q_{c2} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_q^- & -V_d^- & -V_q^+ & V_d^+ \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ -V_d^- & -V_q^- & V_d^+ & V_q^+ \\ V_q^- & -V_d^- & V_q^+ & -V_d^+ \end{bmatrix} \begin{bmatrix} I_d^+ \\ I_q^+ \\ I_d^- \\ I_q^- \end{bmatrix} \tag{3}$$

Observe in (3) that there are four degrees of freedom for the controlled current vector, i.e., I_d^+, I_q^+, I_d^-, and I_q^-; thus, the four current references can be generated based on different individual control targets. It is worth noting that it is not possible to eliminate the negative-sequence current and the oscillations in the powers and the DC Link voltage simultaneously, which requires developing suitable RCG strategies for the two MGCC converters as discussed next.

1) VSC1 RCG Strategy: Fluctuations in the DC Link voltage will affect the MGCC controllers, impacting its operation. In the MGCC topology, the current flowing out of the ADN and injected into the MG are the same; thus, the VSC2 can control the negative-sequence currents at both sides, allowing the VSC1 to suppress the fluctuations of the DC Link voltage. A PNSC strategy is widely used in VSC controls to eliminate the oscillations in the transferred active power; however, due to the MGCC architecture, a PNSC can only eliminate the fluctuations in P_{m1}. Thus, an improved PNSC strategy is proposed next to minimize the oscillations in DC Link voltage.

The dc voltage fluctuates due to the instantaneous energy flowing in and out of the DC Link. Therefore, the proposed PNSC strategy should eliminate the double-frequency oscillations of the sum of active powers flowing into the two converters. Hence, its control objectives should be: $P_{m1_0} = P_{m1_{0ref}}$, $Q_{m1_0} = Q_{m1_{0ref}}$, $P_{VSC1_{s2}} + P_{VSC2_{s2}} = 0$, and $P_{VSC1_{c2}} + P_{VSC2_{c2}} = 0$, where $P_{m1_{0ref}}$ is generated by the dc voltage controller. Thus, the powers of the VSC1 can be obtained as follows:

$$\mathbf{A} \begin{bmatrix} I_{1_d}^+ \\ I_{1_q}^+ \\ I_{1_d}^- \\ I_{1_q}^- \end{bmatrix} + \mathbf{B} \begin{bmatrix} I_{VSC1_d}^+ \\ I_{VSC1_q}^+ \\ I_{VSC1_d}^- \\ I_{VSC1_q}^- \end{bmatrix} = \frac{2}{3} \begin{bmatrix} P_{m1_0} \\ Q_{m1_0} \\ P_{VSC1_{s2}} \\ P_{VSC1_{c2}} \end{bmatrix} \tag{4}$$

where:

$$\mathbf{A} = \begin{bmatrix} V_{m1_d}^+ & V_{m1_q}^+ & V_{m1_d}^- & V_{m1_q}^- \\ V_{m1_q}^+ & -V_{m1_d}^+ & V_{m1_q}^- & -V_{m1_d}^- \\ \multicolumn{4}{c}{\mathbf{0}_{2\times4}} \end{bmatrix} \tag{5}$$

$$\mathbf{B} = \begin{bmatrix} \multicolumn{4}{c}{\mathbf{0}_{2\times4}} \\ V_{VSC1_q}^- & -V_{VSC1_d}^- & -V_{VSC1_q}^+ & V_{VSC1_d}^+ \\ V_{VSC1_d}^- & V_{VSC1_q}^- & V_{VSC1_d}^+ & V_{VSC1_q}^+ \end{bmatrix} \tag{6}$$

On the other hand, the expressions of positive and negative-sequence dq components of I_{VSC1} in (4) can be obtained from the VSC1 RLC filter as follows:

$$\begin{bmatrix} I_{VSC1_d}^+ \\ I_{VSC1_q}^+ \\ I_{VSC1_d}^- \\ I_{VSC1_q}^- \end{bmatrix} = \mathbf{I} \begin{bmatrix} I_{1_d}^+ \\ I_{1_q}^+ \\ I_{1_d}^- \\ I_{1_q}^- \end{bmatrix} + \mathbf{C} \begin{bmatrix} V_{x_d}^+ \\ V_{x_q}^+ \\ V_{x_d}^- \\ V_{x_q}^- \end{bmatrix} \tag{7}$$

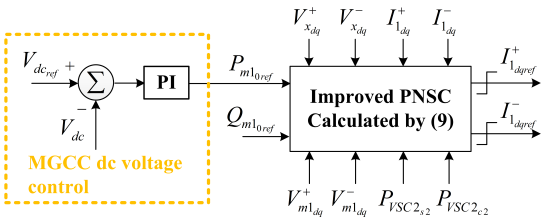


Fig. 4. VSC1 RCG control strategy.

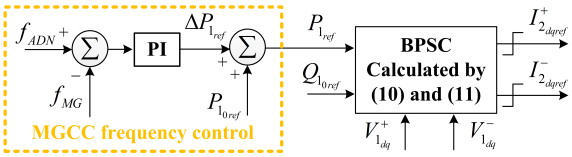


Fig. 5. VSC2 RCG control strategy.

where:

$$\mathbf{C} = \begin{bmatrix} 0 & \omega_0 C_{f1} & 0 & 0 \\ -\omega_0 C_{f1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\omega_0 C_{f1} \\ 0 & 0 & \omega_0 C_{f1} & 0 \end{bmatrix} \tag{8}$$

Hence, combining (4) to (8) with the four control objectives, the current references for VSC1 can be calculated as follows:

$$\begin{aligned} \begin{bmatrix} I_{1_{dref}}^+ \\ I_{1_{qref}}^+ \\ I_{1_{dref}}^- \\ I_{1_{qref}}^- \end{bmatrix} =& \frac{2}{3} (\mathbf{A} + \mathbf{B})^{-1} \begin{bmatrix} P_{m1_{0ref}} \\ Q_{m1_{0ref}} \\ -P_{VSC2_{s2}} \\ -P_{VSC2_{c2}} \end{bmatrix} \\ & - (\mathbf{A} + \mathbf{B})^{-1} \mathbf{B}\, \mathbf{C} \begin{bmatrix} V_{x_d}^+ \\ V_{x_q}^+ \\ V_{x_d}^- \\ V_{x_q}^- \end{bmatrix} \end{aligned} \tag{9}$$

where $P_{VSC2_{s2}}$ and $P_{VSC2_{c2}}$ can be calculated based on equations similar to (4) to (8) with $V_{y_d}^+$, $V_{y_q}^+$, $V_{y_d}^-$, $V_{y_q}^-$, $I_{2_d}^+$, $I_{2_q}^+$, $I_{2_d}^-$, and $I_{2_q}^-$. Fig. 4 shows the control diagram of the designed VSC1 RCG strategy, which is fed by the MGCC dc voltage controller. Note that $V_{x_d}^+$, $V_{x_q}^+$, $V_{x_d}^-$, $V_{x_q}^-$, $I_{1_d}^+$, $I_{1_q}^+$, $I_{1_d}^-$, and $I_{1_q}^-$ are required for computing the matrix $\mathbf{B}$.

2) VSC2 RCG Strategy: Based on the MGCC topology, its grid and MG terminal currents are identical and controlled by VSC2. To minimize the impact of the MG imbalance on the grid, the negative-sequence component of $\widetilde{I}_2$ can be eliminated using a BPSC strategy. Fig. 5 shows the designed RCG strategy for the VSC2, which is fed by the required MGCC frequency control that fast-synchs the MG frequency after a disturbance. Since the MGCC is controlling the grid powers, the grid voltage is used to calculate the current references as follows:

$$\begin{bmatrix} I_{2_{dref}}^+ \\ I_{2_{qref}}^+ \end{bmatrix} = \frac{2}{3} \begin{bmatrix} V_{1_d}^+ & V_{1_q}^+ \\ V_{1_q}^+ & -V_{1_d}^+ \end{bmatrix}^{-1} \begin{bmatrix} P_{1_{ref}} \\ Q_{1_{0ref}} \end{bmatrix} \tag{10}$$

$$I_{2_{dref}}^- = I_{2_{qref}}^- = 0 \tag{11}$$

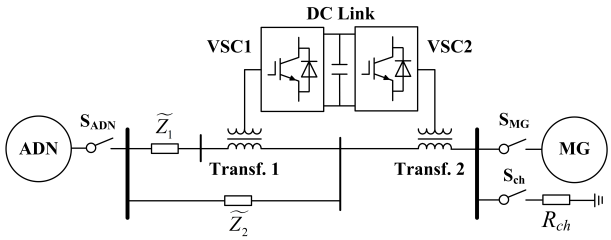


Fig. 6. Proposed MGCC start-up strategy.

D. Start-up Strategy

The DC Link initial charging process was not discussed in [12], using an external dc source for this purpose, which would be an issue in MGCC practical implementations. Thus, a start-up strategy without an external source is proposed here. Fig. 6 shows the circuit designed for the device start-up. Based on the MGCC power flow analysis, the active power always flows from VSC2 to VSC1 due to the $\widetilde{Z_2}$ branch; thus, only the VSC2 can be used to charge the DC Link capacitor. Furthermore, due to the series connection of two converters, a charging resistor is needed to provide a current path during the start-up process. This R_{ch} also divides the VSC2 input voltage to match the low ratings of the MGCC components.

The proposed charging procedure consists of four stages. Thus, in the Stage I, the anti-parallel diodes of the VSC2 are used as a diode rectifier to charge the DC Link to a certain voltage level with no controls. In this case, the DC Link can be charged to approximately the peak-to-peak line voltage of the ac side of the rectifier, as follows:

$$\begin{aligned} V_{dc} &= \sqrt{2}\,|\widetilde{V_y}| \\ \widetilde{V}_y &= \frac{|\widetilde{V_1}|}{1 + j\omega R_{ch} C_{f2}} \end{aligned} \tag{12}$$

where $|\widetilde{V_1}|$ is the amplitude of the utility terminal line voltage. Hence, with the desired voltage $V_{dc\mathrm{I}}$ for Stage I, the value of R_{ch} can be chosen to be:

$$R_{ch} = \frac{1}{\omega C_{f2}} \sqrt{\frac{2|\widetilde{V_1}|^2}{V_{dc\mathrm{I}}^2} - 1} \tag{13}$$

In Stage II, the switches of VSC2 are appropriately controlled to charge the DC Link capacitor to its reference value. As discussed in [37], it's preferable to charge dc capacitors with a constant current instead of a constant voltage. Thus, PQ control is adopted for the VSC2 in this case, where the active power setpoint can be obtained as follows for a constant charging current I_{dc_0}:

$$P_{ref} = \frac{I_{dc_0}}{C_{dc}} \int I_{dc_0} dt \quad \Rightarrow \quad P_{ref} = \frac{I_{dc_0}^2}{C_{dc}} t + V_{dc\mathrm{I}} I_{dc_0} \tag{14}$$

The reactive power setpoint in this case is set to 0 [37].

There is a buffer zone in which there is no DC Link voltage regulation before the VSC1 controls are activated, ensuring the MGCC operational constraint mentioned in Section II.B is satisfied, i.e., $P_y > P_{loss_{VSCs}} > 0$. Thus, in Stage III, with the initialized voltage from Stage II, the two systems can be connected through the MGCC by activating the VSC2 controllers, opening S_{ch} and closing S_{MG} simultaneously, while the VSC1 controllers are deactivated.

TABLE I
MGCC START-UP PROCEDURE

Stage	Procedure
I	Close S_{ADN} and S_{ch} for uncontrolled charging using anti-parallel diodes of VSC2 as a diode rectifier.
II	Controlled charging to the reference value of the DC Link voltage through PQ control of VSC2.
III	Simultaneous actions: • Activate VSC2 controllers. • Open S_{ch} to remove the charging resistor. • Close S_{MG} to connect the MG.
IV	Activate VSC1 controllers.

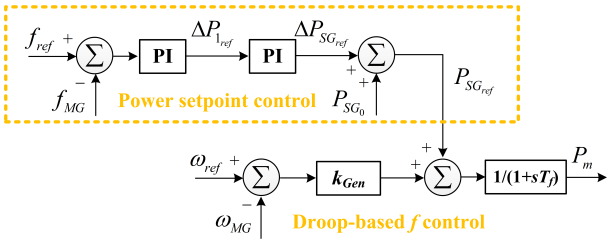


Fig. 7. Diagram of the SG frequency controller.

Table I shows the four stages of the proposed start-up procedure. The simulation results presented and discussed in the results section illustrate the efficiency of the proposed strategy, as the DC Link voltage reaches the required steady state value in a few seconds, being cost-effective and reliable since no external devices are required.

E. MGCC Small-Perturbation Stability Analysis

A modal estimation approach based on the Prony method, which does not require detailed system information, is used in this paper to investigate the system modes and dynamics based on TDS models and related data.

A detailed representation of the three-phase Synchronous Generator (SG) model is used for the simulations and studies. Small SGs are likely to use simple PI voltage regulators; thus, an IEEE Alternator Supplied Rectifier Excitation System 4 is chosen here [35]. As shown in Fig. 7, the SG governor is modeled as a droop-based frequency regulator, where k_{Gen} is the droop parameter, and P_m is the mechanical input power into the generator [38]. The power setpoint $P_{SG_{ref}}$ is generated by a designated control loop with two cascaded PI controllers to keep the MGCC frequency control output at 0, i.e., $\Delta P_{1_{ref}} = 0$ in Fig. 5. Thus, for any frequency deviations in the MG, the MGCC would respond quickly and balance the supply-demand from the ADN, while the MG SGs relax the requirements of the interface auxiliary frequency control after a delay and cover all the load changes locally [12].

Lines are modeled as coupled π branches, and loads are treated as constant impedances [35]. A load unbalance factor is defined to denote the most significant power deviations

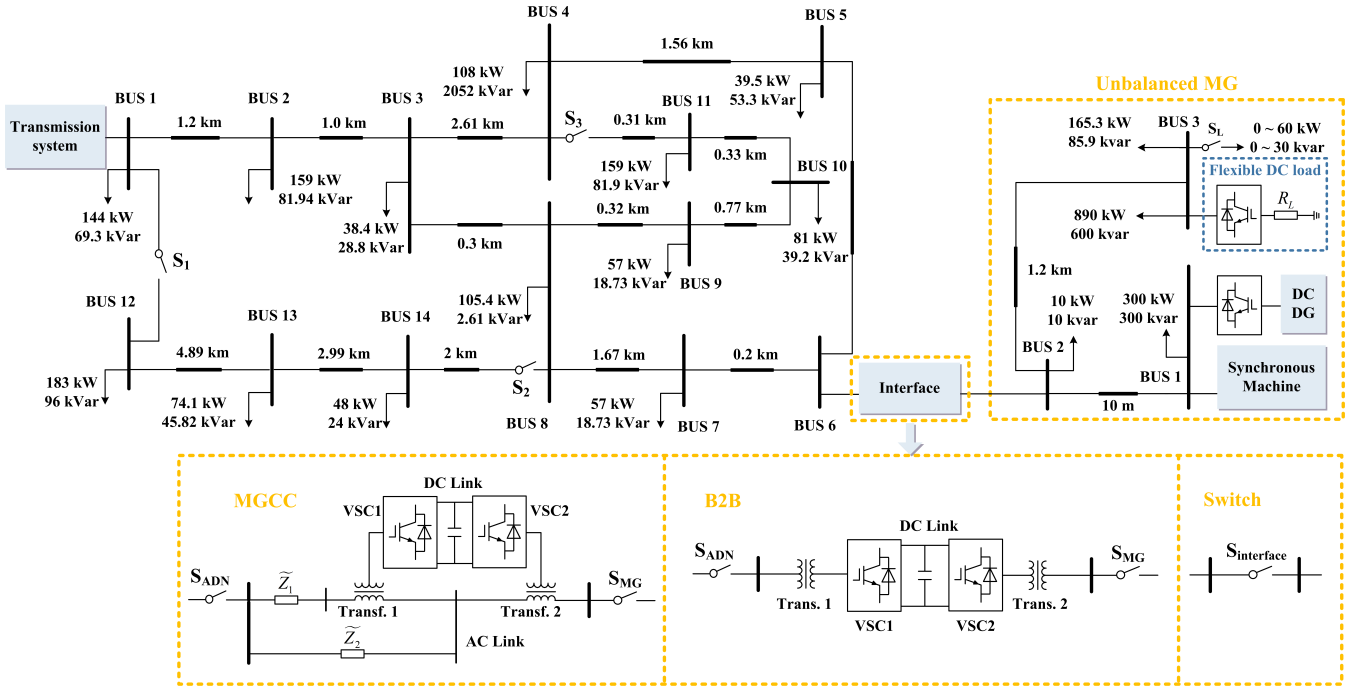


Fig. 8. Topology and loads of the balanced ADN and the unbalanced MG.

between the three phases to model different MG unbalance scenarios, as follows:

$$\begin{aligned} P_{MG_a} &= (1-\frac{k}{2})\ \frac{P_{MG}}{3} \quad & Q_{MG_a} &= (1-\frac{k}{2})\ \frac{Q_{MG}}{3} \\ P_{MG_b} &= \frac{P_{MG}}{3} & Q_{MG_b} &= \frac{Q_{MG}}{3} \\ P_{MG_c} &= (1+\frac{k}{2})\ \frac{P_{MG}}{3} & Q_{MG_c} &= (1+\frac{k}{2})\ \frac{Q_{MG}}{3} \end{aligned} \tag{15}$$

where k is the unbalance factor, and the subscripts a, b, and c denote the three phases [33], [35]. Thus, as the MG load in phase a increases, the load in phase c decreases, so that the total three-phase MG load remains constant.

The MGCC interface is modeled in detail based on its topology and the proposed improved controllers. The TDSs are carried out in PSCAD/EMTDC [39].

TABLE II
MGCC PARAMETERS

	Parameters	Values
Main Circuit	$\widetilde{Z_1}, \widetilde{Z_2}$	$10\ \Omega, 0.0001\ \Omega$
	R_{f1}, R_{f2}	$0.1\ \Omega, 0.1\ \Omega$
	L_{f1}, L_{f2}	40 mH, 60 mH
	C_{f1}, C_{f2}	$10\ \mu$F, $10\ \mu$F
	C_{dc}	2 mF
Control System	PLL (k_p, k_i)	$(100, 9000)$
	Active I Controller (k_{p1}, k_{i1})	$(5, 100)$
	Reactive I Controller (k_{p2}, k_{i2})	$(5, 100)$
	V_{dc} Controller $(k_{pV_{dc}}, k_{iV_{dc}})$	$(10, 50)$
	f Controller (k_{pf}, k_{if})	$(2, 3.33)$
	Switching Frequency	8 kHz

IV. RESULTS

A. Test System

The test system is a 12.47 kV, 60 Hz network based on the North American CIGRE distribution system comprising an MG connected to the grid via an MGCC, a B2B, or a switch [12]. As shown in Fig. 8, the studied ADN includes three switches to form loops and test various DGs under different configurations in the context of smart grids. Switches S_1, S_2, and S_3 are assumed to be close, open, and close, respectively, in this paper. The MG is assumed to represent an industrial site or a residential area, including 1 diesel generator, 3 buses, 5 ac loads, 1 inverter-based DG, and 1 controllable inverter-based dc load. The power rating of the SG is 4 MVA, and its inertia, droop parameter k_{Gen}, and governor time constant T_f are set to 2 s, 30 MW/Hz, and 0.2 s, respectively.

The inverter-based DG represents a typical PV system connected to the MG via a VSC operating under PQ control, delivering 0.2 MW and 0 Mvar. On the other hand, the 30-kW controllable dc load consists of a 19.2 kΩ resistive load connected to the MG via a VSC that maintains the DC Link voltage of 24 kV. The total loads of the MG are approximately 1.4 MW and 1 Mvar. Only the MG loads are assumed to be unbalanced, as per (15), to more clearly demonstrate the impact of imbalance on the MG, and on the imbalance and power quality of the ADN at the connecting bus, so that different control strategies for the MGCC to mitigate unbalancing at both the MG and ADN can be properly studied. The main parameters of the MGCC and B2B interfaces are shown in Table II and Table III, respectively. The B2B is modeled similarly to the MGCC in PSCAD/EMTDC. A switching frequency of 8 kHz is employed for both interfaces, as recommended in [39].

TABLE III
B2B PARAMETERS

	Parameters	Values
Main Circuit	R_{f1}, R_{f2}	$0.1\ \Omega, 0.1\ \Omega$
	L_{f1}, L_{f2}	40 mH, 60 mH
	C_{f1}, C_{f2}	$10\ \mu$F, $10\ \mu$F
	C_{dc}	2 mF
Control System	PLL (k_p, k_i)	$(100, 9000)$
	Active I Controller (k_{p1}, k_{i1})	$(5, 100)$
	Reactive I Controller (k_{p2}, k_{i2})	$(5, 100)$
	V_{dc} Controller $(k_{pV_{dc}}, k_{iV_{dc}})$	$(10, 50)$
	Switching Frequency	8 kHz

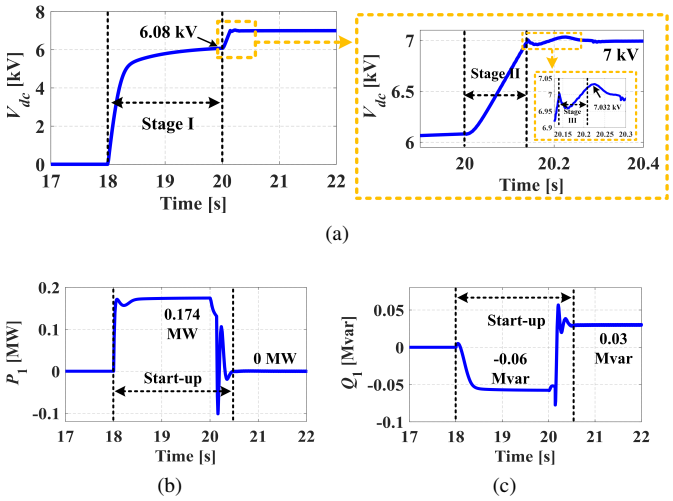


Fig. 9. MGCC start-up: (a) DC Link voltage; (b) active power flowing out of the ADN; and (c) reactive power flowing out of the ADN.

B. MGCC Start-up

The MGCC start-up is analyzed here based on the procedure proposed in Section III.D. Thus, the ADN and MG systems are assumed to operate separately at steady state before Stage I starts at t = 18 s. The MGCC setpoints are $V_{dc_{ref}} = 7$ kV and $Q_{m1_{0ref}} = 0$ Mvar for VSC1, and $P_{1_{0ref}} = 0$ MW and $Q_{1_{0ref}} = 0.03$ Mvar for VSC2. Note that 0.03 Mvar is approximately the minimum reactive power required to satisfy the mandatory operational limitation of the MGCC, as explained in Section II.B. The MG unbalance factor is set to 100%, i.e., $k = 1$. The charging resistor R_{ch} is 800 Ω

The simulation results of the MGCC start-up are shown in Fig. 9. Note that the DC Link voltage shown in Fig. 9 (a) reaches the setpoint value in 2.5 seconds, illustrating the effectiveness of the proposed strategy. Specifically, in Stage I, the input voltage of VSC2 is about 4.4 kV; thus, the DC Link voltage is initially charged to 6.08 kV using the VSC2 anti-parallel diodes. Stage II then begins at t = 20 s and lasts for roughly 0.14 seconds, where the VSC2 controls the capacitor charging with a constant I_{dc_0} = 0.1 kA, and charges the DC Link to 7 kV through PQ control. Next, Stage III creates a buffer zone lasting 0.04 seconds, in which the VSC1 controls are deactivated, allowing the transmitted powers reach values that satisfy the MGCC power flow limitations, i.e., $P_y > P_{loss_{VSCs}} > 0$. Finally, the VSC1 is connected in Stage IV, with V_{dc} stabilizing at 7 kV after a small oscillation at about t = 20.5 s. Figs. 13 (b) and (c) show the powers at the ADN side, illustrating that these transferred powers are kept at their setpoint values after the start-up process is completed.

C. Comparisons of Interfaces and Various Controls

The results of applying the proposed MGCC improved controls under unbalanced MG conditions are presented and discussed here. Table IV illustrates the considered relevant case studies, where Case 3 corresponds to the proposed improved controls. Note that the interfaces in all conditions regulate the powers on the grid side to facilitate the comparison of results for the different case studies.

Several common scenarios are analyzed, including the ADN-MG connection, changes in the interface power setpoints, three-phase fault conditions at the end of an MG feeder, and gradual load changes of the MG. The two systems are assumed to operate separately at steady state before the MGCC start-up at 18 s and ADN-MG interconnection. The MG unbalance factor is set to $k = 1$. The setpoints of the MGCC are $V_{dc_{ref}} = 7$ kV and $Q_{m1_{0ref}} = 0$ Mvar for VSC1, and $P_{1_{0ref}} = 0$ MW and $Q_{1_{0ref}} = 0.03$ Mvar for VSC2. The setpoints of B2B are $P_{1_{0ref}} = 0$ MW and $Q_{1_{0ref}} = 0$ Mvar for VSC1, and $V_{dc_{ref}} = 24$ kV and $Q_{2_{0ref}} = 0$ Mvar for VSC2. To demonstrate the control capabilities of the interfaces, the active power setpoint changes to 0.25 MW and then 0.5 MW at 40 s and 60 s, respectively. The performances of the interfaces under fault conditions are studied next; thus, three-phase resistive faults at Bus 3 of the MG and Bus 8 of the ADN are simulated, with the fault occurring at 80 s and 100 s, respectively, and clearing after 120 ms [40]. Finally, load changes and fluctuations in the MG are considered by closing Switch S_L in Fig. 8 with the load abruptly increasing from 0 to 33 kW and 16.5 kvar at 120 s, and then increasing to 60 kW and 30 kvar at a rate of 3 kW and 1.5 kvar every 2 s, respectively.

Table V shows the steady-state voltage and current imbalances at the grid side for $P_{1_{0ref}} = 0.5$ MW. Several voltage and current unbalance factors, including Percentage Voltage Unbalance Factors (%VUFs) and Percentage Current Unbalance Factors (%CUFs), defined in [41] and [42], respectively, which measure the ratio of the negative and zero sequence component to the positive sequence component, are used to evaluate unbalancing in the simulation results. Observe that the transferred powers cannot be controlled when using the switch as the interface, causing a significant voltage and current distortion at the grid side. The negative-sequence current is nearly eliminated due to the RCG strategy on the VSC2 when using the MGCC with the proposed controls, thus improving the power quality of the grid. Observe that there is no zero-sequence current or voltage when using the B2B due to the Y/Δ transformers. The MGCC introduces zero-sequence current and voltage to the utility because the primary sides of the transformers are connected in series, and the secondary windings have a grounded Y connection, which provides a zero-sequence component path between the two systems.

TABLE IV
CASE STUDIES

		MGCC			B2B		Switch
		Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
PLL		SRF PLL	DDSRF PLL	DDSRF PLL	SRF PLL	DDSRF PLL	
Current Control		Balance	Unbalance	Unbalance	Balance	Unbalance	
RCG Strategies	VSC1	IARC + V_{dc} Control	PNSC + V_{dc} Control	Proposed Strategies in Section III.C	IARC	BPSC	−−
	VSC2	IARC + f Control	BPSC + f Control		IARC + V_{dc} Control	BPSC + V_{dc} Control	

TABLE V
GRID SIDE SEQUENCE VOLTAGES AND CURRENTS FOR $P_{1_{0ref}} = 0.5$ MW

Variable	MGCC			B2B		Switch
	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
I^+ [A]	23.28	23.28	23.28	23.23	23.23	48.41
I^- [A]	2.192	0.019	0.011	0.031	0.002	16.81
I^0 [A]	0.686	0.684	0.684	0	0	2.637
%CUF$^-$	9.4%	0.1%	0.0%	0.1%	0.0%	34.7%
%CUF^0	2.9%	2.9%	2.9%	0%	0%	5.4%
V_1^+ [kV]	7.172	7.172	7.172	7.176	7.176	7.202
V_1^- [V]	6.077	0.061	0.041	0.084	0.006	46.71
V_1^0 [V]	3.999	3.985	3.994	0	0	15.31
%VUF$^-$	0.1%	0.0%	0.0%	0.0%	0.0%	0.6%
%VUF^0	0.1%	0.1%	0.1%	0%	0%	0.2%

TABLE VI
PEAK-TO-PEAK VALUES OF DC LINK VOLTAGE AND POWER OSCILLATIONS FOR $P_{1_{0ref}} = 0.5$ MW

Variable	MGCC			B2B		Switch
	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
V_{dc} [V]	9.028	4.315	0.483	12.13	11.31	−−
P_1 [kW]	4.806	2.258	0.913	0.223	0.142	48.16
Q_1 [kvar]	8.301	2.244	0.909	0.086	0.102	50.41
P_2 [kW]	3.606	3.699	2.156	4.136	3.984	48.16
Q_2 [kvar]	9.797	3.947	2.699	10.23	3.794	50.41

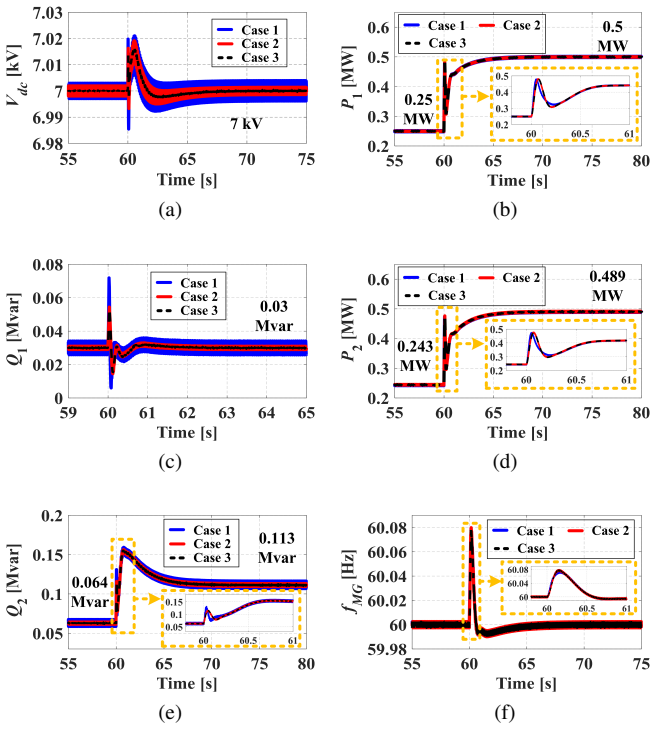


Fig. 10. Setpoint change from 0.25 MW to 0.5 MW for MGCC Cases 1 to 3: (a) DC Link voltage; (b) active power at the ADN side; (c) reactive power at the ADN side; (d) active power at the MG side; (e) reactive power at the MG side; and (f) MG frequency.

The oscillations of the DC Link voltage and powers are illustrated in Table VI. Observe that the MGCC with the improved controls can eliminate the impact of the MG imbalance on the grid side to a great extent. Specifically, the proposed improved PNSC strategy for VSC1 in Case 3 can further decrease the oscillations of the DC Link voltage to less than 4.5% of the original control and about 11% of the traditional PNSC strategy. Thus, the oscillations in the MGCC control system introduced by the dc voltage controller are minimized, decreasing the fluctuations in transferred powers. The B2B interface provides a mutually isolated connection between the two power systems, resulting in the negative-sequence current and voltage, as well as the power oscillations at the ADN side, being relatively small when using the B2B with traditional unbalance controls.

The transient responses as the setpoint changes from 0.25 MW to 0.5 MW under different cases are illustrated in Fig. 10 and Fig. 11. Note that the DC Link voltages in Fig. 10 (a) and Fig. 11 (a) are maintained at their desired values, i.e., 7 KV for the MGCC and 24 kV for the B2B. Furthermore, Figs. 10 (b) and (c) and Figs. 11 (b) and (c) show the active and reactive powers flowing out of the grid side, showing that the two interfaces can control these transferred powers accurately and flexibly. The active and reactive powers injected into the MG shown in Figs. 10 (d) and (e) and Figs. 11 (d) and (e) demonstrate that the power losses of the two interfaces are nearly the same, and only the B2B can regulate the reactive power at the MG side. On the other hand, as shown in Fig. 10 (f) and Fig. 11 (f), the MGCC can offer a better frequency response with less deviations than the B2B due to the MGCC frequency controller and the local generator. However, it takes longer for the active and reactive powers to stabilize for the same reason. The transient responses of Cases 2 and 3 are almost the same, slightly slower than Case 1.

Fig. 12 to Fig. 14 illustrate the simulation results for the

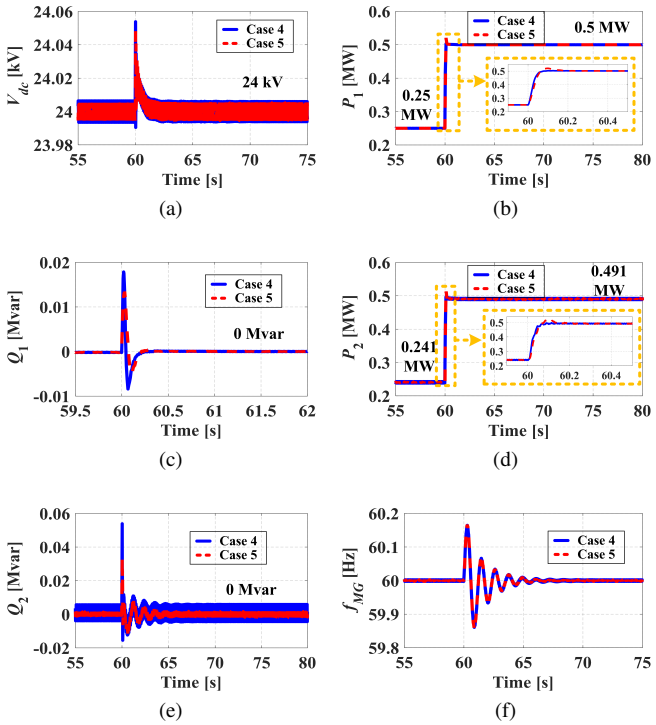


Fig. 11. Setpoint change from 0.25 MW to 0.5 MW for B2B Cases 4 and 5: (a) DC Link voltage; (b) active power at the ADN side; (c) reactive power at the ADN side; (d) active power at the MG side; (e) reactive power at the MG side; and (f) MG frequency.

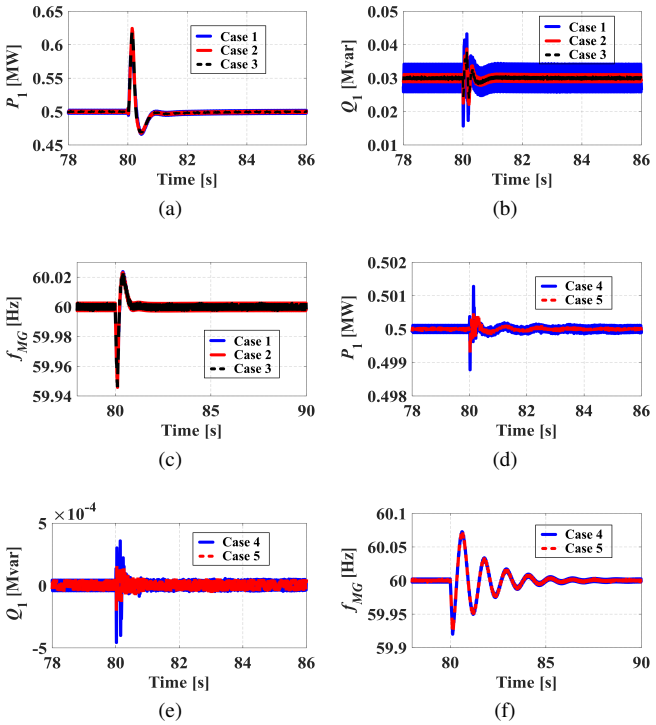


Fig. 12. Three-phase fault condition in the MG: (a) active power at the ADN side for MGCC Cases 1 to 3; (b) reactive power at the ADN side for MGCC Cases 1 to 3; (c) MG frequency for MGCC Cases 1 to 3; (d) active power at the ADN side for B2B Cases 4 and 5; (e) reactive power at the ADN side for B2B Cases 4 and 5; and (f) MG frequency for B2B Cases 4 and 5.

three-phase fault conditions in the MG and the ADN at 80 s and 100 s, respectively, as well as the load changes in the MG at 120 s. Observe that, compared to the B2B, the MGCC first responds to the power changes with its frequency controller, while the MG SG relaxes this requirement after a delay and eventually covers all the supply-demand deviations. Thus, the MGCC-based system shows a smaller frequency deviation but more significant active power fluctuations and longer settling time. The switch connects the two power grids uncontrollably; thus, the transient oscillations are much more significant compared to the MGCC or B2B-based systems, as shown in the simulation results at the ADN-MG connection for Case 6 depicted in Fig. 15.

D. MGCC Stability Analysis

Several scenarios are considered to analyze the effects of the control parameters and MG load unbalance on the MGCC small-perturbation stability. As mentioned in Section III.E, PSCAD/EMTDC simulations provide data to investigate the dynamics of the system, using in the Prony method to accurately estimate the system modes. Note that the MGCC is implemented with the improved unbalance control corresponding to Case 3 in the studies presented next.

1) Frequency Control Parameter: In the first scenario, the effect of the PI parameter k_{i_f} of the MGCC frequency controller on system stability is studied. The MG unbalance factor is set to k = 0.6, and the system is perturbed by changing the active power setpoint $P_{1_{0ref}}$ from 0 to 50 kW,

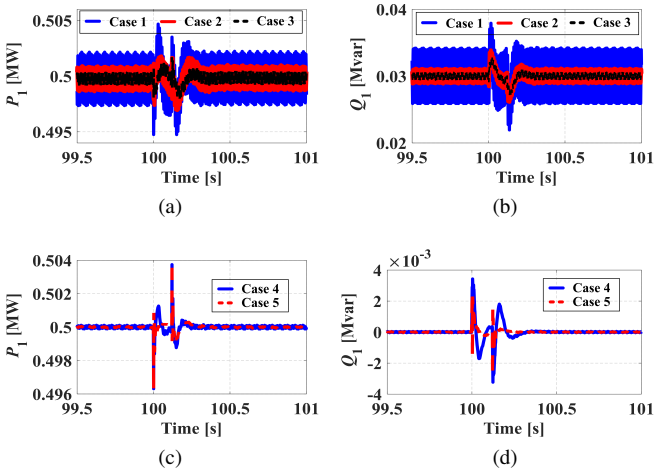


Fig. 13. Three-phase fault condition in the ADN: (a) active power at the ADN side for MGCC Cases 1 to 3; (b) reactive power at the ADN side for MGCC Cases 1 to 3; (c) active power at the ADN side for B2B Cases 4 and 5; and (d) reactive power at the ADN side for B2B Cases 4 and 5.

so that the dominant system modes can be estimated using the identification approach. Since the time step of the TDS in PSCAD/EMTDC is small (10 μs), the output data is sampled at 1000 Hz [35].

Table VII depicts the estimated eigenvalues along with their frequencies and damping ratios for different values of k_{i_f}. Note that as k_{i_f} increases, the frequency increases and the damping ratio decreases. Furthermore, it can be observed that

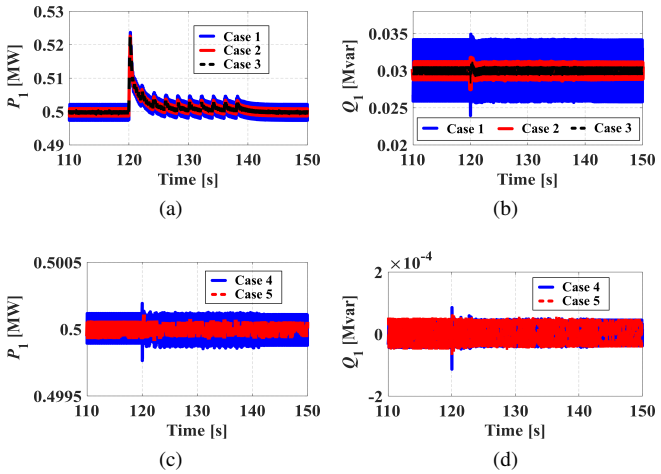


Fig. 14. Load changes in the MG: (a) active power at the ADN side for MGCC Cases 1 to 3; (b) reactive power at the ADN side for MGCC Cases 1 to 3; (c) active power at the ADN side for B2B Cases 4 and 5; and (d) reactive power at the ADN side for B2B Cases 4 and 5.

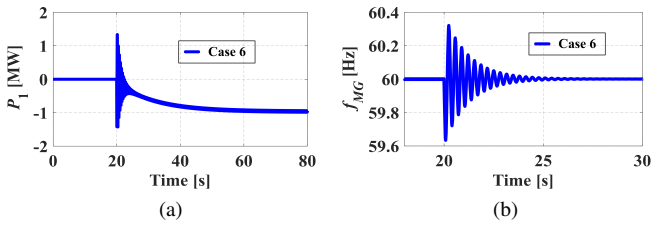


Fig. 15. ADN-MG connection for switch Case 6: (a) active power at the ADN side and (b) MG frequency.

beyond $k_{i_f} = 100$, the eigenvalue crosses the imaginary axis and thus the system becomes unstable.

2) DC Voltage Control Parameter: Similarly, the second scenario analyzes the effect of PI parameters in the MGCC V_{dc} controller. The MG unbalance factor is set to 60%, and a disturbance is created by changing the active power setpoint from 0 to 50 kW. The sampling frequency is 1000 Hz.

Table VIII illustrates the estimated eigenvalues, frequencies, and damping ratios for different values of $k_{i_{V_{dc}}}$. Similar conclusions can be drawn as in the first scenario, i.e., as $k_{i_{V_{dc}}}$ increases, the frequency increases while the damping ratio decreases.

3) MG Load Unbalancing: Finally, the effect of MG load unbalance on system stability is analyzed here. The PI parameters of the MGCC frequency control and DC voltage control are set to (2, 100) and (10, 50), respectively. The same perturbation is chosen for estimating system modes using the Prony method with a sampling frequency of 1000 Hz. Table IX shows the estimated eigenvalues for different values of k. Observe that as k increases, the frequency decreases, while the damping ratio increases. Similar conclusions were reported in [33], [35].

TABLE VII
DOMINANT EIGENVALUES FOR DIFFERENT VALUES OF k_{i_f}

k_{i_f}	Eigenvalue	Frequency	Damping ratio
5	$-4.17 \pm j3.06$	0.4847	0.8061
10	$-5.62 \pm j5.76$	0.9173	0.6981
20	$-4.47 \pm j11.77$	1.8728	0.3554
50	$-3.41 \pm j13.86$	2.6056	0.2035
100	$-0.28 \pm j23.38$	3.7212	0.0121
200	$4.68 \pm j29.19$	4.6451	-0.1583

TABLE VIII
DOMINANT EIGENVALUES FOR DIFFERENT VALUES OF $k_{i_{V_{dc}}}$

$k_{i_{V_{dc}}}$	Eigenvalue	Frequency	Damping ratio
50	$-5.96 \pm j18.72$	2.9793	0.3032
100	$-7.53 \pm j26.81$	4.2673	0.2703
200	$-10.06 \pm j52.46$	8.3493	0.1884
500	$-4.81 \pm j62.86$	10.0045	0.0764
800	$2.74 \pm j76.22$	12.1315	-0.0359

TABLE IX
DOMINANT EIGENVALUES FOR DIFFERENT VALUES OF k

k	Eigenvalue	Frequency	Damping ratio
0	$-0.23 \pm j23.22$	3.6958	0.0099
0.2	$-0.59 \pm j23.04$	3.6677	0.0255
0.4	$-0.95 \pm j22.81$	3.6301	0.0418
0.6	$-1.14 \pm j22.64$	3.6040	0.0503
0.8	$-1.33 \pm j22.43$	3.5695	0.0590

V. CONCLUSION

An improved control system was proposed for the novel MGCC ADN-MG interface to enhance its operation under unbalanced conditions when controlling the power exchanged on the utility side. Two RCG strategies were designed for the converters to reduce the impact of the MG imbalance on the grid side, and an improved PNSC strategy was proposed to minimize the DC Link voltage fluctuations. Furthermore, a four-stage start-up strategy was proposed for initially charging the dc capacitor, making the interface more practical and cost-effective. The improved controls were tested using a realistic system, illustrating the performance of the MGCC with the proposed controls compared to the original controls, a typical B2B interface with different existing controls, and an uncontrolled switch ADN-MG interface. The simulation results show that the MGCC with the proposed controls can minimize the impact of the MG imbalance on the grid side. Finally, the small-perturbation stability of grid-connected MGs with the MGCC interface was studied based on the Prony method to investigate the effects of MGCC control parameters and MG unbalance on the system stability, demonstrating that the PI parameters of V_{dc} and f controllers in the MGCC interface can significantly affect the MG dynamic performance, and thus showing the need to properly tune them.

REFERENCES

[1] D. E. Olivares *et al.*, "Trends in microgrid control," *IEEE Trans. Smart Grid*, vol. 5, no. 4, pp. 1905–1919, Jul. 2014.

[2] R. Lasseter *et al.*, "White paper on integration of distributed energy resources: The CERTS microgrid concept," Dept. Energy, Office Power Technol. Berkeley, CA, USA, Rep. DE-AC03-76SFW098, 2002.

[3] M. Farrokhabadi *et al.*, "Microgrid stability definitions, analysis, and examples," *IEEE Trans. Power Syst.*, vol. 35, no. 1, pp. 13–29, Jan. 2020.

[4] J. M. Guerrero, P. C. Loh, T.-L. Lee, and M. Chandorkar, "Advanced control architectures for intelligent microgrids-Part II: Power quality, energy storage, and ac/dc microgrids," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1263–1270, Apr. 2013.

[5] K. K. Sen and M. L. Sen, *Introduction to FACTS Controllers: Theory, Modeling, and Applications*. Hoboken, NJ, USA: IEEE Press, 2009.

[6] X. Guo, D. Xu, J. M. Guerrero, and B. Wu, "Space vector modulation for dc-link current ripple reduction in back-to-back current-source converters for microgrid applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6008–6013, Oct. 2015.

[7] L. González, G. Garcerá, E. Figueres, and R. González, "Effects of the PWM carrier signals synchronization on the dc-link current in back-to-back converters," *Appl. Energy*, vol. 87, no. 8, pp. 2491–2499, Aug. 2010.

[8] I. D. Souza, P. M. de Almeida, G. A. Fogli, P. G. Barbosa, and P. F. Ribeiro, "Multivariable optimal control applied to a back-to-back power converter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 9406–9418, Sep. 2022.

[9] X. Xu, M. Wu, K. Wang, M. Zhang, H. Li, Y. W. Li, and Y. Li, "Common-mode voltage reduction for back-to-back two-level converters based on zero-sequence voltage injection," *IEEE Trans. Ind. Electron.*, Dec. 2023.

[10] J. Samanes, E. Gubia, X. Juankorena, and C. Girones, "Common-mode and phase-to-ground voltage reduction in back-to-back power converters with discontinuous PWM," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7499–7508, Sep. 2020.

[11] B. R. Andersen and S. L. Nilsson, *Flexible AC Transmission Systems*. Cham, Switzerland: Springer, 2020.

[12] B. Tamimi, H. Gu, and C. A. Cañizares, "An effective controllable grid interface for microgrids," *IEEE Trans. Smart Grid*, vol. 14, no. 2, pp. 914–927, Mar. 2023.

[13] Z. Pan, X. Wang, T. T. G. Hoang, and L. Tian, "An enhanced phase-locked loop for non-ideal grids combining linear active disturbance controller with moving average filter," *Int. J. Electr. Power Energy Syst.*, vol. 149, p. 109021, Jul. 2023.

[14] P. Rodríguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584–592, Mar. 2007.

[15] C. Zhang, S. Føyen, J. A. Suul, and M. Molinas, "Modeling and analysis of SOGI-PLL/FLL-based synchronization units: Stability impacts of different frequency-feedback paths," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 2047–2058, Sep. 2021.

[16] I. Aboudrar, S. El Hani, H. Mediouni, N. Naseri, and A. Daghouri, "LVRT capability enhancement of a grid connected three phase PV system by ADRC and DSOGI FLL," *Int. Trans. Electr. Energy Syst.*, vol. 31, no. 11, p. e13059, Aug. 2021.

[17] S. Gude and C.-C. Chu, "Dynamic performance enhancement of single-phase and two-phase enhanced phase-locked loops by using in-loop multiple delayed signal cancellation filters," *IEEE Trans. Ind. Applicat.*, vol. 56, no. 1, pp. 740–751, Feb. 2020.

[18] S. Mondal, P. K. Gayen, and D. N. Gaonkar, "A fast and robust PLL design with a combination of frequency-adaptive alpha-beta-CDSC and SOGI," *IEEE Trans. Ind. Electron.*, vol. 72, no. 1, pp. 949–958, Jan. 2025.

[19] W. Luo and D. Wei, "A frequency-adaptive improved moving-average-filter-based quasi-type-1 PLL for adverse grid conditions," *IEEE Access*, vol. 8, pp. 54 145–54 153, Mar. 2020.

[20] P. Taheri, J. Amini, and M. Moallem, "Variable window size moving average filter for phase-locked-loop synchronization," *IEEE Access*, vol. 12, pp. 88 111–88 121, Jun. 2024.

[21] H.-S. Song and K. Nam, "Dual current control scheme for PWM converter under unbalanced input voltage conditions," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 953–959, Oct. 1999.

[22] D. G. Holmes, T. A. Lipo, B. P. Mcgrath, and W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, Nov. 2009.

[23] P. Montero-Robina, K. Rouzbehi, F. Gordillo, and J. Pou, "Grid-following voltage source converters: Basic schemes and current control techniques to operate with unbalanced voltage conditions," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 528–544, Oct. 2021.

[24] Y. Gui, X. Wang, H. Wu, and F. Blaabjerg, "Voltage-modulated direct power control for a weak grid-connected voltage source inverters," *IEEE Tran. Power Electron.*, vol. 34, no. 11, pp. 11 383–11 395, Nov. 2019.

[25] S. M. Hoseinizadeh, S. Ouni, H. Karimi, M. Karimi-Ghartemani, and K. L. Lian, "Comparison of PLL-based and PLL-less vector current controllers," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 10, no. 1, pp. 436–445, Feb. 2022.

[26] S. Silwal, M. Karimi-Ghartemani, H. Karimi, M. Davari, and S. M. H. Zadeh, "A multivariable controller in synchronous frame integrating phase-locked loop to enhance performance of three-phase grid-connected inverters in weak grids," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10 348–10 359, Sep. 2022.

[27] S. M. Hoseinizadeh, H. Karimi, M. Karimi-Ghartemani, and S. Ouni, "A multivariable phase-locked loop-integrated controller for enhanced performance of voltage source converters under weak grid conditions," *IEEE Trans. Ind. Electron.*, vol. 69, no. 10, pp. 10 079–10 089, Oct. 2022.

[28] S. M. Hoseinizadeh, H. Karimi, and M. Karimi-Ghartemani, "A robust phase-locked loop-integrated controller in stationary frame for voltage source converters connected to weak and unbalanced grids," *IEEE Tran. Ind. Electron.*, vol. 71, no. 9, pp. 10 647–10 657, Sep. 2024.

[29] Z. Wang, B. Wu, D. Xu, M. Cheng, and L. Xu, "DC-link current ripple mitigation for current-source grid-connected converters under unbalanced grid conditions," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4967–4977, Aug. 2016.

[30] P. Rodriguez, A. V. Timbus, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Flexible active power control of distributed power generation systems during grid faults," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2583–2592, Oct. 2007.

[31] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "Current reference generation based on next-generation grid code requirements of grid-tied converters during asymmetrical faults," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 8, no. 4, pp. 3784–3797, Dec. 2020.

[32] H. Gu and Z. Jiao, "Comprehensive small-signal model and stability analysis of VSC-based medium-voltage dc distribution system," *IET Gener. Transm. Distrib.*, vol. 13, no. 20, pp. 4642–4649, Oct. 2019.

[33] R. H. Salim and R. A. Ramos, "A model-based approach for small-signal stability assessment of unbalanced power systems," *IEEE Trans. Power Syst.*, vol. 27, no. 4, pp. 2006–2014, Nov. 2012.

[34] J. Zhu, J. Hu, S. Wang, and M. Wan, "Small-signal modeling and analysis of MMC under unbalanced grid conditions based on linear time-periodic (LTP) method," *IEEE Trans. Power Deliv.*, vol. 36, no. 1, pp. 205–214, Feb. 2021.

[35] E. Nasr-Azadani, C. A. Canizares, D. E. Olivares, and K. Bhattacharya, "Stability analysis of unbalanced distribution systems with synchronous machine and DFIG based distributed generators," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2326–2338, Sep. 2014.

[36] H. Gu, B. Tamimi, and C. A. Cañizares, "Microgrid connector controller prototyping," in *IEEE PES Innovative Smart Grid Technologies (ISGT)*, pp. 1–6, Oct. 2024.

[37] B. Tamimi and C. A. Cañizares, "Modeling and application of hybrid power flow controller in distribution systems," *IEEE Trans. Power Deliv.*, vol. 33, no. 6, pp. 2673–2682, Dec. 2018.

[38] B. Alghamdi and C. A. Cañizares, "Frequency regulation in isolated microgrids through optimal droop gain and voltage control," *IEEE Trans. Smart Grid*, vol. 12, no. 2, pp. 988–998, Mar. 2021.

[39] "Manitoba Hydro International Ltd." PSCAD. Accessed: Jul. 2024 [Online]. Available: https://www.pscad.com/.

[40] "IEEE recommended practice for protection and coordination of industrial and commercial power systems (IEEE Buff book)," *IEEE Std 242-2001 (Revision of IEEE Std 242-1986)*, pp. 1–710, Oct. 2001.

[41] "Definitions of voltage unbalance," *IEEE Power Engineering Review*, vol. 21, no. 5, pp. 49–51, Sep. 2001.

[42] "IEEE recommended practice for monitoring electric power quality," *IEEE Std 1159-2009 (Revision of IEEE Std 1159-1995)*, pp. 1–94, Jun. 2009.



Hanwen Gu (Student Member, IEEE) received his B.Sc. degree from Northeast Electric Power University, Jilin, China, in 2017. He is pursuing a Ph.D. degree in the School of Electrical Engineering at Xi'an Jiaotong University, Xi'an, China. His research interests include modeling, stability analysis, control, and optimization of microgrids.



Behnam Tamimi (Senior Member, IEEE) is an engineer and educator specializing in electric power and energy systems. He earned his Ph.D. in Electrical and Computer Engineering from the University of Waterloo, Ontario, Canada, in 2018. He holds two US patents in microgrid applications and distribution systems. He has also served on the IEEE Power Systems Dynamic Performance Committee and participated in two IEEE-PES task forces focused on benchmarking test systems for stability analysis. He has received multiple national and international awards, including two IEEE recognition awards in 2016 and 2017. Currently, he is the Lead Grid Modeling and Integration Engineer at Canadian Energy Management Division. His research interests include sustainable energy systems, electric vehicles, power electronics applications, and data-driven controls and optimization in modern energy systems.



Claudio Cañizares (Fellow, IEEE) is a University Professor, the Hydro One Endowed Chair, and the Executive Director of the Waterloo Institute for Sustainable Energy (WISE) at the ECE Department of the University of Waterloo, where he has been since 1993. His highly cited research focuses on modeling, simulation, computation, stability, control, and optimization of power and energy systems in the context of decarbonization and grid-edge technologies. He is a former IEEE Trans. Smart Gird EIC and Division VII Director to the IEEE Board; a Fellow of the IEEE, the Royal Society of Canada, the Canadian Academy of Engineering, and the Chinese Society for Electrical Engineering; and has received the 2017 IEEE PES Outstanding Power Engineering Educator Award, the 2016 IEEE Canada Electric Power Medal, and multiple awards and recognitions from PES Technical Committees.