A High-Resolution CMOS Single-Photon-Counting Spectrographic X-Ray Imager

by

Michael Wright

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2023

© Michael Wright 2023

Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Digital X-ray imagers for clinical mammography and computed tomography (CT) have been recently taking advantage of the noise-rejection properties of single-photon-counting (SPC) architectures. However, conventional SPC imagers are limited in spatial and energy resolution due to the substantial circuit area required to accommodate signal processing and digitization components in each pixel. To enable higher spatial resolution using smaller pixels, while simultaneously increasing energy resolution for multi-spectral imaging, new circuit architectures are required for SPC X-ray imagers.

This thesis presents the design and experimental characterization of the first complementary metal-oxide-semiconductor (CMOS) SPC X-ray imager readout integrated circuit (ROIC) to use frequency-division-multiplexed (FDM) readout for improved spatial and energy resolution. FDM readout allows the pixels in our ROIC to share analog-to-digital converter (ADC) resources, so that fewer components are integrated in each pixel. This enables us to shrink the pixel area, improving spatial resolution. Shared ADCs also have higher resolution than those in conventional implementations, enabling higher overall energy resolution.

Our proposed ROIC, designed in a 180-nm CMOS technology, includes an 8×16 pixel array and 16 ADCs. To achieve high spatial resolution and sufficient count rate for mammography and CT, we design our pixels with an area of only $35 \times 35\,\mu\text{m}^2$, approximately 50% smaller than commercial SPC imagers. Our ROIC uses FDM readout to multiplex banks of eight pixels into a shared 8-bit 160-MHz-sample-rate pipelined ADC, enabling full digitization of pixel analog outputs. We achieve six bins of energy resolution, which exceeds the resolution of recently-reported conventional SPC imagers that use larger-area pixels. Our ROIC also has a measured equivalent-noise charge (ENC) of $101\,\text{e}^-_{\text{rms}}$, which is comparable to conventional imagers, and a maximum count-rate of $10^8\,\text{photons/mm}^2\text{/s}$, suitable for mammography and CT.

Acknowledgements

Firstly, I would like to thank my supervisors Dr. Peter Levine and Dr. Ahmet Camlica for their support, guidance, and trust throughout my degree.

I would also like to extend my gratitude to my colleagues Zain Warsi, Reza Mohammadi, and Ahmad Lakhani for their knowledge, support, and helpful discussions.

Additionally, I would like to show my appreciation to Dr. Karim Karim and Dr. John Long for reviewing my thesis, and I would like to thank Vieworks Co. for their support.

Dedication

This is dedicated to Emma.

Table of Contents

Author's Declaration ii

Abstract iii

Acknowledgements iv

Dedication v

List of Figures xi

List of Tables xvi

List of Abbreviations xviii

1 Introduction 1

1.1 X-Ray Imagers 2

1.1.1 CMOS Direct-Conversion Digital X-Ray Imagers 2

1.1.2 X-ray Sensor Material Properties 4

1.1.3 Integration-Mode vs. Single-Photon-Counting Imagers 5

1.1.4 Conventional Single-Photon-Counting Architectures 6
1.2 Performance Metrics 8
1.2.1 Count Rate 9
1.2.2 Noise 10
1.2.3 Spatial Resolution 11
1.2.4 Spectral Resolution 11
1.3 Techniques for Improved Resolution 12
1.3.1 Resource Sharing 14
1.3.2 Frequency-Division Multiplexing 16
1.4 Imager Design Overview 18
1.4.1 Amorphous Selenium Material Properties 19
1.4.2 System Specifications 20
1.5 Thesis Organization 23

2 System Modelling and Design **25**

2.1 System Overview 25
2.2 Pixel Modelling 29
2.2.1 Pixel Specifications 30
2.2.2 Pixel Noise 32
2.2.3 Power Specification 35
2.3 System Modelling 35
2.4 Pixel Design 39
2.4.1 Charge Sensitive Amplifier 39

2.4.2 Mixer . . . 48
2.4.3 Lowpass Filter . . . 50
2.4.4 Gm Stage and Pixel Bank Summing . . . 52
2.4.5 Pixel Power Consumption . . . 55
2.5 Pipelined ADC Design . . . 55
2.5.1 Fully-Differential OTA . . . 59
2.5.2 Switched-Capacitor Comparator . . . 65
2.5.3 Differential DAC . . . 68
2.5.4 Digital Output Decoder . . . 69
2.5.5 Simulated ADC Performance . . . 71
2.6 Auxiliary Circuits . . . 75
2.6.1 Voltage Regulators . . . 75
2.6.2 Biases . . . 77
2.6.3 Non-Overlapping Clock Generation . . . 79
2.6.4 On-Chip Test Circuits . . . 80
2.6.5 Digital Configuration . . . 81
2.6.6 Other Buffering . . . 81
2.7 Chip Architecture and Layout . . . 82
2.7.1 Full ROIC Layout . . . 82
2.7.2 Pixel Layout . . . 84
2.7.3 Pixel Array Layout . . . 85
2.7.4 ADC Layout . . . 86
2.8 System-Level Functional Simulation Results . . . 87

3 Experimental Results **91**

3.1 Fabricated ROIC 91

3.2 Printed-Circuit Board Design 92

3.2.1 Power Supplies 93

3.2.2 Bias, Reference, and Clock Supplies 94

3.2.3 Input and Output Buffering 95

3.2.4 Microcontroller 96

3.3 Electrical Characterization 96

3.3.1 Charge Sensitive Amplifier Measurements 96

3.3.2 Pixel Bank Measurements 101

3.3.3 ADC Measurements 103

3.3.4 Full System Measurements 109

3.3.5 Discussion 111

4 Conclusion and Future Work **113**

4.1 Future Work 113

References **115**

APPENDICES **125**

A ROIC Pinout **126**

B Bonding Diagram **131**

C Scan Chain Control Bit Map **133**

D PCB Schematics 134

List of Figures

1.1 Structure of a hybrid CMOS X-ray imager. 3

1.2 Functional concept of a direct-conversion X-ray detector pixel. 4

1.3 Conventional SPC pixel circuit [7]. 7

1.4 Comparison of count rate models. 10

1.5 A conventional pixel array. 13

1.6 Pixel array with a separate ADC array. 14

1.7 Pixel array with multiplexed ADCs. 15

1.8 Conceptual diagram of FDM readout where a bank of pixels shares a single ADC. 18

2.1 System-level block diagram of our 8×16 FDM-based readout system. . . . 26

2.2 Signal flow through the pixel from the sensor input to the mixer output. . 27

2.3 (a) Concurrent pixel signals and (b) spectrum of summed signal. 28

2.4 Pixel front-end model. 29

2.5 Pixel front-end model with noise sources. 32

2.6 ENC contributions from various noise sources. 34

2.7 ENC contributions as a function of input capacitance C_P. 35

2.8 Full-system transfer characteristic simulated using MATLAB model. 36
2.9 Short-time Fourier transform of the summed output signal. 38
2.10 Peaks detected in STFT. 39
2.11 Krummenacher CSA with active feedback [51]. 41
2.12 CSA with tunable feedback resistance. 42
2.13 Opamp used in our CSA. 43
2.14 Simulated closed-loop magnitude response of the CSA transimpedance. . . 45
2.15 Simulated CSA pulse response at various feedback resistance tuning currents for an input-current pulse beginning at 0.1 μs with $t_p = 150$ ns. 45
2.16 Input-referred noise charge PSD of the CSA. 46
2.17 Integrated noise charge power of the CSA. 46
2.18 Simulated CSA loop transfer gain and phase. 47
2.19 Simulated CSA transfer characteristic and charge-to-voltage gain. 48
2.20 Mixer circuit. 49
2.21 Active lowpass filter stage. 50
2.22 Simulated mixer output and LPF output pulses. 51
2.23 Summing stage followed by a cascade of open-loop amplifiers. 53
2.24 Simulated time-domain summed output signal and its spectrum from eight coincident pulses. 54
2.25 1.5-bit pipelined ADC architecture [59]. 57
2.26 A single 1.5-bit pipelined analog-to-digital converter (ADC) stage [58] . . . 58
2.27 Two-stage OTA for pipelined ADC stage. 61
2.28 CMFB circuits used for the pipeline stage OTA. 63

2.29 Simulated loop transfer gain and phase of the 2× gain stage with $\beta = \frac{1}{2}$. . 64
2.30 Switched-capacitor network feeding the comparator [58]. 66
2.31 StrongArm comparator. 67
2.32 Simulated comparator latch delay. 68
2.33 Differential mux DAC. 69
2.34 Full-adder bank in decoder. 70
2.35 Least-significant bit generation. 70
2.36 Full mirror adder circuit. 71
2.37 Simulated ADC differential non-linearity. 72
2.38 Simulated ADC integral non-linearity. 72
2.39 Simulated output spectrum of the ADC for a full-scale sinusoidal input. . . 73
2.40 Simulated SNDR and ENOB of the ADC vs. input signal frequency for a full-scale input. 74
2.41 Voltage regulator. 76
2.42 Simulated voltage regulator output vs. dc load current for a target V_{CM} = 1.1 V. 76
2.43 Simulated voltage regulator output for a load current pulse with a 100 ps duration. 77
2.44 Bias-generation circuit for the OTA in the ADC. 78
2.45 Non-overlapping clock generator used to drive the ADCs. 79
2.46 CSA circuit with test input. 80
2.47 Full chip layout. 83
2.48 Pixel layout. 85

2.49 Pixel array layout. 86
2.50 ADC layout. 87
2.51 Results from full-chip post-layout ADC functional simulation. 88
2.52 STFT of the simulated ADC output for pulse inputs on a full bank of pixels. 89

3.1 (a) A microscope image of the fabricated ROIC and (b) the ROIC in its package. 92
3.2 Printed-circuit board for testing. 93
3.3 Variable bias current supply configuration. 95
3.4 Measured CSA output for a 15 ke^- input applied at time 1 μs. 97
3.5 Measured CSA transfer characteristics for each test pixel. 98
3.6 Measured CSA output noise histograms for each test pixel. 99
3.7 Measured input-referred charge noise PSD of the CSA. 100
3.8 Measured test bank output spectrum. 101
3.9 Measured transfer characteristics for each pixel in the test bank. The dashed line is a linear fit. 102
3.10 Measured ADC output with a 996 kHz sinusoidal input. 104
3.11 Measured ADC output spectrum from a 996 kHz sinusoidal input. 105
3.12 Measured ADC output spectrum from a 996 kHz sinusoidal input, zoomed into the harmonic content. 106
3.13 Measured SNDR and SNR of the ADC vs. input amplitude. 107
3.14 Measured fundamental, THD, and noise components plotted against input amplitude. 108
3.15 Detected pulse peaks in the STFT of the measured ADC output with a stream of input pulses. 110

3.16 Measured system-level transfer characteristic. 111

A.1 Pin locations. 130

B.1 Bonding diagram. 132

List of Tables

1.1 Specifications for a line-scanning system for X-ray mammography. 22

1.2 The targeted performance of our work in comparison to previous SPC ROICs. 23

2.1 Opamp parameter summary. 44

2.2 Mixer driver parameter summary. 49

2.3 Active LPF parameter summary. 51

2.4 Summing block parameter summary. 54

2.5 Summary of the simulated power consumption in the pixel circuits. 55

2.6 OTA parameter summary. 62

2.7 OTA specification summary and simulated results. 65

2.8 StrongArm comparator parameter summary. 67

2.9 ADC bias-generation circuit parameter summary. 78

2.10 Power domains. 84

2.11 Simulated performance of our ROIC in comparison to previous works. . . . 90

3.1 Measured performance in comparison to previous works. 112

A.1 Pin list. 129

C.1 Control bit map for the scan chain. 133

List of Abbreviations

a-Se amorphous selenium 1, 4, 18–20, 29, 41, 113

ADC analog-to-digital converter xi, 11–15, 17, 20, 25, 26, 30, 31, 35–37, 55, 56, 58, 59, 64, 69, 71, 73–77, 79–88, 93–96, 103, 106, 108–110, 113, 114

AFE analog front end 12

CDM code-division multiplexing 16

CM common-mode 62, 94

CMFB CM feedback 62

CMOS complementary metal-oxide-semiconductor 1–3, 5, 20, 21, 25, 28, 59, 74, 91, 111, 113

CSA charge-sensitive amplifier 3, 6, 7, 11, 12, 21, 25, 26, 28, 31, 33, 36, 39, 40, 43, 44, 47, 48, 80, 84, 89, 97–101, 109, 111, 112

CT computed tomography 1, 9, 20, 22, 113

DAC digital-to-analog converter 55–59, 68, 75, 108, 109, 114

DAQ data-acquisition system 16

DNL differential non-linearity 71

DNW deep n-well 84, 86

DSP digital signal processing 21

ENC equivalent noise charge 10–12, 21, 34, 37, 44, 89, 100, 110, 111, 113

ENOB equivalent number of bits 73, 74, 107

ESD electrostatic discharge 31, 84

FDM frequency-division multiplexing 16–18, 20, 25, 28, 111, 113

FFT fast-Fourier transform 36

I2C inter-integrated circuit 95

IC integrated circuit 49, 95, 96

INL integral non-linearity 71

LO local oscillator 26, 49

LPF lowpass filter 25, 28, 37, 48, 50–52, 84, 94, 114

LSB least-significant bit 59, 69, 71

MIM metal-insulator-metal 59, 75, 83

MOM metal-oxide-metal 21, 31

MPPC multi-pixel photon counter 20, 29, 31, 94

MSB most-significant bit 56, 69

OTA operational transconductance amplifier 30, 43, 60, 63, 64

PCB printed-circuit board 24, 91–96

PDK process design kit 21, 31, 32, 59

PET positron emission tomography 16

PSD power spectral density 32, 33, 44, 100

QFP quad flat package 91

ROIC readout integrated circuit 1–6, 9, 11, 12, 17, 18, 20–22, 24, 25, 49, 75, 77, 80, 82, 84, 87, 89, 91–96, 109, 111–113, 126

SC switched-capacitor 57, 65, 66, 68, 79, 83

SNDR signal-to-noise-and-distortion ratio 73, 106, 107, 110

SNR signal-to-noise ratio 5, 11, 16, 21, 59, 106, 107

SPC single-photon-counting 1, 5, 6, 8, 11, 13, 20, 22, 113

STFT short-time Fourier transform 37, 88, 109

TDM time-division multiplexing 8, 15, 16

THD total harmonic distortion 107

USB universal serial bus 96

Chapter 1

Introduction

X-ray radiography is a ubiquitous diagnostic tool in modern medicine. However, exposing patients to radiation requires careful consideration when weighing diagnostic benefits against the risk of adverse effects caused by an excessive radiation dose. This is critical for regular screening procedures of otherwise healthy individuals, such as mammography screening [1]. To this end, it is clear that in the development of X-ray imaging systems, radiation dose efficiency must be prioritized. Fortunately, with the advent of digital X-ray imaging, based on solid-state detectors, image data can be collected, stored, and analyzed in greater quantities and with greater detail than with traditional film-exposure methods, allowing for better overall risk mitigation.

To enable state of the art digital imaging, co-optimized sensor materials and readout integrated circuits (ROICs), built using complementary metal-oxide-semiconductor (CMOS) technology, are required to provide the best performance at a given radiation dose. In this thesis, we present the design and experimental characterization of a single-photon-counting (SPC) X-ray imager ROIC for use in mammography and computed tomography (CT). Our imager is designed to interface with an amorphous selenium (a-Se) X-ray sensor, and takes advantage of multiplexing circuit techniques to improve spatial and spectral resolution. In this chapter, we introduce SPC X-ray imagers and compare them to integration-mode

imagers. We then cover conventional design architectures, along with performance metrics and potential improvements. Finally, we derive target specifications for our ROIC design.

1.1 X-Ray Imagers

X-ray imaging is a process in which an object is placed between a radiation source and a two-dimensional (2D) radiation sensing device. As radiation passes through the object, some of the energy is attenuated, creating a shadow signal received by the sensor. Historically, this sensor was a film that would be exposed to the incoming X-ray photons. However, contemporary systems achieve improved results using digital X-ray imagers, where images are formed through electronic readout of discrete pixel sensors instead of continuous film.

1.1.1 CMOS Direct-Conversion Digital X-Ray Imagers

As digital imagers have evolved over the years, flat-panel detectors using thin-film transistor technology have taken the lead in clinical settings. Although these devices are suitable for manufacturing large-area panels, a shift from flat-panel detectors to hybrid detectors, where CMOS ROICs are combined with various X-ray sensor materials, is underway [2]. In Figure 1.1, the structure of a hybrid CMOS detector is shown. Layered on top of the ROIC is an X-ray sensor with a conductive electrode, such as gold, on the surface. This electrode is used to apply a high-voltage bias, establishing a large electric field throughout the sensor. At the interface between the ROIC and the sensor is another set of electrodes used to connect the two and collect the input charge.

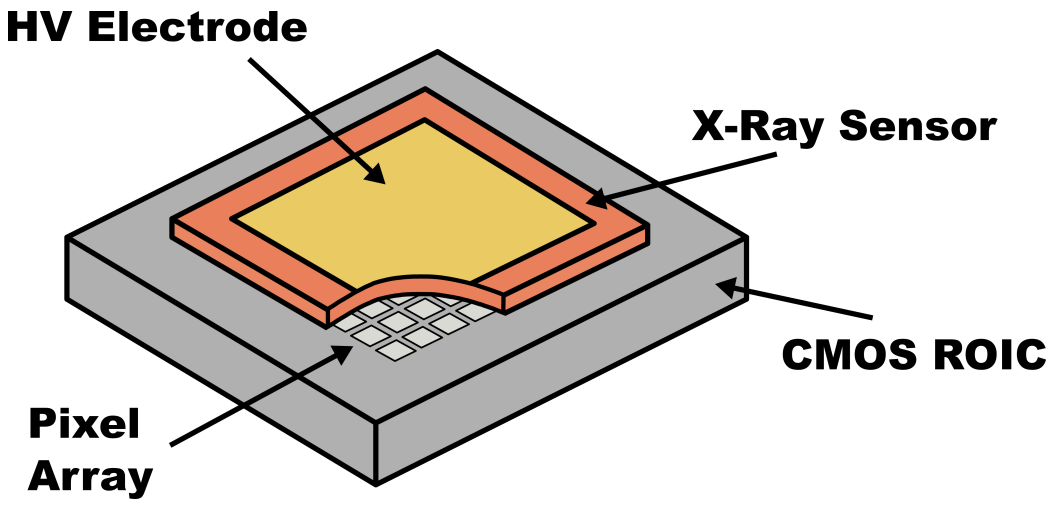


Figure 1.1: Structure of a hybrid CMOS X-ray imager.

CMOS X-ray imagers consist of a large array of pixel sensors similar to a visible-light camera. The functional concept of one of these pixels is shown in Figure 1.2. Incident X-ray photons are absorbed by the X-ray sensor, generating a cluster of electron-hole pairs which are carried to the readout electrodes at the ROIC interface. The charge carriers are then injected into a charge-sensitive amplifier (CSA) to produce a voltage output pulse which is passed on for further signal processing. This sensing method is known as direct conversion.

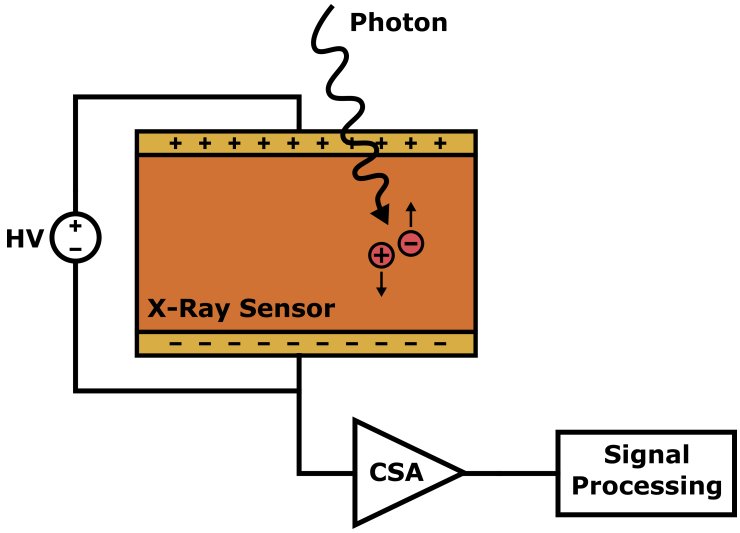


Figure 1.2: Functional concept of a direct-conversion X-ray detector pixel.

1.1.2 X-ray Sensor Material Properties

Direct-conversion X-ray imagers come in various forms, largely dependent on the properties of the sensor material. One important property is the absorption depth for a given photon energy. Silicon, for example, has a much larger absorption depth than higher-atomic-number photoconductors like cadmium telluride (CdTe) or a-Se. This is a disadvantage since a much thicker sensor layer is required to detect incoming photons, and becomes impractical to manufacture and interface with a ROIC. However, solutions for using silicon have been designed for strip detectors [3]. These are used in line-scanning systems where a one-dimensional (1D) sensor array is repeatedly scanned as the object is moved gradually through the radiation field, ultimately generating the data for a 2D image [4, 5]. In this case, the silicon wafer is used with its edge oriented toward the X-ray source, allowing for deeper photon penetration within the material.

Another key property of the sensor material is the amount of photon energy required to create an electron-hole pair. This quantity is defined as the ionization energy $W_{\pm}$ in

units eV/e^-. This energy varies across materials, and is also dependent on the internal electric field strength. Increasing ionization energy can help improve sensor performance by increasing the input signal to the ROIC, but a limit will be reached where the high-voltage bias causes a breakdown in the material. Another drawback to having a large electric field in the sensor stems from dark current, which is the dc current that flows through the sensor despite the absence of radiation. Dark current varies across X-ray sensors due their resistivities and charge-trapping properties, and can limit performance in some systems.

Specifications for digital X-ray imagers vary across the fields of medical imaging, particle physics, crystallography, security, and others. However, many of the same principles apply to the design of CMOS ROICs for direct-conversion detectors, and the following discussion is generalizable across many fields.

1.1.3 Integration-Mode vs. Single-Photon-Counting Imagers

In digital X-ray imagers, there are two main types of sensing implemented by the ROIC: integration mode and SPC mode. Integration-mode detection is a process where photon-induced charges are collected for a specific period of time, usually by integrating the total charge onto a capacitor. Each of these time periods represents a single frame in which the incoming photon energy is accumulated. At the end of the period, the total charge is processed by downstream circuits and the integration begins again for the next frame.

On the other hand, with SPC, each charge packet produced by a photon is processed individually. In this case, data can be read asynchronously in an event-driven fashion, offering the possibility of higher overall throughput compared to integration-mode detectors that have a fixed frame rate [6].

One significant drawback to integration-mode detection is the effect of dark current. Since charge integration operates on a fixed frame period, any dark current from the sensor will be integrated, in addition to the photon-induced signals. This has the overall effect of reducing the signal-to-noise ratio (SNR), degrading the image quality.

In an SPC detector, photon-induced voltage pulses are only counted if the voltage peak exceeds some desired threshold. This threshold is normally set above the level of dark-current-induced voltage output to avoid counting it as an excess photon "hit". The threshold also rejects other sources of injected charge, such as thermal and shot noise associated with the electronics and sensor. Noise rejection in this manner is one of the primary advantages that SPC detectors have over their integration-mode counterparts, as front-end noise is a major limiting factor in the overall system performance.

Another advantage of SPC imagers is that they enable spectrographic imaging, where photons are differentiated based on their energy using multiple thresholds. This is useful in medical imaging, where it offers the possibility of distinguishing between bones and soft tissues [7], since these materials attenuate incident photon energies differently. In integration-mode detectors, when the charge packets of photons with differing energies are integrated over the same period, the contrasting information between them is lost as their energies are summed together. With multi-spectral detectors, the extra information can be used in image processing algorithms, such as contrast-enhanced imaging [8], for improved image construction. With these use cases and more, the trend towards spectrographic imagining in SPC detectors can be seen in several medical and analytical disciplines [2].

The noise rejection and improved image quality provided by spectrographic SPC detectors can also be viewed as an increase in dose efficiency, which is a relative performance increase for a given dose [9, 10]. As mentioned earlier, for clinical applications, improved dose efficiency is one of the primary goals for new imaging systems, making SPC the superior choice for these applications.

1.1.4 Conventional Single-Photon-Counting Architectures

The basic structure of a conventional SPC readout pixel is shown in Figure 1.3. When photon absorption occurs in the sensor, the resulting charge packet $-Q_{IN}$ flows through the input pad interfacing the collecting electrode of the sensor and ROIC with the pixel's input CSA (or "charge preamp"). Assuming the CSA contains an ideal amplifier, and

momentarily ignoring R_{FB}, $-Q_{IN}$ will be completely integrated onto feedback capacitor C_{FB}, causing a step in the output voltage V_{OUT} proportional to Q_{IN}, such that $V_{OUT} = \frac{Q_{IN}}{C_{FB}}$, where we have taken $V_{REF} = 0\,\text{V}$. However, if we now consider R_{FB}, V_{OUT} will be discharged according to the time constant $\tau_f = R_{FB}C_{FB}$. The resulting V_{OUT} is therefore a voltage pulse with peak amplitude proportional to the incident photon energy. The amplitude of this voltage pulse is then compared to a threshold voltage V_{TH} to determine if it is energetic enough to have been produced by an absorbed photon. The comparator output then increments a digital counter which stores the total number of photon hits for the pixel over a specified period of time.

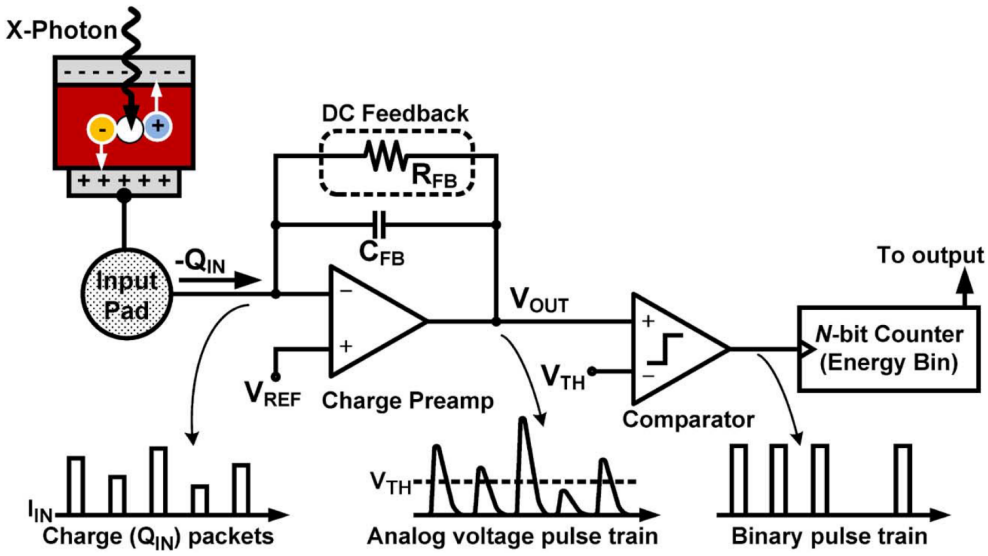


Figure 1.3: Conventional SPC pixel circuit [7].

In some cases, a shaping circuit, usually in the form of a band-pass filter, is placed after the CSA to optimize the pulse duration and bandwidth for count rate and noise performance [11, 12].

The architecture in Figure 1.3 can be easily adapted to multi-spectral sensing by adding comparator and counter pairs in parallel with the original devices. The added comparators

allow the use of different threshold voltages, where each counter is assigned to a unique energy bin. This method is used by several groups to enable spectrographic imaging [13, 14, 15, 16, 17]. An alternative approach, known as "time-over-threshold", has also been adopted by some groups [18, 19, 6, 20, 21]. In this method, an oscillator is enabled while the voltage pulse remains above V_{TH} and the number of clock cycles is counted. In this case, the number of cycles corresponds to the total energy of the incident photon. A drawback, however, is that more digital circuitry per pixel is required compared to the method in Figure 1.3.

Other variations on the general architecture have also been published. For example, an analog counter was used in place of the digital counter [22]. Another approach borrowed from wireline transceiver design was tested to increase pixel count rate by using an inter-symbol interference cancellation technique [23]. In addition, the problem of charge sharing, which occurs when a charge packet disperses and spreads its energy across multiple pixels, was addressed with added arbitration and correction circuitry [16, 24, 25].

One of the main drawbacks to many of these designs is the need for time-division multiplexing (TDM) when reading out the counters from each pixel in an array. Often, the counter outputs are multiplexed to an output bus that is much smaller than the number of pixels, therefore, the acquisition operation needs to pause while the data is read externally for post processing. This bottleneck can limit use for real-time applications, such as angiography, and can require more complex high-speed transceiver designs to match the high data rates required to send data off chip.

1.2 Performance Metrics

Despite the range of applications for SPC imagers, a number of key performance metrics are common to most designs. The following sections present an overview of these metrics.

1.2.1 Count Rate

In most X-ray-radiography applications, the relatively-high radiation intensity means that the ROIC circuits must process input pulses at high speed. Maximum input flux for mammography and CT are on the order of $10^8 \frac{\text{photons}}{\text{mm}^2 \cdot \text{s}}$ [9, 26]. If a photon arrives at a pixel before the previous one has finished being processed (an event known as "pile up"), the energy information can be corrupted and the front-end electronics can saturate. Photon arrival rates follow a Poisson distribution [27] and modelling approaches have been developed to predict pixel output count rates based on input flux. Using these models, the "dead time" t_d for the readout circuit can be specified. Dead time is the period required for a front-end circuit to process a photon signal and return to baseline in order to receive the next charge packet.

Designers commonly choose between the paralyzable and non-paralyzable models to determine the acceptable t_d for an input flux-handling requirement [28]. Pixel output count rate m in the non-paralyzable model, is given by

$$m = \frac{n}{1 + n \cdot t_d}, \tag{1.1}$$

where n is the pixel input count rate (equal to the input flux normalized to the pixel area). In this model, a photon arrival during t_d is not counted, but this arrival does not prolong t_d.

In the paralyzable model, the effective t_d is extended when an early photon arrives. This is modelled by

$$m = ne^{-nt_d}, \tag{1.2}$$

and matches more closely with the conventional readout architecture described previously. In this case, an early photon arrival would add to the height of the voltage pulse and extend the time for it to return to baseline. Other models have been proposed for various applications, including hybrid combinations of these two [29, 27]. However, the paralyzable model is suitable for most conventional front-ends.

In Figure 1.4, the behaviour of both models is shown along with the ideal linear curve. For the paralyzable model, m tends to decrease after a certain point, whereas in the non-paralyzable model, m tends toward an asymptote. To specify t_d using either of these models, an acceptable loss is defined by $\frac{m}{n}$, allowing the designer to solve for t_d. Another important consideration is that n is normalized to the size of the pixel, meaning that for a constant input flux, smaller pixels can enable longer t_d and thus relax other circuit constraints.

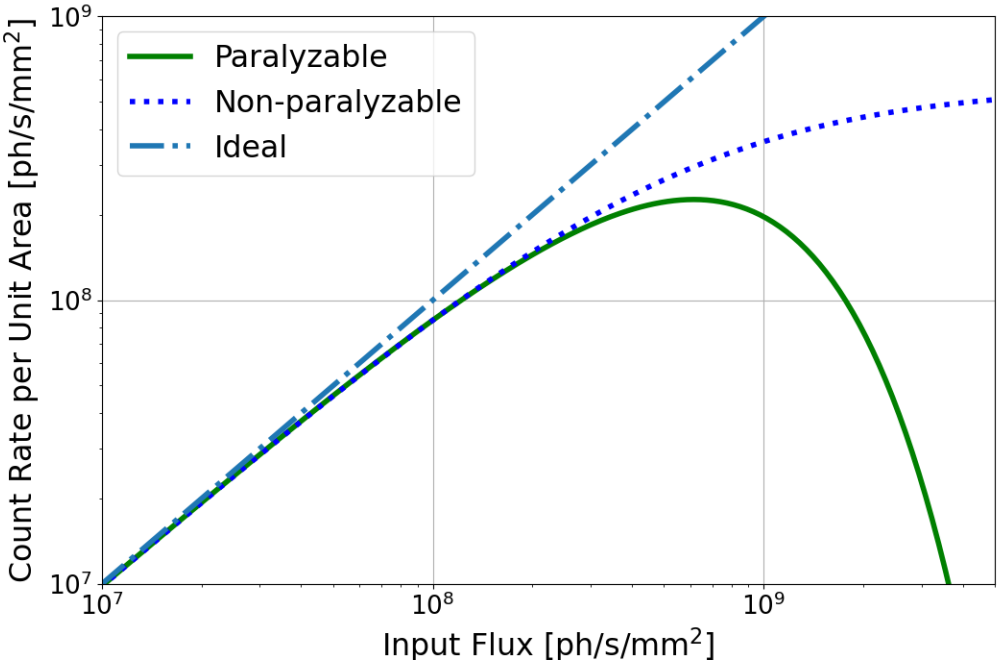


Figure 1.4: Comparison of count rate models.

1.2.2 Noise

Noise limits how low V_{TH} can be set at the comparator input before the comparator begins to register a large number of false photon hits. For radiation detectors, noise is usually quantified as an equivalent noise charge (ENC), which is defined as the amount of charge

injected at the input such that the SNR is 0 dB [12]. In other words, ENC is the input-referred noise of the detector circuits expressed as charge (usually given in electrons). When $W_{\pm}$ of the sensor is known, ENC can also be expressed as an energy.

The front-end CSA is the dominant noise source in ROIC circuits. Often, the input transistors of the CSA make a significant contribution, while R_{FB} can also be a significant thermal noise contributor. Since a larger R_{FB} contributes less input-referred noise, it follows that a longer t_d is desired to reduce the ENC. As mentioned previously, for a certain count-rate specification, a longer t_d is realized as pixel dimensions are decreased, indicating again that smaller pixels are advantageous.

1.2.3 Spatial Resolution

Pixel size also affects the spatial resolution of the detector. Resolution requirements vary across different applications. In medical imaging, chest radiography and fluoroscopy generally use pixel sizes around $200 \times 200\,\mu\text{m}^2$ or larger, while mammography pixels are as low as $50 \times 50\,\mu\text{m}^2$ [26]. However, smaller pixels can still lead to improvements, since the extra data obtained from higher-resolution arrays can support post-processing algorithms for charge-sharing correction or other image-enhancing techniques.

1.2.4 Spectral Resolution

The spectral (or energy) resolution of an SPC system is quantified by the number of energy bins it has available to discriminate between photon-energy levels. It has been shown that having just one extra bin over a conventional system can enable better image processing through the use of techniques like dual-energy subtraction and tomosynthesis [30, 5, 8]. However, adding bins has the potential to unlock more post-processing flexibility. Ideally, each pixel would have a medium-to-high-resolution ADC, instead of a small number of comparators and counters. This way, the CSA analog output pulses could be fully digitized and processed off chip. This approach was used previously, but the extra area required to

include an 8-bit ADC resulted in very-large-area pixels ($756 \times 800\,\mu\text{m}^2$), severely degrading spatial resolution [24].

Another measure of energy resolution is the minimum width of the energy bins. For a ROIC with a certain ENC, the minimum separation between thresholds can be taken as the ENC. This represents the standard deviation (rms value) of the noise, multiplied by some factor depending on the desired confidence level.

1.3 Techniques for Improved Resolution

For the conventional pixel array depicted in Figure 1.5, each pixel contains an input pad that interfaces with the X-ray sensor, an analog front end (AFE) which includes the CSA and any other analog-signal-conditioning stages, and an ADC as implemented by the comparator in Figure 1.3.

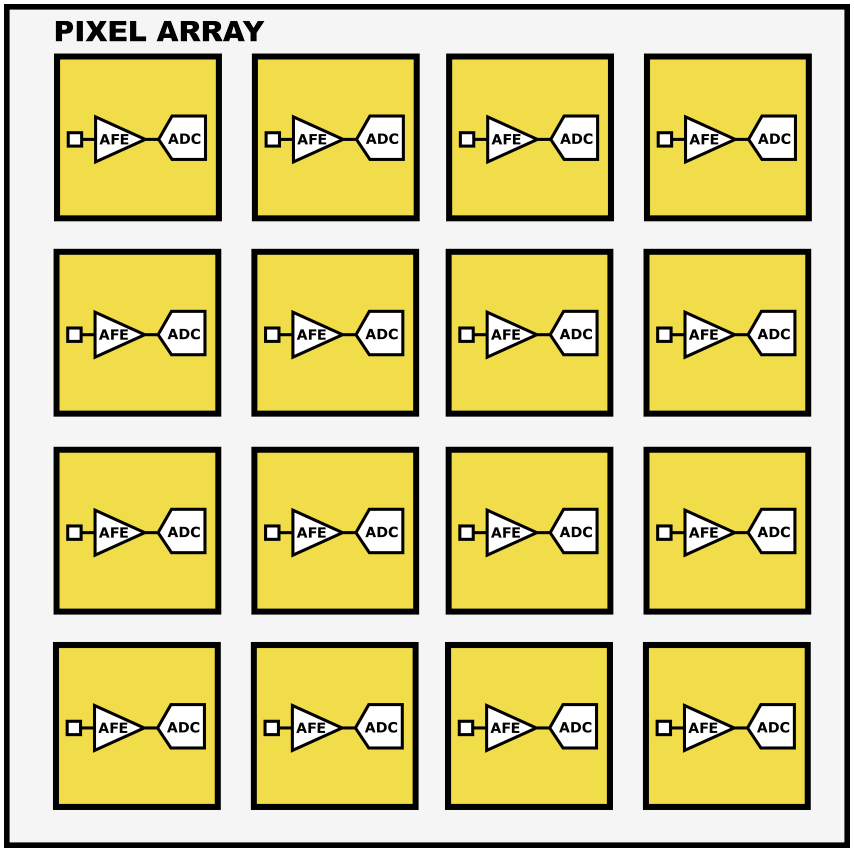


Figure 1.5: A conventional pixel array.

As we have seen, smaller pixels can help improve spatial resolution, count rate, and noise performance in an SPC detector. Consequently, it is important to minimize the overall pixel circuit area. Ultimately, to achieve a minimum pixel size while maximizing energy resolution, the digitization block for each pixel would be placed outside the main array area. Figure 1.6 illustrates this concept where an $N \times N$ pixel array is coupled by $N \times N$ interconnection lines to the corresponding ADC array. In this case, higher-resolution ADCs could be used to measure more energy bins while negating their impact on pixel size. However, as the number of pixels in the array scales up, the ADC array would need to do the same, and could introduce excessive parasitic and cross-talk effects due to the interconnection between the pixel array and ADC array.

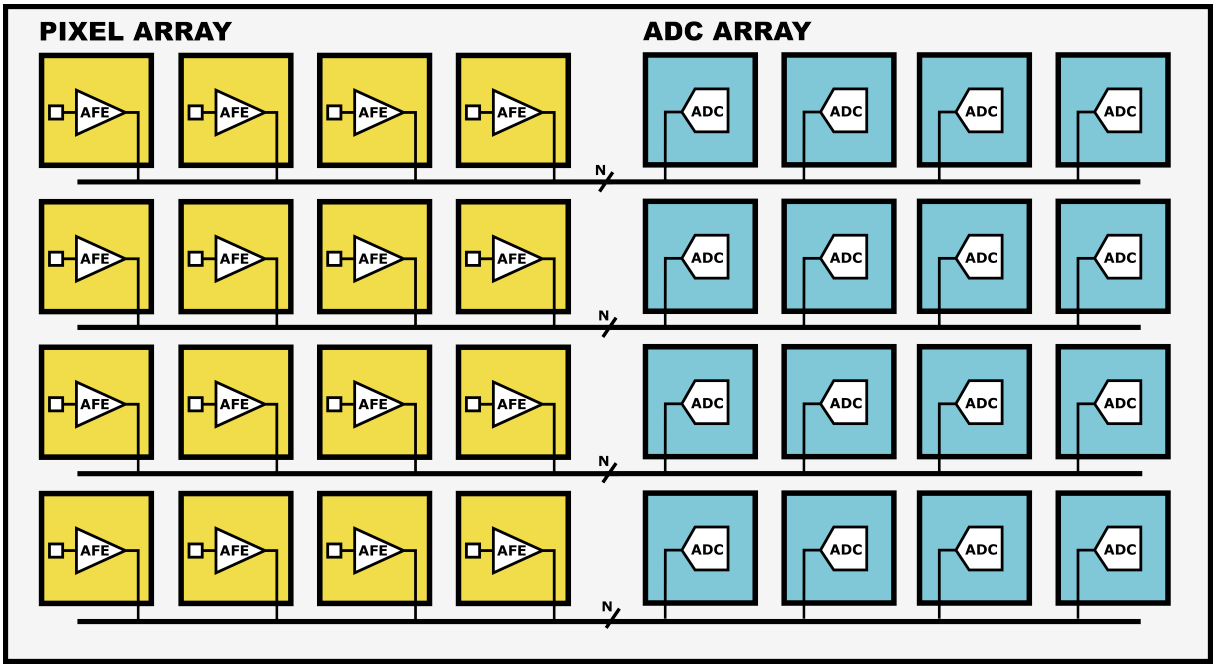


Figure 1.6: Pixel array with a separate ADC array.

1.3.1 Resource Sharing

In order to address these challenges, it is possible to shift the design focus to a resource-sharing concept, where a single ADC is shared by multiple pixel outputs. Resource sharing is generally achieved by multiplexing pixel output signals to an ADC, as shown in Figure 1.7.

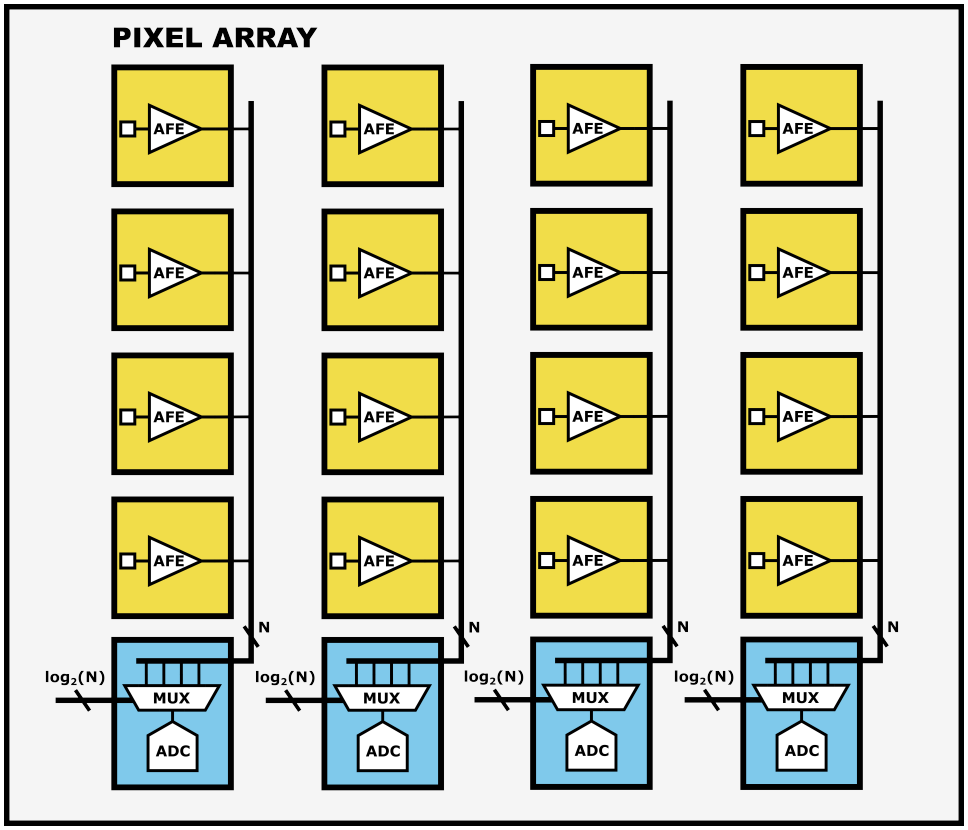


Figure 1.7: Pixel array with multiplexed ADCs.

A natural first choice to investigate for this multiplexing task is TDM. However, for a group of N pixels sharing an ADC, TDM requires that only one pixel output is connected to the ADC at a time. For a multiplexing period t_m, this means that each pixel is only enabled for $\frac{t_m}{N}$ each period. This process has the effect of creating a dead time $t_{d,TDM} = t_m(1-\frac{1}{N})$ that scales up with the number of pixels grouped together in a bank. If the pixel output signals were digital, it would be possible to momentarily store their values while an arbitration circuit controls access to the output bus [6]. However, this is not feasible with analog signals since the goal is to digitize the entire output pulse at medium-to-high resolution. This would require a local ADC, defeating the purpose of the multiplexing scheme.

Other analog multiplexing solutions for similar pixel-based positron emission tomography (PET) detector systems have been proposed [31, 32, 33]. These architectures use a shared four-wire output bus, fed by a network of scaled capacitors, connected in series with the pixel outputs. Using appropriate capacitor ratios, the signal that appears on the output bus is decoded to find the coordinates of the originating pixel. Despite the reduction in wiring, there are several drawbacks to this approach. As the array dimensions increase, a larger unit capacitor is needed to satisfy the required capacitor ratios without mismatch errors. In addition, since the output bus is shared, it is only possible to process one pixel signal from the array at a time. While this may be a practical solution for certain applications, it will not work for the required count rates in X-ray radiography.

Code-division multiplexing (CDM) has also been used for integration-mode sensors [34, 35]. In this method, a bank of input pixel signals are summed after being multiplied by a coding vector at each time step. For N pixels, there are N different coding vectors, and thus it takes N time steps to fully code the signal. After multiplying the output by the inverse of the coding matrix, the recovered vector represents the $N-$point moving average of each pixel output. This is an effective method for improving SNR and reducing the number of interconnect wires in the array. However, due to the inherent averaging, it is not suitable for photon-counting systems.

1.3.2 Frequency-Division Multiplexing

Frequency-division multiplexing (FDM) is a more promising approach for resource sharing compared to TDM, CDM, and capacitive multiplexing. This method has been used for a set of discrete radiation detectors sharing a single data-acquisition system (DAQ) input channel [36, 37]. In these systems, the sensor output pulses are passed through a resonant filter tuned to a specific frequency. The time-domain output of the filter is a decaying sinusoidal pulse that is then summed with the other pixel signals, each tuned to its own frequency. The summed signal is then digitized, making recovery of the original signals possible by applying a bandpass filter around the resonant frequency. As long as the

spacing between frequencies is sufficient to minimize overlap, a high-order filter can be used to recover the spectrum of the original pulse. Furthermore, the total energy of the pulse can be recovered by integrating the Fourier transform magnitude over $f_c \pm f_{BW}$, where f_c is the carrier frequency, and $f_{BW} = \frac{1}{2\pi\tau_f}$ is the pulse signal bandwidth. A multi-spectral measurement system can be implemented using this technique since the energy of the input pulse is proportional to the energy of the incident photon.

More recently, this method has been implemented for biopotential acquisition ROICs [38, 39, 40]. In these works, the resonant filter is replaced by a multiplier and a clock is provided to mix the pulse signal up to the carrier frequency. This is a favourable alternative, as a resonant analog filter may require the use of an inductor or gyrator and would likely consume more power than a simple passive-mixer implementation. In Figure 1.8, the FDM concept is illustrated for a bank of pixels, each with its own mixer, and a summing block placed before a shared ADC. Signal spectra before and after the pixel signals are mixed, and after the mixed signals are summed, are also shown.

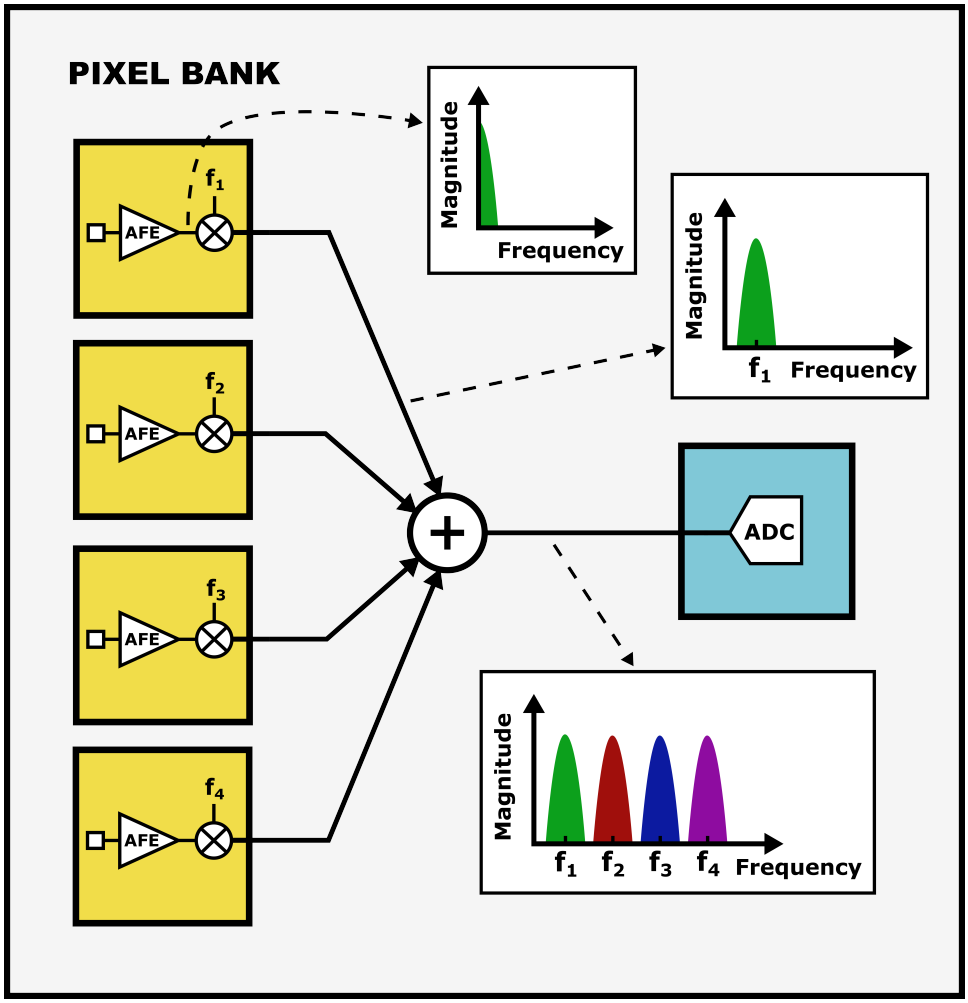


Figure 1.8: Conceptual diagram of FDM readout where a bank of pixels shares a single ADC.

1.4 Imager Design Overview

In this section, we outline our ROIC design for a multi-spectral X-ray imager with FDM readout. Our target application is a line-scanning system, similar to those used for spectral mammography [4, 5], and our target X-ray sensor is a-Se.

1.4.1 Amorphous Selenium Material Properties

We require a-Se sensor properties in order to derive electrical specifications. Many radiation-detection systems have used a-Se due to its relatively-low absorption depth for X-ray photons and economical deposition on large areas using thermal evaporation [41]. Other advantages of a-Se include relatively-low dark current, especially when an appropriate charge-injection blocking layer is used at the electrode interface [42]. A-Se also exhibits high inherent spatial resolution due to the low energy of K-fluorescent photons. These photons can be emitted at the incident X-ray-photon location and collected by a neighbouring pixel, effectively reducing spatial resolution by spreading the input energy in the spatial domain [26].

Despite these favourable properties, a-Se has some drawbacks. Due to its low charge-carrier mobility, particularly for electrons, signal rise times are slow compared with other sensors and, therefore, complete collection of induced charge may not be possible. Charge trapping can also be a problem for slow-moving carriers, creating a lag effect in the output signal, and increasing the probability of pile up. Moreover, the charge-conversion efficiency of a-Se is not as high as in comparable sensor materials. For a-Se biased by a 10-V/μm field, $W_{\pm} \approx 45\,\mathrm{eV/e^-}$, while Si, CdZnTe and HgI_2 all have $W_{\pm} \approx 5\,\mathrm{eV/e^-}$ [43].

Problems with slow carrier mobility in a-Se have been addressed using unipolar charge sensing. The goal of this method is to prioritize collection of holes over electrons, as holes have a faster carrier mobility in a-Se due to the higher concentration of electron traps. Hole mobility is around $0.14\,\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, while electron mobility is $4 \times 10^{-3}\,\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ [26]. We consider the concept of a weighting potential based on the Shockley-Ramo theorem. The weighting potential in a material is dependent on the geometry of the sensor and can be used to calculate the total induced charge on the collecting electrode based on the depth of photon absorption. If the weighting potential is perturbed such that it is no longer a function of detector thickness, but is concentrated close to the collecting electrode instead, then the preferential sensing of holes will be achieved.

Two different methods that have been shown to alter the weighting potential are the

small-pixel effect [44] and the use of a Frisch grid [45, 46]. The small-pixel effect occurs when the pixel-pitch-to-sensor-depth ratio is very small, creating a near-field effect close to the electrode [47, 48]. Use of a Frisch grid structure has been developed for a multi-pixel photon counter (MPPC) [26], where a metal grid is added to the sensor material in close proximity to the electrodes. The grid is also biased in order to increase the local electric field density, ensuring fast collection of holes. The measured rise time of the induced charge was 150 ns, a significant improvement over the $> 1\,\mu$s times recorded for a standard a-Se sensor [26].

Another important consideration when using a-Se is that crystallization is possible over time, altering the properties of the material and degrading its sensing performance. Therefore, when a-Se is in contact with the ROIC surface, it is important to prevent excessive heating by the electronic circuits, since this can accelerate the process of crystallization or cause the material to delaminate from the collecting electrodes.

1.4.2 System Specifications

Our prototype ROIC is the first SPC X-ray imager to use FDM for resource sharing among a bank of pixels. Targeting mammography and CT applications, and designed in a 1.8-V supply 180-nm CMOS technology, our ROIC has an 8×16 pixel array, where the eight pixels in each column bank are summed to share a single ADC located at the column edge. Our array size is based on the total chip area budget and the ADC specifications detailed in the next chapter.

As highlighted in the previous sections, pixel size plays a critical role in many of the performance metrics, while specifications for mammography dictate that pixel size should be no larger than $50\,\mu$m. For our design, we aim for a pixel size of $35 \times 35\,\mu\text{m}^2$ to maximize spatial resolution, meet the count-rate target, minimize noise, and potentially take advantage of the small-pixel effect. Our small pixel size is made possible by our system architecture where the shared ADC is located outside the array.

Knowing the pixel dimensions allows us to calculate t_d using the paralyzable model for pile up. Acceptable count rate losses typically vary between 10 % and 30 % [49, 27, 13]. Specifying a 15 % loss for the full input flux of $10^8 \frac{\text{photons}}{\text{mm}^2 \cdot \text{s}}$ and a half-rate loss of 7.8 %, the resulting t_d found from rearranging (1.2) is 1.327 μs.

To derive a specification for ENC, we define a minimum detectable energy by taking three standard deviations σ of the noise. Keeping this minimum below the typical energy level for mammography, which is around 20 keV, an ENC of 133 e^-_{rms} with $W_\pm = 45\,\text{eV/e}^-$ gives a 3σ value of 18 keV for a minimum detectable energy.

In a conventional detector, the energy resolution is defined by the number comparators used in each pixel. Since each comparator has a different threshold, the number of comparators is equal to the number of energy bins resolved in each pixel. For the proposed architecture to be compared with these systems, we require an estimate for the number of energy bins we can resolve. In our ROIC, photon counts are not directly binned on chip as in the conventional case. Instead, analog pulses are digitized and analyzed using off-chip digital signal processing (DSP). To derive an estimate for the effective number of energy bins, the full linear range of input energy is divided by the energy resolution based on the ENC specification. Assuming a linear input range of 8.9 ke^-, or 400 keV, the number of bins is approximately 67. For a conservative target that still outpaces most conventional designs, we specify the number of bins as ≥ 10.

The CSA charge-to-voltage gain is ideally $\frac{V_{OUT}}{Q_{IN}} = \frac{1}{C_{FB}}$ when $R_{FB} \to \infty$. Since t_d depends on $\tau_f = R_{RB}C_{FB}$, and R_{FB} should be large to minimize its thermal noise contribution, it follows that C_{FB} should be minimized for maximum gain and SNR. Using the minimum available capacitance modelled in our CMOS process design kit (PDK), which is a 6.79 fF metal-oxide-metal (MOM) capacitor, the maximum theoretical CSA gain is 23.6 mV/ke^-. Knowing this, we set the minimum gain target to 10 mV/ke^-, accounting for the effect of the time constant associated with R_{FB} and any parasitic loss.

In order to find a maximum allowable power per pixel, we use a simple thermal model of the ROIC to determine that a power density less than 5 W/cm^2 would prevent junction

temperatures from rising by more than 10° C. This is sufficient to avoid unintentional crystallization. Translating this density to the pixel area, the maximum power consumption we can tolerate is 61 μW/pixel.

In Table 1.1, the specifications for a line-scanning system targeting X-ray mammography are summarized. Table 1.2 presents our target ROIC specifications, and compares them to the measured performance from several previous SPC works for various applications, such as CT, dosimetry, high-energy physics experimentation, and security.

Typical Photon Energy Range	20 keV-40 keV
Spatial Resolution	$< 50\,\mu$m
Max Input Flux	$10^8 \frac{\text{photons}}{\text{mm}^2 \cdot \text{s}}$

Table 1.1: Specifications for a line-scanning system for X-ray mammography.

Reference	[50]	[15]	[18]	[14]	[22]	[7]	[13]	**Our Work (Target)**
Year	2012	2010	2011	2012	2011	2013	2016	2023
CMOS Process (nm)	180	130	130	180	180	130	130	180
X-ray Sensor	Si	Various	Si	Si	Si	HgI_2	Si	a-Se
Readout Method	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per bank (FDM)
Array Size	160 × 1	256 × 256	16 × 16	96 × 192	16 × 16	128 × 128	128 × 256	8 × 16
Pixel Size (um^2)	4000 × 25	55 × 55	220 × 220	100 × 100	100 × 100	60 × 60	75 × 75	35 × 35
# Energy Bins	8	2 to 8	16	2	1	3	2	≥10
CSA Gain (mV/ke^-)	2.1	11.4	11	42.5	400	107	50.3	≥10
ENC (e^-_{rms})	214	130	160	168	15	68	123	≤133
Max Input Flux ($photons/mm^2/s$)	170M	87M	∼100M	∼200M	10M	278M	220M	≥100M
Pixel Power (μW)	5000	15	18	23	20	4.6	26	≤61

Table 1.2: The targeted performance of our work in comparison to previous SPC ROICs.

1.5 Thesis Organization

This thesis is organized as follows:

- Chapter 2 discusses the modelling and design of the full system architecture, as well

as the details of the primary circuit blocks. Simulation results are also presented, in addition to the physical circuit layout.

- Chapter 3 describes the design of a printed-circuit board (PCB) for testing our ROIC and presents experimental results from ROIC characterization.
- Chapter 4 concludes the thesis with a summary and suggestions for follow-up work and investigation.

Chapter 2

System Modelling and Design

In this chapter we describe the modelling and design of our proposed ROIC using the TSMC 180-nm CMOS process. We begin with a description of the overall system architecture, highlighting the required circuit blocks, before discussing design considerations and simulation results for the pixel circuits, ADC, and auxiliary circuits in more detail. We then discuss the ROIC layout and present full-system simulation results.

2.1 System Overview

In Figure 2.1, we show a block diagram of our 8×16 FDM-based readout system, illustrating the signal path from X-ray sensor input to digital output. Beginning at the sensor in Row 1 of Column 1, a charge packet, induced by an X-ray photon absorption in the sensor, forms a current pulse i_{in1} that flows into the CSA. The CSA outputs a voltage pulse at V_{o1} that decays fast enough to meet the t_d and count-rate specifications. Following the CSA is a mixer, operating with carrier frequency f_1, that applies a frequency shift to the voltage pulse, which is then passed through a lowpass filter (LPF) in order to attenuate harmonics associated with the mixing process. At this point in the signal path, the up-converted pulse signal is driven through a transconductance (Gm) stage to generate the pixel output

current i_{o1}. This current is then summed with output currents from Row 2 to Row 8, each one frequency shifted to its own unique band. The combined signal i_{sum} is then converted back into a voltage by the I2V block outside the pixel array, and is then fed into an ADC before the resulting digital data is transferred off chip.

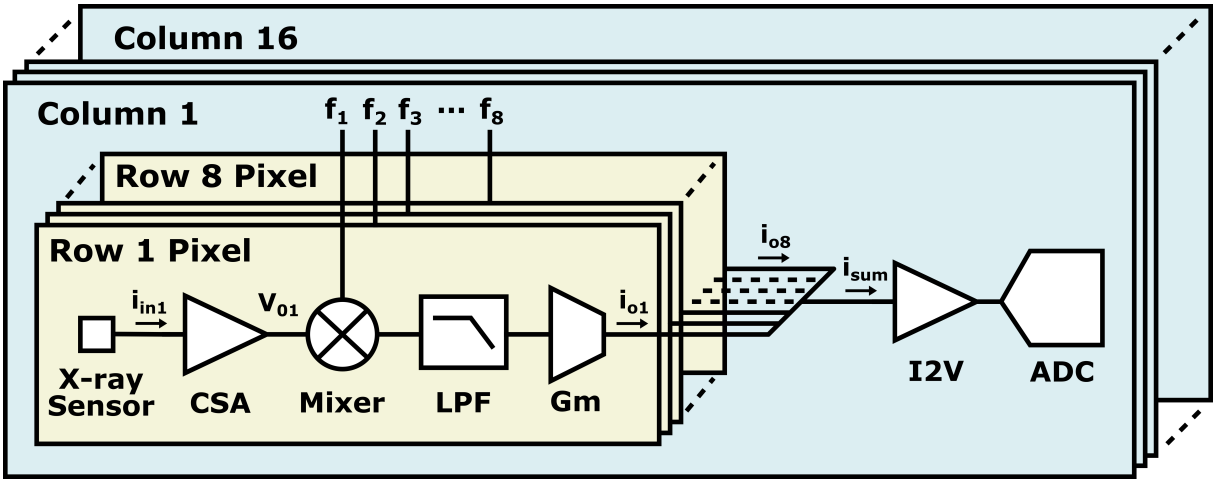


Figure 2.1: System-level block diagram of our 8×16 FDM-based readout system.

While the following sections detail the specifications and signal characteristics for each circuit block, an overview of the signal flow is shown in Figure 2.2, where we plot the waveforms of the signal as it passes from the sensor to the mixer output in one pixel using a MATLAB simulation. This begins with an input current pulse i_{in1} caused by a photon-generated charge packet. Pulse i_{in1} has a duration t_p related to the transport properties of the sensor, while its magnitude is proportional to the total input charge. Next, the CSA voltage output V_{o1} is shown. The exponential rise and decay is dictated by the CSA feedback network that is designed so that V_{o1} returns to zero within t_d. Voltage V_{o1} is then mixed differentially with the local oscillator (LO) at a carrier frequency $f_c = 50\,\text{MHz}$, in this case, to produce the signal in the third plot. The final plot shows the Fourier transform of the upconverted signal, centered around 50 MHz.

As $t_p \to 0$, the Fourier transform of the mixer output $X(j\omega)$ is

$$X(j\omega) = \frac{A}{2j}\left(\frac{1}{j(\omega-\omega_c)+\frac{1}{\tau_f}} - \frac{1}{j(\omega+\omega_c)+\frac{1}{\tau_f}}\right), \tag{2.1}$$

where A is the peak value of V_{o1}, τ_f is the decay time constant of V_{o1}, and $\omega_c = 2\pi f_c$. The magnitude of this response is a pair of Lorentzian pulses centered at ω_c and $-\omega_c$ while the width of the pulse is inversely proportional to τ_f. This illustrates the trade-off between the time-domain pulse duration and the frequency-domain pulse bandwidth [36].

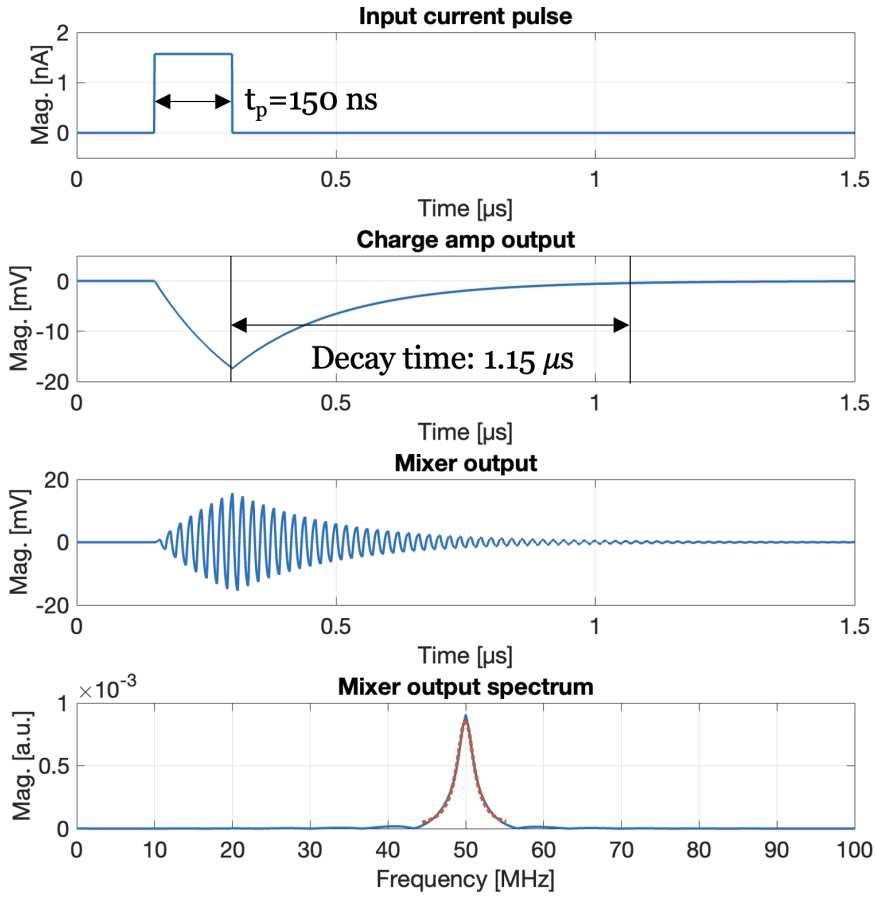
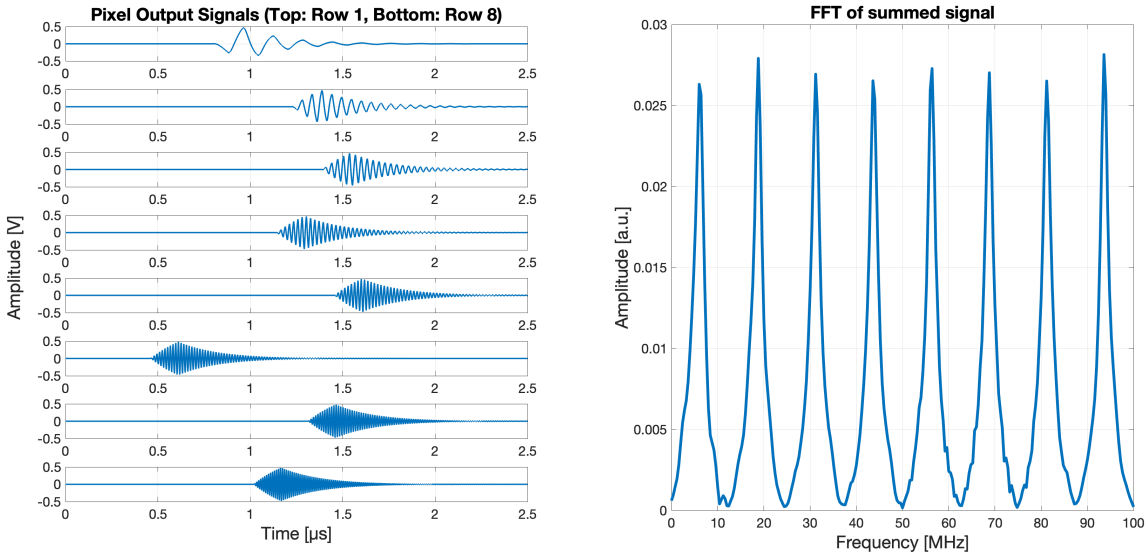


Figure 2.2: Signal flow through the pixel from the sensor input to the mixer output.

To demonstrate and analyze the use of FDM on a full bank of pixels, we create a MATLAB model to generate randomly-timed pulses as inputs to each pixel block, sum their outputs, and plot the spectrum of the combined signal. This model includes an ideal CSA transfer function, mixer, and LPF blocks for each pixel. The results are shown in Figure 2.3(a), which includes time-domain representations of each pulse mixed with a unique f_c. Also shown in Figure 2.3(b) is the spectrum of the summed signal, where the eight pixel channels are evenly spaced, at an interval of 12.5 MHz, over a 100-MHz bandwidth. Generally, more pixels can be summed together when a higher sampling rate f_s is used, since the bandwidth of each pulse remains constant for a given pulse time. Setting $f_s = 200$ MHz is a practical target for our 180-nm CMOS process, and thus each bank can accommodate eight pixels. Disambiguation of the signals for further processing and analysis can be accomplished using a digital bandpass filter for each channel band.



(a) (b)

Figure 2.3: (a) Concurrent pixel signals and (b) spectrum of summed signal.

2.2 Pixel Modelling

To design the pixel blocks from the system diagram in Figure 2.1, we begin by analyzing a simplified model of the the pixel front end in order to derive amplifier and component specifications and satisfy the system-level specifications. Figure 2.4 shows a simplified model which includes a core amplifier with output resistance R_o; a total feedback impedance consisting of R_F and C_F in parallel; an output load capacitor C_L; and an input capacitance C_P, representing the total parasitic capacitance on the input node, composed of wiring and electrode parasitics resulting from the physical layout. Capacitor C_P also includes the sensor capacitance which varies depending on grid layer proximity, in the case of a unipoloar charge-sensing MPPC or a-Se thickness in a standard hybrid detector.

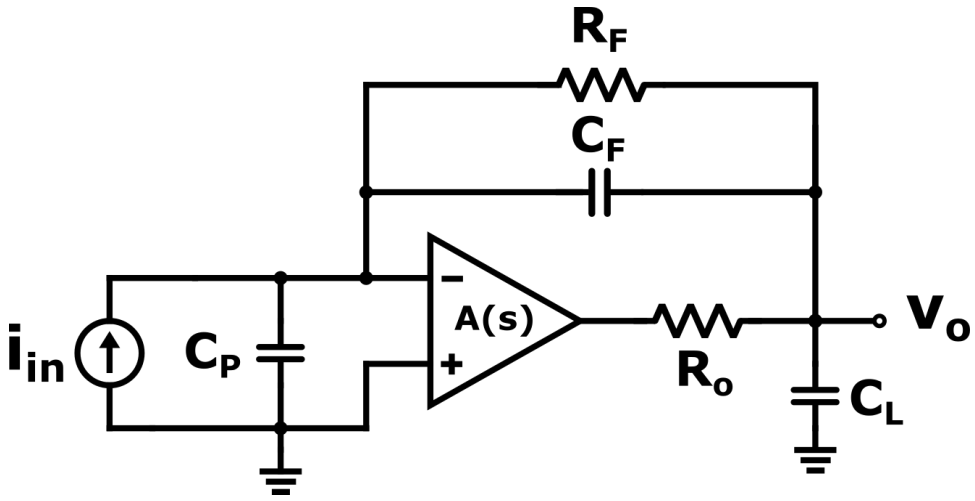


Figure 2.4: Pixel front-end model.

For this analysis, the amplifier is modelled with the single-pole transfer function $A(s)$ given by:

$$A(s) = \frac{A_o}{1 + s\tau_a}, \tag{2.2}$$

where A_o is the open-loop dc voltage gain and τ_a is the time constant of the pole. We also define the gain bandwidth product of the amplifier $GBW = \frac{A_o}{\tau_a}$.

The pixel front end has the transimpedance function $Z_{AFE} = \frac{v_o}{i_{in}}$ given by:

$$Z_{AFE} = \frac{s^2(\frac{R_o\tau_F}{GBW}) + s(\frac{R_o\tau_F}{A_o} + \frac{R_o}{GBW}) + \frac{R_o}{A_o} - R_F}{s^3(\frac{R_oR_fC_T}{GBW}) + s^2(\frac{\tau_T}{GBW} + \frac{R_oR_FC_T}{A_o}) + s(\tau_F + \frac{\tau_T}{A_o} + \frac{1}{GBW}) + 1 + \frac{1}{A_o}}, \tag{2.3}$$

with time constants $\tau_F = R_FC_F$ and $\tau_T = R_F(C_F + C_P) + R_o(C_P + C_L)$. We also define $C_T = C_PC_F + C_PC_L + C_FC_L$. Although Z_{AFE} is a third-order function, this formulation shows the effect of the core amplifier design parameters on the overall response.

For an ideal amplifier with infinite A_o (and thus infinite GBW), the higher-order terms in (2.3) drop out and Z_{AFE} reduces to

$$Z_{AFE} = \frac{-R_F}{1 + s\tau_F}, \tag{2.4}$$

which is an ideal single-pole response, where the pulse-response duration and peak can be controlled by R_F. The functionality of this circuit can also be interpreted as a charge integrator [23], in the case where $R_F \to \infty$ such that $Z_{AFE} \to \frac{-1}{sC_F}$. This is often used in integration-mode readout circuits, where the integration of input charges occurs for a period before being reset by shunting the amplifier feedback with a switch for a short duration. However, this technique requires a reset pulse to control the switch, and creates a corresponding off period during each cycle if the reset pulse is sent synchronously. A scheme to send an asynchronous reset signal only when an input pulse has been processed has been reported [7]. However, this design uses an in-pixel ADC to generate the reset signal, requiring significant layout area.

Another general implication from (2.3) is that a reduction in R_o reduces the effect of the higher-order terms. This justifies the use of a low-output-impedance amplifier, as opposed to a higher-output-impedance operational transconductance amplifier (OTA).

2.2.1 Pixel Specifications

In this section, we derive specifications for the pixel components. We begin with A_o and then determine some expected values for the resistances and capacitances in the circuit.

In the following section, we will see that the ADC is specified for 8-bit resolution, thus we choose a minimum dc gain $A_{o,min}$ that gives 9-bit steady-state settling accuracy in order have some margin. Using the inequality

$$A_o > \frac{1}{2^{-9}} \times \frac{1}{\beta}, \tag{2.5}$$

with feedback factor $\beta = 1$, we get $A_{o,min} = 54\,\text{dB}$.

A large R_F is needed to maximize gain and minimize noise, as will be seen in the ensuing discussion, but we are also bound by τ_F, which is directly related to our system-level t_d specification. Therefore, as mentioned previously, we choose $C_F = 6.79\,\text{fF}$, the minimum unit MOM capacitor size in our process, allowing for the largest possible R_F to meet the τ_F specification.

To determine τ_F, we first calculate the required decay duration $\tau_d = t_d - t_p$, as the CSA output settles from its peak to within the relative settling error specification ε. For 8-bit accuracy, or $\varepsilon = 0.39\%$, τ_d is approximately $5.55 \times \tau_f$. Using $t_d = 1.327\,\mu\text{s}$, found in the previous chapter, and the expected $t_p = 150\,\text{ns}$ of an MPPC, we find that $\tau_F = 212\,\text{ns}$ and thus $R_F = 31.2\,\text{M}\Omega$.

For the remaining components, we derive estimates from typical circuits used to implement these blocks. At the output, C_L mainly consists of the following-stage input gate capacitance, and is estimated to be 150 fF. R_o is also estimated for a source-follower output stage to be $25\,\text{k}\Omega$. For C_P, an estimate of 30 fF is found using a $10 \times 10\,\mu\text{m}^2$ pad geometry and the PDK documentation on layer spacing and dielectric thickness, along with the associated wiring vias and electrostatic discharge (ESD) protection diodes. In addition, we estimate MPPC pixel capacitance in the 30 fF – 60 fF range, so we use a $C_P = 100\,\text{fF}$ to include some margin.

Using the values derived above in (2.3), we sweep GBW and numerically determine a minimum at which the desired ε is reached. This results in $GBW_{min} = 14\,\text{MHz}$.

2.2.2 Pixel Noise

The most critical specification for the pixel front-end circuit is noise. The front-end noise sources are shown in Figure 2.5. Resistors R_F and R_o contribute thermal noise with power spectral densities (PSDs) $\overline{i_{nf}}^2(f) = \frac{4kT}{R_F}$ and $\overline{i_{no}}^2(f) = \frac{4kT}{R_o}$, respectively, where T is absolute temperature and k is Boltzmann's constant. Although R_o represents the core amplifier's output impedance, it is modelled as a resistor here for simplicity. The amplifier is modelled with both thermal and flicker voltage noise components, under the assumption that the main contributors are input devices with transconductances g_m. The amplifier thermal-noise PSD $\overline{v_{nat}}^2(f) = \frac{4kT\gamma}{g_m}$ and flicker-noise PSD $\overline{v_{naf}}^2(f) = \frac{K_f}{WLC_{ox}f^\alpha}$ are based on the expected size and bias conditions of the input device, where γ is the thermal noise excess factor, K_f and α are the flicker-noise constants, and C_{ox} is the oxide capacitance per unit area. In our noise modelling, we quantify these parameters using data from the PDK documentation. The input shot noise PSD is $\overline{i_{ns}}^2(f) = 2qI_{dark}$, where q is the charge of an electron and $I_{dark} \approx 2.5\,\text{pA}$ is the dark current through the sensor material junction with the collecting electrodes.

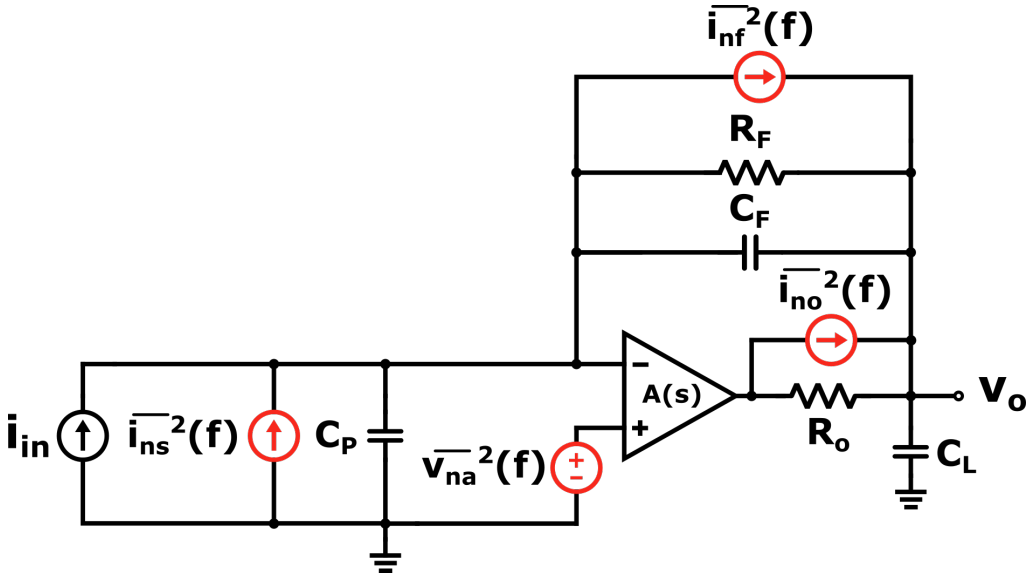


Figure 2.5: Pixel front-end model with noise sources.

The pixel front-end output referred voltage noise PSD $\overline{v_{oa}}^2(f)$ due to $\overline{v_{na}}^2(f)$ is given by:

$$\overline{v_{oa}}^2(f) = \frac{(-\omega R_F(C_P + C_F))^2 + 1}{(1 + \frac{1}{A_o} - \omega^2(\frac{\tau_T}{GBW} + \frac{R_o R_F C_F}{A_o}))^2 + (\omega(R_F C_F + \frac{1}{GBW} + \frac{\tau_T}{A_o}) - \omega^3(\frac{R_o R_F C_T}{GBW}))^2} \times \overline{v_{na}}^2(f), \tag{2.6}$$

while the remaining output referred voltage noise PSD components $\overline{v_{of}}^2(f)$, $\overline{v_{oo}}^2(f)$, and $\overline{v_{os}}^2(f)$, due to $\overline{i_{nf}}^2(f)$, $\overline{i_{no}}^2(f)$, and $\overline{i_{ns}}^2(f)$, respectively, are given by:

$$\overline{v_{of}}^2(f) = \frac{(\omega^2(\frac{R_F R_o C_P}{GBW} - R_F))^2 + (\omega R_o C_P)^2}{|D(j\omega)|^2} \times \overline{i_{nf}}^2(f), \tag{2.7}$$

$$\overline{v_{oo}}^2(f) = \frac{(\frac{R_o}{A_o} - \omega^2(\frac{R_F R_o (C_P + C_F)}{GBW}))^2 + (\omega(\frac{R_F R_o (C_P + C_F)}{A_o} + \frac{R_o}{GBW}))^2}{|D(j\omega)|^2} \times \overline{i_{no}}^2(f), \tag{2.8}$$

and

$$\overline{v_{os}}^2(f) = \frac{(\frac{R_o}{A_o} - R_F - \omega^2(\frac{R_o R_F C_F}{GBW}))^2 + (\omega(\frac{R_o R_F C_F}{A_o} + \frac{R_o}{GBW}))^2}{|D(j\omega)|^2} \times \overline{i_{ns}}^2(f), \tag{2.9}$$

where $|D(j\omega)|^2$ is the denominator of (2.6).

Using (2.6) and (2.7) to (2.9), and the design value estimates from above, we plot the input-referred noise charge PSDs in Figure 2.6 up to 1.18 MHz, the equivalent-noise bandwidth f_{ENBW} of the CSA assuming a single-pole response. Noise charge PSDs are obtained using the input-referred current noise PSDs and the current-to-charge relation $Q_{in} = i_{in} t_p$.

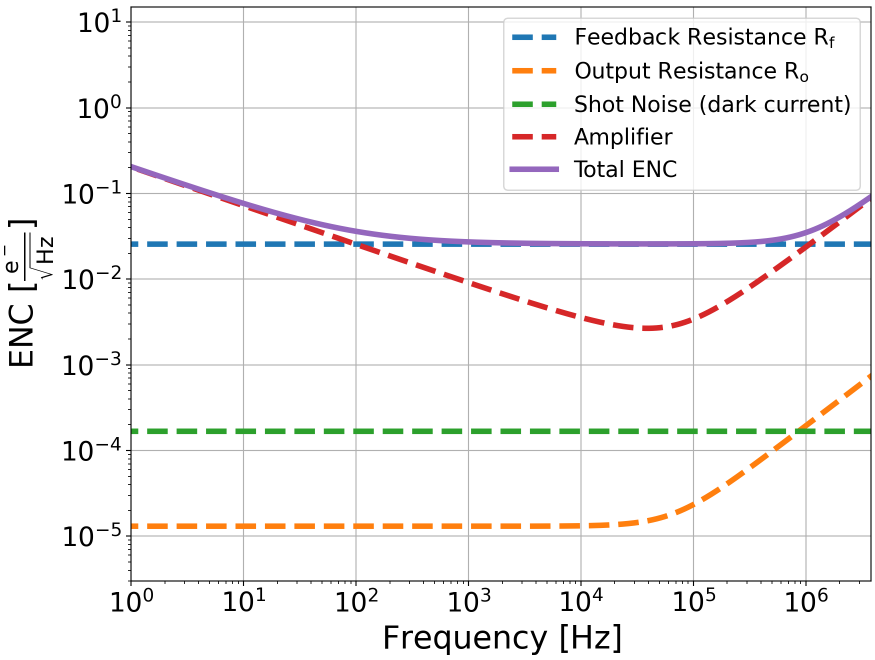


Figure 2.6: ENC contributions from various noise sources.

Calculating the total integrated noise from 1 Hz to f_{ENBW} results in $ENC = 104\,\mathrm{e^-_{rms}}$. From the plot in Figure 2.6, it is clear that the total noise is dominated by R_F and the amplifier noise contributions. The ENC of these two components are $ENC_{amp} = 95\,\mathrm{e^-_{rms}}$ and $ENC_{R_F} = 41\,\mathrm{e^-_{rms}}$, respectively. Since R_f is governed by the t_d specification, design effort should be focused on reducing $\overline{v_{na}}^2$.

Although $C_P = 100\,\mathrm{fF}$ is used to obtain the results above, it is also important to check the ENC performance with respect to C_P, which can vary depending on the type of sensor used. Figure 2.7 shows that ENC increases linearly with the C_P once the amplifier noise begins to dominate the total ENC.

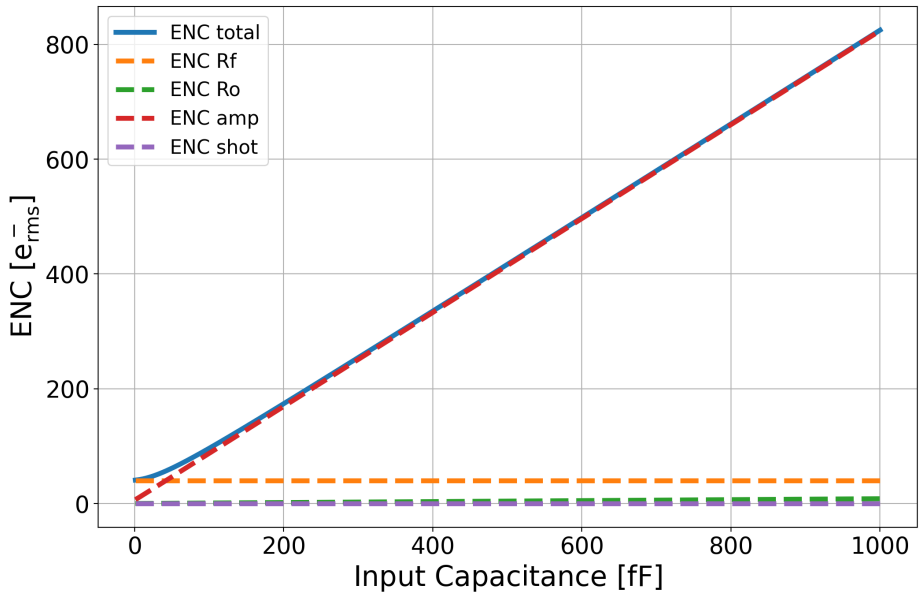


Figure 2.7: ENC contributions as a function of input capacitance C_P.

2.2.3 Power Specification

A final high-level consideration before beginning pixel design at the transistor level is the power specification. The power-density target of $< 5\,\mathrm{W/cm^2}$ translates to a maximum total pixel power of $61.3\,\mu\mathrm{W/pixel}$ for $35 \times 35\,\mu\mathrm{m}^2$ pixels. Using this value, and the standard supply voltage $V_{DD} = 1.8\,\mathrm{V}$, we have a dc bias-current budget of $34\,\mu\mathrm{A}$ for all blocks in the pixel.

2.3 System Modelling

With the general front-end specifications in place, we use a MATLAB model that includes the pixel, summing block, and ADC to estimate full-system performance and obtain a resolution specification for the ADC. This model includes random noise according to the

CSA noise model derived above, as well as other non-idealities such as ADC quantization noise and dc offset introduced prior to the mixing stage.

We perform a Monte Carlo simulation of 25000 runs in MATLAB. Each run has a 20-μs duration, in which a randomly-timed input pulse arrives at each pixel in the bank and is combined with a random noise sequence sampled from the CSA noise distribution. The input energy of each pulse is also randomly sampled from a uniform distribution ranging from $0 - 200\,\text{keV}$. After quantizing the summed signals, a bank of bandpass filters is used to separate the pixel signals. These filters are centred around their respective channel carrier frequencies with 5 MHz bandwidths. Then, using a fast-Fourier transform (FFT), the magnitude spectrum of each isolated pulse is integrated to recover the measured photon energy.

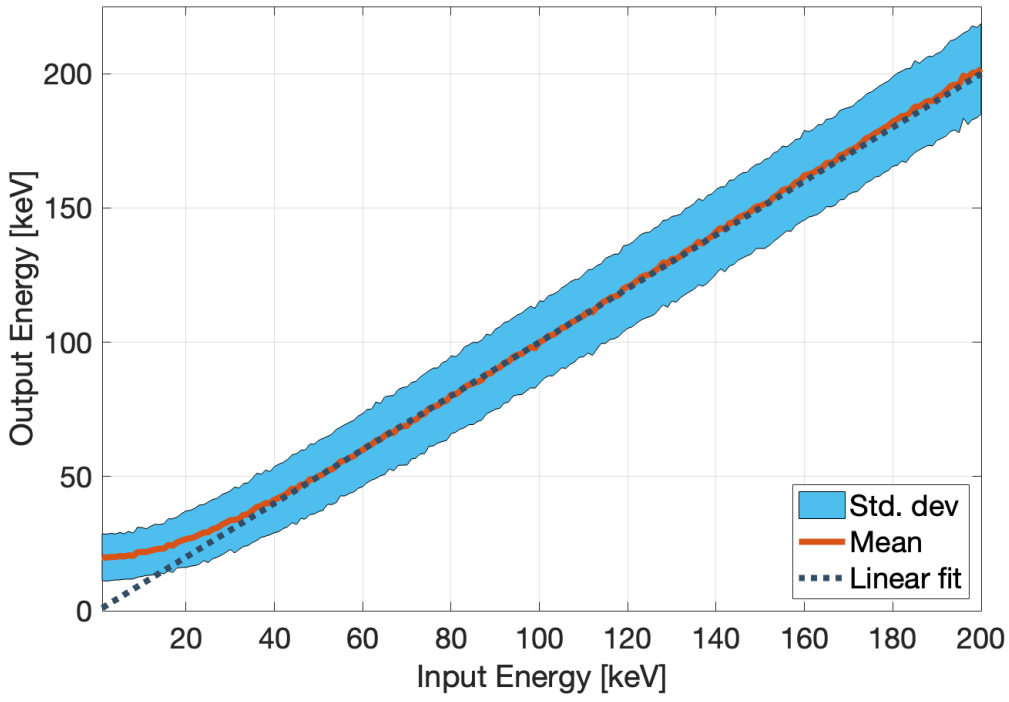


Figure 2.8: Full-system transfer characteristic simulated using MATLAB model.

Figure 2.8 shows the energy transfer characteristic resulting from our Monte Carlo simulation. The average measured output energy matches well with a linear fit, while also displaying the error by plotting the range of the standard deviation, equivalent to the ENC of the full system. Using this result, the total ENC is estimated at $199\,\mathrm{e^-_{rms}}$, equivalent to 8.94 keV for $W_\pm = 45\,\mathrm{eV/e^-}$. Since the pixel signals are summed together, their uncorrelated output noise powers are also summed, producing a total noise higher than that of a single pixel. Although the pixel signals are lowpass filtered after up-conversion, noise energy at frequencies below the pixel band adds to adjacent pixel bands. Applying a steep bandpass filter to each pixel signal after mixing could help alleviate this issue. However, for our design, we use low-power LPFs to minimize impact on pixel area and power consumption.

Our simulation results above assume an 8-bit ADC model. Although we have found that similar performance could be achieved with as few as 6 bits, we use an 8-bit-resolution target to incorporate some margin.

The same simulation data can be viewed by applying a short-time Fourier transform (STFT) to the output, producing a rolling average of the frequency spectrum over time. Figure 2.9 shows the output spectrum from the STFT, where pulses can be easily identified above the added noise and offset. For the input energy $E_{in} = 45\,\mathrm{keV}$ used in this simulation, the output peaks are around 35 dB above the noise floor.

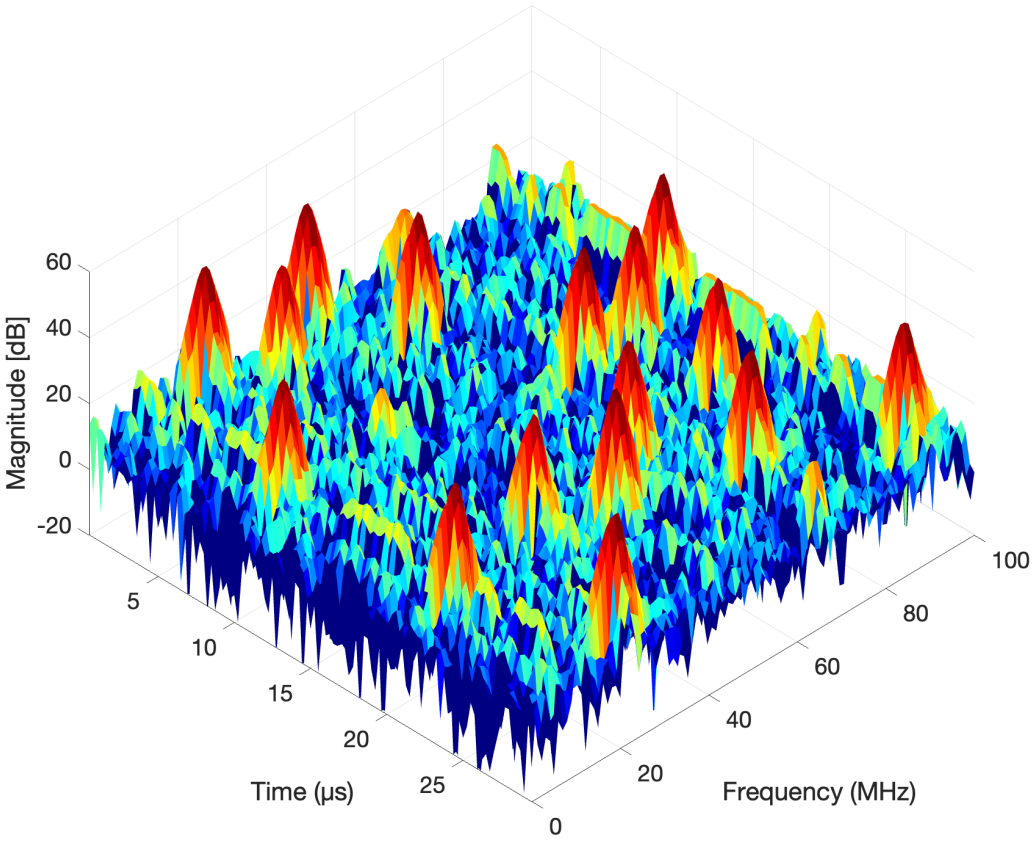


Figure 2.9: Short-time Fourier transform of the summed output signal.

By applying image processing techniques to the 2D data, we can potentially make improvements to the final energy measurements. For example, in Figure 2.10, a Gaussian filter is applied to the image before running a peak-finding algorithm to locate the pulses. Once located, the pulse area can be integrated in two dimensions to capture the energy spread in both time and frequency. In this example, alternating pixel channels are supplied and recovered at different input energies.

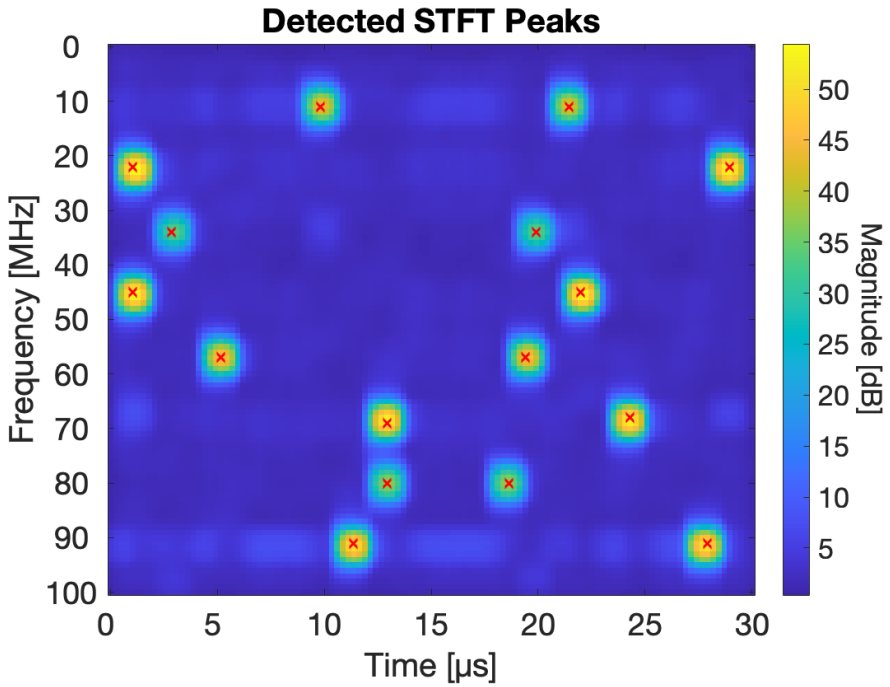


Figure 2.10: Peaks detected in STFT.

2.4 Pixel Design

In the following sections, we present the circuit design of each pixel block based on the modelling presented in the previous sections.

2.4.1 Charge Sensitive Amplifier

For typical CSA time constants, R_F is much larger than what is practical to implement with on-chip passive elements. Therefore, a pseudo-resistor using active components is usually employed as an alternative. This also provides the flexibility to make adjustments to the output-pulse duration, which is useful for calibrating the system to a specified count rate.

Active Feedback With Dark Current Compensation

One popular implementation of a CSA active feedback resistance was first presented by Krummenacher [51], as shown in Figure 2.11. In this design, the effective feedback resistance $R_{F,eff}$ is $R_{F,eff} \approx 2/g_{m1}$, where g_{m1} is the transconductance of both M1a and M1b, and is tunable by adjusting dc bias current I_P.

A secondary function of this circuit is its input-leakage (dark) current compensation, which is shunted away from the feedback path through M2. Without compensation, it is possible for an undesirably large change to occur in the dc level of the amplifier output. A simplified model was developed previously to analyze this feedback network, where the extra leakage compensation is modelled by an inductor in parallel with R_F and C_F [52]. This analysis showed that it is difficult to maintain stability without using a relatively-large shunt capacitor C, often required to be in the pF range. Such a large capacitor hinders efforts to minimize pixel size. Consequently, various alternative designs have been proposed to reduce the overall area required for an RLC equivalent feedback network [53, 54, 55]. However, these approaches require more transistors and design complexity despite using somewhat smaller capacitors.

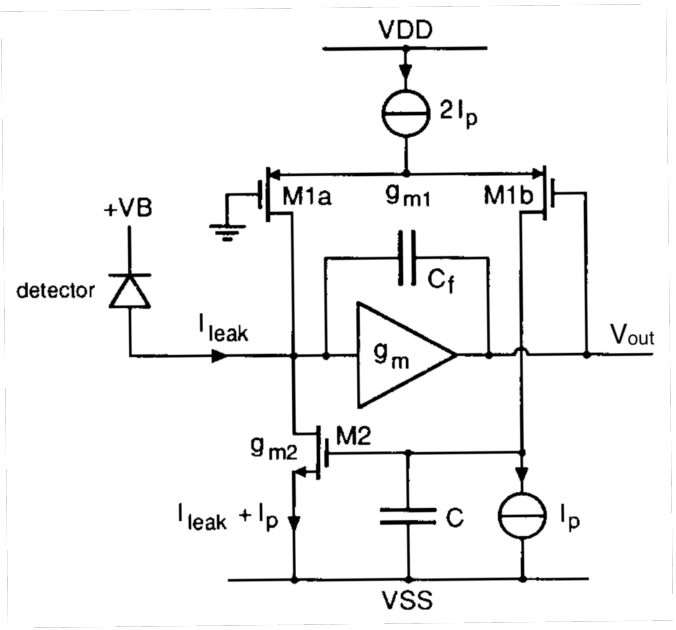


Figure 2.11: Krummenacher CSA with active feedback [51].

Active Feedback Design

While standard active feedback circuits are focused on providing a shunt path for large dark currents, the use of a-Se as the sensor has the significant benefit of low dark current, and thus there should be very small deviations in baseline dc output voltage. As such, our design does not require this added complexity, and instead we can make use of a much simpler smaller-area pseudo-resistance.

Although a single transistor operating in the triode region can be used to generate a high-value resistance, this approach could require a very-long-channel device, and dictates that the polarity of its source-drain voltage V_{SD} remains the same to maintain a high resistance. An alternative pseudo-resistor implementation uses two PMOS devices and provides symmetrical operation for either a positive or negative V_{SD} [56, 57]. We have adapted this design for our front-end circuit, as shown in Figure 2.12.

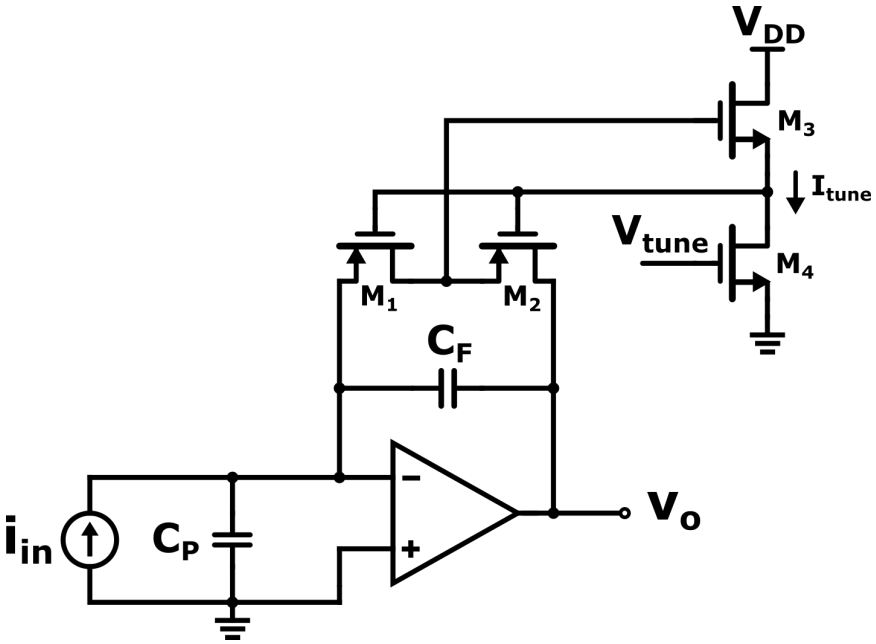


Figure 2.12: CSA with tunable feedback resistance.

To generate a high-value equivalent R_F, M1 and M2 are both operated in the subthreshold region. When $V_{SD1,2} = 0$, their resistances $R_{1,2}$ can be written as

$$R_{1,2} = \frac{V_T}{I_0} e^{-\frac{V_{SG1,2}}{nV_T}}, \tag{2.10}$$

where V_T is the thermal voltage; n is the substrate factor; and $I_0 = 2n\beta V_T^2 e^{\frac{-V_{T0}}{nV_T}}$ is a process dependent current, with a $V_{SB} = 0$ threshold voltage V_{T0} and $\beta = \mu C_{ox}\frac{W}{L}$. Since the total series resistance is controlled exponentially through $V_{SG1,2}$, by also operating M3 in the subthreshold region, V_{GS3} can be controlled logarithmically by varying the bias current I_{tune} supplied by M4. This gives a combined linear relationship between the bias current and total resistance. For our design, $(W/L)_{1,2} = 0.5\,\mu\text{m}/5\,\mu\text{m}$ and $(W/L)_{3,4} = 0.5\,\mu\text{m}/1\,\mu\text{m}$.

Amplifier Design

For the amplifier design, the main considerations are meeting the A_o and GBW specifications, as well as minimizing area and power consumption. Since we calculated earlier that the full-pixel bias-current budget is $34\,\mu$A, we have allocated approximately $10\,\mu$A to the opamp, given that there are four more stages to follow in the pixel and we would like to optimize noise by increasing the g_m of the input devices.

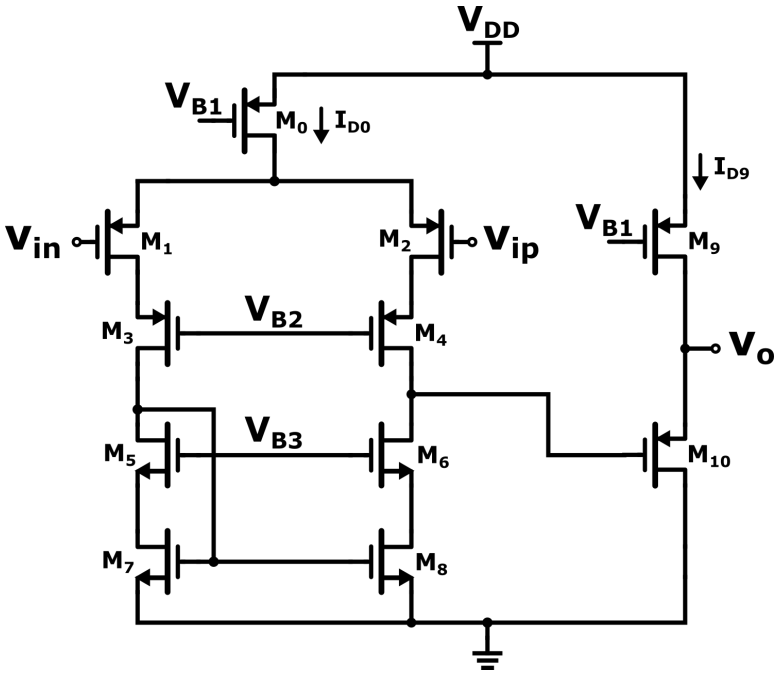


Figure 2.13: Opamp used in our CSA.

Figure 2.13 shows the opamp we use in our CSA. The first-stage telescopic OTA is followed by a source follower output stage in order to provide a relatively low output impedance, as discussed in the modelling section. A biasing branch that generates the bias voltages for both stages is not shown. Table 2.1 shows transistor dimensions and bias currents.

Parameter	Value	Parameter	Value
$(W/L)_0$	$4\,\mu$m/$1\,\mu$m	$(W/L)_9$	$2\,\mu$m/$1\,\mu$m
$(W/L)_{1,2}$	$10\,\mu$m/$0.5\,\mu$m	$(W/L)_{10}$	$2\,\mu$m/$0.18\,\mu$m
$(W/L)_{3,4}$	$4\,\mu$m/$0.5\,\mu$m	I_{D0}	$4.2\,\mu$A
$(W/L)_{5,6}$	$10\,\mu$m/$0.5\,\mu$m	I_{D9}	$2.2\,\mu$A
$(W/L)_{7,8}$	$2\,\mu$m/$1\,\mu$m		

Table 2.1: Opamp parameter summary.

Simulated results of our complete CSA design with $C_P = 100\,\text{fF}$ are shown in Figures 2.14 to 2.19. In Figure 2.14, the closed-loop frequency response is shown with a $-3\,\text{dB}$ bandwidth $f_{-3dB} = 717\,\text{kHz}$ and a first-order ($-20\,\text{dB}$/decade) slope response until the higher-order poles around 30 MHz. In Figure 2.15, the time-domain pulse responses for a range of different tuning currents are shown, where the input is a current pulse beginning at $0.1\,\mu$s, with duration $t_p = 150\,\text{ns}$. As I_{tune} varies, the effective R_F changes linearly, altering the pulse peak and duration as expected. Setting the pulse duration to match the $t_d = 1.327\,\mu$s specification gives a simulated ENC of the CSA of $101\,\text{e}^-_{\text{rms}}$ using the input-referred noise found from noise analysis in the Cadence Spectre simulator and an integration bandwidth from 1 Hz to f_{ENBW}.

In Figure 2.16, we show the input-referred noise charge PSD of the CSA. Three regions can be identified, similar to Figure 2.6. In the first region, up to around 1 kHz, the flicker-noise component of the amplifier dominates. Then, R_F thermal noise has the largest contribution until around 500 kHz, before the amplifier noise is once again the dominant component for higher frequencies. In Figure 2.17, a running integral of the PSD is shown versus frequency, where it is clear that the majority of the total integrated noise power is at frequencies close to f_{ENBW}.

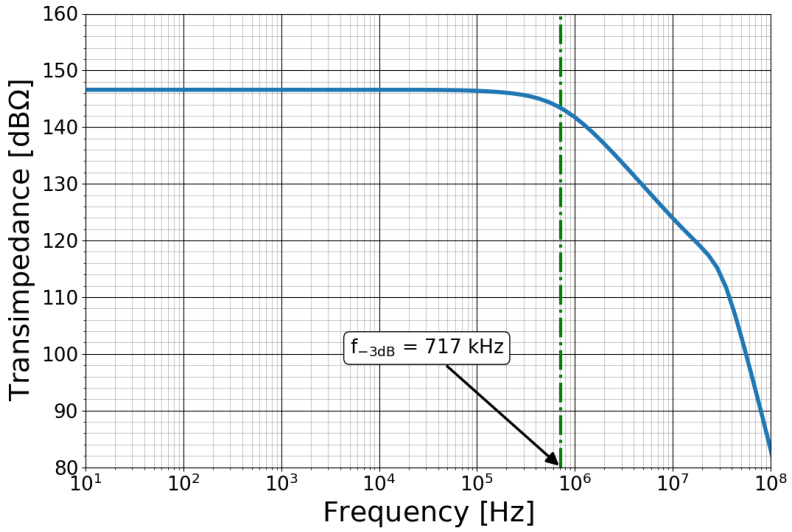


Figure 2.14: Simulated closed-loop magnitude response of the CSA transimpedance.

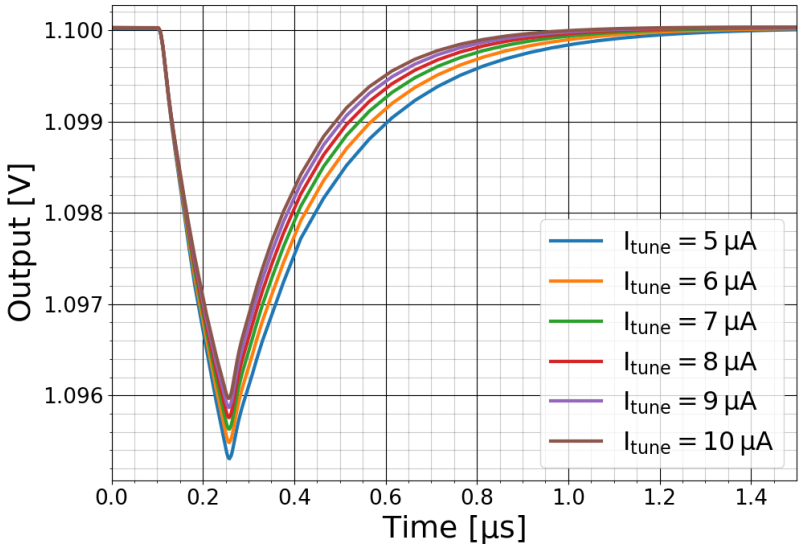


Figure 2.15: Simulated CSA pulse response at various feedback resistance tuning currents for an input-current pulse beginning at 0.1 μs with $t_p = 150$ ns.

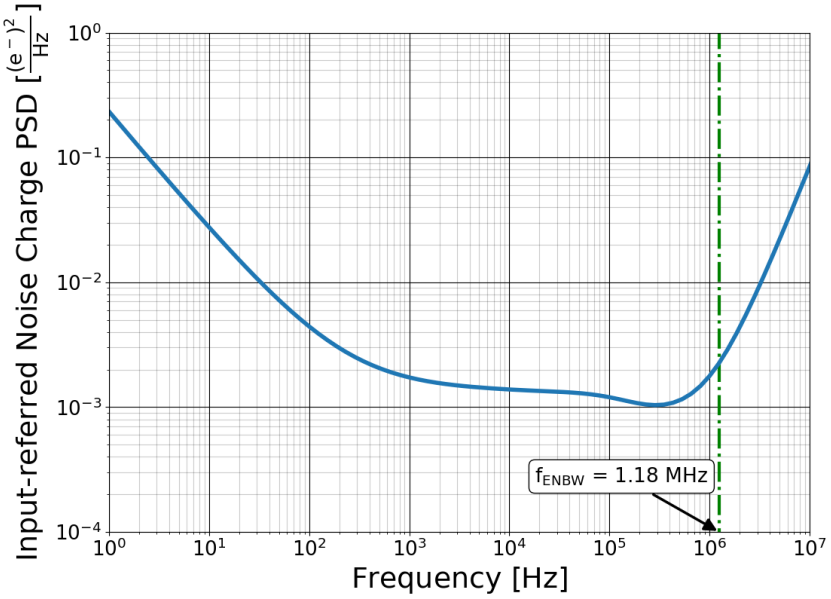


Figure 2.16: Input-referred noise charge PSD of the CSA.

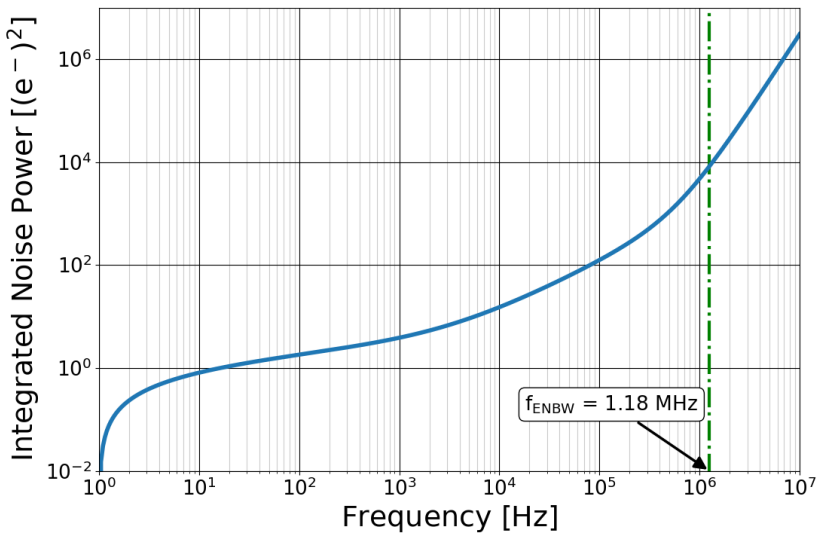


Figure 2.17: Integrated noise charge power of the CSA.

The gain and phase of the CSA loop transfer are shown in Figure 2.18. Since the loop gain is measured as a voltage gain with feedback factor $\beta = 1$, the dc loop gain is equivalent to $A_o = 64.7\,\text{dB}$, and the phase margin is 61.4°. Although this response is not that of a single pole, due to the presence of higher-order poles and zeros, the unity gain frequency $f_t = 22.5\,\text{MHz}$ remains higher than the specified GBW. The simulated slew rate of the CSA is $0.96\,\text{V}/\mu\text{s}$ with a load capacitance of 150 fF. The steady-state gain-error is $\varepsilon = 0.17\%$, which is within the 9-bit accuracy specification. The total simulated static-current draw, which includes the opamp biasing branch, is $8.6\,\mu\text{A}$, also within our specification.

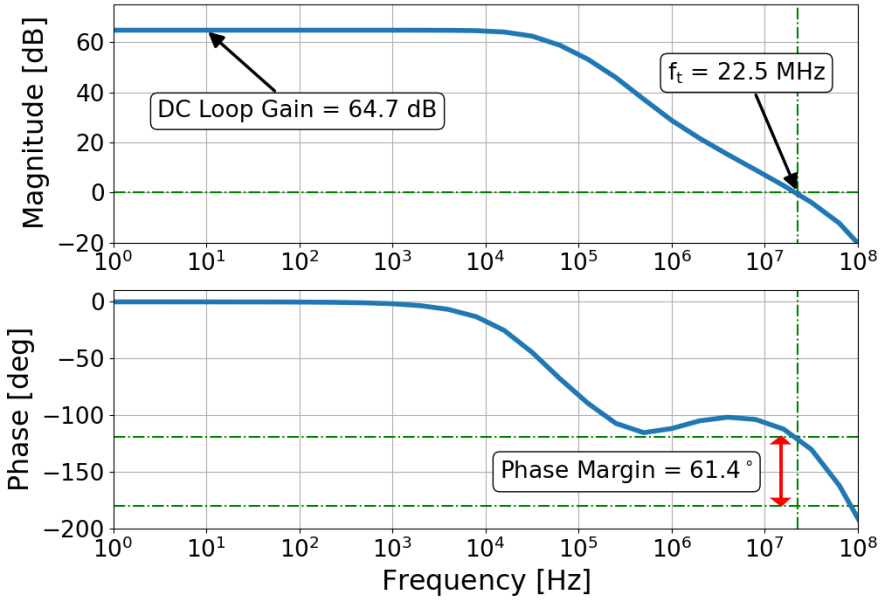


Figure 2.18: Simulated CSA loop transfer gain and phase.

The simulated transfer characteristic in Figure 2.19 shows the input-charge-to-peak-voltage gain of the CSA. Considering the linear region of this curve, the gain is $11.4\,\text{mV}/\text{ke}^-$, while saturation begins to occur at an input charge of about $17\,\text{ke}^-$.

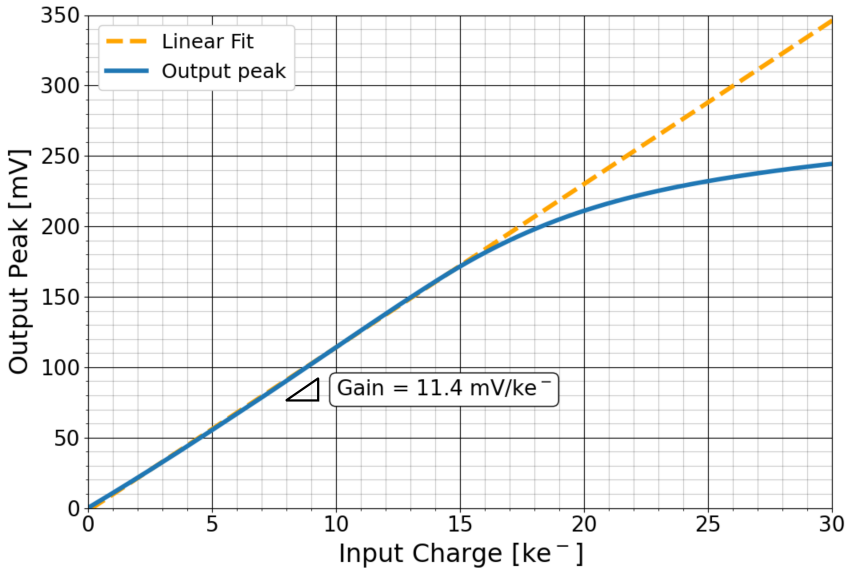


Figure 2.19: Simulated CSA transfer characteristic and charge-to-voltage gain.

2.4.2 Mixer

Figure 2.20 displays the passive mixer used to modulate the output pulses from the CSA. While the CSA output is single ended, we prefer differential signaling throughout the rest of the processing chain for better power-supply and common-mode interference rejection. Therefore, we place a single-ended-to-differential driver before the mixer. This block is a simple low-power differential amplifier with diode-connected loads, where one input is connected to the common-mode voltage V_{CM} that also biases the CSA. This driver also provides around 8.5 dB of gain, compensating for some attenuation in the passive LPF following the mixer, and helping to reduce the effect of unwanted coupling from the switching mixer signals to the CSA output. The dimensions of M1 and M2 are $(W/L)_{1,2} = 18\,\mu\text{m}/2\,\mu\text{m}$, keeping the standard deviation of offset due to random mismatch below 0.3 mV. A dc offset introduced to the mixer input results in a constant modulation of its dc level, translating to an output tone at f_c. This tone can interfere with energy

measurement at the ROIC output, but is found to have minimal impact with offset below 0.3 mV. Transistor dimensions and bias current for the driver are summarized in Table 2.2.

Parameter	Value
$(W/L)_0$	$0.6\,\mu\text{m}/1\,\mu\text{m}$
$(W/L)_{1,2}$	$18\,\mu\text{m}/2\,\mu\text{m}$
$(W/L)_{3,4}$	$2.25\,\mu\text{m}/1.2\,\mu\text{m}$
I_{D0}	$5.85\,\mu\text{A}$

Table 2.2: Mixer driver parameter summary.

The mixer consists of four switches controlled by a differential LO. The switches are implemented with transmission gates using near-minimum size dimensions ($W/L = 0.22\,\mu\text{m}/0.2\,\mu\text{m}$) to ensure low area usage. The LO signals are square waves generated by external clock generation integrated circuits (ICs).

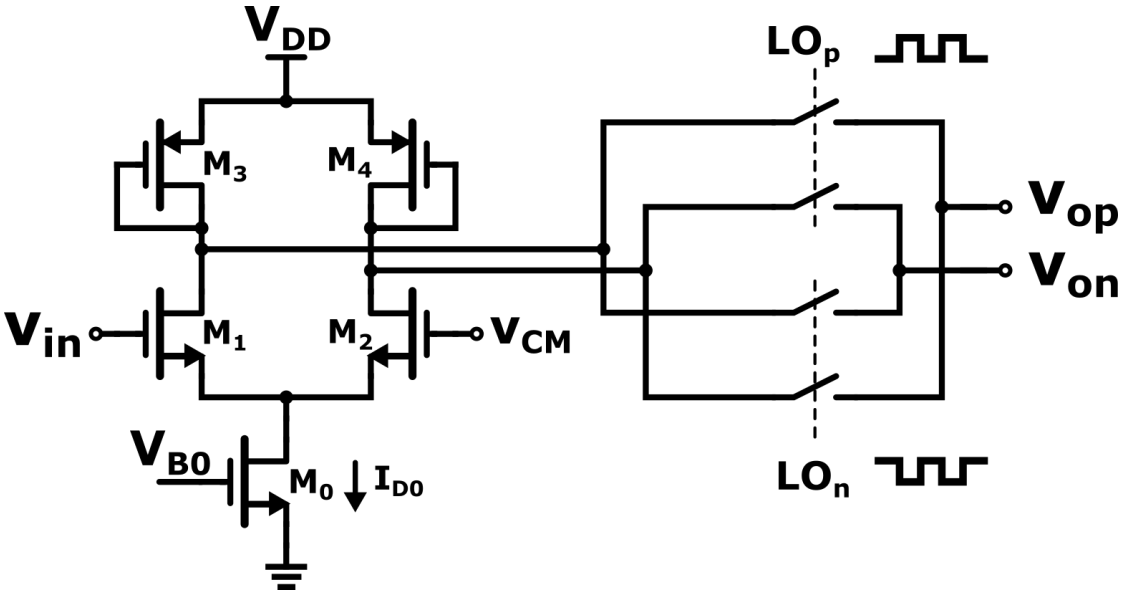


Figure 2.20: Mixer circuit.

2.4.3 Lowpass Filter

Since the mixer switches are driven by square waves, the modulated output pulse has odd-order harmonics that can interfere with adjacent pixel channels. In order to attenuate these components, each pixel employs a second-order LPF with a corner frequency just beyond f_c. We use simple open-loop differential amplifiers with diode-connected PMOS loads and a shunt capacitor across the outputs for the LPF, as shown in Figure 2.21.

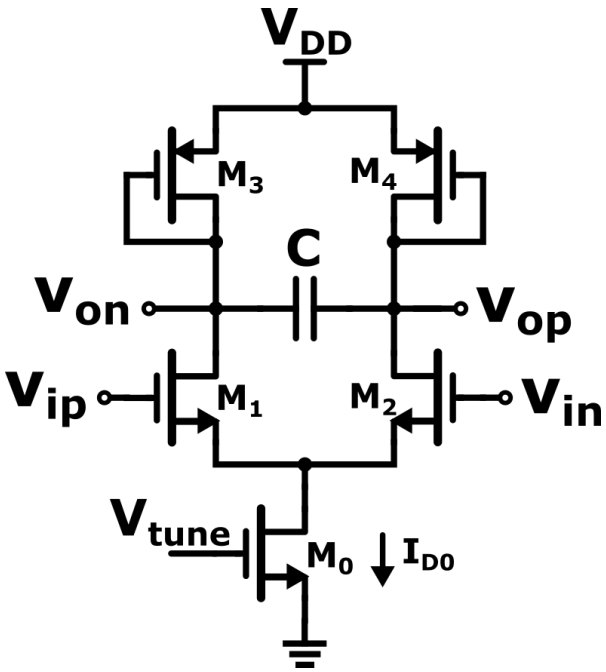


Figure 2.21: Active lowpass filter stage.

Two of these stages are cascaded to provide second-order attenuation. Each filter stage is tunable by varying the bias current I_{D0} over the range 2.5–36 μA, where the time constant of the stage is $\tau = g_{m3,4}/C$. With these cascaded stages, the calculated attenuation at the third harmonic is 13.4 dB below the fundamental. This attenuation is enough to ensure minimal impact on the adjacent channels, and is verified by including it in the full-system model results reported in the section 2.3. Figure 2.22 shows the simulation results of a

pulse at the mixer output and at the LPF output, while component parameters are listed in Table 2.3.

Parameter	Value
$(W/L)_0$	$2\,\mu\text{m}/0.5\,\mu\text{m}$
$(W/L)_{1,2}$	$1.2\,\mu\text{m}/0.8\,\mu\text{m}$
$(W/L)_{3,4}$	$0.9\,\mu\text{m}/0.4\,\mu\text{m}$
C	6.79 fF
I_{D0}	2.5–36 μA

Table 2.3: Active LPF parameter summary.

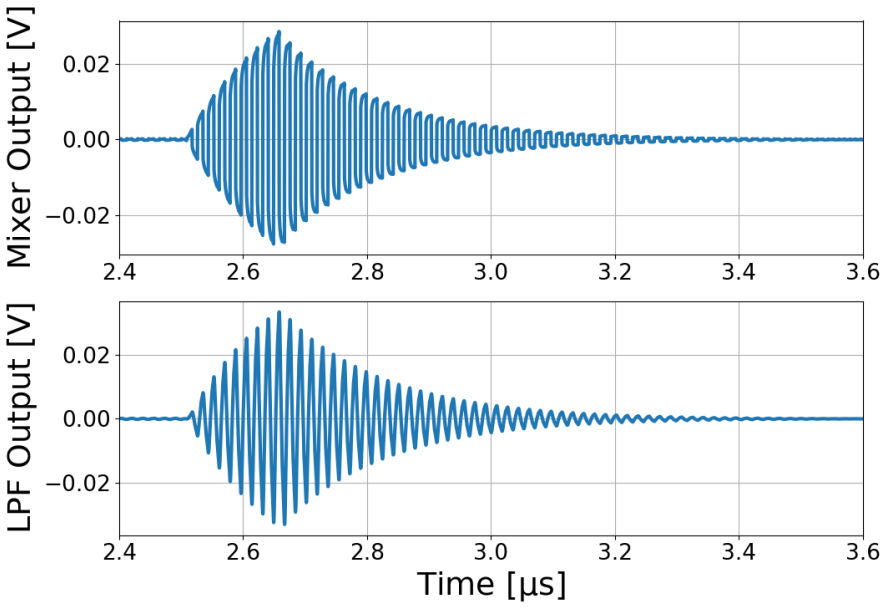


Figure 2.22: Simulated mixer output and LPF output pulses.

2.4.4 Gm Stage and Pixel Bank Summing

We sum the modulated outputs from eight pixels in the current domain. Following the LPF in each pixel is a Gm stage formed by a differential NMOS pair that shares a diode-connected PMOS load with all the other pixels in a bank such that their respective small-signal currents add, generating output voltages V_{op1} and V_{on1} to drive the following stage. This configuration is shown in Figure 2.23, where I_{SUM} is the sum of eight small-signal I_{PX} currents. The I2V stage includes two more cascaded open-loop amplifiers in order to provide an extra 7 dB of gain that is lost in the Gm stage. We could have avoided attenuation in the Gm stage using higher bias current in the differential pairs. However, since the loads for the Gm stage and cascaded amplifiers are located outside the pixel array, it is more efficient, in terms of power density, to use higher bias currents outside the pixel.

In Figure 2.24, we show a simulation result of the summed signal of eight identical coincident pulses in the time domain, along with its spectrum. Table 2.4 summarizes the transistor dimensions and bias currents.

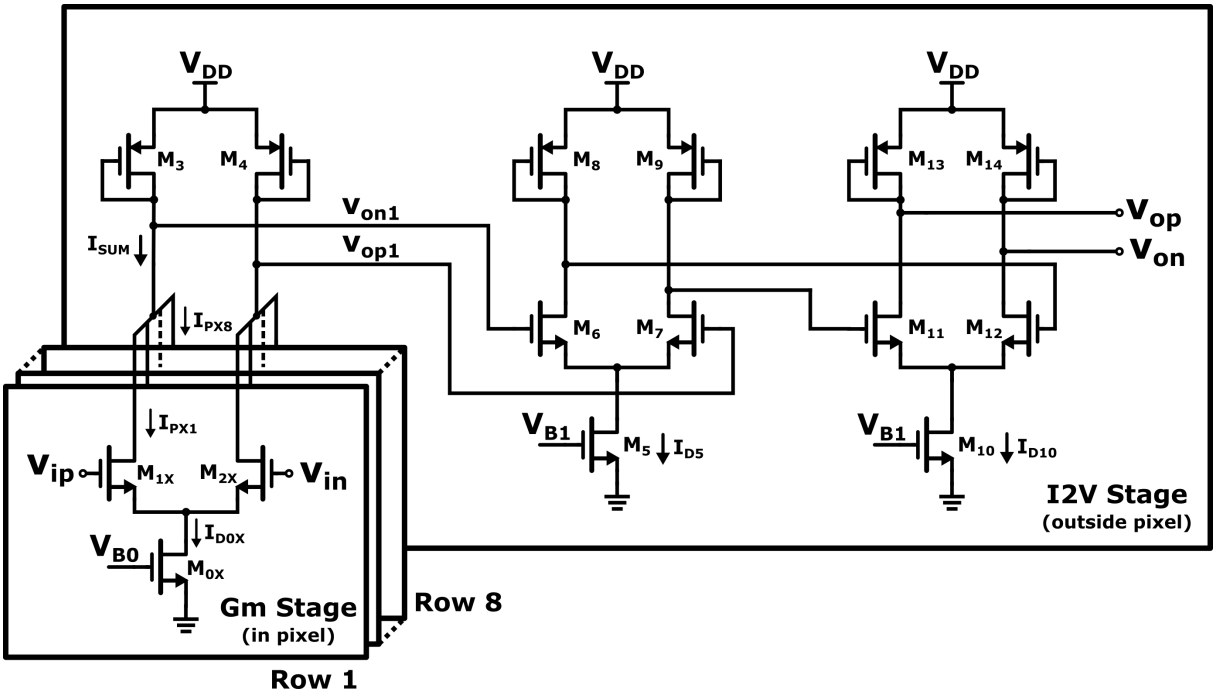


Figure 2.23: Summing stage followed by a cascade of open-loop amplifiers.

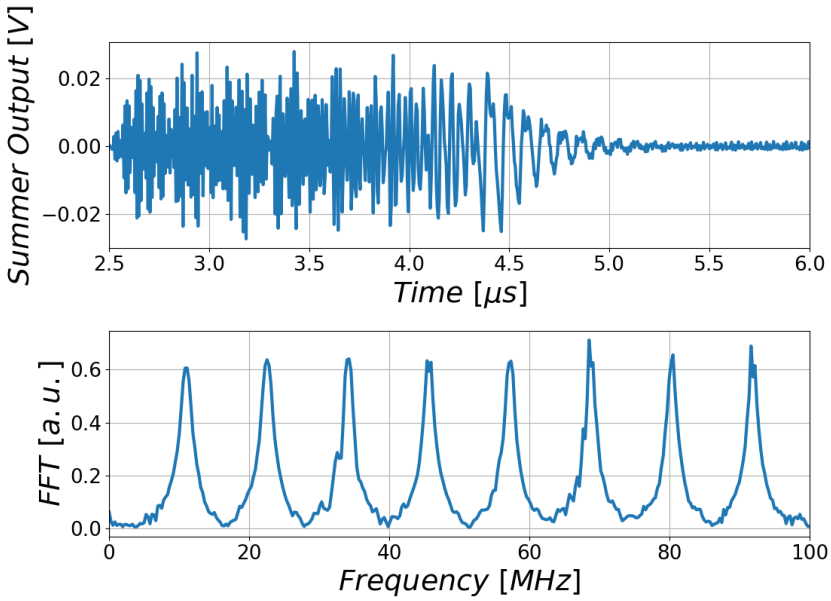


Figure 2.24: Simulated time-domain summed output signal and its spectrum from eight coincident pulses.

Parameter	**Value**	**Parameter**	**Value**
$(W/L)_{0X}$	$0.6\,\mu$m/$1\,\mu$m	$(W/L)_{10}$	$18\,\mu$m/$0.5\,\mu$m
$(W/L)_{1X,2X}$	$1.2\,\mu$m/$0.18\,\mu$m	$(W/L)_{11,12}$	$3\,\mu$m/$0.18\,\mu$m
$(W/L)_{3,4}$	$5\,\mu$m/$1\,\mu$m	$(W/L)_{13,14}$	$30\,\mu$m/$0.5\,\mu$m
$(W/L)_5$	$1.8\,\mu$m/$0.5\,\mu$m	I_{D0X}	$6\,\mu$A
$(W/L)_{6,7}$	$4\,\mu$m/$0.18\,\mu$m	I_{D5}	$29\,\mu$A
$(W/L)_{8,9}$	$3\,\mu$m/$0.5\,\mu$m	I_{D10}	$382\,\mu$A

Table 2.4: Summing block parameter summary.

2.4.5 Pixel Power Consumption

In Table 2.5, the simulated static-power consumption for each pixel block is shown, as well as the total. In addition, the static-power consumption of the I2V stage located outside the pixel is 733 μW.

Circuit	Power
CSA	15.48 μW
Mixer	10.5 μW
LPF	11.81 μW
Gm stage	10.71 μW
Full pixel	48.5 μW

Table 2.5: Summary of the simulated power consumption in the pixel circuits.

2.5 Pipelined ADC Design

Our ADC uses a pipelined architecture, based primarily on the need for the relatively high sample rate $f_s = 200$ MHz. In a 1-bit-per-stage pipelined ADC with input swing V_{REF}, each of the N stages (where N is the ADC resolution in bits) compares its input voltage V_i to $\frac{V_{REF}}{2}$ and generates a single corresponding output bit. This is accomplished using a sub-ADC consisting of a single comparator. The quantized output from the sub-ADC is then subtracted from the input signal using a digital-to-analog converter (DAC) to produce the quantization error signal. The error signal is then multiplied by two and passed to the next stage as the residue voltage V_{res}. This residue is used by the subsequent stage to generate the next bit, and thus the number of stages equals N. Since all stages operate concurrently, f_s is determined by the rate of a single stage. However, since the bits of each input sample are not generated concurrently, each stage is designed to drive a delay-line shift register so that the final output bits are available in parallel on the same clock cycle.

Since there are N cycles of delay for the most-significant bit (MSB), the total latency is N cycles.

An improvement to the 1-bit-per-stage converter is the 1.5-bit-per-stage implementation, where the sub-ADC consists of two comparators with thresholds set above and below $\frac{V_{REF}}{2}$ by $\frac{V_{REF}}{8}$. The two corresponding output bits from the comparators are again used to control a DAC signal that is subtracted from the input ahead of the $2\times$ gain stage. This extra comparator adds redundancy to each stage's output, which is then used for digital error correction at the final output [58]. The main advantage of this approach is that it significantly relaxes the acceptable comparator offset. In a 1-bit-per-stage converter, each subsequent stage requires double the comparator accuracy of the previous stage to resolve the less-significant bits. In the 1.5-bit converter, comparator offsets up to $\frac{V_{REF}}{4}$ are tolerable since this is guaranteed to keep the residue signal within V_{REF} [59].

Residue V_{res} is generated as follows, based on the stage input voltage V_i and resulting DAC output:

$$V_{res} = \begin{cases} 2 \cdot (V_i - \frac{V_{REF}}{4}) & V_i \geq \frac{V_{REF}}{8} \\ 2 \cdot V_i & -\frac{V_{REF}}{8} \leq V_i \leq \frac{V_{REF}}{8} \\ 2 \cdot (V_i + \frac{V_{REF}}{4}) & V_i \leq -\frac{V_{REF}}{8}. \end{cases} \tag{2.11}$$

Since using two comparators divides the input range into three quantization levels at each stage, the sub-ADC has $\log_2(3) \approx 1.5$ bit resolution. However, since each stage generates a 2-bit output, a digital logic is needed to decode the final N-bit output and provide the error correction enabled by the added redundancy.

Figure 2.25 shows a diagram of the signal flow in a 1.5-bit converter, where the final stage is a 2-bit flash ADC since no residue needs to be generated for a subsequent stage.

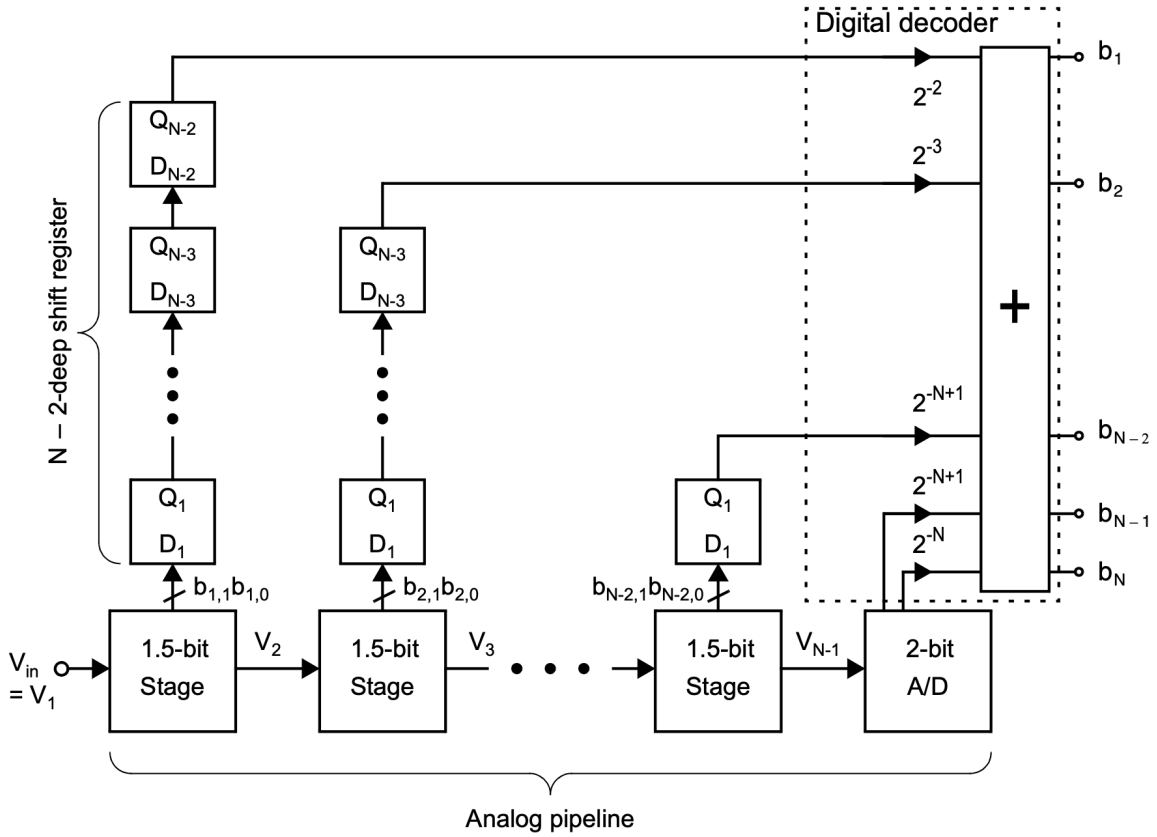


Figure 2.25: 1.5-bit pipelined ADC architecture [59].

In Figure 2.26, a diagram of a single-ended 1.5-bit stage is shown. As discussed, V_i is passed to the sub-ADC consisting of two comparators, which control the DAC signal that is subtracted from the input. Subtraction and gain multiplication are performed by a switched-capacitor (SC) circuit, consisting of an amplifier and two capacitors C_s and C_f, that operates in two phases.

In the first (sample) phase, V_i is sampled onto both C_s and C_f as switches S_1, S_2 and S_3 are closed, as seen in the diagram. During this phase, the comparator outputs are also latched setting up the DAC output.

In the second (amplify) phase, all switches are flipped, and the amplifier is operated

in feedback through C_f. Since V_i charged both capacitors in the sample phase, the virtual ground at the inverting terminal forces the charge on C_s to redistribute partially onto C_f, depending on the DAC output, and generates V_{res} as in (2.11). Since V_{res} is valid at the end of the second phase, the following stage uses alternate phases for its operation.

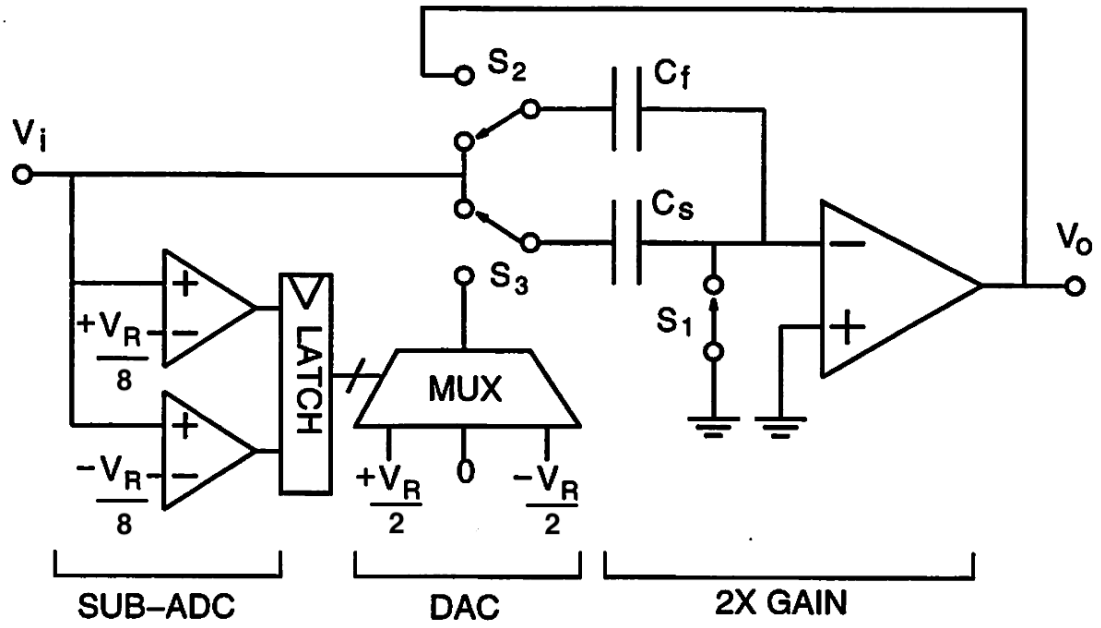


Figure 2.26: A single 1.5-bit pipelined ADC stage [58]

For 8-bit accuracy, it is important that the first stage in the pipeline settles to an error less than 0.39 % in a period of $\frac{1}{2f_s}$. Therefore, the dc gain A_o of the amplifier must be $A_o > 54\,\text{dB}$, since $\beta = \frac{1}{2}$. For each following stage, the accuracy requirements are relaxed by a factor of two. Therefore, the first stage is the most critical for design. Another potential source of relative gain error is mismatch between C_s and C_f, where $\frac{C_s}{C_f} = 1$ ideally, for a gain of two.

We select $V_{REF} = 600\,\text{mV}$ to accommodate the case where all eight pixel output signals are peaking simultaneously, and the summed signal is at its maximum peak-to-peak value.

For $N = 8$, this V_{REF} gives a least-significant bit (LSB) voltage V_{LSB} of

$$V_{LSB} = \frac{V_{REF}}{2^N} = \frac{0.6}{2^8} = 2.34375\,\text{mV}. \tag{2.12}$$

In the absence of noise and mismatch errors, the SNR of the ADC is limited by its inherent quantization noise such that

$$SNR \leq 6.02N + 1.76\,\text{dB}. \tag{2.13}$$

Given this theoretical maximum SNR, we specify that input-referred thermal noise contributions from sampling and the opamp should be less than $\frac{V_{LSB}}{2}$. Using this specification, we allocate $\frac{V_{LSB}}{4}$ to each of the above noise sources. This makes it possible to calculate a minimum size for the sampling capacitors since the average thermal noise power $\overline{v_n}^2$ associated with switching is [58]

$$\overline{v_n}^2 = \frac{1}{\beta}\frac{kT}{C_f}. \tag{2.14}$$

Therefore, the minimum capacitor size C_{min} is

$$C_{min} = \frac{1}{\beta}\frac{kT}{\overline{v_n}^2} = \frac{1}{0.5}\frac{300 \cdot 1.38 \times 10^{-23}}{(2.34375 \times 10^{-3})^2/4} = 6.03\,\text{fF}, \tag{2.15}$$

for both C_f and C_s. However, the minimum unit-size metal-insulator-metal (MIM) capacitor in our 180-nm CMOS technology is approximately 20 fF. Therefore, switching noise will not have much impact. Consequently, we choose $C_s = C_f = 84\,\text{fF}$. This ensures a reasonable ADC layout area, and negligible mismatch effects, where we calculate mismatch error based on the supplied PDK models.

Although the pipelined stage in Figure 2.26 is single-ended, we implement a differential configuration. The following sections describe the design of the amplifier, comparator, DAC, and digital decoder.

2.5.1 Fully-Differential OTA

To design the core amplifier used in the 1.5-bit pipeline stage, we first need to derive specifications based on settling time and accuracy, as well as total input-referred noise. We

aim for a steady-state settling accuracy of 9 bits to allow some margin, which establishes an A_o specification of $A_o > 60\,\text{dB}$. Another critical settling specification is the GBW, where the amplifier is required to settle within $t_{settle} = \frac{1/f_s}{2} = 2.5\,\text{ns}$, for $f_s = 200\,\text{MHz}$. Based on a first-order amplifier response, the required GBW is

$$GBW > \frac{-\ln[1-(1-\varepsilon)(\frac{1+A_o\beta}{A_o\beta})]}{2\pi t_{settle}\beta}, \tag{2.16}$$

where $\varepsilon = \frac{1}{2^{N+1}}$. For our design, with $A_o = 70.4\,\text{dB}$ and $\beta = \frac{1}{2}$, we get $GBW > 841\,\text{MHz}$ (units of $\frac{V}{V}$ are used in (2.16) for A_o). To design for this, we use minimum length input transistors in order to maximize their transition frequency f_T. From characterization curves of the NMOS devices in our technology, we select a large current density $\frac{I_D}{W} \approx 33\,\mu\text{A}/\mu\text{m}$ to provide a high f_T without compromising the intrinsic gain. However, with minimum-length devices, we require a two-stage amplifier to meet the A_o specification. Thus we choose a telescopic-OTA first stage with a common-source second stage. Figure 2.27 shows our fully-differential OTA and Table 2.6 summarizes its design parameters.

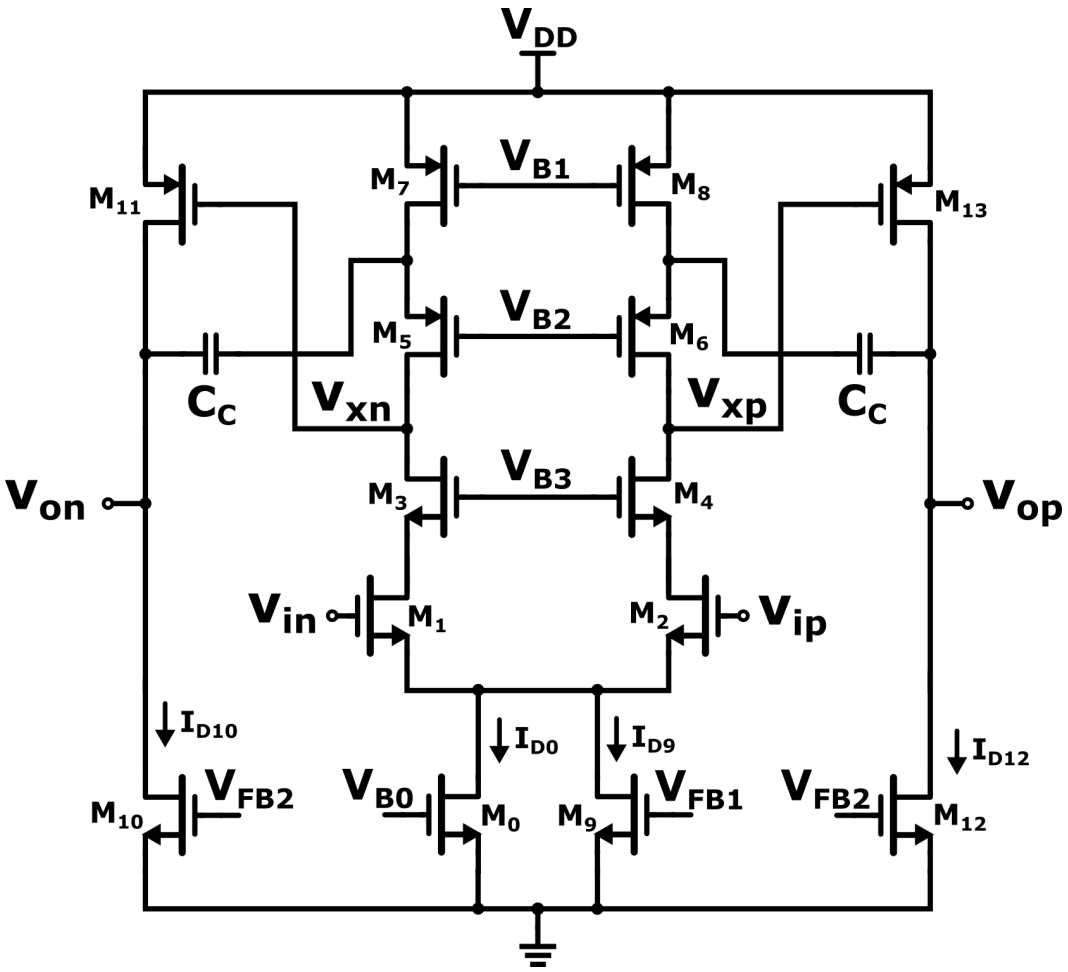


Figure 2.27: Two-stage OTA for pipelined ADC stage.

Parameter	Value	Parameter	Value
$(W/L)_0$	$36\,\mu$m$/2\,\mu$m	$(W/L)_{10,12}$	$20\,\mu$m$/1\,\mu$m
$(W/L)_{1,2}$	$6\,\mu$m$/0.18\,\mu$m	$(W/L)_{11,13}$	$42\,\mu$m$/0.18\,\mu$m
$(W/L)_{3,4}$	$5\,\mu$m$/0.18\,\mu$m	C_C	99 fF
$(W/L)_{5,6}$	$12\,\mu$m$/0.18\,\mu$m	I_{D0}	$346\,\mu$A
$(W/L)_{7,8}$	$12\,\mu$m$/0.18\,\mu$m	I_{D9}	$54\,\mu$A
$(W/L)_9$	$4\,\mu$m$/2\,\mu$m	$I_{D10,12}$	$380\,\mu$A

Table 2.6: OTA parameter summary.

To balance the common-mode (CM) output level from each stage, CM feedback (CMFB) circuits are included as shown in Figure 2.28. We implement a simple dynamic CMFB circuit due to its small area footprint [59]. During the sample phase ϕ_1, capacitors C_1, C_4, C_5, and C_8 are all charged to voltage $V_{CM} - V_{B0}$, where V_{B0} is the tail current bias voltage of M0 in Figure 2.27. Meanwhile, C_2 and C_3 sample $V_{X,CM} - V_{FB1}$, while C_6 and C_7 sample $V_{o,CM} - V_{FB2}$, where $V_{X,CM}$ and $V_{o,CM}$ are the average output voltages from each stage. During phase ϕ_2, any differences between these two voltages are averaged as the capacitors share their charges, bringing the actual CM level closer to the desired value. In the first stage, we split the tail current transistors between the feedback-controlled device M9 and a statically-biased device M0 to attenuate the CMFB loop gain for stability.

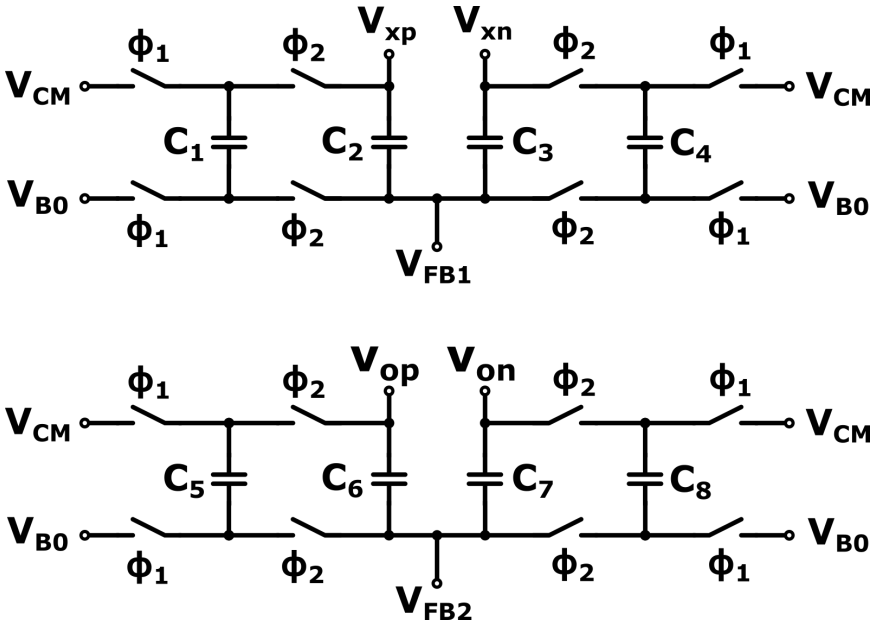


Figure 2.28: CMFB circuits used for the pipeline stage OTA.

We apply indirect feedback compensation to our OTA, where the compensation capacitor C_C is fed back to the low impedance node of the cascoded load devices (M4 to M8) [60, 61]. This is in contrast to typical Miller compensation where C_C is inserted between the output nodes of the two stages. In indirect compensation, the right-half-plane zero, typically associated with Miller compensation, is avoided by attenuating the feed-forward path to the output. Although feedback gain is slightly reduced, since the zero is no longer adding to the loop phase response, a smaller C_C can be used for a given settling time requirement, which translates to a higher unity-gain frequency $f_t \approx \frac{g_{m1,2}}{2\pi C_C}$. In Figure 2.29, the simulated loop gain is shown for feedback factor $\beta = \frac{1}{2}$.

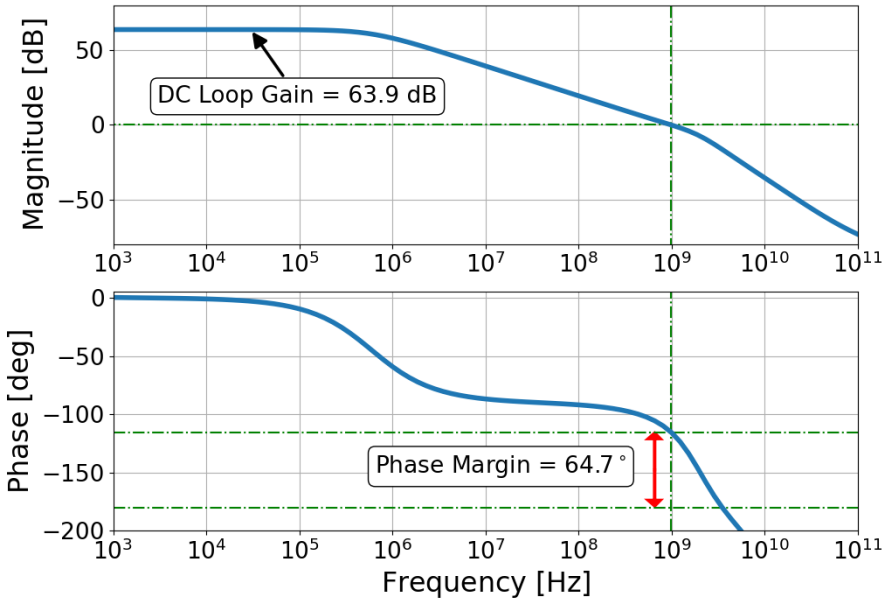


Figure 2.29: Simulated loop transfer gain and phase of the 2× gain stage with $\beta = \frac{1}{2}$.

To meet the average input-referred noise specification $\overline{v}_n \leq 586\,\mu\mathrm{V_{rms}}$ over $f_{ENBW} = 697\,\mathrm{kHz}$, we scale $g_{m1,2}$ accordingly, while still meeting the settling requirements. Static-power consumption of the OTA is 2.1 mW, lower than the 2.6 mW specification derived from the ADC power-density specification. Table 2.7 summarizes our simulated results for the complete OTA design.

Parameter	Specification	Result
DC gain A_o	$\geq 60\,\text{dB}$	$70.4\,\text{dB}$
Bandwidth	$\geq 280\,\text{kHz}$	$444\,\text{kHz}$
Gain Bandwidth Product GBW	$\geq 841\,\text{MHz}$	$1.469\,\text{GHz}$
Input-referred noise $\overline{v}_n$	$\leq 586\,\mu\text{V}_{\text{rms}}$	$137\,\mu\text{V}_{\text{rms}}$
Static power	$\leq 2.6\,\text{mW}$	$2.1\,\text{mW}$

Table 2.7: OTA specification summary and simulated results.

2.5.2 Switched-Capacitor Comparator

In the two comparators of the 1.5-bit pipeline stage, the differential V_i is compared to $\frac{V_{REF}}{8}$ and $-\frac{V_{REF}}{8}$, respectively, around V_{CM}. To create this comparison using the available reference voltage supplies $\pm\frac{V_{REF}}{2}$, we use the SC network in Figure 2.30 [58]. During phase ϕ_2, the C capacitors are charged to $\pm\frac{V_{REF}}{2}$, while the $3C$ capacitors are shorted to give a differential voltage of zero. In phase ϕ_1, V_i^+ and V_i^- are each applied across the pairs of C and $3C$ capacitors in parallel, which effectively redistributes the charges to create a differential voltage $V_c^+ - V_c^- = V_i - V_{REF}/8$. As with the SC network used for the gain stage, the switches are driven by a non-overlapping clock.

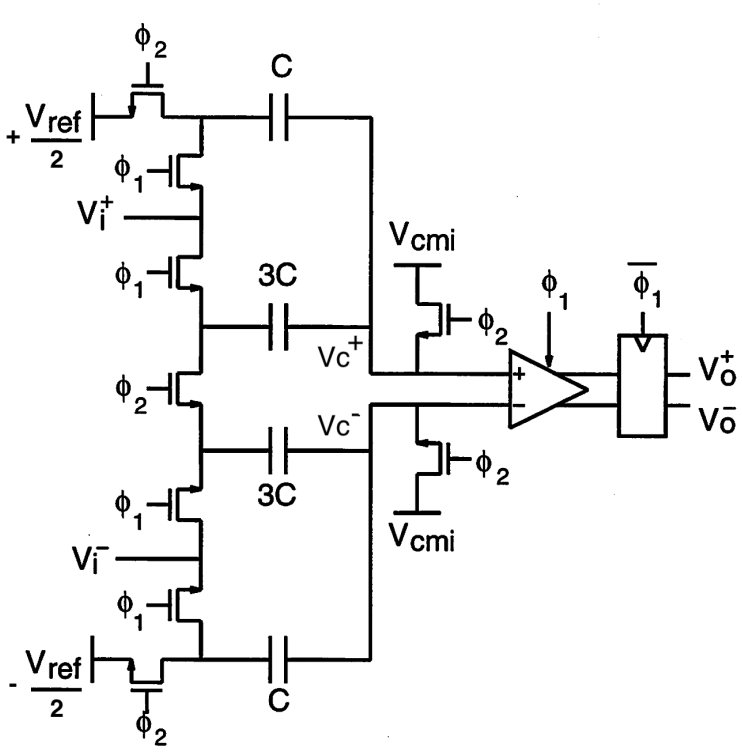


Figure 2.30: Switched-capacitor network feeding the comparator [58].

Following the SC network, we use the StrongArm latch comparator shown in Figure 2.31 [62]. During ϕ_1, a differential input voltage $V_{ip} - V_{in}$ is applied while the outputs are pulled to V_{DD} through M7 and M8. When ϕ_2 goes high, M0 turns on and the two input branches begin to pull the output voltages V_{op} and V_{on} down. However, since the V_{op} and V_{on} are connected with back-to-back inverters, one side will be pulled low faster due to the voltage difference at the inputs. This will trigger a positive-feedback action that pushes the outputs to opposite rail voltages.

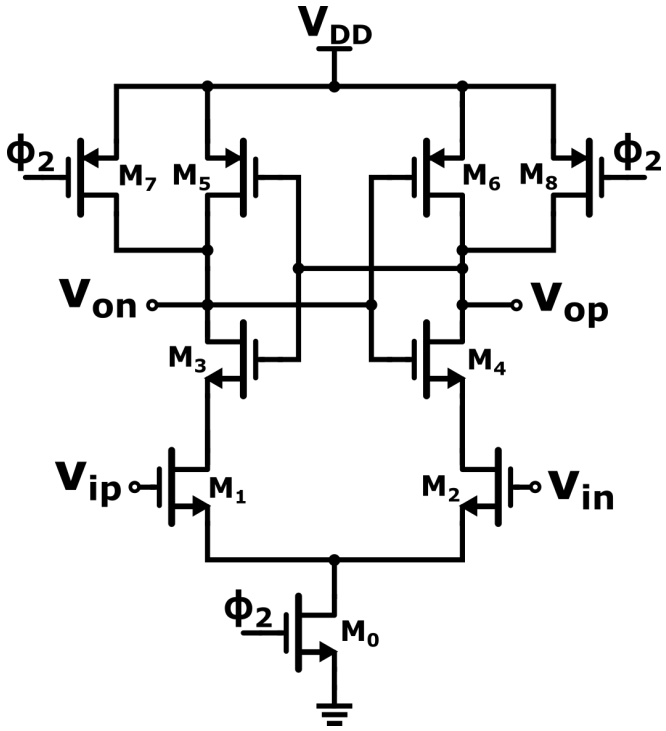


Figure 2.31: StrongArm comparator.

Table 2.8 shows the transistor dimensions used in the comparator. Since the comparator is specified for an input-offset voltage V_{os} less than $\frac{V_{REF}}{4} = 150\,\text{mV}$, random mismatch is not an issue for these dimensions.

Parameter	**Value**
$(W/L)_0$	$2\,\mu\text{m}/0.18\,\mu\text{m}$
$(W/L)_{1,2}$	$2\,\mu\text{m}/0.18\,\mu\text{m}$
$(W/L)_{3,4}$	$5\,\mu\text{m}/0.18\,\mu\text{m}$
$(W/L)_{5,6}$	$10\,\mu\text{m}/0.18\,\mu\text{m}$
$(W/L)_{7,8}$	$2\,\mu\text{m}/0.18\,\mu\text{m}$

Table 2.8: StrongArm comparator parameter summary.

Figure 2.32 shows the simulated delay between the ϕ_2 edge and V_{op} as it latches. Since the comparator output signals drive the DAC, which must settle within a period of $\frac{1}{2f_s}$, this delay of 366 ps is adequate in our design.

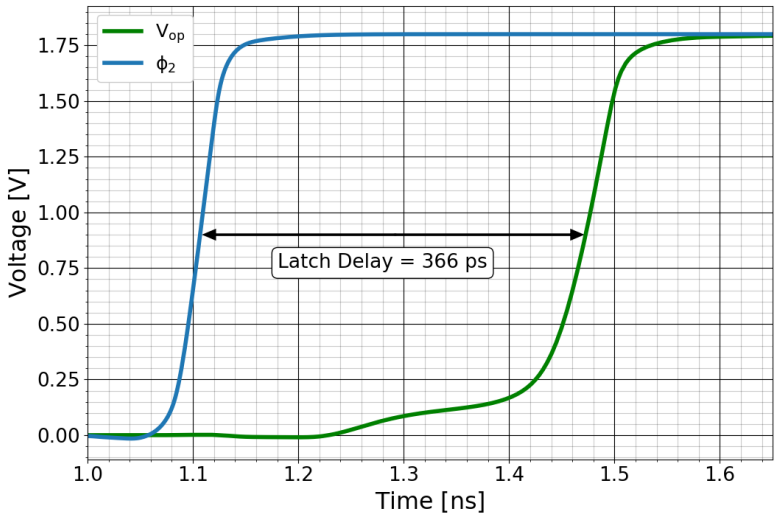


Figure 2.32: Simulated comparator latch delay.

2.5.3 Differential DAC

The differential DAC used to drive the SC circuits is shown in Figure 2.33. This architecture is a simple passive switch multiplexer where each branch of the differential output $V_{op} - V_{on}$ is selected by a bank of transmission gates. Voltage inputs V_{REFP} and V_{REFN} are centred around V_{CM}, such that $V_{REFP} = V_{CM} + \frac{V_{REF}}{2}$ and $V_{REFN} = V_{CM} - \frac{V_{REF}}{2}$. DAC control is based on the outputs of the two comparators which each supply a pair of differential output bits, b_{0p} and b_{0n} for the first comparator, and b_{1p} and b_{1n} for the second. The extra switches in each branch, and at the outputs, act to reset $V_{op} - V_{on}$ to zero during phase ϕ_1 and enable the output multiplexing in phase ϕ_2. The NMOS and PMOS dimensions in the transmission gates are $(W/L)_{NMOS} = 2.5\,\mu\text{m}/0.18\,\mu\text{m}$ and $(W/L)_{PMOS} = 5\,\mu\text{m}/0.18\,\mu\text{m}$, respectively, giving a maximum simulated on resistance $R_{on} = 1.01\,\text{k}\Omega$.

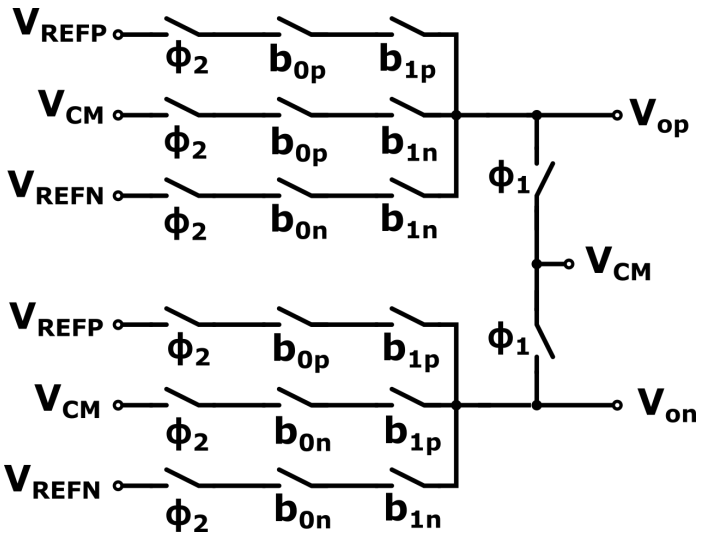


Figure 2.33: Differential mux DAC.

2.5.4 Digital Output Decoder

Since each pipeline stage generates multiple output bits, we require a digital decoder to recover the final 8-bit output after the bits become aligned through their respective shift registers. Since we implement a 2-bit flash ADC as the final ADC stage, the total number of stages in our ADC is $N - 1 = 7$. For simplicity, we denote the output bits of the first (MSB) ADC stage B_{70} and B_{71}, because this stage is used to calculate the MSB, which corresponds to the final output bit D_{out7}. Subsequent stage indices decrease (B_{60} and B_{61}, etc.), while the final flash stage has three output bits denoted B_{10}, B_{11}, and B_{12}. Our decoder is comprised of a bank of full adders, as shown in Figure 2.34, in addition to a small combinational-logic block to generate the LSB, where $D_{\text{out0}} = B_{10} \cdot (\overline{B_{11} \oplus B_{12}})$. Figure 2.35 shows this combinational block.

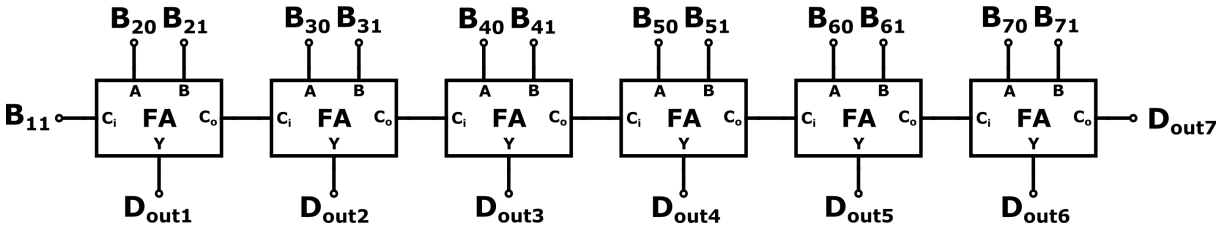


Figure 2.34: Full-adder bank in decoder.

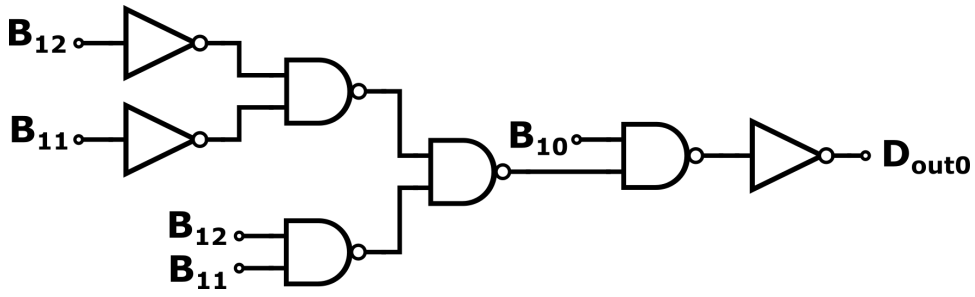


Figure 2.35: Least-significant bit generation.

The full adder is shown in Figure 2.36. In this mirror-type adder [63], the carry bit C_i propagation delay is prioritized over the Y output generation. This is useful due to the ripple-carry nature of the decoder structure, where the critical path follows the carry bit chain. For our design, the total simulated propagation delay from B_{11} to D_{out7} is 580 ps, well within the sampling period $\frac{1}{f_s} = 5$ ns. Omitted from the diagram are extra inverters placed between full-adder stages, since Y and carry out C_o bits are inverted at every second stage.

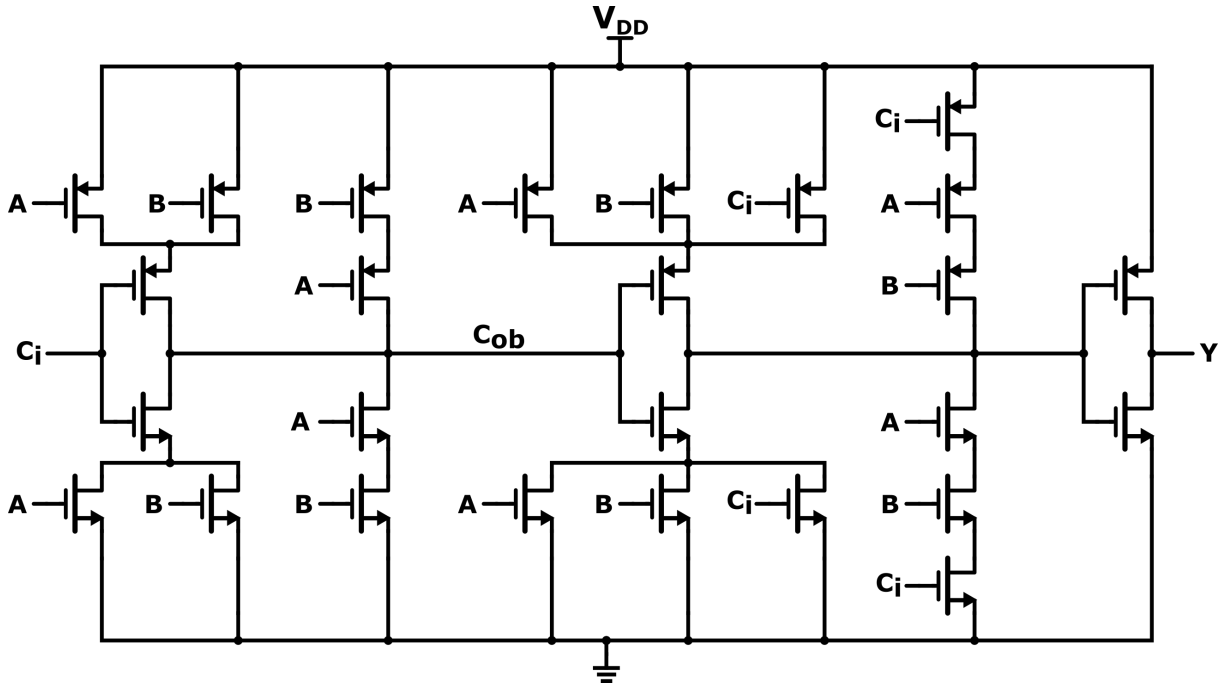


Figure 2.36: Full mirror adder circuit.

2.5.5 Simulated ADC Performance

We simulate the full ADC to evaluate its static and dynamic performance. Figures 2.37 and 2.38 show the differential non-linearity (DNL) and integral non-linearity (INL) of the ADC, respectively. Both results show good performance as the DNL remains below LSB/2 across the full range of output codes, and the INL remains below one LSB over the full range.

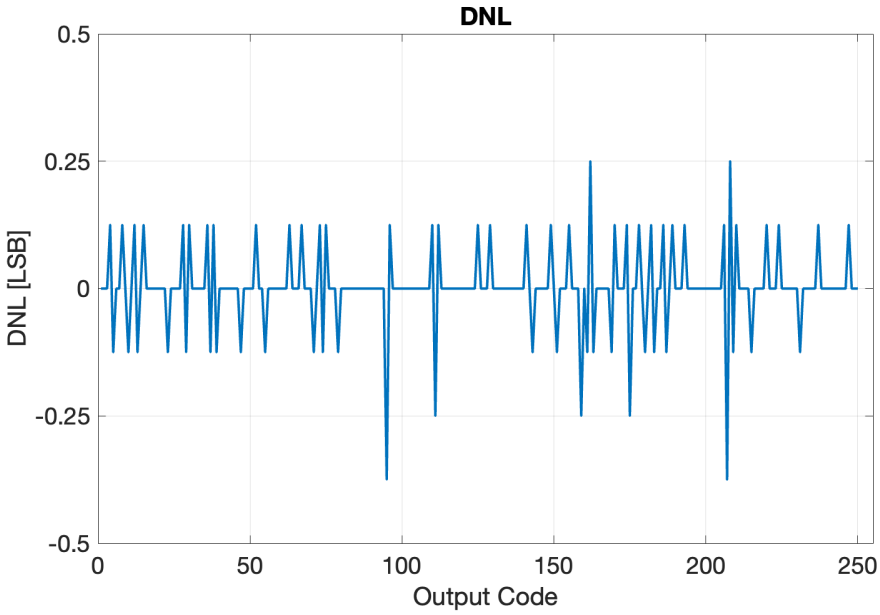


Figure 2.37: Simulated ADC differential non-linearity.

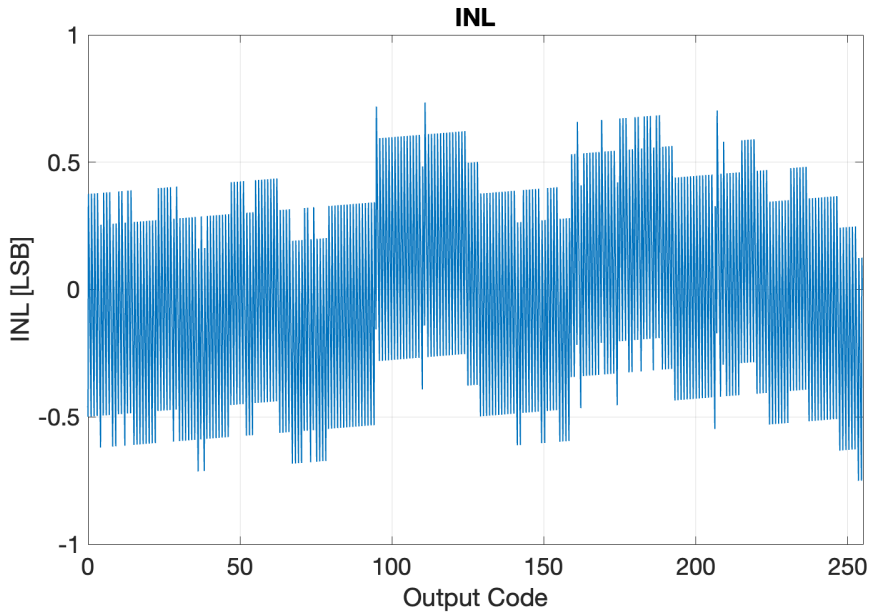


Figure 2.38: Simulated ADC integral non-linearity.

In Figure 2.39, the power spectrum used to calculate the signal-to-noise-and-distortion ratio (SNDR) of the ADC for a full-scale input is shown. Figure 2.40 shows SNDR plotted against input frequency f_{in} with a full-scale input, and includes the equivalent number of bits (ENOB), which is close to 8 bits across the full bandwidth.

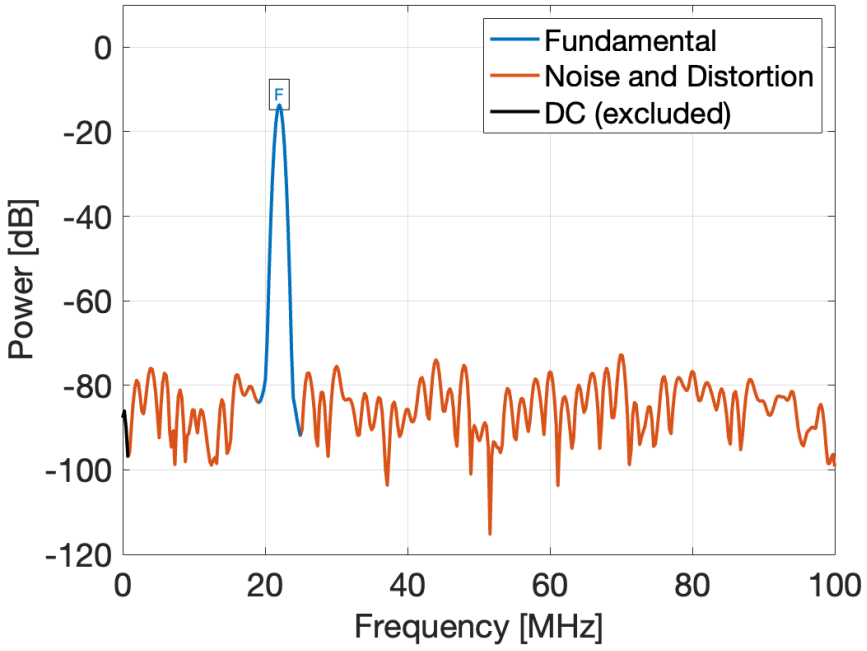


Figure 2.39: Simulated output spectrum of the ADC for a full-scale sinusoidal input.

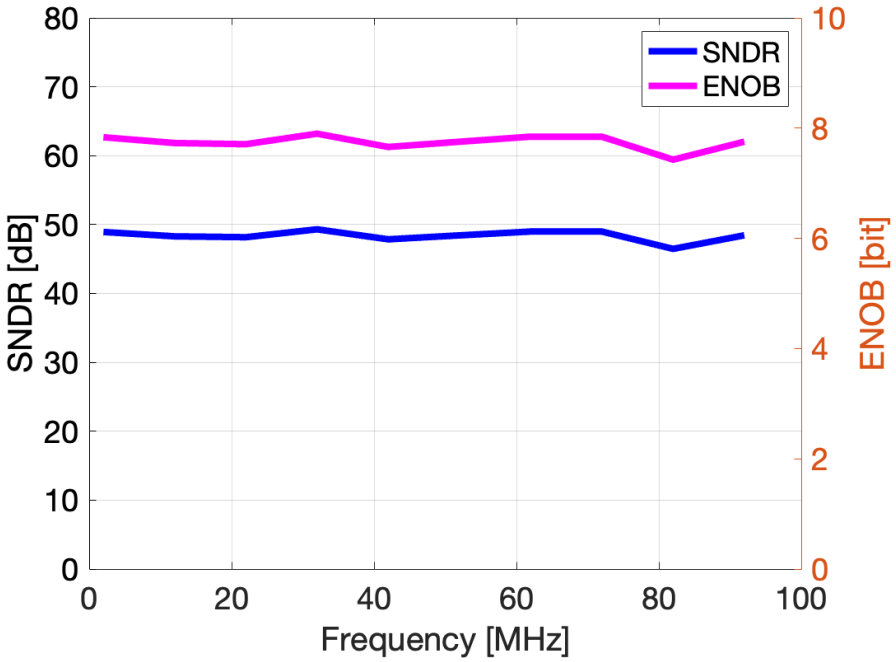


Figure 2.40: Simulated SNDR and ENOB of the ADC vs. input signal frequency for a full-scale input.

The simulated power consumption P of the ADC is 16 mW, which includes static and dynamic power. Using this value with the average ENOB from the plot in Figure 2.40, the Walden figure of merit FoM measuring energy efficiency against f_s is:

$$FoM = \frac{P}{f_s \cdot 2^{ENOB}} = 384 \, \frac{\text{fJ}}{\text{conv}}. \tag{2.17}$$

This result is on the same order as other pipelined ADCs designed in 180-nm CMOS technology [64].

2.6 Auxiliary Circuits

In the following sections, we describe the remaining circuits in the ROIC design. These include voltage regulators used to supply the ADC V_{REF} and pixel V_{CM}, biases for the amplifiers, a non-overlapping clock generator, buffering and multiplexing circuits for input and output pins, a scan chain for digital configuration, and on-chip test circuits to drive and read various internal nodes.

2.6.1 Voltage Regulators

In order to drive the ADC voltage references used by the DAC and comparator, we include on-chip voltage regulators to buffer off-chip-supplied references. This is required since the 16 ADCs combine to draw peak dynamic currents as high as 1 mA from the reference-voltage supplies. Without regulators, these switching currents cause significant ringing in the references due to bondwire inductance, which directly affects the DAC outputs and corrupts V_{res}. Regulators are also included to supply a stable V_{CM} to the pixels and ADCs.

Figure 2.41 shows our regulator circuit. The primary pass device M3, with dimensions $(W/L)_3 = 1280\,\mu\text{m}/0.18\,\mu\text{m}$, is configured as a source follower controlled by a feedback loop through an opamp and a level shifter. The level shifter, consisting of M1 and M2, with dimensions $(W/L)_1 = 4\,\mu\text{m}/2\,\mu\text{m}$ and $(W/L)_2 = 1\,\mu\text{m}/2\,\mu\text{m}$, respectively, is a source follower biased to properly set the dc level at the gate of M3. For the V_{REFP} supply, we use a complementary output configuration using an NMOS pass device for M3, and PMOS devices for M1 and M2, all using the same dimensions as in the regulator shown in Figure 2.41. The internal opamp uses the same topology shown in Figure 2.13. Compensation capacitor $C_C = 2.66\,\text{pF}$ limits the dominant loop pole, while $C_L \approx 20\,\text{pF}$ is the parallel combination of the total load capacitance and a MIM capacitor added to reduce output ripple induced through the supply rails. The load current i_{load} is dynamic and dependent on the switch configuration of the DACs in the ADCs. Figure 2.42 shows the simulated V_{CM} versus a change in i_{load}, where the deviation is less than 1 mV over the full i_{load}

range. In Figure 2.43, the simulated regulator response to an i_{load} pulse similar to the simulated ADC load is shown. The maximum deviation of V_{CM} from its steady-state value is $1.76\,\text{mV} < V_{LSB}$.

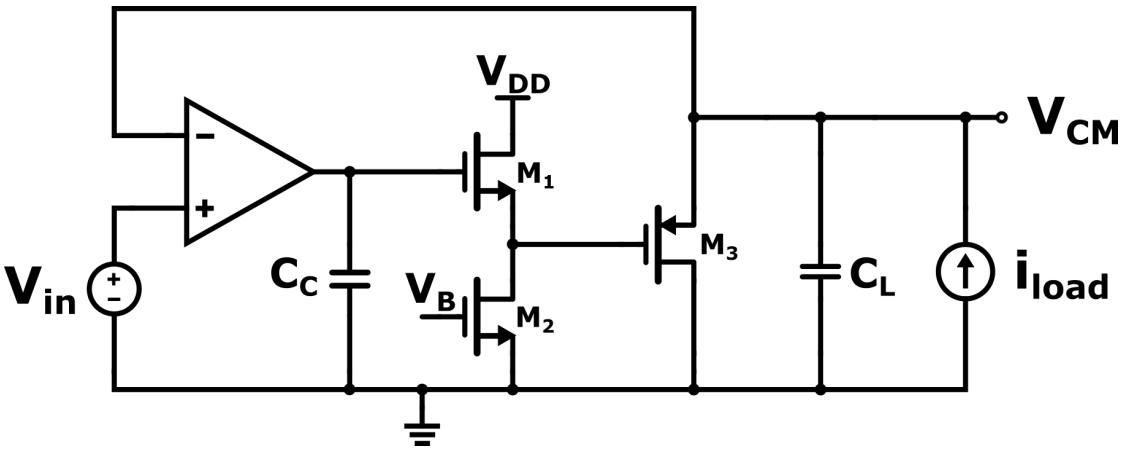


Figure 2.41: Voltage regulator.

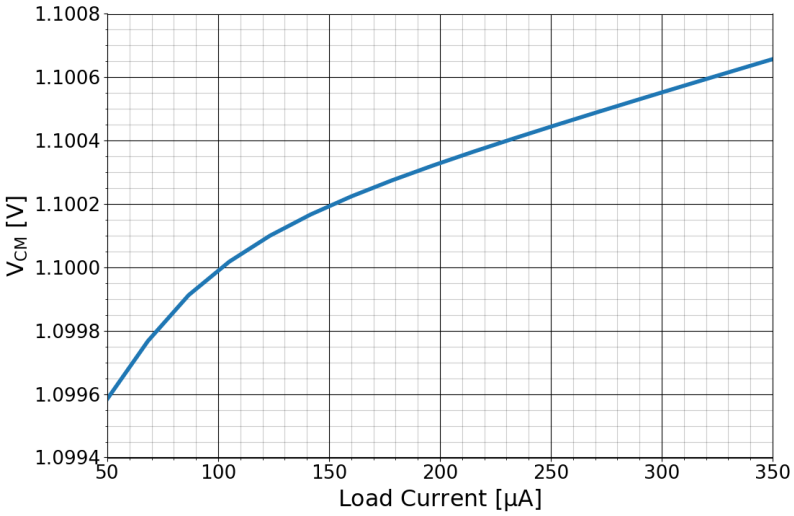


Figure 2.42: Simulated voltage regulator output vs. dc load current for a target $V_{CM} = 1.1\,\text{V}$.

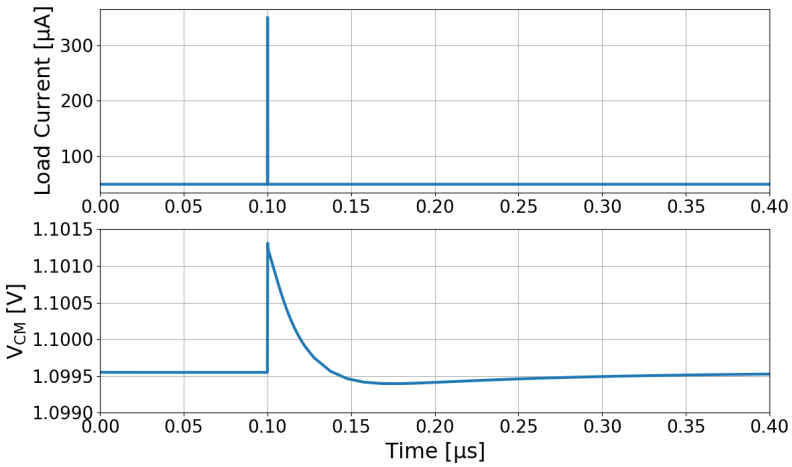


Figure 2.43: Simulated voltage regulator output for a load current pulse with a 100 ps duration.

2.6.2 Biases

Biasing for the majority of the ROIC is provided directly from off-chip current references. This includes bias currents for all pixel circuits, except for the feedback resistance tuning supply, which is on the order nA and is thus scaled down from a larger μA-level off-chip supply. All generated bias voltage nodes are decoupled with large on-chip MOS capacitors in the 1-5 pF range.

Figure 2.44 shows the bias-generation circuit for the telescopic OTA used in the ADC. Table 2.9 summaries the transistor dimensions and currents.

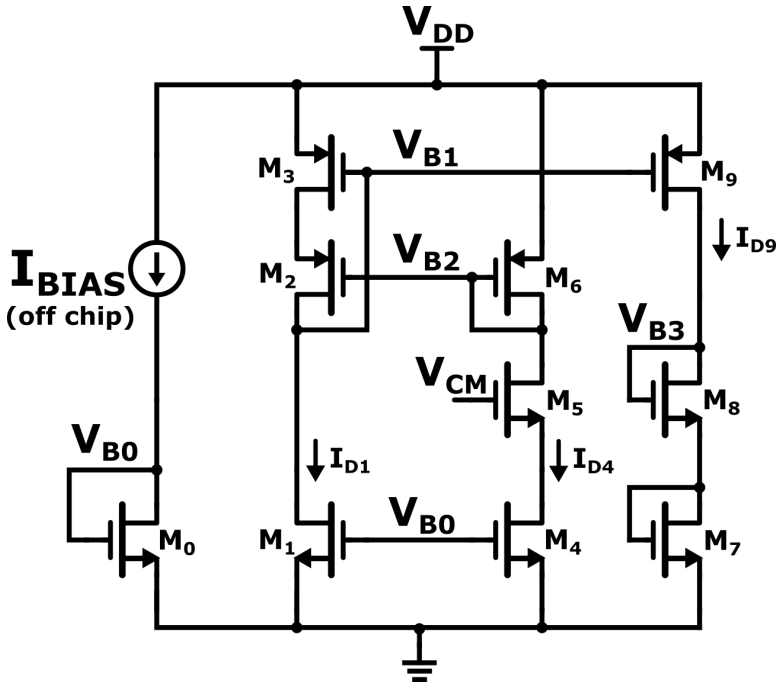


Figure 2.44: Bias-generation circuit for the OTA in the ADC.

Parameter	**Value**	**Parameter**	**Value**
$(W/L)_0$	$40\,\mu$m/$2\,\mu$m	$(W/L)_9$	$6\,\mu$m/$0.18\,\mu$m
$(W/L)_{1,4,7}$	$20\,\mu$m/$2\,\mu$m	I_{BIAS}	$400\,\mu$A
$(W/L)_{2,3,5}$	$12\,\mu$m/$0.18\,\mu$m	I_{D1}	$200\,\mu$A
$(W/L)_6$	$2\,\mu$m/$0.18\,\mu$m	I_{D4}	$200\,\mu$A
$(W/L)_8$	$3\,\mu$m/$0.18\,\mu$m	I_{D9}	$100\,\mu$A

Table 2.9: ADC bias-generation circuit parameter summary.

2.6.3 Non-Overlapping Clock Generation

Although the ADC clock source is off chip, an internal circuit is used to generate the non-overlapping phases used by the SC networks in each stage. Figure 2.45 shows our non-overlapping clock generator, where ϕ_1 and ϕ_2 are opposite-phase outputs such that one will always go to a logic low value before the other goes high, ensuring that no two switches controlled by opposite phases are ever closed simultaneously. In addition, ϕ_1' and ϕ_2' are slightly-advanced versions of ϕ_1 and ϕ_2 that are used to minimize signal-dependent charge injection in the SC circuits. For example, switch S_1 in Figure 2.26 will open right before switches S_2 and S_3 close to put the amplifier in feedback and redistribute the sampled charge. The simulated range of non-overlap intervals over process corner simulations is 280 ps–375 ps.

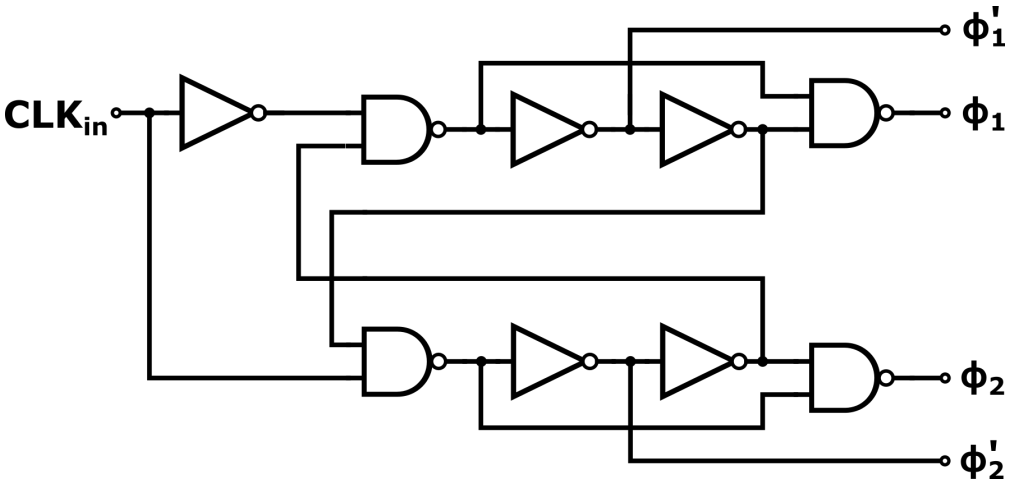


Figure 2.45: Non-overlapping clock generator used to drive the ADCs.

Following the non-overlapping clock generator, the complements of each of the four phases are generated with extra inverters, since all the SC switches are transmission gates driven by differential clocks. The eight clock signals are then fanned out to a set of cascaded inverter buffers driving each ADC individually to ensure high-quality clocks for all ADCs.

2.6.4 On-Chip Test Circuits

In order to carry out functional and performance testing of our ROIC, we equip one of the pixel banks and its associated ADC with a set of external inputs and outputs. One of these inputs allows the option to apply an external voltage input pulse to generate a charge packet on chip. To enable this, we have added a capacitor $C_{test} = 6.79\,\text{fF}$ in series with the test pixel input node, as shown in Figure 2.46. This allows an externally-sourced voltage step to inject a charge Q_{test} into the input node, equivalent to $Q_{test} = C_{test}V_{in}$. In order to minimize the number of I/O pins used for test circuits, the eight external pixel inputs are multiplexed to a single chip input pin.

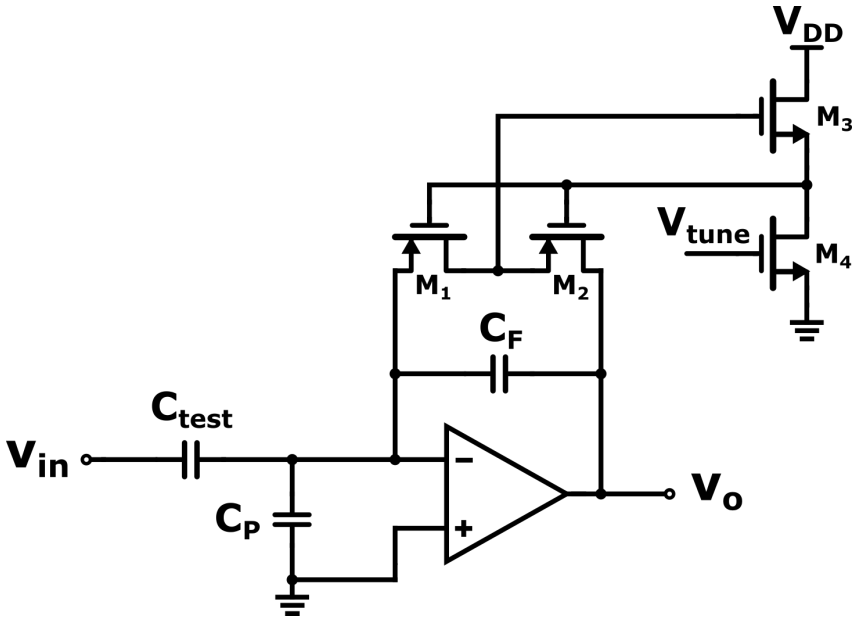


Figure 2.46: CSA circuit with test input.

To evaluate the performance of the CSAs alone, we can probe the output of each CSA off chip as well. In order to minimize additional load capacitance on the CSA, the outputs are buffered by a source follower to drive off chip, and are multiplexed similar to the test pixel inputs.

Testing of the entire pixel bank is also made possible by tapping the differential output of the summed signal. This output is buffered with a low-output-impedance differential amplifier in order to drive external capacitive loads, such as an oscilloscope.

Finally, a differential input to the ADC is available so that we can characterize its performance with external stimuli. We include a set of switches to select whether the bank output is connected to the external buffer or ADC input, while the external ADC input can be enabled or disabled.

2.6.5 Digital Configuration

For our test infrastructure described in the previous section, we use several configuration bits to select the various input and output modes. We set these bits with a scan chain driven by an off-chip microcontroller. The scan chain is a shift register, consisting of cascaded flip flops, that is set by sending a control word in through a serial-data input and clocking the register until it is fully loaded. With the scan chain clock then turned off, the bits remain stored in the register and statically apply their outputs to the multiplexing and selection switches. In addition to the test switches, we include an 8-bit-wide multiplexer to select which ADC output is being sent to the parallel output pins.

2.6.6 Other Buffering

Following the ADC output multiplexer is a set of output buffers sized to drive an external logic analyzer input termination at 200 MHz. Since this load is several pFs, buffering is achieved by cascading an even number of inverters of increasing size and drive strength.

Another set of buffers is used for the carrier frequency clocks that drive the pixels. Since the external clock generator is single ended, the complementary phase is also generated by an inverter before being buffered in parallel with the input phase. The total load driven by each of these buffers is around 150 fF, including wiring capacitance.

2.7 Chip Architecture and Layout

In this section we discuss the layout and physical organization of the ROIC. We first present primary constraints and floorplanning, along with the top-level layout. Then we discuss pixel and ADC layouts in more detail.

2.7.1 Full ROIC Layout

We begin floorplanning the full ROIC by deciding on the number of pixel banks and associated ADCs to include. Based on layout-area estimations of these blocks and the total budgeted area, we include 16 banks and ADCs within a total chip area of $2.0 \times 3.5\,\mathrm{mm}^2$. Although other arrangements are possible, grouping the banks as columns in the array allows for row-wise distribution of bias and oscillator signals to the pixels, while the output lines are oriented vertically. Since our target application is a line-scanning system, we could expand the array simply by adding more bank columns. This means that the area above and below the pixel array can be used for the ADCs, and can be similarly expanded in a larger-area chip. Since the ADCs can be placed on both sides of the array, the pitch-matching requirements are loosened, and each ADC can therefore span the width of two pixels ($70\,\mu\mathrm{m}$). With the pixel array and ADCs sized appropriately, supporting circuits such as biases, voltage references, and test circuits, can be placed in close proximity to their main distribution lines into the arrays. Figure 2.47 shows the layout of the full chip and the floorplan of the main blocks. We have omitted metals M3 and M4 from the image since they are used to make a power-supply grid covering most of the chip.

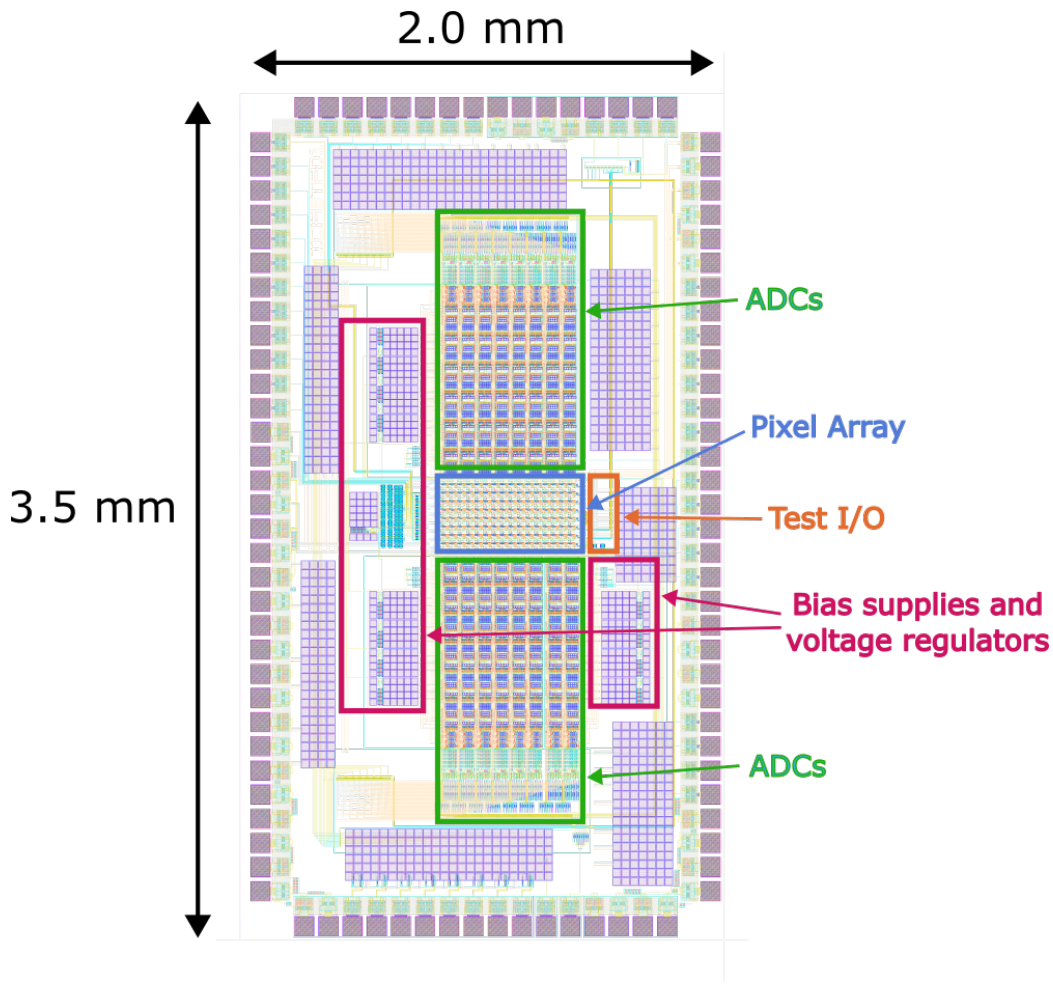


Figure 2.47: Full chip layout.

Not identified in Figure 2.47 are the arrays of MIM capacitors that decouple the power supply rails, output multiplexer, output buffers, clock generator, and scan chain.

We implement separate power domains to reduce interference between the SC ADCs and sensitive pixel analog circuits. We use dedicated supplies for the pixel array, analog ADC blocks, digital ADC blocks, and output drivers. A fifth power domain is also supplied to the analog blocks in two of the ADCs used for testing, making it possible to disable the other ADCs for a potentially quieter environment during testing. These power domains are

summarized in Table 2.10. For an added layer of isolation, we place each of the separate ADC blocks in their own deep n-well (DNW), fully surrounded by guard rings.

Power Domain	**Circuit Blocks**
AVDD/AVSS	ADC analog blocks
TVDD/TVSS	Test ADC analog blocks
DVDD/DVSS	ADC digital blocks
PVDD/PVSS	Pixels
OVDD/OVSS	Output drivers
VDD/VSS	P-substrate and n-well connections

Table 2.10: Power domains.

The pad ring on the chip periphery has 96 bond pads, each with its own ESD protection circuit. Other ESD protection is included on power rails by adding clamping diodes, as well as anti-parallel diodes between supplies and grounds. With five power domains, testing I/O, and many bias, reference, and clock inputs, a major constraint on the prototype design is the overall pin count. Without the time budget to design a high-speed serialized output block, we drive a single 8-bit parallel ADC output off chip at a time. For this reason, we include the output multiplexer to select any of the 16 ADCs.

2.7.2 Pixel Layout

The pixel layout with highlighted circuit blocks is shown in Figure 2.48. Pixel dimensions are $35 \times 35\,\mu\text{m}^2$, while each pixel pad exposed on the top side of the ROIC measures $10 \times 10\,\mu\text{m}^2$ and is located directly above the CSA input node. Signal flow through the pixel occurs in a clockwise direction, from the CSA, through the mixer and LPF, and finally, to the output block consisting of the differential pair that drives the vertical summing bus lines for the associated pixel bank.

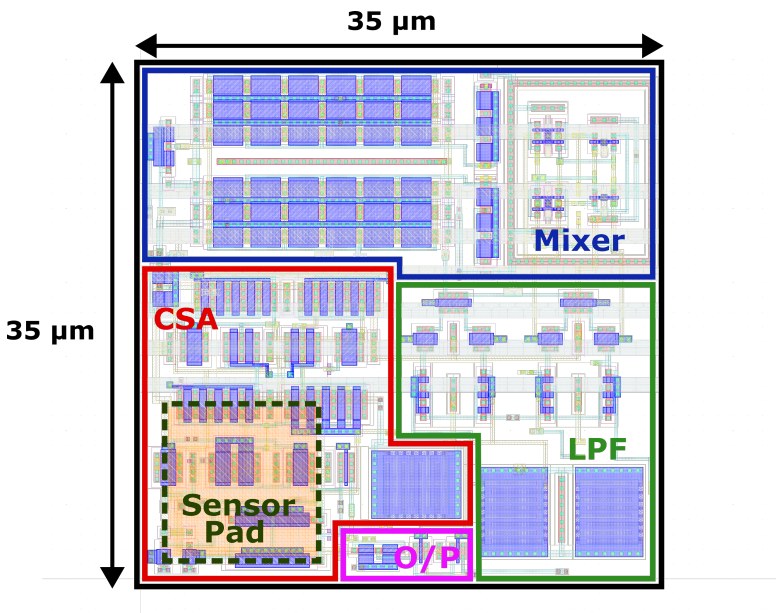


Figure 2.48: Pixel layout.

2.7.3 Pixel Array Layout

The 8 × 16 pixel array layout is shown in Figure 2.49. Arranging each bank as a column allows the oscillator signals to run horizontally, such that each pixel row operates with a unique carrier frequency. The rightmost pixel bank in the array is the dedicated test bank with access to external I/O pins. The second bank from the right has an added feature where the input node is also connected to an I/O pad on the periphery for use with an external X-ray sensor. Below and above each adjacent pair of pixel banks are their respective summer circuits, which are 70-μm wide to match the layout width of the corresponding ADCs.

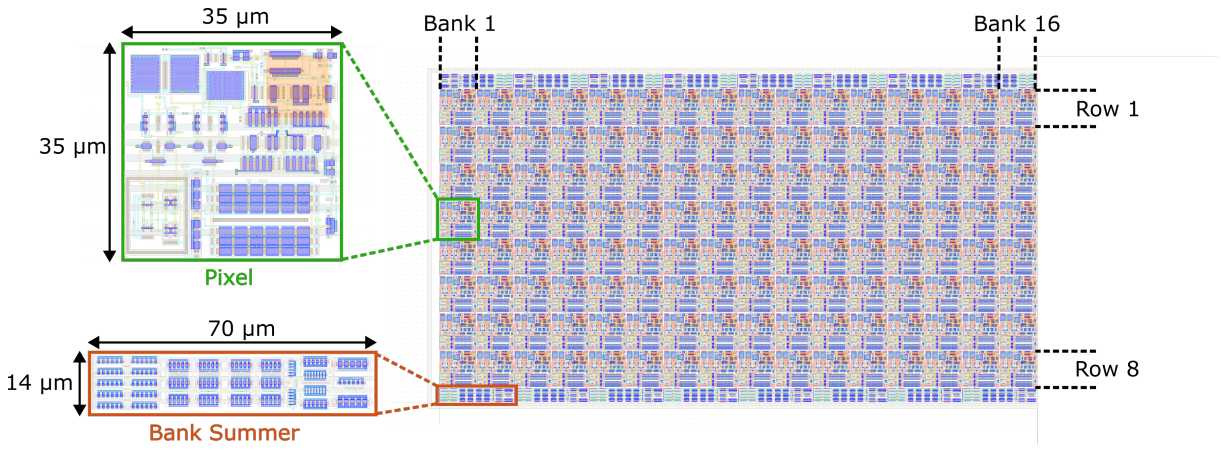


Figure 2.49: Pixel array layout.

2.7.4 ADC Layout

The ADC layout is shown for the lower set of ADCs in Figure 2.50. The pipelined nature of the ADCs allow for the long narrow column layout with a 70-μm pitch. The lower bank also includes two ADCs running on the separate testing supply voltage rail in their own DNW. These two ADCs correspond to the two rightmost pixel banks discussed above. We also indicate the primary ADC blocks, the 1.5-bit and 2-bit analog stages, and the digital block including the delay lines and decoder circuit.

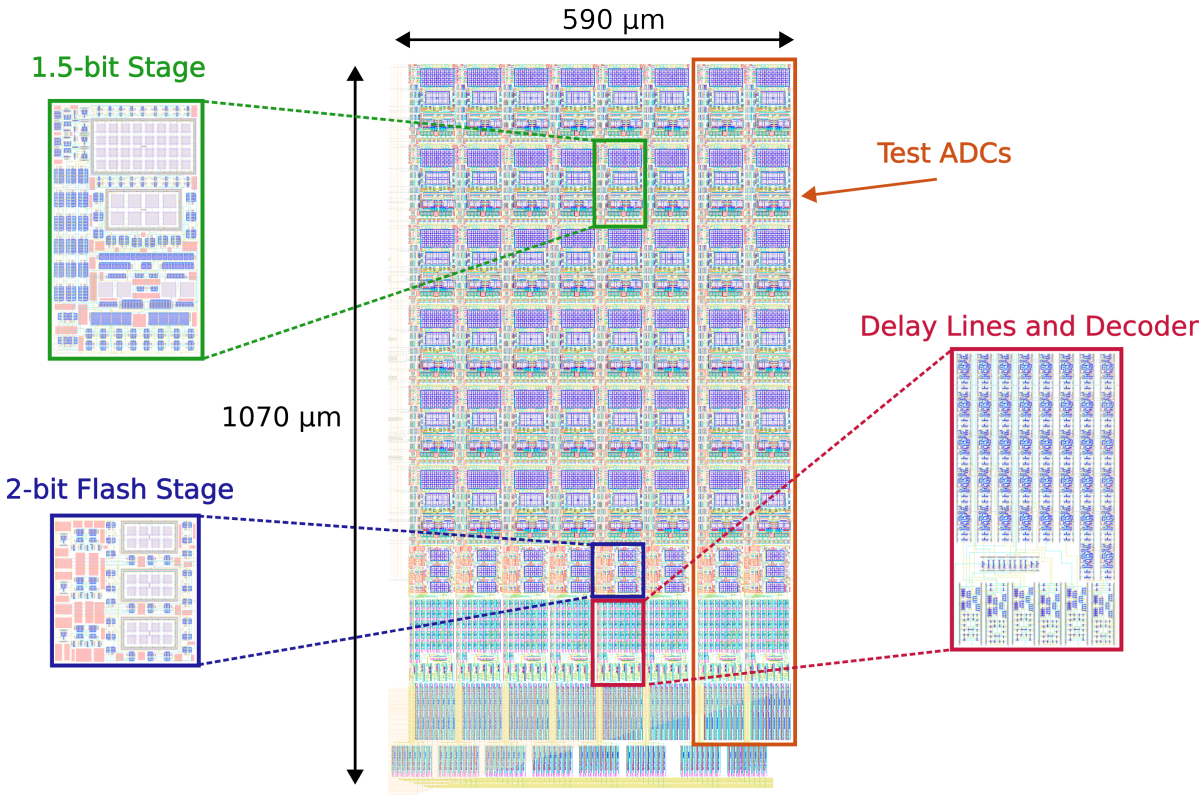


Figure 2.50: ADC layout.

The bottom rows of circuits include the digital output buffers that drive the output multiplexer, and the clock input buffers that drive the sampling clock lines running between each ADC.

2.8 System-Level Functional Simulation Results

To evaluate the functionality of our ROIC, we run simulations using the Cadence Ultrasim simulator. This allows us to verify scan-chain operation, ensure configuration bits are set properly, and allows an input-pad-to-output-pad test through the ADC, done using

extracted parasitic capacitances. In Figure 2.51, we show the simulated ADC input and output through the on-chip test circuit. The time axis begins at $0.5\,\mu s$ since the beginning of the simulation is used to set digital configuration bits through an Ultrasim vector file.

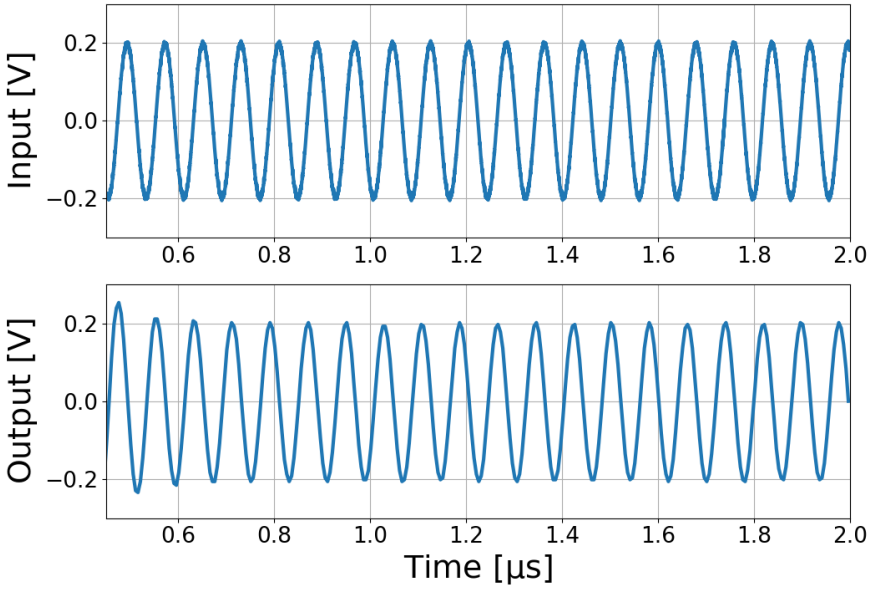


Figure 2.51: Results from full-chip post-layout ADC functional simulation.

We also perform functional verification of the full signal chain by applying input pulses to all eight pixels in a bank and reading the corresponding ADC output. The STFT result of this test is shown in Figure 2.52.

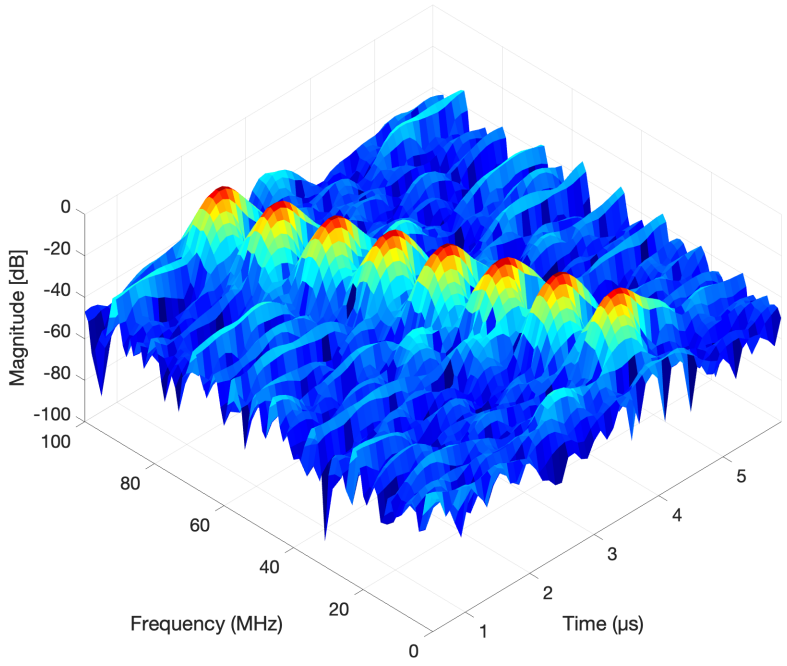


Figure 2.52: STFT of the simulated ADC output for pulse inputs on a full bank of pixels.

Table 2.11 shows a summary of the simulated performance of our ROIC in comparison with previous works. We have calculated the approximate number of available energy bins using the system-level ENC result and the linear range of input charge. Final power consumption per pixel is lower than the target specification, while ENC and CSA gain are also within the specification. The transistor count for the entire chip exceeds 52000.

Reference	[50]	[15]	[18]	[14]	[22]	[7]	[13]	**Our Design (Simulated)**
Year	2012	2010	2011	2012	2011	2013	2016	2023
CMOS Process (nm)	180	130	130	180	180	130	130	180
X-Ray Sensor	Si	Various	Si	Si	Si	HgI_2	Si	a-Se
Readout Method	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per bank (FDM)
Array Size	160 × 1	256 × 256	16 × 16	96 × 192	16 × 16	128 × 128	128 × 256	8 × 16
Pixel Size (um^2)	4000 × 25	55 × 55	220 × 220	100 × 100	100 × 100	60 × 60	75 × 75	35 × 35
# Energy Bins	8	2 to 8	16	2	1	3	2	25
CSA Gain (mV/ke^-)	2.1	11.4	11	42.5	400	107	50.3	11.4
ENC (e^-_{rms})	214	130	160	168	15	68	123	104 (pixel) 199 (system)
Max Input Flux ($photons/mm^2/s$)	170M	87M	∼100M	∼200M	10M	278M	220M	100M
Pixel Power (μW)	5000	15	18	23	20	4.6	26	48.5

Table 2.11: Simulated performance of our ROIC in comparison to previous works.

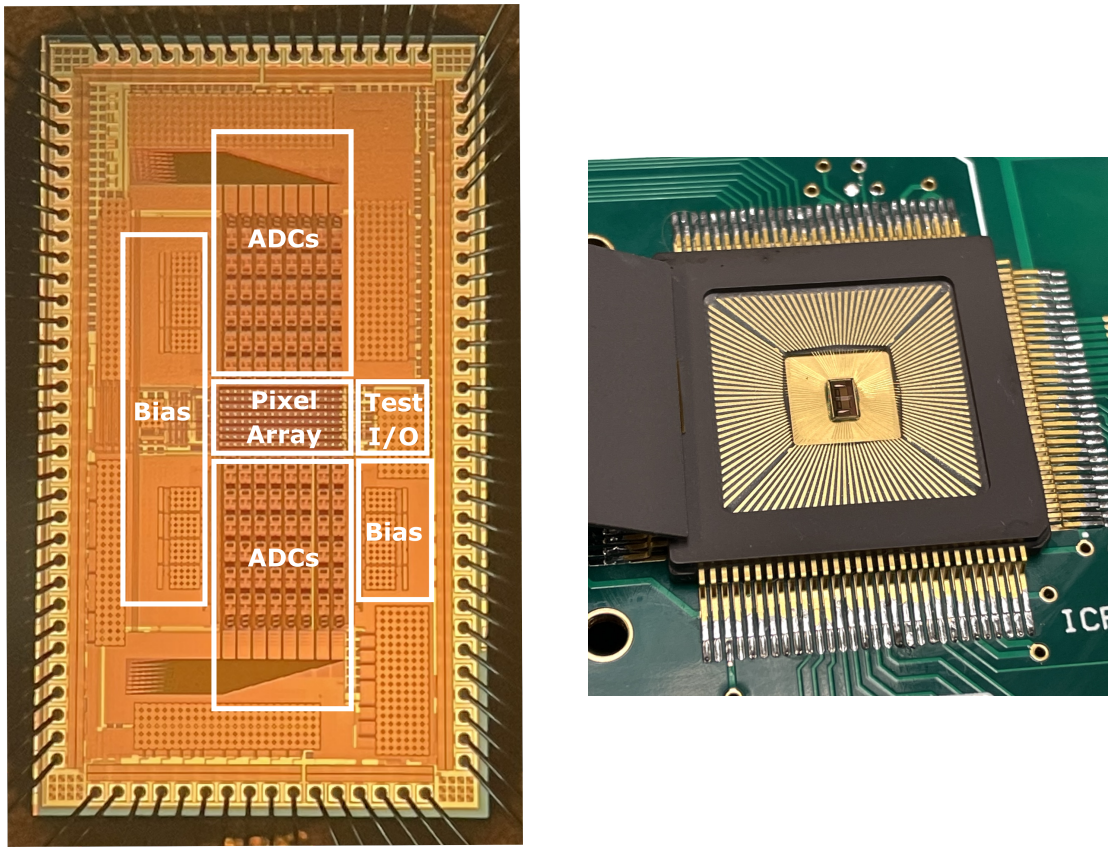
Chapter 3

Experimental Results

In this chapter we present experimental results from the characterization of our fabricated ROIC prototype. First, we discuss our test infrastructure, with a description of our PCB design and test instrumentation setup. Next, we present results from electrical characterization of our ROIC for each of the main circuit blocks.

3.1 Fabricated ROIC

A microscope image of our fabricated $3.5 \times 2.0\,\mathrm{mm}^2$ CMOS ROIC is shown in Figure 3.1(a). Our ROIC is packaged in a 120-pin ceramic quad flat packages (QFPs). A second footprint for the same package is included on the PCB to facilitate the possibility of using an external sensor. Figure 3.1(b) shows the packaged device with the lid lifted to reveal the ROIC wirebonded to the pad frame.



(a) (b)

Figure 3.1: (a) A microscope image of the fabricated ROIC and (b) the ROIC in its package.

3.2 Printed-Circuit Board Design

Figure 3.2 shows the custom four-layer PCB we designed to evaluate the performance of our ROIC. Outlined on the PCB are the different circuit sections, including power-supply regulators, high-voltage inputs, current sources, voltage reference sources, clock supplies, a microcontroller for digital control, and input and output blocks for both analog and digital signals.

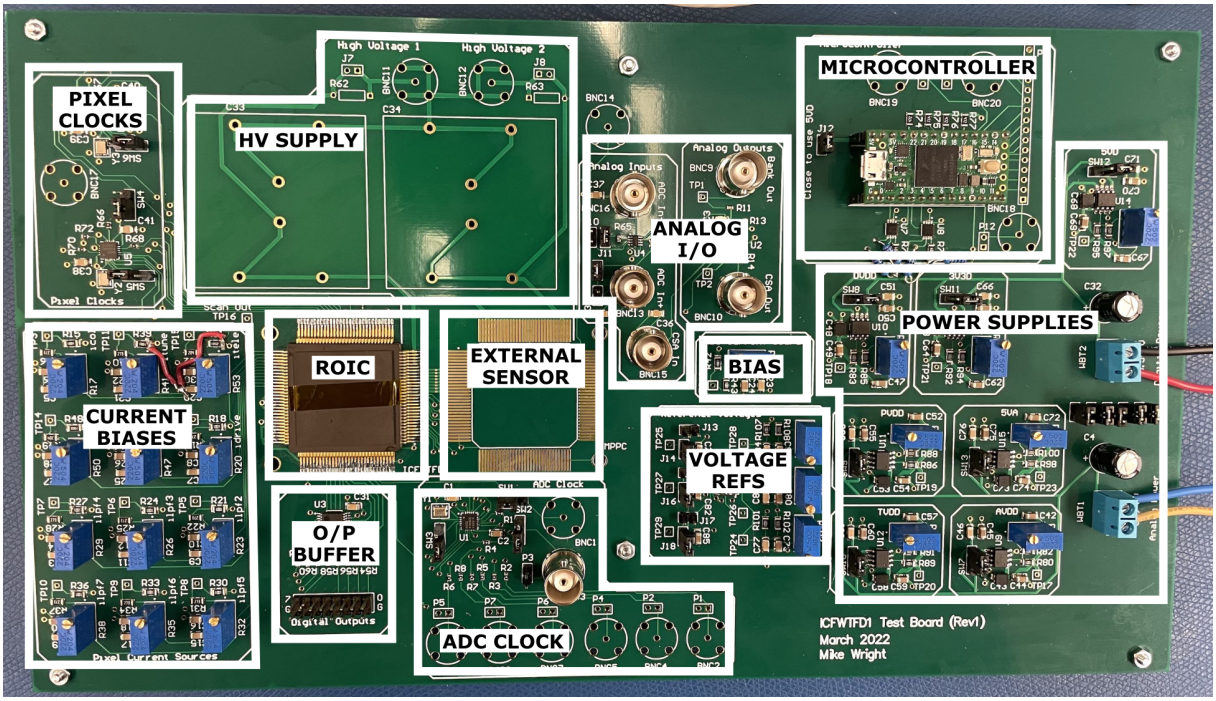


Figure 3.2: Printed-circuit board for testing.

3.2.1 Power Supplies

To power the ROIC and other supporting components, we use a set of linear-low-dropout voltage regulators to generate the various power rails. Included are three analog 1.8 V supplies for the pixel array (PVDD and VDD), ADCs (AVDD), and the two test ADCs (TVDD). We use an additional 1.8 V regulator for the digital ROIC circuits (DVDD and OVDD). On the PCB, the analog supplies share a ground plane (PVSS, AVSS, TVSS, and VSS) that is separate from the digital ground (DVSS and OVSS), which has its own plane. The two grounds are connected at a single point ("star ground") near the external supply input terminals to minimize interference between them. We include two additional digital 3.3 V and 5 V supplies referenced to the digital ground plane, used to power the microcontroller, clock generator, and output buffer. An analog 5 V supply referenced to

the analog ground plane is also included to supply power to the opamp buffers. Each of the voltage regulator outputs are decoupled with capacitors to ground. In addition to large 100 μF bulk polytantalum capacitors, smaller-value ceramic capacitors (100 nF and 10 nF) are connected in parallel to lower the total equivalent series inductance, and ensure the total impedance remains capacitive at high frequencies.

We also include high-voltage inputs on the PCB to bias an integrated or external X-ray sensor. Two inputs are provided to accommodate the use of an MPPC that requires a second bias supply for the grid layer. Supply inputs are passed through a first-order LPF using a high-voltage-tolerant film capacitor.

3.2.2 Bias, Reference, and Clock Supplies

To configure and bias the ROIC circuits, a number of current sources are needed for the various amplifiers and filters, in addition to three voltage supplies for the CM and ADC reference voltages.

The current sources directly feed diode-connected transistors in the ROIC, which are then mirrored and distributed to the various internal bias-generation circuits. To generate variable currents for these supplies, a resistor and potentiometer are connected between the power supply rails and the ROIC input nodes, as shown in Figure 3.3. We also include a decoupling capacitor to help ensure a stable input voltage.

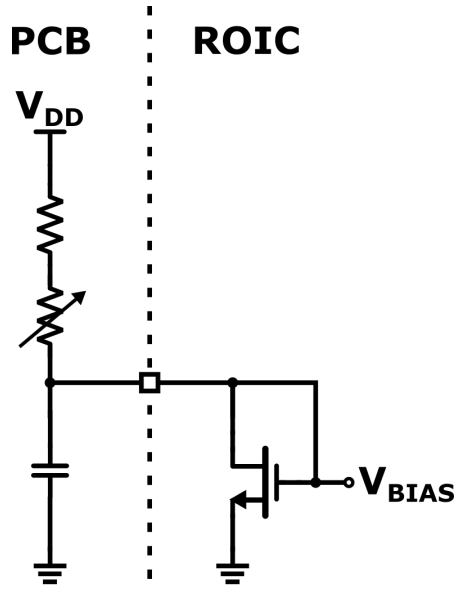


Figure 3.3: Variable bias current supply configuration.

Voltage supplies are generated using simple resistor dividers, and accompanying decoupling capacitors. Since our ROIC uses internal regulators, the supplies act as references and do not require additional buffering. However, the PCB is equipped with the option to switch in opamp buffers in case they are needed.

To generate the clock signals used by the ADC and the pixel circuits, Skyworks Si5351 variable clock-generation ICs are used. These ICs are configured using an inter-integrated circuit (I2C) bus, and use a crystal-oscillator reference. To provide flexibility in testing, we also include options to use externally-supplied clocks.

3.2.3 Input and Output Buffering

For the high-impedance analog inputs to the ROIC test circuits, direct connections are made from a function generator through a BNC cable. In addition, we include an optional unity-gain opamp buffer for the analog test inputs to the ADC test channel.

We also use a low-skew, 8-channel buffer IC to drive the test instrumentation load for the parallel digital output bus. We implement 40 Ω controlled impedance traces for the output bus in order to match the 40 Ω source impedance and minimize reflections.

3.2.4 Microcontroller

To control the configurations for the clock generator IC and the ROIC scan chain, we include a Teensy 4.0 development board with an ARM Cortex-M7 microcontroller. This board is connected to the main PCB using a pin socket, and can be powered by universal serial bus (USB) or through the digital 5 V supply provided on the PCB. Since the output logic levels of the microcontroller are on a 3.3-V rail, we use level-shifter ICs to shift the scan-chain signals to the 1.8 V supply level used by the ROIC. Additional inputs and outputs are also routed to connectors on the PCB for further flexibility.

3.3 Electrical Characterization

In this section we present the electrical characterization of our fabricated ROIC. Characterization includes analog measurements using the test pixel bank, measurements of the ADC using externally-supplied input signals, and measurement of the full signal path from pixel input to ADC output.

3.3.1 Charge Sensitive Amplifier Measurements

We use a Tektronix AFG3101 function generator to inject various stimuli into different pixel inputs within the test pixel bank by configuring the I/O multiplexers with the microcontroller. Output signals are measured using an Agilent MSO-X 3034A oscilloscope. We also create Python scripts to automate some of the input configuration and readout tasks involving the test instrumentation.

Transient Response

We begin characterizing the CSA by validating the pulse shape and width of the output pulse. In Figure 3.4, the CSA output is shown for an input charge $Q_i = 15\,\mathrm{ke}^-$. This input charge is produced by applying a voltage step input $V_i = 353\,\mathrm{mV}$ to the input test capacitor C_{test}. Since the pulse response of the CSA decays with a time constant equal to the designed value $t_{decay} = 1.177\,\mu\mathrm{s}$, the t_d specification is met, indirectly verifying that the count rate specification is also met.

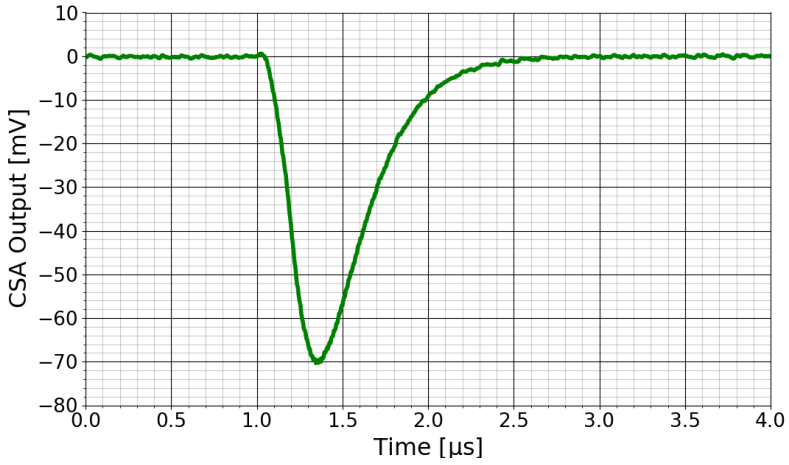


Figure 3.4: Measured CSA output for a $15\,\mathrm{ke}^-$ input applied at time $1\,\mu\mathrm{s}$.

Transfer Characteristic

Using the same configuration, we apply an amplitude sweep of input voltage steps to the test pixels in order to plot the CSA transfer characteristic for each pixel. Figure 3.5 shows the CSA transfer characteristics for each of the eight test pixels. Similar to the simulated results, we see a saturation point at an input of about $17\,\mathrm{ke}^-$, while noise distorts the curves at the lowest input charges. Charge-to-voltage gains are also indicated on the plots, where the average measured gain is $8.94\,\mathrm{mV/ke}^-$, which is slightly lower than the simulated gain of $11.4\,\mathrm{mV/ke}^-$, with a relative error of 21.6%. This is potentially explained by process

variation or by the duration of the injected charge pulse. Since the rise-time of the voltage step applied to C_{test} corresponds to the duration of the input pulse, the CSA gain will be lower if this rise time is slower than the simulated $t_p = 150\,\text{ns}$.

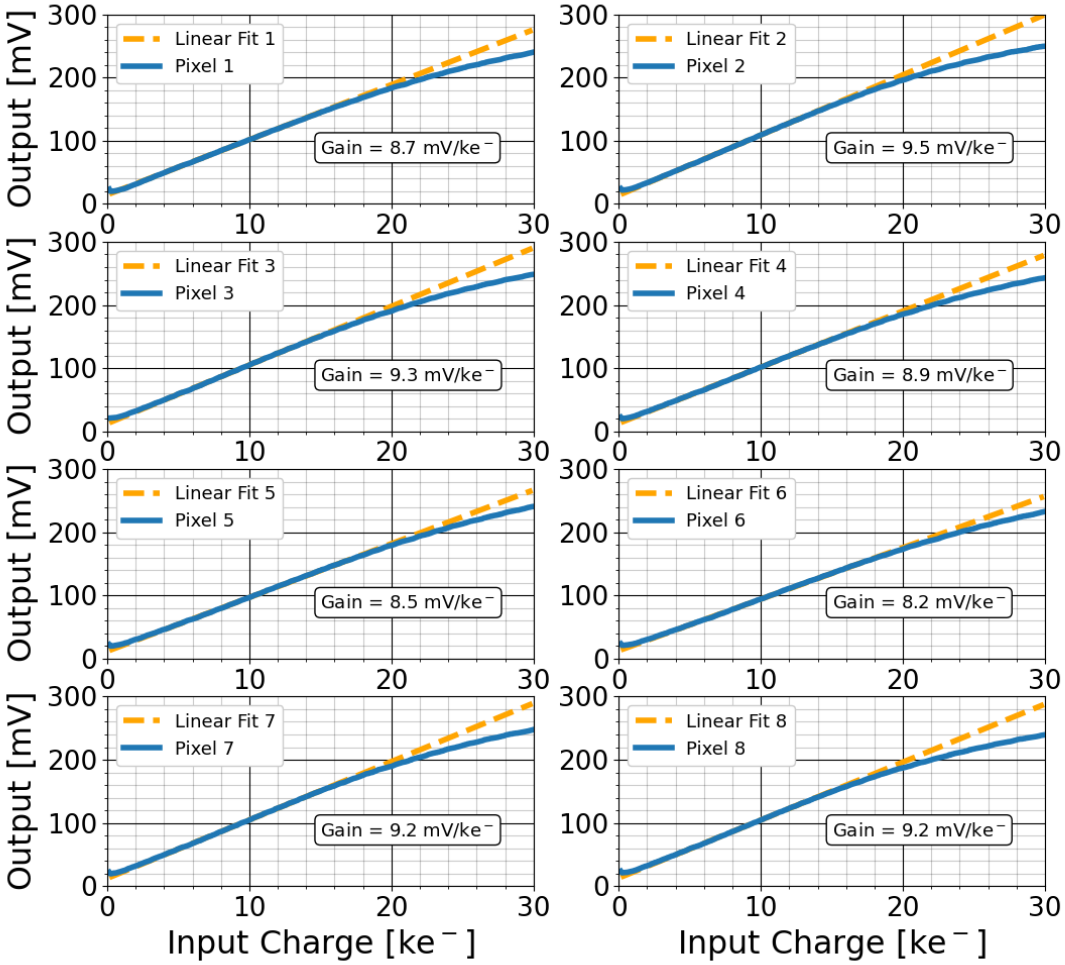


Figure 3.5: Measured CSA transfer characteristics for each test pixel.

Noise

We measure noise performance of the test-pixel CSAs by acquiring the output without applying any input signal. Since the input terminal to C_{test} is now floating, it does not contribute to parasitic input capacitance. Sampling the CSA output voltage with a bandwidth equal to its f_{ENBW} allows us to quantify the output noise.

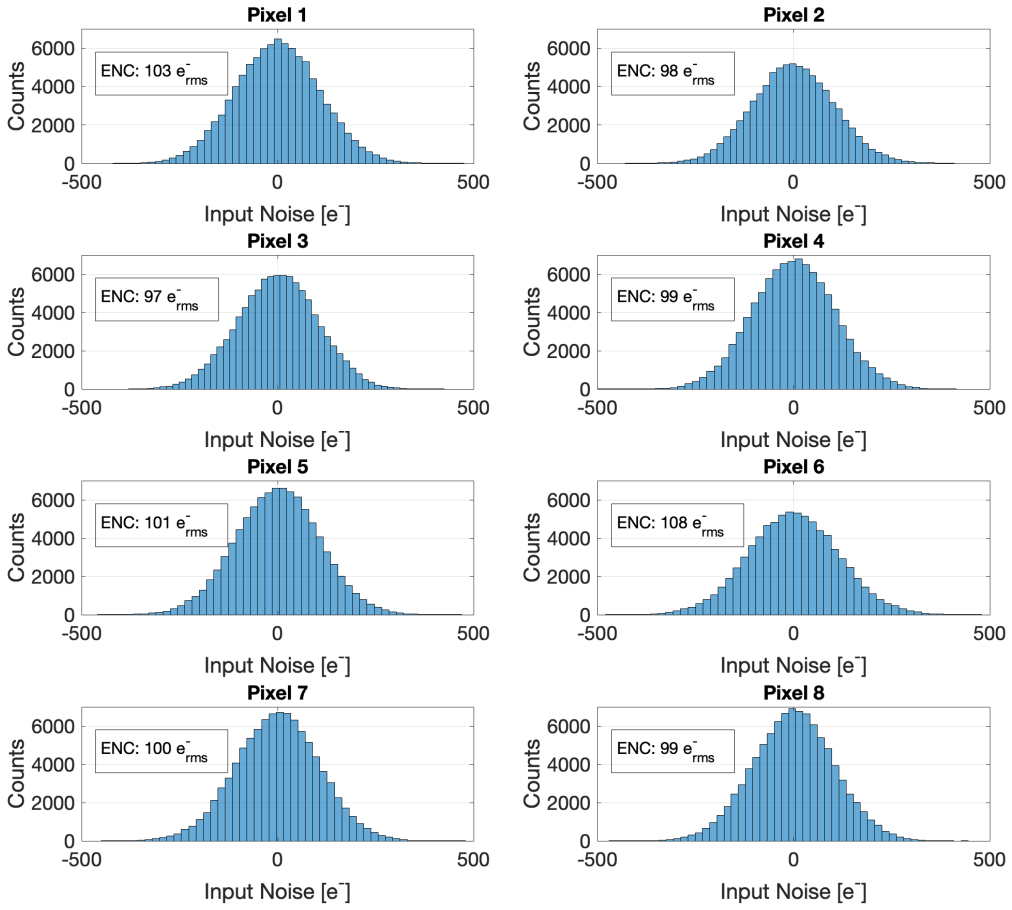


Figure 3.6: Measured CSA output noise histograms for each test pixel.

Figure 3.6 shows a histogram of the CSA input noise for each pixel. This noise is clearly Gaussian in nature, thus taking the standard deviation directly gives us the rms input noise. For each pixel, the measured ENC is shown in Figure 3.6, with an average ENC of 100.8 e^-_{rms}. In Figure 3.7, the input-referred charge noise PSD of the CSA in Pixel 1 is shown, with a resolution bandwidth of 976 Hz. This is obtained by dividing the output referred PSD by the constant CSA gain up to f_{ENBW}. Integrating this PSD from 1 kHz up to f_{ENBW} gives an ENC of 108 e^-_{rms}, similar to the results found from the standard deviation of the histograms in Figure 3.6. Two interference tones at 65 kHz and 98 kHz are present in the PSD, and although we have not identified their source, removing these contributions from the integrated noise only reduces the ENC by 2 e^-.

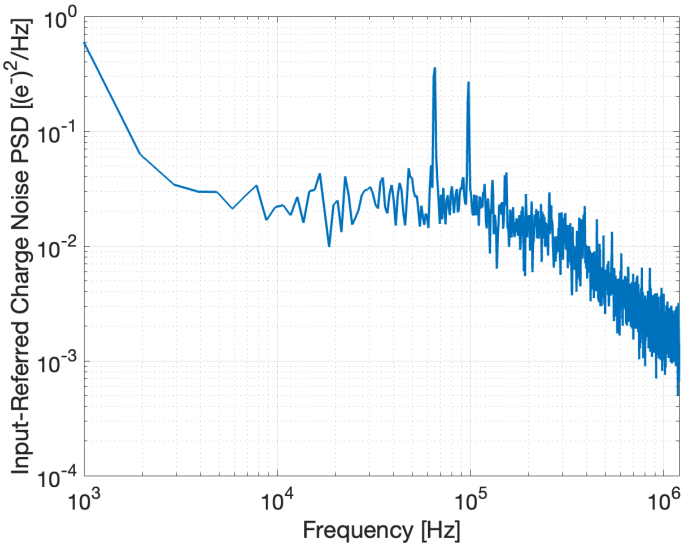


Figure 3.7: Measured input-referred charge noise PSD of the CSA.

Crosstalk

To characterize carrier-signal crosstalk between adjacent pixels, we measure the magnitude of neighbouring pixel carrier frequencies at the output of the CSA. The range of these

interference tones is between $25\,\mu V_{rms}$ and $85\,\mu V_{rms}$, approximately $10\times$ lower than the CSA output noise.

3.3.2 Pixel Bank Measurements

In Figure 3.8, the spectrum of the test bank output is shown with no input stimulus and resolution bandwidth 20 kHz. Offset voltages introduced prior to the mixer in each pixel are upconverted to the carrier frequencies and are indicated in Figure 3.8. An aliased harmonic is also present in the spectrum at 97.3 MHz, but remains outside of the signal bands.

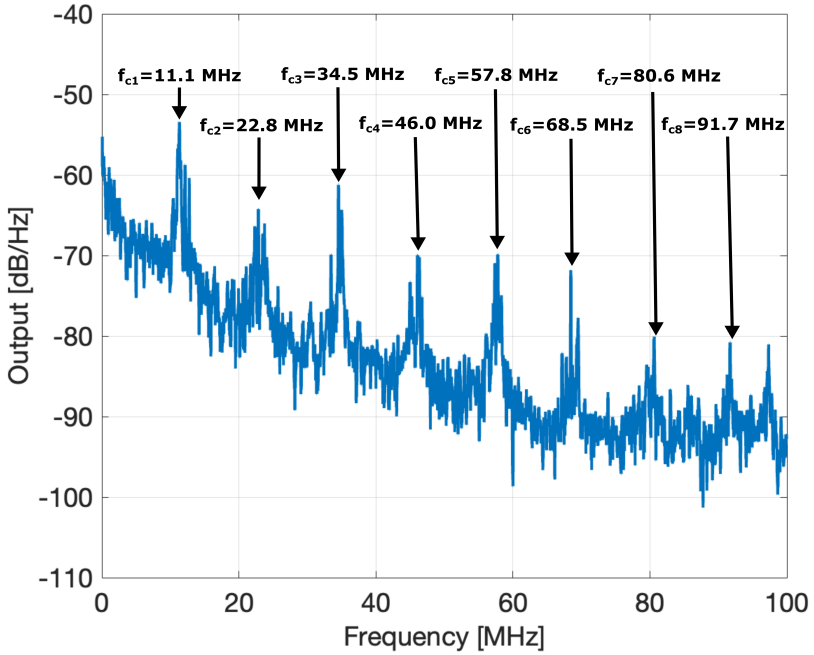


Figure 3.8: Measured test bank output spectrum.

To test the mixing operation, we measure the output of the test pixel bank while applying an input to one of the eight pixels in the bank. Using a sinusoidal input voltage

at 1 MHz, we generate a transfer characteristic for each pixel. This involves sweeping the input signal amplitude over a 15 mV to 35 mV range and measuring the corresponding sidebands from the summed output spectrum. Figure 3.9 shows the transfer curves for each pixel in the test bank.

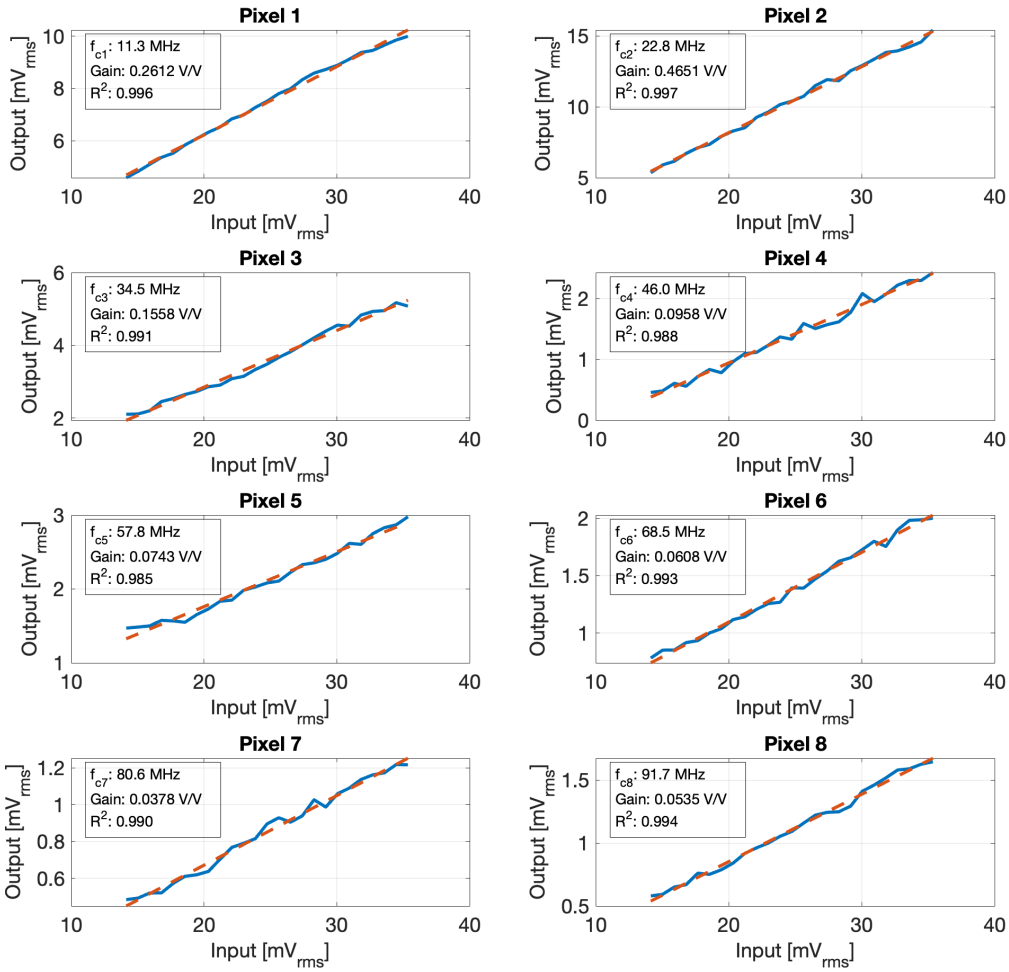


Figure 3.9: Measured transfer characteristics for each pixel in the test bank. The dashed line is a linear fit.

Unfortunately, due to a bandwidth limitation of the output buffer driving an oscilloscope, where the cutoff frequency is limited to about 60 MHz, we observe a decrease in gains over the pixel channels. However, the curves do remain linear over the input range with high R^2 values, demonstrating effective frequency translation to each of the pixel carrier frequencies. Gain variability across the pixels can be corrected with full-system calibration in post-processing by using a monochromatic radiation source.

3.3.3 ADC Measurements

To make ADC measurements, we set the I/O configuration switches so that we can apply an external input signal. We also connect a Keysight 16821A logic analyzer to the parallel digital output bus. This instrument allows us to optimize the sampling position of each input bit to compensate for any timing skew in the output lines. For the following results, we operate the ADC at $f_s = 160$ MHz to further relax potential signal integrity degradation on the output bus.

We use a sinusoidal input voltage at -2 dbFS and $f_{in} = 996$ kHz for coherent sampling. Figure 3.10 shows the time-domain output, demonstrating that the ADC is functional.

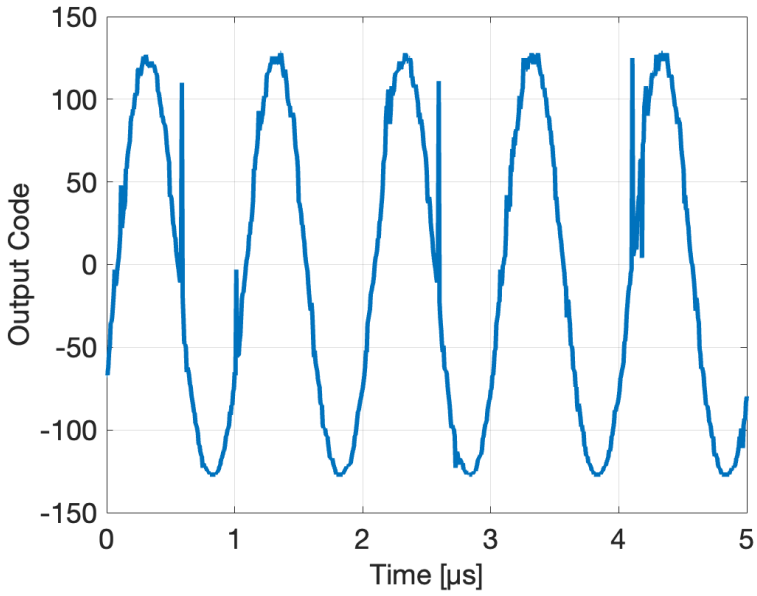


Figure 3.10: Measured ADC output with a 996 kHz sinusoidal input.

Although this output is approximately as expected, there are some bit errors indicated by the large excursions near where the signal passes through the midpoint of the input range. To investigate this further, we sweep the dc input level over the input range and find that for several input values, including the midpoint, the measured output is not constant, but fluctuates over several output levels.

The spectrum of the output is plotted in Figure 3.11 with resolution bandwidth 19.5 kHz, where the fundamental is indicated separately from noise and distortion components.

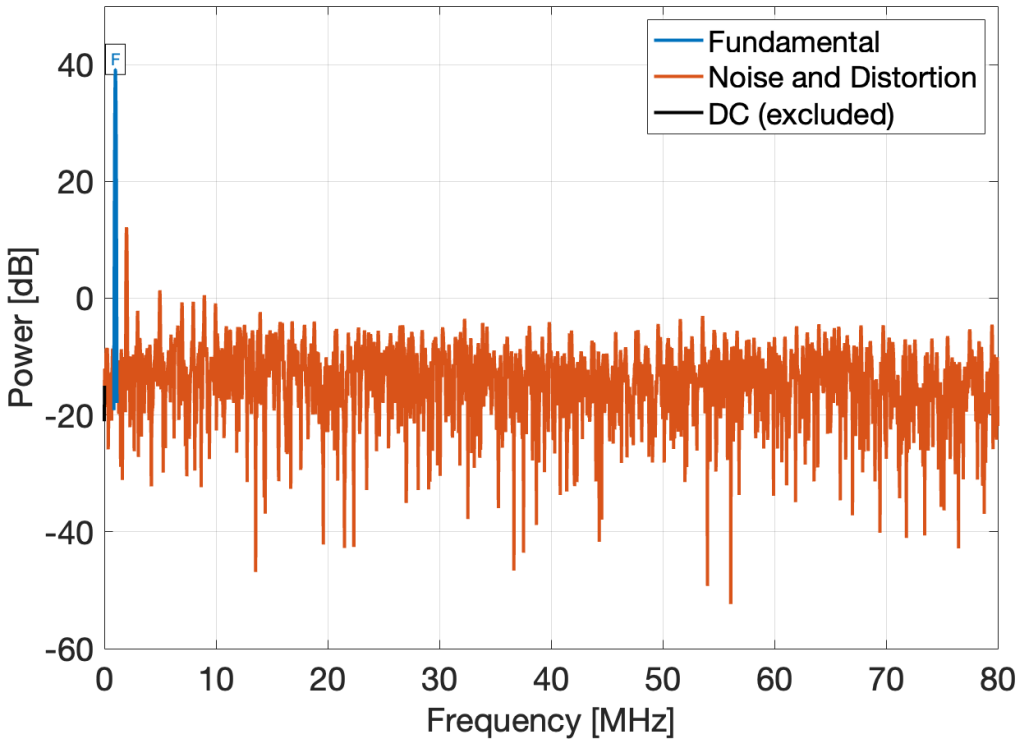


Figure 3.11: Measured ADC output spectrum from a 996 kHz sinusoidal input.

In Figure 3.12, the same plot is shown up to 10 MHz in order to better view the harmonic content. We observe that a strong second harmonic is present despite the fully-differential ADC architecture. We also note that the 3^{rd}, 5^{th}, and 7^{th} to 10^{th} harmonics remain above the noise floor.

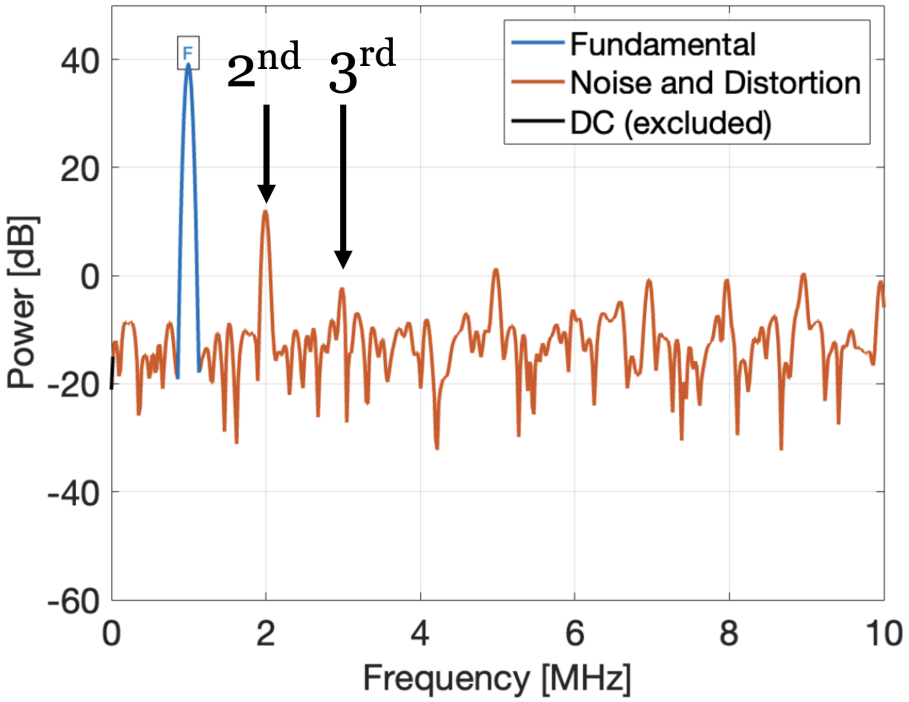


Figure 3.12: Measured ADC output spectrum from a 996 kHz sinusoidal input, zoomed into the harmonic content.

To quantify the error we see in the time-domain response, we measure the SNDR over a range of input amplitudes. Figure 3.13 shows the measured SNDR and SNR of our ADC.

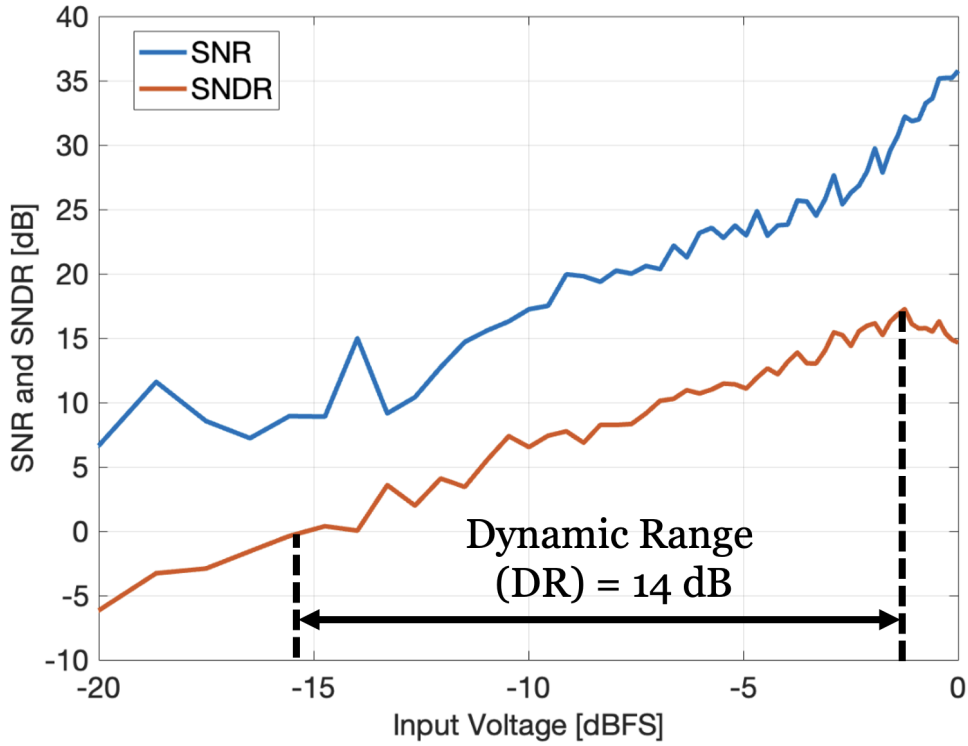


Figure 3.13: Measured SNDR and SNR of the ADC vs. input amplitude.

From this plot, the peak measured SNDR is 17.3 dB, which is equivalent to an ENOB of 2.6 bits, and the peak SNR is 35.8 dB, or 5.7 bits. In Figure 3.14 we plot the fundamental, total harmonic distortion (THD), and noise components individually. From these plots we see that the errors observed in the time-domain response manifest as a high distortion across the input range.

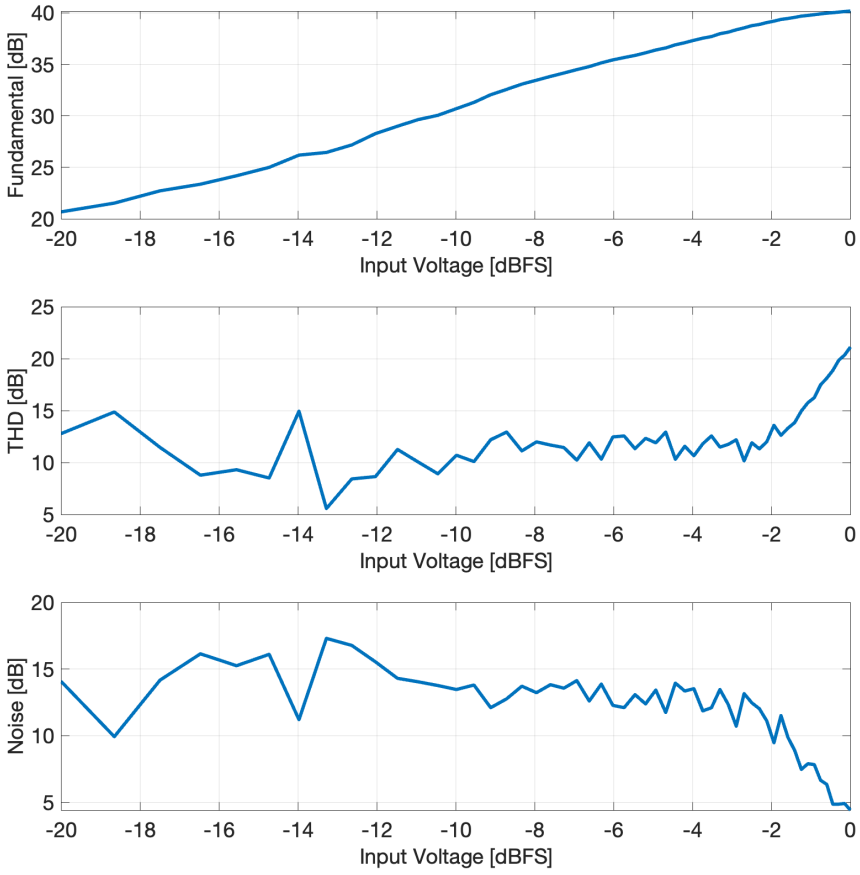


Figure 3.14: Measured fundamental, THD, and noise components plotted against input amplitude.

The most likely cause of this error is the integrity of the reference voltages used to supply the DACs in each pipeline stage. Since the regulators have single-ended outputs, they are subject to power-supply fluctuations caused by large switching currents pulled through the bondwire inductances. For a bank of ADCs sharing a set of reference voltage supplies, the current drawn from the pass devices in the regulators is dependent on the input signal values of all the ADCs, as these inputs are sampled by the comparators

which set up the DAC configurations, altering the regulator loads. This means that an input-signal-dependent ripple is introduced on the reference supplies, causing errors in the residue-voltage-generation circuits. Although this effect is seen in simulation with a bondwire inductance model, it is likely that the large decoupling capacitors on the regulator outputs are not adequate to mitigate the problem. Using differentially-supplied reference voltages with better power-supply rejection would be a better approach to deal with this problem.

3.3.4 Full System Measurements

To test the full ROIC signal path, which includes the pixel, bank, and ADC circuits, we measure the system-level transfer characteristic. In this case, the input signal is a stream of charge packets injected into the test CSA of the second pixel, which is modulated by a 16.75-MHz carrier frequency. For a 50-μs duration, ten pulses arrive at an interval of 5 μs. Figure 3.15 shows the STFT, and detected peaks, of the ADC output after the pixel channel has been post-processed using a digital bandpass filter.

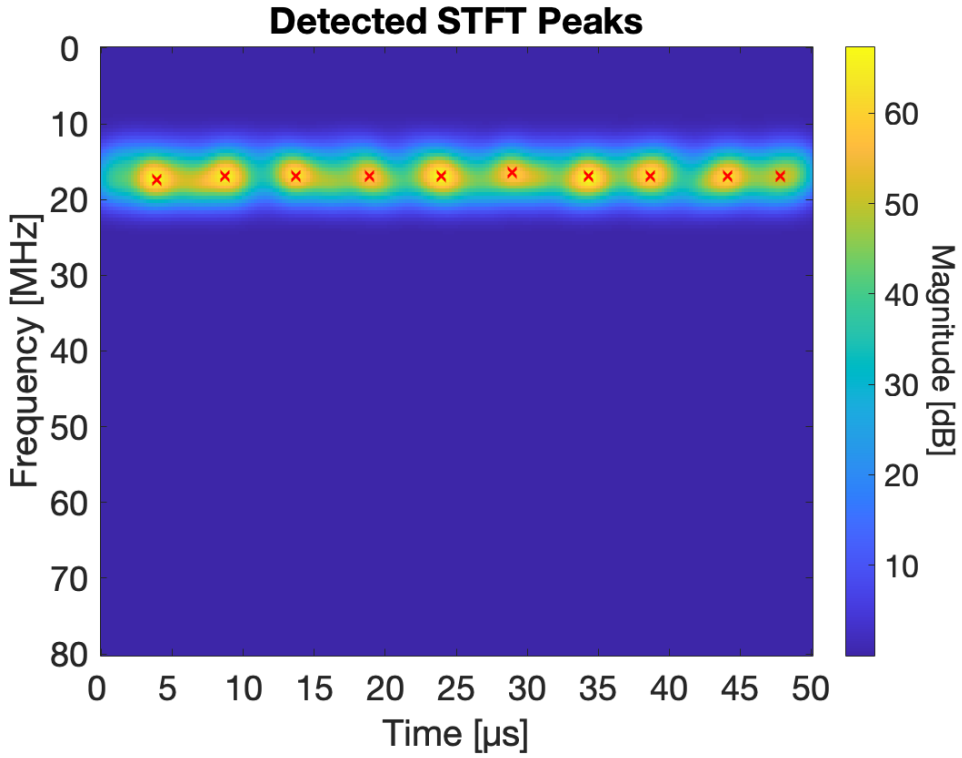


Figure 3.15: Detected pulse peaks in the STFT of the measured ADC output with a stream of input pulses.

Figure 3.16 shows the energy measured transfer characteristic of the ADC. We obtain the statistics for this plot by measuring the output energy of 100 samples at each input energy. Despite the relatively low SNDR of the ADC, the measured ENC is $683\,\mathrm{e}^-$, or $30.7\,\mathrm{keV}$ for $W_\pm = 45\,\mathrm{eV/e}^-$, while a 10% deviation from the linear fit occurs at $201\,\mathrm{keV}$, or $4.47\,\mathrm{ke}^-$.

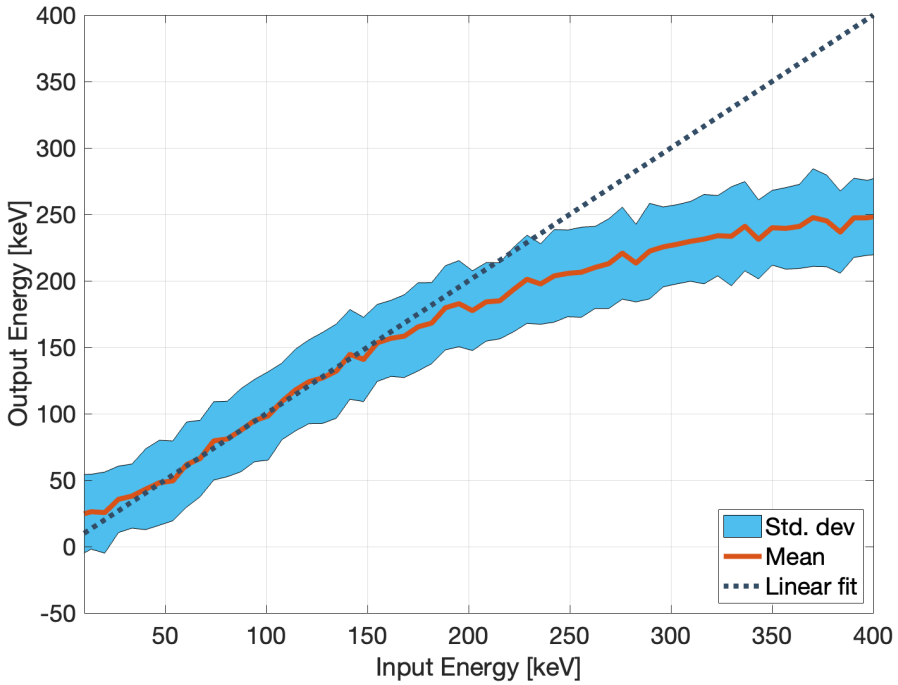


Figure 3.16: Measured system-level transfer characteristic.

3.3.5 Discussion

Although the measured ENC does not meet its specification, it is in the targeted order of magnitude for ENC, and still allows us to demonstrate the fundamental FDM-readout concept. Based on the measured ENC and linear range R, the number of energy bins is calculated as

$$no.Bins = \left\lfloor \frac{R}{ENC} \right\rfloor = \left\lfloor \frac{4470 - 683}{683} \right\rfloor = 6. \tag{3.1}$$

Measured system results are shown in Table 3.1 in comparison with previous works. Our ROIC has the smallest pixels, while also using the largest CMOS process. In addition, our CSA ENC is lower than many of the other works. Despite our relatively-high system-level ENC, we still achieve a higher number of energy bins than most of the other works.

Pixel power, CSA gain, and maximum input flux are all in the ranges of the other works.

Due to time constraints, testing the ROIC with an integrated or external X-ray sensor has not been possible at the time of writing, but is an ongoing effort.

Reference	[50]	[15]	[18]	[14]	[22]	[7]	[13]	**Our Design (Measured)**
Year	2012	2010	2011	2012	2011	2013	2016	2023
CMOS Process (nm)	180	130	130	180	180	130	130	180
X-Ray Sensor	Si	Various	Si	Si	Si	HgI_2	Si	a-Se
Readout Method	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per pixel	Per bank (FDM)
Array Size	160 × 1	256 × 256	16 × 16	96 × 192	16 × 16	128 × 128	128 × 256	8 × 16
Pixel Size (um^2)	4000 × 25	55 × 55	220 × 220	100 × 100	100 × 100	60 × 60	75 × 75	35 × 35
# Energy Bins	8	2 to 8	16	2	1	3	2	6
CSA Gain (mV/ke^-)	2.1	11.4	11	42.5	400	107	50.3	8.9
ENC (e^-_{rms})	214	130	160	168	15	68	123	101 (pixel) 683 (system)
Max Input Flux ($photons/mm^2/s$)	170M	87M	∼100M	∼200M	10M	278M	220M	100M
Pixel Power (μW)	5000	15	18	23	20	4.6	26	48.5

Table 3.1: Measured performance in comparison to previous works.

Chapter 4

Conclusion and Future Work

In this thesis, we presented the modelling, design, and testing of a novel CMOS spectrographic SPC X-ray imager. Our ROIC targets mammography and CT applications and is intended for use with an a-Se X-ray sensor. Our pixel size of only $35 \times 35\,\mu\text{m}^2$ provides the highest reported spatial resolution for an SPC imager targeting these applications. Using FDM as a means to share ADC resources among a bank of pixels allows the ADC to be physically located outside the pixel array, effectively reducing pixel area and relaxing count rate constraints at the pixel level. Our ROIC meets its power, pixel size, and count-rate specifications, while the system-level ENC is higher than expected due to ADC performance limitations. Despite these shortcomings, we have successfully demonstrated the concept of using FDM in an SPC imager and improvements to our implementation can be made in future iterations.

4.1 Future Work

In order to build on the work presented in this thesis, several improvements can be made to our first-generation ROIC:

- The use of bandpass filters, instead of LPFs, in the pixels will help minimize additive pixel noise across output bands.
- Providing a truly differential voltage reference supply to the ADCs will enable better power-supply interference rejection, ensuring stable voltage inputs to the DACs.
- Implementing high-speed serialized transmitters for the ADC output data would enable concurrent readout of multiple ADCs and provide a higher total throughput for the number of output pins used.

References

[1] E. Fredenberg, F. Kilburn-Toppin, P. Willsher, E. Moa, M. Danielsson, D. R. Dance, K. C. Young, and M. G. Wallis, "Measurement of breast-tissue X-ray attenuation by spectral mammography: solid lesions," *Physics in Medicine and Biology*, vol. 61, no. 7, pp. 2595–2612, Apr. 2016.

[2] E. H. Heijne, "History and future of radiation imaging with single quantum processing pixel detectors," *Radiation Measurements*, vol. 140, p. 106436, Jan. 2021.

[3] B. Chen, I. Reiser, J. C. Wessel, N. Malakhov, G. Wawrzyniak, N. E. Hartsough, T. Gandhi, C.-T. Chen, J. S. Iwanczyk, and W. C. Barber, "Si-strip photon counting detectors for contrast-enhanced spectral mammography," in *Medical Applications of Radiation Detectors V*, H. B. Barber, L. R. Furenlid, and H. N. Roehrig, Eds., vol. 9594, San Diego, California, United States, Aug. 2015, p. 959406.

[4] E. Fredenberg, M. Hemmendorff, B. Cederström, M. Åslund, and M. Danielsson, "Contrast-enhanced spectral mammography with a photon-counting detector," *Medical Physics*, vol. 37, no. 5, pp. 2017–2029, Apr. 2010.

[5] E. Fredenberg, M. Lundqvist, B. Cederström, M. Åslund, and M. Danielsson, "Energy resolution of a photon-counting silicon strip detector," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 613, no. 1, pp. 156–162, Jan. 2010.

[6] T. Poikela, J. Plosila, T. Westerlund, M. Campbell, M. D. Gaspari, X. Llopart, V. Gromov, R. Kluit, M. van Beuzekom, F. Zappon, V. Zivkovic, C. Brezina, K. Desch, Y. Fu, and A. Kruth, "Timepix3: A 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout," *Journal of Instrumentation*, vol. 9, no. 05, pp. C05 013–C05 013, May 2014.

[7] H.-S. Kim, S.-W. Han, J.-H. Yang, S. Kim, Y. Kim, S. Kim, D.-K. Yoon, J.-S. Lee, J.-C. Park, Y. Sung, S.-D. Lee, S.-T. Ryu, and G.-H. Cho, "An asynchronous sampling-based 128 x 128 direct photon-counting X-ray image detector with multi-energy discrimination and high spatial resolution," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 541–558, Feb. 2013.

[8] R. Ballabriga, J. Alozy, M. Campbell, E. Frojdh, E. Heijne, T. Koenig, X. Llopart, J. Marchal, D. Pennicard, T. Poikela, L. Tlustos, P. Valerio, W. Wong, and M. Zuber, "Review of hybrid pixel detector readout ASICs for spectroscopic X-ray imaging," *Journal of Instrumentation*, vol. 11, no. 01, pp. P01 007–P01 007, Jan. 2016.

[9] M. Danielsson, M. Persson, and M. Sjölin, "Photon-counting X-ray detectors for CT," *Physics in Medicine & Biology*, vol. 66, no. 3, Feb. 2021.

[10] C. Sundberg, M. Persson, A. Ehliar, M. Sjölin, J. Wikner, and M. Danielsson, "Increased count-rate performance and dose efficiency for silicon photon-counting detectors for full-field CT using an ASIC with adjustable shaping time," in *Medical Imaging 2019: Physics of Medical Imaging*, H. Bosmans, G.-H. Chen, and T. Gilat Schmidt, Eds. San Diego, United States: SPIE, Mar. 2019.

[11] A. Rivetti, *CMOS: Front-End Electronics for Radiation Sensors*, ser. Devices, Circuits, and Systems Series. Boca Raton, FL, USA: CRC Press, 2017.

[12] H. Spieler, "Front-end electronics and signal processing," in *AIP Conference Proceedings*, vol. 674. Morelia, Michoacan (Mexico): AIP, 2003, pp. 76–100.

[13] P. Grybos, P. Kmon, P. Maj, and R. Szczygiel, "32k channel readout ic for single photon counting pixel detectors with pitch, dead time of 85 ns, offset spread and 2% rms gain spread," *IEEE Transactions on Nuclear Science*, vol. 63, no. 2, pp. 1155–1161, Apr. 2016.

[14] P. Maj, P. Grybos, R. Szczygiel, M. Zoladz, T. Sakumura, and Y. Tsuji, "18k Channels single photon counting readout circuit for hybrid pixel detector," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 697, pp. 32–39, Jan. 2013.

[15] R. Ballabriga, "The design and implementation in 0.13um CMOS of an algorithm permitting spectroscopic imaging with high spatial resolution for hybrid pixel detectors," Ph.D. dissertation, E.T.S. d'Enginyeria Electrònica i Informatica La Salle, 2009.

[16] R. Ballabriga, J. Alozy, G. Blaj, M. Campbell, M. Fiederle, E. Frojdh, E. H. M. Heijne, X. Llopart, M. Pichotka, S. Procz, L. Tlustos, and W. Wong, "The Medipix3RX: A high resolution, zero dead-time pixel detector readout chip allowing spectroscopic imaging," *Journal of Instrumentation*, vol. 8, no. 02, pp. C02 016–C02 016, Feb. 2013.

[17] R. Ballabriga, M. Campbell, and X. Llopart, "An introduction to the Medipix family ASICs," *Radiation Measurements*, vol. 136, p. 106271, Aug. 2020.

[18] W. Wong, G. Anton, R. Ballabriga, M. Böhnel, M. Campbell, E. Heijne, X. Llopart, T. Michel, I. Münster, R. Plackett, P. Sievers, P. Takoukam, L. Tlustos, and P. Valerio, "A pixel detector asic for dosimetry using time-over-threshold energy measurements," *Radiation Measurements*, vol. 46, no. 12, pp. 1619–1623, Dec. 2011.

[19] X. Llopart, R. Ballabriga, M. Campbell, L. Tlustos, and W. Wong, "Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 581, no. 1-2, pp. 485–494, Oct. 2007.

[20] T. Poikela, M. D. Gaspari, J. Plosila, T. Westerlund, R. Ballabriga, J. Buytaert, M. Campbell, X. Llopart, K. Wyllie, V. Gromov, M. van Beuzekom, and V. Zivkovic, "VeloPix: The pixel ASIC for the LHCb upgrade," *Journal of Instrumentation*, vol. 10, no. 01, pp. C01 057–C01 057, Jan. 2015.

[21] M. D. Gaspari, J. Alozy, R. Ballabriga, M. Campbell, E. Fröjdh, J. Idarraga, S. Kulis, X. Llopart, T. Poikela, P. Valerio, and W. Wong, "Design of the analog front-end for the Timepix3 and Smallpix hybrid pixel detectors in 130 nm CMOS technology," *Journal of Instrumentation*, vol. 9, no. 01, pp. C01 037–C01 037, Jan. 2014.

[22] B. Dierickx, B. Dupont, A. Defernez, and N. Ahmed, "Indirect X-ray photon-counting image sensor with 27T pixel and 15e- rms accurate threshold," in *2011 IEEE International Solid-State Circuits Conference*. San Francisco, CA, USA: IEEE, Feb. 2011, pp. 114–116.

[23] M. A. Disi, A. M. Zaki, Q. Fan, and S. Nihtianov, "High-count rate, low power and low noise single electron readout ASIC in 65nm CMOS technology," in *2021 XXX International Scientific Conference Electronics (ET)*. Sozopol, Bulgaria: IEEE, Sep. 2021, pp. 1–5.

[24] A. Peizerat, J.-P. Rostaing, P. Ouvrier-Buffet, S. Stanchina, P. Radisson, and E. Marche, "A 256 energy bin spectrum X-ray photon-counting image sensor providing 8Mcounts/s/pixel and on-chip charge sharing, charge induction and pile-up corrections," in *2017 Symposium on VLSI Circuits*. Kyoto, Japan: IEEE, Jun. 2017, pp. C246–C247.

[25] P. Maj, P. Grybos, R. Szczygiel, P. Kmon, R. Kleczek, A. Drozd, P. Otfinowski, and G. Deptuch, "Measurements of matching and noise performance of a prototype readout chip in 40 nm CMOS process for hybrid pixel detectors," *IEEE Transactions on Nuclear Science*, vol. 62, no. 1, pp. 359–367, Feb. 2015.

[26] A. Camlica, "Device architectures for improved temporal response with amorphous selenium radiation detectors," Ph.D. dissertation, University of Waterloo, 2019.

[27] X. Liu, F. Grönberg, M. Sjölin, S. Karlsson, and M. Danielsson, "Count rate performance of a silicon-strip detector for photon-counting spectral CT," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 827, pp. 102–106, Aug. 2016.

[28] S. H. Lee and R. P. Gardner, "A new G–M counter dead time model," *Applied Radiation and Isotopes*, vol. 53, no. 4-5, pp. 731–737, Nov. 2000.

[29] M. Jurdit, A. Brambilla, V. Moulin, P. Ouvrier-Buffet, P. Radisson, and L. Verger, "Characterization of spectrometric photon-counting X-ray detectors at different pitches," *Journal of Instrumentation*, vol. 12, no. 09, pp. T09 008–T09 008, Sep. 2017.

[30] E. Fredenberg, M. Lundqvist, M. Åslund, M. Hemmendorff, B. Cederström, and M. Danielsson, "A photon-counting detector for dual-energy breast tomosynthesis," in *SPIE Medical Imaging*, E. Samei and J. Hsieh, Eds., Lake Buena Vista, FL, Feb. 2009, p. 72581J.

[31] E. Downie, X. Yang, and H. Peng, "Investigation of analog charge multiplexing schemes for SiPM based PET block detectors," *Physics in Medicine and Biology*, vol. 58, no. 11, pp. 3943–3964, Jun. 2013.

[32] H.-J. Choe, Y. Choi, W. Hu, J. Yan, and J. Ho Jung, "Development of capacitive multiplexing circuit for SiPM-based time-of-flight (TOF) PET detector," *Physics in Medicine and Biology*, vol. 62, no. 7, pp. N120–N133, Apr. 2017.

[33] P. D. Olcott, G. Glover, and C. S. Levin, "Cross-strip multiplexed electro-optical coupled scintillation detector for integrated PET MRI," *IEEE Transactions on Nuclear Science*, vol. 60, no. 5, pp. 3198–3204, Oct. 2013.

[34] H. Ouh and M. L. Johnston, "Code-division multiplex encoding analog front end for current-mode sensor arrays," *IEEE Solid-State Circuits Letters*, vol. 1, no. 5, pp. 118–121, May 2018.

[35] K. Hu, E. Kennedy, and J. K. Rosenstein, "High frequency dielectric spectroscopy array with code division multiplexing for biological imaging," in *2019 IEEE Biomedical Circuits and Systems Conference (BioCAS)*. Nara, Japan: IEEE, Oct. 2019, pp. 1–4.

[36] S. W. Belling, L. Fabris, J. Mattingly, M. Mishra, J. Newby, and P. Barbeau, "A frequency domain multiplexing technique for multi-channel detector instrumentation," in *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC)*. Sydney, NSW, Australia: IEEE, Nov. 2018, pp. 1–6.

[37] M. Mishra, J. Mattingly, J. Mueller, and R. Kolbas, "Frequency domain multiplexing of pulse mode radiation detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 902, pp. 117–122, Sep. 2018.

[38] J. Kim, C. V. Fengel, S. Yu, E. D. Minot, and M. L. Johnston, "Frequency-division multiplexing with graphene active electrodes for neurosensor applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 5, pp. 1735–1739, May 2021.

[39] J. Kim, H. Ouh, and M. L. Johnston, "Multi-channel biopotential acquisition system using frequency-division multiplexing with cable motion artifact suppression," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 6, pp. 1419–1429, 2021.

[40] ——, "A 43.8μW per channel biopotential readout system using frequency division multiplexing with cable motion artifact suppression," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, Boston, MA, USA, 2020, pp. 1–4.

[41] H. Huang and S. Abbaszadeh, "Recent developments of amorphous selenium-based x-ray detectors: A review," *IEEE Sensors Journal*, vol. 20, no. 4, pp. 1694–1704, Feb. 2020.

[42] S. Kasap, J. B. Frey, G. Belev, O. Tousignant, H. Mani, L. Laperriere, A. Reznik, and J. A. Rowlands, "Amorphous selenium and its alloys from early xeroradiography to high resolution X-ray image detectors and ultrasensitive imaging tubes: Amorphous se from early xeroradiography to high resolution X-ray image detectors," *Physica Status Solidi (B)*, vol. 246, no. 8, pp. 1794–1805, Aug. 2009.

[43] A. Camlica, M. Z. Kabir, J. Liang, P. M. Levine, D. L. Lee, and K. S. Karim, "Use of pulse-height spectroscopy to characterize the hole conduction mechanism of a polyimide blocking layer used in amorphous-selenium radiation detectors," *IEEE Transactions on Electron Devices*, vol. 67, no. 2, pp. 633–639, Feb. 2020.

[44] H. H. Barrett, J. D. Eskin, and H. B. Barber, "Charge transport in arrays of semiconductor gamma-ray detectors," *Physical Review Letters*, vol. 75, no. 1, pp. 156–159, Jul. 1995.

[45] A. H. Goldan, J. A. Rowlands, O. Tousignant, and K. S. Karim, "Unipolar time-differential charge sensing in non-dispersive amorphous solids," *Journal of Applied Physics*, vol. 113, no. 22, p. 224502, Jun. 2013.

[46] A. Camlica, D. Lee, H. Jang, M. Z. Kabir, and K. Karim, "Energy resolution of amorphous selenium detectors: conventional vs unipolar charge sensing," in *Medical Imaging 2022: Physics of Medical Imaging*, W. Zhao and L. Yu, Eds., vol. PC12031, International Society for Optics and Photonics. SPIE, 2022, p. PC120310G.

[47] R. Mohammadi, P. M. Levine, and K. S. Karim, "Experimental demonstration of the small pixel effect in an amorphous photoconductor using a monolithic spectral single photon counting capable cmos-integrated amorphous-selenium sensor," in *2022*

International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 467–470.

[48] A. El-Falou, "Hybrid amorphous selenium-cmos photon-counting X-ray imager," Master's thesis, University of Waterloo, 2018.

[49] A. El-Falou, A. Camlica, R. Mohammadi, P. M. Levine, and K. S. Karim, "A monolithic amorphous-selenium CMOS single-photon-counting X-ray detector," *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 1746–1752, Apr. 2021.

[50] M. Gustavsson, F. U. Amin, A. Bjorklid, A. Ehliar, C. Xu, and C. Svensson, "A high-rate energy-resolving photon-counting ASIC for spectral computed tomography," *IEEE Transactions on Nuclear Science*, vol. 59, no. 1, pp. 30–39, Feb. 2012.

[51] F. Krummenacher, "Pixel detectors with local intelligence: An IC designer point of view," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 305, no. 3, pp. 527–532, Aug. 1991.

[52] R. Szczygiel, "Krummenacher feedback analysis for high-count-rate semiconductor pixel detector readout," in *Proceedings of the 17th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2010*, Wroclaw, Poland, 2010, pp. 412–415.

[53] P. Kmon, G. Deptuch, F. Fahim, P. Grybos, P. Maj, R. Szczygiel, and T. Zimmerman, "Active feedback with leakage current compensation for charge sensitive amplifier used in hybrid pixel detector," *IEEE Transactions on Nuclear Science*, vol. 66, no. 3, pp. 664–673, Mar. 2019.

[54] P. Kmon, L. Kadlubowski, and P. Kaczmarczyk, "Design of analog pixels front-end active feedback," *Journal of Instrumentation*, vol. 13, no. 01, pp. P01 018–P01 018, Jan. 2018.

[55] G. Wegrzyn, R. Kleczek, and P. Kmon, "Active feedbacks comparative analysis for charge sensitive amplifiers designed in CMOS 40 nm," in *2020 27th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*. Lodz, Poland: IEEE, Jun. 2020, pp. 78–82.

[56] D. Djekic, G. Fantner, J. Behrends, K. Lips, M. Ortmanns, and J. Anders, "A transimpedance amplifier using a widely tunable PVT-independent pseudo-resistor for high-performance current sensing applications," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*. Leuven: IEEE, Sep. 2017, pp. 79–82.

[57] A. Tajalli, Y. Leblebici, and E. Brauer, "Implementing ultra-high-value floating tunable CMOS resistors," *Electronics Letters*, vol. 44, no. 5, p. 349, 2008.

[58] A. M. Abo, "Design for reliability of low-voltage, switched-capacity circuits," Ph.D. dissertation, EECS Department, University of California, Berkeley, 1999.

[59] T. C. Carusone, D. Johns, K. W. Martin, and D. Johns, *Analog Integrated Circuit Design*, 2nd ed. Hoboken, New Jersey, USA: J. Wiley and Sons, 2012.

[60] V. Saxena, "Indirect feedback compensation techniques for multistage operational amplifiers," Ph.D. dissertation, Boise State University, Oct. 2007.

[61] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, 3rd ed. Hoboken, New Jersey, USA: John Wiley & Sons, 2010.

[62] S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 2, pp. 343–352, Feb. 2014.

[63] M. Alioto and G. Palumbo, "Analysis and comparison on full adder block in submicron technology," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 6, pp. 806–823, Dec. 2002.

[64] B. Murmann. ADC performance survey 1997-2021. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

APPENDICES

Appendix A

ROIC Pinout

Table A.1 lists our ROIC pins with their functions and nominal values. In Figure A.1, pin locations are shown.

Pin Name	Description	I/O/Power/GND	Analog/Digital	Nominal Value
dvdd0	Supply rail	Power	Digital	1.8 V
dvdd1	Supply rail	Power	Digital	1.8 V
dvdd2	Supply rail	Power	Digital	1.8 V
dvdd3	Supply rail	Power	Digital	1.8 V
dvss0	Supply rail	GND	Digital	0 V
dvss1	Supply rail	GND	Digital	0 V
dvss2	Supply rail	GND	Digital	0 V
dvss3	Supply rail	GND	Digital	0 V
vdd0	Supply rail	Power	Analog	1.8 V
vdd1	Supply rail	Power	Analog	1.8 V
vss0	Supply rail	GND	Analog	0 V
vss1	Supply rail	GND	Analog	0 V
avdd0	Supply rail	Power	Analog	1.8 V
avdd1	Supply rail	Power	Analog	1.8 V
avdd2	Supply rail	Power	Analog	1.8 V
avdd3	Supply rail	Power	Analog	1.8 V

avdd4	Supply rail	Power	Analog	1.8 V
avdd5	Supply rail	Power	Analog	1.8 V
avdd6	Supply rail	Power	Analog	1.8 V
avss0	Supply rail	GND	Analog	0 V
avss1	Supply rail	GND	Analog	0 V
avss2	Supply rail	GND	Analog	0 V
avss3	Supply rail	GND	Analog	0 V
avss4	Supply rail	GND	Analog	0 V
avss5	Supply rail	GND	Analog	0 V
avss6	Supply rail	GND	Analog	0 V
tvdd0	Supply rail	Power	Analog	1.8 V
tvdd1	Supply rail	Power	Analog	1.8 V
tvdd2	Supply rail	Power	Analog	1.8 V
tvdd3	Supply rail	Power	Analog	1.8 V
tvss0	Supply rail	GND	Analog	0 V
tvss1	Supply rail	GND	Analog	0 V
tvss2	Supply rail	GND	Analog	0 V
tvss3	Supply rail	GND	Analog	0 V
pvdd0	Supply rail	Power	Analog	1.8 V
pvdd1	Supply rail	Power	Analog	1.8 V
pvdd2	Supply rail	Power	Analog	1.8 V
pvdd3	Supply rail	Power	Analog	1.8 V
pvss0	Supply rail	GND	Analog	0 V
pvss1	Supply rail	GND	Analog	0 V
pvss2	Supply rail	GND	Analog	0 V
pvss3	Supply rail	GND	Analog	0 V
ovdd	Supply rail	Power	Analog	1.8 V
ovss	Supply rail	GND	Analog	0 V
ext0	External sensor input	I	Analog	-
ext1	External sensor input	I	Analog	-
ext2	External sensor input	I	Analog	-
ext3	External sensor input	I	Analog	-
ext4	External sensor input	I	Analog	-

ext5	External sensor input	I	Analog	-
ext6	External sensor input	I	Analog	-
ext7	External sensor input	I	Analog	-
out0	ADC output	O	Digital	0 - 1.8 V
out1	ADC output	O	Digital	0 - 1.8 V
out2	ADC output	O	Digital	0 - 1.8 V
out3	ADC output	O	Digital	0 - 1.8 V
out4	ADC output	O	Digital	0 - 1.8 V
out5	ADC output	O	Digital	0 - 1.8 V
out6	ADC output	O	Digital	0 - 1.8 V
out7	ADC output	O	Digital	0 - 1.8 V
rn	ADC reset	I	Digital	0 - 1.8 V
clk	ADC clock input	I	Digital	0 - 1.8 V
iota	ADC OTA bias current	I	Analog	400 μA
vcm	Reference voltage input	I	Analog	1.1 V
vrefp	Reference voltage input	I	Analog	1.25 V
vrefn	Reference voltage input	I	Analog	0.95 V
itele	CSA opamp bias current	I	Analog	2.2 μA
itune	CSA feedback bias current	I	Analog	6 μA
icol	Pixel Gm bias current	I	Analog	6 μA
idrive	I2V bias current	I	Analog	25 μA
ilpf0	LPF bias current	I	Analog	2.5 μA
ilpf1	LPF bias current	I	Analog	5.5 μA
ilpf2	LPF bias current	I	Analog	7.5 μA
ilpf3	LPF bias current	I	Analog	11 μA
ilpf4	LPF bias current	I	Analog	15 μA
ilpf5	LPF bias current	I	Analog	20 μA
ilpf6	LPF bias current	I	Analog	26 μA
ilpf7	LPF bias current	I	Analog	36 μA
lo0	LO input	I	Analog	0 - 1.8 V
lo1	LO input	I	Analog	0 - 1.8 V
lo2	LO input	I	Analog	0 - 1.8 V
lo3	LO input	I	Analog	0 - 1.8 V

lo4	LO input	I	Analog	0 - 1.8 V
lo5	LO input	I	Analog	0 - 1.8 V
lo6	LO input	I	Analog	0 - 1.8 V
lo7	LO input	I	Analog	0 - 1.8 V
csain	Test CSA input	I	Analog	-
csaout	Test CSA output	O	Analog	-
coloutp	Test bank output	O	Analog	-
coloutn	Test bank output	O	Analog	-
pipeinp	ADC input	I	Analog	-
pipeinn	ADC input	I	Analog	-
scanclk	Scan chain clock	I	Digital	0 - 1.8 V
scanrst	Scan chain reset	I	Digital	0 - 1.8 V
scanin	Scan chain input	I	Digital	0 - 1.8 V
scanout	Scan chain output	O	Digital	0 - 1.8 V

Table A.1: Pin list.

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16			
		lo0	lo1	lo2	lo3	lo4	lo5	lo6	lo7	dvss	dvdd	dvss	dvdd	scanin	scanout	scanrst	scanclk			
1	itele																	vdd		
2	itune																	vss		
3	icol																	pvdd		
4	idrive																	pvss		
5	ilpf0																	pvdd		
6	ilpf1																	pvss		
7	ilpf2																	ext0		d power
8	ilpf3																	ext1		a power
9	ilpf4																	ext2		p power
10	ilpf5																	ext3		t power
11	ilpf6																	ext4		o power
12	ilpf7																	ext5		
13	vdd																	ext6		
14	vss																	ext7		
15	pvdd																	csain		
16	pvss																	csaout		
17	pvdd																	coloutp		
18	pvss																	coloutn		
19	avdd																	pipeinp		
20	avss																	pipeinn		
21	avdd																	tvdd		
22	avss																	tvss		
23	avdd																	tvdd		
24	avss																	tvss		
25	avdd																	iota		
26	avss																	vcm		
27	avdd																	vrefp		
28	avss																	vrefn		
29	avdd																	tvdd		
30	avss																	tvss		
31	avdd																	tvdd		
32	avss																	tvss		
		ovdd	ovss	out0	out1	out2	out3	out4	out5	out6	out7	rn	clk	dvdd	dvss	dvdd	dvss			

Figure A.1: Pin locations.

Appendix B

Bonding Diagram

Figure B.1 shows the bonding diagram for our ROIC, which is packaged in a 120-pin Spectrum Semiconductor Materials CQZ12003 QFP. The cavity size of this package is $8.128 \times 8.128\,\mathrm{mm}^2$.

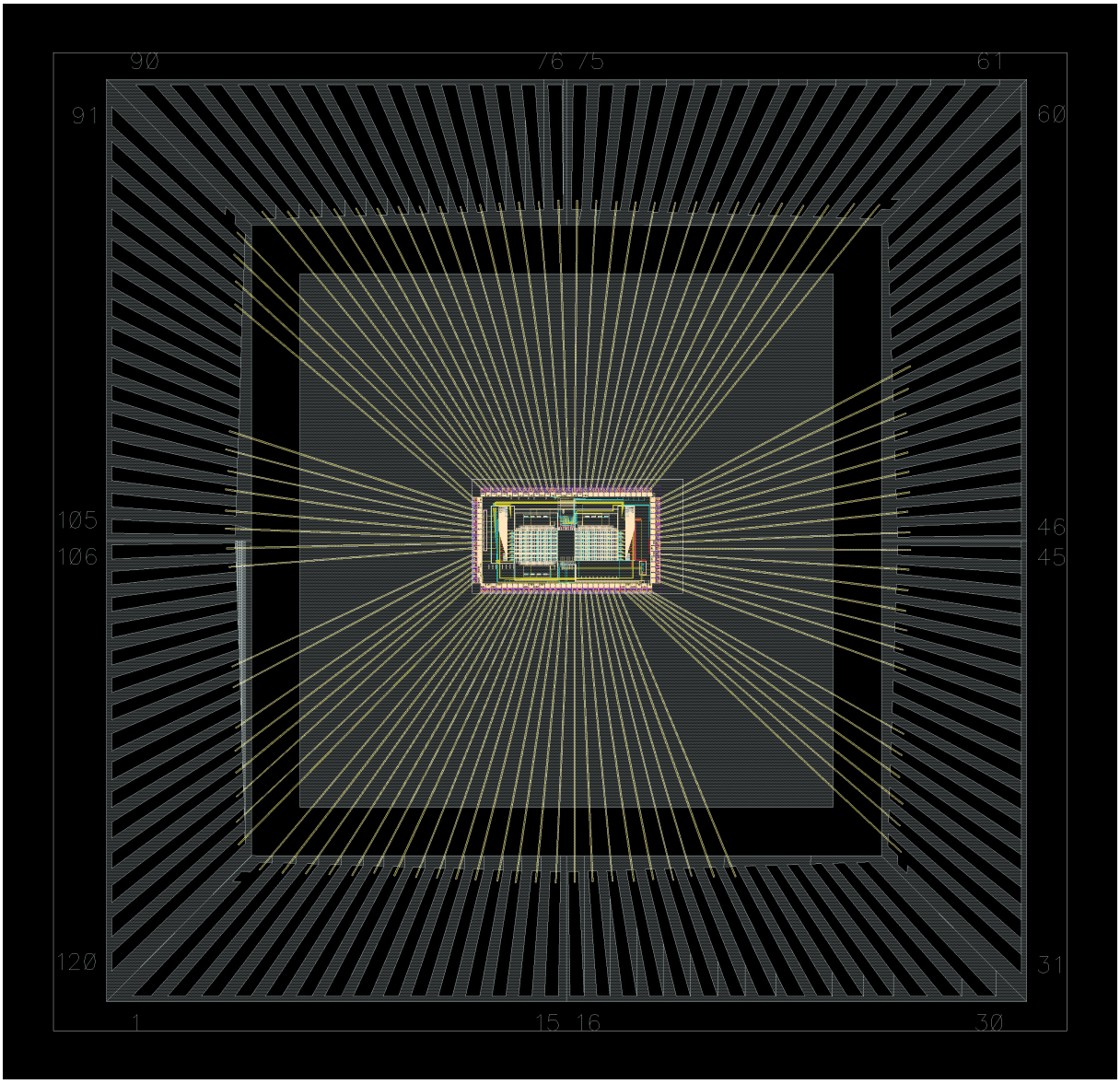


Figure B.1: Bonding diagram.

Appendix C

Scan Chain Control Bit Map

Table C.1 shows the scan chain bit map. The MSB is B9, which is sent first when loading the scan chain.

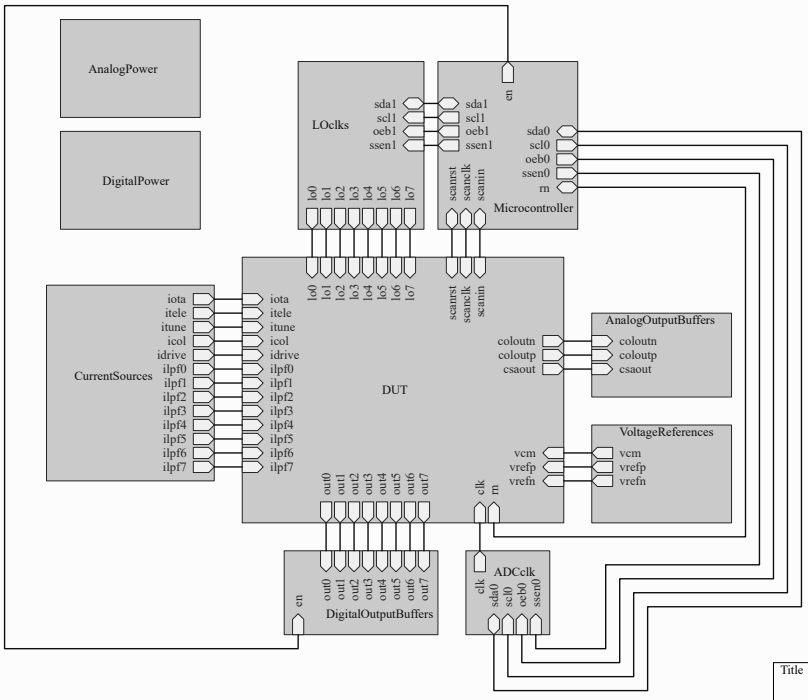
Control Bit	Name	Function
B9	adc in	Connect external ADC input pins to ADC
B8	col - adc	Connect column output to ADC
B7	col out	Enable column output buffer
B6	csa select 2	Select which pixel the CSA input and output are connected to
B5	csa select 1	Select which pixel the CSA input and output are connected to
B4	csa select 0	Select which pixel the CSA input and output are connected to
B3	output select 3	Select which ADC is connected to the output bus
B2	output select 2	Select which ADC is connected to the output bus
B1	output select 1	Select which ADC is connected to the output bus
B0	output select 0	Select which ADC is connected to the output bus

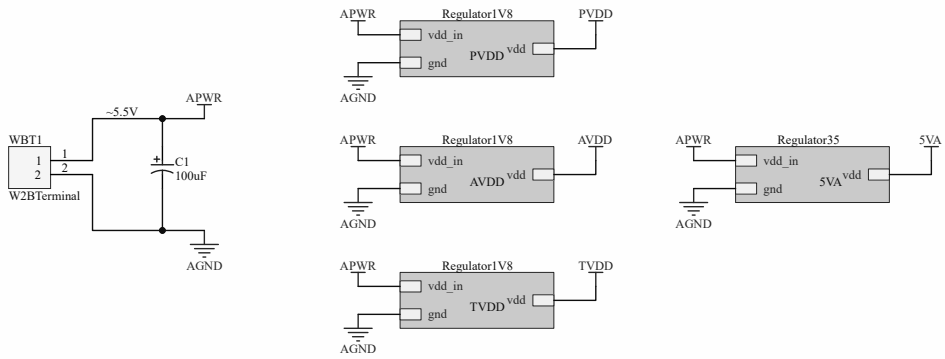
Table C.1: Control bit map for the scan chain.

Appendix D

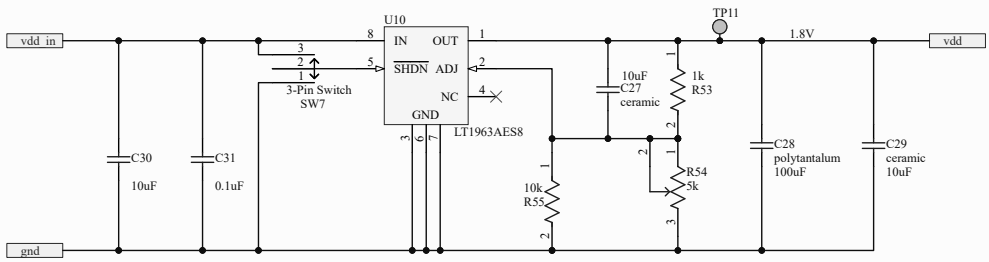
PCB Schematics

Schematics for the PCB are shown below, along with the layouts for each of the four PCB metal layers.

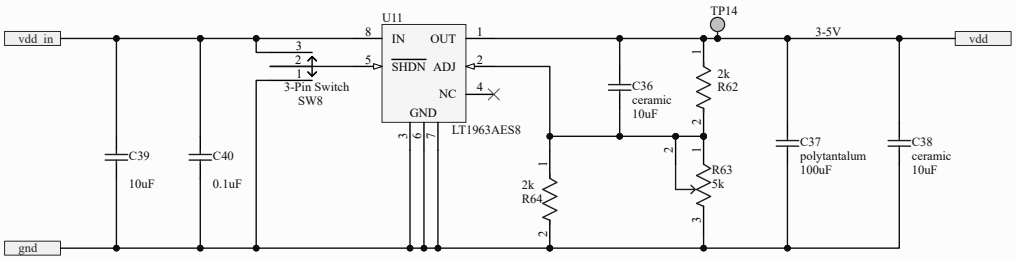

AnalogPower
DigitalPower
LOclks
sda1
scl1
oeb1
ssen1
lo0
lo1
lo2
lo3
lo4
lo5
lo6
lo7
en
sda1
scl1
oeb1
ssen1
sda0
scl0
oeb0
ssen0
rn
scanrst
scanclk
scanin
Microcontroller
CurrentSources
iota
itele
itune
icol
idrive
ilpf0
ilpf1
ilpf2
ilpf3
ilpf4
ilpf5
ilpf6
ilpf7
DUT
coloutn
coloutp
csaout
AnalogOutputBuffers
vcm
vrefp
vrefn
VoltageReferences
out0
out1
out2
out3
out4
out5
out6
out7
clk
rn
DigitalOutputBuffers
ADCclk
Title
Size
A4
Number
Revision
Date:
8-21-2023
Sheet of
File:
C:\Users\..\Top.SchDoc
Drawn By:



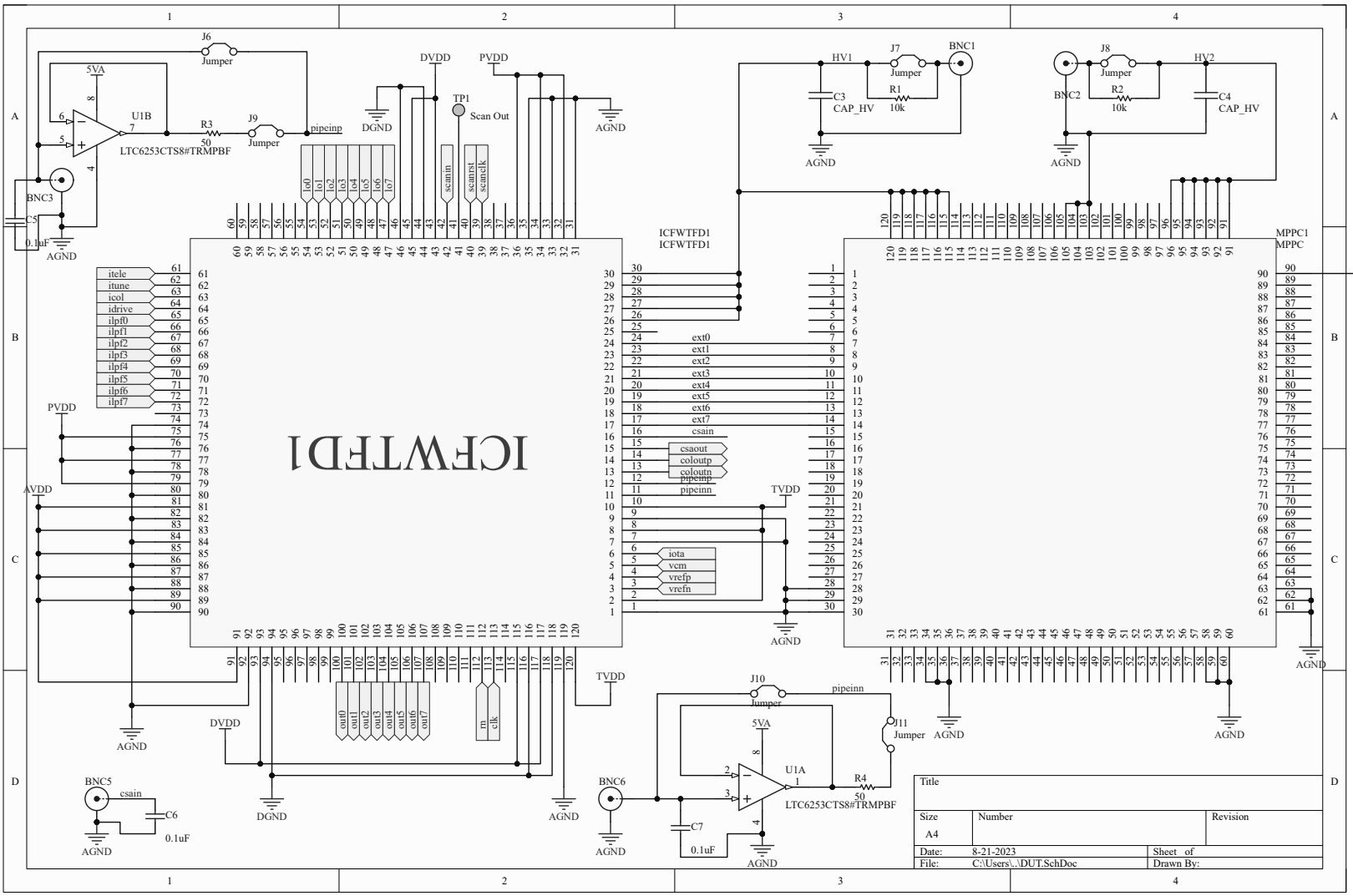
Title	ANALOG POWER		
Size A4	Number		Revision
Date:	8-21-2023	Sheet of	
File:	C:\Users\..\AnalogPower.SchDoc	Drawn By:	

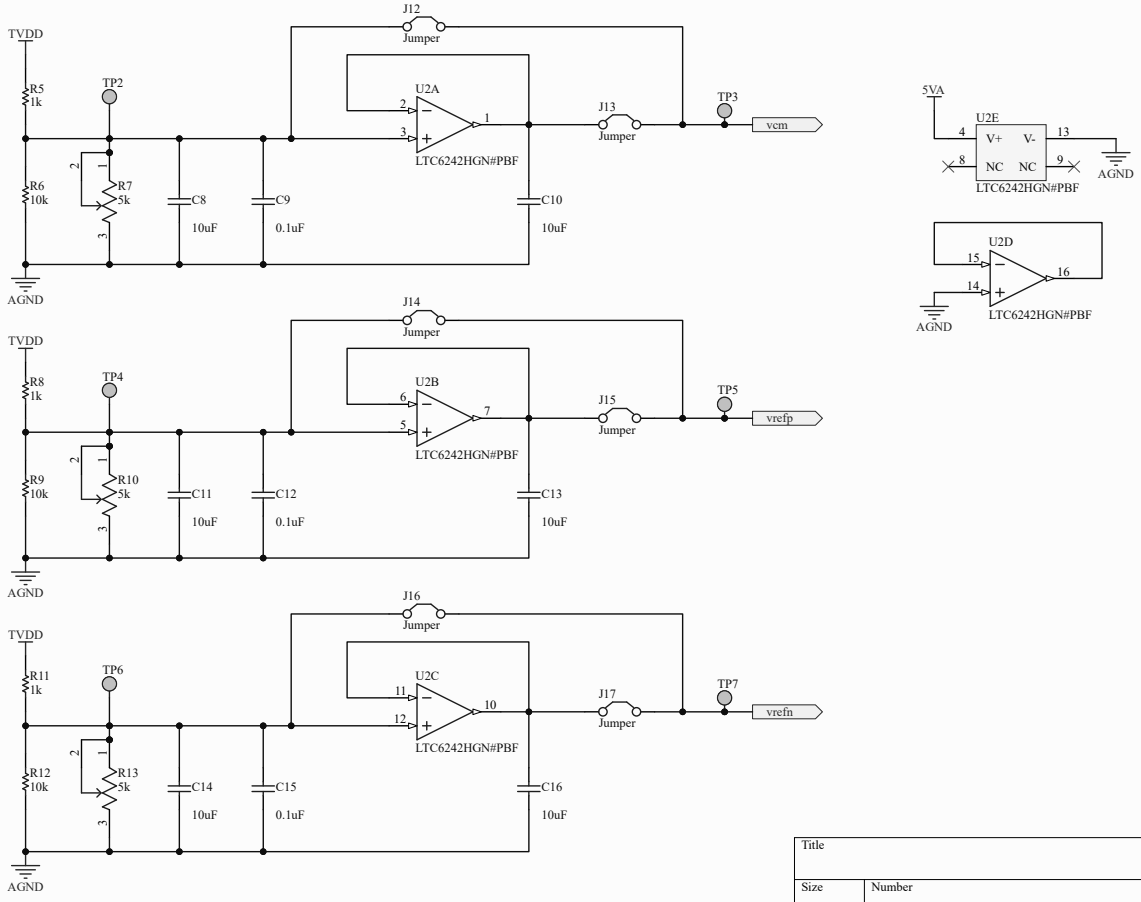


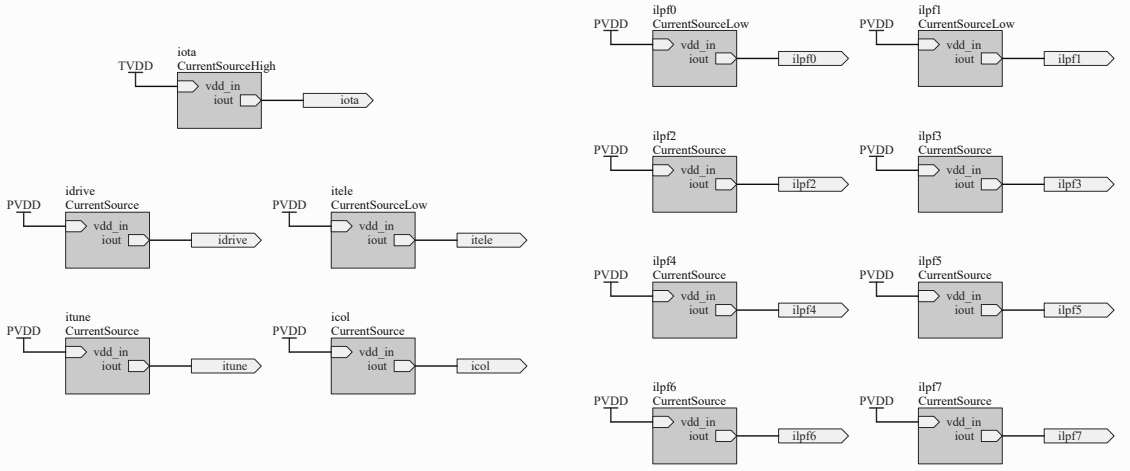
Title			
Size: A4	Number:		Revision:
Date: 8-21-2023		Sheet of	
File: C:\Users\..\Regulator1V8.SchDoc		Drawn By:	



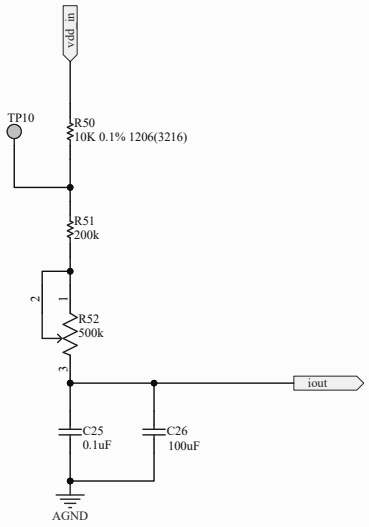
Title			
Size A4	Number		Revision
Date:	8-21-2023	Sheet of	
File:	C:\Users\..\Regulator35.SchDoc	Drawn By:	


J6
Jumper
5VA
U1B
LTC6253CTS8#TRMPBF
R3
50
J9
Jumper
pipeinp
DGND
DVDD
PVDD
TP1
Scan Out
AGND
BNC3
C5
0.1uF
HV1
J7
Jumper
BNC1
C3
CAP_HV
R1
10k
J8
Jumper
HV2
BNC2
R2
10k
C4
CAP_HV
ICFWTFD1
MPPC1
MPPC
itele
itune
icol
idrive
ilpf0
ilpf1
ilpf2
ilpf3
ilpf4
ilpf5
ilpf6
ilpf7
ext0
ext1
ext2
ext3
ext4
ext5
ext6
ext7
csain
csaout
coloutp
coloutn
pipeinp
pipeinn
iota
vcm
vrefp
vrefn
AVDD
TVDD
out0
out1
out2
out3
out4
out5
out6
out7
rn
clk
J10
Jumper
J11
Jumper
BNC5
csain
C6
0.1uF
BNC6
C7
0.1uF
R4
50
Title
Size
A4
Number
Revision
Date:
8-21-2023
Sheet of
File:
C:\Users\..\DUT.SchDoc
Drawn By:

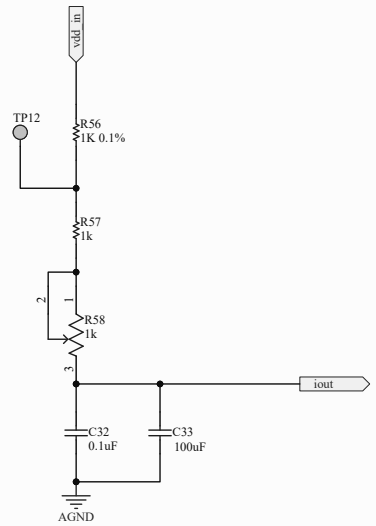

J12
Jumper
TVDD
R5
1k
TP2
U2A
2
3
1
J13
Jumper
TP3
vcm
LTC6242HGN#PBF
R6
10k
R7
5k
C8
10uF
C9
0.1uF
C10
10uF
AGND
J14
Jumper
TVDD
R8
1k
TP4
U2B
6
5
7
J15
Jumper
TP5
vrefp
LTC6242HGN#PBF
R9
10k
R10
5k
C11
10uF
C12
0.1uF
C13
10uF
AGND
J16
Jumper
TVDD
R11
1k
TP6
U2C
11
12
10
J17
Jumper
TP7
vrefn
LTC6242HGN#PBF
R12
10k
R13
5k
C14
10uF
C15
0.1uF
C16
10uF
AGND
5VA
U2E
4
V+
V-
13
8
NC
NC
9
LTC6242HGN#PBF
AGND
U2D
15
16
14
LTC6242HGN#PBF
AGND
Title
Size
A4
Number
Revision
Date: 8-21-2023
Sheet of
File: C:\Users\..\VoltageReferences.SchDoc
Drawn By:



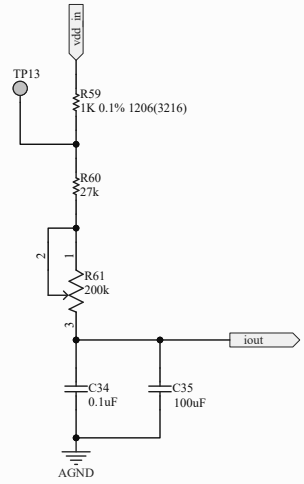
Title		
Size A4	Number	Revision
Date: 8-21-2023		Sheet of
File: C:\Users\..\CurrentSources.SchDoc		Drawn By:



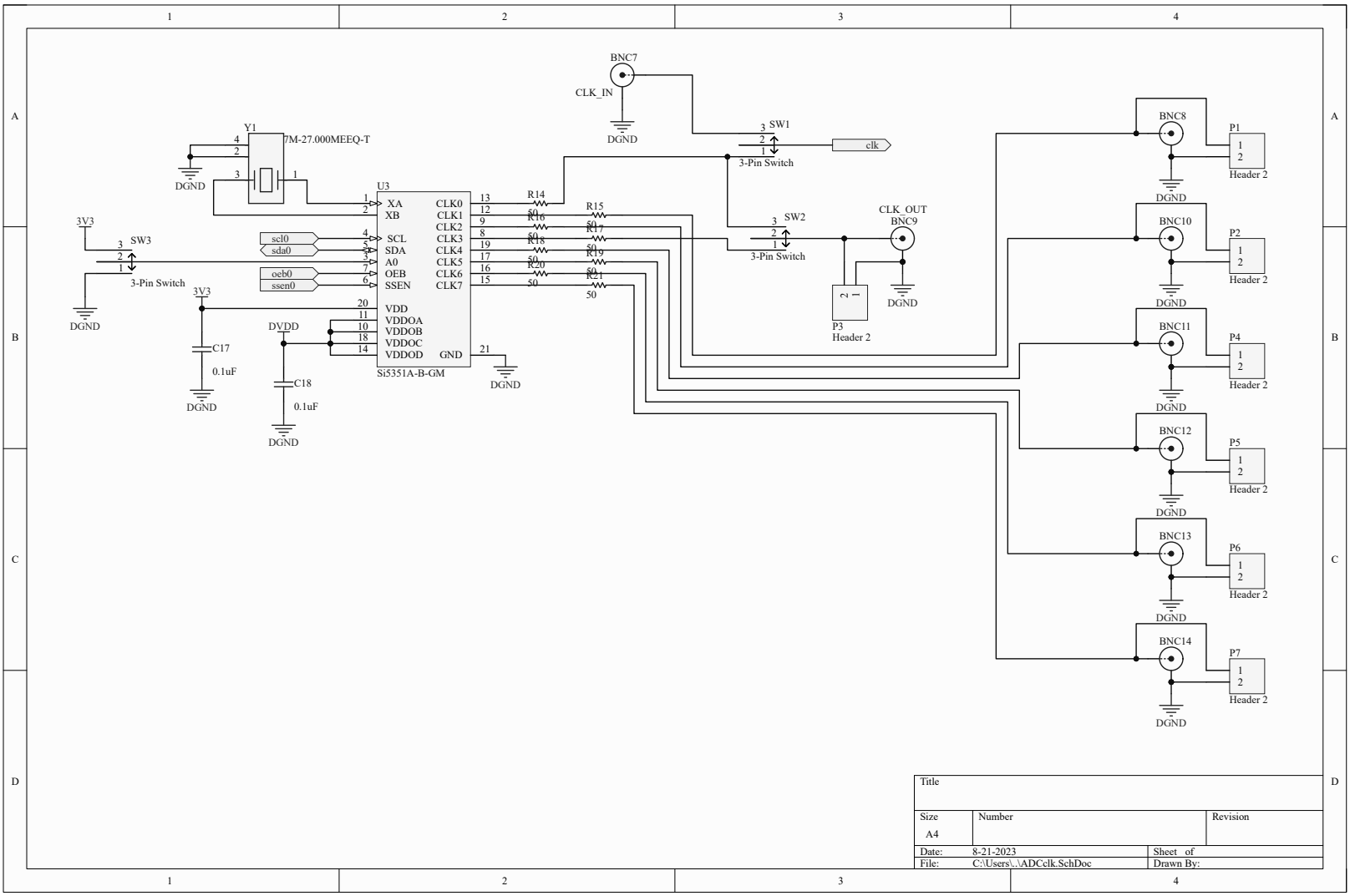
Title			
Size A4	Number		Revision
Date:	8-21-2023	Sheet of	
File:	C:\Users\..\CurrentSourceLow.SchDoc	Drawn By:	

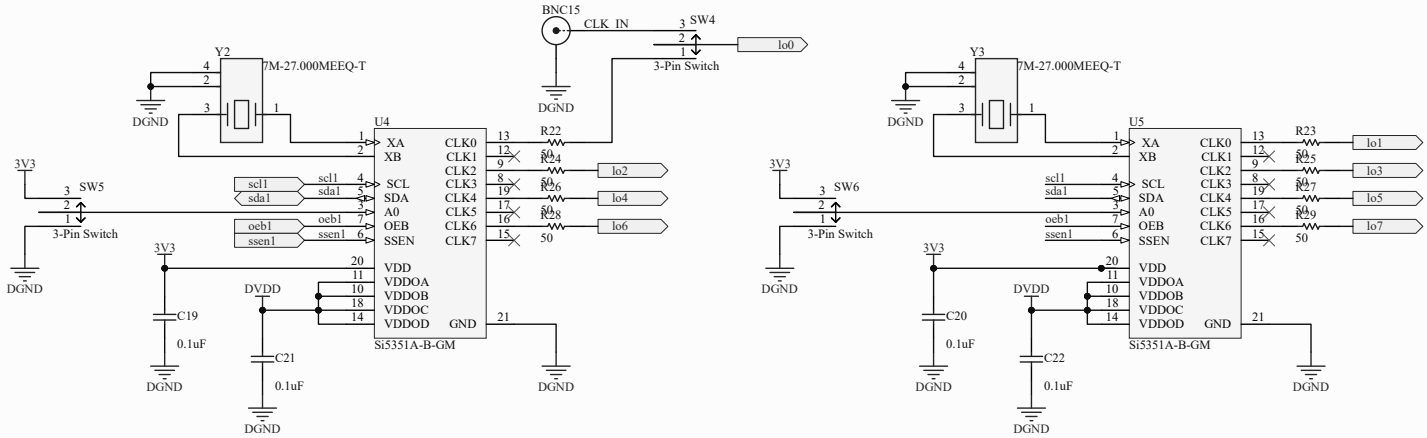


Title			
Size A4	Number		Revision
Date:	8-21-2023	Sheet of	
File:	C:\Users\..\CurrentSourceHigh.SchDoc	Drawn By:	

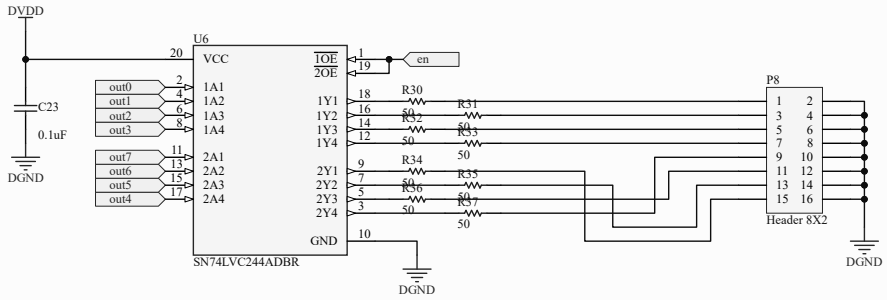


Title			
Size A4	Number		Revision
Date:	8-21-2023	Sheet of	
File:	C:\Users\..\CurrentSource.SchDoc	Drawn By:	

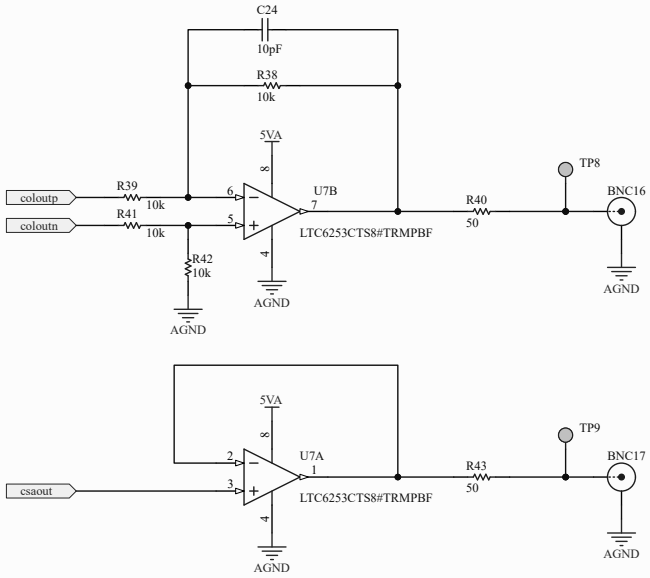

BNC7
CLK_IN
DGND
Y1
7M-27.000MEEQ-T
U3
XA
XB
SCL
SDA
A0
OEB
SSEN
CLK0
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
VDD
VDDOA
VDDOB
VDDOC
VDDOD
GND
Si5351A-B-GM
R14
R15
R16
R17
R18
R19
R20
R21
50
3V3
SW3
3-Pin Switch
scl0
sda0
oeb0
ssen0
C17
0.1uF
DVDD
C18
SW1
SW2
clk
CLK_OUT
BNC9
P3
Header 2
BNC8
BNC10
BNC11
BNC12
BNC13
BNC14
P1
P2
P4
P5
P6
P7
Title
Size
A4
Number
Revision
Date: 8-21-2023
File: C:\Users\..\ADCclk.SchDoc
Sheet of
Drawn By:



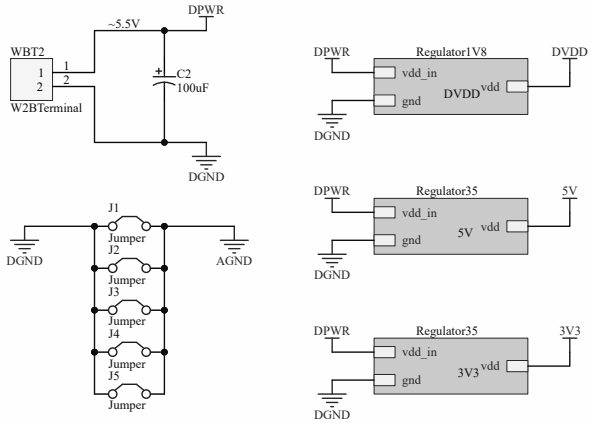
Title		
Size: A4	Number	Revision
Date: 8-21-2023		Sheet of
File: C:\Users\..\LOclks.SchDoc		Drawn By:

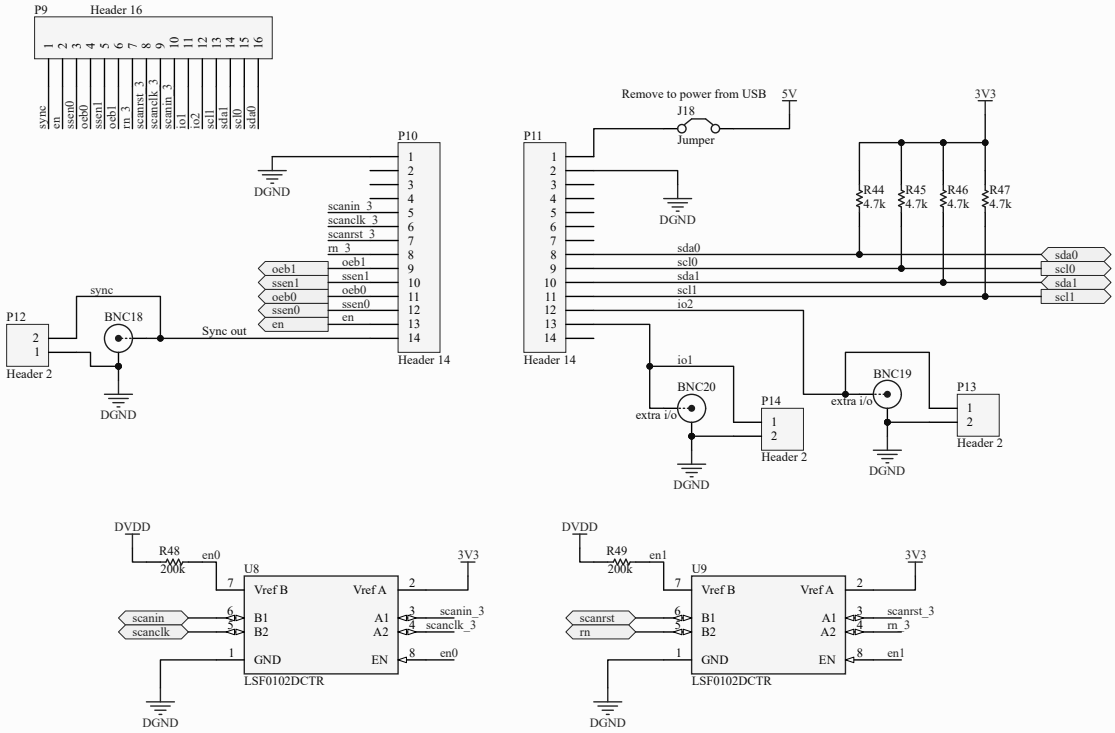


Title			
Size A4	Number		Revision
Date:	8-21-2023	Sheet of	
File:	C:\Users\..\DigitalOutputBuffers.SchDoc	Drawn By:	



Title			
Size A4	Number		Revision
Date:	8-21-2023	Sheet of	
File:	C:\Users\..\AnalogOutputBuffers.SchDoc	Drawn By:	


DPWR
~5.5V
WBT2
1
2
1
2
W2BTerminal
C2
100uF
DGND
J1
Jumper
J2
Jumper
J3
Jumper
J4
Jumper
J5
Jumper
DGND
AGND
DPWR
Regulator1V8
vdd_in
gnd
DVDD
vdd
DVDD
DGND
DPWR
Regulator35
vdd_in
gnd
5V
vdd
5V
DGND
DPWR
Regulator35
vdd_in
gnd
3V3
vdd
3V3
DGND
DigitalPower
DIGITAL POWER
A4
Date: 8-21-2023
File: C:\Users\..\DigitalPower.SchDoc
Sheet of
Drawn By:



Title		
Size A4	Number	Revision
Date: 8-21-2023		Sheet of
File: C:\Users\..\Microcontroller.SchDoc		Drawn By:

