

Low Power TFT Logic Implementation on Display Backplane, Using Unipolar TFTs

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

Abstract

Active-Matrix (AM) displays are key components in devices such as computer monitors, smartphones, laptops, portable gaming consoles, and wearable devices. These displays are trending towards becoming the primary display technology in today's market. The demand for current displays has surpassed 4K (4096 rows by 2160 columns) and have even reached 8K Ultra-High-Definition (UHD, 7680 rows by 4320 columns). The display panel is generally fabricated on low-cost thin-film transistors (TFT), while the driver and control circuits are built using conventional Complementary-Metal-Oxide-Semiconductor (CMOS) circuits. A bonding pad serves as interface between CMOS circuits and TFT display panel. For each row and column of pixels added to the display backplane, an additional bonding pad needs to be added to properly interface the off-panel peripheral row and column control circuit with TFT and OLED pixel array. As the pixel density of the display increases, the bonding pad pitch must decrease, to accommodate. However, the pitch can only reduce finitely, and this imposes a bottleneck on achieving high-density large-scale displays. Additionally, with each row-line connected to a gate of thousands of pixels, there is a high capacitive load, which contributes to a high dynamic power consumption. Recent research has been investigating the use of TFTs to change the off-panel integrated-circuit (IC) and integrate it onto the display backplane, eliminating the need for bonding pads, while also reducing the overall power consumption. Amorphous silicon (a-Si:H) TFTs have good uniformity and low mask count fabrication process, making it suitable for large-scale displays, in comparison to Low-Temperature-Polysilicon (LTPS) TFTs. However, a-Si:H TFTs are naturally unipolar, which make it hard to replicate the CMOS like logic that the off-panel ICs have. This thesis aims at tackling the bottlenecks of large-scale displays, that is, the high dynamic power consumption, and the limited space from the bonding pads. The proposed row driver circuit presented in this thesis can be used to eliminate the off-panel row IC, and be integrated into the display backplane, while reducing the dynamic power consumption, with a-Si:H TFT technology.

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Dedication

To my family, friends, and my girlfriend.

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List of Abbreviations

a-Si:H: Hydrogenated amorphous silicon
ACF: Anisotropic conductive film
AM: Active-matrix
AMLCD: Active-matrix liquid crystal display
AMOLED: Active-matrix organic light emitting diode
CMOS: Complementary metal-oxide semiconductor
CRT: Cathode ray tube
CS: Charge-sharing
DAC: Digital to analog converter
DOS: Density of states
FCB: Flip-chip bonding
IC: Integrated circuit
LCD: Liquid crystal display
LTPS: Low-temperature polysilicon
OLED: Organic light emitting diode
PDN: Pull-down network
PECVD: Plasma enhanced chemical vapour deposition
PM: Passive-matrix
PUN: Pull-up network
PWM: Pulse width modulation
QVGA: Quarter video graphics array
RIE : Reactive ion etching
TFT: Thin-film transistor
UHD: Ultra-high definition
VGA: Video graphics array

Chapter 1: Introduction

1.1 Overview on Display Technology Evolution and Market Trends

Whether it is viewing the news on the smartphone, using the car dashboard to navigate to work, or even sitting at home and watching a movie, the ease of access to news, entertainment and social interaction has been thanks to the evolution display technology. Display technology is a big part of day-to-day life and has been integrated in all parts of society. In 1897, W.K. Braun invented the Cathode Ray Tube (CRT). The image being displayed is based on an electron scanning method. Once the cathode is heated up from the filament, electrons are then fired through an electron gun. The trajectory of the electrons is accelerated and deflected by grid electrodes, and the variation in voltage changes the electron's placement on the screen. The entire screen is scanned from this process, and an image is formed for the viewer. Commercial CRTs were first brought into the international market later in the early 20th century. The first images were black and white, and had an exceptionally low brightness, around 10 cd/m². Since then, research has been implemented to not only raise the brightness, but also introduce colour onto the screen. The CRT display made a huge milestone in the mid-20th century, when RCA invented the shadow-mask, which allowed for the first red blue and green (RGB) display, bringing full colour displays to the market [1].

CRTs saw relevance in the market for about half a century. However, their bulkiness, low brightness and contrast led to research into a newer generation of displays. [2]. In aims of addressing these issues, the liquid crystal display (LCD) was introduced in the mid-to-late 20th century. This display technology is non-emissive, meaning that a backlight unit is required. In this technology, the backlight emits a light, which is then polarized and sent to the liquid crystals. The alignment and orientation of these crystals affect the amount of light that passes through, which is then sent through another polarization filter. Following this, the light would go through an RGB colour filter, and the viewable image is now present on the screen [1], [3], [4]. Later in the late 20th century, LeComber et. al developed the amorphous silicon thin-film transistor (a-Si:H TFT) [5], [6]. Its high on/off ratio, as well as its low mask requirement for fabrication helped innovate active-matrix LCDs (AMLCDs). In this technology, these TFTs write the data which is stored into a capacitor containing the liquid crystal. This helped maintain the image quality, and helped innovate products such as the 10.4-inch a-Si:H TFT based TFT LCD notebook PC [1], [2], [7].

While the LCD helped spark the innovation for other display products, the main drawback was the power consumption and the thickness of the display, due to the backlight. Moreover, the difficulty in achieving small-scale displays for smartphones with high resolution and form factor from LCDs led to the innovation of organic-light-emitting-diode (OLED) based displays. OLEDs have gained a lot of recent research interest, due to their dark state, freeform factor, lightweight, and being self-emissive [1], [2], [3], [8]. This technology has helped innovate devices such as high-resolution smartphones, high dynamic range televisions, foldable devices and vibrant, high-contrast portable gaming consoles. OLED displays being self-emissive mean that there is no need for a backlight to constantly be on, saving significant power over the LCD. Instead, current-driver electronics are needed, to send data and timing to the TFT + capacitor pixels, turning them on when necessary. OLED-based displays have made noteworthy progress in the market, being a significant rival for the LCD. However, the low lifetime of OLEDs, their burn-in and low brightness ($<1000\text{cd/m}^2$) has sparked the research interest of micro-LEDs (μLEDs). This class of LED is a type III-V semiconductor material, typically Gallium Nitride (GaN), and are also self-emissive. μLED -based displays have gained popular research interest due to their longer lifetime, lower driving current required and higher brightness than OLEDs, making it more suitable for devices such as smartphones. However, this technology is still maturing and very costly, due to the expensive fabrication process, requiring significant research before it can be seen in the commercial market. [3], [9]. Despite the shortcomings of OLED technology, research is still committed to improving the lifetime, architecture and power consumption of these devices. OLED-based displays continue to remain as the most power efficient display, serving a wide variety of applications, as seen in Figure 1a). Pioneers, such as Apple and Samsung are continuing to release portable-OLED display devices at an exponential rate (see Figure 1b), such as the iPhone 15 Pro Max having an OLED display with 2796 by 1290 resolution, and a 2,000,000:1 contrast ratio. This has enabled displays for other technologies, such as the Internet-of-Things (IoT).

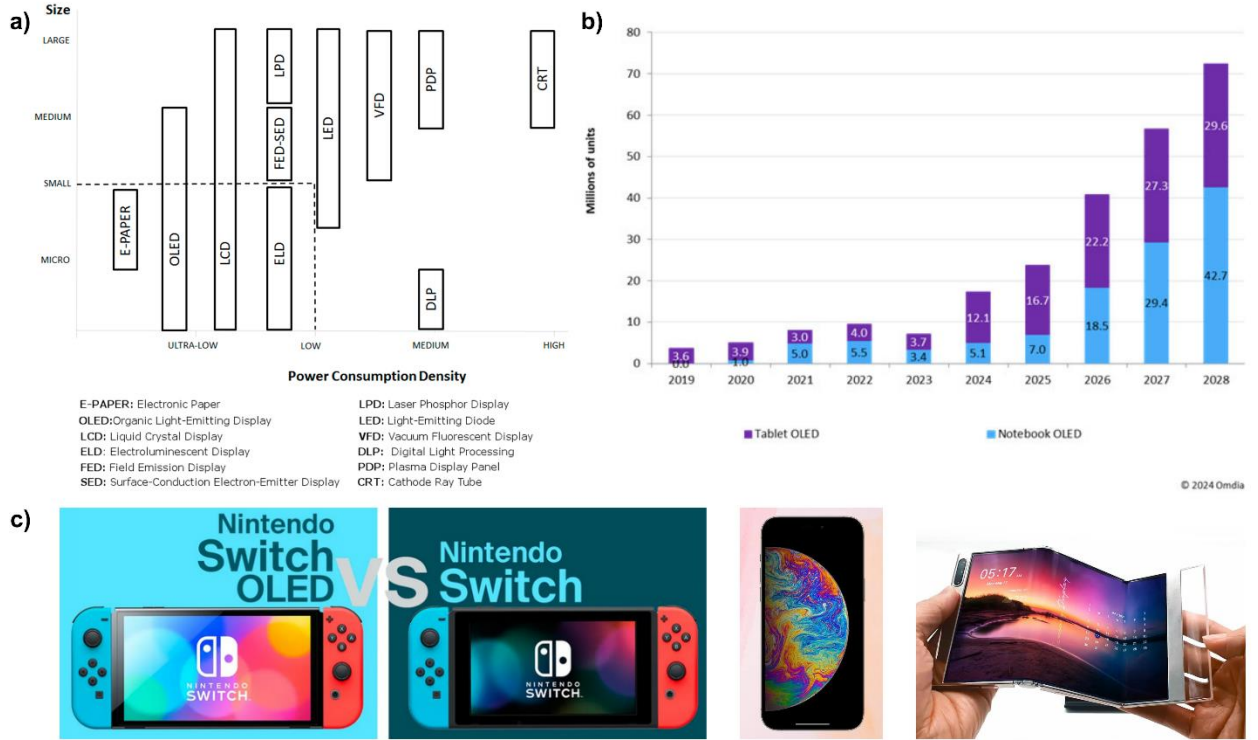


Figure 1.1: a) Size VS power consumption for different types of displays, [10], b) Shipment projection for portable OLED displays [11] and c) various OLED-based devices.

1.2 Components of the Display Panel

There are multiple components that make up the current display panel technology. These components are placed into two main groups, the bulk display panel itself, and the off-panel peripheral circuit. Figure 1.2 shows the general architecture of the display panel. The bulk consists of the display backplane, which has a pixel array of size $N \times M$ (N rows and M columns, respectively). This portion takes up most of the area of the display panel. Meanwhile, the off-panel peripheral circuit consists of multiple integrated circuits (ICs). See Fig. 1.2, IC#1 is responsible for generating and sending the data and timing to IC#2 and IC#3, which are the column and row ICs, respectively. The data sent into IC#2 is shifted and sent along the columns of the pixel array, while the data sent into IC#3 is sent along the rows of the pixel array. To properly interface the off-panel ICs with the pixel array, bonding pads are placed on the display backplane. Common methods for bonding include anisotropic conductive film (ACF) or flip-chip bonding (FCB) [12], [13], [14].

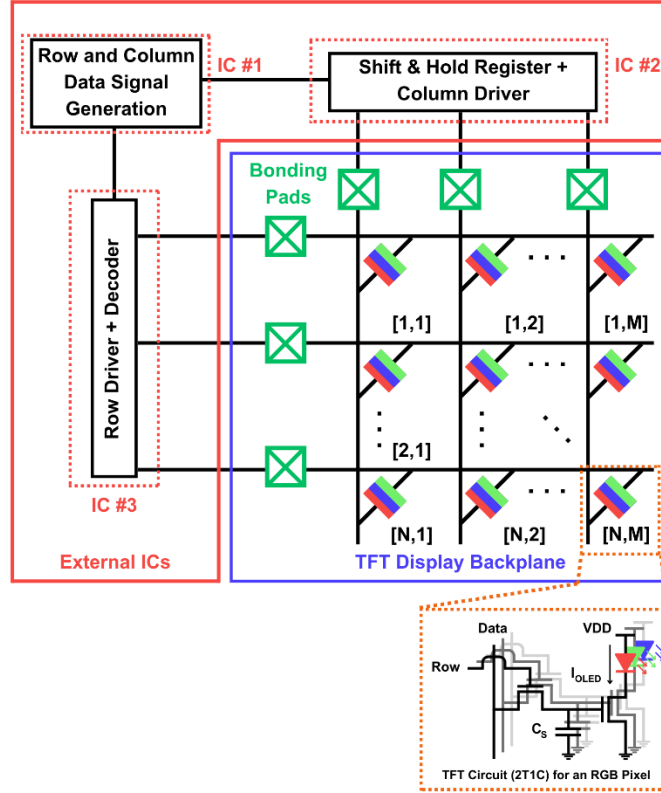


Figure 1.2: Conventional display panel architecture.

1.3 Research Motivation

With active-matrix organic light emitting diode (AMOLED) and AM μ LED displays becoming the driving force in the display market and an emerging research interest, respectively, the demand for these displays have reached resolutions surpassing even 4K. With the growing demand in resolution, so too has the pixel density in these display panels. While pixels have reached dimensions in the micron scale, the bonding pad pitch cannot reduce infinitely. Additionally, the increase in pixel density also contributes to an increase in higher capacitive loads, raising the dynamic power consumption significantly. There is a growing research interest to integrate the row and column driver component onto the TFT display backplane and replace the off-panel peripheral ICs. This will help reduce the fabrication masks, the cost and realize a fully integrable display using TFTs [15], [16], [17], [18]. Amorphous silicon (a-Si:H) TFTs have emerged as the primary technology for large-scale displays, owing to their low fabrication mask requirement, and great large-scale uniformity. However, a-Si:H TFTs are naturally n-type, due to their amorphous nature, and do not have a complementary transistor

type. This makes it difficult to achieve CMOS-like logic. This is further exemplified by their low mobility and electrical degradation over time.

This thesis proposes a solution to tackle the bottlenecks of large-scale displays, that is, the high dynamic power consumption, and creating a low-power row-driver circuit with CMOS-like logical functionality. The proposed row-driver circuit presented in this thesis implements additional logic to reduce the dynamic power consumption, using address row-decoders. These decoders can reduce the amount of row bonding pads to $3N/8$ decoder pads instead. This removes the need for IC#3 (see Figure 1.3) and can instead be integrated onto the TFT backplane. The schematic is shown in Figure 1.3.

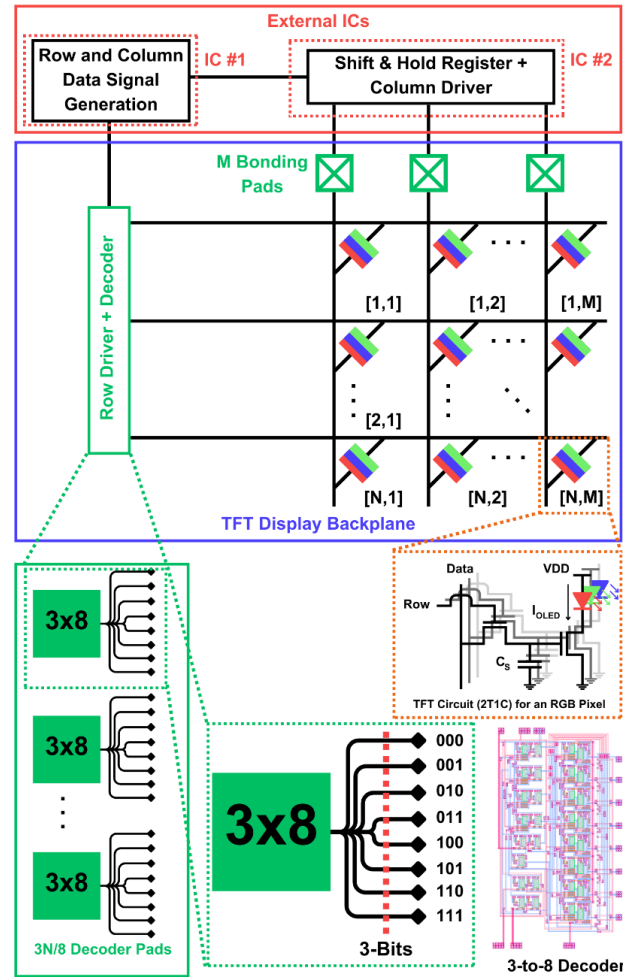


Figure 1.3: Proposed display panel architecture, with an integrated TFT row-driver circuit.

1.4 Thesis outline

This thesis is structured as follows:

Chapter 1 provides a history of the display technologies, the emergence in the market, and the current bottlenecks that modern-day display technology is facing. The research motivation, in aims of addressing these bottlenecks are also addressed.

Chapter 2 presents the relevant background information regarding display panel technology. Starting from the macro-scale with the display architecture, comparing the active and passive matrix, and the analog and digital driving, to the individual TFTs involved in the driving and pixel array. This chapter also introduces the TFT technology used in this research, and the key considerations when implementing it in unipolar TFT technology.

Chapter 3 presents background history of CMOS-like logic using unipolar a-Si:H TFTs. This chapter starts off, by looking at the conventional 2 transistor inverter, and investigates strategies implemented to optimize the output swing and reduce the static power dissipation. These techniques include adding additional stages and bootstrapping, eventually leading up to the state-of-the-art 5 transistor bootstrapped inverter, using a feedback capacitor.

Chapter 4 proposes low-power charge-sharing unipolar logic, building upon the state-of-the-art inverter. The proposed logic is then implemented in an address row-decoder. Measurement results are done and compared with the simulated to validate the realization of a row-driver circuit integrated onto a TFT display backplane.

Chapter 5 concludes this thesis and suggests steppingstones for future work and milestones.

Chapter 2: Background Information

This chapter will provide the necessary information to help understand the following sections of this thesis. The background information in this chapter will focus on the display panel and its components. It will start with the panel architecture and its circuitry, and go down to the individual devices, such as the pixels in the array.

2.1 Display Architectures

The area of a backplane display panel (see Figure 1.2, in the blue box) is primarily composed of the pixel array. There are two types of arrays, the passive-matrix and active-matrix.

2.1.1 Passive-Matrix Architecture

Figure 2.4 shows the passive-matrix backplane display architecture. In this architecture, the intersection of the row and column lines form the pixels. The cathode and anode of the RGB diodes are connected to the respective column and row lines, respectively. The driving mechanism of the passive-matrix is relatively simple, done by a matrix-addressing/multiplexing method [19]. The row-lines are scanned in a row-by-row manner. For a selected row-line, the row is driven by a row voltage, while the rest of the other rows are kept at ground. Meanwhile, while the selected row is active, the column driver sends the voltage data to the corresponding pixels. Once the data is sent through all the columns in that corresponding row, the row voltage is driven to ground, allowing for the next row to turn on. This happens sequentially, row-by-row, at a rate such that instead of the human eye detecting the image as a line, the eyes perceive the screen as a planar image [20]. This is typically done at a refresh rate of typically 60 *Hz*, so that this illusion is maintained, and the human eyes do not perceive a flickering image instead [20], [21].

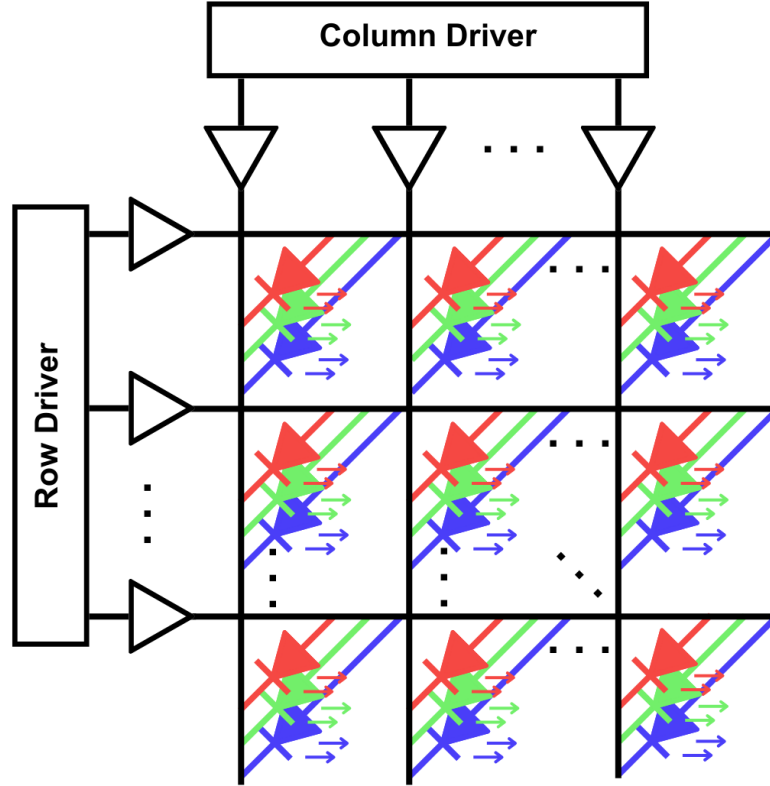


Figure 2.4: Passive-matrix display architecture.

This design is relatively simple, requiring only $N+M$ interconnections [22]. However, because only one row-line can be scanned at a time, this limits the resolution needed to maintain that visual image illusion. For each additional row added to an $N \times M$ display, the row scan time must reduce, to allow other row lines to be scanned and prevent that visual flickering. This typically limits the resolution of passive-matrix backplane displays to 320×240 , which is that of a QVGA. With this limitation, passive-matrix displays are typically used in small handheld IoT devices [20].

2.1.2 Active-Matrix Architecture

To address the primary concerns related to the passive-matrix architecture, the active-matrix architecture was developed, and the schematic is shown in Figure 2.5.

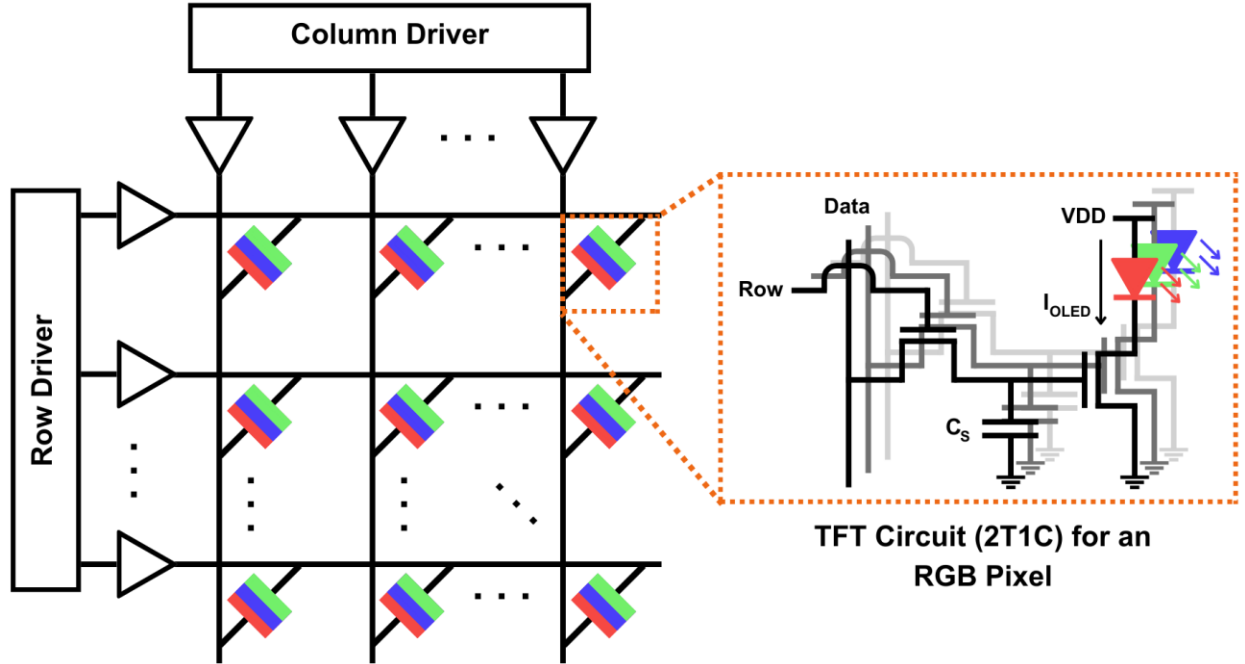


Figure 2.5: Active-matrix display architecture.

In comparison to the passive-matrix display architecture, there is additional complexity, with the incorporation of a TFT circuit. In the passive-matrix method, there is no way to store any data provided to the pixel [23], [24]. However, in the active-matrix method, there is now a circuit for each pixel, which allows for a more precise control of the data. The circuit is a TFT circuit with a storage capacitor, C_s [24]. Figure 2.5 shows the conventional 2T1C circuit for an individual pixel. With the additional complexity of the device layout, the signal generation and timing are more detailed as well. For the column signal generation, there are two main phases, programming and emitting. To program the pixels, the voltage generated by the signal generator will be stored in the pixel circuit, row-by-row, until the end of the panel is reached. Then, in the emitting phase, the LEDs will emit light. The intensity of the emitted LED depends on the amount of data stored in the pixel circuit [21], [25]. Not only does this circuit have more precise control of the sub red, blue and green pixels, but it also addresses the bottleneck with the passive-matrix method, allowing this display to be used in larger-scale displays such as laptops, televisions, etc. [4]. This research will focus with the active-matrix method in mind.

2.2 Driving Mechanisms of the Display Panel

This section will focus on the driving mechanisms to send the desired row and column timing to the pixel array. See Figure 1.2, this section pertains to the peripheral circuit. The row and column signals

are generated, which are then fed to a row and column driver. There are two types of driving mechanisms – analog and digital. In the analog driving scheme, a digital to analog converter (DAC) or an analog buffer array. In this driving scheme, the frame is timed (see Figure 2.6), such that in the programming phase (T_p), an n-bit sized data is fed into the data line by the DAC, and the rows are then scanned sequentially during the emission phase.

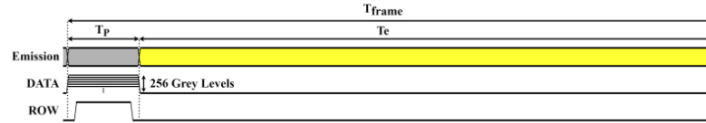


Figure 2.6: Frame timing diagram for an analog driving scheme [24].

Contrary, the digital driving method does not require a DAC or analog buffer array. This in turn reduces the area footprint, allowing for higher resolution and more cost efficiency. In digital driving, the timing is different, in which each frame is split into n-bit sized subframes (see Figure 2.7). The timing for digital driving follows a weighted or unweighted pulse-width-modulation method (PWM). In the unweighted PWM method, each subframe has an identical time frame, and the frame brightness is affected by the number of ON pulses in that frame period. In the weighted PWM method however, the pulse-width is modulated, based on the binary representation. While the weighted PWM method requires more complex circuitry, it is more power efficient compared to the unweighted PWM method [24].

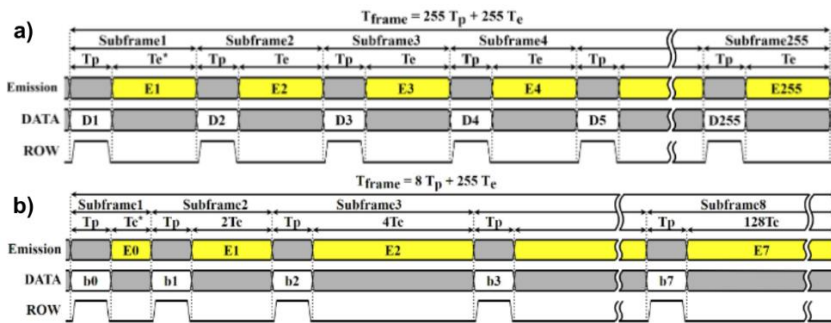


Figure 2.7: Frame timing diagram for a digital driving scheme for a) unweighted PWM and b) weighted PWM [24].

2.3 TFT Display Panel Technologies

In the market, there are two main TFT technologies incorporated for the backplane display, low-temperature-poly-silicon (LTPS) and hydrogenated amorphous silicon (a-Si:H) [21]. Table 2.1 provides a comparative analysis of these TFTs and their properties.

Table 2.1: Comparison between LTPS and a-Si:H TFT technology for display backplanes [26]

Property	LTPS	a-Si:H
Carrier mobility	100 cm ² / V s	1 cm ² / V s
Polarity	p-type and n-type	Only n-type
Spatial uniformity	poor	good
Leakage current	10 ⁻¹² A	10 ⁻¹³ A
Fabrication masks	7 (PMOS) to 9 (CMOS)	4-5
Fabrication process	Laser annealing and crystallization	Plasma Enhanced Chemical vapour deposition (PECVD)

The high mobility of LTPS arises from it having a long-range order of atomic structure. Additionally, it has a lower parasitic capacitance due to its self-aligned structure, which helps mitigate power consumption, and increase the operation speed. However, LTPS has a poor device uniformity and scalability due to the irregular grain boundaries on the polysilicon layer. This makes it difficult to incorporate LTPS TFTs in large scale displays, such as laptop monitors and televisions [26], [27].

On the contrary, while a-Si:H TFTs have a low carrier mobility compared to LTPS, it is enough to drive a μ LED, and provide a bright emission in the pixel [21]. Additionally, it has less fabrication masks required, and its amorphous nature raises its inertia to effects such as trap and defect density, which cause variations in its electrical properties. This makes a-Si:H TFTs more suitable for large scale displays and mass manufacturing [26], [27]. a-Si:H TFTs are also the TFT technology used in this work. The following subsection will go more into the device physics of a-Si:H TFTs and their structures.

2.4 a-Si:H Device Physics and Operation

To understand the operation of a-Si:H TFTs, it is important to look at the semiconductor physics for this material. Figure 2.8 shows the density-of-states (DOS) diagram for a-Si:H and compares it to crystalline silicon.

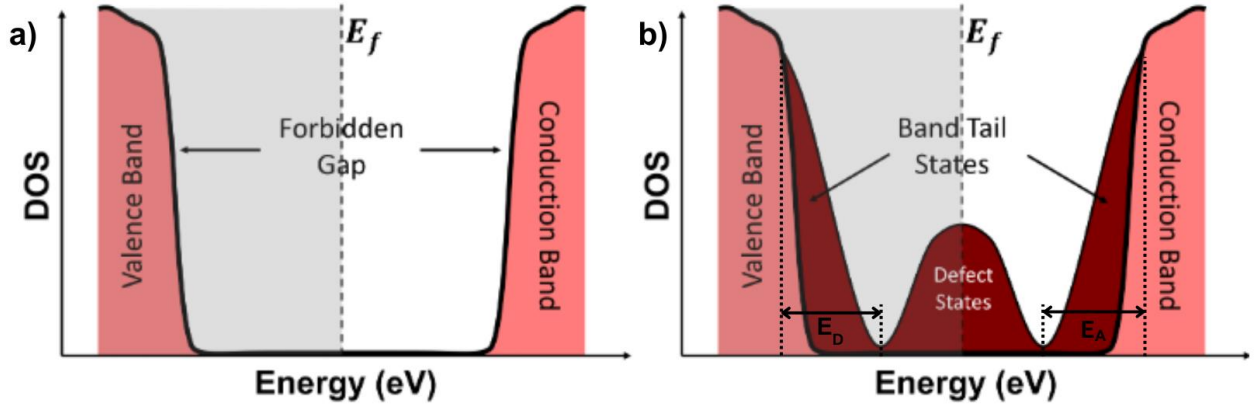


Figure 2.8: DOS diagram for a) crystalline silicon and b) intrinsic $a\text{-Si:H}$ [28].

From the figure, with crystalline silicon, there is a defined band gap, as shown by the abrupt band discontinuities for the valence and conduction band. However, this is not the same case for amorphous silicon as the DOS is continuous across the energy range. Unlike crystalline silicon, there is no defined order due to its amorphous-like nature. In the middle of the forbidden gap, there is a presence of defect states that are attributed by dangling and strained Si-Si bonds [28]. A lot of these dangling and strained bonds are introduced during fabrication processes. Additionally, the presence of the localized states causes a tail broadening to extend into the valence and conduction band. E_D and E_A represent the valence tail-band width and the conduction tail-band width, respectively [29]. While $a\text{-Si:H}$'s amorphous nature gives it a larger area uniformity than LTPS, these dangling bonds result in a lower carrier mobility. These dangling bonds also result in its threshold voltage, V_T being more sensitive to large, induced stress [21], [26], [30]. Additionally, the naturally occurring n-type nature of $a\text{-Si:H}$ does not allow for a complementary transistor type, making it difficult to implement CMOS-like logic [21].

2.5 Fabrication of $a\text{-Si:H}$ TFTs

Fabrication techniques can be employed to reduce the defect density at the semiconductor/dielectric interface of $a\text{-Si:H}$ TFTs. Figure 2.9 shows various device architectures employed.

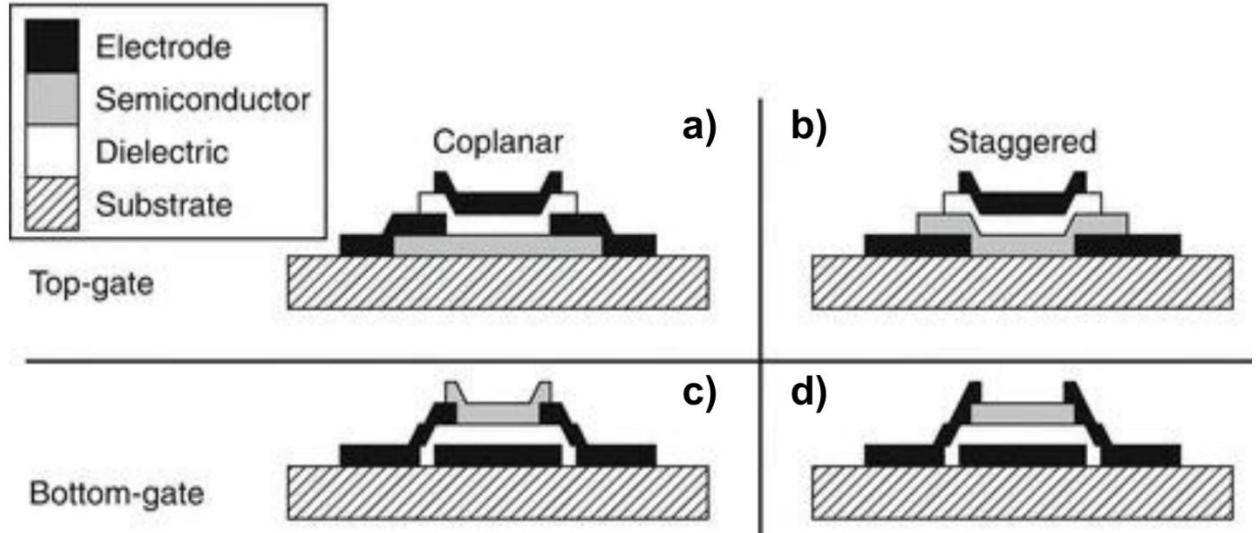


Figure 2.9: TFT device architectures for a) top-gate coplanar, b) top-gate staggered, c) bottom-gate coplanar and d) bottom-gate staggered $a\text{-Si:H}$ TFTs [31].

The names “top-gate” and “bottom-gate” refer to the location of the gate electrode in relation to the dielectric. Top gate TFTs are formed by having the gate electrode on top of the dielectric, whereas bottom-gate TFTs have the gate electrode sandwiched between the dielectric and the substrate. Likewise, the terms “coplanar” and “staggered” refer to the location of the source and drain electrodes and the dielectric, relative to the channel. For coplanar structures, the source and drain electrodes and the dielectric are located on the same side of the channel, whereas for staggered, the dielectric and semiconducting layer is sandwiched in between the source and drain electrodes [21], [32].

In terms of performance, the bottom-gate staggered architecture is the best for $a\text{-Si:H}$ TFTs. In coplanar structures, the semiconductor and dielectric would have to be deposited separately. Doing so increases the defect density at the semiconductor/dielectric interface. For staggered structures however, the semiconductor and dielectric can be deposited subsequently, without having to open the vacuum chamber, reducing the defect density. This helps improve the carrier mobility. Additionally, the staggered structure gives a lower contact resistance than the coplanar structure, which contributes to a higher carrier mobility [21], [31], [33].

Typically, the fabrication for bottom-gate staggered $a\text{-Si:H}$ TFTs uses a 4-5 mask process. After the gate metal is deposited and patterned, the dielectric ($a\text{-SiN}_x\text{:H}$), intrinsic $a\text{-Si:H}$, and the n^+ $a\text{-Si:H}$ doped layer is deposited in a PECVD process in the same vacuum [21], [31]. This can be done in a quick, sequential process, thanks to its staggered structure. The PECVD process is normally done at

temperatures less than 300°C, which is significantly lower than CMOS technology. Following that, the source and drain electrodes are deposited. These electrodes are patterned and etched, commonly using reactive ion etching (RIE) to do so. This RIE etch continues until the n^+ a-Si:H layer is etched enough to the point where the intrinsic a-Si:H channel is exposed. There is a slight degree of over-etching into the intrinsic a-Si:H as there is no etching selectivity between the n^+ a-Si:H and intrinsic a-Si:H. Post-etch annealing is commonly employed to minimize the defect density on the back surface.

2.6 Summary

This chapter summarized the key components and operation of the display panel. The components include the off-panel peripheral circuitry, the display panel, and the TFT devices implemented in the pixel array. This chapter also investigated the device physics and operation of a-Si:H TFTs. With the growing demand in high resolution displays, there is also growing interest into integrating the peripheral circuitry onto the backplane. This, however, is bottlenecked by the bonding pad pitch, connecting the peripheral circuit to the display backplane. Additionally, for an $N \times M$ display containing N row drivers and M data drivers, the relative cost of the display driver to the backplane scales with $1/N$. This is an indication that a huge area of the display is taken up by the drivers, also leading to a high cost [34]. One way to approach this problem is to find a TFT alternative to realizing CMOS-like logic. a-Si:H TFTs are an ideal candidate for large scale displays as they have more uniformity over LTPS TFTs, and they require less fabrication masks, making it more cost-friendly to fabricate. However, a-Si:H TFTs are naturally n-type, which makes it hard to implement CMOS-like logic as a replacement to the off-panel circuitry. To make this idea possible, it is imperative that smart circuit design techniques are realized to innovate energy-efficient, full-swing TFT logic gates, with CMOS-like functionality. The following chapter will investigate CMOS-like logic gates formed by unipolar a-Si:H TFTs, and the design changes leading up to the state-of-the-art a-Si:H unipolar inverter.

Chapter 3: TFT Design and Evolution for Realizing CMOS-Like Logic

With rapid demand in the research of wearable devices, flexible electronics, displays and the Internet-of-Things (IoT) devices, TFTs have been investigated as the main device element for these display systems. TFTs have been seen as a promising device element due to their low fabrication cost and ease of mass production. Additionally, unlike rigid CMOS, TFTs can also be fabricated onto a glass and flexible substrate. Currently, amorphous silicon (a-Si:H) and transition metal-oxide TFTs have demonstrated their capabilities on glass and flexible substrate.

AM displays are key components in devices such as computer monitors, smartphones, laptops, portable gaming consoles and wearable devices. These displays are trending towards becoming the primary display technology in today's market. In the conventional display backplane, the use of TFTs is still quite limited, mostly being used for forming the pixel arrays. The rest of the peripheral timing-control and signal generation is done off the backplane and are realized by off-panel CMOS integrated circuits (ICs). The bonding pads connect the row and column driver components to the respective rows and columns of the display pixel array (see Figure 1.2).

This design, however, is facing severe limitations. As the demand for displays has been increasing, so too has the resolution. Nowadays, demands for displays have been reaching as high as 4K (4096 rows x 2160 columns) and even 8K Ultra-High Definition (UHD) (7680 rows x 4320 columns). With each new row and column of pixels added to the display, an additional bonding pad needs to be connected, to properly interface the off-panel ICs with the display panel. This puts a limitation on the display size, as the bonding pad pitch cannot be reduced infinitely [21]. Thus, it is important to find an alternative to the off-panel IC component and integrate it onto the display backplane. Doing so will help reduce the cost, power consumption and fabrication steps.

Recent research has been investigating the use of TFTs to change the off-panel CMOS row driver and integrate it onto the display backplane. However, unlike CMOS, disordered a-Si:H semiconductor TFTs are primarily unipolar, lacking the complementary type that CMOS has. While it is possible to implement CMOS-like logic with additional TFTs, this makes it hard to implement this type of logic, due to the high static leakage current, high dynamic power consumption, and low stage-to-stage gain. This chapter will focus on the evolution of unipolar TFT logic gates, and their implementation onto address logic for integration onto a backplane display.

3.1 The 2T NMOS Inverter

Any complex circuit can be realized by using any combination of the inverter (NOT), NAND and NOR gate. These gates are commonly referred to as the fundamental building blocks of a circuit, performing any sort of desired logical operation. In CMOS technology, these advanced combinational circuits are typically formed by a Pull-Up-Network (PUN) and a Pull-Down-Network (PDN). The PUN and PDN consists of PMOS transistors, passing logic 1, and NMOS transistors, passing logic zero, respectively. These network implementations are complementary to each other. For example, a series configuration in the PUN performing an AND logical operation would be complemented by a parallel configuration in the PDN performing an OR operation. Figure 3.10 shows the complementary logic gate as a combination of the PUN and PDN. With this general connection, the output can pass either a logic 1 or a logic 0, perfectly [35].

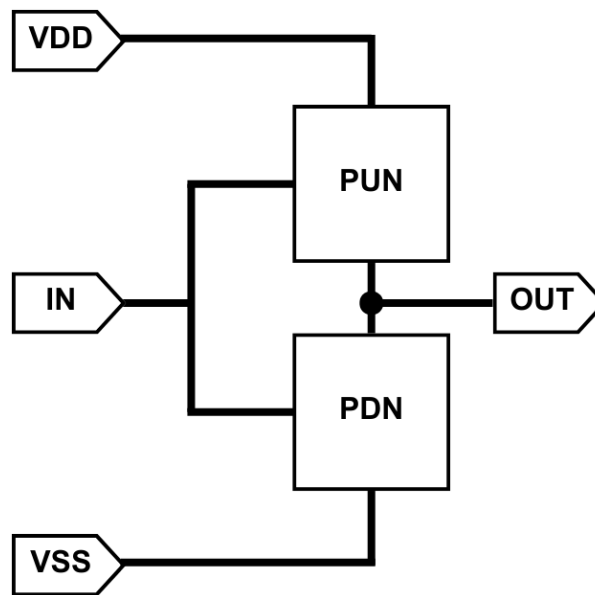


Figure 3.10: Combinational Circuit Connection.

This idea, however, cannot exactly be replicated in TFT design so easily. In the case of a-Si:H TFTs, these TFTs are unipolar. Unlike CMOS technology, in which electrons and holes are the charge carrier, a-Si:H TFTs use n-type carriers, or electrons as their primary charge carrier. a-Si:H TFTs also exhibit n-type behaviour naturally, which makes implementation of fundamental gates like the inverter difficult. The simplest NMOS implementation of the conventional CMOS inverter is the 2T NMOS

inverter, as shown in Figure 3.11. The PDN and PUN are formed by devices T_0 and T_1 , respectively. The input is connected to gate of T_0 , and T_1 is diode configured load with its gate connected to V_{DD} .

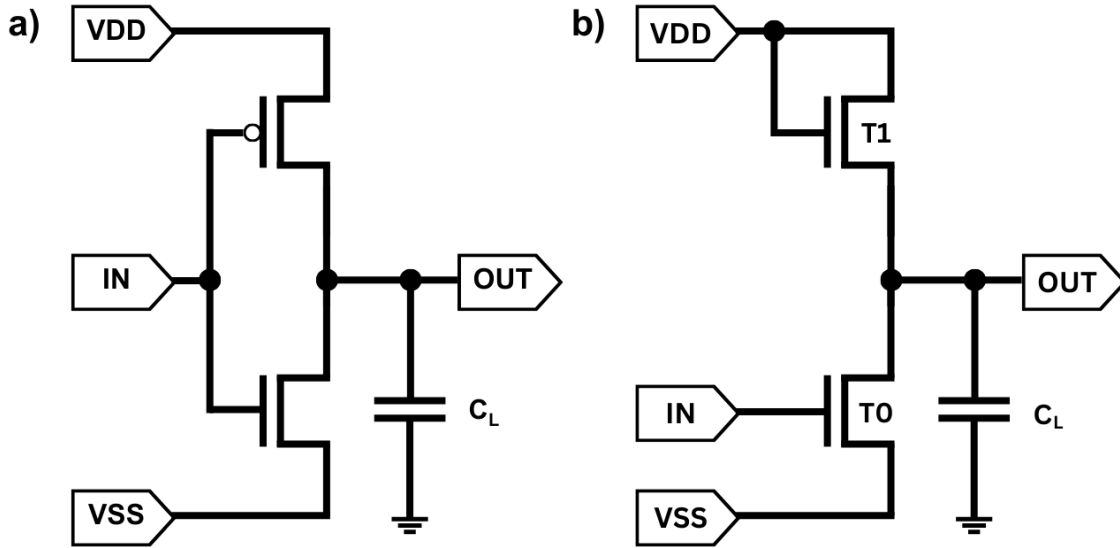


Figure 3.11: a) CMOS inverter and b) 2T NMOS inverter schematic.

To understand the behaviour of the 2T inverter, it is important to understand how the output responds to the different input transitions. For a $1 \rightarrow 0$ input transition, T_0 will be turned off, and the voltage can pass from V_{DD} , through T_1 , and charge the load capacitor, C_L . Because T_1 is diode configured load, it will always remain on and in saturation mode. However, NMOS devices are weak at passing logic 1. As a result, there will be a voltage drop at the output, equating to $V_{out} = V_{DD} - V_{TH}$, where V_{TH} is the threshold voltage of T_1 . Conversely, for a $0 \rightarrow 1$ input transition, T_0 will be switched on. However, unlike the CMOS inverter, where the PMOS and NMOS transistor will be OFF and ON, respectively, allowing for a direct path to ground, here both T_0 and T_1 will be on during this transition. The output voltage will not be able to fully dissipate to ground, as both T_0 and T_1 being on will result in voltage division at the output. This is seen in the transient simulation in Figure 3.12, as the output cannot reach V_{DD} for a $1 \rightarrow 0$ input transition, and V_{SS} for a $0 \rightarrow 1$ input transition. Additionally, because T_1 is always on, there is always a conductive path from V_{DD} to the output node, resulting in high short-circuit current (I_{sc}) and static power dissipation. While this is the simplest implementation of an inverter, in terms of device footprint and complexity, using only two unipolar NMOS TFTs, the 2T inverter is a poor choice for achieving fast rail-to-rail swing, with minimal power consumption (for subsequent subsections describing other inverters, C_L will be omitted from the circuit schematic for simplicity).

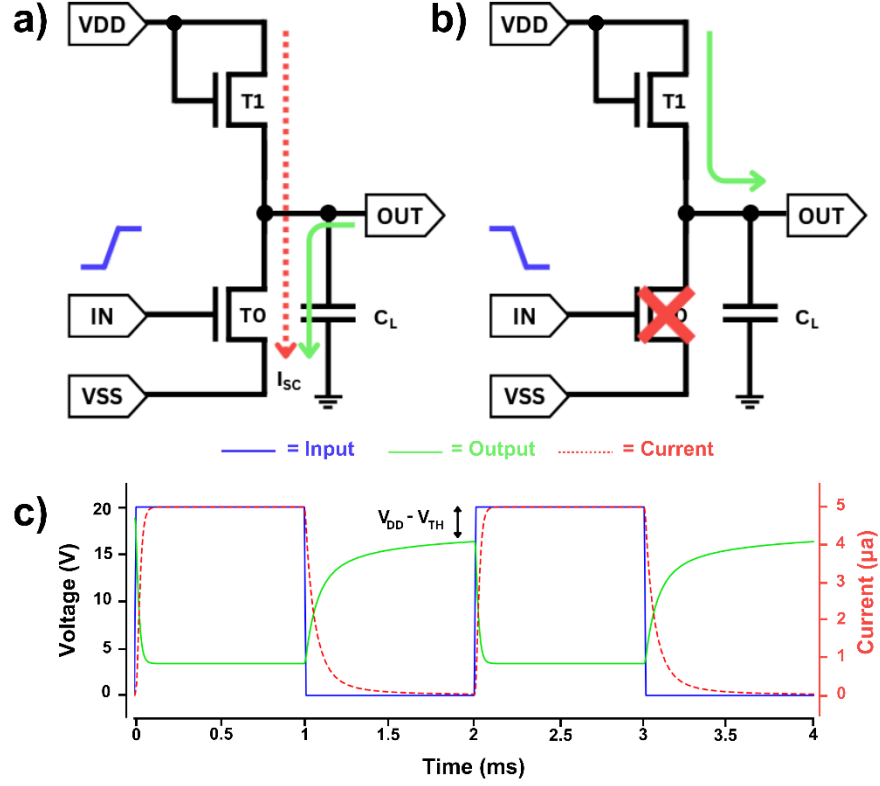


Figure 3.12: a) 0→1 input transition, b) 1→0 input transition and c) transient output waveform for the 2T inverter.

3.2 Prior work - 4T Inverter

The 4 TFT inverter (4T) was developed by Zhao et. Al, in hopes of tackling the high I_{sc} and static power dissipation [36], [37]. This is done, by adding an additional stage to the 2T inverter, similar to the 4T Pseudo-CMOS inverter, as shown in Figure 3.13 [38]. Devices T_0 and T_1 consist of the first stage, akin to the 2T inverter, and devices T_2 and T_3 consist of the second stage, along with a boost capacitor, C_{Boost} . T_0 and T_2 serve as the pull-down devices, and T_3 and T_1 serve as the pull-up devices. Node A is connected to the gate, source and drain of T_1 , T_3 , and T_2 , respectively. T_3 , being diode connected to V_{DD} , will always remain on and in saturation mode, charging node A.

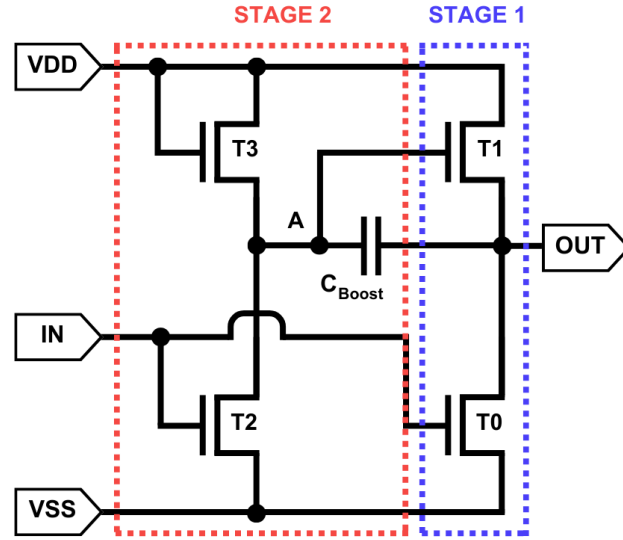


Figure 3.13: Prior work - 4T inverter schematic.

In the case of a $0 \rightarrow 1$ input transition, T_0 and T_2 will turn on, forming a conductive path for node A to fully discharge to roughly V_{SS} . This is done so by having a considerable size mismatch between T_2 and T_3 . The channel width of T_3 is kept very low, so that the amount of I_{sc} is kept very low. Conversely, the channel width of T_2 is kept very large, especially in comparison to T_3 . By doing so, the on resistance (R_{ON}) is kept very low, which allows node A to discharge near V_{SS} , thus minimizing node A's voltage. Additionally, with the node A voltage being minimized, its voltage does not exceed the V_{TH} of T_1 , preventing T_1 from turning on. For a $1 \rightarrow 0$ input transition, devices T_0 and T_2 will turn off. The node voltage, A, will turn T_1 on, forming a conductive path to charge the output. This is done so, in tandem with C_{Boost} , raising the output voltage to near V_{DD} , thus improving the output swing, that the 2T inverter was not able to achieve. The input transitions and output transient waveform is shown in Figure 3.14.

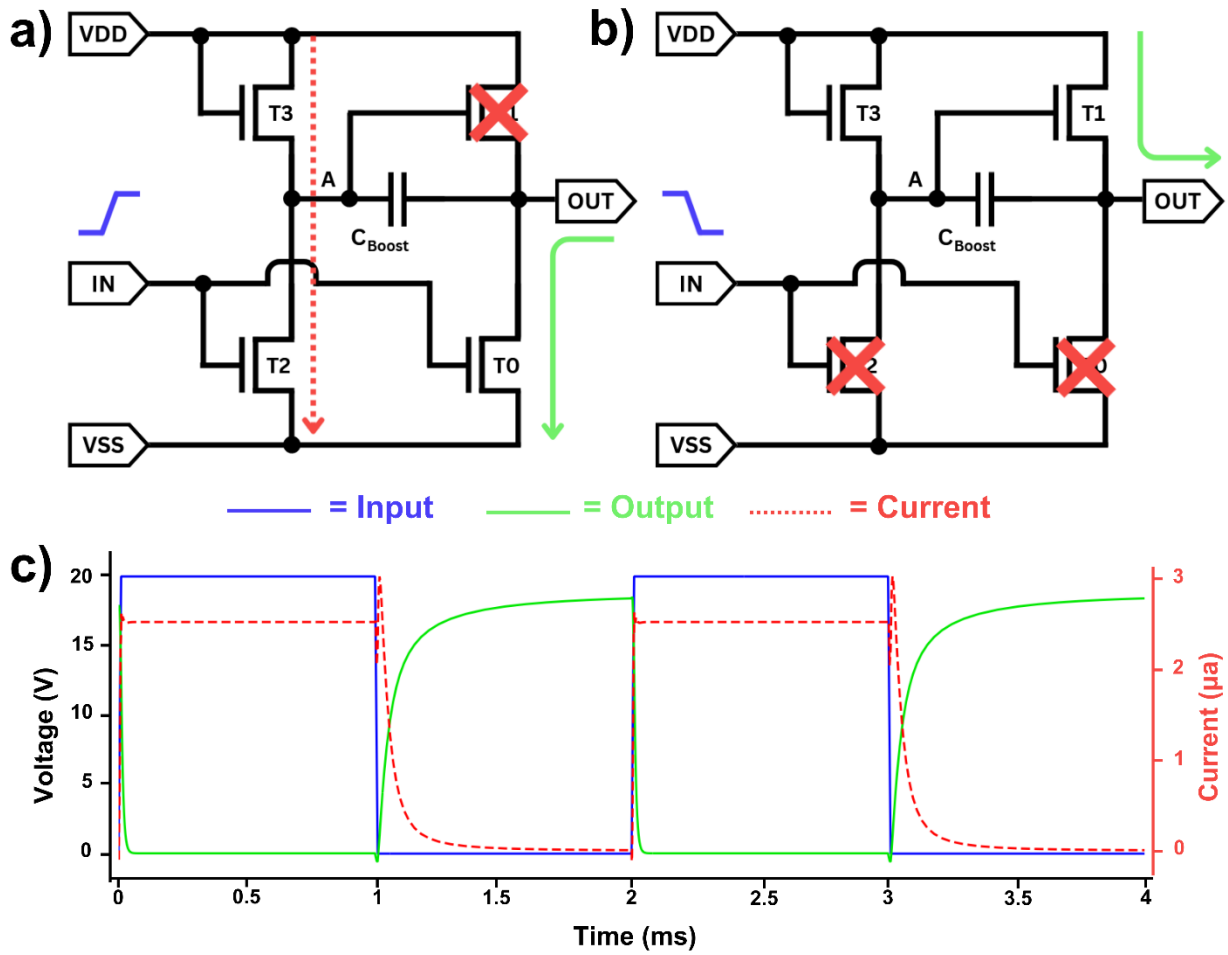


Figure 3.14: Prior work - 4T inverter showing different input transitions and transient waveform.

3.3 Prior work – 7TFT+1C inverter with an external bias applied.

Hwang et. Al developed a 7TFT + 1C (7T1C) inverter with an external bias (V_{Bias}) in aims of addressing the challenges with achieving full output swing, and the schematic is shown in figure 3.15 [39]. T_2 , T_4 , and T_6 serve as pull-down devices, and T_3 , T_5 and T_7 serve as pull-up devices. T_1 is driven by an external V_{bias} . Similar to the case of the 4T inverter, node C drives the gate voltage of T_5 , and node B + the boost capacitor drives the gate voltage of T_3 and T_7 .

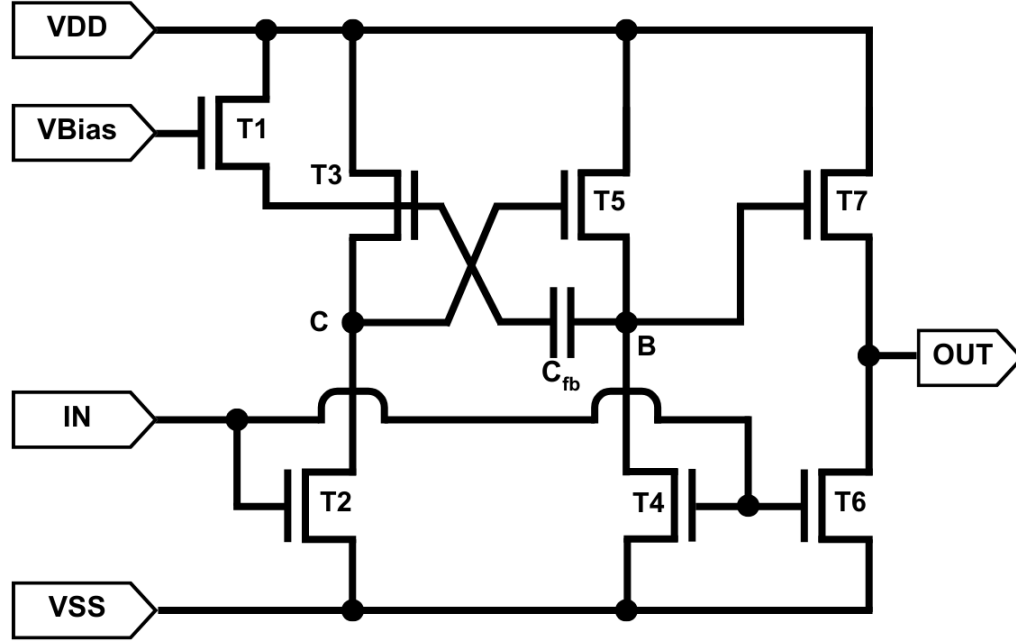


Figure 3.15: Prior work – 7T1C inverter with external V_{Bias} circuit schematic.

In the case of a $0 \rightarrow 1$ input transition, devices T_2 , T_4 , and T_6 will turn on. A conductive path is formed, allowing for nodes B and C to discharge to ground, and this allows T_3 , T_5 and T_7 to turn off, as the node voltages driving their gate voltages discharge to ground. This allows the output to dissipate near V_{SS} . Conversely, for a $1 \rightarrow 0$ input transition, devices T_2 , T_4 and T_6 will turn off. The drain-source current from T_3 will increase the gate voltage of T_5 , which is followed by V_{DD} , further driving the gate voltages of T_3 and T_5 . As a result, a positive feedback loop is formed between T_3 and T_5 . The external V_{Bias} plays a key role in charging the boost capacitor, C_{fb} . By doing so, the gate voltage of T_3 is kept above its V_{TH} , and the 7T1C inverter can achieve a full output swing to V_{DD} . However, this does so at the cost of an extra bias signal, leading to extra power dissipation and layout area. Additionally, T_3 and T_5 are cross coupled, which contributes to the area footprint and complexity of the layout, making this design difficult to integrate on a display. The input transitions and output transient waveform is shown in Figure 3.16.

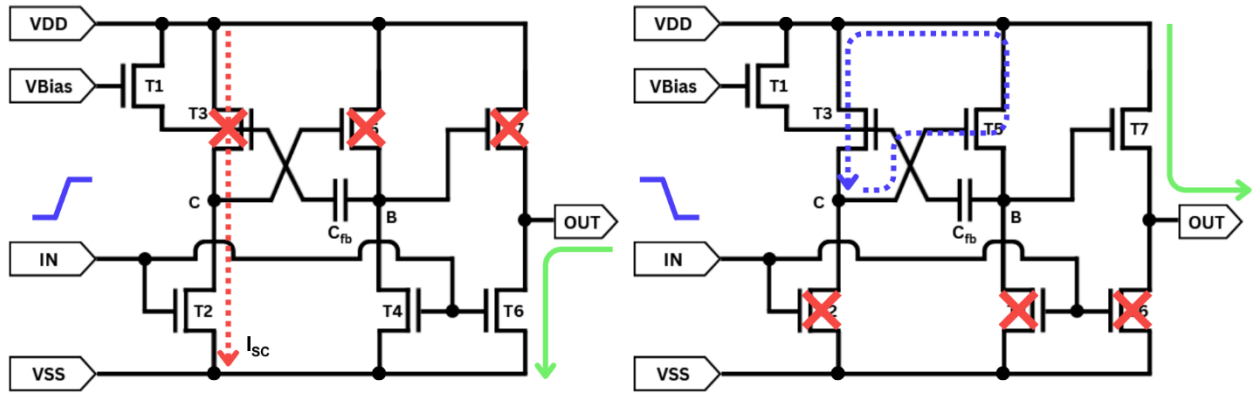


Figure 3.16: Prior work - 7T1C inverter showing different input transitions.

3.4 Prior work – The bootstrapped 7T inverter

In the aim of achieving rail-to-rail output swing while minimizing power consumption, Papadopoulos et. al proposed a bootstrapped 7T inverter, shown in Figure 3.17 [40]. T_0 , T_2 and T_6 are pull-down TFTs and T_1 , T_3 and T_4 are pull-up TFTs, respectively.

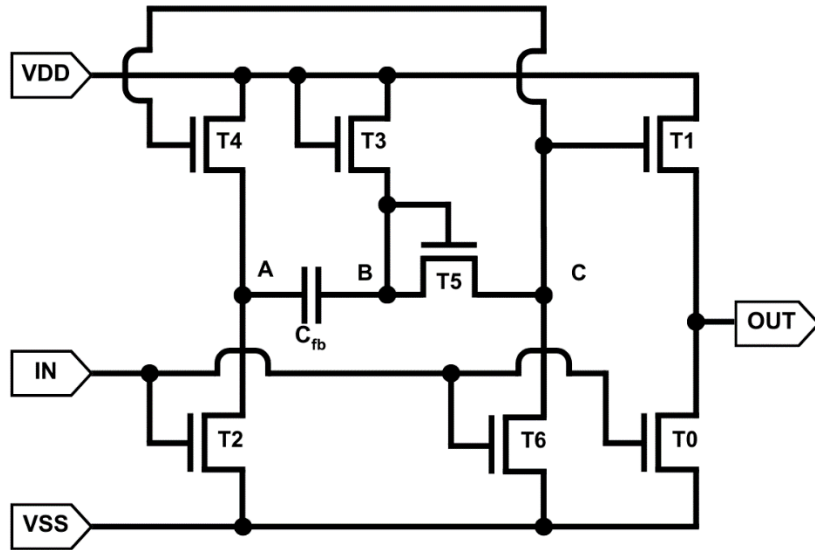


Figure 3.17: Prior work - 7T bootstrapped inverter circuit schematic.

For a $0 \rightarrow 1$ input transition, T_0 , T_2 and T_6 will turn on. This allows nodes A and C to drain fully, and this turns off T_1 and T_4 . T_5 and T_6 play a crucial role in eliminating the direct path of T_1 and T_4 to V_{SS} during this input transition. T_5 and T_6 are sized accordingly to minimize the conductivity of T_1 and T_4 . T_3 and T_5 being diode-connected, form a conductive short-circuit path, connecting V_{DD} to ground. This helps lower the static power consumption by eliminating the short circuit paths from V_{DD} to ground,

going through T_1 or T_4 . For a $1 \rightarrow 0$ input transition, T_0 , T_2 and T_6 will be turned off. This allows node B to be boosted by node A and the feedback capacitor, C_{fb} . Being boosted to above V_{DD} , node B can drive the gate voltage of T_1 , such that the output can still achieve a full output swing. The input transitions and output transient waveform is shown in Figure 3.18. More will be discussed on the bootstrapping mechanism in the following subsection.

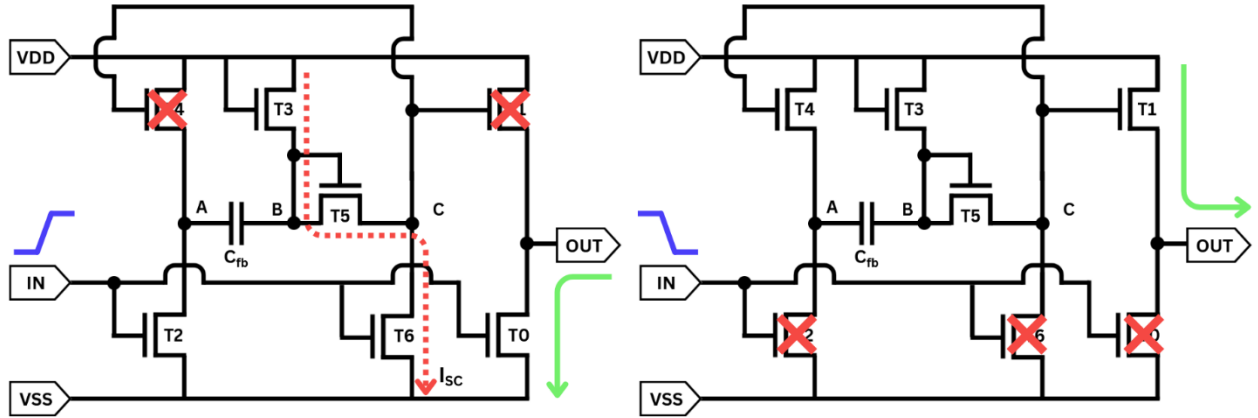


Figure 3.18: Prior work - 7T bootstrapped inverter showing different input transitions.

3.5 Prior work – state of the art bootstrapped 5T inverter

Currently, the bootstrapped 5T inverter is the most recent implementation of the bootstrapped inverter. While the 7T bootstrapped inverter provides rail-to-rail output swing, this does so at the expense of a larger device footprint. Qing et. al presents a similar bootstrapped inverter, using 5 TFTs, (5T), instead of 7. This is shown in Figure 3.19 [41].

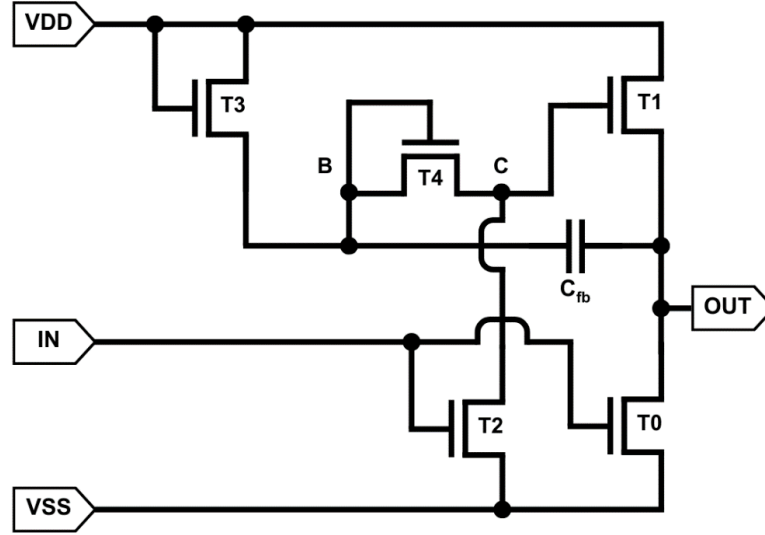


Figure 3.19: Prior work – state of the art 5T bootstrapped inverter circuit schematic.

A detailed explanation of the bootstrapped mechanism is provided below. For a $0 \rightarrow 1$ input transition, T_0 and T_2 will turn on. A short circuit path (see figure 3.12a) indicated by the dashed red arrow shows the leakage path formed by T_3 and T_4 . T_4 and T_4 are diode-connected and will be operating in the linear regime during this transition. This path allows node C to drain to V_{SS} and as a result, T_1 will be turned off. This allows the output to fully drain to ground. Additionally, the voltage stored in the feedback capacitor, C_{fb} will be $\approx \frac{1}{2} V_{DD}$ because of the voltage division onto node B. The voltage stored on C_{fb} is important for a $1 \rightarrow 0$ input transition. During this transition, T_0 and T_2 will be turned off. The voltage on node C will slowly go up, and this node voltage, driving the gate of T_1 will turn T_1 on. As T_1 turns on, a positive feedback loop forms between T_1 , T_4 and C_{fb} , boosting all the node voltages along this path. Their steady-state voltages reach to $V_B \approx \frac{3}{2} V_{DD}$, $V_C \approx \frac{3}{2} V_{DD} - V_{TH}$ and $V_{out} = V_{DD}$, thus allowing for the full output swing [42]. It should be noted that with the dielectric thickness and the steady state voltage across C_{fb} being V_{TH} , C_{fb} doesn't experience breakdown at the operational voltage of 20V. To investigate the breakdown, a test bench supply voltage of 30V was applied to V_{DD} . Even at this voltage, C_{fb} did not experience breakdown, and the voltage across C_{fb} would never be above 20V. The transient behaviour is shown in Figure 3.20. The transistor device sizing for the 5T bootstrapped inverter is also shown in Table 3.2.

This same bootstrapped logic can be used to build the other fundamental gates, the NAND and the NOR gate. Figure 3.21 shows the circuit schematic for these gates. The overall complexity of the circuit remains unchanged. The bootstrapping mechanism still follows that same positive feedback loop of T_1 ,

T_4 and C_{fb} . The only changes implemented are the connections in the PDN, either performing a NAND or NOR operation, with the addition of T_5 and T_6 .

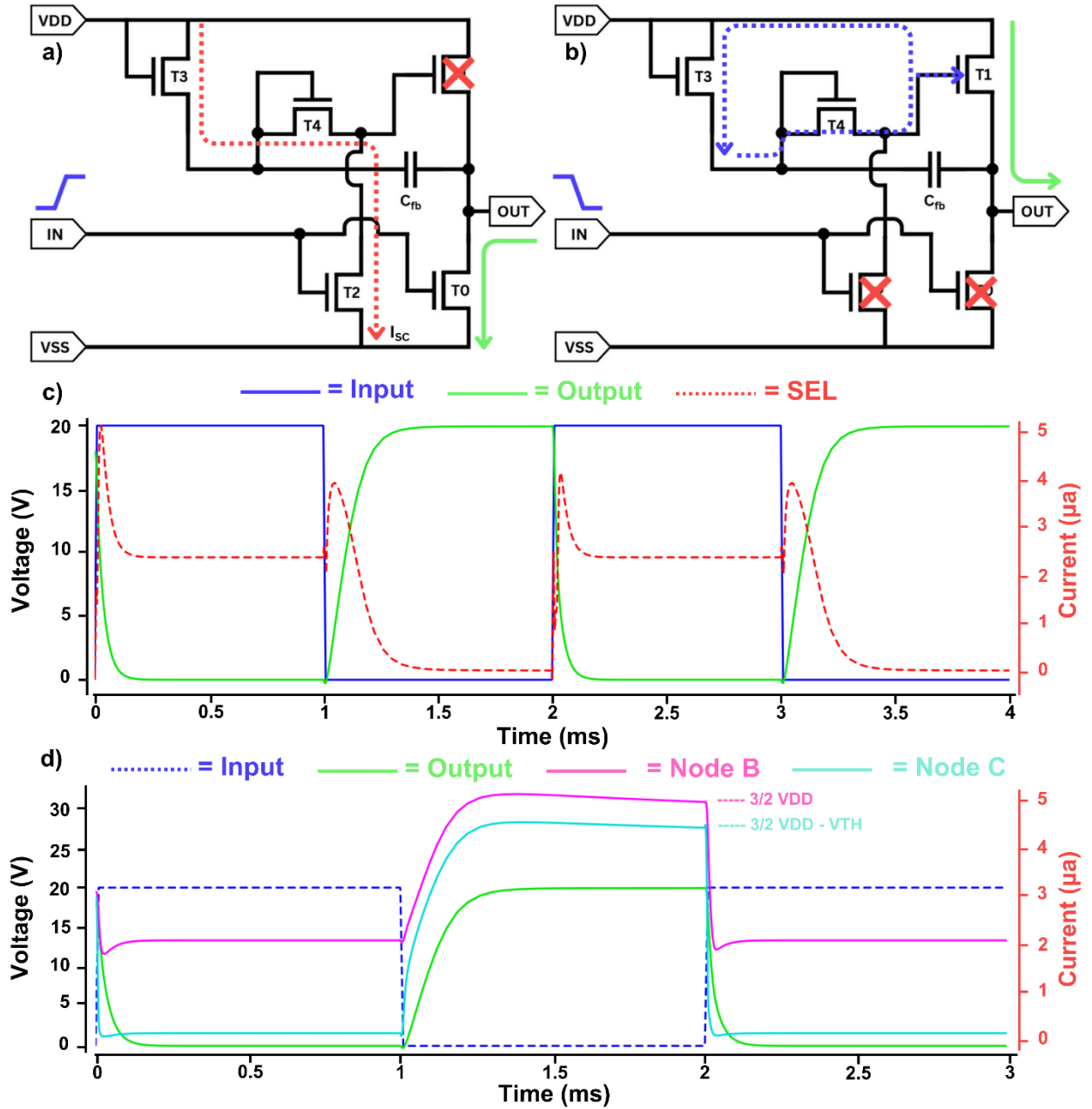


Figure 3.20: a) 0→1 input transition b) 1→0 input transition c) output transient waveform and d) transient waveform showing steady state voltages for nodes B and C and output.

Table 3.2: Transistor sizing for the 5T bootstrapped inverter

	T_0	T_1	T_2	T_3	T_4	C_{fb}
W/L	100/20	100/20	100/20	200/20	40/20	12.51pF

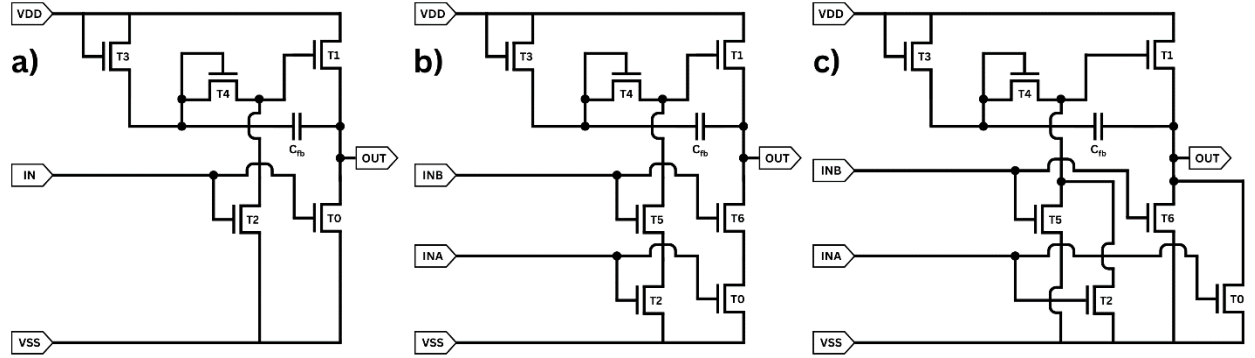


Figure 3.21: Circuit schematic for the a) 5T bootstrapped inverter, b) 7T bootstrapped 2-input NAND gate and c) 7T bootstrapped 2-input NOR gate.

3.6 Summary of Chapter 3

To revisit the introduction of this chapter, the growing demand in the display industry has given rise to the pixel density, and the number of bonding pads required to interface the external IC to the display panel. This, however, is reaching its limit, due to the size of the bonding pads. Recent research interest has investigated implementing CMOS-like logic in TFTs, so that the external ICs can be replaced with TFT logic gates, and thus, more of the backplane can be fully integrated. However, the main problem with realizing CMOS-like logic in TFTs is the limited rail-to-rail output swing and high static power dissipation. Many changes have been implemented, to improve upon the conventional 2T inverter. The 4T inverter looked at adding an additional stage, helping eliminate static leakage paths and boosting the output swing through a feedback capacitor. The 7T inverter with an additional bias helps further drive the output voltage to V_{DD} , by providing additional voltage to charge the boost capacitor, forming a feedback loop that raises the output voltage node. The more recent work, the 5T bootstrapped inverter, eliminates the need of an additional bias, and forms a bootstrapping network, which serves as a positive feedback loop to help drive the output to V_{DD} at steady state, while lowering the static power dissipation. These changes have made realizing CMOS-like logic possible in TFT circuits.

The logic gates shown in Figure 3.21 serve as the fundamental building blocks for implementing address logic to drive the pixel array. The following chapter will focus on this logic implementation via address decoders, as well as energy saving methods to make this an ideal alternative to the off-panel ICs, and thus be integrated onto the display panel.

Chapter 4: Implementing Low Power Address Logic with TFTs

In the previous chapter, the bottlenecks addressed to realizing CMOS-like logic with unipolar TFTs was from the low stage-to-stage gain and high static power dissipation, due to the static leakage paths present. However, these bottlenecks can be mitigated by adding additional stages to the conventional 2T inverter, and through bootstrapping, forming a positive feedback loop to help drive the output voltage to its desired levels. With these major findings implemented, it is possible to realize address logic. Going back to the proposed schematic as shown in Figure 4.22, research interest has been invested into fully integrating the IC components onto the backplane.

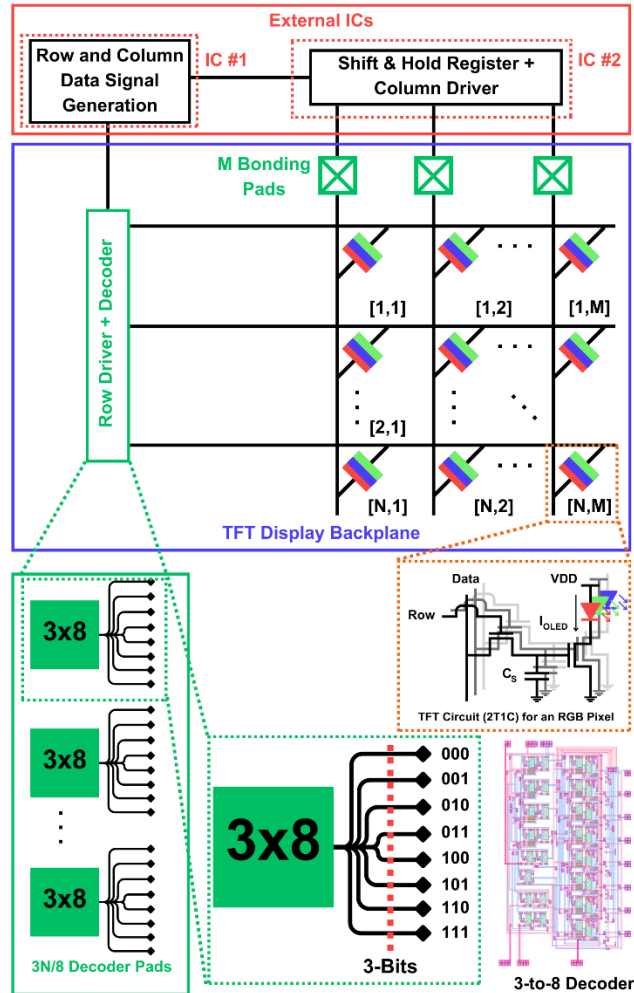


Figure 4.22: Proposed display panel architecture, with an integrated TFT row-driver circuit.

The upside to this approach is that it reduces the overall cost of fabrication, power consumption, and scalability. Recent work has shown a unipolar TFT row-addressing scheme, in which it reduces the number of bonding pads from N to $3N/8$ decoder pads instead. This presents a good framework to integrate the row-driving component onto the display panel. However, there is still additional work to be done, in terms of reducing the power consumption even further. As the pixel density increases, so too does the row-line capacitance for each row. This contributes to a high dynamic power, and this has been the bottleneck for realizing large-scale unipolar TFT displays.

This chapter focuses on reducing the dynamic power consumption via charge-sharing. In memory logic for example, where the signal timing is indeterministic, it is not reasonable to implement a charge-sharing scheme. However, for row addressing logic, in which the timing of the signals is known and follows row-by-row, it is possible to implement charge-sharing between each row. This is done by implementing tri-stating logic, and connecting the rows, such that the charge can be distributed sequentially. This work done in this chapter presents a charge-sharing scheme for various row address decoders, and compares the power consumption to the conventional decoders, using simulated and measurement results.

4.1 Address Decoders Using the State-of-the-art 5T Bootstrapped Inverter

In a display panel, each row is driven, one at a time, with the following row driven after the current row is off. A way to implement this sequential row driving is through a row-decoder. Figure 4.23 shows the general operation of the row driver circuit with the output waveform, and 1-to-2 row-decoder cell.

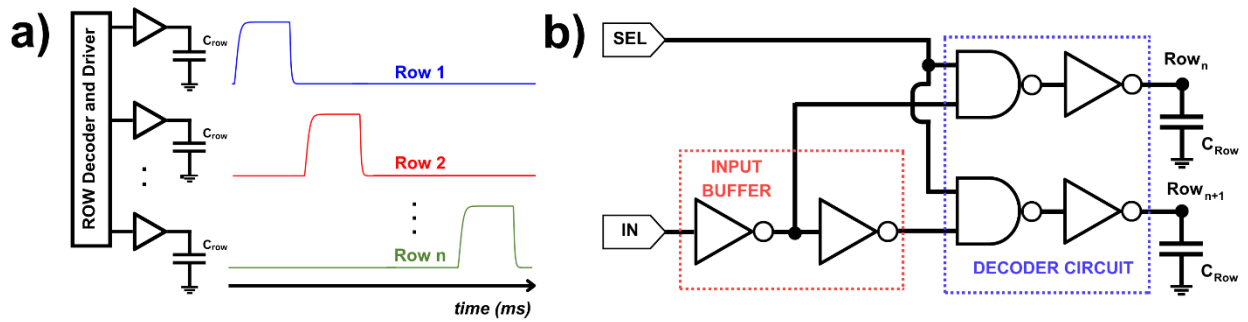


Figure 4.23: a) Row driving scheme for an AM pixel array and b) Gate-level schematic of the row-decoder cell.

Recently, Qing Li et. al presented a unipolar row decoder, using the state-of-the-art bootstrapped inverter for a cell size of 1-to-2 and 3-to-8. Figure 4.24 shows the output transient waveform for the proposed 3-to-8 decoder, using the state-of-the-art unipolar TFT inverter, and compared it against the

conventional 2T inverter. From the transient simulations, with the conventional inverter in the decoder circuit, the decoder is unable to achieve the desired rail-to-rail output swing and have high power consumption. This can be attributed to the leakage path present, regardless of the input transition, as well as the voltage division at the output node. Contrary to the conventional 2T inverter, with the 5T bootstrapped inverter in the decoder circuit instead, the decoder was able to achieve the desired rail-to-rail output swing. Additionally, the elimination of the static leakage paths allows for the internal nodes to fully discharge to V_{SS} , also allowing the output node to discharge fully. This in turn, also reduces the overall power consumption, by over 50%.

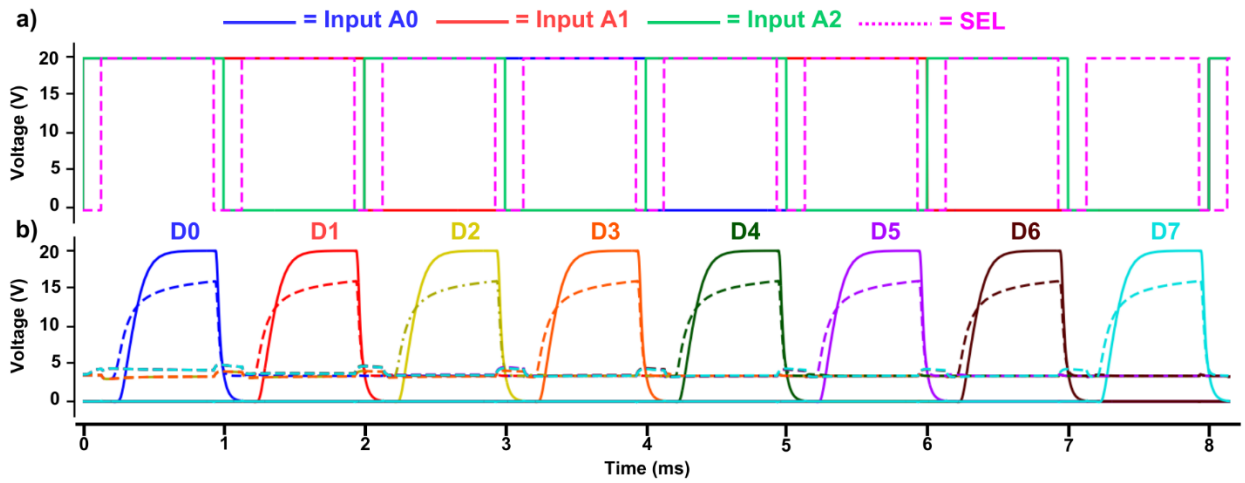


Figure 4.24: a) Input signals and b) output transient waveform for the 3-to-8 decoder. The dotted line in b) is the decoder circuit using the conventional 2T inverter.

4.2 Charge-Sharing Implementation in Address Logic

Power consumption is an important metric to consider, especially as the devices scale down, and the resolution demand goes up. For self-emissive AM display panels, the power consumption is divided into two main components – power consumption by the self-emissive media and the row and column control IC [10], [43], [44]. In CMOS circuit technology, common techniques employed to reduce the power consumption involve lowering the supply voltage and/or lowering the V_{TH} of the transistors. This cannot be easily translated into display panel driving as lowering the supply voltage will compromise the luminescence intensity of the OLED. Additionally, with a-Si:H TFTs having low mobility, compromising the switching speed even further would make it unable to produce the address logic as desired [45], [46].

The work done by Qing Li et. al presents a satisfactory proof of concept for the design of a low power row decoder, using the state-of-the-art 5T bootstrapped inverter in the decoder circuit. To fully realize a low-power display using unipolar TFTs however, extra attention must be taken to reduce the dynamic power consumption of the display. Theoretically, the energy withdrawn from the supply voltage can be described by the following equation [35]:

$$E_{V_{DD}} = C_L V_{DD}^2 \quad (4.1)$$

Where C_L represents the load capacitor of the row-line. In the case where the output goes high and is stored into the load capacitor, the energy stored in the capacitor is as follows:

$$E_c = \int_0^\alpha i_{V_{DD}}(t) V_{out} dt \quad (4.2)$$

Rearranging equation 4.2 to integrate in terms of V_{out} leads to the following equation:

$$E_c = \int_0^\alpha \frac{C_L dV_{out}}{dt} V_{out} dt \quad (4.3)$$

Applying the integration bounds from 0 to V_{DD} , equation 4.3 can be simplified to the following equation:

$$E_c = \int_0^{V_{DD}} C_L V_{out} dV_{out} \quad (4.4)$$

Thus, the energy stored on C_L equates to:

$$E_c = \frac{1}{2} C_L V_{DD}^2 \quad (4.5)$$

Each row line is connected to a gate of hundreds/thousands of pixels. In the case of an 8K UHD display, where each row is connected to 7680 pixels, and therefore there is a staggering contribution to the high capacitance of the row line, and this in turn results in a high dynamic power consumption of the row-driver circuit. Recently, charge-sharing for low-power circuits has been researched, to further lower the dynamic power consumption as the technology nodes further scale down, and the performance and/or resolution demands go up. Some previously implemented methods include differential logic [47], [48]. The main drawback behind differential logic, however, is the circuit complexity and the area footprint, which make it not suitable for integrating onto the display panel. Other methods include using multiple independent inputs to drive the transistors, which helps in

reducing the charge distributed amongst the internal junction capacitances, by splitting apart the conductive paths [49]. Likewise, the addition of extra inputs contributes to extra wiring and capacitance, posing the same area footprint problem as the former solution. However, using an additional input can help reduce the dynamic power consumption through charge-sharing. Instead of letting the stored output fully dissipate to V_{SS} (see equation 4.5), if a portion of that stored charge can be used to drive other outputs, then the dynamic power consumption can be reduced. Pakbaznia *et. al* implemented power gating, cutting off portions of the logical block to enable charge-sharing to the desired locations of the circuit, via a switching transistor [45]. Implementing logic for charge-sharing requires careful attention. In the case where the timing of the signals is indeterministic, it is difficult to achieve a charge-sharing pattern. However, for a row-decoder scheme where the output of the rows follows a sequential pattern, it is possible to innovate logic for charge-sharing. Sheida *et. al* proposed a row charge-sharing method, in which the row charge is recycled to charge sub-sequent rows to reduce the dynamic power consumption. This is done with a transmission gate, and the output charging a capacitor bank. The capacitor bank acts as a reservoir, charging up the subsequent row. The transmission gates along with the timing help maintain that row-by-row charge-sharing pattern [24], [50]. They further introduced row to row charge sharing, eliminating the need of capacitor bank, where a row before being discharged is shorted to subsequent row through a transmission gate. Thus, the subsequent row is charged to $\sim \frac{1}{2} V_{DD}$, before getting charged to full V_{DD} through its row driver. As the row driver is required to charge row only from $\sim \frac{1}{2} V_{DD}$ to full V_{DD} , instead of V_{SS} to V_{DD} , the dynamic power consumption of row driver was reduced. However, this method was implemented for micro-displays with a CMOS backplane. For unipolar TFT logic, additional logic must be implemented to enable charge-sharing in a unipolar row-decoder scheme.

To implement charge-sharing logic in unipolar TFTs, there are two major factors that must be considered. Firstly, additional logic must be implemented, such that the area is not majorly compromised, and can store an available floating voltage for charge-sharing. Secondly, proper timing must be implemented to properly distribute the stored charge. These two factors are addressed by a) implementing tri-stating logic and b) adding additional transistor gates and timing to the conventional decoder scheme.

4.2.1 Design and operation of the 6 Transistor Tri-state Inverter for Charge-Sharing

The design of the 6T tri-state inverter (6T_CS) builds upon the state-of-the-art 5T bootstrapped inverter. To enable charge-sharing, T_3 is driven by a SEL signal, along with T_5 . When SEL is '1', this functions as inverter with full output swing, while when SEL is '0', the output is in floating state (i.e., not driven to V_{DD} or V_{SS}). To reduce power consumption, charge-sharing method is employed. During charge sharing, the SEL signal is '0' and output of driver is in floating state. Since T_3 is not always drawing power from V_{DD} (like other state-of-the-art designs, shown in Fig. 3.17), the pull-up strength is reduced. To compensate for this, the width of T_1 is increased from $100\ \mu\text{m}$ to $200\ \mu\text{m}$. This is shown, through the rise time decreasing by $\sim 40\%$, from $752\ \mu\text{s}$ to $460\ \mu\text{s}$. Figure 4.25 shows the device level schematic of the 6T_CS inverter, along with its output behaviour waveform. The 6T_CS design also has a small impact on the area footprint, relative to the 5T bootstrapped inverter. The W/L (in μm) of the 5T and 6T_CS layouts are 855/670 and 1066/533, corresponding to a 2.9% increase in inverter area. The transistor sizing is also provided in Table 4.3.

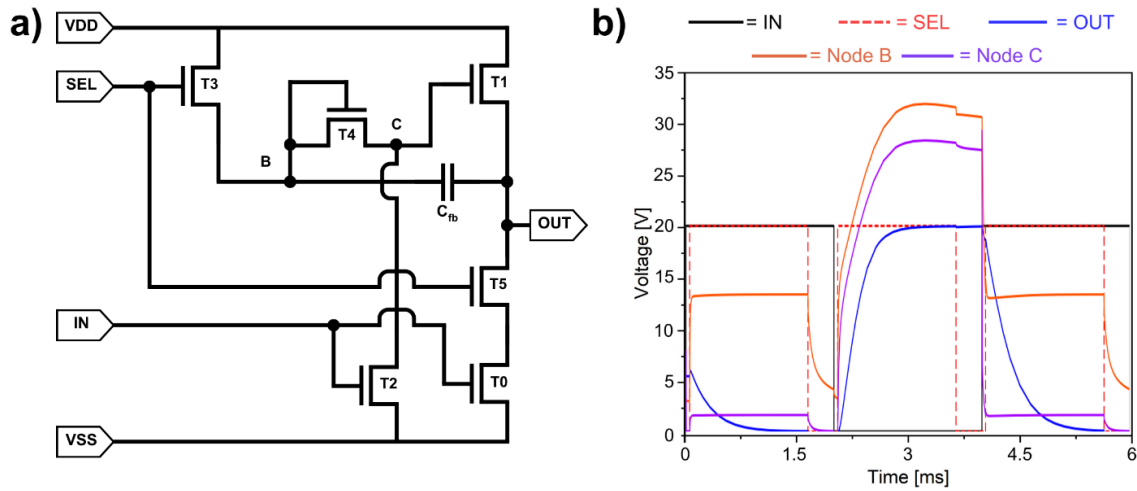


Figure 4.25: a) Device level schematic for the 6T_CS inverter and b) output waveform behaviour.

Table 4.3: W/L transistor sizing for the 6T_CS tri-state inverter.

	T_0	T_1	T_2	T_3
	100/20	200/20	100/20	200/20
W/L ratio	T_4	T_5	C_{fb}	
	40/20	100/20	15.012 pF	

In the case where IN and SEL are 1 or 0, the 6T_CS tri-state inverter behaves like the 5T bootstrapped inverter. Internal nodes B and C follow the same bootstrapping behaviour as the 5T bootstrapped inverter, rising to $\approx 3/2 V_{DD}$ and $\approx 3/2 V_{DD} - V_{TH}$, respectively. The main difference is that the rise time is significantly faster, going from $748 \mu s$ to $268 \mu s$, for the 5T inverter to the 9T_CS inverter. This can be attributed to the higher impedance on the pull-down path, now that T_5 is in series with T_0 . When $SEL = 1$ and $IN = 0$, the voltage is put in a floating state. This can be modulated, by changing the pulse width of the SEL signal. Conversely, when $SEL = 0$, and $IN = 1$, there is a high impedance on the pull-down path. A proposed charge-sharing decoder cell, utilizing the 6T_CS tri-state inverter is shown in Figure 4.26, along with the timing diagram. The changes to the conventional decoder are marked with a yellow box below. Instead of using the 5T bootstrapped inverter as the final driver, the 6T_CS tri-state inverter is utilized instead. Typically, in a row-driving scheme, a valid signal is sent to the corresponding row-line to de-assert it. The SEL signal employed in this design also helps in de-asserting the line, eliminating the need to implement an extra external signal. Additionally, a switching transistor is connected between row n and row n+1. When SEL goes low, the BK signal goes high. Instead of the stored voltage completely dissipating to V_{SS} , the floating voltage stored in row n when SEL is high can now be used to pre-charge row n+1, while SEL is low. Theoretically, half of the voltage stored in row n will go towards row n+1 during this time, and the remaining voltage will dissipate to V_{SS} once BK goes low.

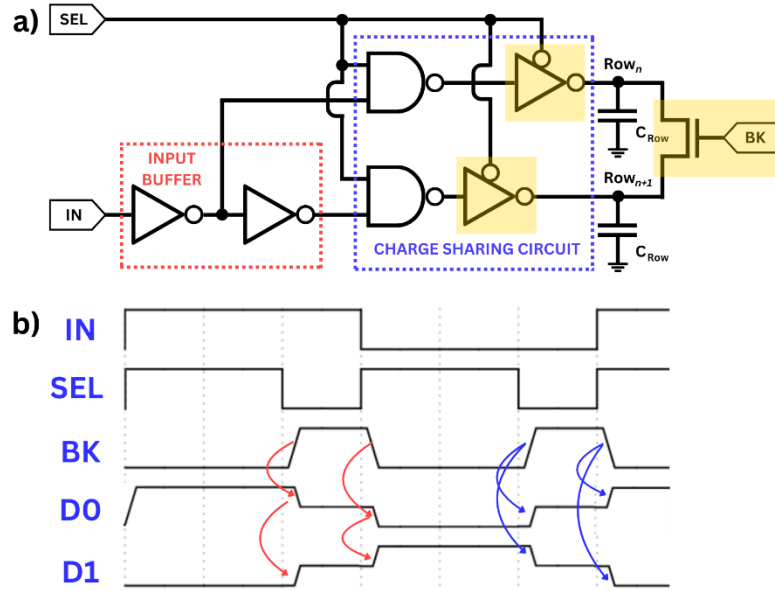


Figure 4.26: a) Proposed charge-sharing decoder cell and b) timing diagram for charge-sharing.

To validate the charge-sharing, a transient simulation was done on a 1-to-2 decoder utilizing the 6T_CS tri-state inverter, and these results were compared to the conventional decoder, using the 5T bootstrapped inverter. The output waveform is shown in Figure 4.27 below. For clarity, the BK signal, which is inverse of the SEL signal is omitted. When SEL goes low, D_0 and D_1 (corresponding to row 0 and row 1, respectively) go low for the conventional decoder without charge sharing. However, for the decoder with charge-sharing using the 6T_CS tri-state inverter, once SEL goes low and BK goes high, D_0 discharges to ~ 7.78 V. During this time window, D_1 also rises, and pre-charges to ~ 7.65 V. As the BK signal is on, that floating output stored when SEL can charge the following row. This is further demonstrated by the power statistics. The average current was $7.42 \mu A$ and $6.28 \mu A$, respectively, equating to a 15.31% power saving.

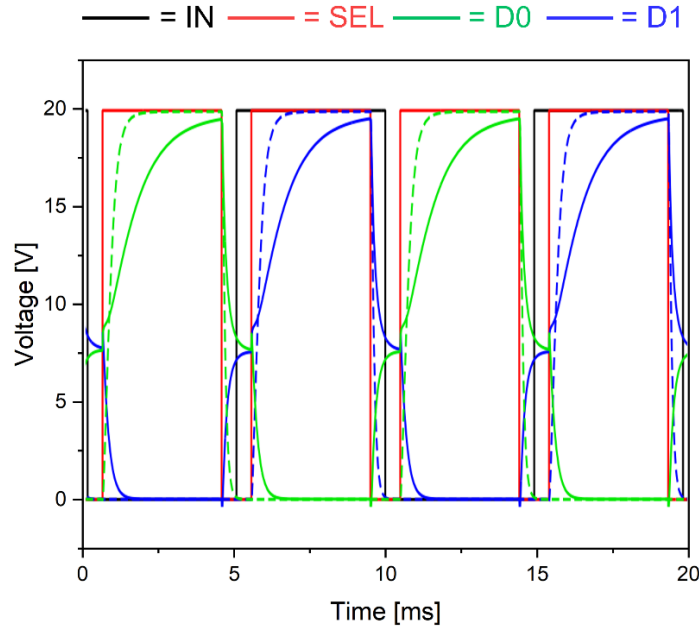


Figure 4.27: Transient output simulation for the 1-to-2 decoder with charge-sharing, utilizing the 6T_CS tri-state inverter. The conventional decoder without charge-sharing is shown in the dotted lines.

4.2.2 Design and operation of the 9 Transistor Tri-state Inverter for Charge-Sharing

The charge-sharing decoder utilizing the 6T_CS tri-state inverter presents a good proof-of-concept for low dynamic power row-driver circuits. However, the rise time and fall time are increased significantly, limiting its use case in display circuits. To further minimize the dynamic power consumption and improve rise-time/fall-time, a new tri-state gate was proposed. This tri-state gate uses 9 transistors

(denoted as 9T_CS). The circuit schematic along with its output waveform is shown in Figure 4.28. The transistor sizing is shown in Table 4.4.

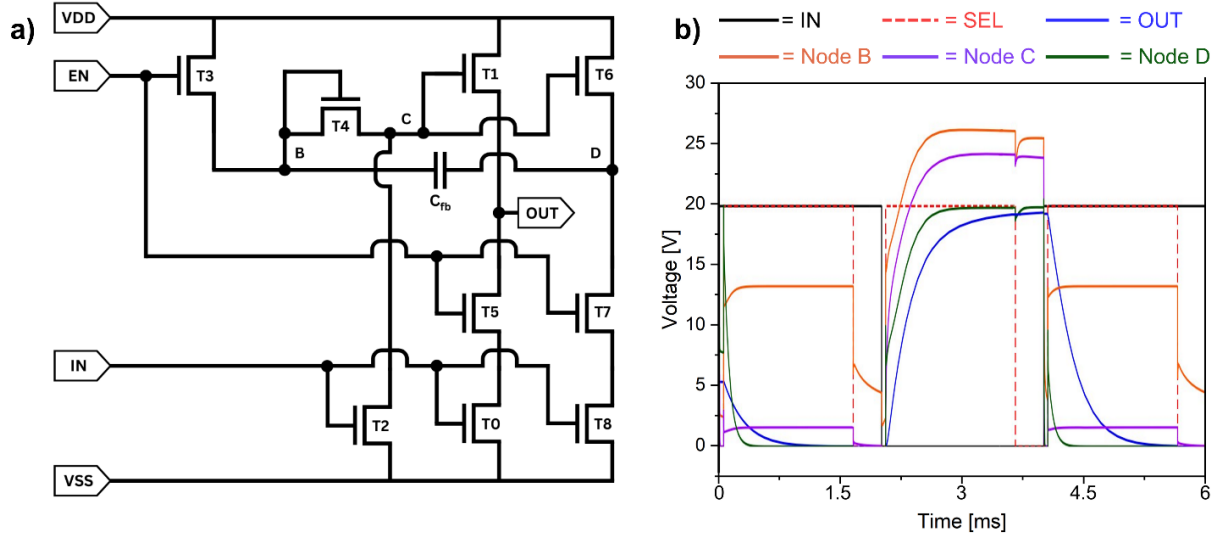


Figure 4.28: a) Device level schematic for the 9T_CS inverter and b) output waveform behaviour.

Table 4.4: W/L transistor sizing for the 9T_CS inverter

	T ₀	T ₁	T ₂	T ₃	T ₄
W/L ratio	100/20	200/20	100/20	200/20	40/20
	T ₅	T ₆	T ₇	T ₈	C _{fb}
	100/20	40/20	40/20	40/20	15.012pF

In the 6T_CS design, C_{fb} would be driving the output node, as well as driving the feedback path. In the 9T_CS design, C_{fb} is now just driving the feedback path, connecting to the new arm at node D. A new arm is added to this feedback path, with T₆ as the pull-up transistor, and T₇ and T₈ as the pull-down transistors. These transistors are kept at the minimum fabrication W/L ratio of 40/20 to minimize the contribution to the area footprint. Node C now drives the gates of T₁ and T₆. While this lowers the internal node B and C voltages by $\sim V_T$, the output is still able to achieve rail-to-rail swing. The new stage added helps boost the pre-charging of the subsequent rows, and this is demonstrated in the transient waveform shown in Figure 4.29.

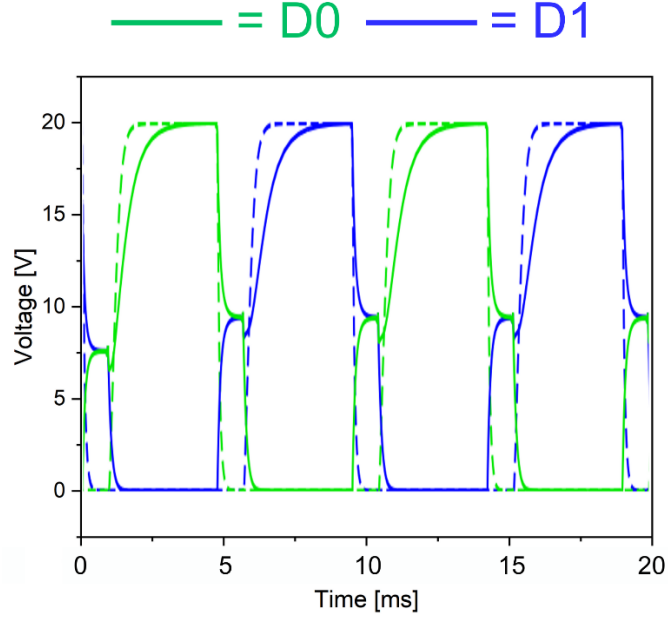


Figure 4.29: Transient output simulation for the 1-to-2 decoder with charge-sharing, utilizing the 9T_CS tri-state inverter. The conventional decoder without charge-sharing is shown in the dotted lines.

As expected, the simulated results follow a similar pattern to the charge-sharing decoder using the 6T_CS tri-state inverter. However, the main difference here is the rise-time/fall-time. This comes from the fact that output load is significantly reduced, as the feedback capacitor is not connected to output node. This also increases the pre-charge voltage during charge-sharing. The boost in pre-charge voltage further reduces the dynamic power consumption, and this is shown, as the average current reduces from $6.28 \mu\text{A}$ to $5.74 \mu\text{A}$, from the charge-sharing decoder using the 6T_CS tri-state inverter, to the one using the 9T_CS tri-state inverter, respectively. This equates to a 22.55% power saving, in comparison to the conventional decoder, showing a substantial improvement. For higher decoder architectures, the simulations and measurements will be done using the 9T_CS tri-state inverter. The W/L (in μm) of the 9T_CS tri-state inverter 1066/599, being 11.5% bigger and 8.3 % bigger in area footprint than 5T bootstrapped inverter, and the 6T_CS tri-state inverter, respectively. Despite the additional area, this trade-off is well worth the cost, considering the additional power saving demonstrated. Moreover, in a 3-to-8 row-decoder, the overall area only increases by $\sim 2\%$. The layout is shown in Figure 4.30.

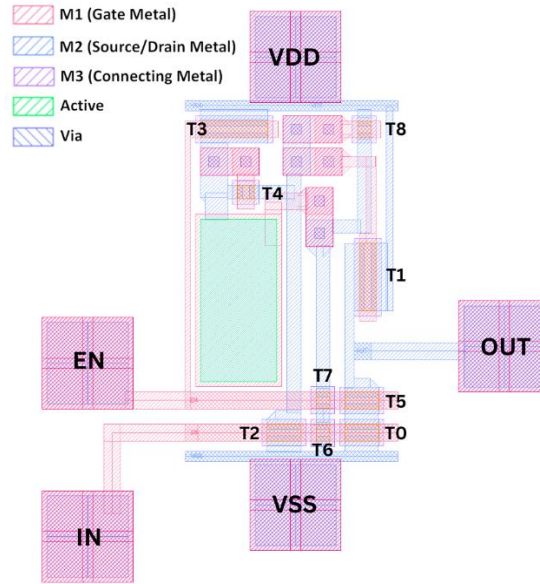


Figure 4.30: Measured output waveforms for the 1-to-2 decoder using the a) 5T inverter, b) 6T_CS inverter and c) 9T_CS inverter.

4.3 Simulated Results for the 3-to-8 Charge-Sharing Decoder

This charge-sharing behaviour can be extended to higher decoder systems, such as the 3-to-8 decoder. Figure 4.31 shows the gate-level schematic of the proposed 3-to-8 decoder circuit, replacing IC#3 (see Figure 1.2). In this design, a pre-decoder stage is implemented to reduce the 4-input NAND gate into 3-inputs instead. Additionally, instead of a singular BK switching transistor between row n and row $n+1$, two additional transistors are placed in series, being driven by the same inputs driving their respective output stage. These additional switching transistors are necessary, to ensure the desired charge-sharing behaviour. This circuit is designed, such that no additional external signals are required.

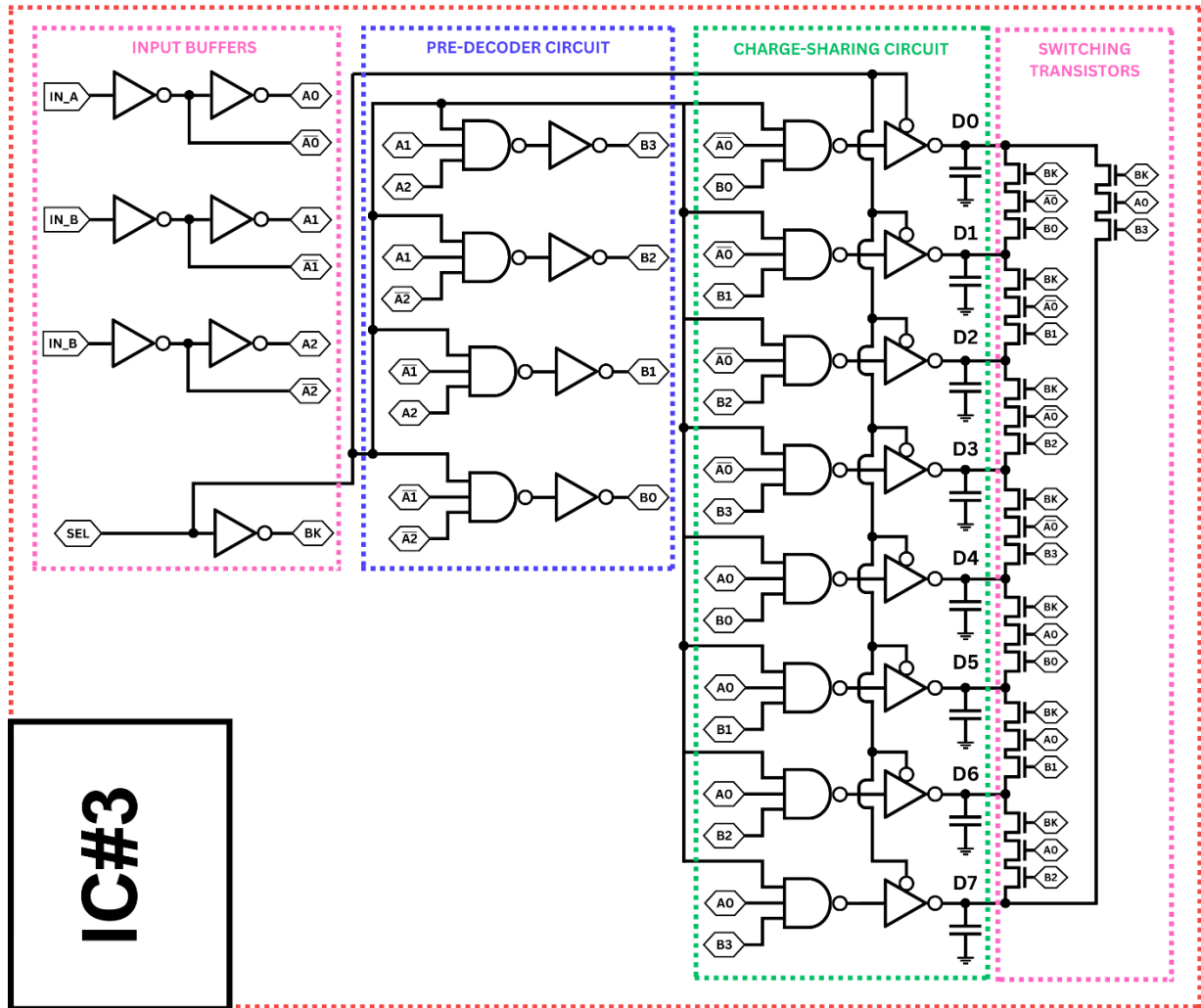


Figure 4.31: Gate-level schematic for the 3-to-8 charge-sharing decoder.

A transient simulation was performed once again, to observe the charge-sharing behaviour for the 3-to-8 decoder. Figure 4.32 shows the input signal timing, alongside the output waveform plotted with the SEL signal.

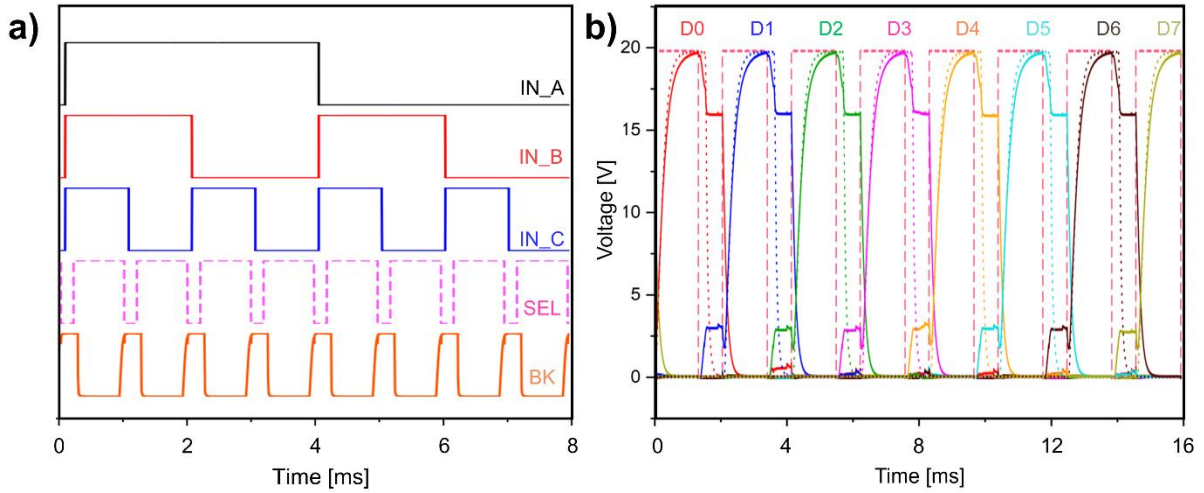


Figure 4.32: Transient output simulation for the 3-to-8 decoder with charge-sharing, utilizing the 9T_CS tri-state inverter. The conventional decoder without charge-sharing is shown in dotted lines.

As seen in the output waveform, Row n and row $n+1$ do not discharge and pre-charge to $\sim \frac{1}{2} V_{DD}$, in comparison to the 1-to-2 decoder. Instead, it would discharge and pre-charge to ~ 16.2 V and ~ 3.5 V, before discharging and charging to V_{SS} and V_{DD} , respectively. Nonetheless, there is still a degree of dynamic power saving present. While the pre-charging phase is reduced, there is still power reduction from the static leakage paths being less present during the tri-stating operation. With more charge-sharing drivers present in the overall circuit, the power saving increased from 22.55% to 31.12%. This is further exemplified, by the power trend, from 1-to-2 to 5-to-32, tabulated in Table 4.5.

Table 4.5: Simulated power analysis for decoders with and without charge-sharing

Decoder Size	Current (μA)		Power (μW)		Power Saving (%)
	5T	9T_CS	5T	9T_CS	
1-to-2	7.42	5.74	148.3	114.9	22.55
2-to-4	9.95	7.44	199.1	148.7	25.31
3-to-8	18.96	13.06	379.2	261.2	31.12
4-to-16	37.30	23.18	746.0	463.6	37.86
5-to-32	75.10	42.37	1502	847.4	43.58

4.4 Measurement Data Extraction and Results

The following subsections will go into the measurement results and the analysis. To start off, a device model is needed. A-Si:H TFTs are fabricated onto a glass substrate, using the 5-mask industrial standard model, at a maximum process temperature of 170°C. To start off, 70nm of Cr gate metal is deposited and patterned at room temperature. This is followed by a tri-layer deposition of a-SiN_x:H gate dielectric, a-Si:H channel and n⁺ a-Si:H source/drain contacts, with thicknesses of 350nm, 200nm and 40nm, respectively. These layers were deposited via PECVD at 170°C and at 13.5 MHz. A second mask is utilized to pattern the active area via dry-etching, to allow the deposition and patterning of the Al and Cr source-drain metal contacts. The thicknesses of these layers are 80 nm and 20 nm, respectively. The n⁺ a-SiN_x:H layer is then back-etched via dry-etching, to make room for the channel region. 500nm of a-SiN_x:H is then deposited across the substrate, followed by the patterning of the vias for the source/drain/gate contacts. To conclude the fabrication process, a 1 μm Al-contact is deposited at room temperature and patterned, yielding the a-Si:H TFT. The cross-sectional fabrication model is shown in Figure 4.33 [41], [51].

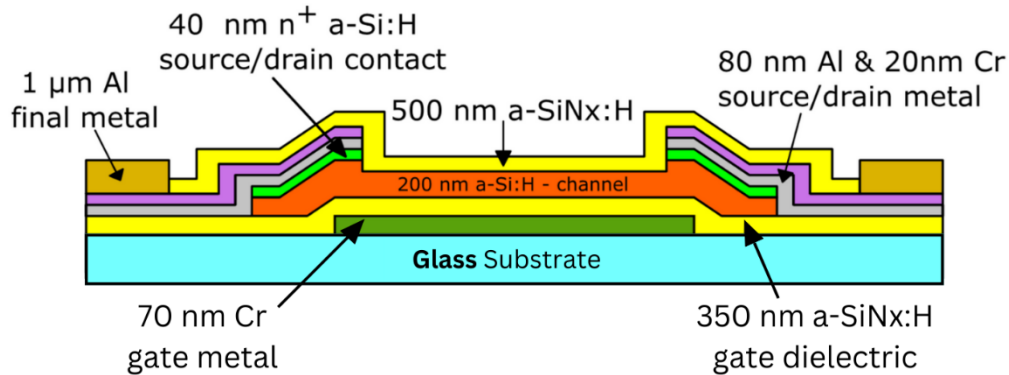


Figure 4.33: Cross-sectional fabrication model for a-Si:H TFTs fabricated onto glass substrate.

Circuit simulations and layouts are done through Cadence Virtuoso, using the level-61 a-Si:H TFT model. The signal generation is done by an Arduino Mega 2560 Microcontroller. These input signals are fed into TLE2144 non-inverting amplifiers to raise the input signals to 20 V. The Keithley source meters (model 2400 and 6430) are used as the power supply. These amplified signals are then fed into the input probes of the test-circuit, and the output probes are connected to TLE2144 unity-gain amplifiers. The output signals are then extracted by the Tektronix MDO3104 Mixed Domain Oscilloscope and are then saved for analysis. The testing setup schematic, along with the physical test bench, is shown in Figure 4.34.

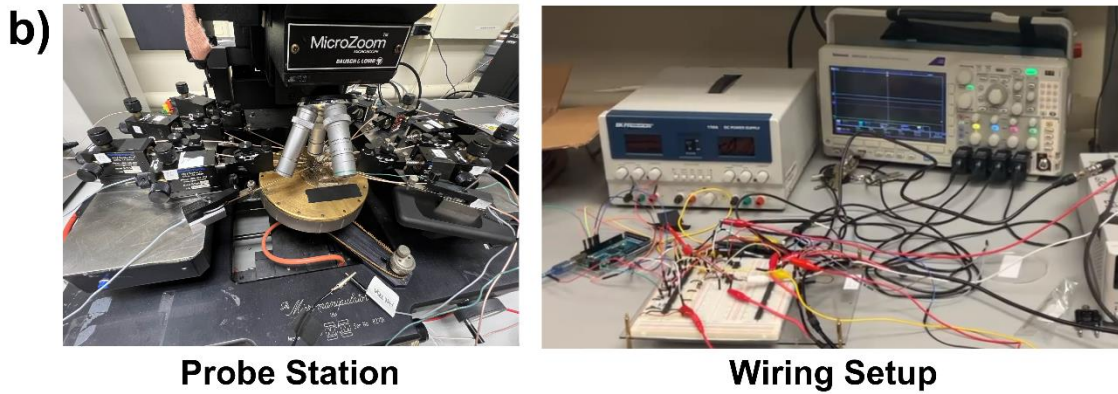
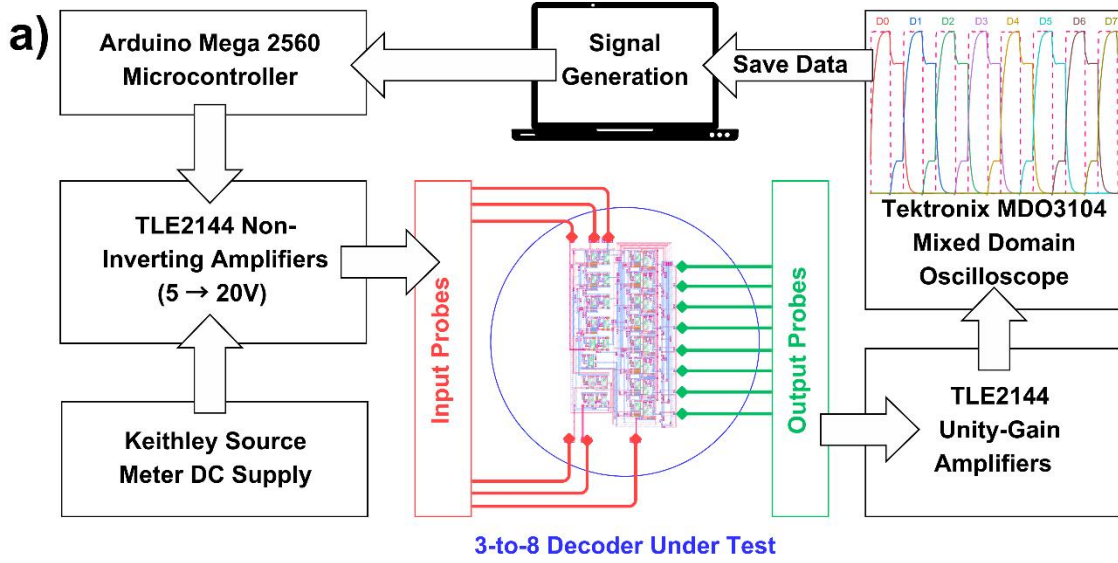


Figure 4.34: a) Testing setup and data extraction schematic and b) Physical probe station and wiring setup.

A DC analysis was performed on isolated a-Si:H TFTs to measure the output and transfer curves, and the curves are shown in Fig. 4.35. As seen in fig. 4.35, the output curves for the physical and simulated curves follow a similar pattern, with the slight difference being the simulated curves exhibiting a higher channel length model, especially once V_{Ds} is greater than or equal to 10 V. Likewise, the transfer curves for the simulated and physical cases seem to align with each other very closely. The field effect mobility, sub-threshold slope and V_{TH} was extracted from this model and was found to be $1.05 \text{ cm}^2/\text{Vs}$, 0.62 V/decade and 3.1 V , being close with the theoretical model.

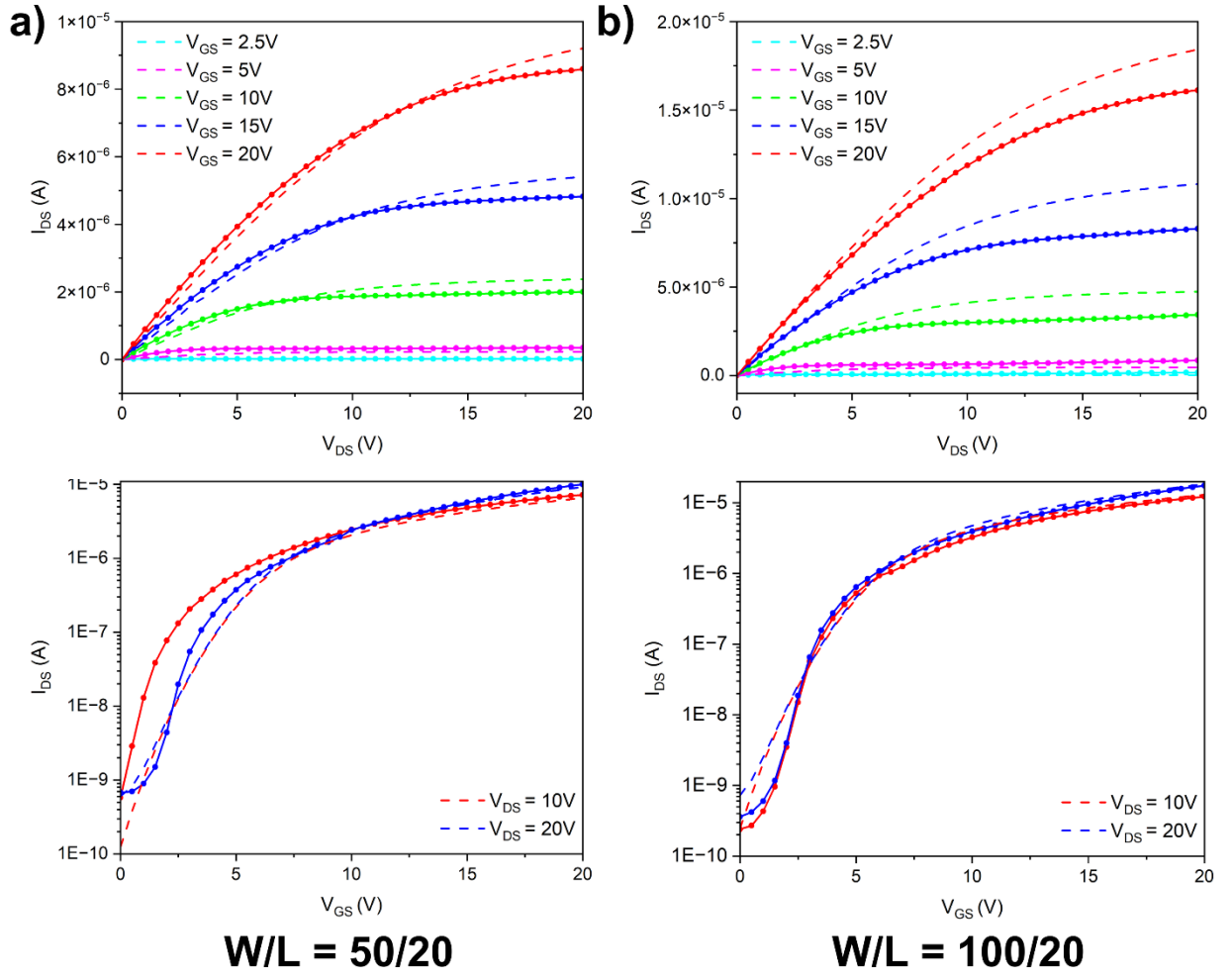


Figure 4.35: Output and transfer curves for a-Si:H TFTs with a) $W/L = 50/20$ and b) $W/L = 100/20$. The dots indicate measured, and the dashed lines indicate simulated results.

To validate the charge-sharing behaviour, measurements were done on the 1-to-2 decoder and the 3-to-8 decoder. The charge-sharing decoder, using the 6T_CS and 9T_CS tri-state inverter is compared to the decoder using the 5T bootstrapped inverter. The measured waveforms are shown in Figure 4.36.

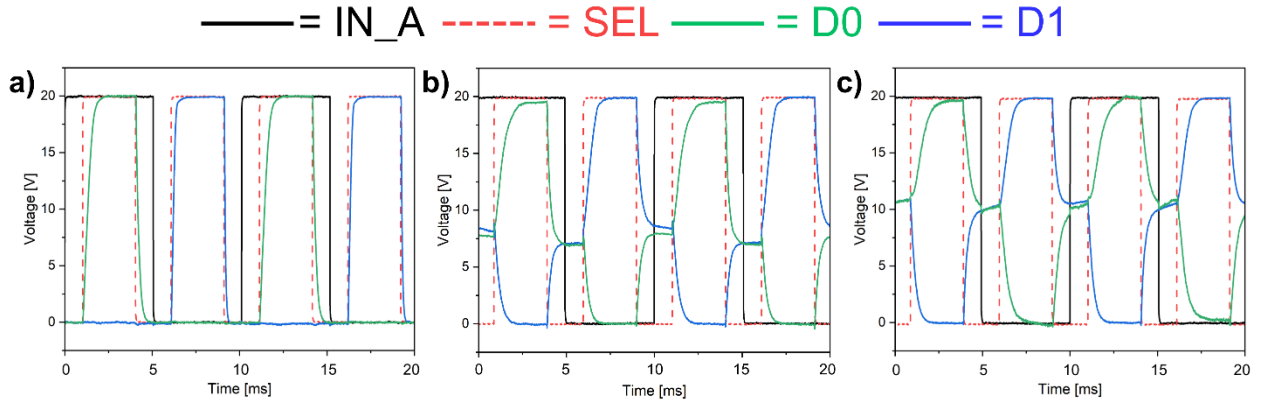


Figure 4.36: Measured output waveforms for the 1-to-2 decoder using the a) 5T inverter, b) 6T_CS inverter and c) 9T_CS inverter.

The measurement results show the proposed charge-sharing behavior. The decoder using the 5T bootstrapped inverter behaves as expected. Once SEL goes low, the outputs follow the same behaviour. In the case of the decoder using the 6T_CS, once SEL goes low, D₀ and D₁ (corresponding to row 0 and row 1, respectively) discharge and pre-charge to ~ 6.9 V, respectively. However, in the following stage, there is a slight mismatch in the discharge and pre-charge voltage, with D₁ and D₀ discharging and pre-charging to ~ 8.3 V and ~ 7.9 V, respectively. Regardless, they're still in a comparable range, and there is still a significant amount of dynamic power saving present. The dynamic power saving increases for the decoder utilizing the 9T_CS design, pre-charging and discharging to ~ 10.1 V, for all cycles. This is shown through the power analysis, with the current for the 5T, 6T_CS and 9T_CS being $7.66 \mu\text{A}$, $6.7 \mu\text{A}$ and $6.12 \mu\text{A}$, respectively. This equates to a measured power saving of 12.53% and 20.10%, for the 6T_CS design and 9T_CS design, respectively. These results are in similar range to the simulated results.

Likewise, comparable results are shown for the 3-to-8 decoder using the 9T_CS. Figure 4.37 shows the measured results for the 3-to-8 decoder. The charge-sharing decoder, using the 9T_CS tri-state inverter is compared to the decoder using the 5T bootstrapped inverter. Like the 1-to-2 decoder without charge-sharing present, it behaves as the conventional decoder. On the other hand, for the decoder with charge-sharing in Figure 4.12b, when SEL goes low, row n would discharge to ~ 16.2 V and row $n+1$ would pre-charge to ~ 3.8 V. There was still significant charge-sharing behaviour present, and there was a significant reduction in power consumption. The current was found to be $20.98 \mu\text{A}$ and $15.54 \mu\text{A}$, respectively, equating to a measured power saving of 25.93%. The use of 9T_CS tri-state inverters with charge-sharing mechanism in the circuit help reduce the overall power consumption. Table 4.6

summarizes the power consumption for the decoders using the 5T bootstrapped inverter and the 9T_CS tri-stating inverter. For all cases, the charge-sharing decoder, utilizing the 9T_CS design saved significant power, compared to the conventional state-of-the-art decoder using the 5T bootstrapped inverter. Discrepancies in the simulated and measured results are a result of the parasitic capacitances of the external physical testbench, resulting in the measured circuits showing a slightly lower power consumption than the simulated results. These results are still in comparable range, showing a promising result.

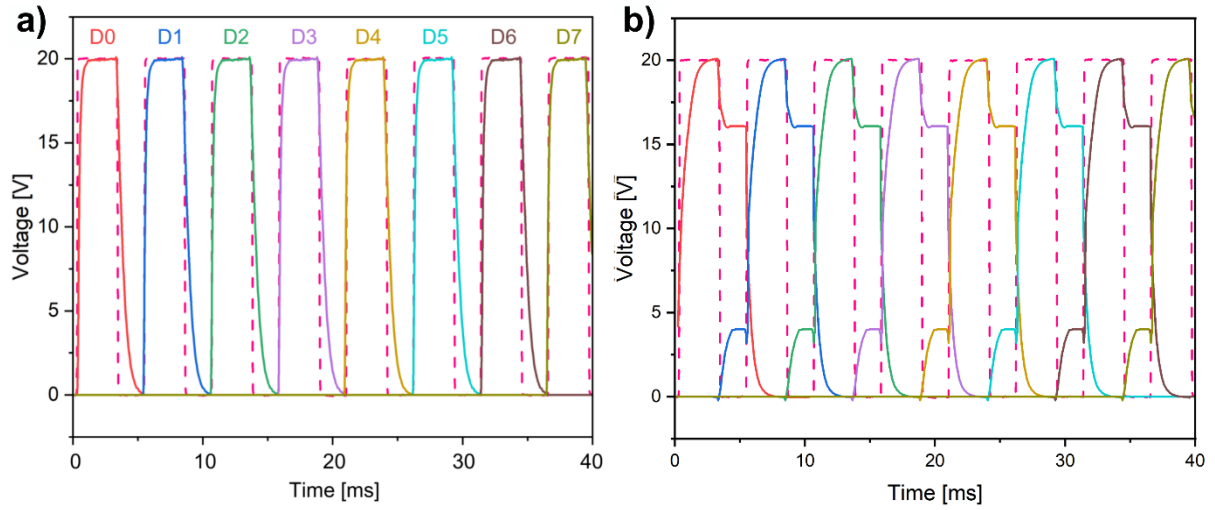


Figure 4.37: Measured output waveforms for the 3-to-8 decoder using the a) 5T inverter, b) 9T_CS inverter.

Table 4.6: Comparative power analysis of decoders with (9T_CS) and without charge-sharing (5T).

Decoder Size	Power (μW)				Power Saving (%)	
	Simulated		Measured		Simulated	Measured
	5T	9T_CS	5T	9T_CS	5T	9T_CS
1-to-2	148.3	114.9	153.2	122.4	22.55%	20.10%
3-to-8	379.2	261.2	419.6	310.8	31.12%	25.93%

4.5 Summary of Chapter 4

In this chapter, simulation results validated the performance of the 6T_CS and 9T_CS tri-state inverter. Both tri-state inverters helped the decoder achieve charge-sharing. The implementation of switching transistors in the decoder circuit helped ensure the proper charge-sharing timing, showing a proper cyclic pattern. With the additional stage added to the 9T_CS tri-state inverter, the decoder circuit was able to reduce the dynamic power consumption to a further extent. Additionally, the power saving was shown to improve for bigger decoders.

Chapter 5: Conclusions and Future Work

5.1 Conclusions

To fully realize a high-resolution fully integrated display backplane using unipolar TFTs, it is important to find viable alternatives to replace the off-panel peripheral CMOS control circuit. It is important that the proposed alternative can realize CMOS-like logic, reduce power consumption, and have a high fabrication yield.

The major contribution presented in this thesis is a low-power address logic row-decoder circuit with charge-sharing behaviour, using unipolar amorphous silicon TFTs. This work tackles the issue of the bonding pad size, by replacing bonding pads interfacing the peripheral circuit with the pixel array. This work is an extension on the state-of-the-art bootstrapped 5T inverter, which was able to achieve CMOS-like full output swing. In this work, additional circuit design was implemented to the 5T inverter, to realize full-swing tri-stating logic. The simulated results showed that the proposed 9T_CS inverter was able to maintain a floating state, which can be utilized for charge-sharing. In this decoder, the conventional final output driver is replaced by the 9T_CS tri-state inverter. The decoder was also re-designed, to connect the rows between each other and enable charge-sharing. The simulated and measured results show that the newly designed decoder was able to reduce the dynamic power consumption through charge-sharing. The 9T_CS tri-state inverter, which was able to store the floating voltage from its tri-stating behaviour, and this floating voltage was able to pre-charge the following row line, before fully discharging. Additionally, the switching transistors added to the decoder circuit helped maintain that charge sharing timing behaviour. This was all done, without adding any external signals to the conventional row-decoder. This work has been demonstrated for a 1-to-2 and 3-to-8 scheme. The proposed scheme reduces the total power consumption of row driver in displays by 25.93% compared to state-of-the-art design.

5.2 Future Work

This work presents a good framework for integrating the peripheral circuit row-driving component onto the display backplane. However, additional work needs to be done to realize full integration of all components.

For the 9T_CS tri-state inverter, future iterations should focus on minimizing the device footprint. In CMOS logic, the inverter requires only 2 transistors, while a tri-state inverter requires 4. Currently,

in unipolar TFT logic, there are 5 transistors + a feedback capacitor and 9 transistors + a feedback capacitor for the state-of-the-art bootstrapped inverter and the tri-state inverter, respectively. Minimizing the device footprint will not only reduce the overall area layout, but will also increase the yield, especially for large-scale fabrication, like monitor displays.

Building upon this work, additional TFT logic can be implemented for areas such as charge-sharing in the data-driving component, conversion of data and implementing memory to hold and shift the data whenever necessary. Research into these topics will help fully realize a smart display, using unipolar TFT logic. Additionally, this will help lower the fabrication costs.

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