

Low-noise Amplifier for Neural Recording

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

With a combination of engineering approaches and neurophysiological knowledge of the central nervous system, a new generation of medical devices is being developed to link groups of neurons with microelectronic systems. By doing this, researchers are acquiring fundamental knowledge of the mechanisms of disease and innovating treatments for disabilities in patients who have a failure of communication along neural pathways.

A low-noise and low-power analog front-end circuit is one of the primary requirements for neural recording. The main function for the front-end amplifier is to provide gain over the bandwidth of neural signals and to reject undesired frequency components. The chip developed in this thesis is a field-programmable analog front-end amplifier consisting of 16 programmable channels with tunable frequency response. A capacitively coupled two-stage amplifier is used. The first-stage amplifier is a Low-Noise Amplifier (LNA), as it directly interfaces with the neural recording micro-electrodes; the second stage is a high gain and high swing amplifier. A MOS resistor in the feedback path is used to get tunable low-cut-off frequency and reject the dc offset voltage.

Our design builds upon previous recording chips designed by two former graduate students in our lab. In our design, the circuits are optimized for low noise. Our simulations show the recording channel has a gain of 77.9 dB and input-referred noise of $6.95 \mu\text{V}_{rms}$ (Root-Mean-Square voltage) over 750 Hz to 6.9 kHz. The chip is fabricated in AMS 0.35 μm CMOS technology for a total die area of $3 \times 3 \text{ mm}^2$ and Total Power Dissipation (TPD) of 2.9 mW. To verify the functionality and adherence to the design specifications it will be tested on Printed-Circuit-Board.

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Dedication

This is dedicated to my husband and my son Daksh with lots of love.

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Nomenclature

- ADC** Analog-to-Digital Converter. 18
- BMI** Brain Machine Interface. 2
- BMR** Beta Multiplier Reference. 57
- CMFB** Common Mode Feedback. 30, 31
- CMRR** Common Mode Rejection Ratio. 24
- CNS** Central Nervous System. 1
- DAC** Digital-to-Analog Converter. 23
- HCF** High Cut-off Frequency. 52
- LCF** Low Cut-off Frequency. 52
- LNA** Low-Noise Amplifier. iii, 22
- PSRR** Power Supply Rejection Ratio. 24
- TPD** Total Power Dissipation. iii

Chapter 1

Introduction

1.1 Motivation and Application

The human brain and its function has always been a topic of great curiosity for researchers. Neuroscientists strive to understand the mechanisms, i.e., the electrophysiological activities in the nervous system that correspond to, and cause, specific physiological actions.

In recent years, the pace of research in the field of neuroscience has accelerated drastically. With a combination of engineering and neurophysiological knowledge of the nervous system, a new generation of medical devices is being developed to functionally link large groups of neurons in the Central Nervous System (CNS) with human-made recording systems [3]. By a direct interaction with the CNS, researchers are acquiring new scientific knowledge of the mechanisms of disease and innovating treatments for disabilities in patients who have a failure of communication between neural structures (or output to the

external environment) due to illness, stroke, or injury. The idea to build a direct functional interface between the brain and artificial devices has led to the establishment of a new area of research in the field of neuroscience, known as Brain Machine Interface (BMI). Figure 1.1 shows the block diagram of Brain-Machine-Interface.

BMIs can provide solutions for disabilities like epilepsy and Parkinson's disease. Epilepsy is a common brain disorder characterized by recurrent seizures. The invention of several neural recording systems has opened up avenues to make a significant change in the lives of the epilepsy patients [4]. Parkinson's disease is a degenerative disorder of the central nervous system mainly affecting the motor system. Deep brain stimulation is one of the treatment methods for Parkinson's disease. In this method, tiny electrodes are implanted in some specific part of the brain. Stimulating this part of brain often greatly reduces involuntary movements and tremors. This is the area where human-machine interfacing plays a great role in our health system. Developing a brain-machine-interface requires an accurate understanding of neurons and their performance. For the same, we should record and analyze neurons in their normal and excited modes. An understanding on the neural functioning helps us to determine a proper pattern for stimulating the brain [5]. This will also equip scientists to restore neurons functions in parts of the nervous system damaged by different diseases or paralysis.

Scientists performed observations in animal and human neural network and they detected and recorded the action potentials of many neurons corresponding to motor control to develop analytical models that predict limb movements in real time. Some research groups have created prosthetic limbs that can duplicate the natural movement of human body parts [6]. Unlike passive artificial versions, these prosthetic limbs have the capability

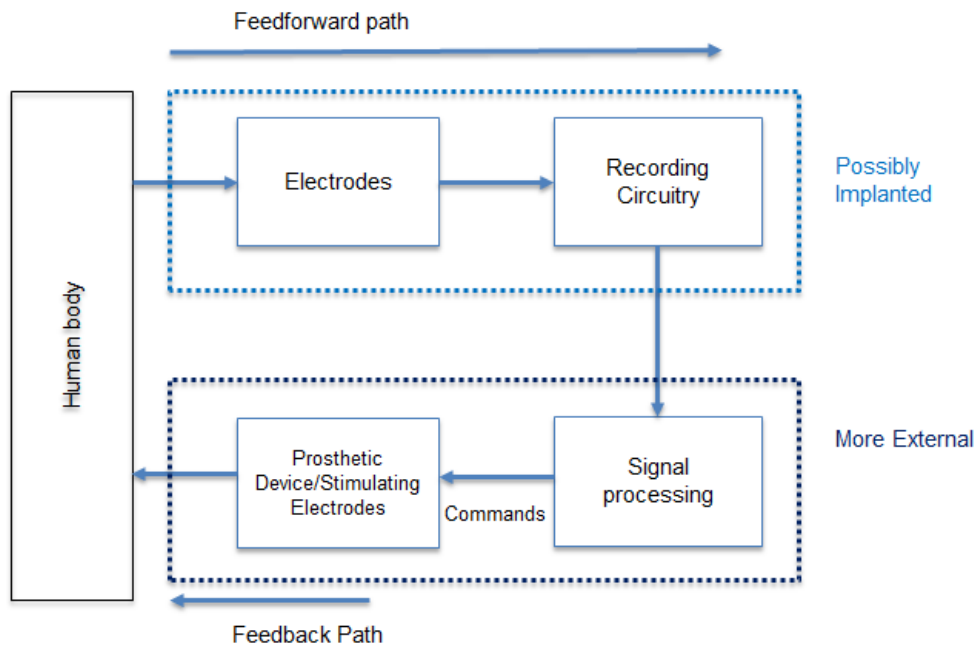


Figure 1.1: Block diagram of a conceptual Brain Machine Interface.

of moving independently and out of sync with its user’s movements. Cochlear implants and retinal stimulators [7] are excellent examples of successful neural interfacing technologies that have reached widespread clinical applications [8]. Future neuroprostheses are expected to be seamlessly integrated with the human body as much as possible and to use the most advanced developments in material science, data computing, electrical engineering and robotics.

State-of-the-art neural interfacing microsystems capable of continuously monitoring large groups of neurons are being actively researched by leveraging recent advances in neurosciences, microelectronics, communications, microfabrication, packaging and miniaturization. Such microsystems are intended to directly tap into the source of voluntary control, the CNS, to feed prosthetic devices restoring or replacing sensory, motor, or cog-

nitive functions. One of the key components in these microsystems is known as the analog front-end circuitry. After probing the neural signal using microelectrodes, these signals are fed into this block. This block filters out undesired dc and high frequency components and amplifies the signals from an order of a few micro-volts to a range which is suitable for subsequent circuitry.

Though many prosthetic devices have been successfully implemented in recent years, there still remain many issues and challenges concerned with the failure to meet the 'ideal' requirements of a satisfactory prosthetic. It starts from finding the right material for the electrodes which are bio-compatible with the human tissues, long lasting wireless charging for the neural implanted devices, to making a prosthetic device which is easy to control, comfortable to wear, and cosmetically pleasing.

1.2 Objective

This neural recording project is a component of an ongoing collaboration with neuroscientists from the Faculty of Medicine at the University of Alberta. They are our clinical partners to do live testing of our neural recording chips. The chip developed in this thesis, called AF7 is a field programmable analog front end amplifier for a neural recording system and it consists of 16 programmable channels whose frequency response can be tuned to take care of the process variations of the chip into account.

There was a previous generation of this chip (AF5) implemented by previous students in our research group in AMS 0.35 μm CMOS technology. The fabricated chip was tested

on a custom PCB; while the chip was capable of recording, it was found to be too noisy for successful implantation.

The goal of this thesis is to find the design gaps and issues with the previous generation chip and solve these issues with suitable architecture and design decisions. The previous generation chip used 4 blocks of 4 different channel architectures. The aim is to study the trade-off of the various channel architectures, with a consideration of low input-referred noise, bandwidth and stability. The target is to design a functional analog front end amplifier for neural recording system, aligned with the project specifications.

To be consistent, our chip is fabricated in AMS 0.35 μm CMOS technology. The AMS 0.35 μm process technology has been selected for the fabrication of the chip, as it is very stable and well tested fabrication process technology with minimal fabrication issues. It has high yield and is inexpensive.

1.3 Organization

The organization for rest of the thesis is as follows.

Chapter 2 presents the background information on neuron functionality, their characteristics and existing challenges for a highly efficient and feasible neural recording device. The different recording techniques and the specifications of neural recording systems are described further. A review of the works of various research groups involved in the design of neural recording systems is also covered.

Channel architectures are analyzed with respect to input-referred noise, power con-

sumption and signal amplification factor, to find the best choice for the implementation of the recording channels in Chapter 3. The selected channel architecture used for implementing the neural recording system is discussed with its design details.

Chapter 4 includes the simulation results for the front-end neural recording system.

Chapter 5 gives a summary of the work done in the thesis. Conclusions and suggested future research problems are outlined.

Chapter 2

Background

2.1 Characteristics of Neural signals

The neuron is the basic working unit of the brain. It is a specialized cell designed to transmit information to other nerve cells, muscles, or gland cells. Neurons have a cell body (soma), an axon, and dendrites. There are over 10 billion neurons in the human brain [9]. An ion channel is formed in the neuron cell membranes with ions such as sodium, potassium, chloride, and calcium. To develop a neural recording system, it is important to have a basic understanding of neuron functioning. This chapter provides an insight in functioning of neurons.

2.1.1 Resting Membrane Potential

When a neuron is not sending a signal, it is considered to be 'at rest'. At this time the potential inside of the neuron is negative relative to the outside (approximately -70 mV). This potential is developed because the membrane that surrounds the neurons is semi-permeable, which allows some ions to pass through and blocks the passage of other ions. The distribution of various ions is very different in intracellular and extracellular fluids.

Table 2.1 shows the intracellular and extracellular concentration of these ions during rest [1]. Concentrations of K^+ ions are mostly inside the cell (intracellular), and Na^+ ions are mostly concentrated outside the cell (extracellular). There also exist other ions such as Ca^{2+} and Cl^- , in lower concentrations.

The concentration gradients for Na^+ and K^+ are set up by the active transport of Na^+ and K^+ by an Na^+/K^+ ATPase known as the Na^+/K^+ pump. ATPase pumps three Na^+ ions out of every two K^+ ions it puts in, finally when all these forces balance out, and the difference in the voltage between the inside and outside of the neuron is developed.

At rest, a membrane is slightly permeable to K^+ and almost impermeable to Na^+ , which means that K^+ will diffuse due to the concentration gradient and an electrical potential develops, with an excess of negative charge inside the neuron. The negative charge inside the neuron creates an electrical potential gradient which tends to pull positively charged ions into the cell. As the membrane is impermeable to Na^+ , the only ion that can be attracted is K^+ . The net flow of each ion across the membrane is zero at a particular voltage. At this voltage, the concentration gradient and electrical potential gradient of the ion reach equilibrium, and this voltage is called, equilibrium potential [1]. The voltage is

calculated using Nernst's equation (2.1).

$$V_m = (RT/ZF)\log_e[C_o]/[C_i] \quad (2.1)$$

Where V_m is the voltage across the membrane ($V_{inside\ membrane} - V_{outside\ membrane}$), R is the gas constant, F is Faradays constant, T is absolute temperature in Kelvins, Z is valency of the ion. $[C_o]$ and $[C_i]$ are the external and internal concentrations of the ion, respectively.

Table 2.1: Distribution of ions around neural cell membrane [1]

Ions	Intracellular Concentration/(mM)	Extracellular Concentration/(mM)
Na ⁺	12	145
K ⁺	139	4
Cl ⁻	4	120
Large anions(A ⁻)	140	-
Ca ²⁺	< 0.0002	1.8

2.1.2 Action Potential

Neurons are excitable cells and they can generate and conduct action potentials. This is the one of the principal characteristics of neurons. Action potentials are rapid changes in the potential difference across the plasma membrane. The ability of neurons to generate action potentials is due to the presence of ion channels in their plasma membrane that respond to changes in the membrane potential.

Figure 2.1 illustrates the different phases of an action potential which are due to the opening of two types of voltage sensitive channel, which are Na⁺ and K⁺ selective. The

different properties of these two types of channels determine the characteristics of the action potential [1]. The shape of the neuron membrane potentials remains fairly constant for all the neurons as shown in Figure 2.1.

When a neuron is sufficiently stimulated, the Na^+ ion channels open and diffuse Na^+ ions through the cell, causing increased potential (depolarization). The potential required for opening K^+ ions is larger than that needed for Na^+ ions. Therefore, when the membrane potential is high enough, the K^+ channels open. The Na^+ channels close after 1ms. These two incidents produce repolarization, which decreases the membrane potential toward the resting potential level. The K^+ ion channel will be closed for a period after that of Na^+ , resulting in an undershoot. Eventually, the membrane potential reaches to resting state with the help of ion pumps [10].

2.2 Neural Recording Methods

The electro-physiological responses of the neurons can be measured using high-impedance microelectrode system penetrating 1-2 mm in the cortex [11]. When a neuron generates an action-potential (AP), the signal propagates down the neuron as a current which flows in and out of the cell. This method provides the highest degree of spatial specificity for the neural signals and it was most used method for measuring the action-potential through arrays of micro-electrodes earlier.

The bioelectrical activity, transmitted along the axon of a neuron can either be measured intracellularly or extracellularly. Intracellular APs can be measured by penetrating

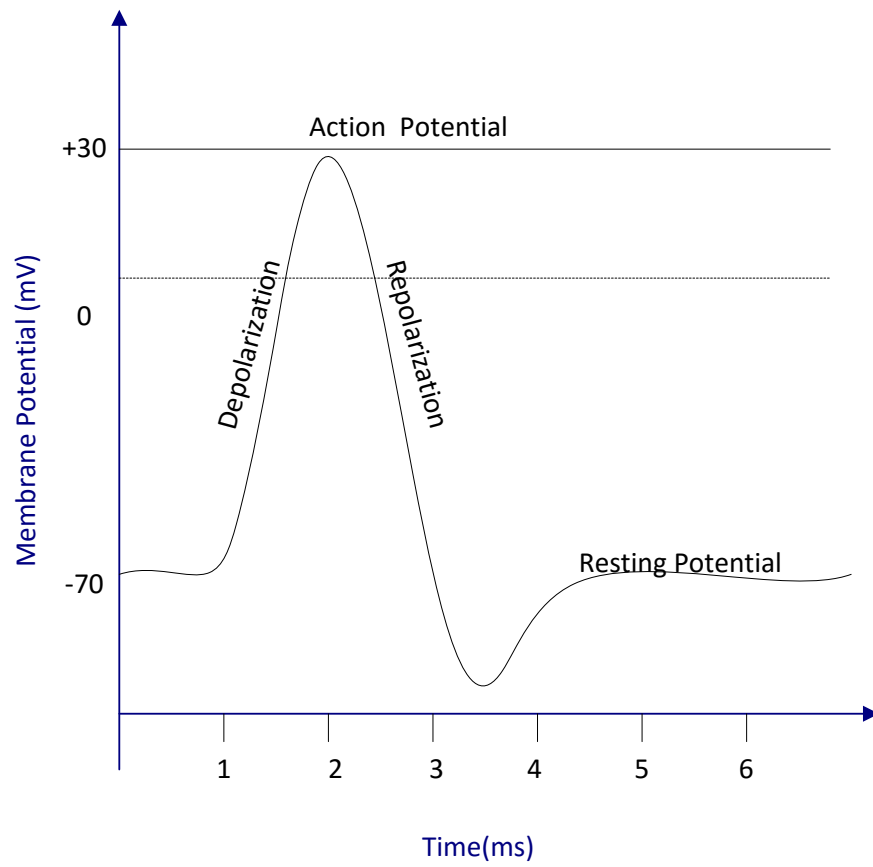


Figure 2.1: The neuron membrane potentials.

the membrane of a neuron with a sharp glass micropipette. This causes the death of the cell within a few hours after the recordings [8], so it is not recommended for chronic implants. In extracellular recording method, a micro-electrode with a sufficiently small tip [12], is placed adjacent to the neuron. In this method, the neuron action potential or spike is much smaller than that obtained with intracellular recording. Intracellular APs have amplitudes in the range of 70 mV_{pp} (peak-to-peak voltage) [13], whereas extracellular APs have weak amplitudes ranging from 50 μ V_{pp} to 500 μ V_{pp} with a bandwidth of 100 Hz to 6 kHz, depending on the distance between the active neuron and the recording electrodes [14].

The summed electrical activity from many neurons can be recorded through lower impedance electrodes. The electrodes can be placed within the cortex (i.e., called Local Field Potential or LFP), just above the cortex (i.e., called subdural electrocorticography or ECoG), above the protective dura (i.e., called epidural ECoG), above the skull (subdermal) or above the skin (i.e., called electroencephalography or EEG) [15]. Local field potential (LFP) consists of lower-frequency neural waveforms (mHz to 200 Hz) having amplitudes ranging from 500 μ V_{pp} to 5 mV_{pp}. LFPs are also recorded using extracellular microelectrodes. Extracellular neural signals reduce in amplitude in proportion of 1/distance².

An EEG is a non-invasive method but ECoG is invasive as the electrode is implanted inside the skull yet outside the brain. A method is called invasive when the neuron activity is recorded directly from the cortex under the skull. Such methods require surgery and provide high spatial and time resolution at the same time. The LFP method is preferred to record the activity of a group of neurons located within millimeters while ECoGs and EEGs collect the neural signals over much larger areas, such as several square centimeters

at the cortical surface and scalp, respectively [16].

Initially, recording of the neural signals was limited to a single site, but during 1950s multi-electrode arrays were used to observe the simultaneous activity of many neurons in the brain. By observing the action potentials, or spikes, of many neurons in a localized region of the brain it is possible to gather enough information for that. As a result of improvements in the electronics and technology, the data processing speed has grown exponentially, which has enabled tremendous growth in the number of simultaneously recorded single neurons.

2.3 Characteristics and Challenges for Neural Recording Systems

Neural data is recorded from implanted multi-electrode arrays using bundles of fine wires and head-mounted connectors; then it is amplified and processed further. Chronically implanted multi-electrode arrays offer the best compromise between safety, recording longevity and neuronal yield required to operate BMIs. It works well in experimental settings, but many significant improvements are required before it becomes fully applicable for long-term (months to years) chronic clinical applications in humans.

2.3.1 Biocompatibility

Biological compatibility with human body is a big challenge for neural implants. Devices for neural recording and stimulation interact with neural tissues with different degrees of

precision and invasiveness. Neural recording and stimulation devices have generally been fabricated out of hard materials like silica, silicon or metals [17]. The mismatch in the stiffness of materials of the neuron and recording electrode contributes to tissue damage and decrease in recording quality. Also, the probe insertion itself produces a certain amount of initial damage. The implants are treated as foreign substance in the body so its very important to design and develop implants which are bio-compatible to the human tissues.

2.3.2 Wireless Operation and Power Supply

Another critical requirement for implantable recording devices is to replace the hardwired connections with a wireless link to eliminate cable tethering and risks of infection. Fully wireless implantable neural recording devices lower the risk of infection and patients have more freedom of movement and much better aesthetics.

A wire line supply source in implantable neural recording devices makes the tissues highly prone to infections. Rechargeable batteries are seen as a promising source of energy. But the power must be delivered wirelessly across the skin through an inductive link formed by a pair of coils. Inductive coupling is among the safest methods, researched so far, to power up implants as it avoids wires [8]. Although maximizing wireless power transfer efficiency, to get a small physical battery size with a long life is still a challenge.

2.3.3 Power Consumption

The state-of-the-art multi-channel neural recording systems produce large quantities of continuously streaming data that must be transmitted for amplification and further pro-

cessing, yet the power dissipation of the small implanted devices must be strictly limited. Low power operation (<100 mW) is essential for any implanted devices to prevent excessive tissue heating that can kill neuron cells [18]. A heat flux of only 80 mW/cm² can cause necrosis in muscle tissue [19], so for small chronic implants, power dissipation should not exceed a few hundred milliwatts [9]. Power scheduling mechanisms are researched extensively to decrease the power consumption in dense implantable microsystems featuring power hungry modules such as low-noise sensory circuits, data converters or data transmitters [8].

2.3.4 Noise Immunity and Form Factor

The recorded neural signals are very small in amplitude, typically $\sim 10\mu\text{V}$ to $500\mu\text{V}$. External noise and interfering signals easily couple to the wires conveying these weak neural signals, so it is very critical that the interfaces in the neural recording systems for example analog front-end should be designed to have a very low input-referred noise. Also the implantable neural recording systems should be small in dimension so that it can be easy to implant them in the body.

2.4 History and State-of-the-Art Neural Recording Systems

The experimental setups to study the central nervous system at the cellular level started way back in the 1950s. Around sixty years ago, Hodgkin and Huxley [20] performed

intracellular recordings using glass capillary electrodes filled with seawater to characterize the axons of the giant squid. These experiments built an understanding about the precise modeling of action potentials generated by neurons [8].

During the 1950s and the 1960s, Mountcastle [21] and Hubel [22] performed single cell recording using extracellular metal microelectrodes. This led to path-breaking discoveries about the structure and the organization of the cerebral cortex. Research contributions by several neuroscientists in the 1980s revealed the complex correlation between limb movement and neural activity in many motor areas of the cortex. Georgopoulos demonstrated that while single unit recordings correlate poorly with hand motion, the combined activity of several neurons provides the precise direction of movement [23]. Such results generated a great curiosity in the simultaneous recording of the activity of several individual neurons in the cortex, i.e., multi-unit recordings. Since then, the multi-unit approach has been extensively researched. During the 1990s, huge research efforts were directed towards extracting neural signals and using them to control various prosthetic devices. For neural recording front-end chip design, significant contributions are done by the research groups at the University of Michigan [24] [25] [26] [27], University of Toronto [28] [29], University of Utah [30] [31] and University of California [32] [33] [34] .

In 1986, at the University of Michigan, Najafi and Wise proposed a chip-compatible multichannel recording array using on-chip circuitry [24]. It combined a micro-machined silicon microprobe with on-chip CMOS analog circuitry to amplify, multiplex, and transmit analog intra-cortical neural activity recorded acutely from a number of neurons in the CNS. In 1992, Ji and Wise [25], designed an extension of the previous chip with higher gain, electronic positioning of the active recording sites, reduced noise, band-limiting, bidi-

rectional signaling over a single output lead, and functional upward compatibility with the previous circuit generation.

Soon it was realized that for future systems, recorded signals should be digitized before transmission to the outside world. On-chip analog-digital conversion is required for enhancing signal-to-noise ratio, simplifying wireless data transfer, and allowing limited on-chip digital signal processing for data compression and higher bandwidth. Inductively coupled RF telemetry for both power and data transfer are desirable, so that this implantable unit should have no interconnect wire, which could potentially cause infection. In 1998, Najafi and Akin developed a telemetrically powered neural recording system with multichannel, fully integrated circuitry in a bipolar CMOS process [26] [27]. [26] is one of the few complete telemetry systems developed for neurophysiological applications which combines signal amplification and filtering, low-power A/D conversion, bidirectional user interface and RF telemetry units for power and data transfer all integrated monolithically on a single chip. The most recent chip from the research group at the University of Michigan (A. M. Sodagar et al.) was developed in 2009 [35]. It is a fully wireless neural recording microsystem. The system is powered and programmed through an inductive RF link and telemeters the recorded neural information to an external host through a wireless link. It could detect spike occurrences on all channels simultaneously, and provided the signal wave shape on any one of the channels with 8-bit resolution.

In-between in year 2003, R. H. Olsson et al. [36] designed a fully integrated band-pass amplifier for neural recording systems. It uses diode-connected NMOS transistors that are biased in the sub-threshold region in the feedback loop of the amplifier. This amplifier design is referenced for our circuit.

In 2010, Perlin and Wise [37] [38] proposed a new probe and 64-channel analog front-end which had digitally programmable gain from 40dB to 60dB. All the existing circuits had unacceptable noise levels or consumed too much power to be fully implanted in large quantities. Implantable bio-amplifiers must dissipate little power so that surrounding tissues are not damaged by heating, so Harrison and his colleagues at the University of Utah developed a low-noise and low-power bio-amplifier for neural recording systems [39]. The topology has a MOS-bipolar pseudo-resistor in the feedback loop. Soon it was found that the frequency content of bio potentials of EEG, EMG, ECG span over four decades of frequency, from less than 1 Hz to around 10 kHz and over four decades of amplitude, from 1 μ V to over 10 mV. In 2007, Harrison designed a 16-channel front-end for neural recording systems with a tunable high frequency [30]. This chip has the ability to record different types of bioelectrical signals such as EEG, EMG, ECG, etc. Finally, in 2009, Harrison's group proposed a 100-channel integrated circuit for wireless neural recording systems [31] [40]. The chip contains amplifiers, a 10-bit Analog-to-Digital Converter (ADC) and a transmitter for sending out the data with programmable low and high cut-off neural signal frequency.

Another group which contributed significantly to neural recording systems is at the University of Toronto under the direction of Prof. R. Genov. Previously reported neural interfaces integrated with on-chip 3-D microelectrodes have typically had no more than 100 recording channels [40]. So in 2007, Genov's group designed a 256-channel analog front-end for neural recording systems [28].

Later in 2011 R. Shulyzki et al. (Prof. Genov research group at the University of Toronto) reported a closed-loop neural recording and stimulation system [29]. It has 256

recording channels and based on the given data taken from the recording channels, it generates stimulation signals for 64 channels. The analog front-end of the recording part is comprised of a two-stage fully differential amplifier with adjustable low-cutoff frequency. It also has a sample-and-hold cell and an ADC. This research group also designed wireless neural/EMG telemetry systems for small freely moving animals [41].

Significant contributions have been done by the research group (Biomimetic Research Laboratory, Prof. W. Liu et al) at the University of California, Los Angeles (UCLA). In 2006, they designed a wireless system for recording the neural activity of sharks [32]. In 2008, they designed a wearable neural recording system with wireless telemetry for monitoring live animal bio-potentials. The wireless capability with small power consumption and the minimal size and weight made it really suitable for monitoring the behavior of live animals [33]. In 2011, the same group developed a 64-channel fully integrated analog front-end [34]. Every channel has a two-stage amplifier with adjustable gain and corner frequency.

Recently they have designed a telemetry comprised of a pair of low-power, gigabit data rate transmitter and receiver operating at 60 GHz. It establishes a short distance wireless link to transfer the massive amount of neural signals outward from the implanted device. It could achieve a the high data rate of 6 Gb/s with a bit-error-rate of 10^{-12} at a transmission distance of 6 mm [42]. It is able to support thousands of recording channels while ensuring a low energy cost per bit of 2.08 pJ/b.

While great improvements have been made in this area neuroscientists want more channels for ample data recording which will allow them to look deeper into the functionality

of the nervous system. An input-referred noise lower than $2 \mu\text{V}_{rms}$ is desirable with sufficiently low power consumption for recording device's longevity. Our clinical partners have indicated a requirement of mid-band gain of 75 dB and low cut-off frequency and high cut-off frequency of 750 Hz and 7.5 kHz respectively.

Table 2.2 summarizes the specifications of the major state-of-the-art neural recording systems till date.

Table 2.2: State-of-the-art neural recording systems

Year	Reference	Technology (μm)	Power Supply(V)	TPD (mW)	TPD per channel (μW)	Chip-area(mm^2)	Area per channel (mm^2)	Gain(dB)	LCF (Hz)	HCF (Hz)	Input-referred Noise (μV_{rms})	# of Channels	Innovation
1986	[24]	6	5	5	-	1.3	-	40	-	-	-	10	Embedded signal Processing
1992	[25]	3	5	2.5	-	2.5	-	49.5	15	7k	15	32	Reduced noise, band-limiting
1998	[26]	3	5	90	-	4x6	-	-	100	3.1k	-	32	RF telemetry interface
2003	[36]	3	1.5	-	92	-	0.082	38.2	0.066	24k	16.6	1	MOS-transistor as resistor
2003	[39]	1.5	2.5	-	80	-	0.16	39.5	0.025	7.2k	2.2	1	Bipolar pseudo resistor in FB
2007	[30]	0.6	5	41	460	4.3x3.1	0.37	46	0.05	10-10k	2	16	Recording EEG, EMG, ECG
2009	[35]	0.5	1.8	14.4	75	-	0.072	59.5	<100	9.1k	8	64	Wireless Signal transmission
2010	[37]	0.5	1.5	-	50	3.1x4.8	0.098	40-60	10-100	9.1k	4.8	64	Programmable gain
2011	[29]	0.35	3.3	13.5	52	-	0.035	53-72	0.5-10	10k	7.99	256	Programmable gain-8 modes
2011	[34]	0.065	1.2	2.56	-	3x4	-	47-59	0.5-300	500-12k	3.8	64	Independent channel sampling

Chapter 3

Design of Field Programmable Analog Front-End Amplifier

This chip (AF7) is the next generation of a previous one designed by students in our research group. The previous chip, called AF5, has 16 programmable channels which are 4 blocks of 4 different channel types. Each channel contains a Low-Noise Amplifier (LNA) as the first-stage and a fully differential amplifier as the second.

Four blocks on that chip are classified based on whether the second stage amplifier of the channel is fully differential or single-ended, and if the MOS resistor used in the feedback path is PMOS or NMOS. The 4 blocks of the channels are classified as follows:

1. Second stage fully differential and NMOS feedback resistor (FDNMOS)
2. Second stage fully differential and PMOS feedback resistor (FDPMOS)

3. Second stage single-ended and NMOS feedback resistor (SENMOS)
4. Second stage single-ended and PMOS feedback resistor (SEPMOS)

Digital-to-Analog Converter (DAC) blocks digitally control the gate voltages of the feedback transistors which enable tuning frequency response of the recording channels. MUXs in design provide access to outputs of the channels and to select the desired tuning voltage for the MOS feedback transistors.

The AF5 analog front-end was fabricated in AMS 0.35 μm CMOS technology. A custom four-layer PCB (AF5PCB) was designed using Altium software. Attenuated outputs of signal generators were used to simulate the neural signals. A simple resistor divider was used for attenuation of signal generator outputs. An Opal-Kelly XEM6010 board with XC6SLX45 Xilinx FPGA was used to provide the digital data needed for the digital part of the chip as well as for getting the digital output data of the AF5. In board testing, the LNA and recording channels' gain were within 3-4 dB variation from the simulated values. The measured input-referred noise in channel was quite high, on the order of millivolts; this is too high for practical applications where input-referred noise should be on the order of a few microvolts(rms). Figure 3.1 shows the time-domain graph of data recorded from the previous chip. It is not the pure recording, i.e., it has been post-processed. Dual-threshold technique is used to identify true spikes. The thresholds are the two black lines, and they evolve over time. To be considered a spike, there must be two threshold crossings within a short, predefined window of time. The spike in the middle looks genuine (i.e., it was sufficiently amplified to be detected). However, there is a lot of noise in the channel. Also, out of 16 channels, some of the channels were not functional in the chip.

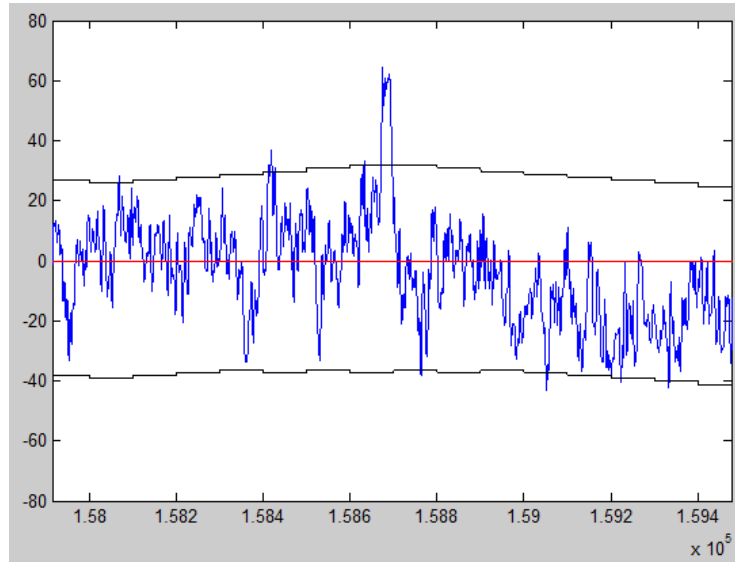


Figure 3.1: Measured noise in recording channel on PCB in AF5 chip. [Courtesy: Russell Dodd and Brendan Crowley]

The design goal for the AF7 chip is to reduce the noise in the recording channel. Also the focus is to identify the design issues behind the non-functional recording channels, rectify them and choose the most suitable channel architecture to design all 16 channels of this neural front-end. All the design blocks of AF5 are simulated using Cadence Virtuoso and potential design issues are discovered in simulations e.g. common-mode-feedback-loop instability and incorrect tuning voltage range for PMOS feedback resistor based channels.

In this chapter, various circuits available for the channel design are introduced. A comparison of these channel architectures is presented with respect to input-referred noise, power consumption, Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR), and common-mode-feedback loop stability.

3.1 Neural Recording Front-End Amplifier Specifications

The recorded neural signals have very small amplitude, usually in hundreds of microvolts with a bandwidth from 750 Hz to 7.5 kHz. For data conversion and signal processing these signals need to be amplified. Meanwhile, due to electrochemical effects at the electrode-tissue interface, there is typically an offset of 1-2 V across differential recording electrodes. An offset that is larger than the neural signals, will cause the amplifiers to be saturated. The local field potentials (LFP) are often accompanied by noise components, typically 0.1 mV_{rms} to 50 mV_{rms} below 300 Hz. The neural amplifier designed for neural recording should get rid of this low frequency interference.

3.2 Design Approach

The main characteristic for the neural recording front-end amplifier is to provide gain over the bandwidth of neural signals and reject the undesired frequency components outside this band. To achieve this, a two-stage amplifier is used for the channel design. The first-stage amplifier is an LNA as it directly interfaces with the neural recording micro-electrodes and other neural circuitry. The second stage is a high-gain and high swing amplifier.

To reject the DC offset and amplify only the small neural signals, a capacitive feedback amplifier circuit is used for both stages as shown in Figure 3.2. The DC feedback path through MOS-resistor ensures a low output offset voltage by forcing the output offset

voltage to be equal to the input offset voltage. This offers properties of a band-pass filter, where the amplifier's bandwidth can be limited to the desired range to filter out the noise that exists outside of the bandwidth.

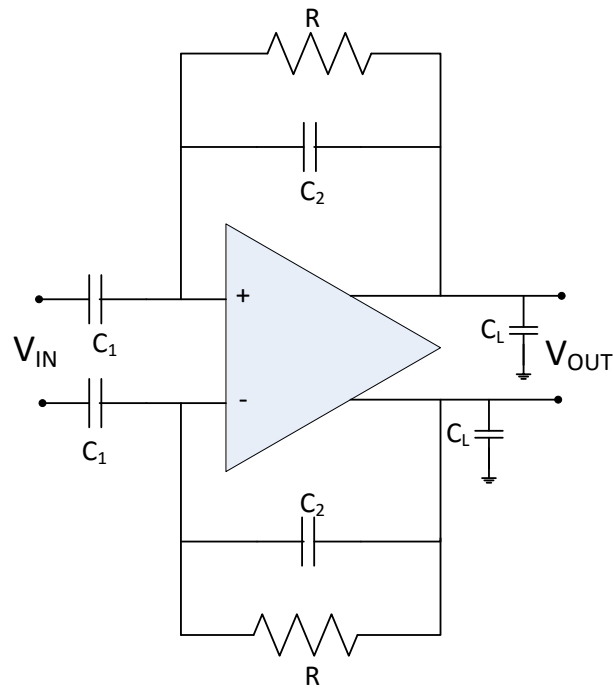


Figure 3.2: Band-pass filter for neural recording channel.

The corner (cut-off) frequencies of this band-pass filter are given by Eq. (3.1) and (3.2)

$$f_L = 1/2\pi RC_2 \quad (3.1)$$

$$f_H = G_m/A_v C_L, \quad (3.2)$$

where, in the high corner frequency equation, G_m is the trans-conductance of the amplifier, C_L is the equivalent capacitance of node V_{OUT} , and A_V is the mid-band gain of the filter given by Eq. (3.3)

$$A_V = C_1/C_2 \quad (3.3)$$

To filter out the noise outside the desired frequency band, appropriate values are selected for capacitances C_2 and C_L .

As per Eq. (3.1), the lower cut-off frequency is controlled using resistor R , so it should be set to a very large value to obtain a low cut-off frequency (750 Hz in our case). MOS resistors occupy smaller layout area than actual resistors. So in the proposed design, R is implemented using a MOS transistor that is biased in the sub-threshold region [43]; the gate voltage is set by a programmable DAC. Another important benefit of using a MOS resistor is that by controlling the bias voltage of the transistor the resistor, R , can be varied over a wide range. This approach is used to design the programmable recording channels and will be described in the following sections in more detail.

3.3 Evaluation and Comparison of Available Design Choices

Figure 3.3 shows the high level architecture of the neural recording channel, which contains a low noise amplifier (LNA) as the first-stage and a high-gain amplifier as the second stage.

Here is a quick comparison of the available design options.

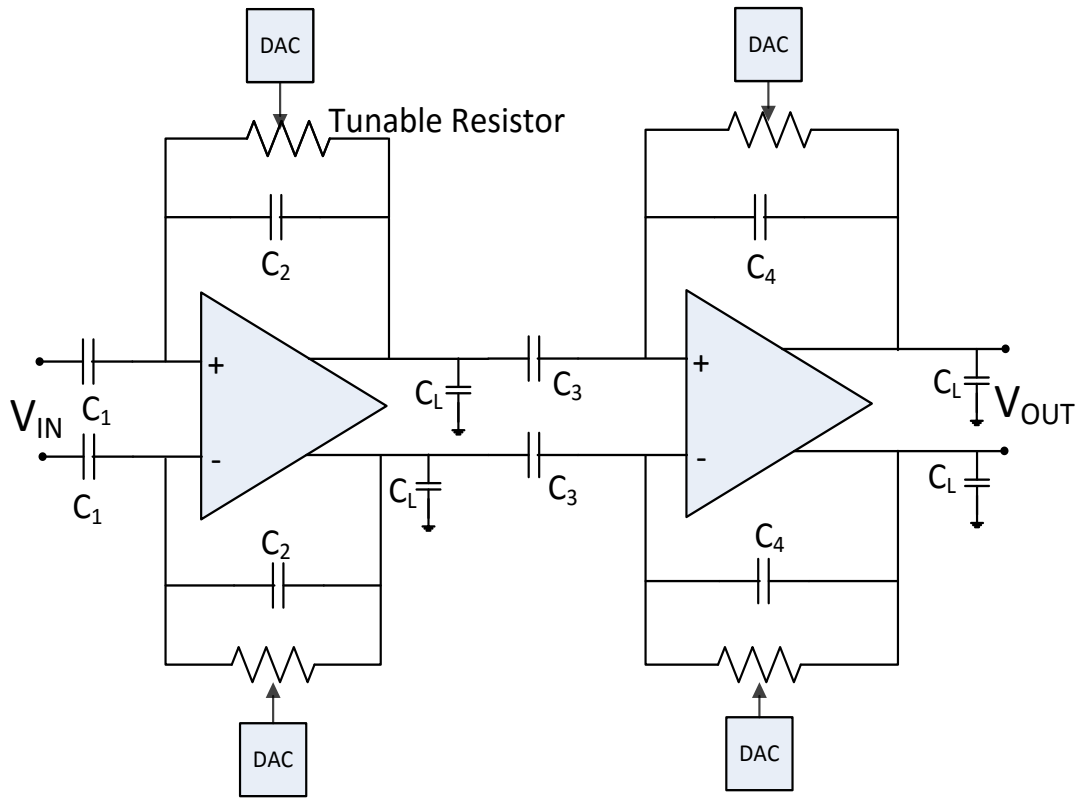


Figure 3.3: Generic architecture of neural recording channel.

3.3.1 Fully Differential vs. Single-Ended Amplifier

For choosing the amplifier structure for neural recording channel, power consumption and noise rejection are important factors. The amplifiers can be implemented in fully differential or single-ended configuration. Table 3.1 summarizes the comparison of various design

parameters for differential and single-ended architecture which can be used for the channel. Fully differential amplifiers have a higher common-mode-noise rejection than single-ended amplifiers. The power-supply-rejection ratio is approximately four times better for fully differential amplifiers than single-ended ones. On the other hand, single-ended amplifiers have less power dissipation and occupy a smaller area. These amplifiers are simpler to design and do not need common-mode feedback circuits.

Table 3.1: Comparison of fully differential and single-ended amplifier

Performance	Fully differential	Single-ended
Power Dissipation	High	Low
Area	High	Low
CMRR/PSRR	High	Low

3.3.2 NMOS vs. PMOS resistors

The resistors, which are used for the frequency tuning of the recording channel can be implemented using PMOS or NMOS transistors operating in weak inversion. The PMOS transistor has higher equivalent resistance than NMOS for same geometry and under same operating conditions. Flicker noise in PMOS is less in comparison to NMOS. A PMOS is fabricated in an N-well which provides better substrate noise isolation.

Based on the simulation results of the four channel architectures (FDNMOS, FDPMOS, SENMOS and SEP MOS), fully differential with NMOS resistor (FDNMOS) is selected for the design implementation. Simulation results will be discussed in the next Chapter.

3.4 Design Blocks

The main design blocks used for the neural recording system are an LNA for first stage, a high-gain and high-swing amplifier for second stage, DACs, and multiplexers. When designing a chip, it is important to develop a proper test strategy. Test structures are implemented using multiplexers in the design so that all the channels outputs and important nodes could be observed.

3.4.1 Low-Noise Amplifier (LNA)

The first stage of the analog front-end, which interfaces with the recorded neural signals, should have good noise performance. The recorded neural signals are very small in amplitude [13], so this stage should boost the neural signal power while adding as little noise and distortion as possible. For the same reason, a low-noise-amplifier is the best choice for implementing this stage.

Another important characteristic for LNA is input impedance. The input impedance of an LNA should match the high impedance of the recording electrode [44] to get a maximum signal power transfer between recording electrode and LNA. Gain is not very critical for this stage, as the second stage amplifier is especially designed for high gain and high swing.

Table 3.2 shows a comparison for various operational amplifier topologies [2] for gain, swing, power dissipation and noise. It reveals that telescopic amplifier offers low-noise and low-power dissipation, hence it is a good choice for the first stage. A fully-differential topology is used to get high noise-rejection-ratio, which requires a Common Mode Feedback

(CMFB). Figure 3.4 shows the schematic of a telescopic amplifier with its CMFB circuit. In this circuit V_{OCM} is common-mode voltage provided as input and based on this the CMFB circuit generates common-mode-feedback voltage which is fed back to LNA block. The transistor sizes of LNA are shown in Table 3.3.

Table 3.2: Comparison of different op-amp topologies. Referenced from [2](page 314)

Topology	Gain	Swing	Power Dissipation	Noise
Telescopic	Medium	Medium	Low	Low
Folded-Cascode	Medium	Medium	Medium	Medium
Two-Stage	High	Highest	Medium	Low
Gain-Boosted	High	Medium	High	Medium

The noise performance of this stage is highly critical for good quality neural recording system. Dominant sources of noise are: thermal noise and flicker noise.

Table 3.3: Transistor sizing of LNA and its CMFB circuit.

Transistor	W/L(μm)
$M_{1,2}$	40/20
$M_{3,4}$	8/10
$M_{5,6}$	2/10
$M_{7,8}$	4/20
$M_{9,10}$	8/10
$M_{11,12}$	4/20
$M_{13,14}$	2/10
$M_{15,16}$	4/10
$M_{17,18}$	4/10
$M_{19,20}$	8/10

The total input-referred noise, thermal and flicker for this telescopic amplifier circuit can be represented by Eq. (3.4) and (3.5).

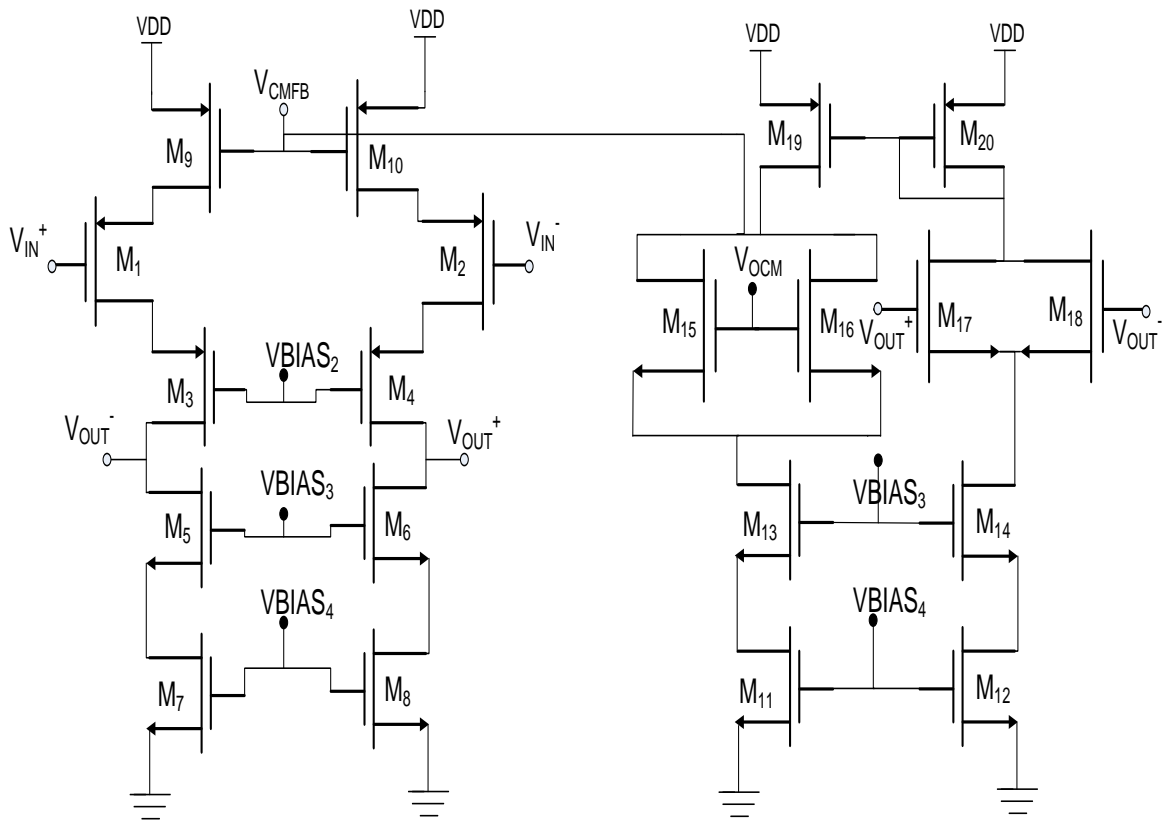


Figure 3.4: Schematic of LNA circuit and its CMFB circuit.

$$\bar{V}_n^2 = 4KT(2 * \frac{2}{3g_{m1,2}} + 2 * \frac{2g_{m7,8}}{3g_{m1,2}^2}) \quad (3.4)$$

$$\bar{V}_n^2 = 2\frac{K_P}{(WL)_{1,2}C_{ox}f} + 2\frac{K_N}{(WL)_{7,8}C_{ox}f}\frac{g_{m7,8}^2}{g_{m1,2}^2} \quad (3.5)$$

where in the thermal noise equation, K is the Boltzmanns constant, T is the temperature, and g_m is the trans-conductance of the transistor. In the flicker noise equation, W and L are the width and length of the transistor, C_{ox} is the MOS oxide capacitance, f is the working frequency, and K_N and K_P are the flicker noise coefficients of NMOS and PMOS transistors, respectively.

At relatively low frequencies, the cascode devices have negligible effect on the noise. While M_1 , M_2 and M_7 , M_8 are the primary transistors which control the noise in LNA. The noise contribution of M_1 and M_2 are equivalent, as the sizing of transistors on the left branch and right branch is the same. The same holds true for M_7 and M_8 as well.

The PMOS transistor has less flicker noise than NMOS [45]. Since M_1 and M_2 are the biggest contributors of input-referred noise, it is better to select PMOS transistors for M_1 and M_2 to alleviate the flicker noise. According to Eq. (3.5), for low flicker noise, the sizing of M_7 and M_8 should be smaller than that of M_1 and M_2 . Equivalently, g_{m7} becomes smaller than g_{m1} , resulting in less thermal noise in Eq. (3.4).

The amplifier gain is a critical factor for the amplifiers to be used in neural recording applications. In our circuit, the gain is defined by Eq. (3.6)

$$A_V \approx g_{m1}[g_{m3}r_{o3}r_{o1}||g_{m5}r_{o5}r_{o7}] \quad (3.6)$$

where, r_o is the output resistance of a MOS transistor.

A high open-loop gain is desirable for an LNA, to get good linearity in the amplifier performance. The transistor sizing is very important to meet these constraints for low-noise and high-gain.

In the LNA circuit, the V_{CMFB} needs to be set to a required voltage value for common mode output voltage. The design approach for Common Mode Feedback (CMFB) circuit is referenced from [46]. Together transistors M_{17} and M_{18} produce a current based on the common-mode voltage of V_{OUT}^+ and V_{OUT}^- . This current will be mirrored, I_{19} , and will be compared with the current created in M_{15} and M_{16} (I_{OCM}). It is desirable to get the same current in the branches of the current mirror. Transistors M_{15} - M_{18} are consequently chosen to be exactly same in size. The same procedure is followed to provide identical currents in M_{19} and M_{20} . If the common mode (CM) voltage of V_{OUT}^+ and V_{OUT}^- matches V_{OCM} , currents I_{19} and I_{OCM} become the same, and thus V_{CMFB} will be fixed. On the other hand, the larger common-mode voltage in V_{OUT} nodes than in V_{OCM} causes I_{19} to be greater than I_{OCM} , which decreases V_{CMFB} . As a result, the voltage of V_{OUT} decreases until its common-mode voltage equals V_{OCM} . This procedure also happens if the common-mode voltage of V_{OUT} becomes lower than V_{OCM} due to increased DC levels in V_{CMFB} . Finally, the sizing of other transistors is determined depending on the biasing voltages required for our circuit.

3.4.2 Second Stage Amplifier (High-Gain)

The primary requirement for this amplifier is high-gain and high-swing. The noise performance of this stage is not as critical as first stage amplifier. The impact of the second stage on the total input-referred noise of our recording system is reduced as the input-referred noise of the second-stage is divided by the gain of the first-stage in the our circuit. The fully differential folded-cascode configuration shown in Figure 3.5 is selected to implement the second stage.

Mobility of electrons is higher than holes under same operating conditions, so an NMOS transistor offers more transconductance than PMOS for the same size. Therefore, NMOS transistors are used for M_1 and M_2 in the folded-cascode amplifier to provide high gain. The gain of the second stage is defined by Eq. (3.7). The sizing of transistors is given in Table 3.4.

$$A_V \approx g_{m1} [g_{m10} r_{o10} r_{o12} || g_{m8} r_{o8} (r_{o16} || r_{o15})] \quad (3.7)$$

Table 3.4: Transistor sizing of folded-cascode amplifier circuit.

Transistor	W/L(μm)
M_{1-6}	1/1
M_{7-8}	4/1
R_{9-12}	1/1
R_{13-16}	4/1

This circuit has a good CMRR and PSRR [2]. The symmetric configuration of fully differential amplifiers introduces less non-ideality in the amplifier characteristics by elimi-

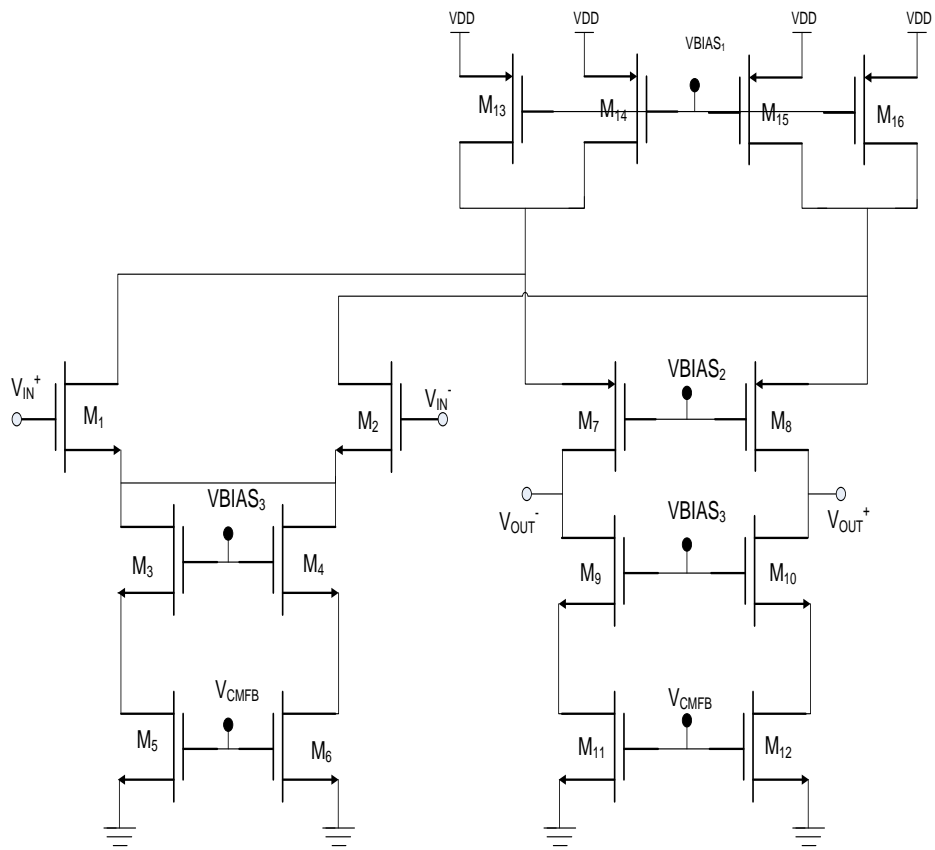


Figure 3.5: Schematic of fully differential folded-cascode amplifier circuit.

nating even-order types of distortion. The peak-to-peak output swing of this amplifier is given as Eq. (3.8).

$$V_{o,max(PP)} = V_{DD} + |V_{SS}| - 4|V_{OV}| \quad (3.8)$$

where V_{OV} denotes the overdrive voltage ($V_{GS} - V_{th}$) of a transistor. This swing is one overdrive voltage larger than that of a telescopic amplifier.

The CMFB circuit for a folded-cascode configuration is shown in Figure 3.6. This circuit senses the common-mode level of the two differential outputs and accordingly adjusts one of the bias currents in the amplifier.

The common mode voltage of the output is sensed using a resistive divider then this voltage is compared with V_{REF} and finally the error voltage is returned to the amplifier bias network [2]. This method of sensing the common-mode voltage is simple to implement, although it limits the differential output swing of the amplifier. The sizing details of the CMFB circuit of the folded-cascode can be seen in Table 3.5.

In folded-cascode architecture both the folding node and the output node contribute poles, so these op-amps must usually be compensated. In this circuit a compensating capacitor of 100 fF is added in CMFB circuit. This capacitor moves the dominant pole closer to the origin and improves the stability of CMFB circuit, but for a smaller bandwidth. The block diagram of the second stage amplifier with CMFB circuit, and compensating capacitor is shown in Figure 3.7.

A high-gain is required to amplify small neural signals ($100\mu\text{V} \sim 500\mu\text{V}$) up-to a reason-

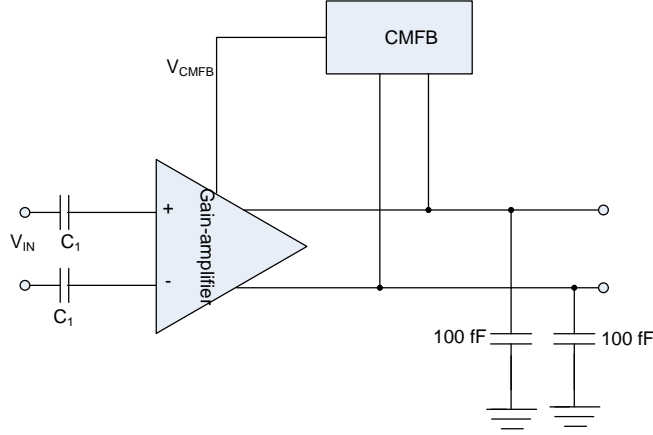


Figure 3.7: Second stage amplifier and compensating capacitor.

able voltage range for further signal processing. Since gain is ratio of maximum swing at the output and the amplitude of the input signal, the overall gain of the neural recording amplifier is set to be 78.2 dB. This is a reasonable gain to amplify the neural signals which are in the order of microvolts to 1-2 V range. Consequently, the gain requirement for LNA and second-stage is chosen as 38.2 dB and 40 dB, respectively.

As shown in Eq. (3.3), capacitors govern the gain of the amplifier. Area is an important constraint for finding proper value for capacitors. It is important to keep area as small as possible and this limits the value of the capacitor chosen. High cut-off frequency, i.e, 7.5 kHz and transconductance of LNA are determining factors for load capacitor (C_L). The capacitor C_3 acts as a load for LNA block so it should be chosen carefully. The capacitor values are shown in Table 3.6.

Table 3.6: Capacitor values for channel

Capacitor name	value
C_1	10.6 pF
C_2	129 fF
C_3	1 pF
C_4	10 fF
C_L	3.18 pF

3.4.3 Digital-to-Analog Converter

The neural recording amplifier is designed for a tunable frequency response. As described earlier, this is achieved in the design using MOS-based resistors in feedback. The MOSFET transistors in feedback operate in the sub-threshold region. These devices suffer from significant process variation and mismatch, which cause change in the frequency response of the recording channel. The equivalent resistance of the MOS device can be varied by changing the gate voltage of the MOS transistor. This feature enables tuning the frequency response of recording channels.

The gate voltage of these transistors can be changed using a 5-bit Digital-to-Analog Converter (DAC), which provides a tuning for frequency response of the channel. The 5-bit DAC is implemented using Kelvin-divider circuit. An N-bit version of this DAC simply consists of 2^N equal resistors in series between V_{HIGH} and V_{LOW} supply voltages. There are 2^N switches, one between each tap and the output. The output is taken from the appropriate tap by closing just one of the switches. It is one of the simplest DAC architectures, but it requires large number of resistors and switches.

The voltage of the i_{th} node from the 2^N stack of the resistors can be given as Eq. (3.9).

$$V_i = V_{LOW} + [(V_{HIGH} - V_{LOW}) * \frac{i}{2^N}] \quad (3.9)$$

Figure 3.8 shows the 5-bit DAC implemented in the chip. In our design the function of 2^N switches is implemented using a 32x1 multiplexer circuit. The details of multiplexer architecture is provided further.

3.4.4 Multiplexer

The multiplexer circuit used in the design is implemented in pass transistor logic. The pass-gate 2x1 multiplexer schematic is shown in Figure 3.9 [47]. Eq. (3.10) and (3.11) show the functionality of the MUX circuit.

$$V_{OUT} = A \quad \text{when } S = '1' \text{ and } SN = '0' \quad (3.10)$$

$$V_{OUT} = B \quad \text{when } S = '0' \text{ and } SN = '1' \quad (3.11)$$

Here SN is complementary of signal S. This logic style significantly reduces the number of transistors for a multiplexer circuit as compared to any other logic style.

As previously stated, the DAC has a 5-bit multiplexer in its architecture. This 5-bit MUX is implemented using a 2-bit MUX circuit in series with 3-bit MUX as shown in Figure 3.10.

Figure 3.11 shows a schematic of the 8x1 MUX circuit used in the chip.

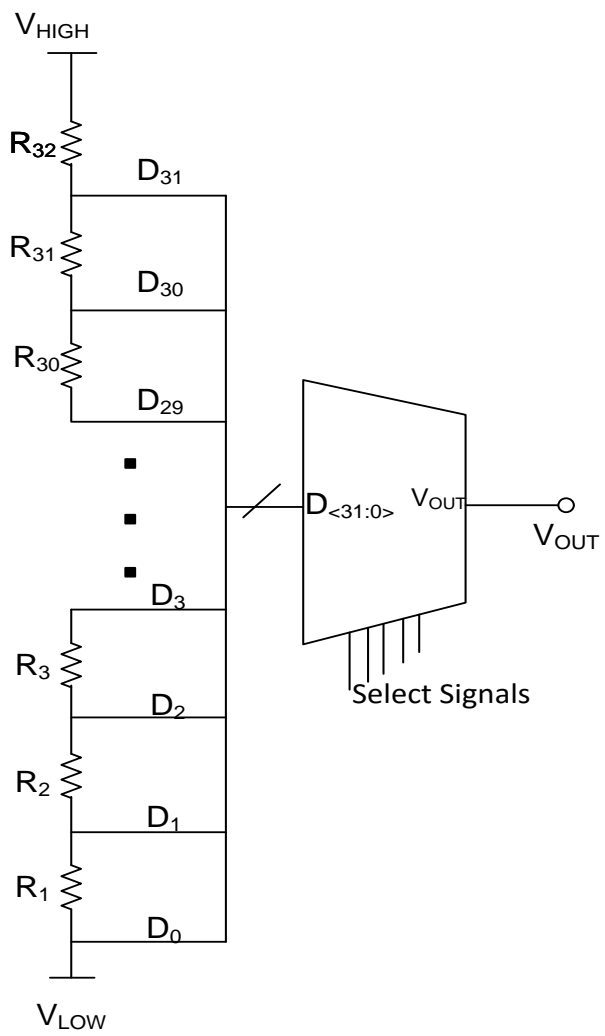


Figure 3.8: 5-bit DAC circuit.

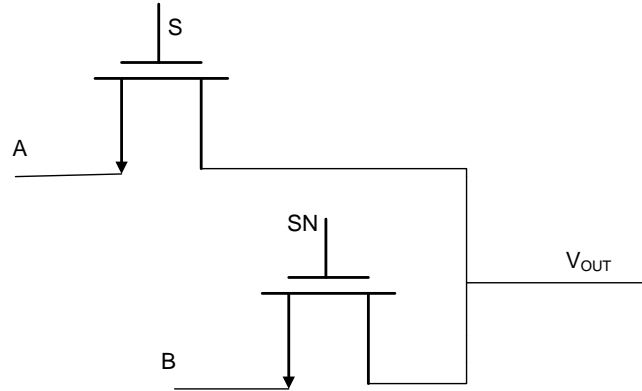


Figure 3.9: Pass-transistor implementation of MUX cell.

3.4.5 Access to Internal Nodes

It is important to test the critical internal nodes and voltages in the chip. But due to fabrication constraints it is not feasible to provide port for each of these nodes on the chip. As an intelligent solution, access to important internal nodes is implemented using multiplexer circuit (test MUX-block).

To monitor common-mode-feedback voltage of the amplifiers 8x1 MUXs are used. These provide access the V_{CMFB} of the desired channel. To monitor the outputs of LNAs and second stage amplifiers, the output of the channels 1,5,9,13 are directly connected to output pins, while the others can be accessed using MUX blocks. The output of each amplifier for a desired recording channel can be obtained using proper select signal for the MUXs.

To reduce the loading effect, each MUXs output was connected to an amplifier with a unity gain feedback as a buffer. The buffer needs to have a high gain with a fairly high swing. A basic two-stage amplifier, shown in Figure 3.12 was used for the buffer. The gain

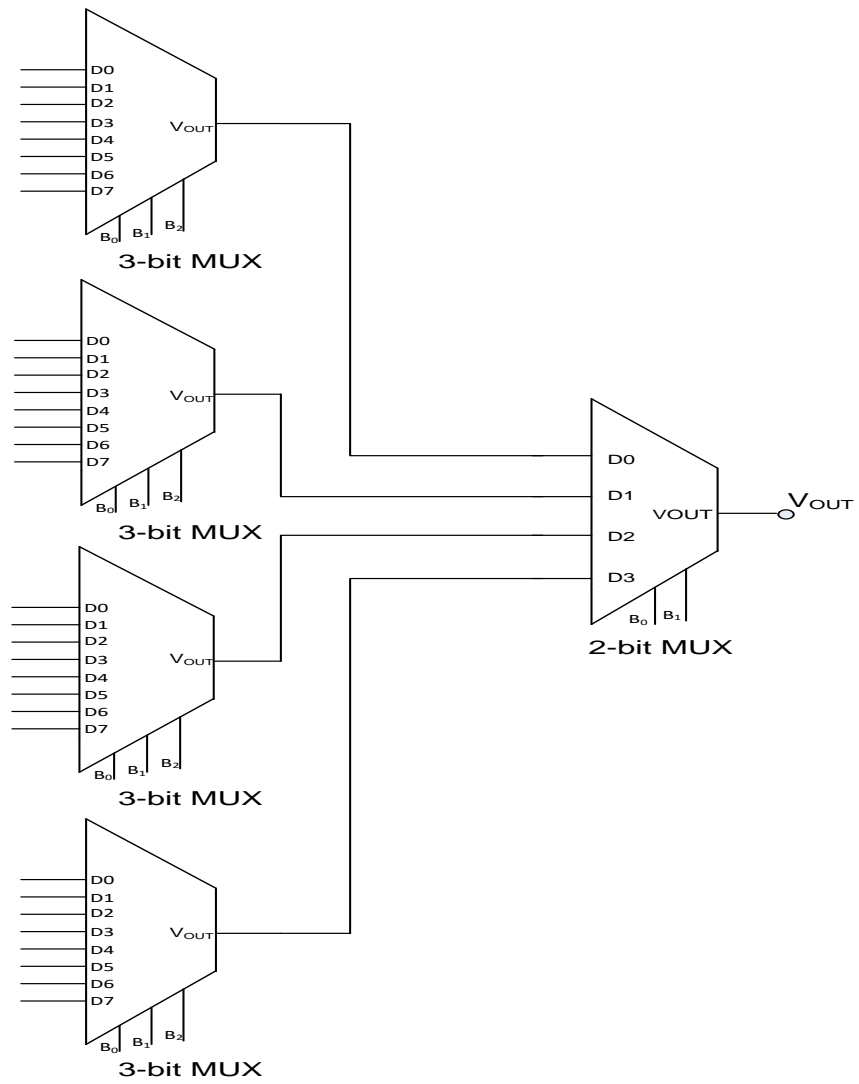


Figure 3.10: Architecture of 32x1 MUX (5-bit) circuit for DAC.

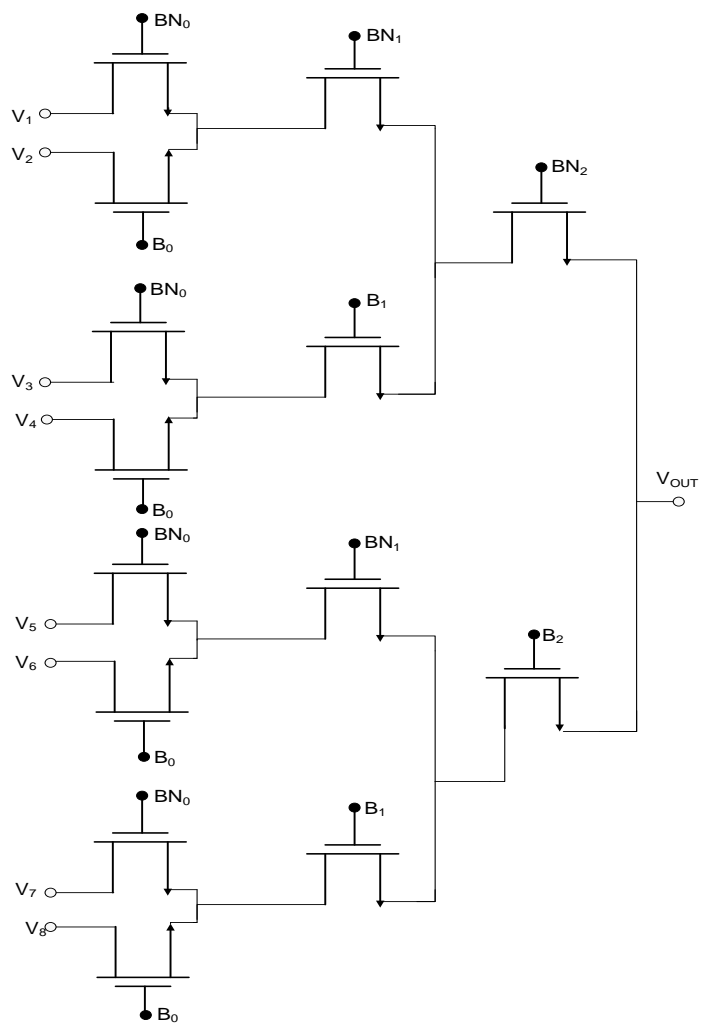


Figure 3.11: Schematic of 8x1 MUX circuit for DAC. Here B_0 , B_1 and B_2 are select signals for MUX and BN_0 , BN_1 and BN_2 are complement of these signals.

equation for the two-stage amplifier is given by Eq. (3.12).

$$A_V \approx g_{m1}[(r_{o2}) || (r_{o4})] g_{m7}[(r_{o7}) || (r_{o8})] \quad (3.12)$$

Table 3.7 provides the sizing details for the Miller amplifier circuit.

Table 3.7: Transistor sizing of Miller amplifier

Transistor	W/L(μm)
M _{1,2}	4/0.5
M _{3,4}	1/0.5
M _{5,6}	4/0.5
M ₇	6.65/0.5
M ₈	5* 4/0.5

Bias voltages for LNA and second stage amplifiers are critical for correct functioning of recording channels. Access to the bias voltages are provided from the chip ports using multiplexers. Tuning voltages which change the frequency response of each channel can be obtained at the output pin using correct set of select signals in the multiplexers.

3.4.6 Digital Block

MUXs are used for two purposes in the design: To access the internal nodes and to select tuning voltage from the DAC blocks. These multiplexers have controlling or select inputs that use digital signals.

These digital signals are generated, using a digital block comprised of serial shift registers implemented in design. One of shift registers (48-bit width) is used for multiplexer, for accessing nodes. While 64, 5-bit registers are required to get tuning voltages from DACs.

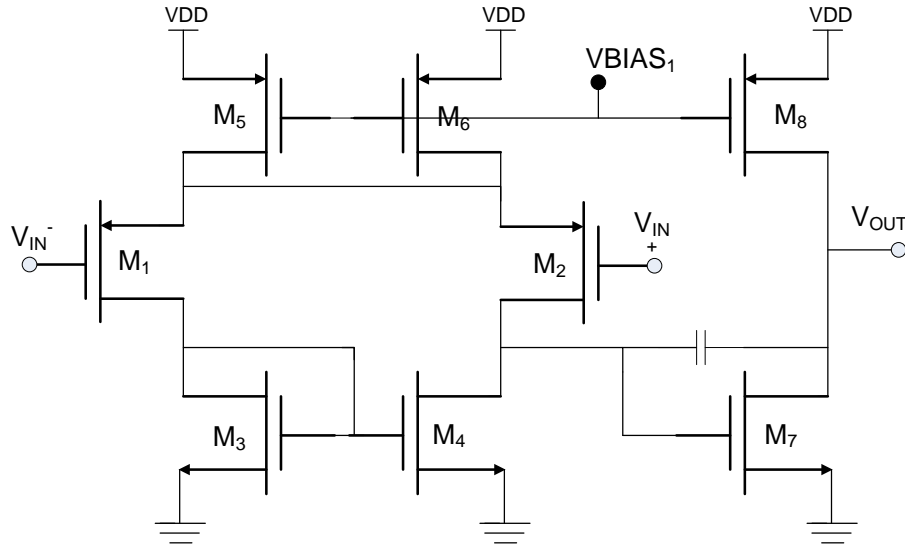


Figure 3.12: Schematic of Miller Amplifier circuit.

The digital values are sent to the input of the chip, then shifted inside. The last bit in the shift register will be connected to the outside pin of the chip to make sure the data is being sent correctly. The MUXs are also connected to the desired bit of the shift registers to get the proper value. The shift registers are the standard ones from the library of AMS 0.35 μm technology.

Chapter 4

Simulation and Measurement Results

4.1 Simulation Results

Our circuit is tested for correct functionality and other design parameters as power dissipation, speed and noise. In this chapter, the simulation results for various design blocks of neural front-end circuitry are provided.

Cadence-ADE simulations are performed for the four architectures to find the most suitable architecture for implementing the channel. Results for CMRR, PSRR, input-referred noise and power-dissipation are compiled in Table 4.1. Based on Table 4.1 results, it is concluded that differential architecture wins over single-ended architecture for noise performance.

Monte-Carlo simulations are done to find the gain and bandwidth deviations for FDN-MOS and FDP MOS. Based on these simulation results fully differential architecture with

Table 4.1: Comparison of different channel architectures

Parameter	FDNMOS	FDFPMOS	SENMOS	SEPMOS
CMRR(dB)	120	140	100	90
PSRR(dB)	31	30	12	18
Power Dissipation(μ W)	149.7	149.7	124.9	124.9
Input-referred Noise (μ V _{rms})	6.97	6.9	6.9	6.9

NMOS feedback resistor is selected for design implementation of all 16 channels of neural recording front-end.

4.1.1 Low-Noise Amplifier

Figure 4.1 and Figure 4.2 show the AC and transient analysis results of the LNA block, where the input signal amplitude is 250 μ V at 2.5 kHz. As shown in Figure 4.1 gain of the LNA block is 37.9 dB and the low and high cut-off frequencies are 765 Hz and 6.84 kHz respectively.

Noise analysis is performed for LNA block and result is shown in Figure 4.3. The input-referred noise of the LNA integrating from 750 Hz to 6.9 kHz is equal to 6.95 μ V_{rms}.

4.1.2 Second Stage Amplifier

Second-stage amplifiers is designed for high-gain with a target of 40 dB. Figure 4.4 shows the frequency response of fully differential folded-cascode amplifier with NMOS feedback resistor. It can be seen that the gain is 39.92 dB, which is quite close to the design target of 40 dB.

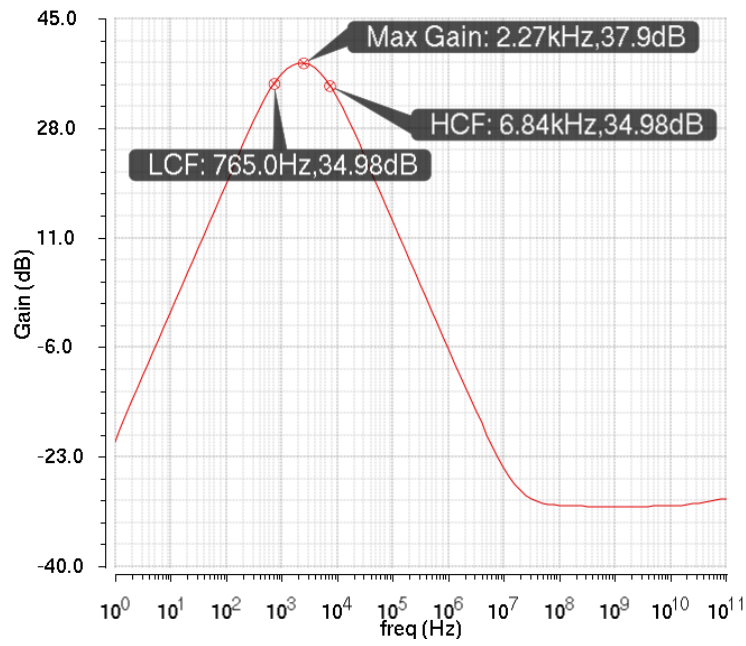


Figure 4.1: Frequency response of the LNA.

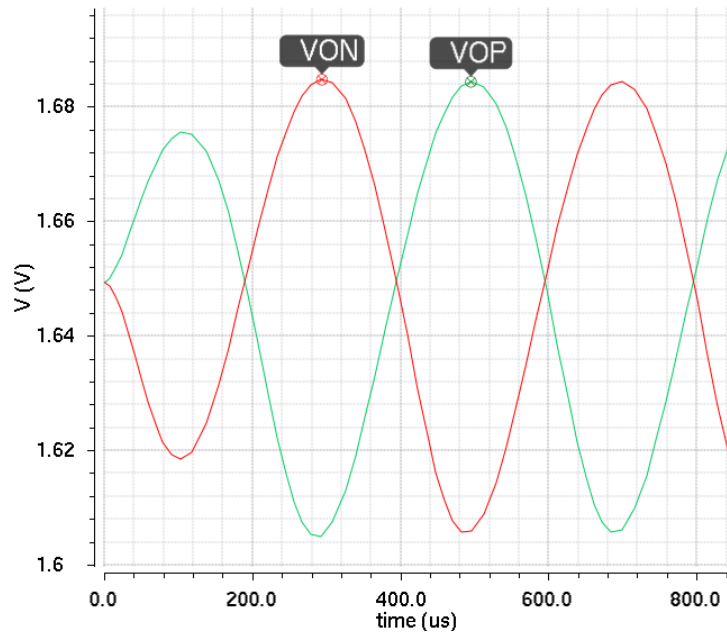


Figure 4.2: Transient simulation of the LNA.

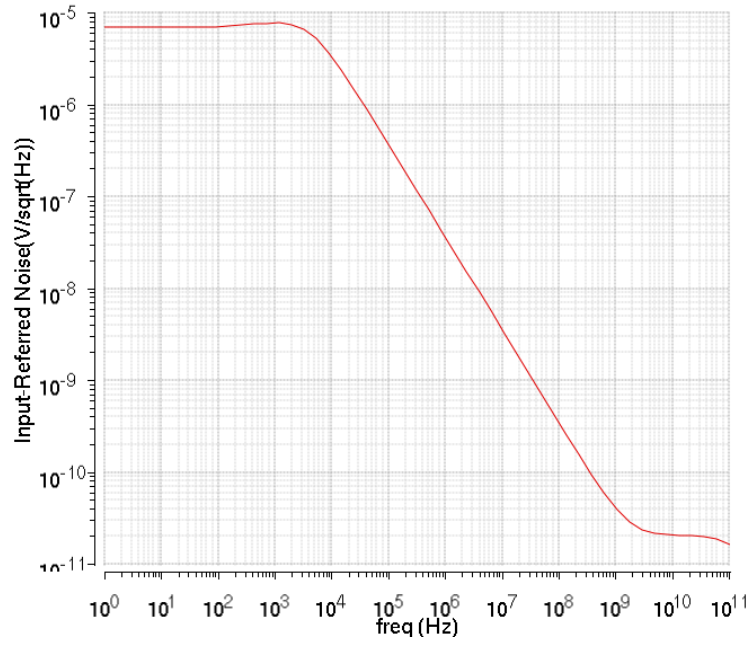


Figure 4.3: Noise simulation of the LNA.

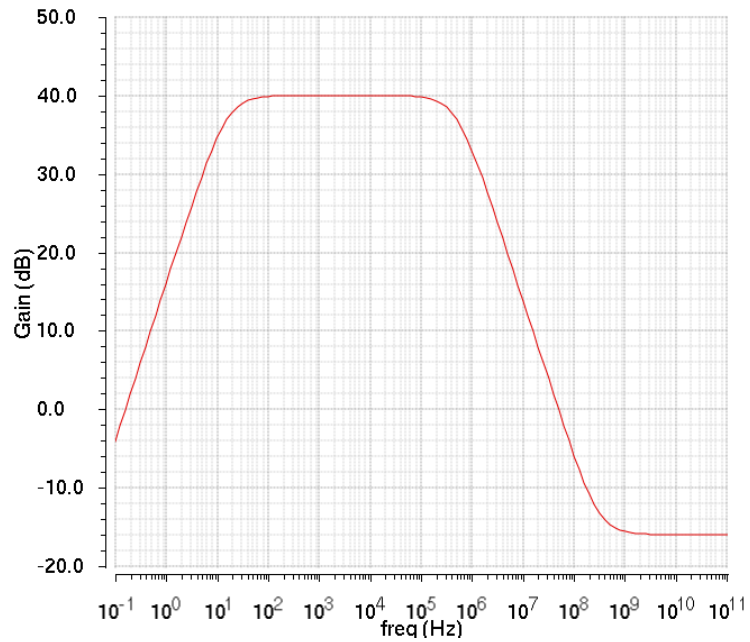


Figure 4.4: Frequency response of the second-stage amplifier.

4.1.3 Recording Channel

Figure 4.5 shows the frequency response of the complete recording channel. The total gain of the channel is 77.9 dB, and Low Cut-off Frequency (LCF) and High Cut-off Frequency (HCF) of the channel are 750.7 Hz and 5.41 kHz, respectively. The input-referred noise of the recording channel integrating from 750 Hz to 6.9 kHz is $6.95 \mu\text{V}_{rms}$. It meets the design specifications as the input-referred noise is lower than $10 \mu\text{V}_{rms}$.

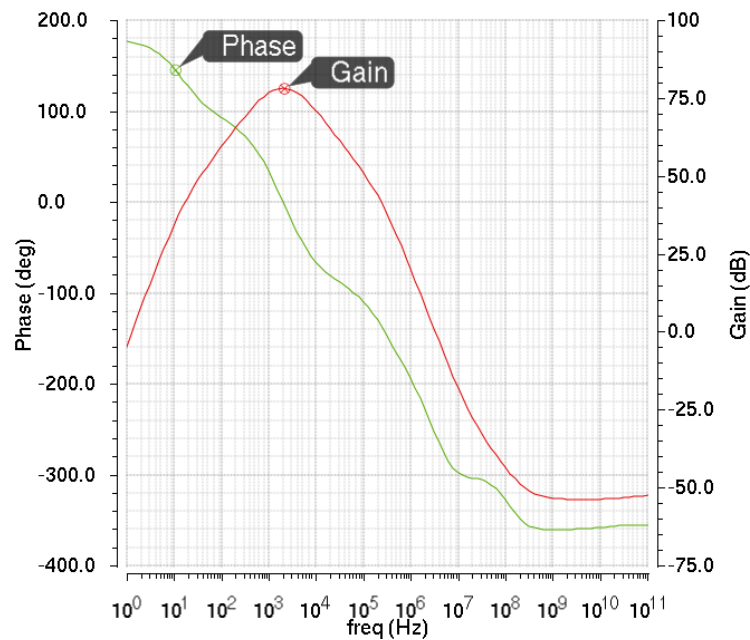


Figure 4.5: Frequency response of the recording channel.

Chapter 5

Conclusions

5.1 Summary and Contributions

In this thesis, a low-noise amplifier for a neural recording system is designed and fabricated on AMS 0.35 μm technology. The noise performance and power consumption are critical requirements for neural recording applications so this neural recording system is optimized for low-noise and low-power.

The recording channel consists of two stages, an LNA and a high-gain and high-swing amplifier. MOS resistors in feedback provide a band-pass filter characteristic for the channel. The channel is designed to get a high-gain in the desired frequency range and attenuate the noise outside this bandwidth. It has DACs to tune the frequency response of each channel digitally to overcome process variation, and other mismatches.

Several blocks are referenced from a previous generation chip (AF5) for this project.

The various channel architectures are compared for noise performance using simulations and based on the comparison results an LNA is selected for first stage and a fully differential folded-cascode amplifier is used for second stage. An NMOS transistor is used in the feedback loop of the amplifier. CAD simulations revealed that previous generation chip(AF5) has some design issues in certain blocks, e.g., common-mode-feedback loop instability, incorrect tuning voltage range for PMOS resistor based channels etc. Appropriate design changes are implemented in the chip to take care of these issues.

One of the primary characteristic for the future neural recording systems is to be fully implantable to avoid risk of infection. So the tuning for these systems should be done automatically without any human intervention. This chip is designed as programmable so that a self-tuning feature can be implemented on chip. The goal is to digitally tune the frequency response of the channels with the aid of DACs. On the test board, FPGA and ADCs can drive the DACs to provide self-tuning capability.

5.2 Future Work

- We have just received our test chips and will be testing that in the next 2 months.
- To devise a complete implantable neural recording system, it is required to combine the neural front-end designed in this thesis with an on-chip digital signal processing block and wireless power and data transmission modules.
- Further advances are needed to make more compact neural recording front-end which can enable packaging the neural recording system with the probing micro-electrodes

together locally. The amplified signals can be transmitted wirelessly for further processing.

- To increase implanted neural recording system's longevity and to avoid frequent surgeries, it is important to co-design an efficient power delivery method for the neural front-end circuitry. Currently batteries used in most common implantable applications such as cardiac pacemakers are cumbersome which require frequent surgeries to replace them and some sort of encapsulation which do not scale well down to the millimeter sizes.

Energy harvesting within the body is one potential alternative, but its power density and longevity, remain insufficient for miniature implants. Several other modalities of power supply, including via radio frequency by induction, or infrared light via a photovoltaic converter which demonstrate high power density can be used as promising choices.

APPENDICES

Appendix A

Current and Voltage Reference

A.1 Design of Current Reference

Robust current and voltage references are necessary to provide stable and correct biasing voltages for the circuits. For an ideal voltage reference source, the reference voltage should be independent of any fluctuations in power supply and temperature variations.

Band-gap circuits are popular circuits to generate stable and reliable reference voltages; however, the architecture is not preferred in our design. These circuits are more suitable for bipolar transistors while their CMOS implementation is cumbersome. Moreover, Beta Multiplier Reference (BMR) circuit does not have substrate current injection, the biggest disadvantage of the bandgap references. Therefore, a Beta Multiplier Reference (BMR) suggested in [45] for CMOS technology is used for our design. Figure A.1 shows a schematic for this circuit with its start-up circuit. Table A.1 shows the transistor sizing for the BMR

circuit.

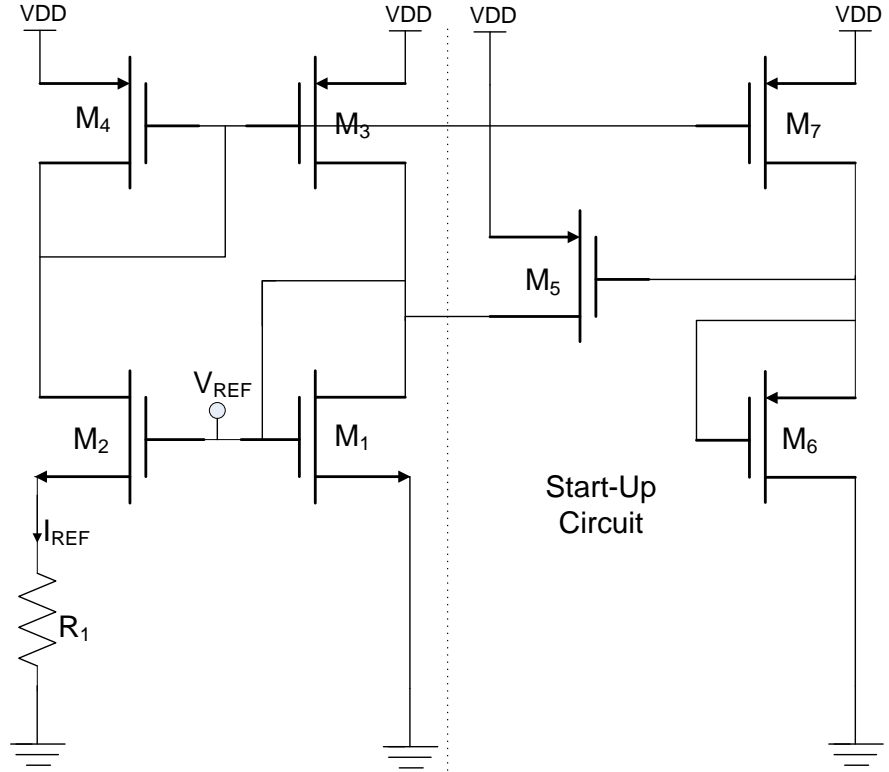


Figure A.1: Schematic of Beta multiplier reference circuit

The sizes (W/L) of transistors M_3 and M_4 are equal to force same current through each leg of circuit. For the BMR circuit the gate-to-source voltages for M_1 and M_2 can be related as Eq. (A.1)

$$V_{GS1} = V_{GS2} + I_{REF}R_1 \quad (\text{A.1})$$

where V_{GS} is the voltage between the gate and source of the transistor.

Table A.1: Transistor sizing of BMR circuit.

Transistor	W/L(μm)
M ₁	2/2
M _{2,3,4}	4*2/2
M ₅	2/1
M ₆	1/80
M ₇	2*4/1

The size of MOSFET M₂ is made larger than that of M₁ so that the difference in the gate to source voltage of M₁ and M₂ is dropped across R. To ensure that the circuit works correctly, V_{GS1} should be greater than V_{GS2} . This condition is satisfied by making the W of transistor M₂, K time larger than that of M₁ (its transconductance parameter, beta, is larger than M₁'s), while K is greater than 1. The difference in the gate to source voltage of M₁ and M₂ is dropped across R. Furthermore, K greater than 1 guarantees positive feedback in the circuit, resulting in a stable circuit. Using Eq. (A.1) and the current equations of transistor M₁ and M₂, I_{REF} and V_{REF} values can be derived as equation (A.2) and (A.3).

$$I_{REF} = \frac{2}{(R_1)^2 K \mu_n C_{ox} \frac{W_1}{L_1}} \left(1 - \frac{1}{\sqrt{K}}\right) \quad (\text{A.2})$$

$$V_{REF} = \frac{2}{(R_1) K \mu_n C_{ox} \frac{W_1}{L_1}} \left(1 - \frac{1}{\sqrt{K}}\right) + V_{thn} \quad (\text{A.3})$$

where V_{thn} is the threshold voltage of the NMOS transistor. It can be seen that both V_{REF} and I_{REF} values are independent of power supply.

Resistor, R_1 , has a positive temperature coefficient i.e., a rise of temperature increases the voltage drop across R_1 , while V_{GS} reduces with temperature increase. V_{GS2} shows this inverse trend as V_{th} has negative temperature coefficient. Therefore, by finding a proper value for R_1 , these two voltages can compensate for each other and produce a voltage that is not a function of temperature [48]. Eq. (A.4) and (A.5) show the temperature coefficients of I_{REF} and V_{REF} , respectively.

$$\frac{\partial I_{REF}}{\partial T} = I_{REF} \left[\frac{-2}{R_1} \frac{\partial R_1}{\partial T} - \frac{1}{K \mu_n C_{ox}} \left(\frac{\partial K \mu_n C_{ox}}{\partial T} \right) \right], \quad (\text{A.4})$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{thn}}{\partial T} - \frac{2}{R_1 K \mu_n C_{ox} \frac{W_1}{L_1}} \left(1 - \frac{1}{\sqrt{K}} \right) \left(\frac{1}{R_1} \frac{\partial R_1}{\partial T} + \frac{1}{K \mu_n C_{ox}} \frac{\partial K \mu_n C_{ox}}{\partial T} \right) \quad (\text{A.5})$$

Above equations show that the I_{REF} and V_{REF} temperature coefficients depend on W/L , R_1 and K , and choosing proper values for these parameters results in the desired reference values. The K value is usually set to 4 in most designs, and known as constant-gm bias circuit. By choosing $K=4$, g_m is equal to Eq. (A.6) It can be seen that, g_m is not a function of MOSFET process shifts, and is a constant value [45].

$$g_m = \sqrt{2K \mu_n C_{ox} \frac{W_1}{L_1}} \cdot I_{REF} = 1/R_1 \quad (\text{A.6})$$

The BMR circuit is a self-biased circuit, and so it is essential to use a startup circuitry ($M_5 - M_8$) to avoid working at the undesired operating point (zero current). If a circuit

works in this situation, transistors M_1 - M_4 are off at time zero. The gate voltage of M_1 and M_2 is zero, while the voltage at the gate of M_3 and M_4 is V_{DD} , causing M_7 and then M_6 to be turned off. Consequently, the gate-source voltage of M_6 is less than V_{thn} , causing M_5 to be ON, which runs the current flow through M_1 and M_2 . The voltage of gate M_1 and M_2 keeps increasing until all 4 transistors are ON. When the circuit works at the desired biasing points, M_6 turns OFF.

The biasing circuit to generate the required biasing voltages for both amplifiers in the design is shown in Figure A.2 [45]. Different biasing voltages are needed to bias the telescopic and folded-cascode amplifiers, so the sizing of transistors for each amplifier is different. Tables A.2 and A.3 show the transistor sizing for the telescopic and folded-cascode amplifiers, respectively.

Table A.2: Transistor sizing of LNA-biasing circuit.

Transistor	W/L(μm)
M_1	1/16
$M_{2,5}$	2/2
$M_{3,6,9}$	8/10
$M_{4,7,10}$	4/1
M_8	1/40
M_{11}	1/1
M_{12}	2/10

A.2 Simulation and Test Results

Table A.4 shows the simulation values of the various biasing voltages of used in the design. To ensure that the circuit is biased correctly the reference voltage and other bias voltages

can be probed from the output pin. The V_{REF} is connected directly to the output pad. The 8 bias-points for each amplifier stage were connected to an 8x1 MUX and the output of the MUX is connected to one output pad.

Table A.4: Simulation values of biasing voltages.

Biasing Voltages	Values(V)
V_{REF}	0.673
VBIASL ₁	2.298
VBIASL ₂	1.306
VBIASL ₃	1.699
VBIASL ₄	0.889
VBIASF ₁	2.4
VBIASF ₂	1.984
VBIASF ₃	1.308
VBIASF ₄	0.678

Appendix B

Other Simulation Data

Monte-Carlo simulation results for FDNMOS are shown in Table B.1.

Table B.1: Monte-Carlo Simulations for FDNMOS channel

FDNMOS	Min	Max	Mean	Median	Stddev
Gain(dB)	74.67	78.26	77.49	77.85	0.8325
HCF(kHz)	2.1	16.3	6.7	5.4	3.4
LCF(Hz)	45.62	9365	1986	729	2512

Common-mode-feedback loop stability simulations are done using Cadence 'stb' analysis. As shown in Table B.2, CMFB loop has a good gain and phase margin, and is stable.

Table B.2: CMFB loop stability analysis for FDNMOS channel

Parameter	value
Gain Margin	15.32 dB
Phase Margin	67.92 deg

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