

# **Numerical and Statistical Performance Analysis of Multi-Gate Negative Capacitance Field-Effect Transistors**

by

Andrew Richard Bahlmann

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# Author's Declaration

This thesis consists of material all of which I authored or co-authored: see Statement of Contributions included in the thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

# Statement of contributions

I was the sole author for Chapters 1, 2, and 5 which were written under the supervision of Dr. Youngki Yoon and were not written for publication. This thesis consists in part of two manuscripts which were prepared during the course of this Master's degree. As of the submission of this thesis they have not yet been submitted. My own individual contributions to these works are indicated below:

- Chapter 3: The work in this chapter is adapted from a paper currently in preparation for submission to a scientific journal. I performed all of the simulations during this studying and contained within this paper, prepared all figures, and wrote the corresponding sections, assisted by Hyunjae Lee from the University of Waterloo. The project was supervised by Prof. Youngki Yoon (University of Waterloo).
- Chapter 4: The work in this chapter is adapted from a paper currently in preparation for submission to a scientific journal. I performed all of the simulations during this studying and contained within this paper, prepared all figures, and wrote the corresponding sections, assisted by Hyunjae Lee from the University of Waterloo. The project was supervised by Prof. Youngki Yoon (University of Waterloo).

# Abstract

With the continued scaling of field-effect transistors (FETs) we have past the point where short-channel effects (SCEs) become a dominate factor in device performance. In particular, FETs suffer from increased leakage currents in their OFF-state, resulting in sub-optimal performance characteristics. Simultaneously, increased power densities place a strain on methods of cooling computer processors. To alleviate these effects and meet future computing demands, there are two avenues of research which must be pursued in parallel, namely, (i) low-power FETs which operate at reduced supply voltages, achieving their ON-state currents at lower gate voltages and (ii) multi-gate FET architectures which aid in the mitigation of SCEs by increasing gate controllability.

This thesis addresses these obstacles and possible solutions by studying multi-gate negative capacitance (NC) FETs, whereby a ferroelectric (FE) material is used to modify the gate structure and increase the electric field to improve device performance. Computer simulations in Synopsys Sentaurus TCAD are used to simulate the device operation of NCFETs and study the use of FE material layers in the gate stack of multi-gate FETs.

The body of this thesis is composed of two works of original research. The first studies the effect of a tapered NC-FinFET structure on the resulting device performance characteristics. The simulation results of devices with a tapered fin and FE layer indicate the optimum subthreshold swing and ON-state current can be obtained when the taper of the fin is minimal and the taper of the FE is significant. The second work investigates the relationship between statistical variations in the FE thickness of an NC nanosheet (NS) FET device and its resulting performance. The simulated sample sets of NC-NSFET devices show that as the variance of the FE thickness decreases the variability in performance characteristics diminishes. Guidelines are established for obtaining a particular variance in performance metrics which depend on the variance in FE material thickness.

The research conducted in these works establishes design principles of multi-gate NCFET devices for specific applications and target performances, expands the contemporary understanding of FE materials for achieving NC enhancement in multi-gate FETs, and will aid engineers and designers in the continued scaling of FET technology without sacrificing future performance criteria.

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*“It is not knowledge, but the act of learning, not possession but the act of getting there,  
which grants the greatest enjoyment.” - Johann Carl Friedrich Gauss*

# Chapter 1

## Introduction

Humanity's technological progress in the last half century can be directly attributed to the invention and continued development of the metal-oxide-semiconductor field-effect transistor (MOSFET). The fundamental goal in the advancement of MOSFETs has remained unchanged, namely, scaling the dimensions and operating voltages of complementary MOS (CMOS) technology. As the length of MOSFETs decreased the number of transistors that can be placed on a computer chip increased in accordance with Moore's Law [1]. Currently, the channel length of MOSFETs are on the order of 10 nm, however, the advancements in material engineering and fabrication techniques of MOSFETs, while successful in the continuation of Moore's Law, present unique challenges [2]. In particular, FETs of such dimensions are susceptible to quantum mechanical short channel effects (SCEs) which negatively impact their performance. In addition, as the gate lengths of MOSFETs continue to decrease the power densities on contemporary computer chips will increase exponentially, ultimately resulting in a limitation on cooling capabilities of logic devices [3, 4]. Due to the advent of 5G and the Internet of Things, the demands on computing power are only expected to increase. Given the current status of MOSFET developments, how can we move forward? How can we meet the future demands of higher operating frequencies without an increase in power density and fabricate FETs which operate at lower voltages to reduce their power consumption?

To meet the challenges of designing and fabricating sub-10 nm MOSFETs there has been a significant investment in the research of such devices in both academia and the semiconductor industry. The further scaling of MOSFET technology in recent years has led to the development of multi-gate MOSFET architectures with larger effective gate widths and improved gate controllability. Specifically, the FinFET architecture has been implemented for scaling below 10 nm. Currently, gate-all-around (GAA) FETs with their further increased gate control are being investigated and will most likely be the successor to the FinFET design in future years [5]. However, the increasingly complicated MOSFET structures require more involved fabrication procedures. At the same time, there has been substantial interest in sub-60 mV/dec, i.e., low-power, technologies, including tunnel FETs (TFETs) and the use of ferroelectric (FE) materials to fabricate so called negative capacitance (NC) FETs [6, 7]. These devices, with their steep subthreshold behaviour, operate at lower voltages reducing the amount of heat generated by a single transistor. Hence, to meet the future requirements outlined in the IEEE International Roadmap for Devices and Systems, continued research of multi-gate MOSFET architectures in conjunction with low-power technologies is crucial [8]. Moving forward in the decades to come, the engineering and scaling of MOSFETs will continue to impact all facets of our

lives and society itself in both foreseen and unforeseen ways.

Therefore, the goals of this thesis and purpose of the work herein are: (i) to provide an understanding of the performance of multi-gate NC-FETs with physical non-uniformities, and (ii) to present novel design strategies for the enhancement of negative capacitance effects in such devices. This thesis is organized as follows: First, we provide a brief introduction to multi-gate FET architectures, the Boltzmann tyranny of the subthreshold swing in CMOS technologies, NC-FETs and their ability to move beyond the Boltzmann limit, followed by a summary of previous literature on negative capacitance technology in logic devices. Next, we present the Landau Theory of ferroelectric materials exhibiting negative capacitance characteristics. In addition, we discuss the simulation methodology implemented in Synopsys Sentaurus technology-aided design (TCAD) to model multi-gate NC-FETs. Finally in the body of the thesis, we present two advances in engineering the performance of NC-FETs before summarizing the conclusions and future prospects of these works.

## 1.1 Scaling and Power Consumption of Field-Effect Transistors

Since its invention the planar MOSFET architecture was the standard design fabricated in the semiconductor industry for the latter part of the twentieth and early twenty-first centuries. During this time the continued miniaturization of MOSFETs followed Dennard’s scaling, i.e., the operating voltages and the dimensions of MOSFETs, including the gate length,  $L_g$ , and oxide thickness,  $T_{ox}$ , were scaled by the same factor,  $\kappa$ , such that the electric field remained constant, as shown in Table 1.1 [9]. However, since the size of MOSFETs have entered the nano regime, i.e., below 90 nm, the operating voltages have remained relatively the same while the physical dimensions of MOSFETs continue to scale downward. The trend of MOSFET technology in recent decades is illustrated in Fig.1.1. This abandonment of Dennard’s scaling became problematic as the increase in power densities lead to a corresponding increase in the temperature of computer chips. To mitigate this effect, the frequency of processors was not increased and, as with operating voltages, has remained relatively the same in recent years [10]. To continue the trend of Moore’s law, manufactures have migrated from single-core to multi-core designs. Yet still, with the physical dimensions of MOSFETs continuing to decrease, we have past the point in MOSFET miniaturization where SCEs dominate. Without the development of new technologies MOSFETs will be unable to meet future requirements.

| Device or Circuit Parameter           | Scaling Factor |
|---------------------------------------|----------------|
| Device dimension $T_{ox}$ , $L$ , $W$ | $1/\kappa$     |
| Doping concentration $N_a$            | $\kappa$       |
| Voltage $V$                           | $1/\kappa$     |
| Current $I$                           | $1/\kappa$     |
| Capacitance $\epsilon A/t$            | $1/\kappa$     |
| Delay time/circuit $VC/I$             | $1/\kappa$     |
| Power dissipation/circuit $VI$        | $1/\kappa^2$   |
| Power density $VI/A$                  | 1              |

Table 1.1: Dennard’s scaling of MOSFET parameters. Adapted from ref. [9]

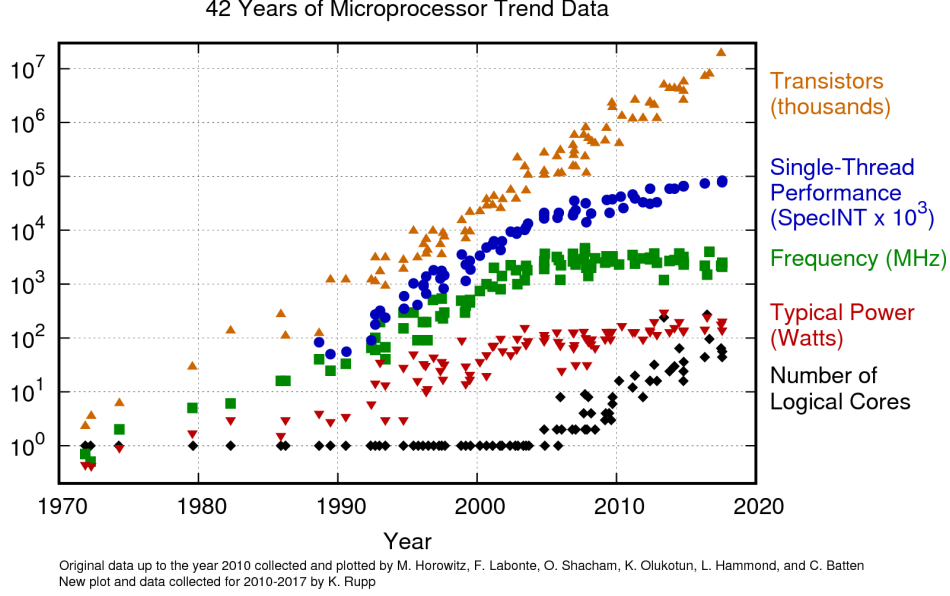


Figure 1.1: The trend of microprocessors over the last 42 years. To deal with the flattening of power consumption and clock frequency, the number of cores has recently increased to continue Moore’s Law. Taken from ref. [11]

The problem of approaching a physical limitation in the scaling of MOSFETs has been on the horizon for decades. Consequently, the twenty-first century has been marked with an exponential increase in material science and engineering research. As thickness of the gate insulator,  $T_{ox}$ , of MOSFETs decreased the gate capacitance increased, since the capacitance and thickness of the gate oxide, typically a dielectric (DE), is given by the relation  $C_{ox} \propto \epsilon_{ox}/T_{ox}$ . However, with decreasing  $T_{ox}$ , the leakage currents of MOSFETs increased, leading to a reduction in the ON-state current,  $I_{ON}$ , and overall device performance. Traditionally, silicon dioxide ( $\text{SiO}_2$ ), with its permittivity of  $\epsilon_{\text{SiO}_2} = 3.9$ , has been used as the gate oxide material in MOSFET technology. To overcome the limitations of decreasing  $T_{ox}$  when using  $\text{SiO}_2$  as the gate oxide, high- $\kappa$  materials with larger permittivities,  $\epsilon_{\kappa}$ , have been studied and used instead [12, 13]. To quantify the effectiveness of such materials in relation to  $\text{SiO}_2$  the equivalent oxide thickness, EOT, can be calculated:

$$\text{EOT} = \frac{\epsilon_{\text{SiO}_2} T_{\kappa}}{\epsilon_{\kappa}} \quad (1.1)$$

Hence, the same electrostatic characteristics of  $\text{SiO}_2$  can be achieved with high- $\kappa$  oxides at a larger  $T_{ox}$ , thereby reducing drain leakage. There are several high- $\kappa$  materials which have been extensively studied, such as hafnium dioxide ( $\text{HfO}_2$ ) and zirconium dioxide ( $\text{ZrO}_2$ ), where  $\epsilon_{\kappa} > \epsilon_{\text{SiO}_2}$ . Among these  $\text{HfO}_2$ , with its high dielectric constant, has emerged as one of the preferred gate oxide materials in MOSFET devices [14]. While the progress in material science has enabled further advancements in miniaturizing MOSFET technology, there still exist fundamental scaling limitations which need to be addressed.

## 1.2 Multi-Gate Field-Effect Transistor Structures

The conventional single-gate MOSFET transistor with dimensions in the nano regime suffers from SCEs leading to drain leakage and carrier mobility degradation, effectively lowering the drive current. To move

forward other architectures such as planar double-gate MOSFETs have been studied [15, 16]. However, to meet future computing requirements innovative three-dimensional structures have been of great interest such as FinFETs and gate-all-around (GAA) FETs, including nanowire (NW) and nanosheet (NS) FETs, which are compared in Fig.1.2.

In recent years the FinFET design has proved itself as one of the most promising architectures for succeeding planar FETs. In such a design, the channel consists of a rectangular vertical silicon fin, with height,  $H_{fin}$ , and width,  $W_{fin}$ , etched on a silicon substrate. The gate structure surrounds the channel on three sides, with the oxide deposited on the top and sides of the fin. Thus, the gate control is extended from the planar MOSFET structure with a larger effective gate width [17]. In addition, the structure of FinFET is comparably more simple to fabricate than the double-gate planar design, however, due to limitations in the etching process, fabricating a perfectly rectangular fin is difficult. Instead the result is a vertical fin with a trapezoidal shape which can lead to variations in performance [18]. As of this writing FinFETs have been implemented to the 5-nm technology node and have been fabricated commercially.

To move beyond the 5-nm node, GAA-FETs are among the contenders to succeed the FinFET architecture [19]. In particular, vertically stacked NW-FET and NS-FET structures are promising candidates for meeting future computing requirements. The GAA-FET structure consists of multiple silicon channels stacked on top of one another, where each channel, i.e., silicon wire or sheet, is surrounded by the gate insulator and metal on all sides [20]. The channels are arranged such that the gate insulator of one channel is physically separated from the channels adjacent by the gate metal. This four sided gate structure is a natural extension of the FinFET design with improved electrostatic control [21, 22]. There are two classes of GAA-FETs, namely, vertically and laterally stacked GAA-FETs, of which we will focus on the vertically stacked structure in this thesis. The GAA-FET architecture allows for a larger density of transistors since the inherent design lends itself well to scalability, since the number of stacked channels can be increased. One draw back is that the fabrication process of GAA-FETs is much more complicated than planar and FinFET architectures. Looking to the future of MOSFETs, NW/NS-FETs must be implemented to move beyond the 5-nm technology node and it is therefore of critical importance that the performance of these devices be optimized.

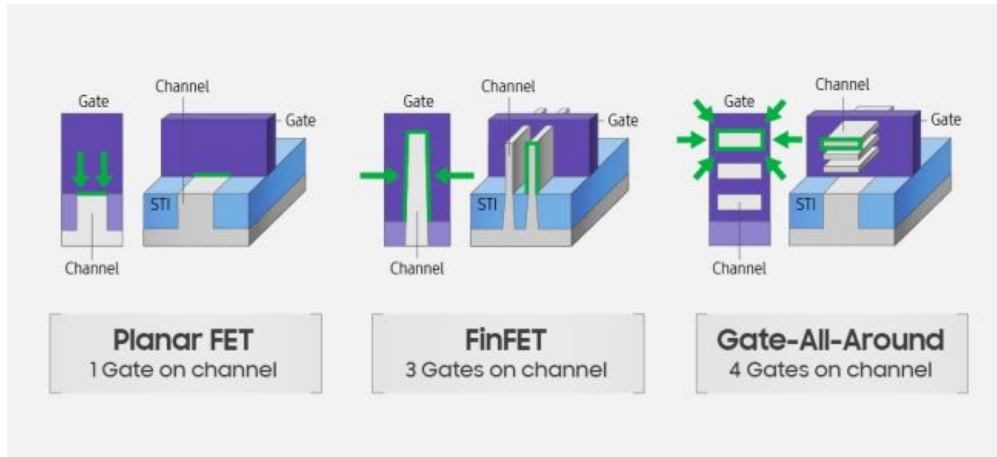


Figure 1.2: Three-dimensional structures of planar FET, FinFET and GAA-FET (NS-FET) architectures with the insulator-channel interfaces indicated. Taken from ref. [23]

### 1.3 Boltzmann Tyranny and Low Power Field-Effect Transistors

Architectures beyond planar MOSFETs, while further increasing the number of transistors on a single computer chip, do not address the fundamental problem of increased power density which impedes the ability to dissipate thermal energy generated by MOSFETs when switching between OFF and ON-states. This limit is often referred to as the Boltzmann Tyranny and has lead to an interest in so called low-power devices. Before discussing the particularities of such FETs we begin with a brief discussion on the origin of the Boltzmann limit.

#### The Boltzmann Limit

To facilitate our discussion we consider a simplified model of a planar MOSFET device, shown in Fig.1.3. The capacitance of the gate insulator is defined as,  $C_{ins}$ , and the remaining device capacitances, namely, the source-to-channel, source-to-drain, and depletion capacitances, are combined into a single quantity as,  $C_S$ . Despite the simplicity of this model it is sufficient for illustrating the fundamental limit in logic devices. Using  $Q = CV$ , the surface potential of the insulator-channel interface,  $\psi_s$ , can be written as:

$$C_S \psi_s = \left( \frac{1}{C_{ins}} + \frac{1}{C_S} \right) V_g \quad (1.2)$$

$$\Rightarrow \psi_s = \frac{C_{ins}}{C_{ins} + C_S} V_g \quad (1.3)$$

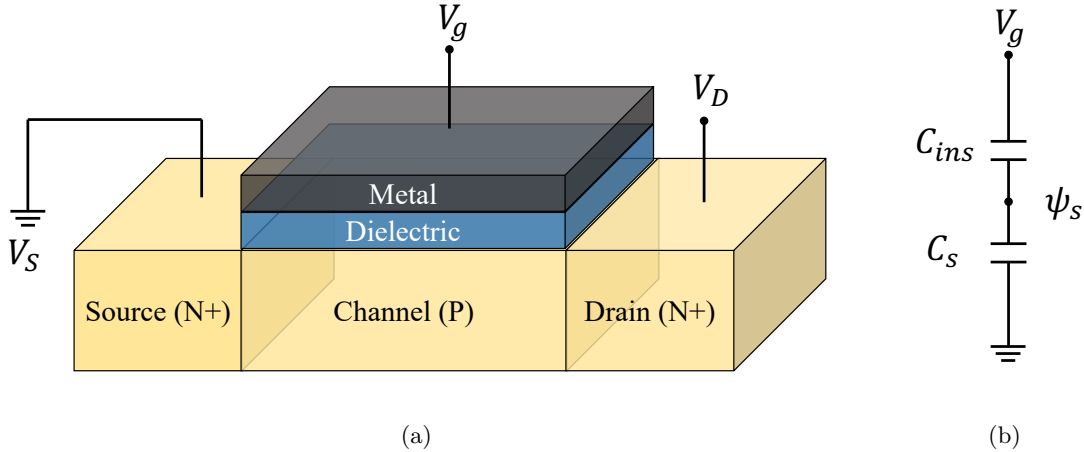


Figure 1.3: (a) Simplified planar MOSFET structure where  $I_d$  is controlled by  $V_g$ . (b) The simplified circuit schematic of the planar MOSFET places the insulator material capacitance,  $C_{ins}$ , in this case a dielectric, and the semiconductor capacitance,  $C_S$ , which includes the source-to-channel, channel-to-drain, and depletion capacitances, in series.

In the analysis of MOSFETs the subthreshold swing,  $SS$ , quantifies how sharply the transistor is turned off by a change in the gate voltage. Mathematically, it is defined as the change in gate voltage,  $V_g$ , required to change the drain-current,  $I_d$ , by one order of magnitude:

$$SS := \frac{\partial V_g}{\partial(\log_{10} I_d)} \quad (1.4)$$

Writing the  $SS$  in terms of  $\psi_s$  yields:

$$SS = \frac{\partial V_g}{\partial \psi_s} \cdot \frac{\partial \psi_s}{\partial(\log_{10} I_d)} \quad (1.5)$$

At room temperature, i.e., 300 K, the second term equates to the thermionic limit [24]:

$$\frac{\partial \psi_s}{\partial(\log_{10} I_d)} = \ln 10 \frac{kT}{q} \approx 60 \text{ mV/dec} \quad (1.6)$$

The first term, called the “body factor”,  $m$ , can be written in terms of the device capacitances. From Eqn.1.3 the body factor becomes:

$$m = \frac{\partial V_g}{\partial \psi_s} = \frac{C_{ins} + C_S}{C_{ins}} = 1 + \frac{C_S}{C_{ins}} \quad (1.7)$$

Hence, the  $SS$  of the MOSFET device is then:

$$SS = \left(1 + \frac{C_S}{C_{ins}}\right) \cdot 60 \text{ mV/dec} \quad (1.8)$$

We note for any positive value of  $C_{ins}$ , as is the case for any dielectric, the  $SS$  cannot be lower than the Boltzmann limit, namely, 60 mV/dec [25]. Even if a high- $\kappa$  material is used as the gate oxide with an extremely high capacitance the  $SS$  cannot be less than 60 mV/dec, since  $m > 1$ . How then can we move beyond this physical limit? To address the problem there has been substantial research on sub-60 mV/dec technologies, which reduce the power per switching event, enabling a transistor to achieve its ON-state current at a lower  $V_g$ .

## Negative Capacitance FETs

Low-power devices such as Tunnel FETs (TFETs), impact-ionization MOSFETs (i-MOS), negative capacitance FETs (NCFETs) are currently being studied [26]. However, TFETs exhibit a low ON-current and i-MOS devices are difficult to scale [27, 28]. On the other hand NCFETs, which incorporate a ferroelectric material into the gate structure of a CMOS device, exhibit a higher ON/OFF-current ratio,  $I_{ON}/I_{OFF}$ , for the same supply voltage,  $V_{DD}$ , compared to a conventional MOSFET. In addition, the integration of a FE layer into the gate structure is a relatively simple modification in contrast to other low-power devices since, it requires no changes in the basic transistor operation [29, 30]. Thus, given the current set of low-power FET candidates NCFETs are one of the most viable options.

The gate structure of a planar NCFET device is similar to its MOSFET counterpart. We consider a simplified NCFET structure as an extension of the model illustrated in Fig.1.3. Above the gate oxide a FE material is deposited with capacitance,  $C_{FE}$ , in addition to a metal layer such that the DE and FE are in series. See Fig.1.4. In this case, to compare with the MOSFET structure, it is convenient to define the capacitance of the MOSFET device,  $C_{MOS}$ , as the series capacitance of  $C_S$  and  $C_{DE}$ , and the gate insulator capacitance,  $C_{ins}$ , as the series capacitance of  $C_{FE}$  and  $C_{DE}$ .

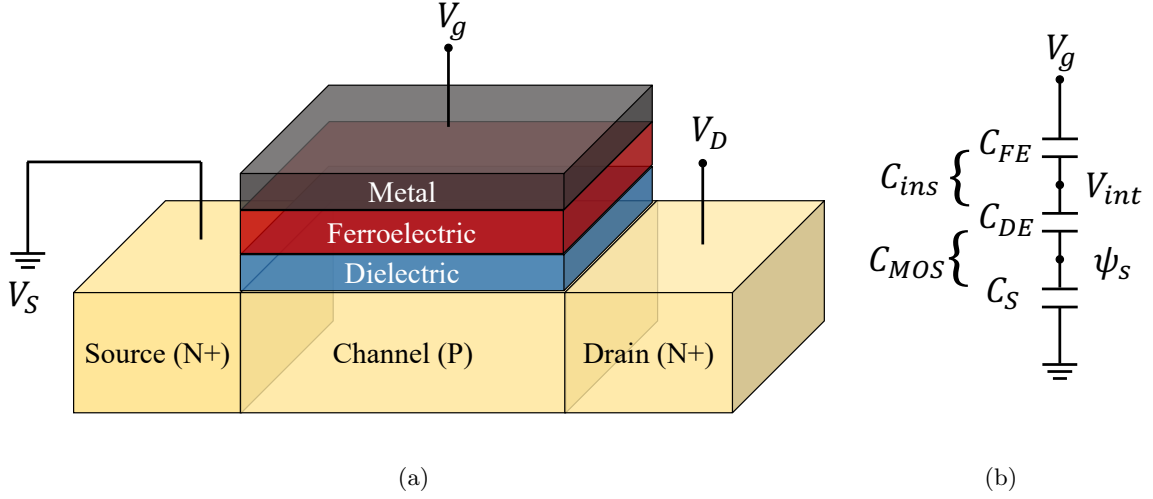


Figure 1.4: (a) Similar to Fig.1.3, a planar NCFET device with FE layer incorporated into the gate structure. This is referred to as a metal-ferroelectric-insulator-semiconductor (MFIS) structure. (b) Circuit schematic of MFIS device, where the FE and DE capacitances are in series. Using this model it is sometimes convenient to define the gate insulator capacitance,  $C_{ins}^{-1} = C_{FE}^{-1} + C_{DE}^{-1}$ , and the capacitance of the conventional MOSFET,  $C_{MOS}^{-1} = C_{DE}^{-1} + C_S^{-1}$ .

Starting from Eqn.1.8, if  $C_{ins} < 0$  then it is possible for the FET to exhibit sub-60 mV/dec behaviour [24]. If we constrain the ferroelectric capacitance to be negative, i.e.,  $C_{FE} = -|C_{FE}|$ , then we can write the insulator capacitance in terms of  $C_{FE}$  and  $C_{DE}$  as:

$$\frac{1}{C_{ins}} = \frac{1}{C_{DE}} - \frac{1}{|C_{FE}|} \quad (1.9)$$

Substituting Eqn.1.9 into Eqn.1.8 the subthreshold swing of the NCFET device becomes:

$$SS = \left( 1 + C_S \left[ \frac{1}{C_{DE}} - \frac{1}{|C_{FE}|} \right] \right) \cdot 60 \text{ mV/dec} \quad (1.10)$$

To achieve  $SS < 60 \text{ mV/dec}$  the following inequality must be satisfied:

$$\left( 1 + C_S \left[ \frac{1}{C_{DE}} - \frac{1}{|C_{FE}|} \right] \right) < 1 \quad (1.11)$$

$$\Rightarrow |C_{FE}| < C_{DE} \quad (1.12)$$

Hence, for the subthreshold swing of the NCFET device to be below the Boltzmann limit we that require two conditions are met, namely, 1)  $C_{FE} < 0$ , and 2)  $|C_{FE}| < C_{DE}$ .

For the moment we have succeed in our objective to give a brief introduction to NCFETs and illustrated how a ferroelectric layer with sufficient negative capacitance can result in  $SS < 60 \text{ mV/dec}$ . There are additional subtleties which need to be discussed in order for the full picture of NCFET to be understood.

In the following chapter we will discuss the microscopic origins of the NC effect in ferroelectric materials and the conditions under which  $C_{FE}$  can be negative and stabilized resulting in a NCFET device with sub-60 mV/dec behaviour. For the moment we simply state that negative values of  $C_{FE}$  are possible.

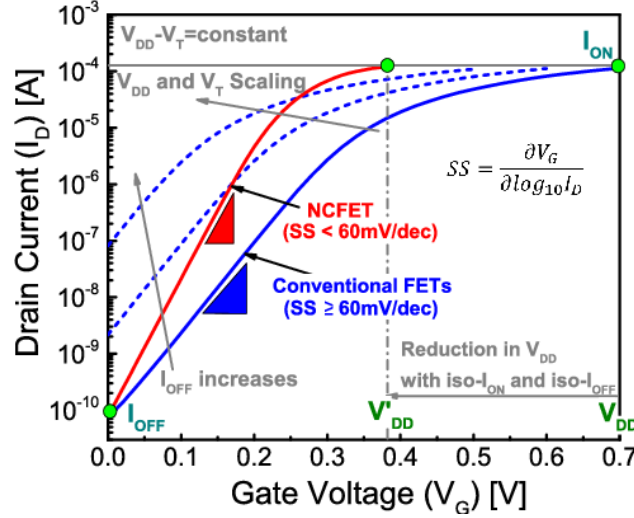


Figure 1.5:  $I_d$ - $V_g$  curves of MOSFET (blue) and NCFET (red) devices. The NC device is able to obtain the same  $I_{ON}$  as the MOSFET but at a lower  $V_g$ . Thus, the NCFET is able to switch to the ON-state at a lower supply voltage. Taken from ref. [31]

To illustrate the performance enhancement of NCFET Fig.1.5 compares the drain current vs. gate voltage ( $I_d$ - $V_g$ ) curves of a conventional MOSFET and NCFET device. In the case of MOSFET the  $SS$  is greater than the Boltzmann limit as expected, however, the NCFET device, with its added ferroelectric layer and resulting negative capacitance, has sub-60 mV/dec behaviour. The significance of this improved switching characteristic is highlighted when examining the ON-state currents of both devices. In particular, the MOSFET device with OFF-state current,  $I_{OFF} = 10^{-10}$  A, achieves its ON-current state at  $V_g = 0.7$  V, whereas the NCFET device with the same OFF-state current achieves the same ON-current as the MOSFET at a lower gate voltage  $V_g = 0.4$  V. Hence, the NCFET device is able to operate at a lower supply voltage.

## 1.4 Summary of Previous Work

Ferroelectricity is a well known phenomenon. The class of oxide materials known as perovskites, with general chemical formula ( $ABO_3$ ), are among the most studied ferroelectric materials. Barium titanate ( $BaTiO_3$ ), was one of the first perovskite oxides found to exhibit ferroelectric properties. To describe the FE phenomenon and hysteresis behaviour of  $BaTiO_3$  A.F. Devonshire, in his 1949 paper, applied Landau's theory of phase transitions to create a microscopic theory of ferroelectric materials which was able to predict experimental results. [32, 33]. The details of the Landau-Devonshire theory are discussed in the following chapter.

The NCFET concept of a ferroelectric layer integrated into the gate stack of a MOSFET device was first proposed in the seminal paper by Salahuddin and Datta in 2008 [24]. Their fundamental breakthrough was the realization that the negative capacitance state, illustrated by the dashed line within the hysteresis loop of the polarization-electric field 'S'-curve of  $BaTiO_3$  in Fig.1.6, could be stabilized with an additional

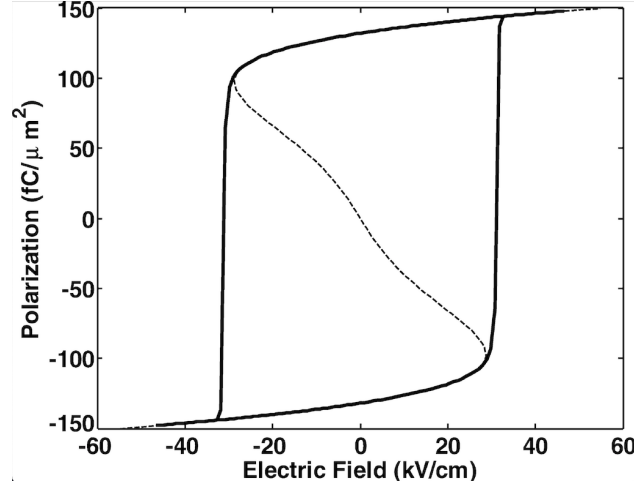


Figure 1.6: Polarization vs. electric field hysteresis loop of BaTiO<sub>3</sub>. The negative capacitance region, where  $dP/dE < 0$ , is indicated by the dashed line. This region can be stabilized if the FE material is placed in series with a normal capacitor. Taken from ref. [24]

capacitor acting in series with the ferroelectric. This coupled system would then be able to move beyond the Boltzmann limit and the FET device could achieve sub-60 mV/dec behaviour. The experimental observation of negative capacitance was later demonstrated by Khan et al. [34]. Using a ferroelectric-dielectric (FE-DE) heterostructure, composed of Pb(Zr<sub>0.2</sub>Ti<sub>0.8</sub>)O<sub>3</sub> and SrTiO<sub>3</sub>, it was found that the total capacitance of the bilayer system was greater than the capacitance of the isolated SrTiO<sub>3</sub> dielectric proving the viability of the NCFET concept as a low-power logic device technology.

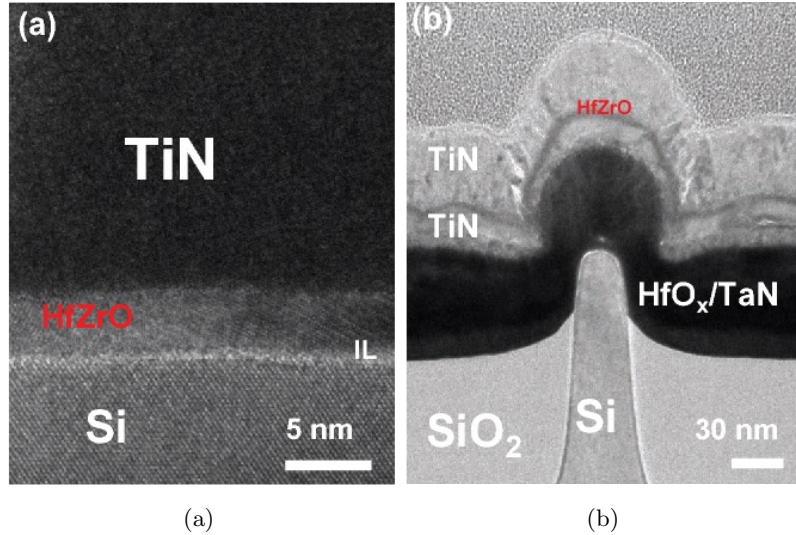


Figure 1.7: Transmission electron microscopy images of (a) planar HfZrOx capacitor and (b) NC-FinFET device with HfZrOx FE layer in the gate structure. Taken from ref. [35]

Within the past decade, ferroelectric materials have been successfully integrated into the gate structure of FETs to produce planar NCFET devices with  $SS$  below 60 mV/dec and high ON-currents [36, 37]. The

discovery of ferroelectricity in doped  $\text{HfO}_2$  has acted as a catalyst for continued research of ferroelectric materials in both memory and logic devices [24, 38]. Doped hafnium oxides have several advantages over traditional perovskite ferroelectrics such as  $\text{Pb}(\text{Zr}_{0.5}\text{Ti}_{0.5})\text{O}_3$  (PZT) and  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  (SBT). In particular, doped  $\text{HfO}_2$  is CMOS compatible since it is already commonly used as a high- $\kappa$  gate insulator in MOSFETs as previously mentioned [39]. Additionally, doped hafnium oxides lend themselves well to the scaling of FETs since they can be deposited in thin films on the order of a few nanometers (5 – 30 nm) whereas the film thicknesses of PZT and SBT are greater than (70 nm) and (25 nm) respectively [40, 41].

The first NC-FinFET device with doped  $\text{HfO}_2$  was fabricated in 2015 with a  $SS$  of 55 mV/dec and reported a 25% increase in  $I_{ON}$  compared to its non-NC analogue [35]. More recent experimental studies have shown improved steep switching behaviour for NC-FinFET and NC-GAAFET with doped  $\text{HfO}_2$  FE layer thicknesses of 5 – 5.5 nm. The average subthreshold swings reported for these devices were 38 mV/dec and 22 mV/dec respectively [42]. The  $I_d - V_g$  curves of the NC-FinFET and NC-GAAFET devices are shown in Fig.1.8.

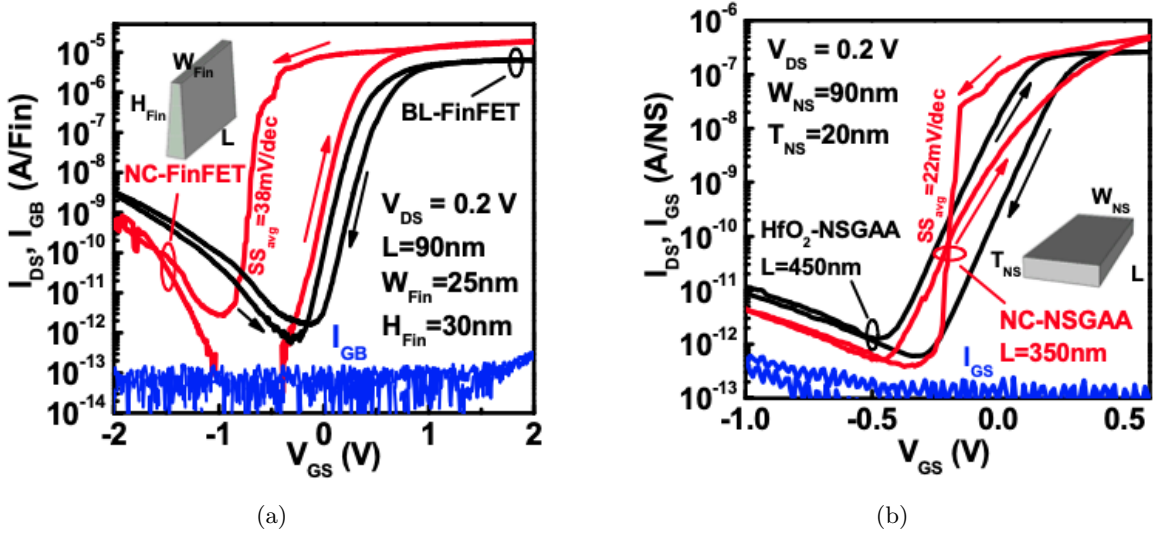


Figure 1.8: Measured  $I_d - V_g$  curves of fabricated (a) NC-FinFET and (b) NC-NSFET devices. The average  $SS$  of both devices are 38 mV/dec and 22 mV/dec. Taken from ref. [42]

Simultaneously, over the past decade several investigations have simulated the operation of NCFET devices. These works have studied ferroelectric materials and negative capacitance through the lens of Landau theory, which will be covered in Chapter 2. Many of these investigations have implemented the NCFET device structure and Landau model in Sentaurus TCAD, a commercial electron device simulation tool, which calculate the voltage across the FE layer,  $V_{FE}$ . These studies were able to accurately obtain the  $I_d - V_g$  curve and performance characteristics when compared to experimental results of NCFET devices [43]. Furthermore, the simulated dynamic behaviour was consistent with experimental results when considering different sweep times, as shown in Fig.1.9 [44].

In addition to the Landau model for ferroelectric materials an alternative model, namely, the Miller model, has been used to simulate NCFET devices [45]. The Miller model can more accurately simulate the po-

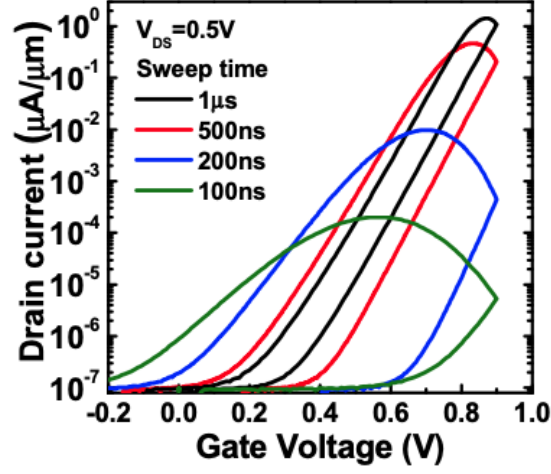


Figure 1.9: Simulated fast sweep of NCFET device with 1.5 nm FE layer. The hysteresis becomes more prominent with increasing sweep speed. Taken from ref. [44]

larization switching behaviour of the ferroelectric material and allows for polarization interactions to be considered. These studies have used non-equilibrium Green's functions, the Poisson equation, and Miller model to simulate the carrier transport, electrostatics, and spontaneous polarization respectively. Recently, the Miller model was used as a means to explain the origin of the experimentally observed critical FE thickness, i.e., where the subthreshold swing is minimized [46].

This thesis extends from contemporary works where multi-gate FET designs and FE materials are utilized to further develop and understand the optimization and engineering of NCFETs for low-power applications in the continued scaling of MOSFET technology.

## Chapter 2

# Landau Theory of Ferroelectrics and Simulation Methodology

In this chapter we discuss the theoretical background of ferroelectric materials through the lens of Landau theory to obtain a sufficient understanding of their properties as relates to semiconductor devices. First, we consider the atomic structure of an arbitrary FE material and explain how spontaneous polarization of the intrinsic ferroelectric arises. We then introduce the energy function and describe the information encapsulated within its terms which themselves depend on the polarization of the material. The Landau equation describes the time-evolution of the polarization as a function of energy and by considering the system in a state of equilibrium we can express the electric field in terms of the polarization. We then determine under what conditions FE materials exhibit negative capacitance behaviour, which can only be stabilized when coupled to a dielectric capacitor in series with the ferroelectric. The capacitance of the composite system is thus larger than the isolated DE capacitance which has been verified by experimental studies. We then illustrate how our preceding analysis can be applied to FETs where the integration of a FE layer, with negative capacitance, gives rise to an NCFET device with sub-60 mV/dec steep switching behaviour before finally discussing the simulation of FE materials in multi-gate FETs using Synopsys Sentaurus TCAD.

### 2.1 Spontaneous Polarization of Ferroelectrics

We can understand how the ferroelectricity of a material arises on a microscopic scale by using Landau Theory [32]. This phenomenological theory, which describes a systems behaviour in equilibrium near phase transitions using an order parameter, was adapted by Devonshire to FE materials where the polarization,  $\vec{P}$ , was used as the order parameter, with units  $[C/cm^2]$  [33]. We facilitate our discussion by considering the atomic structure and symmetries of an arbitrary ferroelectric unit cell with a perovskite oxide structure,  $ABO_3$ , shown in Fig.2.1a [47]. The spontaneous polarization of the perovskite oxide originates from the displacement of the body centred atom (B). In general the atom can be displaced in any direction, however, for our discussion we consider the simplest case where the atom can only be displaced along the  $\hat{z}$ -direction, i.e., the polarization is unidirectional, where  $\vec{P} = P_z \hat{z}$ . For the remainder of our discussion we will treat the polarization as a scalar quantity. In this case there exist two possible polarization states,  $-P_z$  and  $+P_z$ , where the structures are illustrated in Fig.2.1b and Fig.2.1c respectively [48]. In addition, will assume that the ferroelectric is a single domain such that all constituent unit cells of the FE region exhibit a polarization

with the same direction.

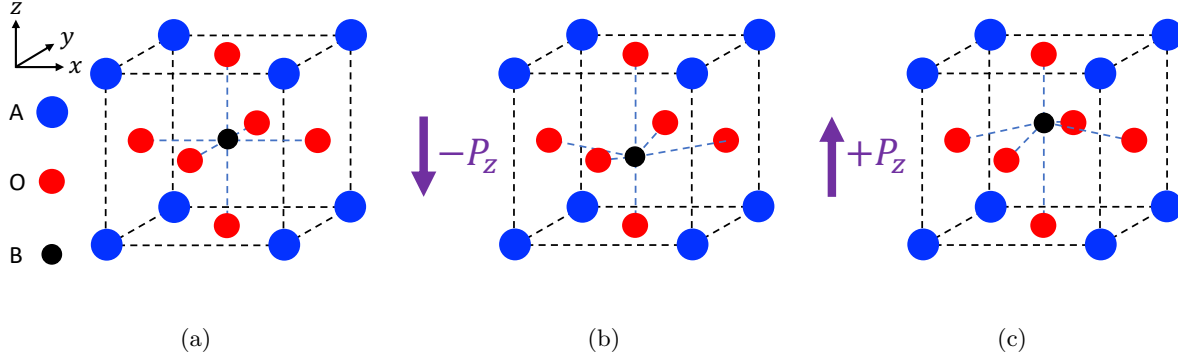


Figure 2.1: (a) An arbitrary perovskite oxide,  $\text{ABO}_3$ , unit cell where the polarization depends on the displacement of the body centred atom, B. In the simplest case of FE polarization the displacement of the atom is unidirectional leading to two polarization states, namely, (b)  $-P_z$  and (c)  $+P_z$ . Adapted from ref. [49]

### 2.1.1 The Energy Function of Ferroelectrics

In a FE material the spontaneous polarization states  $-P_z$  and  $+P_z$ , shown in Fig.2.1b and Fig.2.1c, correspond to states of minimum energy. In addition, no displacement in B, equivalent to  $P_z = 0$ , corresponds to a state of localized energy maximum, i.e., a saddle point. The free energy density of the intrinsic ferroelectric material can be written as a Taylor series expansion of even powers of  $P$ , as a consequence of symmetry arguments [50]. It is sufficient to expand the free energy function to  $\mathcal{O}(P^6)$ :

$$\mathcal{F}_{\text{free}}(P) = \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 \quad (2.1)$$

The parameters,  $\alpha$ ,  $\beta$ , and  $\gamma$  are material dependent constants known as the Landau coefficients, with units  $[\text{cm}/\text{F}]$ ,  $[\text{cm}^5/\text{FC}^2]$ , and  $[\text{cm}^9/\text{FC}^4]$  respectively, which are determined experimentally. The coefficients  $\beta$  and  $\gamma$  are temperature independent, however,  $\alpha$  is related to temperature by way of the following equation:

$$\alpha = \alpha_0(T - T_C) \quad (2.2)$$

The constant  $\alpha_0 > 0$  is a material parameter and  $T_C$  is the Curie temperature. When  $T < T_C$  the result is  $\alpha < 0$ . In this case the free energy function of the material manifests a double-well landscape with two local minima reflecting polarization states  $P = \pm P_z$ , as illustrated in Fig.2.2. Hence, for  $\alpha < 0$  spontaneous polarization switching can take place and the material exhibits FE behaviour [51]. On the other hand, if  $T > T_C$  then  $\alpha > 0$ , which results in an energy landscape with positive convexity and only one minimum, also shown in Fig.2.2. The stabilized polarization state is  $P_z = 0$ , meaning no spontaneous polarization can take place and the material displays no ferroelectricity [47]. The FE materials which have been used in the gate structure of NCFETs have a  $T_C$  sufficiently above room temperature so they will exhibit ferroelectric behaviour [39].

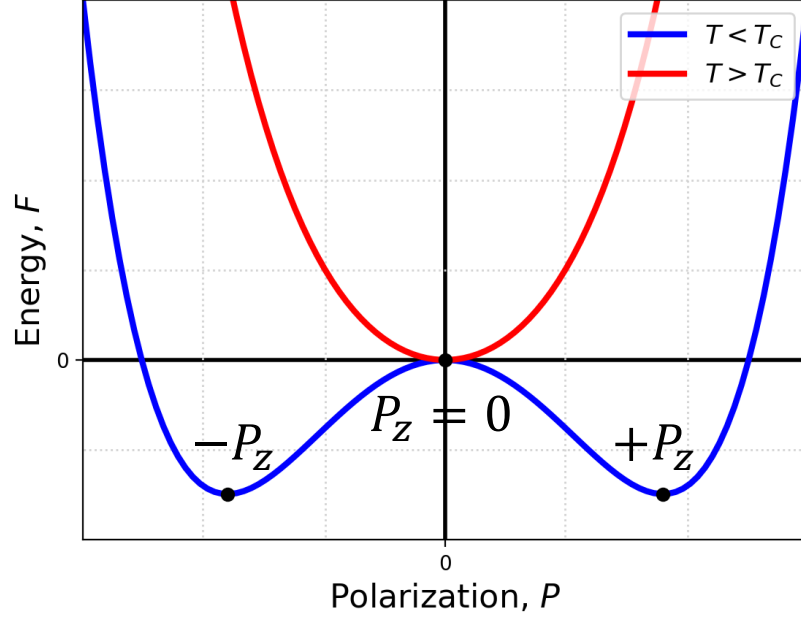


Figure 2.2: Free energy landscape as a function of polarization.  $T < T_C$  yields  $\alpha < 0$  and the energy landscape is a double-well profile (blue) where spontaneous switching can occur, and the material behaves as a ferroelectric.  $T > T_C$  yields  $\alpha > 0$  where the energy function (red) has only one minimum and the material does not exhibit ferroelectric properties.

In addition to the free energy of the intrinsic material, Landau theory can also account for other terms which incorporate electric field interactions. We consider the interaction of an electric field,  $E_{FE}$ , with units [V/cm]. This electrostatic energy density can be expressed as [39, 52]:

$$\mathcal{F}_{\text{elec}}(P) = -E_{FE} \cdot P \quad (2.3)$$

In general, there may exist spatial variations in the polarization, i.e.,  $P$  may be non-uniform, resulting in a gradient energy density, which contains information regarding the coupling between unit cells. This gradient energy density can be written in general terms as [53]:

$$\mathcal{F}_{\text{grad}}(P) = g_x \left( \frac{\partial P}{\partial x} \right)^2 + g_y \left( \frac{\partial P}{\partial y} \right)^2 + g_z \left( \frac{\partial P}{\partial z} \right)^2 \quad (2.4)$$

The coupling parameters,  $g_x$ ,  $g_y$ , and  $g_z$  are called the gradient coefficients along the  $\hat{x}$ ,  $\hat{y}$ , and  $\hat{z}$  directions respectively, with units  $[\text{cm}^3/\text{F}]$  [54]. The total energy density can be expressed as the sum of Eqn.2.1, Eqn.2.3, and Eqn.2.4:

$$\mathcal{F}_{\text{total}}(P) = \mathcal{F}_{\text{free}}(P) + \mathcal{F}_{\text{elec}}(P) + \mathcal{F}_{\text{grad}}(P) \quad (2.5)$$

$$= \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 - E_{FE} \cdot P \quad (2.6)$$

$$+ g_x \left( \frac{\partial P}{\partial x} \right)^2 + g_y \left( \frac{\partial P}{\partial y} \right)^2 + g_z \left( \frac{\partial P}{\partial z} \right)^2 \quad (2.7)$$

In our discussion we have considered the case where the polarization is unidirectional along the  $\hat{z}$ -direction. Hence, the total energy density function becomes [47, 49]:

$$\boxed{\mathcal{F}_{\text{total}}(P) = \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 - E_{FE} \cdot P + g_z \left( \frac{\partial P}{\partial z} \right)^2} \quad (2.8)$$

### 2.1.2 The Landau–Khalatnikov Equation

To model the time-evolution of the spontaneous polarization, the Landau–Khalatnikov (L-K) equation, or simply called the Landau equation, is used [52]:

$$\boxed{\rho \frac{\partial P}{\partial t} + \frac{\partial \mathcal{F}(P)}{\partial P} = 0} \quad (2.9)$$

The parameter  $\rho$  is the viscosity coefficient, with units  $[\Omega \cdot \text{cm}]$ . Substituting the expression for the total energy function (Eqn.2.8) into the L-K equation (Eqn.2.9):

$$\rho \frac{\partial P}{\partial t} + \frac{\partial}{\partial P} \left[ \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 - E_{FE} \cdot P + g_z \left( \frac{\partial P}{\partial z} \right)^2 \right] = 0 \quad (2.10)$$

$$\implies \rho \frac{\partial P}{\partial t} + \alpha P + \beta P^3 + \gamma P^5 - E_{FE} - 2g_z \frac{\partial^2 P}{\partial z^2} = 0 \quad (2.11)$$

### Static Behaviour

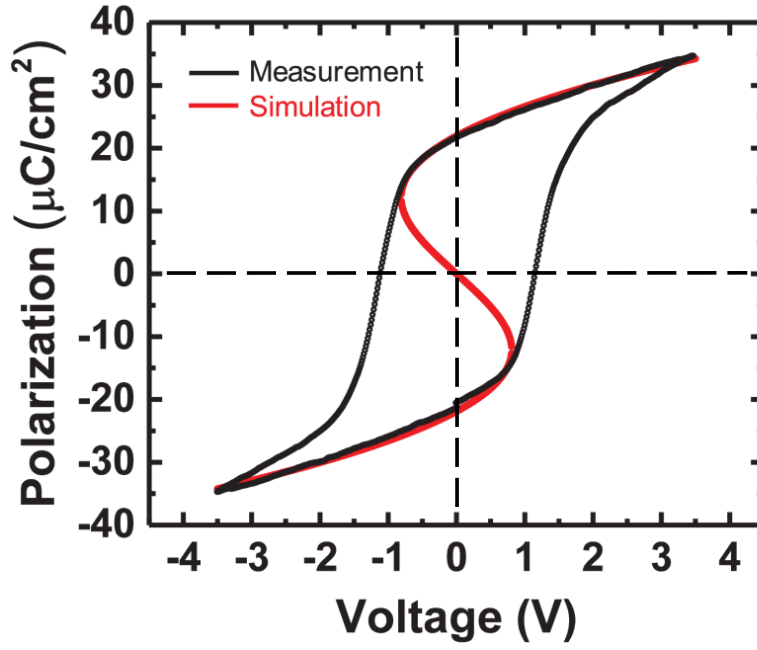
Under the quasi-static condition,  $\partial P / \partial t = 0$ , which corresponds to a state of thermal equilibrium, we obtain an expression for the electric field as a function of the polarization [55]:

$$E_{FE}(P) = \alpha P + \beta P^3 + \gamma P^5 - 2g_z \frac{\partial^2 P}{\partial z^2} \quad (2.12)$$

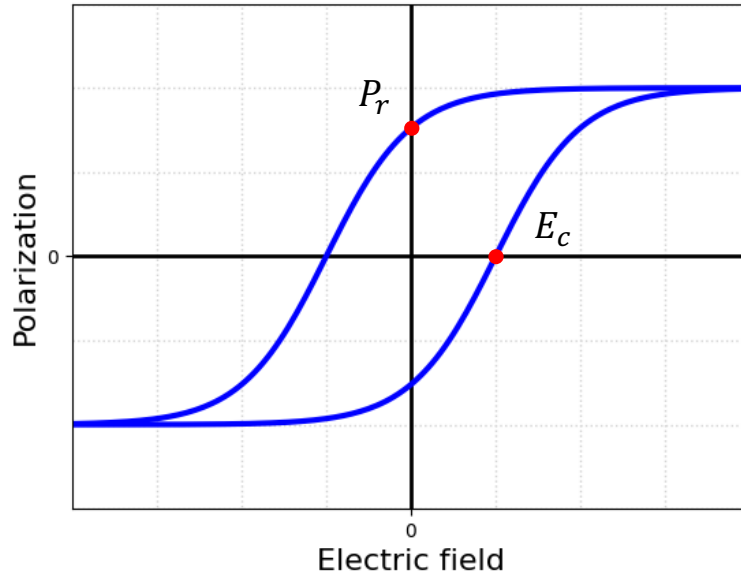
In the simplest case where we assume there is a uniform polarization, i.e.,  $\mathcal{F}_{\text{grad}} = 0$ , then the electric field becomes [39]:

$$\boxed{E_{FE}(P) = \alpha P + \beta P^3 + \gamma P^5} \quad (2.13)$$

Using Eqn.2.13 we can apply the Landau theory for FE materials toward understanding negative capacitance. First, we examine the relationship between  $E_{FE}$  and  $P$  in more detail.



(a)



(b)

Figure 2.3: (a) Polarization vs. Voltage comparison of Landau equation ‘S’-curve and experimental hysteresis result. Taken from ref. [56] (b) Hysteresis curve where the remnant polarization,  $P_r$ , and coercive electric field,  $E_c$ , are indicated.

The predicted polarization vs. voltage ( $P$ - $E$ ) ‘S’-curve from Eqn.2.13 is shown in Fig.2.3a along with the experimental hysteresis curve. In a hysteresis curve the electric field at  $P = 0$  is defined as the coercive electric field  $E_c$ , which is the magnitude of the electric field required to switch the polarization state. Similarly, the polarization at  $E = 0$  is the remnant polarization  $P_r$ , i.e., the amount of polarization which remains after the electric field has been removed. Both are shown in Fig.2.3b. For a sufficiently large electric field the polarization becomes saturated,  $P_s$  [56].

For a ferroelectric material undergoing a second-order (continuous) phase transition,  $\beta > 0$  and  $\gamma = 0$ , as opposed to a first-order (discontinuous) phase transition,  $\beta < 0$  and  $\gamma > 0$  [51]. In the case of second-order phase transitions the Landau coefficients  $\alpha$  and  $\beta$  can be calculated from experimental values of  $E_c$  and  $P_r$  using [57]:

$$\alpha = -\frac{3\sqrt{3}}{2} \frac{E_c}{P_r} \quad (2.14)$$

$$\beta = \frac{3\sqrt{3}}{2} \frac{E_c}{P_r^3} \quad (2.15)$$

## Dynamic Behaviour

In the above discussion leading to Eqn.2.13 we invoked the quasi-static condition. Now as a self-contained discussion we consider the case of dynamic behaviour where  $\partial P/\partial t \neq 0$ . Once again assuming there is a uniform polarization, i.e.,  $\mathcal{F}_{grad} = 0$ , then the electric field becomes [58]:

$$E_{FE} - \rho \frac{\partial P}{\partial t} = \alpha P + \beta P^3 + \gamma P^5 \quad (2.16)$$

In the case of dynamic behaviour the equivalent circuit model of the ferroelectric consists of a resistor,  $R_{FE}$ , and capacitor,  $C_{FE}$ , in series as shown in Fig.2.4a. The voltage drop across the resistor and capacitor is  $V_{R_{FE}}$  and  $V_{C_{FE}}$  respectively, where  $V_{FE} = V_{R_{FE}} + V_{C_{FE}}$ . Using  $E_{FE} = V_{FE}/T_{FE}$ , where  $T_{FE}$  is the thickness of the ferroelectric material and  $A_{FE}$  is the FE area, the  $P - V_{FE}$  relation can be written as:

$$V_{FE} - \rho T_{FE} \frac{\partial P}{\partial t} = T_{FE} (\alpha P + \beta P^3 + \gamma P^5) \quad (2.17)$$

$$\Rightarrow V_{FE} - \underbrace{\left( \rho \frac{T_{FE}}{A_{FE}} \right) \cdot \left( A_{FE} \frac{\partial P}{\partial t} \right)}_{V_{R_{FE}}} = T_{FE} (\alpha P + \beta P^3 + \gamma P^5) \quad (2.18)$$

Where  $\rho T_{FE}/A_{FE}$  is the resistance,  $R_{FE}$ , and  $A_{FE} \partial P/\partial t$  is the displacement current due to polarization switching. Hence, the entire term is the voltage drop across the resistor,  $V_{R_{FE}}$ . In addition, the voltage drop across the capacitor,  $V_{C_{FE}}$ , is:

$$V_{C_{FE}} = T_{FE} (\alpha P + \beta P^3 + \gamma P^5) \quad (2.19)$$

Fig.2.4b plots the  $P - V_{C_{FE}}$  ‘S’-curve, where  $C_{FE} < 0$  when  $dP/dV_{C_{FE}} < 0$ , along with the  $P - V_{FE}$  curves

for different frequencies. At higher frequencies the current increases causing the voltage drop across the resistor to increase. Thus, the hysteresis of the  $P - V_{FE}$  curve increases with increasing frequency.

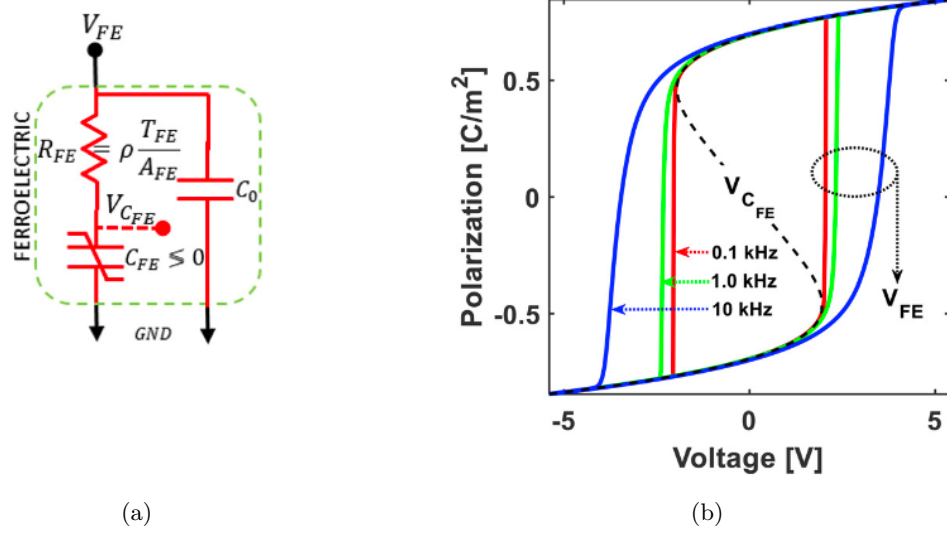


Figure 2.4: (a) Equivalent circuit model of ferroelectric capacitor in the case of dynamic behaviour. (b)  $P - V_{FE}$  curve (solid lines) for different frequencies and  $P - V_{C_{FE}}$  curve (dashed line). Taken from ref. [58]

## 2.2 Capacitance of Ferroelectrics

In the first chapter we briefly covered the capacitance of the gate insulator in MOSFET devices. We saw that for a DE material, with large  $C_{DE}$ , the subthreshold swing would improve. In addition, for a NCFET device we can achieve sub-60 mV/dec  $SS$  if the capacitance of a ferroelectric material is negative. We will now see how negative capacitance states can manifest in a FE material, and how we can stabilize the NC state through a coupled ferroelectric-dielectric heterostructure.

### 2.2.1 Negative Capacitance of Isolated Ferroelectrics

From Eqn.2.13 we can obtain the voltage across the ferroelectric as a function of polarization, since  $V_{FE} = T_{FE} E_{FE}$ , where  $T_{FE}$  is the thickness of the ferroelectric [59, 60]:

$$V_{FE}(P) = \alpha T_{FE} P + \beta T_{FE} P^3 + \gamma T_{FE} P^5 \quad (2.20)$$

The polarization vs. voltage ( $P - V_{FE}$ ) curve, or ‘S’-curve, for different values of  $T_{FE}$  is shown in Fig.2.5. As mentioned in the introduction chapter the  $P - V_{FE}$  curve obtained from experimental results of an isolated ferroelectric material displays hysteresis. The region where  $dP/dV_{FE} < 0$  corresponds to a state of negative capacitance for which an isolated FE is not stable.

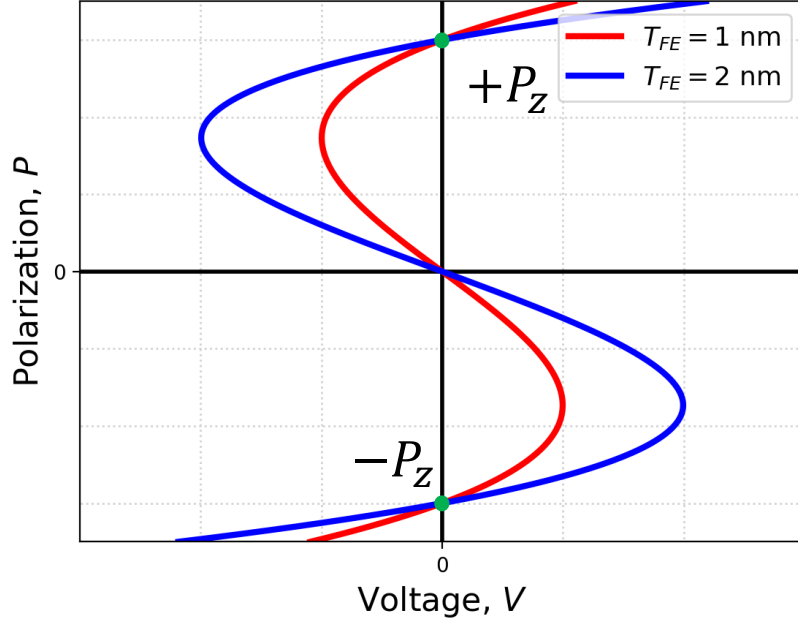


Figure 2.5:  $P$  vs.  $V_{FE}$  curve for  $T_{FE} = 1$  nm (red) and 2 nm (blue). The two extrema indicated reflect  $\pm P_z$  polarization states. Landau theory states, when  $dP/dV_{FE} < 0$  the FE is in a state of negative capacitance.

Writing the polarization in terms of charge,  $P = QA$ , where  $A$  is defined to be the unit area, we can rewrite  $V_{FE}$  in terms of  $Q$  [39, 59]:

$$V_{FE} = \alpha T_{FE} Q + \beta T_{FE} Q^3 + \gamma T_{FE} Q^5 \quad (2.21)$$

Using  $V_{FE}$  we can obtain the capacitance from the inverse of the derivative of voltage with respect to charge,  $C_{FE} = (dV_{FE}/dQ)^{-1}$ . Alternatively the capacitance can be calculated using  $C_{FE} = [\partial^2 U / \partial Q^2]^{-1}$  [47]:

$$\frac{dV_{FE}}{dQ} = \alpha T_{FE} + 3\beta T_{FE} Q^2 + 5\gamma T_{FE} Q^4 \quad (2.22)$$

$$\Rightarrow C_{FE} = \frac{1}{T_{FE} (\alpha + 3\beta Q^2 + 5\gamma Q^4)} \quad (2.23)$$

The capacitance vs. charge ( $C_{FE} - Q$ ) curves for the FE material with  $\alpha > 0$  and  $\alpha < 0$  are plotted in Fig.2.6. For the case where  $\alpha < 0$  there exists a capacitance region where  $C_{FE} < 0$  as expected. Comparing the energy curve of the intrinsic ferroelectric in Fig.2.2 with negative  $\alpha$ , i.e.,  $T < T_C$ , the regions of positive and negative capacitance correspond to regions where the convexity of  $\mathcal{F}_{\text{free}}(P)$  is positive and negative respectively [50].

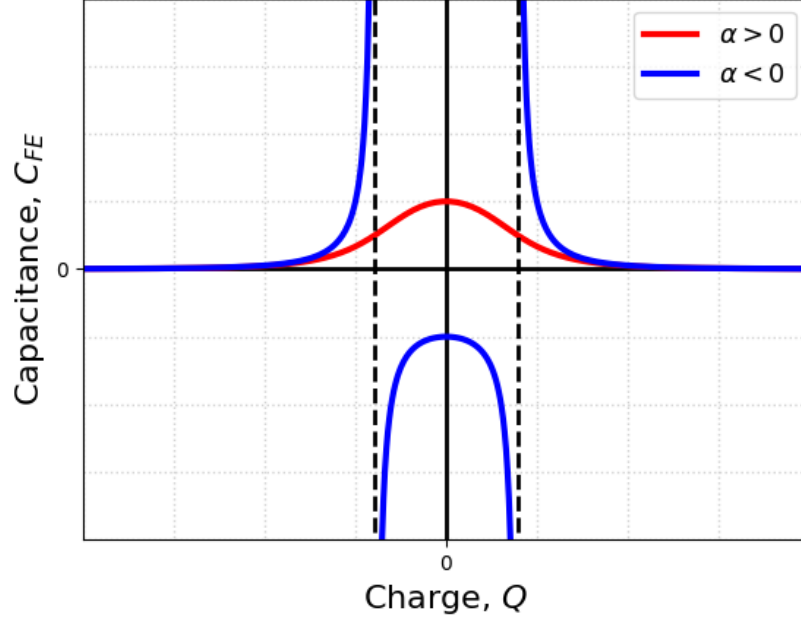


Figure 2.6:  $C_{FE} - Q$  curves for  $\alpha > 0$  (red) and  $\alpha < 0$  (blue). In the case when  $\alpha < 0$  there exists a region where  $C_{FE} < 0$ .

Thus, for an isolated ferroelectric system, an NC state is possible in accordance with Landau theory, however, in experiment this state is unstable [56]. So, the question arises: how can we stabilize the negative capacitance of an FE material?

### 2.2.2 FE-DE Bilayer Capacitance Stabilization

To achieve stability the ferroelectric material must be coupled to a system with a positive capacitance such that the capacitance of the composite system is greater than zero. We consider a FE-DE bilayer with individual capacitances  $C_{FE}$  and  $C_{DE}$  respectively [57]. The simplified circuit model is illustrated in Fig.2.7. The total series capacitance can be obtained in the usual manner:

$$C_T^{-1} = C_{DE}^{-1} + C_{FE}^{-1} \quad (2.24)$$

$$\implies C_T = \frac{C_{DE}C_{FE}}{C_{DE} + C_{FE}} \quad (2.25)$$

If we plot the total capacitance of the coupled FE-DE system vs. the ferroelectric capacitance ( $C_T - C_{FE}$ ) we can see how the capacitance of the dielectric in series with the ferroelectric layer stabilizes  $C_{FE}$ . As the capacitance of the ferroelectric layer is varied three  $C_T$  regions of interest exist, as shown in Fig.2.7. In the case of  $C_{FE} > 0$ , i.e., region ‘A’, we see that  $C_T$  of the heterostructure is less than  $C_{DE}$  as expected, since the ferroelectric will behave as a normal capacitor when  $C_{FE} > 0$ . Within the context of logic devices if the capacitance of the material is positive it should be as large as possible to enhance performance, therefore, region ‘A’ is undesirable. Furthermore, for  $C_{FE} > 0$  steep switching behaviour is impossible. In

region ‘B’, the interval of negative capacitance where,  $0 < |C_{FE}| < C_{DE}$ , yields a bilayer system with a negative total capacitance, and thus the purpose of the dielectric capacitor is void since the entire FE-DE system is unstable. Finally, in region ‘C’ where the ferroelectric capacitance is positive and its magnitude is greater than that of the isolated dielectric, i.e.,  $|C_{FE}| > C_{DE}$ , the total capacitance of the system is positive and greater than  $C_{DE}$  [61]. Thus, the coupled ferroelectric-dielectric system is stabilized and results in a capacitance enhancement ( $C_T > C_{DE}$ ) in region ‘C’.

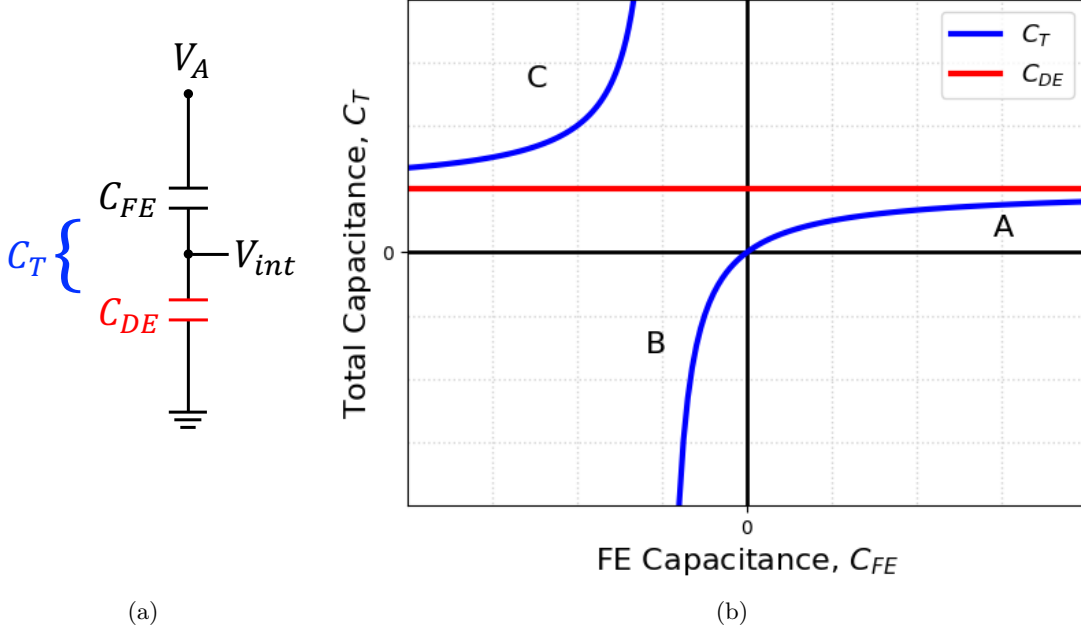


Figure 2.7: (a) Circuit diagram of FE-DE bilayer heterostructure in series. (b)  $C_T$ - $C_{FE}$  plot. Regions ‘A’ and ‘B’ result in series capacitances which are less than  $C_{DE}$  and therefore undesirable. Region ‘C’ produces a capacitance improvement ( $C_T > C_{DE}$ ) when  $C_{FE} < 0$  and  $|C_{FE}| > C_{DE}$ . Adapted from ref. [61]

## 2.3 Design Considerations of NCFETs

We now move beyond the FE-DE bilayer system and reconsider an NCFET device. Based on our preceding discussion of Landau theory and negative capacitance of ferroelectrics we are now able to provide a more in-depth treatment of our discussion of NCFET than was possible in Chapter 1. In particular, we will determine the range of  $C_{FE}$  such that the total device capacitance will be stable and sub-60 mV/dec behaviour achieved. This criteria will serve as a “design space” for  $C_{FE}$  where the NCFET attains stable steep switching behaviour.

Starting with the circuit diagram in Fig.1.4 recall:

$$\frac{1}{C_{MOS}} = \frac{1}{C_S} + \frac{1}{C_{DE}} \quad (2.26)$$

$$\Rightarrow C_{MOS} = \frac{C_S C_{DE}}{C_S + C_{DE}} \quad (2.27)$$

Using Eqn.2.27 we can define the voltage drop across the ferroelectric-dielectric interface,  $V_{int}$ , as:

$$C_{MOS} V_{int} = \left( \frac{1}{C_{FE}} + \frac{1}{C_{MOS}} \right) V_g \quad (2.28)$$

$$\Rightarrow V_{int} = \frac{C_{FE}}{C_{FE} + C_{MOS}} V_g \quad (2.29)$$

Writing the  $SS$  in terms of  $V_{int}$  and  $\psi_s$  we obtain:

$$SS = \frac{\partial V_g}{\partial V_{int}} \cdot \frac{\partial V_{int}}{\partial \psi_s} \cdot \frac{\partial \psi_s}{\partial (\log_{10} I_d)} \quad (2.30)$$

Once again, the third term is the thermionic limit of 60 mV/dec and the second term is equivalent to the body factor from the MOSFET analysis. Using Eqn.2.29, we can define the “voltage amplification factor” of the FE layer as,  $A_V = \partial V_{int} / \partial V_g$  [39]. At this point in our calculations we must constrain the ferroelectric capacitance to be negative, i.e.,  $C_{FE} = -|C_{FE}|$ , else the FE-DE gate stack will certainly result in  $SS > 60$  mV/dec. In this case, the first term becomes [62]:

$$A_V = \frac{\partial V_{int}}{\partial V_g} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \quad (2.31)$$

$$\Rightarrow \frac{1}{A_V} = 1 - \frac{C_{MOS}}{|C_{FE}|} \quad (2.32)$$

Hence, the  $SS$  of the NCFET device can be written in a similar form to Eqn.1.8:

$$SS = \underbrace{\left( 1 - \frac{C_{MOS}}{|C_{FE}|} \right)}_{1/A_V < 1} \cdot \underbrace{\left( 1 + \frac{C_S}{C_{DE}} \right)}_{m > 1} \cdot 60 \text{ mV/dec} \quad (2.33)$$

Simplifying the first two terms we retrieve Eqn.1.10:

$$\boxed{SS = \left( 1 - C_S \left[ \frac{1}{|C_{FE}|} - \frac{1}{C_{DE}} \right] \right) \cdot 60 \text{ mV/dec}} \quad (2.34)$$

From this analysis we have defined  $A_V$ , which was not present in our discussion in Chapter 1. Essentially, the values of  $m$  and  $A_V$  determine whether the device exhibits sub-60 mV/dec switching characteristics. For steep switching behaviour to exist the inequality,  $m/A_V < 1$ , must hold true. At the same time, the voltage amplification must be small enough such that  $SS > 0$ , otherwise the total capacitance of NCFET will be unstable, i.e.,  $C_{NCFET}^{-1} = C_{FE}^{-1} + C_{DE}^{-1} + C_S^{-1} < 0$  [30]. The explicit conditions are:

$$0 < \frac{1}{A_V} \cdot m < 1 \quad (2.35)$$

$$\Rightarrow 0 < \left( 1 - C_S \left[ \frac{1}{|C_{FE}|} - \frac{1}{C_{DE}} \right] \right) < 1 \quad (2.36)$$

$$\Rightarrow \boxed{C_{MOS} < |C_{FE}| < C_{DE}} \quad (2.37)$$

Therefore, in addition to the condition that 1)  $C_{FE} < 0$ , we also have the constraints that 2)  $|C_{FE}| < C_{DE}$  for the NCFET device to exhibit  $SS < 60$  mV/dec, and 3)  $C_{MOS} < |C_{FE}|$  to enforce  $SS > 0$  [50]. These conditions serve as design requirements on the possible values of  $C_{FE}$  to ensure that the NCFET device is an improvement over its MOSFET counterpart. We determined from our overview of Landau theory and negative capacitance that the ferroelectric thickness and temperature are critical parameters for controlling  $C_{FE}$  and the behaviour of NCFET. In particular, from Eqn.2.23, an increase in  $T_{FE}$  decreases  $C_{FE}$ , thereby increasing  $A_V$  and improving the device's subthreshold characteristics [39].

## 2.4 Simulation of Ferroelectrics in Sentaurus

Now that we have a sufficient overview of Landau theory, negative capacitance of ferroelectric materials, and their relation to the design of NCFETs, we are now in a position to discuss the implementation of the Landau model for FE materials in Sentaurus TCAD. General details of the device structures and simulation methodologies used in Chapter 3 and 4 are covered in Appendix A.

In Sentaurus Structure Editor (SDE), to deposit a ferroelectric material or region the usual syntax for the creation of a material or region is used. The important difference is in the name of the material which is defined. In general for any FE, the material name **InsulatorX** is used [63]. The specific material and Landau equation parameters then are defined in a parameter file. In our simulations, as previously mentioned, we shall consider second-order continuous phase transitions for the remainder of our discussion. We define the parameters of our FE material, shown in Table 2.1, using the coercive field (1 MV/cm) and polarization (12  $\mu\text{C}/\text{cm}^2$ ). From [64] we can calculate the Landau coefficients using Eqn.2.14 and Eqn.2.15.

| Parameter | Value                  | Units                               |
|-----------|------------------------|-------------------------------------|
| $\alpha$  | $-2.16 \times 10^{11}$ | cm/F                                |
| $\beta$   | $1.5 \times 10^{21}$   | cm <sup>5</sup> /(FC <sup>2</sup> ) |
| $\gamma$  | 0.0                    | cm <sup>9</sup> /(FC <sup>4</sup> ) |
| $g$       | $1.0 \times 10^{-2}$   | cm <sup>3</sup> /F                  |
| $\rho$    | $1.0 \times 10^2$      | $\Omega \cdot \text{cm}$            |

Table 2.1: L-K equation parameters specified in Sentaurus TCAD. Adapted from ref. [64]

To implement the Landau physics model for an FE material the keyword **FEPolarization** must be included in the region-wise or material-wise “Physics Sections” of the Sentaurus Device (SDevice) command file. In addition, the polarization direction in the **FEPolarization** statement must be specified [63]. For example:

```
Physics (Region="REGION_NAME") {FEPolarization( direction="z" )}
```

In this case, "z" is defined as the polarization component that is accounted for in the Landau model. The direction of spontaneous polarization can take only x, y, or z as its parameter. In an NCFET device the polarization switching direction needs to be defined as perpendicular to the channel surface for the FE layer to be effective. To model multi-gate NCFET structures different ferroelectric regions are defined, where each region has its polarization direction specified separately. For example, in the case of a FinFET architecture three FE regions are created such that the polarization directions are normal to each surface.

In addition to activating the L-K equation in the Physics section, for the equation to be solved **FEPolarization** must be included in Solve section [\[54\]](#). For example:

```
Coupled{ Poisson Electron Hole FEPolarization }
```

This solves the coupled Poisson, carrier continuity, and Landau equations self-consistently. The further details of the Solve section in the SDevice command file are discussed in Appendix A.

## Chapter 3

# Engineering a Tapered Fin and FE Layer for NC-FinFETs

### 3.1 Background

NCFETs, with their ferroelectric layer exhibiting negative capacitance, are an area of active research. Their sub-60 mV/dec subthreshold behaviour and improved ON/OFF-current ratio make NCFETs ideally suited for low-power applications [24, 29, 30, 47, 49, 61]. Unlike other steep switching devices, exhibiting an  $SS$  below 60  $mV/dec$ , the incorporation of a FE layer between the DE and gate metal in a planar MOSFET design is a relatively simple modification, which has been incorporated using contemporary CMOS fabrication techniques [65, 31, 66]. Depositing an NC layer in a three-dimensional gate structure, such as FinFET, however, presents difficulties in the fabrication process. In particular, achieving a fin of uniform width and a uniformly deposited FE layer is complicated [67, 68, 50]. Hence, a performance assessment of geometric variation in the fin and FE structures is required to guide future experiments. Previous studies have investigated geometric variations in the fin structure of FinFET devices, [69, 70, 71, 72], however, an understanding of such variations in the fin and FE layer of an NC-FinFET device is lacking. In this chapter, for the first time, multiple configurations with non-uniform fin widths and FE thicknesses in an NC-FinFET device are investigated using Sentaurus TCAD.

The remainder of this chapter is organized as follows: In Section 3.2 we discuss the nominal NC device and the physical models incorporated into our simulations. In Section 3.3 we study the characteristics of an NC-FinFET device with non-uniform fin width and uniformly deposited FE layer. Next, a non-uniform FE thickness with an ideal rectangular-shaped fin is studied to elucidate how such FE layers effect device performance. Finally, we provide a general performance assessment of the tapered NC-FinFET device by examining cases of independent and simultaneous changes in fin width and FE thickness, thereby gaining insight into the impact resulting from tapered fins and FEs. Furthermore, such an analysis allows us to propose optimized fin and FE geometries for different target performances. Finally, the conclusions of this investigation are presented in Section 3.4.

## 3.2 Methodology

Sentaurus TCAD is used to simulate the design and operation of the NC-FinFET device. The Landau-Khalatnikov and Poisson equations are solved simultaneously, and mobility degradation along with FE polarization models are implemented [73]. In this research, the device parameters are based on the low power 8-/7 nm technology node from the IEEE International Roadmap for Devices and Systems [74]. The fin and FE thicknesses in the idealized case, i.e., rectangular fin and FE geometry, are 6 nm and 2 nm respectively. The height of the fin is 42 nm, and the gate length is 16 nm. Source and drain doping were defined as  $2 \times 10^{20} \text{ cm}^{-3}$  and the body doping was set to  $1 \times 10^{18} \text{ cm}^{-3}$ . Detailed device parameters are summarized in Table 3.1 along with a three-dimensional TCAD rendering in Fig.3.1a, and a cross-sectional view of the NC-FinFET device structure with tapered fin and FE in Fig.3.1b, where significant device parameters are indicated.

| Parameter                             | Value                        |
|---------------------------------------|------------------------------|
| Fin Height ( $H_{fin}$ )              | 42 nm                        |
| Fin Thickness ( $T_{Fin}$ )           | 6 nm                         |
| EOT ( $T_{ox}$ )                      | 0.9 nm                       |
| Ferroelectric Thickness ( $T_{FE}$ )  | 2 nm                         |
| Gate Length ( $L_g$ )                 | 16 nm                        |
| Spacer Length ( $L_{sp}$ )            | 6 nm                         |
| Supply Voltage ( $V_{DD}$ )           | 0.7 V                        |
| Coercive Field ( $E_c$ )              | 1 MV/cm                      |
| Remnant Polarization ( $P_r$ )        | $12 \mu\text{C}/\text{cm}^2$ |
| Fin Angle ( $\theta_{Fin}$ )          | $85^\circ - 89.7^\circ$      |
| Ferroelectric Angle ( $\theta_{FE}$ ) | $85^\circ - 89.7^\circ$      |

Table 3.1: Physical parameters of the NC-FinFET device.

The gate stack design follows a MFIS structure, [75, 76, 77]. The FE layer deposited such that the FE polarization is oriented normal to the rectangular fin surface, i.e., the polarization on the sides of the fin is defined in the  $\hat{y}$ -direction while on top it is defined in the  $\hat{z}$ -direction. The remnant polarization is  $12 \mu\text{C}/\text{cm}^2$  and the coercive electric field is 1 MV/cm [64]. The Landau coefficients are obtained via the equations from, [39, 78], yielding  $\alpha = -2.16 \times 10^{11} \text{ cm}/\text{F}$ ,  $\beta = 1.5 \times 10^{21} \text{ cm}^5/\text{FC}^2$ , and  $\gamma = 0 \text{ cm}^9/\text{FC}^4$ . Using the IEEE International Roadmap for Devices and Systems, [8], the OFF-current was defined as 100 pA/ $\mu\text{m}$ , and the ON-current was obtained by interpolating  $I_d$  at  $V_g = V_{OFF} + V_D$ .

Following a similar approach to, [69, 70, 71], we model a non-uniform fin width and FE thickness by defining two angles between the outer surfaces of the respective materials and the silicon substrate, namely,  $\theta_{Fin}$  and  $\theta_{FE}$  respectively. These angles are shown in Fig.3.1b. In addition, we validate our simulations of the NC-FinFET device by first modelling its FinFET counterpart with variable  $\theta_{Fin}$  and compare the results with previous studies [64, 67, 79].

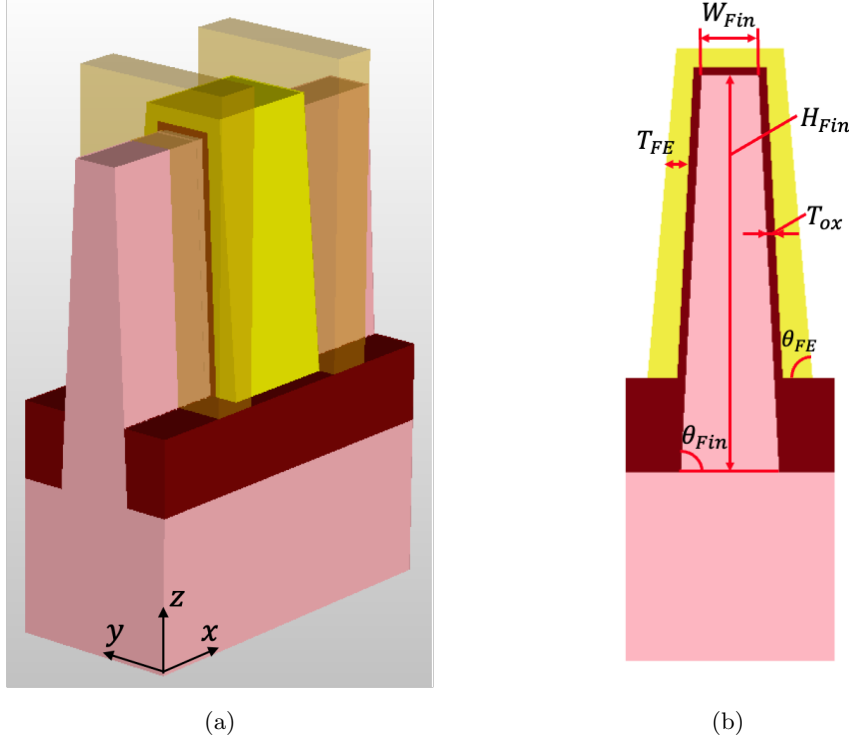


Figure 3.1: (a) 3D TCAD rendering of simulated NC-FinFET device structure, and (b) cross-sectional view of NC-FinFET device, where  $\theta_{Fin} = 87^\circ$ ,  $\theta_{FE} = 85^\circ$  and other significant device parameters are indicated.

### 3.3 Results

#### 3.3.1 Tapered Fin

We first consider the NC-FinFET device with a tapered fin while maintaining a nominal FE layer thickness of 2 nm on all sides of the fin, as defined in Table 3.1. Therefore, we constraint  $\theta_{Fin} = \theta_{FE}$  to ensure that the FE thickness remains 2 nm independent of the  $\theta_{Fin}$ . Such a device can be easily compared to its FinFET counterpart since for a particular value of  $\theta_{Fin}$  the two devices only differ structurally by the addition of a uniform FE layer in the case of NC-FinFET. Because the NC-FinFET device with rectangular fin has been studied extensively, [64, 78, 43, 80], we consider a range of  $\theta_{Fin}$  from  $89.7^\circ$  to  $85^\circ$ . As we decrease  $\theta_{Fin}$  the tapering of the silicon fin becomes more prominent.

Fig.3.2a plots the  $I_d$ - $V_g$  curves of the FinFET and NC-FinFET devices. A cross-section of the NC device in the  $y$ - $z$  plane in the channel region is also shown. In addition, Fig.3.2b plots the  $SS$  as a function of  $\theta_{Fin}$  for both NC and non-NC devices. As in [69, 70, 81], the  $SS$  of the FinFET device increases as  $\theta_{Fin}$  decreases. Effectively, as  $\theta_{Fin}$  is increased the width at the base of the fin increases, thereby reducing the gate controllability in the lower region of the fin and degrading overall performance. Similarly, in the case of NC-FinFET, as the fin angle is decreased the  $SS$  worsens. Sub-60 mV/dec switching is observed for the NC-FinFET device when  $\theta_{Fin} \geq 88$ . Furthermore, the difference in  $SS$  between the non-NC and NC devices for a given value of  $\theta_{Fin}$  changes. Specifically, when  $\theta_{Fin} = 89.7^\circ$  the  $SS$  of the NC device is reduced by 11.5 mV/dec compared to its non-NC counterpart, whereas when  $\theta_{Fin} = 85^\circ$  it is only reduced by, 7.5 mV/dec.

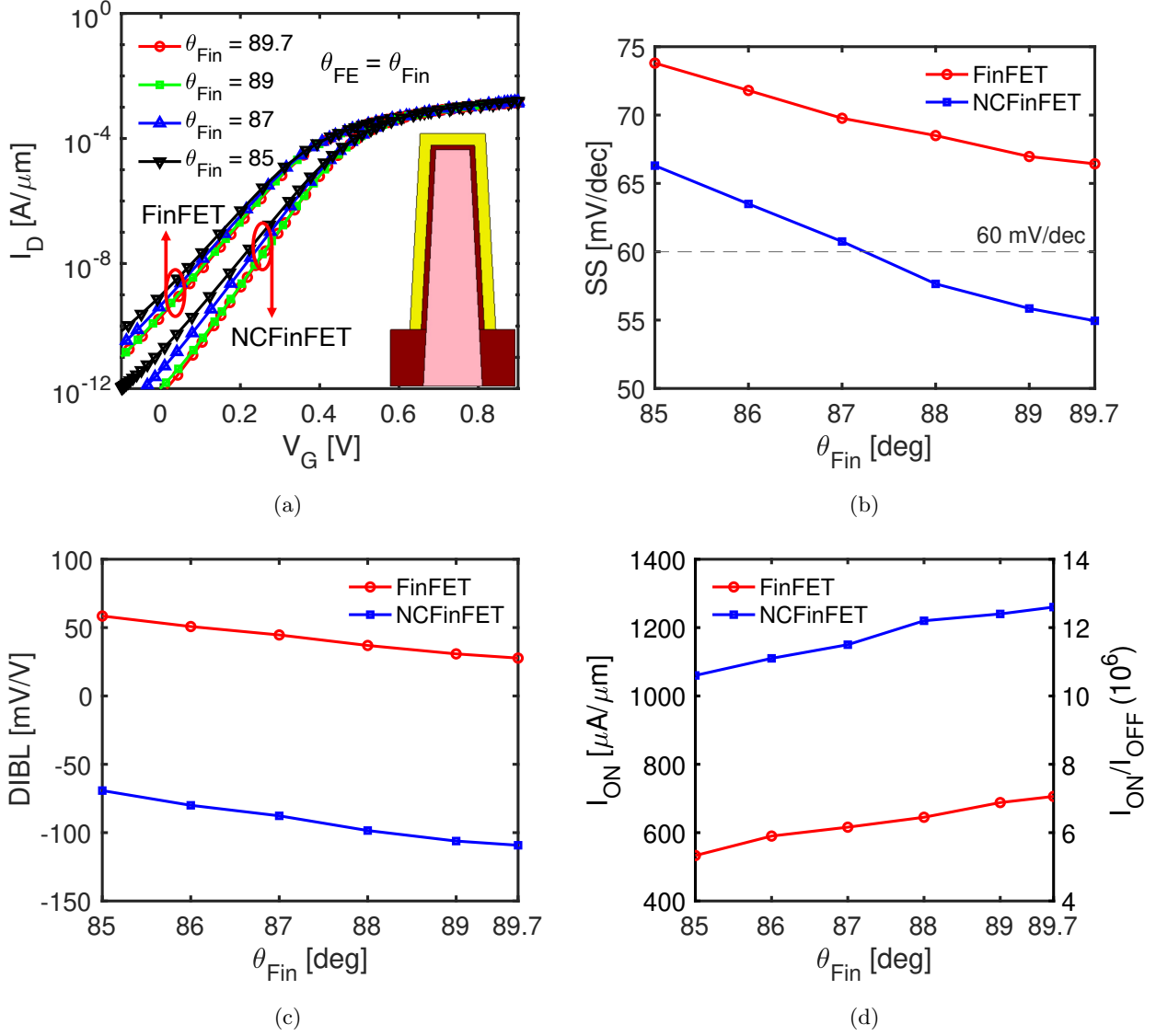


Figure 3.2: (a)  $I_D$ - $V_G$  curves of FinFET and NC-FinFET devices where  $\theta_{Fin}$  is varied from  $89.7^\circ - 85^\circ$ , where  $T_{FE} = 2$  nm. (b)  $SS$  of FinFET (red) and NC-FinFET (blue) devices as a function of fin angle with 60 mV/dec Boltzmann limit shown, (c) DIBL, and (d) ON-current and ON/OFF ratio.

The reason for this difference is illustrated in Fig.3.3. In the idealized case with rectangular fin and FE geometry the maximum NC effect is observed when the FE layer is deposited such that the polarization is perpendicular to the fin surface, Fig.3.3a. In Sentaurus TCAD the FE polarization can only be defined in one of the basis directions, i.e., ' $\hat{x}$ ' ' $\hat{y}$ ' ' $\hat{z}$ ', and not as vector with multiple components [54]. For a rectangular structure the idealized polarization would be in the  $\hat{y}$ -direction on the sides of the fin and in the  $\hat{z}$ -direction on the top, however, with tapered fin angles the situation becomes more complicated.

Fig.3.3b shows that for a device where  $\theta_{Fin} = 85^\circ$  if the FE polarization on the sides of the fin remains

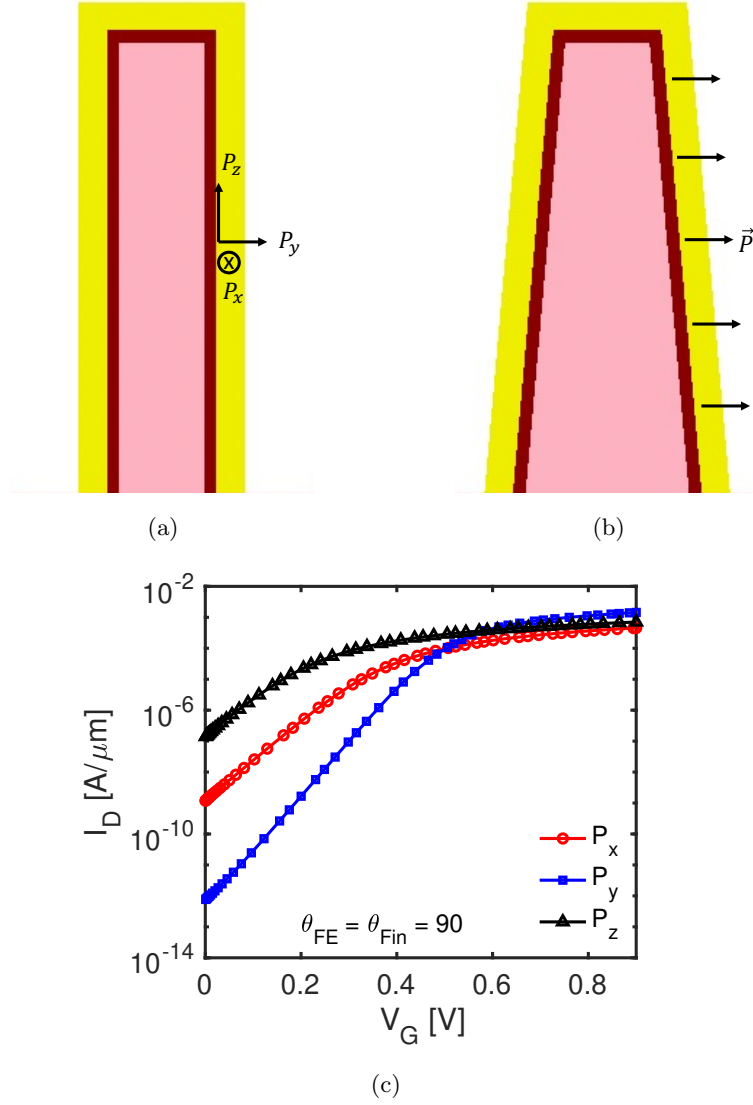


Figure 3.3: (a) Cross section of NC-FinFET device with rectangular geometry and FE polarization directions, which can be used in Sentaurus TCAD, indicated. (b) Cross section of NC-FinFET device with  $\theta_{Fin} = \theta_{FE} = 85^\circ$  and FE polarization in  $\hat{y}$ -direction, (c)  $I_d$ - $V_g$  curves of NC-FinFET device  $\theta_{Fin} = \theta_{FE} = 90^\circ$  where FE polarization in  $\hat{x}$  (red),  $\hat{y}$  (green) and  $\hat{z}$  (blue) directions.

defined in the  $y$ -direction it is no longer exactly perpendicular to the fin surface. Hence, the NC effect becomes reduced as the polarization cannot be expressed as the superposition of  $\hat{y}$  and  $\hat{z}$  components which would be required for the FE polarization to be perpendicular to the fin surface. Fig.3.3c plots the  $I_d$ - $V_g$  results of the unidirectional polarizations in the direction of the Cartesian unit vectors. The polarization remains in the  $z$ -direction on the top side of the fin while the polarization of the FE regions on the sides of the fin are changed. When the FE polarization of the side regions are in the  $y$ -direction the NC effect is maximized as expected.

The drain-induced barrier lowering (DIBL) of the FinFET and NC-FinFET devices is shown in Fig.3.2c.

In calculating the DIBL the lower  $V_D$  value is defined to be 0.05 V. As the fin angle becomes smaller, and the thickness of the fin at the base is widened, the DIBL is increased resulting from the degradation in gate controllability [82]. In addition, the magnitude of the DIBL for the NC device increases with  $\theta_{Fin}$ . Due to the NC effect of the FE layer the DIBL of the NC-FinFET device is negative [83], and this difference in the DIBL between FinFET and NC-FinFET devices is consistent as the fin angle is varied.

The ON-current and ON/OFF ratio of the FinFET and NC-FinFET devices is plotted in Fig.3.2d. Both trends indicate that an increase in  $\theta_{Fin}$  yields a higher ON-current. When  $\theta_{Fin} = 85^\circ$  the ON-current of the NC device is approximately doubled when compared with the non-NC device from  $533 \mu\text{A}/\mu\text{m}$  to  $1060 \mu\text{A}/\mu\text{m}$ . Similarly, when  $\theta_{Fin} = 89.7^\circ$  the ON-current is increased from  $706 \mu\text{A}/\mu\text{m}$  to  $1260 \mu\text{A}/\mu\text{m}$ .

### 3.3.2 Tapered Ferroelectric

In this section, we independently determine the effects of a tapered FE layer by considering the NC-FinFET device with a variable  $\theta_{FE}$  while maintaining the fin angle at its maximum value of  $\theta_{Fin} = 89.7^\circ$ . Effectively, the FE material on top of the gate oxide maintains its nominal thickness of 2 nm while the FE thicknesses on the sides of the fin change via  $\theta_{FE}$ . Fig.3.4 illustrates the effects of changing  $\theta_{FE}$  to achieve a non-uniform  $T_{FE}$  compared to a uniform variation in the FE thickness while the fin and FE angles are at their maximum values,  $\theta_{Fin} = \theta_{FE} = 89.7^\circ$ . The  $I_d$ - $V_g$  curves of the NC-FinFET device with varied  $\theta_{FE}$  and a cross section of the device where  $\theta_{FE} = 85^\circ$  shown in Fig.3.4a. In addition, Fig.3.4b shows the  $I_d$ - $V_g$  curves of the device with varied uniform  $T_{FE}$  from 1 nm to 3 nm in comparison with the results from Fig.3.4a and previous literature, [31, 68, 70], which found that the performance characteristics improve as the FE thickness increases.

The  $SS$  of the NC-FinFET devices, whose  $I_d$ - $V_g$  curves are shown in Fig.3.4a and Fig.3.4b, are plotted in Fig.3.4c as a function of  $\theta_{FE}$  and  $T_{FE}$  respectively. In the latter case, when the FE thickness is increased uniformly the NC effect becomes more prominent and leads to an increase in device performance reflected in a lower  $SS$ . Similarly, in the case of a tapered FE material as  $\theta_{FE}$  is decreased, which causes the FE thickness near the base of the fin to increase, the  $SS$  also improves. The negative DIBL for both devices are shown in Fig.3.4d. In the case where the FE thickness is uniformly changed, as  $T_{FE}$  is increased the magnitude of the DIBL increases. This can be explained by the change in the conduction bands of low and high  $V_D$  values of 0.05 V and 0.7 V respectively. Fig.3.5 shows the conduction band energy trends for both NC-FinFET devices. Fig.3.5a plots conduction band energies, corresponding to  $V_D = 0.7$  V and  $V_D = 0.05$  V, for the device with a uniform FE thickness of 3 nm. Each conduction band is obtained at the OFF-state gate voltage,  $V_{OFF}$ , in both the low and high  $V_D$  cases. Then, the difference between the maxima,  $\Delta E_b$ , is obtained.  $\Delta E_b$  as a function of  $T_{FE}$  and  $\theta_{FE}$  is shown in Fig.3.5b. It is evident from both trends that as the FE thickness becomes larger there is an increase in the difference between the two maxima. Hence, we see that as  $\Delta E_b$  increases the magnitude of the DIBL also increases.

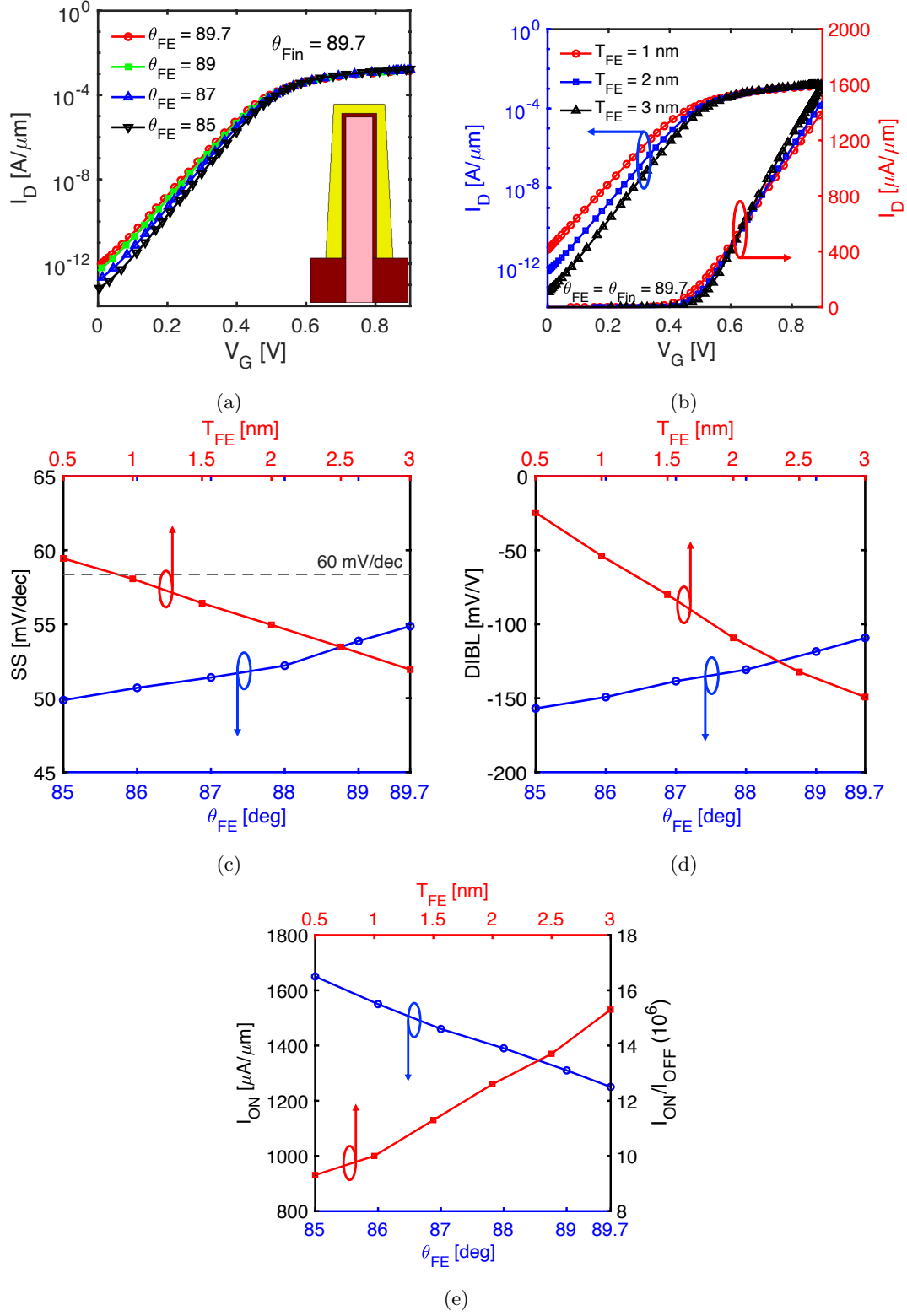


Figure 3.4: (a)  $I_D$ - $V_G$  curve for NC-FinFET where  $\theta_{Fin} = 89.7^\circ$  and  $\theta_{FE}$  varies, (b)  $I_D$ - $V_G$  curves for uniform  $T_{FE}$  variation where  $\theta_{Fin} = 89.7^\circ$ , (c)  $SS$  (d) DIBL, (e) ON-current and ON/OFF ratios of the NC-FinFET devices as a function of  $\theta_{FE}$  and  $T_{FE}$  respectively.

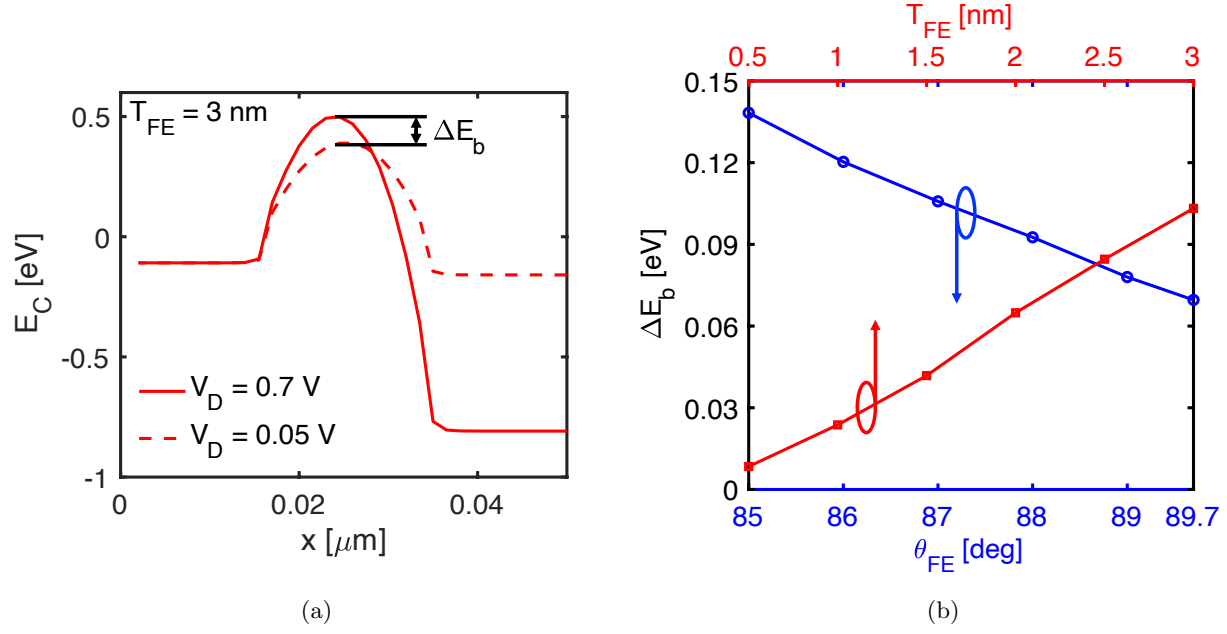


Figure 3.5: (a) Conduction band of NC-FinFET when  $V_D = 0.7$  V and  $V_D = 0.05$  V. The difference between the conduction bands,  $\Delta E_b$ , is indicated. (b)  $\Delta E_b$  as a function of  $\theta_{FE}$  and  $T_{FE}$ .

Lastly, in Fig.3.4e the ON-current and ON/OFF current ratio is plotted. As in previous work, [39], the ON-current is amplified as  $T_{FE}$  increases uniformly. Similarly, as  $\theta_{FE}$  decreases the ON-current is amplified accordingly since this too increases the FE thickness albeit in a fashion that is non-uniform.

### 3.3.3 Optimization of Fin and Ferroelectric Angles

Now that the fin and FE thickness have been varied independently it is possible to consider NC-FinFET devices where the fin and FE thicknesses are changed simultaneously. We consider the set of devices such that  $\theta_{Fin} \geq \theta_{FE}$  since cases where  $\theta_{FE} > \theta_{Fin}$  are not likely and have not been produced in previous experiments. Hence, for each  $\theta_{Fin}$  we consider the set of  $\theta_{FE}$  subject to the constraint. The generalized results for such devices are shown in Fig.3.6.

Fig.3.6a plots the  $I_d$ - $V_g$  curves of the NC-FinFET device in the case where the FE angle is  $85^\circ$  and  $\theta_{Fin}$  is varied. The channel cross section of such a device, where  $\theta_{Fin} = 87^\circ$ , is shown to the right.

Fig.3.6b plots the  $SS$  for various values of  $\theta_{Fin}$  as a function of  $\theta_{FE}$ . In all simulations, as the FE angle is decreased, resulting in an increased FE thickness near the base of the fin, the  $SS$  decreases. In addition, if we consider any value of  $\theta_{FE}$ , decreasing  $\theta_{Fin}$  results in a decrease in the FE thickness. Consequently, the NC effect due to the FE layer is reduced and the  $SS$  increases. Based on the results from Fig.3.6b we see that for the devices where  $\theta_{Fin} = 89.7^\circ$ ,  $89^\circ$ ,  $88^\circ$  the  $SS$  remains in the sub-60 mV/dec region. It is important to note that for a given device with any  $\theta_{Fin}$  and  $\theta_{FE}$ , increasing the fin angle or decreasing the FE angle will result in an improvement in  $SS$  since both effectively increase  $T_{FE}$ . However, increasing  $\theta_{Fin}$  by one degree will yield a greater improvement in the  $SS$  when compared to decreasing  $\theta_{FE}$  by the same amount.

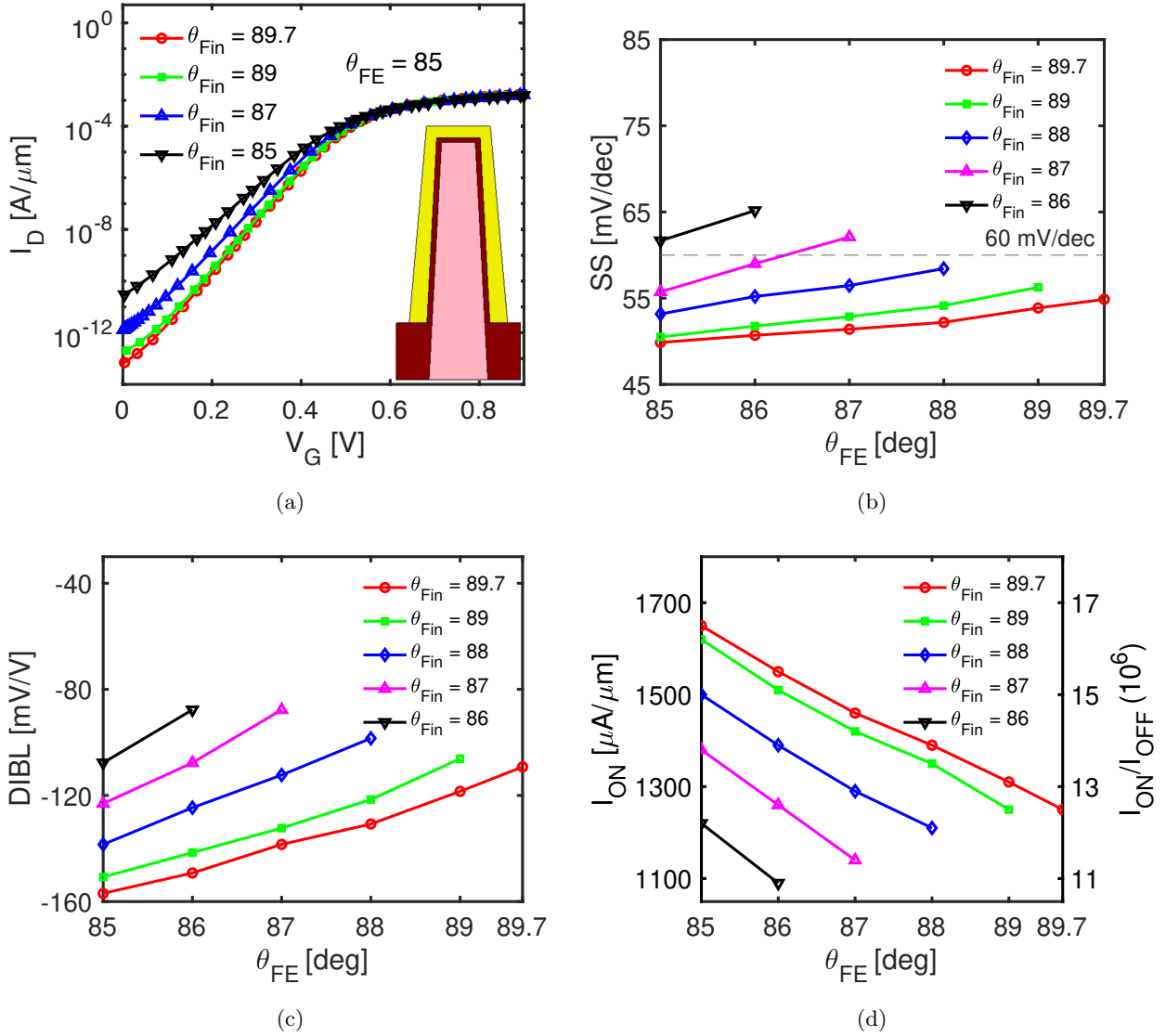


Figure 3.6: (a)  $I_d$ - $V_g$  curve of NC-FinFET devices where  $\theta_{FE} = 85^\circ$  and  $\theta_{Fin}$  is varied. (b)  $SS$ , (c) DIBL, (d)  $I_{ON}$  and  $I_{ON}/I_{OFF}$  ratios of NC-FinFET devices where  $\theta_{Fin} = 89.7^\circ$  (red),  $89^\circ$  (green),  $88^\circ$  (blue),  $87^\circ$  (magenta), and  $86^\circ$  (black) as a function of  $\theta_{FE}$ .

The DIBL is plotted in Fig. 3.6c for different values of  $\theta_{Fin}$  as a function of  $\theta_{FE}$ . Regardless of  $\theta_{Fin}$  as the FE angle is increased, in turn reducing the thickness of the FE material, the NC effect is diminished and the magnitude of the DIBL decreases. This is consistent with the results from Section 3.3.2. In general, decreasing  $\theta_{Fin}$  and increasing  $\theta_{FE}$  will be more desirable toward improving the DIBL effect, however based on the results in Fig. 3.6b, any value of  $\theta_{Fin} > 88^\circ$  should not be considered since this would not yield sub-60 mV/dec behaviour and the purpose of the FE layer would be void. Hence, the devices with  $\theta_{Fin} = \theta_{FE} = 89.7^\circ, 89^\circ, 88^\circ$  minimize the magnitude of DIBL. However, such devices would not maximize  $I_{ON}/I_{OFF}$ , as shown in Fig. 3.6d. For the highest ON-current to be achieved  $\theta_{Fin}$  should be at its greatest value, namely,  $89.7^\circ$ , and  $\theta_{FE}$  should be at its smallest value,  $85^\circ$ , resulting in the maximum FE layer thickness which can be attained.

### 3.4 Conclusion

In this work the effect of an NC-FinFET device with non-uniform fin width and FE layer thickness was investigated. The device, which follows the 8-/7 nm technology node, was simulated using Sentaurus TCAD. To model a tapered fin and FE we treated the sides of the fin as a continuum, defining  $\theta_{Fin}$  and  $\theta_{FE}$  as our tuning parameters.

We first studied independent variations of  $\theta_{Fin}$  with a FE material layer of constant thickness on all sides. Such a device exhibited the greatest improvement in sub-60 mV/dec behaviour when the fin angle was closest to the idealized rectangular geometry since the leakage current was minimized. In the case of a rectangular fin and tapered FE the device exhibited similar characteristics compared with the uniform device. A smaller  $\theta_{FE}$  increases the overall FE layer thickness and reduces the  $SS$ , while increasing the ON-current due to the amplification of the NC effect.

Finally, to engineer the device with optimum performance we varied  $\theta_{Fin}$  and  $\theta_{FE}$  simultaneously. To minimize the  $SS$  and maximize the ON/OFF current ratio the fin angle should be large, i.e., close to the idealized case, however, such a device would have an increased negative DIBL. To minimize the magnitude of the DIBL a thinner FE layer is more desirable. Ultimately, there is a tradeoff between achieving a device exhibiting low  $SS$  with higher ON-current and a device with a smaller DIBL.

Engineering an NC-FinFET device will rely heavily on the performance specifications. A fin with maximum  $\theta_{Fin}$  is ideal, however, if such a device cannot be fabricated perfectly a tapered FE material layer with sufficient  $\theta_{FE}$  can compensate to yield greater gate controllability and achieve the desired performance requirements.

## Chapter 4

# Statistical Variations in FE Thickness for NC-NSFETs

### 4.1 Background

Over the last decade, the continued miniaturization of MOSFET technology has led to the successful development of the FinFET architecture. The reduced gate length, operating voltage, and short channel effects have increased gate control making FinFETs ideally suited for scaling beyond the 10-nm technology node [42, 84]. To meet future requirements beyond the capabilities of the FinFET design other multi-gate FET architectures have been studied. GAA-FETs, such as vertically stacked nanowire and nanosheet FETs, are potential successors to FinFET in future years [85]. GAA-FETs with their further improved SCEs and gate controllability, in addition to having similar fabrication steps to FinFET, lend themselves well to continued scaling past the 3-nm technology node [86].

As chip power densities may soon outstretch cooling capabilities, low-power FETs with their sub-60  $mV/dec$  steep switching characteristics have been under investigation for some time. Devices including NCFETs, which have been studied extensively for low-power applications, is among the field of candidates [31, 74]. NCFETs, which incorporate a ferroelectric material into the gate structure, have shown an improvement in their ON-current compared to MOSFET counterparts with the same supply voltage  $V_{DD}$  [24, 31]. When compared to other sub-60 steep switching devices, the addition of a FE layer into the gate stack is a relatively simple modification in the gate structure making it compatible with existing CMOS fabrication techniques [47].

Recent studies have investigated the performance enhancement of FinFETs and GAA-FETs resulting from the integration of a FE layer in the gate structure [42]. Some have also compared the FinFET with NSFET and NWFET designs [87]. However, to date there have been no studies characterizing the performance of GAA-FETs with statistically varied device parameters as would result from the fabrication process of such devices. An investigation into the statistical variation of the thickness of the FE material and the effect on device performance, particularly its sub-60 steep switching behaviour, for an NC-NSFET is lacking. Such a study is needed for future experimental research of NC-NSFETs.

In this chapter, for the first time, variations in the FE layer thickness of an NC-NSFET device are modelled statistically using a Gaussian distribution exploring multiple standard deviations reflecting different levels of precision in the fabrication process. By sampling values for the ferroelectric thickness from these Gaussian distributions, which are implemented in Python, we are able to simulate large sample sets of NC-NSFET devices in Sentaurus TCAD. First, we calibrate our device in Sentaurus by simulating an NC-NSFET device with a specifically varied ferroelectric thickness and compare its behaviour with previous results. Then we model three sample sets of devices using three Gaussian distributions with separate standard deviations to elucidate how such variations impact device performance of a sample set. Finally, we provide an assessment of the resulting performance variations from the three simulation data sets.

## 4.2 Methodology

In this paper, the nominal device parameters are based on the low power 2.1-nm technology node from the 2022 IEEE International Roadmap for Devices and Systems [8]. The NC-NSFET device consists of three thin channel layers or ‘sheets’, each 30 nm wide,  $W_{NS}$ , and 5 nm in thickness,  $T_{NS}$ . The separation thickness between sheets,  $T_S$ , is defined as 8 nm,  $L_G = 14$  nm, EOT = 0.7 nm, and the nominal FE layer thickness is 2 nm. All the important physical and FE parameters are summarized in Table 4.1, in addition to a three-dimensional and cross-sectional view of the nominal device in Sentaurus TCAD with dimensional parameters indicated, which are shown in Fig.4.1a and Fig.4.1b respectively. The gate structure follows a MFIS structure where the gate oxide and FE layer surround each nanosheet on four sides [87]. The FE layer is deposited in such a manner that the FE polarization is normal to the surface of the channel to maximize the NC effect. The remnant polarization is  $12 \mu\text{C}/\text{cm}^2$  and the coercive electric field is 1 MV/cm [64]. Utilizing the equations from, [57], the Landau coefficients are obtained,  $\alpha = -2.16 \times 10^{11} \text{ cm}/\text{F}$ ,  $\beta = 1.5 \times 10^{21} \text{ cm}^5/\text{FC}^2$ , and  $\gamma = 0 \text{ cm}^9/\text{FC}^4$ . In our TCAD simulations the Landau-Khalatnikov equation, Poisson equation, and mobility degradation model are implemented and solved self-consistently [54]. From the IEEE International Roadmap for Devices and Systems we define the OFF-current at 100 pA/ $\mu\text{m}$ , and obtain the ON-current from  $V_g = V_{OFF} + V_D$  [8].

| Parameter                            | Value                        |
|--------------------------------------|------------------------------|
| Sheet Width ( $W_{NS}$ )             | 30 nm                        |
| Sheet Thickness ( $T_{NS}$ )         | 5 nm                         |
| Sheet Separation ( $T_S$ )           | 8 nm                         |
| EOT ( $T_{ox}$ )                     | 0.7 nm                       |
| Ferroelectric Thickness ( $T_{FE}$ ) | 2 nm                         |
| Gate Length ( $L_g$ )                | 14 nm                        |
| Spacer Length ( $L_{sp}$ )           | 5 nm                         |
| Supply Voltage ( $V_{DD}$ )          | 0.7 V                        |
| Coercive Field ( $E_c$ )             | 1 MV/cm                      |
| Remnant Polarization ( $P_r$ )       | $12 \mu\text{C}/\text{cm}^2$ |

Table 4.1: Physical parameters of NC-NSFET device.

To validate that our simulations produce similar results from previous investigations, we vary the FE thickness on the top and bottom of each nano-sheet, where  $T_{FE}$  ranges from 1.0-3.0 nm. We compare our 2.1-nm

NC-NSFET device with previously simulated NC-NSFET devices by examining the trend of performance metrics as a function of  $T_{FE}$ . To model variations in the NC effect arising from limitations in the fabrication process of NC-NSFET, we only consider variations in the thickness of the FE layer to simplify our simulations. In addition, our changes in  $T_{FE}$  are confined to the top and bottom sides of each nanosheets since variations in the side thicknesses of FE would produce negligible variations in the performance of the device due to the size of  $T_{NS}$  compared with  $W_{NS}$ . The  $I_d$ - $V_g$  curves of the NC-NSFET device are shown in Fig.4.2a, and the  $SS$  as a function of  $T_{FE}$  on the top and bottom of the FE layer surrounding each channel is related in Fig.4.2b. As expected, the subthreshold swing decreases as the ferroelectric material thickness is increased due to the increase in gate controllability resulting from the enhanced NC effect [88]. In the case of the nominal device, i.e.,  $T_{FE} = 2$  nm, the subthreshold swing is 54.05 mV/dec. The threshold voltage,  $V_{th}$ , and  $I_{ON}$  are shown as a function of  $T_{FE}$  in Fig.4.2c and Fig.4.2d respectively. They both illustrate that as the FE thickness on the top and bottom of each nanosheet becomes larger both  $V_{th}$  and  $I_{ON}$  increase. Again, due to the increase in the NC effect [39, 68].  $V_{th}$  and  $I_{ON}$  for the nominal device are 0.297 V and  $1.793 \times 10^{-3} \mu A/\mu m$ .

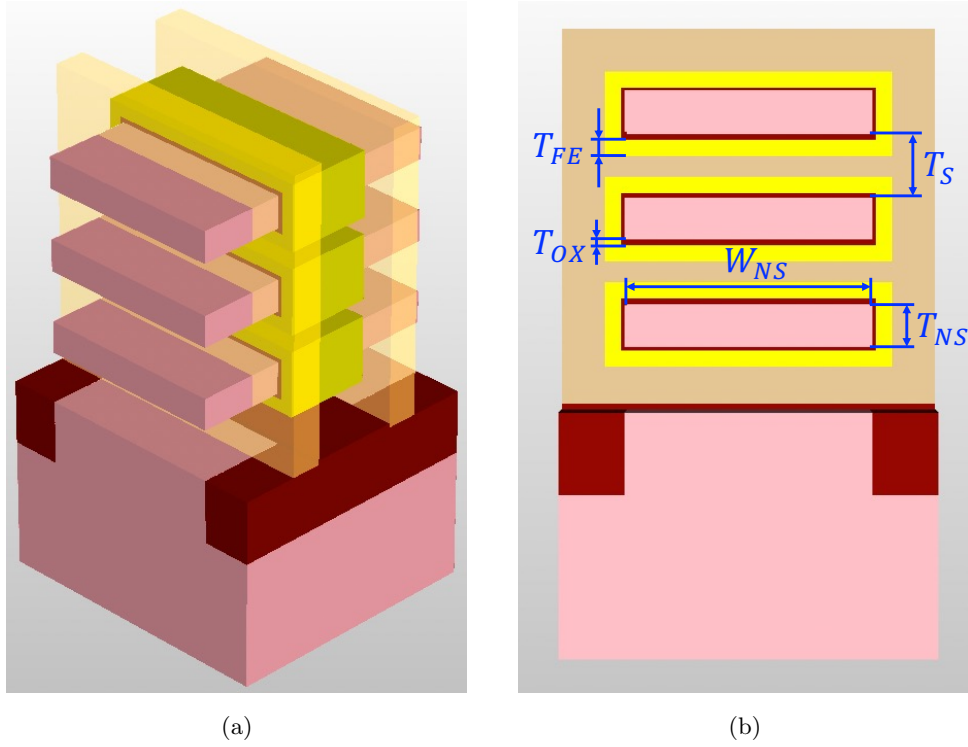


Figure 4.1: (a) 3D TCAD NC-NSFET device structure, and (b) cross-sectional view of NC-NSFET with physical parameters indicated.

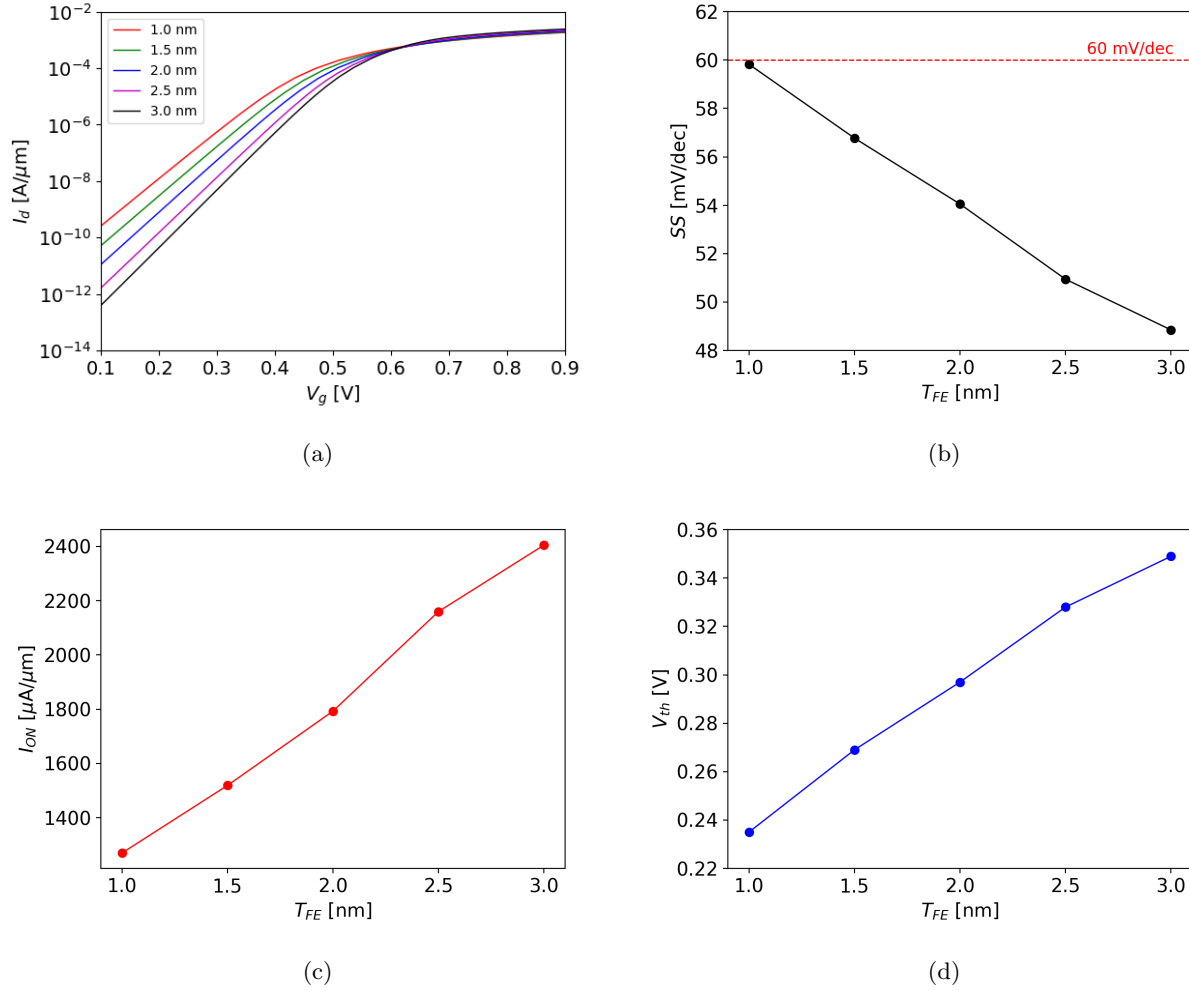


Figure 4.2: (a)  $I_d$ - $V_g$  curve for NC-NSFET device where  $T_{FE}$  ranges from 1.0 nm – 3.0 nm, (b)  $SS$ , (c)  $V_{th}$ , and (d)  $I_{ON}$  as a function of  $T_{FE}$ . As the FE thickness is increased the performance characters improve.

### 4.3 Results

To statistically analyze the variation in  $T_{FE}$  and the resulting performance arising from the fabrication of a large set of NC-NSFET devices, we consider a Gaussian distribution of  $T_{FE}$ . We define three distributions, where the mean value of  $T_{FE}$  is the previously defined nominal value, i.e.,  $\mu = 2$  nm, and define  $3\sigma$  as the upper and lower limit of  $T_{FE}$  for each distribution. Defining the maximum and minimum values as  $T_{FE} \pm 3\sigma$  we are able to encompass a significant amount of the Gaussian distribution. Since it is difficult to obtain the variation in terms of a  $3\sigma$  value from experimental results we consider three values of  $3\sigma$ , namely, 0.8, 0.4, 0.2 nm.

Thus, we examine the overall trend in performance as the variation in  $T_{FE}$  is reduced by decreasing  $3\sigma$ . As previously mentioned, in our simulations for the nominal device we only consider changes in the thickness of the top and bottom FE layers of each thin nanosheet. Hence, each simulation requires 6 randomly sampled

points from the Gaussian distribution under consideration. In addition, for each  $3\sigma$  we simulate 100 devices, thus 600 randomly sample points are obtained in each case. Fig.4.3 shows the results of the randomly sampled distributions with mean,  $\mu$ , defined as  $T_{FE} = 2$  nm. Fig.4.3a, Fig.4.3b, and Fig.4.3c contain the histograms where  $3\sigma = 0.8$ ,  $0.4$ , and  $0.2$  nm respectively. The randomly sampled Gaussian distributions with 600 values are all centred around the nominal  $T_{FE}$  value. As  $3\sigma$  is decreased the occurrences of the mean increase as expected.

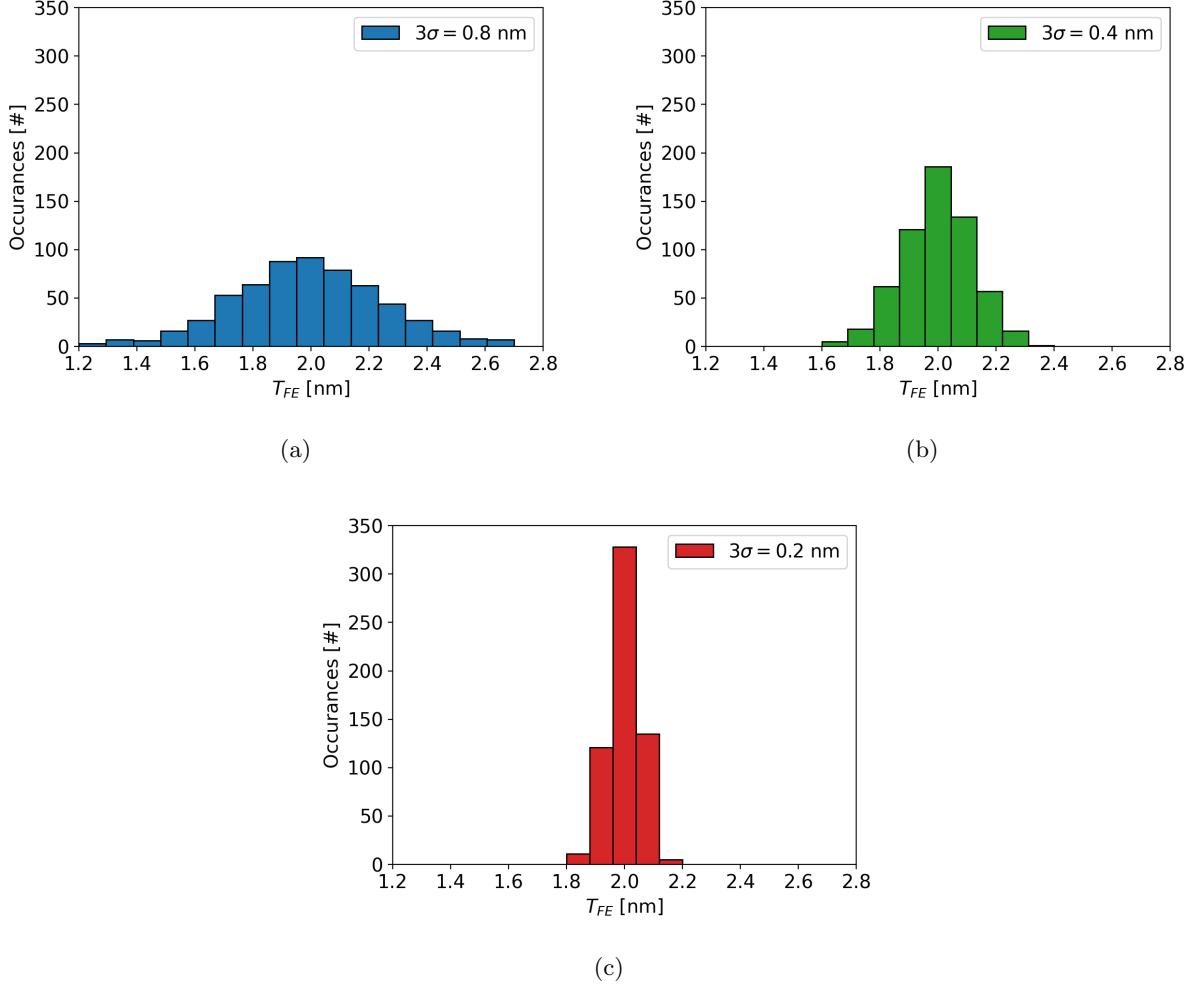


Figure 4.3: Histograms of 600 randomly sampled values of  $T_{FE}$  from Gaussian distribution where (a)  $3\sigma = 0.8$  nm, (b)  $3\sigma = 0.4$  nm, and (c)  $3\sigma = 0.2$  nm.

The  $I_d$ - $V_g$  curves for each group of simulations are shown in Fig.4.4 along with the boundary cases where each of the 6 values for the FE thickness are defined to be  $2 \pm 3\sigma$  nm. For example, in the case of  $3\sigma = 0.8$  nm the boundary cases are  $T_{FE} = 2 \pm 0.8$  nm. In addition, the idealized case where  $T_{FE} = 2$  nm is indicated by a dotted curve for reference. Fig.4.4a illustrates the  $I_d$ - $V_g$  curves in the scenario where  $3\sigma = 0.8$  nm. The boundary cases where  $T_{FE} = 1.2, 2.8$  nm are plotted as solid curves and the  $I_d$ - $V_g$  curves arising from the statistically varied values of the FE thickness are shown as dotted curves. Similarly, the  $I_d$ - $V_g$  curves

for the cases where  $3\sigma = 0.4, 0.2$  nm are shown in Fig.4.4b and Fig.4.4c respectively. As  $3\sigma$  decreases the cluster of  $I_d$ - $V_g$  curves resulting from the combined data sets increases in density and is centred around the idealized device,  $T_{FE} = 2$  nm, as expected from the Gaussian distributions shown in Fig.4.3. Furthermore, with smaller  $3\sigma$  values, the distance between the  $I_d$ - $V_g$  curves with statistically varied  $T_{FE}$  become closer to the boundary cases,  $T_{FE} = 1.6, 2.4$  nm when  $3\sigma = 0.4$  nm and  $T_{FE} = 1.8, 2.2$  nm when  $3\sigma = 0.2$  nm.

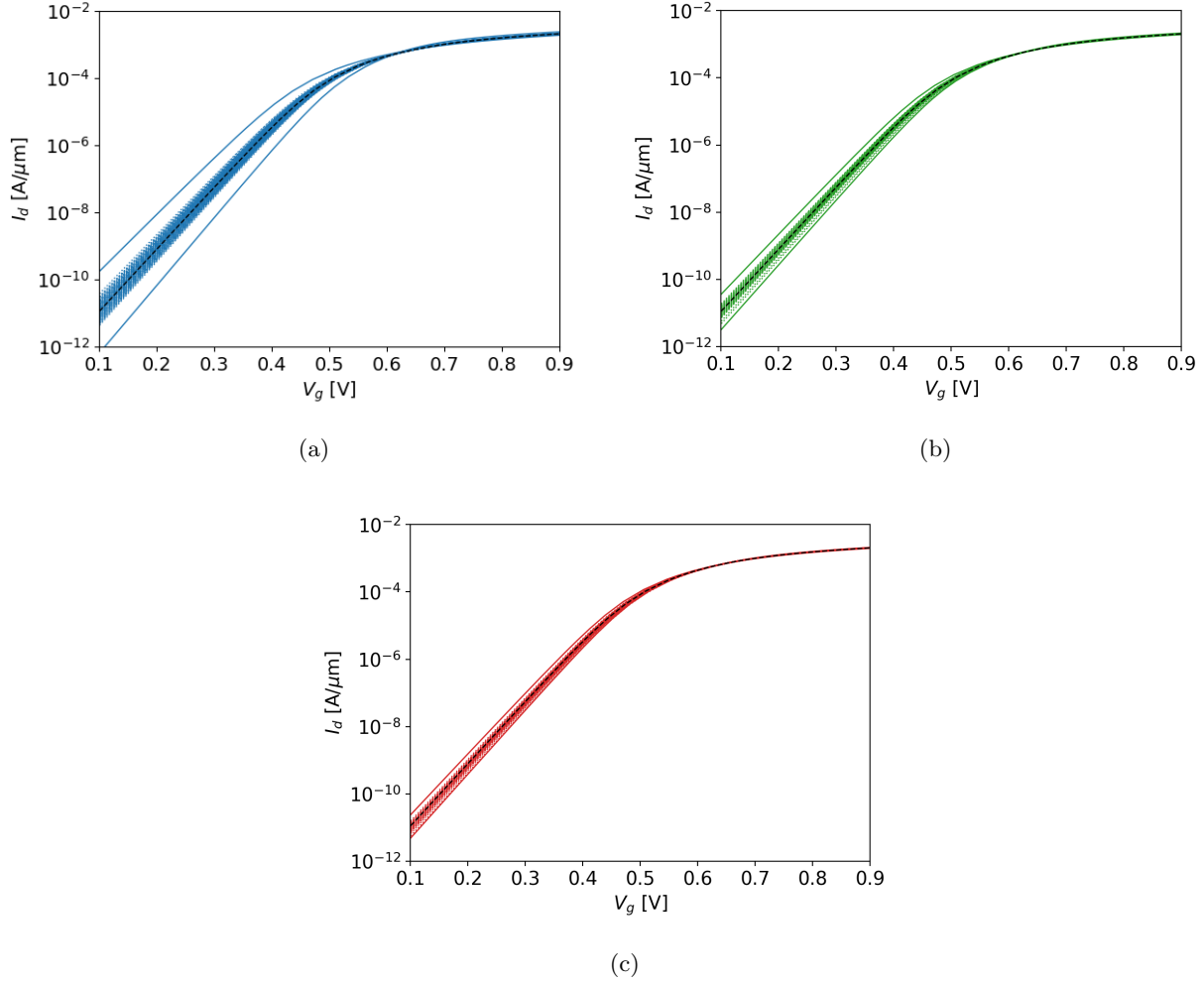


Figure 4.4:  $I_d$ - $V_g$  curves of all simulations from each data set where (a)  $3\sigma = 0.8$  nm, (b)  $3\sigma = 0.4$  nm, and (c)  $3\sigma = 0.2$  nm. The  $I_d$ - $V_g$  curve of the nominal device is shown in black along with the  $I_d$ - $V_g$  curves of each ‘boundary case’.

The  $SS$ ,  $V_{th}$  and ON-current are shown in Fig.4.5 as a function of the average variation in  $T_{FE}$ .  $\langle T_{FE} \rangle$ , is calculated using the six values for  $T_{FE}$  obtained from the respective Gaussian distribution for a given device simulation. The  $SS$  is plotted in Fig.4.5a with the Boltzmann limit of 60 mV/dec indicated. The trend of  $SS$  from Fig.4.2b is plotted in black for comparison to the statistically modelled simulations. Each set of simulations follow the trend of  $SS$  from Fig.4.2b. We see that as  $3\sigma$  decreases the cluster of points around the nominal curve become more concentrated. Furthermore, both the difference between the maximum and

minimum values for the  $SS$ , and  $\langle T_{FE} \rangle$  become smaller as  $3\sigma$  is decreased. Similarly,  $V_{th}$  and  $I_{ON}$  are shown in Fig.4.5b and Fig.4.5c respectively with the trends from Fig.4.2c and Fig.4.2d superimposed over the data sets. We see that both the threshold voltage and ON-current follow the expected trends. As  $\langle T_{FE} \rangle$  increases both  $V_{th}$  and  $I_{ON}$  increase. In addition, as the upper and lower limit is decreased via  $3\sigma$  the density of points for each data set increases and the difference between the maximum and minimum values for  $V_{th}$  and  $I_{ON}$  decreases. Comparing the results for each case of  $3\sigma$  we note that as the standard deviation decreases the spread of  $\langle T_{FE} \rangle$  decreases. The upper and lower bounds of  $\langle T_{FE} \rangle$  are smaller than the outliers of the individual Gaussian distributions since the device consists of three nanosheets, thus the average value of  $T_{FE}$  is closer to the nominal thickness of 2 nm. The performance metrics for the boundary cases of each distribution, i.e., the devices where  $\langle T_{FE} \rangle = 2 \text{ nm} \pm 3\sigma$ , are not included in Fig.4.5. Their inclusion would obscure the relative density of points for each distribution since in the case where  $3\sigma = 0.8 \text{ nm}$  the upper and lower values of  $\langle T_{FE} \rangle$  are 1.2 nm and 2.8 nm respectively.

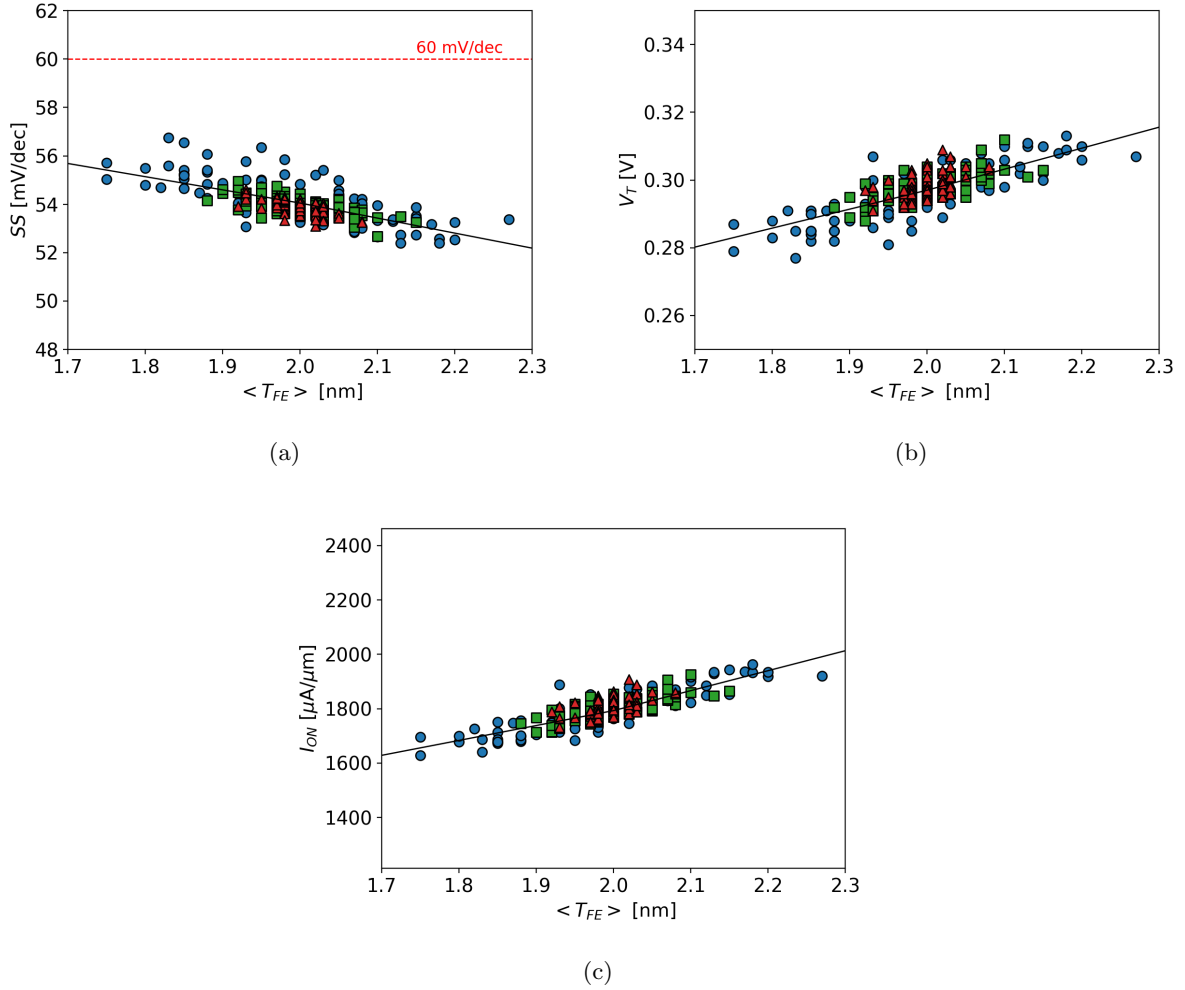


Figure 4.5: Scatter plots of the performance characteristics (a)  $SS$ , (b)  $V_{th}$ , and (c)  $I_{ON}$ , as a function of  $\langle T_{FE} \rangle$  from the simulation data sets with  $3\sigma = 0.8 \text{ nm}$  (blue circle),  $3\sigma = 0.4 \text{ nm}$  (green square), and  $3\sigma = 0.2 \text{ nm}$  (red triangle). The trend of each parameter from Fig.4.2 is shown by the black line.

Ultimately, what matters is the difference in each variable describing device performance in the context of a particular value of  $3\sigma$ . We now move to quantify these differences between distributions. Fig.4.6 shows the results of the maximum and minimum values for each performance characteristic in addition to the values of the boundary limits for each  $3\sigma$ . Fig.4.6a, Fig.4.6b, and Fig.4.6c compare the variation in  $SS$ , threshold voltage, and ON-current of the simulations with the respective maximum and minimum values. We see that, for each performance characteristic the difference between the boundary case simulations is always larger than the results obtained from the statistical variation of  $T_{FE}$  as expected. However, as the standard deviation decreases the differences arising from the statistical variations approach the difference from the boundary cases. In particular,  $\Delta SS$  in the boundary cases for  $3\sigma = 0.4, 0.2$  nm are 4.196 mV/dec and 2.73 mV/dec respectively, while the statistical results yield a difference of 2.273 mV/dec and 1.357 mV/dec. In addition, statistical modelling of  $3\sigma = 0.4$  nm yields an improvement over  $\Delta SS$  in the boundary values for  $3\sigma = 0.2$  nm. Hence, for a certain tolerance requirement in  $SS$ , quantified by  $\Delta SS$ , a fabrication method with a larger, but still appropriate  $3\sigma$ , will produce the desired performance range. The results for the threshold voltage and ON-current produce a similar result when comparing  $3\sigma = 0.8, 0.4$  nm and  $3\sigma = 0.4, 0.2$  nm.

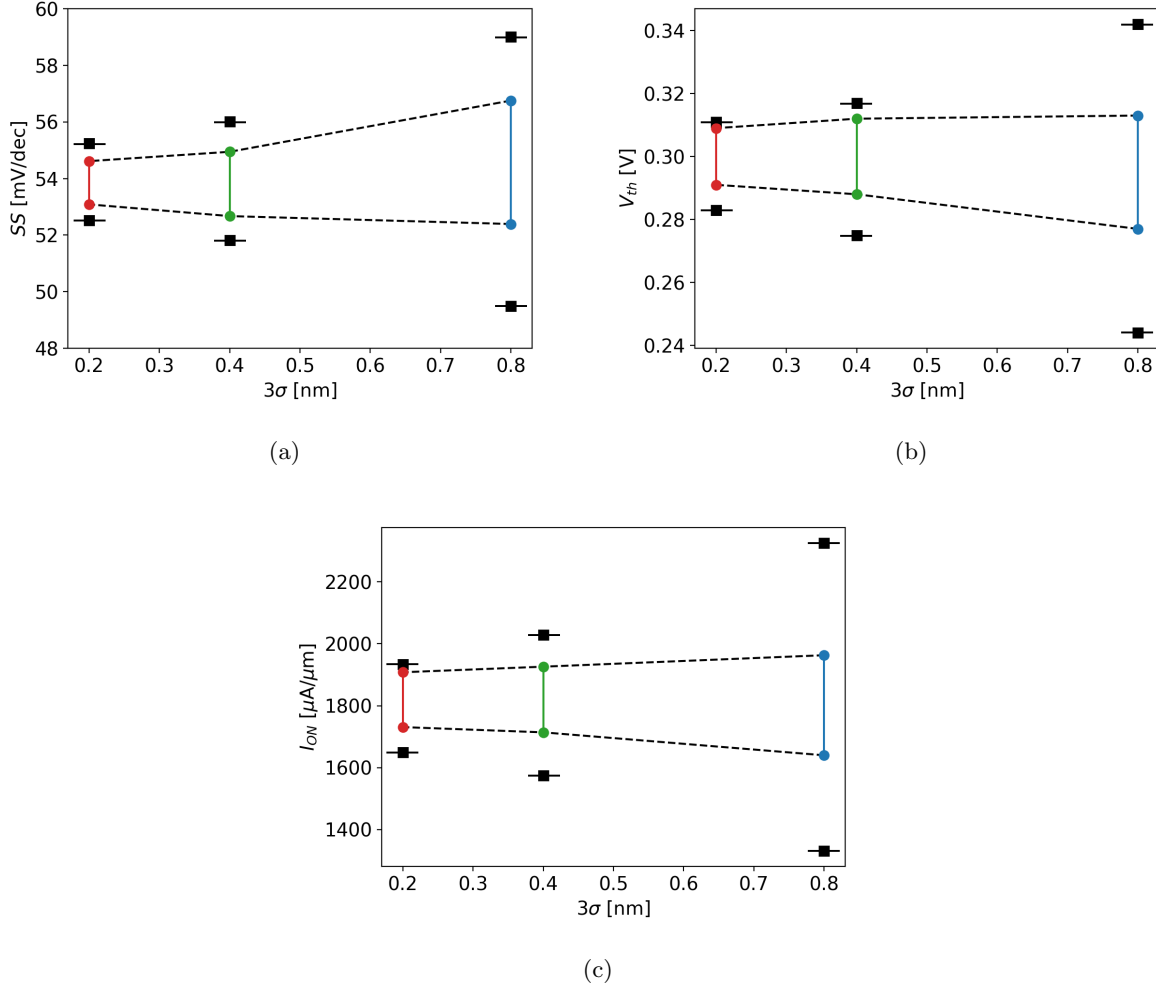


Figure 4.6: (a)  $SS$ , (b)  $\Delta V_{th}$ , and (c)  $I_{ON}$  as a function of  $3\sigma$  with the limiting cases from the statistical modelling of  $T_{FE}$  alongside the boundary simulation results in each case of  $3\sigma$ . The trend of the upper and lower boundary cases as a function of  $3\sigma$  is shown by dashed lines.

## 4.4 Conclusion

In this work, statistical variations in the thickness of the FE material for an NC-NSFET device was studied. The nominal device is based on the 2.1-nm technology node consisting of three nanosheets. To simplify our Sentaurus TCAD simulations, the top and bottom FE layer of each nanosheet was varied since variations in  $T_{FE}$  for the sides of the nanosheets is negligible due to the thickness of  $T_{NS}$  compared to  $W_{NS}$ . Three Gaussian distributions were implemented with  $\mu = 2$  nm and different standard deviations, controlled by the definition of  $3\sigma$  as the upper and lower  $T_{FE}$  limit (0.8, 0.4, 0.2 nm). For each case of  $3\sigma$ , 100 devices were simulated with 6 randomly sampled values of  $T_{FE}$  obtained from each Gaussian distribution per simulation. The results of our statistical analysis indicate that as  $3\sigma$  decreases, the density of performance characteristics,  $SS$ ,  $V_{th}$ , and  $I_{ON}$ , become more concentrated around their nominal values. Finally, to obtain a particular bound on a performance characteristic, which would correspond to a device with  $T_{FE} = 2 \pm 3\sigma$ , a larger  $3\sigma$

value can be considered since the statistical variations are extremely unlikely to produce results at or near the boundary cases. Future experimental studies of the 2.1-nm technology node with an NC-NSFET architecture, can use the methods outlined in Fig.4.6 to quantify the standard deviation arising from imperfections in the fabrication process.

## Chapter 5

# Conclusions and Future Works

### 5.1 Conclusions

In this thesis, Synopsys Sentaurus TCAD simulations were implemented to study the effect of geometric non-idealities in negative capacitance multi-gate FETs. In Chapter 3, we developed NC-FinFET devices with tapered fin channels and FE structures to determine the effects on device performance. We found that a more tapered fin resulted in a degradation of ON-current and subthreshold behaviour. In addition, a highly tapered FE layer resulted in performance enhancement since it effectively increased the ferroelectric thickness. Therefore, we proposed that to improve the subthreshold swing and  $I_{ON}$  the fin should be as close as possible to the idealized rectangular geometry whereas the FE material should be tapered. However, such a device also exhibits large DIBL. In Chapter 4, we modelled the statistical variation in the ferroelectric thickness of an NC-NSFET device for using several Gaussian distributions. We found that as the standard deviations of the distributions became smaller the variability in performance characteristics reduced. Additionally, for a sufficient standard deviation,  $\sigma_1$ , the NC-NSFET devices will be within the boundary devices of  $T_{FE} = 2 \text{ nm} \pm 3\sigma_2$  for another distribution with a smaller standard deviation  $\sigma_2$ . Therefore, a wider dispersion of  $T_{FE}$  can achieve a desired performance range.

### 5.2 Future Works

Based on the work contained within this thesis there are several avenues of research which can be pursued. Regarding the work in Chapter 3, angles were defined which treated the sides of the fin and FE layer as a continuum. In future works, this can be replaced by a more discrete, or jagged surface, to better approximate the fabrication of NC-FinFETs. Such studies should be based on the current fabrication capabilities. In addition, moving beyond the work contained in Chapter 4, statistical variations in the thickness of the ferroelectric on the sides of the nanosheets in an NC-NSFET device can also be studied along with non-rectangular channel cross sections which would closely resemble previously fabricated NC-NSFETs. Furthermore, it would be interesting to explore the statistical distributions for other device parameters, such as sheet width and thickness, along with studying large sample sets where the number of nanosheet layers is increased.

The computational models of the work in Chapter 3 and 4 followed the Landau theory of ferroelectric materials to simulate negative capacitance effects. Apart from the Landau model, the Miller model [45], which can

account for possible hysteresis, can also be used to study the switching behaviour of ferroelectric materials integrated into multi-gate FET architectures. To carry out such studies would be beyond the capabilities of Sentaurus TCAD since only the Landau model is currently supported, therefore, the numerical simulations would most likely have to be performed without the aid of commercial design tools for logic device simulation. In addition, the research in Chapter 3 and 4 treated ferroelectric regions as a single-domain, however, other numerical studies have simulated both single-domain and multi-domain FEs [49, 56]. Future work should consider these types of FE regions and implement more advanced models of FE materials to deepen the contemporary understanding and further the development of multi-gate NCFET devices.

Looking beyond the work contained in this thesis, to advance the development and understand of negative capacitance in multi-gate FETs continued experimental work is of central importance. In particular, improvements in the fabrication techniques of 3D FET designs and the integration of ferroelectric materials must be made for the commercialization of NCFETs to come to fruition. If the polarization directions of deposited FE materials are not orthogonal to channel surfaces NC effects will be nonexistent. Therefore, experimental research must advance in parallel with computational work for the scaling of FETs to continue in the decades to come.

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# APPENDICES

# Appendix A

## Sentaurus TCAD

In this Appendix we discuss in further detail the Sentaurus TCAD simulation methodologies for the research of multi-gate architectures as pertains to the contents of this thesis. In particular, we provide an overview of the design procedures for the FinFET and NSFET devices used in Sentaurus Structure Editor. Then, we discuss important aspects of the methods used to simulate the operation of the multi-gate architectures. The details of physics and models used in Sentaurus to simulate negative capacitance FETs and ferroelectric materials is examined in Chapter 2. Therefore, in this chapter we consider conventional MOSFET gate structures without a ferroelectric layer as examples to facilitate our discussion.

### A.1 Simulation of Multi-Gate Structures

The Sentaurus Structure Editor (SDE) is used to model the structure and obtain the mesh information file for the FET devices studied in Chapters 3 and 4. The SDE command file which uses its own scripting language syntax can be broken down into sections [63]. First, the geometric and doping parameters must be specified. Then, the physical device structure can be created using a series of commands which using the parameter definitions as input. For later simulations of device functions the gate and source/drain contacts, i.e., interfaces between metal electrodes and MOSFET, must be defined. In addition, the doping regions have to be created from the doping concentration definitions. Finally, the meshing information needs to be defined and a mesh file created as output. Apart from the total volume encompassing the device structure additional regions can be defined for a mesh with higher resolutions, e.g., channel region. We now go into the specifics of the nominal FinFET and NSFET structures studied in Chapter 3 and 4 without a ferroelectric material.

#### A.1.1 FinFET

The FinFET device is based on the 8/7-nm technology node specifications outlined in the IEEE International Roadmap for Devices and Systems. In the SDE command file the geometric parameters and doping concentrations are first defined. To create the basic structure of the device the bulk and silicon fin, with source and drain regions, are defined separately. The insulating material is deposited on top of the exposed bulk region on both sides of the fin, and the gate oxide surrounds the channel region. The gate metal is then deposited on the gate stack. (See Fig. A.1a). In order to define the device contacts, metals around the source and drain regions are created. There are four contacts that are then defined: the bulk contact on the

bottom of the device, the gate contact which is the interface between the metal gate and insulator, and the source and drain contacts as the interfaces between metals and the device. Since the boundary of the metal material is important in the simulation process the metal regions are removed. (See Fig. A.1b). Finally, the nitride spacers are defined after the contacts have been created since to prevent an contact between the metal gate and nitride which would not change the results of any simulations.

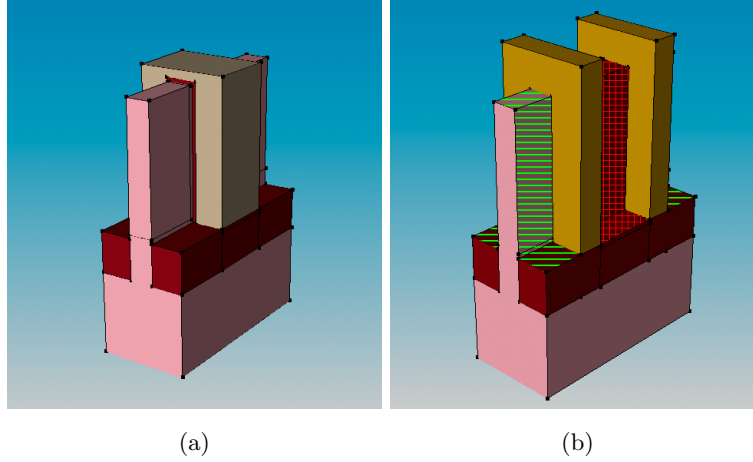


Figure A.1: (a) 3D SENTAURUS TCAD model of FinFET device with silicon fin and gate structure shown, which surrounds the channel on three sides. (b) FinFET with source, drain, and gate metal contact interfaces defined.

After the contacts have been defined we create two regions for the device mesh. First we define a mesh with a relatively higher density surrounding the channel region. (Fig. A.2a). This ensures that we will be able to model the device physics accurately. Then we define a mesh with lower density that surrounds the entire FinFET device. (Fig. A.2b). The mesh previously defined around the channel will remain unchanged.

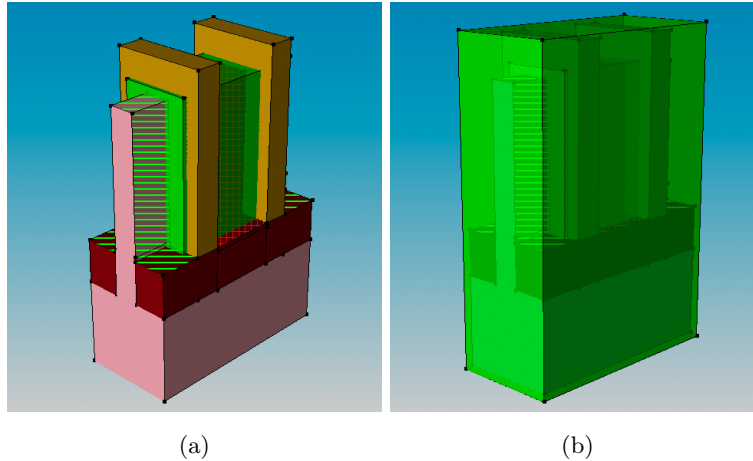


Figure A.2: (a) 3D SENTAURUS TCAD model of FinFET device where gate mesh and (b) device mesh are defined. The mesh in the channel region is of higher resolution.

### A.1.2 NSFET

The NSFET geometric and concentration parameters follow the 2.1-nm technology node. After the parameters are defined the physical structure is created. First, the bulk silicon and trench filled with insulating material is made. On top of the bulk section where the gate metal is deposited a thin insulating layer is deposited. The nanosheet device is made of three thin silicon channel layers. For each layer the source and drain regions are defined and the channel is surrounded by the gate insulator on all sides. The metal gate then surrounds all of the nanosheets. (Fig. A.3a). In addition, the source and drain regions for each of the nanosheets is surrounded by metal contacts. We define the source, drain and nanosheet gate contacts as the interfaces between the metals and the device. (Fig. A.3b). As in the case of FinFET only the interfaces are necessary for simulations.

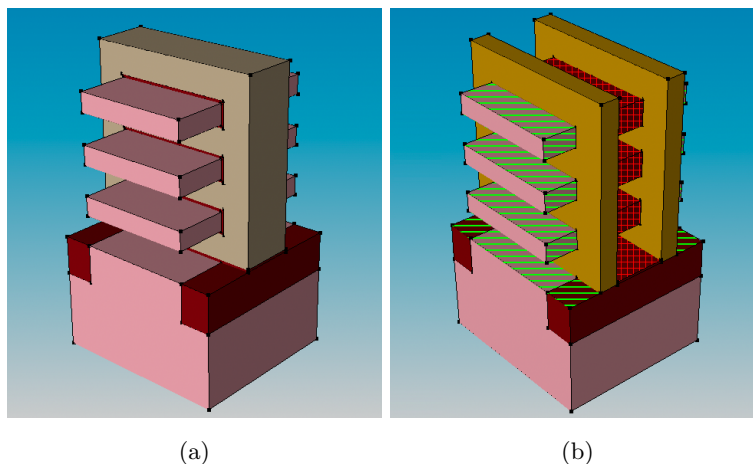


Figure A.3: (a) 3D Sentaurus TCAD model of NSFET device with silicon nanosheets and gate structure shown, which surrounds the channel on four sides. (b) NSFET with source, drain, and gate metal contact interfaces defined.

The mesh for the NSFET device is similar to the FinFET case. Now, three regions which surround each nanosheet are defined with a large density of points. (Fig. A.4a). The entire device is then surrounded by a larger region with a lower density of mesh nodes. (Fig. A.4b). Thus, the mesh is able to simulate the device physics in a reliable manner without unnecessarily long simulation times.

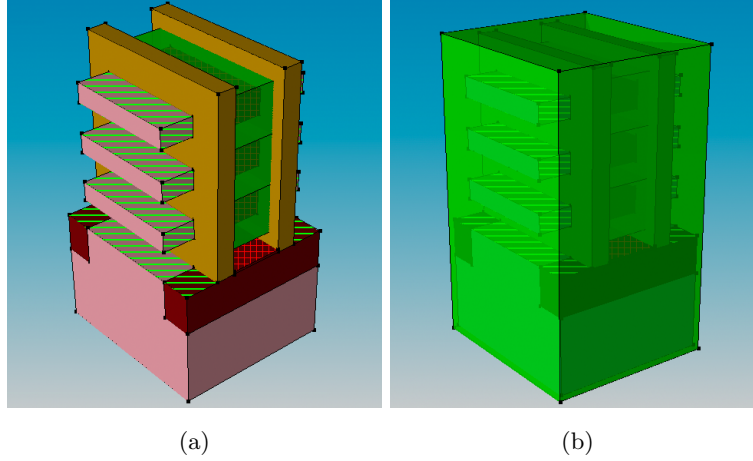


Figure A.4: (a) 3D Sentaurus TCAD model of NSFET device where gate mesh and (b) device mesh are defined. The mesh in the channel region is of higher resolution.

## A.2 Simulation of Multi-Gate Physics

Sentaurus Device (SDevice) is used for the simulation of the FET devices. Similar to SDE, SDevice uses its own scripting language and syntax [54]. The SDevice command file is broken into sections using the syntax `section-name {}`. First, the *File* section is where the input, e.g., the mesh information file, and output files, e.g., plot file, of the simulation are defined. The *Electrode* section the electrical contacts and boundary conditions are defined. In the *Physics* section the physical models used in the simulation are declared. Variables whose solutions are to be saved must be specified in the *Plot* section. The setting for numeric solvers is changed via the *Math* section. Finally, in the *Solve* section the details for solving transport models is specified. The significant sections of the SDevice command file are *Physics*, *Math*, and *Solve*. We will go into more detail about these sections for the FinFET and NSFET devices whose SDevice command files are essentially identical.

### A.2.1 Physics

In the Physics section we declare the models that are to be used our simulations. A particular physics model can be specified for a material, region or interface. In our simulations we use the statement `Physics {Fermi}` to model Fermi statistics for the entire device. In addition, we make use of the high-field saturation mobility model which describes the mobility degradation in high electric fields where the drift velocity of the carriers is not proportional to the electric field.

### A.2.2 Solve Section

In the Solve section we define the solutions to be obtained. In our Solve section there are two quasistationary statements. The first ramps the drain voltage from 0.0 to 0.7 V, defined in the Electrode section. The second ramps the gate bias from 0.0 to 0.9 V. For each statement the initial, max, and min steps are defined. In each statement as the voltages are incremented the Poisson and carrier continuity equations are solved self consistently using the statement `CoupledPoisson Electron Hole`. Sudo commands are shown below:

```

Solve{
  #-ramp drain
  Quasistationary(
    InitialStep = SPECIFY_VALUE
    MaxStep = SPECIFY_VALUE
    Minstep = SPECIFY_VALUE
    Increment = SPECIFY_VALUE
    Goal { Name = "drain" Voltage=@Vd@ }
  ){ Coupled{ Poisson Electron Hole } }

  #-ramp gate:
  Quasistationary(
    InitialStep = SPECIFY_VALUE
    MaxStep = SPECIFY_VALUE
    Minstep = SPECIFY_VALUE
    Increment = SPECIFY_VALUE
    Goal{ Name = "gate" Voltage=@Vg@ }
  ){ Coupled{ Poisson Electron Hole }

}

```