Silicon-Based Integration Technology for Terahertz Systems

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Low-loss integration technologies are essential for the design of high-frequency systems and components. Conventional PCB methods, such as metallic transmission lines, become challenging to employ in the Terahertz (THz) region due to significant ohmic and radiation losses. This thesis aims to design, fabricate, and test THz systems using a promising all-silicon multi-band integration technology: Effective Medium-Suspended Silicon Waveguide (EM-SSW). The technology utilizes high-resistivity silicon (HR-Si) and photonic crystal-like effective medium structures to construct waveguides with high-modal confinement. Additionally, suspending the waveguide's core minimizes substrate-modal interaction, enabling multi-band high-performance up to the THz range. To assess the practical performance of the proposed technology, our research investigates two systems: D-band and Y-band frequency up-converted sources. These devices are implemented using cascaded tripler blocks that leverage the non-linearity of GaAs Schottky diode chips to generate harmonic output power. The chips are mounted on the silicon wafer using an embedded-chip ultra-short wire bonding packaging technique within the high-precision three-mask process of the proposed integration technology. The system components, i.e., filters, matching circuits, transitions, and combiners, are designed using the proposed all-silicon technology and are hybrid integrated with the active chips to build the operational THz system. The excitation method uses contactless silicon probes made in-lab for on-wafer probing of the devices. A novel self-contained THz probe is effectively designed and fabricated to overcome assembly challenges at high frequencies. Two different THz probe designs are used to characterize the source prototypes at D-band and Y-band. Based on the simulations and measured data, the passive components exhibited high performance with the proposed integration technology and were effectively employed to build the prototype of the THz source. Upon excitation with a V-band input signal at the first stage, the generated power at D-band reached -1 dBm. Consequently, novel designs incorporating two combined signal branches were fabricated to adequately drive the second tripler stage with sufficient input power, resulting in an approximate Y-band power level of -18 dBm at a frequency of 0.5 THz.

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Cheers!

Dedication

This Ph.D. thesis is dedicated to my mother, Ola, my wife, Ghada, and my kids, Pearla and Zayd.

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List of Abbreviations

ADS	Advanced Design System
BW	Bandwidth
BWO	Backward Wave Oscillators
CIARS	Center Of Intelligent Antennas And Radios Systems
CPS	Coplanar Stripline
CPW	Coplanar Waveguide
DIG	Dielectric Image Guide
DRIE	Deep Reactive Ion Etching
DUT	Device Under Test
DWG	Dielectric Waveguide
EM-Simulator	Electromagnetic Simulator
EM-SSW	Effective Medium-Suspended Silicon Waveguide
EM-Waveguide	Effective Medium Waveguide
EPIC	Electronic-Photonic Integrated Circuits
FEA	Finite Element Analysis
FEM	Finite Element Method

FIR	Far Infrared Gas Laser
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
HBV	Heterostructure Barrier Varactor
HEMT	High Electron Mobility Transistor
HFSS	High Frequency Simulation Software
HMDS	Hexamethyldisilazane Solution
HR-Si	High Resistivity Silicon
JPL	Jet Propulsion Laboratory
MMIC	Monolithic Microwave Integrated Circuits
MmW	Millimeter Wave
MSL	Microstrip Line
PBG	Photonic Bandgap
PhC	Photonic Crystals
PM	Power Meter
PR	Photoresist
QCL	Quantum Cascaded Lasers
QNFCF	Quantum Nanofabrication And Characterization Facility
SBD	Schottky Barrier Diode
SEM	Scanning Electron Microscope
SIW	Substrate Integrated Waveguide

SOI Silicon On Insulator

THz Terahertz

TRL Through, Reflection, And Line

TWT Traveling Wave Tubes

VDI Virginia Diodes Incorporation

VNA Vector Network Analyzer

WR Rectangular Waveguide

List of Symbols

L	Length of transmission line or waveguide
λ	wavelength
$tan\delta$	Dielectric loss tangent
w_{V-band}	Width of V-band waveguide channel
w_{D-band}	Width of D-band waveguide channel
w_{Y-band}	Width of Y-band waveguide channel
h_{V-band}	Height of V-band waveguide channel
h_{D-band}	Height of D-band waveguide channel
h_{Y-band}	Height of Y-band waveguide channel
h_s	Height of silicon wafer
S_{21}	Insertion loss
k_0	Wave number
$\epsilon_\perp$	Effective permittivity for the perpendicular mode
$\epsilon_\parallel$	Effective permittivity for the parallel mode
β	Phase shift constant
ϵ_0	Free space permittivity

ζ	The filling factor
Px	Periodicity of PhC lattice in X-direction
Py	Periodicity of PhC lattice in Y-direction
V_c	Volume of the unit cell
V_h	Volume of the cylindrical holes
S_{11}	Return loss
R	Radius of the cylindrical holes
a	Lattice constant
ζ_{max}	Maxiumum filling factor
D	Dose of lithography process
R_s	The diode's series resistance
$R_{epitaxial}$	Epitaxial layer resistance
R_{spread}	Spreding resistance
R_{ohmic}	Ohmic contact resistance
f_c	Cutoff frequency
C_j	Junction Capacitance
α	Attenuation constant
Nd	Epitaxial layer doping concentration
ϕ_b	Built-in junction potential
q	Electron charge
I_o	Diode's reverse current

n	Ideality factor
K	Boltzmann's Constant
T	temperature
$G(v)$	Diode's equivalent conductance
CL	Conversion Loss
$P_{in_{source}}$	Input power of the source
$E_{x_{11}}$	Electric field of the horizontal DWG mode
$P_{out_{harmonic}}$	Output harmonic power
Zin	Input impedance
$Zout$	Output impedance
ηs	System efficiency
$E_{y_{11}}$	Electric field of the vertical DWG mode
w_s	Width of strip
s	CPW gap distance
ϵ_r	Relative permittivity
h	Substrate height

Chapter 1

Introduction

The Terahertz (THz) spectrum, encompassing frequencies ranging from 0.1 to 10 THz, possesses unique properties that have directed the attention of researchers toward an advanced generation of applications [8]. THz waves combine the features of millimeter waves and photonics. For example, THz non-ionizing radiation, which has low photon energy, is suitable for medical imaging of fatty tissues without causing damage to living tissues and DNA [9]. Another critical application of THz Spectroscopy is in material characterization, offering a viable solution because the interacting materials do not undergo any chemical changes due to molecular absorption. Consequently, it is well-suited for biomedical applications, such as distinguishing between healthy and cancerous tissues based on their absorption spectra in biochemistry [10]. Moreover, properties such as a high penetration depth and low scattering, combined with spatial resolution, give rise to various applications in quality control, security, and space imaging. For example, imaging defects in a manufacturing process and security screening for weapons and explosive materials [11].

Recently, modern communication systems operating beyond 100 GHz, such as D-band 6G systems, are rapidly flourishing due to their extremely high-speed data transmission and wide bandwidth [12].

Despite this potential, the terahertz frequency range remains one of the least utilized electromagnetic bands commercially, primarily due to the absence of reliable THz sources, components, and high-performance integration technologies [13]. As a result, the THz band has been referred to as the THz gap, and scientists and engineers have invested considerable effort into narrowing this gap. However, progress in terahertz systems, while notable, has not been as rapid. Until recently, there were only a few efficient and compact electronic-based systems with coherent THz sources available, particularly within the frequency range of 1 to 3 THz [14]. In addition, most of the research conducted in this area involves separate modular designs for different components, mostly adding system integration complexity, such as achieving precise alignment. Such challenges lead to additional design phases, including high-quality transitions across different module technologies, which increase the prototyping design cycle and cost. In summary, there is a need for a high-performance, cost-effective integration technology to build THz components, such as THz sources, on a single platform efficiently. Moreover, this technology shall be compatible with different types of existing technologies. [15]

1.1 Silicon Integrated Terahertz Systems

Extensive effort has been devoted to downsizing THz technology. Importantly, recent efforts have concentrated on solid-state semiconductor technology that can be manufac-

tured cost-effectively, leveraging economies of scale. This marks a significant shift from the pursuit of standalone ideal THz modules and reflects a more comprehensive approach to achieving novel properties at the system level, capable of enabling reasonably efficient functionality at the high-yield production level [16]. Playing the most significant role in the build of THz systems, THz sources can measure how effectively the integration technology and the system as a whole perform.

Power at millimeter-wave (mmW) frequencies can be generated using various methods, depending on the application's band. Oscillators, amplifiers, p-i-n diode generators, and other devices are commonly employed. However, utilizing these devices for generating THz frequencies presents challenges and has several limitations [17]. For example, semiconductor amplifiers have achieved a cutoff frequency of around 1 THz; however, operating at these extreme limits introduces design and modeling complexities, in addition to high fabrication cost [18]. Utilizing these on-chip active devices necessitates metallic on-chip interconnects. Although these interconnects are compact and compatible with conventional chip fabrication processes, metallic losses become dominant at THz frequencies when integrated with on-chip passive elements. Additionally, they occupy a comparatively large area on the die, leading to increased manufacturing costs [19].

To overcome the challenges that arise when integrating on-chip passive elements with active devices, one common approach involves separating interconnects and passive components from the chip design. These components are then integrated off-chip using a separate low-loss technology distinct from the chip. This strategy is known as hybrid integration, which entails integrating different technologies with low-loss transitions to leverage the advantages of each technology and ultimately achieve optimal performance. An example of

this hybrid configuration is the integration of metallic reduced-height split blocks; however, machining, positioning, and alignment become immensely complex and expensive at THz frequencies [20] [21] [22].

Electronic-based sources can generate THz frequencies in the lower range of the band, typically up to a few THz. The most widely adopted method to achieve this is solid-state frequency multiplication. This method involves a chain of frequency multipliers, including doublers and triplers, with relatively high conversion efficiency, driven by a conventional microwave source. However, a critical challenge is to develop an efficient, easily fabricated, compatible, and cost-effective THz integration technology that can accommodate all multiplier stages on a single platform. An alternative approach involves a modular design for each stage, with the input/output of each successive stage matched accordingly. However, this method is bulky and requires precise machining [23].

1.2 Motivation and Research Contributions

This research aims to develop a compact and low-loss silicon (Si)–based integration technology using a precise and cost-effective microfabrication process. Subsequently, the technology is intended to integrate a semiconductor frequency multiplication-based THz source on a single wafer platform that accommodates all the multiplier stages and to create a proof-of-concept prototype for a low-cost, scalable, and compact system. The targeted frequency for the prototype is 0.5 THz due to the limitations of available commercial semiconductor devices and in-lab test instruments. However, the proposed methodology can be extended to generate power at higher frequencies using different combinations of multipli-

cation stages. This vision was achieved through continuous developmental efforts focused on three main objectives: Si-based integration technology development, THz source design and system integration, and advanced silicon probe excitation. The research motivations and contributions are discussed in the following subsections.

1.2.1 Silicon Integration Technology

Silicon technology is promising and feasible as THz frequencies are approached. While materials generally exhibit high absorption of THz waves, certain materials such as high-resistivity undoped silicon (HR-Si), germanium (Ge), gallium arsenide (GaAs), quartz, and others show low absorption at THz frequencies [24] [25]. Such property makes them suitable for guiding channels of THz waves due to their minimal signal attenuation [26]. Table 1.1 displays the measured power absorption coefficients at the terahertz frequencies for the mentioned materials [27] [7]. High-resistivity silicon exhibits relatively low absorption of THz power. Hence, it is a suitable candidate for use as the wafer material to form the guiding structure of the host platform in the integrated technology. The HR-Si wafers are fabricated using the float-zone (FZ) process to ensure high purity. [5] [6].

Table 1.1: Reported measured power absorption coefficient of dielectrics [5] [6] [7]

	Absorption Coefficient (α,cm^{-1})	**Frequency (THz)**
HR-GaAs	0.2 / 0.4	0.25 / 0.5
Intrinsic Ge	$\approx$ 0.5	0.2 – 2
HR-Si	$\approx$ 0.025/ $\approx$ 0.15	0.1 - 2 / 0.1 - 4
Alumina	254 / 3870	1 / 3

Waveguides and transmission lines at lower frequency ranges, such as mm-Wave, are

typically supported by metallic ground planes [28]. However, the conduction loss results in significant attenuation at THz frequencies. Conversely, dielectric materials exhibit minimal loss and can be employed as handling substrates for the guiding structure when having lower permittivity than the guiding channel. Silicon-on-Glass (SOG) integration technology is considered one of the most successful in building high-quality interconnects up to 1 THz. The THz spectroscopy in [29] has reported the absorption coefficient and refractive index of different types of glasses, e.g., amorphous silica, quartz, Pyrex, etc. Silica and quartz, which result from fabrication processes involving other silicon dioxide compounds, exhibit similar absorption in the THz range, which is comparably low $\approx 2.7\,\mathrm{cm}^{-1}$ at 1 THz. Nevertheless, bonding to the HR-Si wafer poses a challenge due to the differences in thermal expansion coefficients. This adds complexity to the fabrication process and increases costs.

On the contrary, Pyrex exhibits a higher absorption coefficient in the THz range relative to silica and quartz. Nevertheless, it presents fewer challenges in the fabrication process due to its compatibility with silicon. Pyrex shares approximately the same thermal expansion coefficient as silicon and can be bonded using anodic bonding, a bonding process widely employed in Micro-Electromechanical Systems (MEMS) for device substrates [30]. However, the interaction between guided waves and Pyrex at THz frequencies should be minimized to prevent excessive attenuation in the substrate, as observed in the U-shaped SOG technology [31]. This requirement complicates the fabrication process, particularly concerning multi-band operation, which holds importance in our source implementation. The complexity arises from the guided mode's dependency on the channel's height. Additionally, patterning a glass substrate, as demonstrated in the corrugated and suspended SOG technologies, is not straightforward. As a result, Pyrex no longer remains an excep-

tional candidate as a handle material for THz applications.

Taking the above points into consideration, an all-silicon integration technology was pursued. This involves high-resistivity silicon wafers for implementing guided channels and handle layers. [31]. While it is challenging to maintain modal guidance using an all-silicon technology due to substrate leakage, this challenge can be overcome by utilizing silicon defects that function as tunable dielectric constant effective media. The structure is designed to support frequencies from the V-Band up to the THz range through two multiplication steps involving two frequency tripler stages. Each stage is analyzed to study the modal parameters of the structure and determine the proper excitation of the operating mode. Additionally, transitions between off-chip interconnect and integrated on-chip metallic lines are designed at each stage to ensure compatibility with the fabrication process and to optimize power transfer to and from the chip. The key contributions of this study are as follows:

1. The design and simulation of the proposed Effective Medium-Suspended Silicon Waveguides (EM-SSW) and the multi-band all-silicon technology components performing modal analysis for the operating bands of each multiplier stage. In addition, the utilization of photonic crystal-like (PhC) structures to function as embedded effective media;

2. The design of a three-mask double-sided lithography process to pattern the multi-band waveguides and the metal layer of the off-chip transitions.

3. The fabrication of the EM-SSW, designed to operate in the V-band, D-band, and Y-band, is conducted using the proposed integration technology. The fabricated

waveguide's performance is then measured to compare it with the simulated designs and to verify the success of the technology

1.2.2 Advanced Silicon Probe Excitation

RF probes play a crucial role in developing and testing RF components, as they enable direct measurements to characterize chip and RF system performance. Commercial RF probes are often used for developing small on-wafer chips up to debugging the final production boards; however, these probes are expensive and require direct contact with the measured samples, especially at millimeter wave and THz frequencies. Additionally, the fragility of the structures leads to difficulties in the setup process when working at THz frequencies. Consequently, there is a need for a low-cost, robust, and easy-to-set-up RF probing technology that covers frequencies up to the THz range [32].

Various types of RF probes are employed in the verification of RF components. Among the different types of commercial RF probes, dielectric waveguide (DWG) probes are highly favored due to their excellent performance up to the terahertz frequency range, low loss, and significantly lower cost. They also have a significant advantage over other direct contact probes since they enable contactless excitation, enabling repeatable measurements without causing damage to the samples and prolonging the lifespan of the probes [33]. DWG probes can function with various commercial technologies, exciting waveguides, and transmission lines. Furthermore, at high frequencies, such as millimeter waves and THz, the small features of samples increase the sensitivity to fabrication and alignment errors, fabrication costs, and metallic contact transition losses. Therefore, DWG probes offer an

easy setup RF probing technology that operates up to the THz frequency range.

Planar technologies such as Microstrip lines (MSL), Coplanar Striplines (CPS), and Coplanar Waveguides (CPW) are prevalent in MMIC packaging. These technologies are frequently employed as standard terminations for MMICs and interconnections within and between chips on the board. [34] As a result, high-quality transitions between different technologies are crucial, especially during prototyping and on-wafer component characterization. These transitions enable the reuse of RF probes regardless of their technology and structure, owing to the diversity of on-chip RF pad designs. Consequently, they offer a cost-effective and time-efficient solution, particularly when utilizing a contactless probing method that streamlines the calibration process [35].

Summarizing the previously mentioned requirements, the demand for a proper excitation method for different technologies used for on-chip and on-board levels is growing with the continuous development and exploration of high-frequency electronics such as mmW and THz bands. Therefore, a part of our research has been dedicated to designing contactless silicon probes, incorporating high-quality transitions to test the proposed THz sources and components. The significant contributions of this study are as follows:

1. We propose a design of silicon-based excitation probes with high-quality transitions for exciting dielectric waveguides, MSs, CPWs, and CPSs. The probes and transitions are fabricated, measured, and, importantly, used in characterizing the proposed THz components and systems of our research;

2. We introduced an enhanced version of silicon-based probes to address the challenges arising from the packaging and assembly of conventional probes at THz frequencies.

The new probes feature a packaging component made of silicon, with a guiding probe structure similar to the silicon ribbon waveguide.

1.2.3 Terahertz Source Integration

Among all THz power generation methods, two primary categories are leading the significant progress in THz source research: photonic-based and electronically-based methods [36]. Photonic sources, such as lasers, can directly generate high THz power, i.e., not through harmonic power generation. However, they are limited by the materials used in the technology [37]. In other words, they require materials with sufficiently small bandgaps to generate power in the terahertz range. For instance, pumped gas lasers, vacuum electronic devices (VEDs) such as backward wave oscillators (BWO), and traveling wave tubes (TWT) are commonly used [38], as well as solid-state lasers, e.g., silicon lasers and p-doped germanium lasers [39]. Far Infrared Gas Laser (FIR) sources are optically pumped lasers capable of generating power in the low terahertz range (0.5 - 3 THz) at levels of tens of milliwatts [40]. However, the bands available for FIR sources are highly restricted due to the discrete nature of molecular transitions. On the other hand, tubes such as BWO and TWT are highly efficient and can generate power in the THz range, albeit limited to only a few milliwatts. Nevertheless, they have bulky sizes, limited tuning capabilities, and a short lifespan. Solid-state lasers, such as silicon lasers, can generate power in the THz range, up to hundreds of milliwatts; however, they require cryogenic cooling and exposure to high magnetic fields.

Another THz power generation photonic method is *frequency down-conversion*. Down-

conversion THz sources are based on the principle of converting an optical signal to a lower harmonic in the terahertz range [41]. One commonly used method for this is optical heterodyne using photo-mixing. This method involves combining the power of two optical laser sources and mixing them using a photo-diode to generate power in the terahertz range. However, the performance of this method is poor in terms of frequency stability and phase noise compared to other sources, requiring an extra phase-locked loop circuitry to maintain frequency stability. Despite this limitation, this method can still generate a few milliwatts of power for frequencies down to 0.1 THz [42].

Moreover, Terahertz Quantum Cascaded Lasers (THz-QCLs) are rapidly developing and increasingly significant THz sources for several reasons. One important reason is that, unlike other diode lasers, they are not dependent on the material used, such as the recombination energy and bandgap. Furthermore, QCLs are already dominant in mid-infrared semiconductor lasers, which means that the technology has already been studied and achieved progress. THz-QCLs consist of tens of alternating layers of semiconductor materials that form quantum energy wells, which can confine electrons to specific energy states. When voltage is applied, electrons are driven, and photons are emitted as their energy transfers from one state to another in regions named active regions. The output wavelength depends on the structure of the active region's layers rather than the material itself, thus eliminating the material dependency issue in lasers. Consequently, the generated output power from the THz-QCLs extended to the THz gap; however, the cost of the source is high due to the need for high-precision low-noise drivers and stable temperature controllers [43].

On the other hand, electronic sources can generate power up to a few terahertz, but

the available power diminishes as the frequency rises. Although several methods exist for generating power at millimeter waves, these methods are constrained and face limitations as they approach the terahertz region. For instance, semiconductor amplifiers based on various technologies, such as CMOS and BiCMOS, encounter restrictions determined by the cutoff frequency of the device [16]. However, significant progress is still required to extend this frequency limit into the THz range. High Electron Mobility Transistors (HEMTs), Heterojunction Bipolar Transistors (HBTs), and recently developed THz transistors and diodes have the potential to generate power slightly beyond 1 THz [44]. Furthermore, the Gunn-diode-based harmonic oscillators can produce acceptable power up to 0.5 THz, and a resonant tunneling diode fundamental oscillator can generate power at 1 THz [45].

Up-conversion THz sources employ a chain of frequency multipliers to generate the harmonics of a fundamental millimeter wave signal in the THz range. Various types of THz sources utilize this method, including Transistor-Based Multipliers, Heterostructure Barrier Varactor (HBV) Multipliers, Sideband Generators, and GaAs Schottky Barrier Diode (SBD) Based Multipliers [46] [47]. The maximum operating frequency of transistor-based multipliers has been pushed beyond the THz range. For instance, InP HBTs and HEMT can generate 10 mW of power at 0.3 THz [48]. Sideband generators work similarly to frequency multipliers; however, they mix two close millimeter wave signals to generate summation and difference harmonics and filter out to leave only the upper sideband. HBV multipliers have symmetric C-V characteristics suitable for operating odd harmonics without biasing, as the capacitance modulation region is centered at the zero-bias point. Therefore, they are likely used to implement triplers and quintuplers [49]. They have high voltage handling and are often used at the lower end of the THz band as the initial stage of

the chain due to their high power handling capability. However, the conversion efficiency of the HBV still needs to be higher to work at the higher-end stages [50].

In recent years, significant advances have been made in using GaAs Schottky barrier diodes for frequency multiplier-based terahertz sources. These diodes can generate higher-order harmonics of an input signal using either reactive or resistive nonlinearity. Well-matched embedded impedances can efficiently generate power at the output harmonic frequencies. Compared to other diodes, GaAs barrier diodes are the most efficient in generating harmonic frequencies in the THz range [2]. To design a frequency multiplier-based THz source with an output beyond 1 THz, several multiplier stages can be cascaded in any combination of doublers, triplers, or higher orders [50]. Doublers and triplers are the focus of most diode devices, with doublers being simpler to design and triplers requiring input/output filtering to eliminate unwanted frequencies. However, using a balanced diode configuration, such as an anti-parallel connection, can simplify the circuitry as the nature of the configuration filters out the even harmonics [2].

Based on the previously mentioned points, we introduce frequency multiplier-based THz sources that utilize planar Schottky barrier diodes as non-linear devices. These sources are integrated into silicon wafers using all-silicon technology. All passive components of the system, such as interconnects, filters, and transitions, are designed to maximize the overall conversion efficiency of the system. The significant contributions of this study are as follows:

1. The design of two frequency tripler stages that provide outputs at the D-band and the Y-band utilizing a pump signal at the V-band using a commercial anti-parallel

GaAs SBD supplied by Virginia Diodes Incorporation (VDI). The hybrid integration of the chip was achieved using an ultra-short wire bonding packaging, involving wire bonds with lengths of less than 75 μm, to minimize the parasitic effects and push the limits of current wire-bonding techniques to work at the THz;

2. The design involves the implementation of photonic crystal filters using all-silicon wafer technology at the V-band and the D-band, serving as crucial components for each tripler stage. These filters capitalize on the bandgap operation of PhCs to establish a rejection band at the respective output frequencies;

3. All components and systems are fabricated on the same wafer, leveraging the rapid prototyping capabilities offered by the all-silicon integration technology. The fabrication and packaging processes are meticulously fine-tuned at the Quantum Nanofabrication and Characterization Facility (QNFCF) at the University of Waterloo. The measurements for all components were conducted in the laboratories of the Center of Intelligent Antennas and Radios Systems (CIARS) to validate the functionality of the source prototypes;

4. Introducing a modified version of the triplers using power combiners to increase the systems' overall conversion efficiency, increasing the output power.

1.3 Research Objectives and Thesis Outline

The objective of this Ph.D. research is to develop solutions for multi-band hybrid integration of THz systems on silicon wafers, specifically focusing on frequency multiplier-based

THz sources in our research. To achieve this overarching objective, the following milestones are examined sequentially:

1. To develop an all-silicon integration technology that is cost-effective, high-performance, and sufficiently mature to accommodate components operating across multiple frequency bands, including the THz range;

2. To introduce appropriate excitation methods for various chip and PCB technologies and employ the designed probes to stimulate all the THz outputs of components and systems developed through our research;

3. To deliver a prototype of harmonic-based frequency triplers capable of operating independently and in a cascaded configuration to generate power within the THz range.

Figure 1.1 presents a set of devices that glimpses the outcomes of our research. The devices include D-band and Y-band triplers, PhC filters, all-silicon waveguides, and 0.5 THz sources. The compatibility of the multi-band integration technology allows the fabrication of different devices on the same wafer, offering a reliable and swift method for testing the prototypes in addition to system designs at the production level. Alongside their comparable efficient performance and accuracy, this approach significantly diminishes manufacturing and testing costs during the prototyping stage, reducing to less than 10% associated with the metallic split-block machining. The upcoming chapters will discuss in detail the design steps and the performance of these devices.

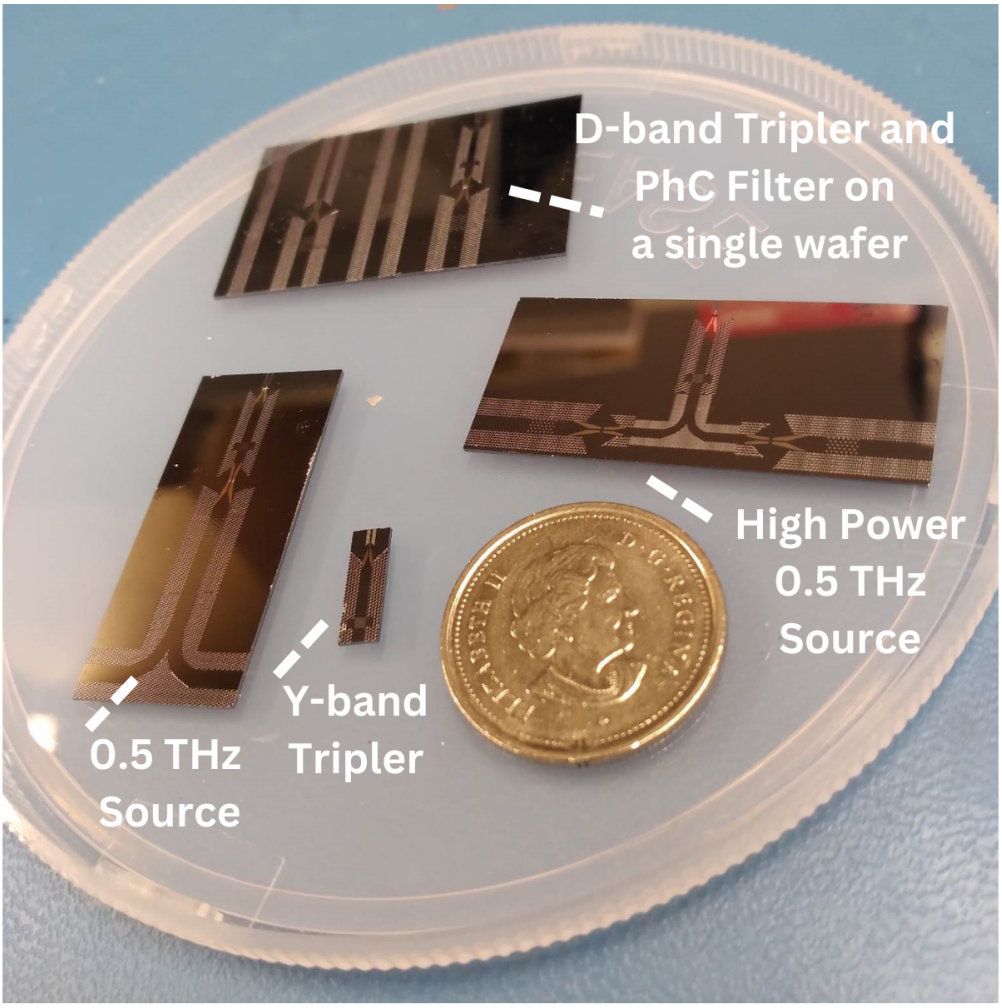


Figure 1.1: Different fabricated devices using the rapid prototyping all-silicon technology.

The structure of the thesis is organized as follows. Chapter 2 provides a comprehensive literature review of the most relevant work. Chapter 3 introduces a novel all-silicon integration technology based on silicon waveguide operation and photonic crystal-like effective structures. Moreover, the chapter details the fabrication process of the proposed platform and evaluates its performance through testing different-band waveguide struc-

tures. In Chapter 4, contactless dielectric probes designed for exciting different PCB and chip technologies up to the THz frequency range are investigated. We outline the design of these probes along with the required modal transitions to excite various transmission lines. Chapter 5 maps out the design steps of the proposed THz sources, encompassing all essential components required for building each tripler stage. We delve into the design of Photonic Crystal-based filters, which serve as pivotal blocks within our tripler designs. Moreover, we offer a comparative analysis between the results of the fabricated prototypes and the simulated designs. Finally, Chapter 6 concludes the research endeavor, providing insights into future research directions.

Chapter 2

Literature Review

In this chapter, we present the related work in the literature that inspired our designs. Such work can be divided into three sections: available THz integration technologies, probing techniques, and frequency multiplier sources. First, we introduce the most recent and related high-performance integration technologies at the THz, especially silicon-based platforms. Next, a brief introduction to the measurement setups used in characterizing THz systems is provided, focusing on the different types of probes at such high frequencies. Finally, we summarize the concept of frequency up-converter THz sources, listing a few of the most related systems.

2.1 THz Integration Technlogies

Over the past two decades, there has been a growing interest in THz radiation, leading numerous scientists and engineers to focus on developing high-performance millimeter wave

(mmW) and THz systems to fill the THz gap. Two primary methods have been utilized in creating THz hybrid integrated circuits: the use of reduced height metallic split-blocks through the planar design of traditional microwave metallic waveguides and the use of dielectric waveguides inspired by the technology used in photonic integrated circuits [51].

The use of metallic waveguides in the microwave frequency band is widespread due to their low insertion loss [52]. However, their bulky nature makes integration with planar circuit technologies complex. Various connectors and transitions have been developed to address this issue to convert the TE_{10} mode to planar transmission line modes. While these transitions provide acceptable insertion loss for microwave frequencies, their transition loss experiences a notable increase at millimeter wave and terahertz frequencies [53]. Therefore, researchers have developed an alternative method by realizing a planar form of metallic waveguides, such as the substrate-integrated waveguide (SIW) [54]. The SIW structure consists of two parallel plates on both sides of a substrate with periodic metallic vias in the substrate, replacing the side conducting walls. Although this structure provides high performance in terms of loss and compactness for the lower band of the millimeter wave, it faces difficulties when frequency increases up to the sub-millimeter and terahertz bands. One of the challenges is fabricating miniature metallic vias with high precision, which is critical at THz since the field confinement is determined by the proper design of the size and positioning of the periodic vias [55].

Planar miniaturized metallic waveguides overcame the challenges accompanied by fabrication. These waveguides have complete metallic sidewalls instead of vias, and their high precision requirement is at mmW/THz frequencies. However, the fabrication of suitable conducting sidewalls is a complex process. Micromachining techniques offer multiple

methods to fabricate these waveguides [56]. One way involves forming a planar dielectric channel and coating it with metal. The channel can be formed using photolithography, wet etching of silicon substrate, or deep reactive ion etching (DRIE) of silicon substrate [57]. However, the high etching selectivity required when fabricating the vertical sidewalls is a problem. To overcome this issue, the channel is split into two halves and processed separately, then combined to form the channel, a method known as a split-block waveguide [58]. This method requires precise alignment between the two blocks to maintain the proper mode within the channel, which can be challenging. Despite miniaturized planar metallic guides, including split-block waveguides, providing acceptable performance at THz frequencies, integrating them with active devices is expensive and poses technological challenges. Achieving precision in transitions between the waveguide and the chip is difficult. For instance, [59] implemented a transition by placing an E-plane probe inside the waveguide to couple the TE_{10} mode to CPW mode.

One alternative to miniaturized planar metallic waveguides is using highly transparent and low-loss dielectric materials as the primary guiding structures [60]. This approach is based on the technology used in optical integrated circuits and has gained interest at the mmW and THz frequencies as an alternative to conventional PCB technologies. The operation band of such waveguides depends on the dimensions of the guiding channel, which utilizes the concept of total internal reflection, unlike surface currents as in metallic technologies providing independence on high-frequency degrading phenomena, e.g., skin effect. Unlike metallic waveguides, the electric field of guided modes in dielectric waveguides is not confined to the filling material. As a result, the packaging of guiding channels is a core challenge as it is required to maintain modal confinement and suppress field radiation,

coupling, and effective modal index dependency on substrate materials. Such degradation phenomena dominate as frequency increases, i.e., reaching the THz region. Therefore, most high-frequency limitations of dielectric technologies depend on providing high-quality packaging that can provide less field interaction with surrounding materials, in addition to mechanical stability and proper integration with active devices [61].

Researchers of different silicon technologies at mmW and THz frequencies are mainly competing to provide innovative packaging solutions that can push the operation limit to the THz gap. Handle structures or substrates are major performance components since they are in direct contact with the guiding channels, thus highly contributing to the modal attenuation while propagating through the waveguide [62]. There are various choices for handle structures: Grounding plane-based structures, such as image guides, are composed of a silicon channel on a metallic ground layer. The grounding plane acts as a mirror for the guided mode, providing mechanical support and heat dissipation for active components, which are integrated on the same platform. However, the grounding plane contributes to conduction losses, which can be reduced by inserting a low permittivity insulating film between the slab and the grounding plane. This structure is called an insulated dielectric image guide. Another form of the dielectric image guide is the silicon-on-insulator dielectric image guide (SOI-DIG) [63]. It is similar to the principle of operation of the insulated dielectric image guide built with alumina. The difference is using high-resistivity silicon wafers for building guiding structures and silica as an insulating material. The reported attenuation shows better performance up to the mmW D-band; however, extending beyond this band dramatically increases the attenuation of the structure due to the presence of the ground plane [64].

Removing or isolating the ground plane is a crucial requirement for the THz operation of silicon waveguides. Other methods, including hard dielectric materials such as glass, are preferred to confine power in guided channels while retaining the benefits of mounting components, electrical insulation, low-power heat sink, and mechanical support. Figure 2.1 illustrates examples of silicon waveguides built on glass substrates. These waveguides are all fabricated using photolithography and deep reactive-ion etching (DRIE). DRIE is essential for producing such vertical structures accurately with a relatively high aspect ratio, unlike wet etching technology, which generates isotropic etching with inaccurate undercuts. All technologies strive to achieve the performance level of the ribbon waveguide, i.e., a single HR silicon channel suspended in the air, by providing structures that minimize guided-field interaction with the substrate. For example, ridge waveguides underperform in comparison to other waveguides as the guiding channel is directly attached to the substrate; therefore, the material of the substrate should be of low loss, e.g., Silicon-BCB-Quartz (SBQ), to achieve comparable performance at the THz. However, the thermal incompatibility of Quartz with silicon presents challenges in the bonding process; thus, there is an interest in using Pyrex as the substrate material despite its relatively higher absorption at THz. The reported attenuation constant α is 0.053 dB/mm at 90-110 GHz for silicon-on-Pyrex [65] [66]. On the contrary, the silicon-on-quartz reported in [67] has an attenuation constant of 0.026 dB/λ at 0.5 THz.

To overcome the limitation of using high-loss substrate materials, the common feature of all proposed solutions is that they aim to eliminate the direct attachment of guiding silicon to the cladding. For instance, silicon rib waveguides reduced substrate interaction using a thin silicon layer on top of the substrate. The attenuation constant (α) of rib

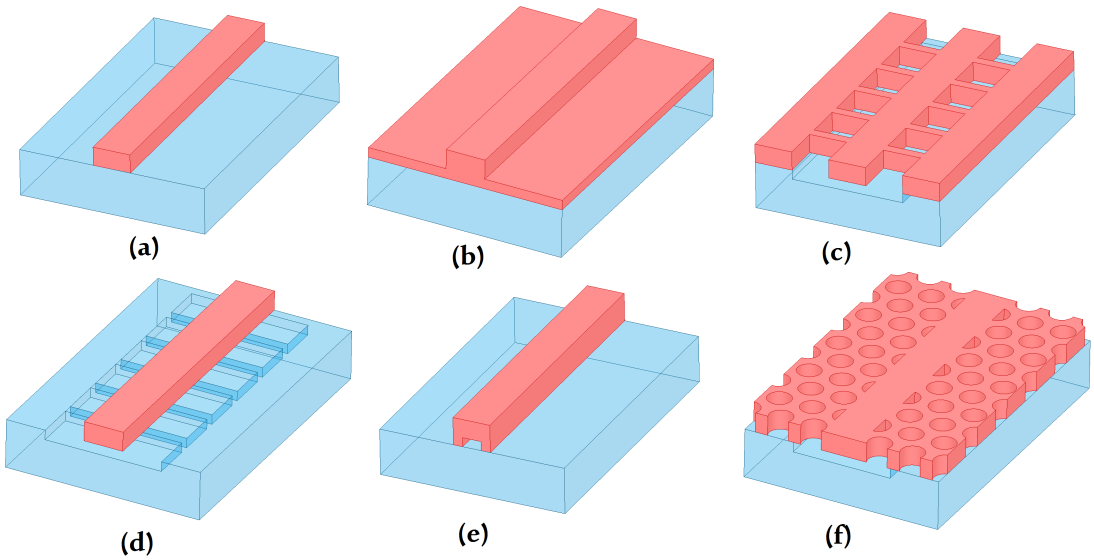


Figure 2.1: Cross section view of THz silicon waveguides (a) ridge waveguide (b) rib ridge waveguide (c) Suspended SOG (d) corrugated SOG (e) U-shaped SOG (f) PhC waveguide.

waveguides is measured to be 0.107 dB/mm in the frequency range of 750 GHz to 1 THz. Although rib waveguides offered better performance than ridge waveguides, the confinement of the guided mode in silicon is limited by the maximum thickness of the rib layer that avoids substrate leakage. In contrast, suspended and corrugated SOG waveguides utilized substrate etching to minimize the interaction with Pyrex; suspended SOG used periodic silicon beams to support the floating waveguide, while corrugated SOG used periodically built thin Pyrex beams attached to the waveguide. The reported attenuation constant α is 0.0349 dB/mm at 500 GHz and 0.021 dB/mm at 300 GHz for suspended and corrugated SOGs, respectively. On the other hand, the U-shaped SOG is designed to position the guiding silicon a level higher than the Pyrex using two side-supporting silicon beams. This is achieved by adding an extra mask lithographic process to pattern the supporting

silicon beams. Therefore, no additional patterning or sophisticated etching in the Pyrex is required. The U-shaped SOG can operate up to 1.1 THz, and the recorded attenuation constant α is 0.024 dB/λ.

All-silicon technologies reveal the potential of building complete THz systems independently of cladding, achieving total modal confinement in the silicon core and surrounding air. One of the significant structures in realizing all-silicon integration is Photonic Crystals (PhC). A photonic crystal lattice can be used in two modes: Photonic Bandgap Structures (PBG) and Effective Medium Operation (EM). Although both operation modes share a similar structure, they have different working principles. PBG depends on the rejection of electromagnetic propagation at tuned frequency bands designed by the lattice structure. Meanwhile, EM operation utilizes the lattice's inhomogeneity to create a medium with a tunable effective modal index [68] [51]. PBG and EM waveguides have achieved excellent performance, reporting an attenuation constant α of ¡0.01 dB/mm at 300 GHz and 0.005 dB/mm at 350 GHz for PBG and EM, respectively. Although EM has the advantage of increased bandwidth over PBG waveguides, the size of the PhC lattice is comparably smaller than that of PBG to maintain medium homogeneity, which presents a fabrication challenge. Despite these challenges, PhC-based technologies are considered promising in THz integration. Table 2.1 compares the attenuation constants for the recognized THz silicon technologies.

Table 2.1: A comparison between different types of THz waveguide technologies

Technology	Study	Attenuation Constant	Frequency
HR Si Ribbon	[69]	0.0087 dB/mm	140-220 GHz
Ridge SOG	[66]	0.053 dB/mm	90-110 GHz
Suspended SOG	[66]	0.0349 dB/mm	440-500 GHz
Corrugated SOG	[65]	0.021 dB/mm	440-500 GHz
U-SOG	[31]	0.061 dB/λ	0.9-1.08 THz
Rib Waveguide	[70]	0.107 dB/mm	750–1 THz
SBQ	[67]	0.026 dB/λ	500-508 GHz
Metallic Waveguide	[67]	0.06 dB/λ	500-750 GHz
PBG-PhC Waveguide	[71]	0.01 dB/mm	324-361 GHz
EM-PhC Waveguide	[71]	0.005 dB/mm	260-400 GHz

2.2 THz Systems Excitation and Probing

The measurement of RF device characteristics at the chip level is enabled by RF probes, which are essential throughout the design and prototyping stages. Tektronix developed these probes in the 1980s, and they have since evolved with a significant increase in their maximum frequency. The connector typically limits the maximum frequency to interface the RF probe with the test equipment, even though the demand for operating frequencies up to 1.1 THz is required. Standardized coaxial connectors, as shown in Figure 2.2, offer a continuous operating frequency range up to a maximum frequency determined by the connector type, such as 40 GHz for the 2.92 mm (K) connector, 67 GHz for the 1.85 mm connector, and 110 GHz for the 1 mm connector. Coaxial connectors with dimensions

operating above 220 GHz become impractical, and the only option is rectangular waveguide interconnects. While these interconnects can operate up to 1.1 THz, they have limited bandwidth and are expensive [34].

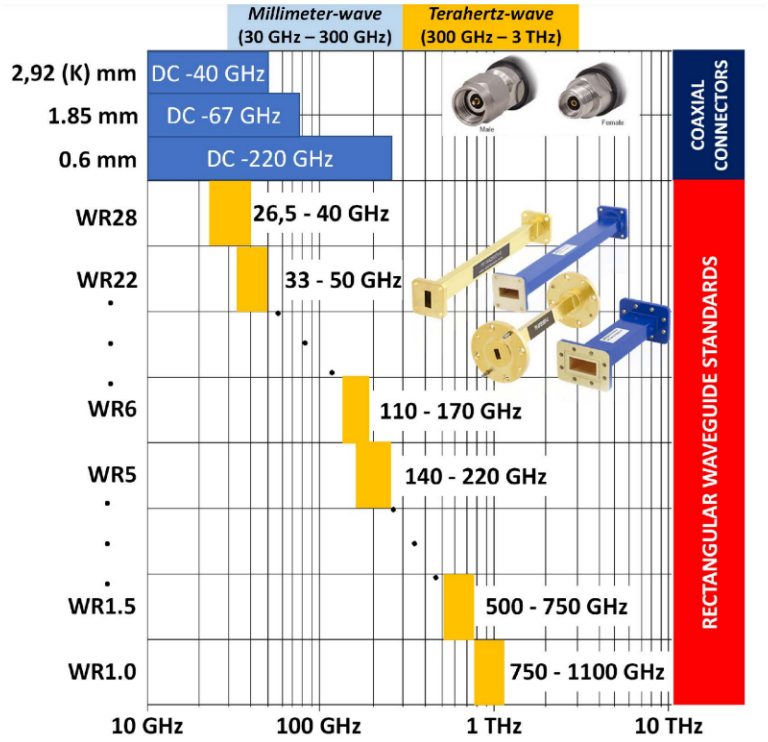


Figure 2.2: Coaxial and rectangular waveguide standards at the mmW and THz [1].

Accurate and repeatable measurements of RF devices during design and prototyping are desired features that rely on RF probes. These probes connect to the device under test (DUT) through a 50Ω RF planar transmission line at the probe tip. However, at higher frequencies, the spacing between DUT pads decreases to the μm scale, making this approach challenging. Achieving measurements above 100 GHz requires precision in

probe placement to avoid phase uncertainty and the excitation of parasitic modes. It's also important to minimize probe crosstalk and the physical wear of the probe tip. Despite these challenges, the correct design of RF probes is crucial for achieving precise and repeatable measurements in the mmW and THz wave ranges [4].

Contactless probing offers numerous advantages, including providing repeatable measurements without damaging landing pads or probe tips, avoiding contact between pads and probes at THz frequencies (which is crucial due to the fragility of DUTs' small features), and conferring more stable measurements. Several non-contact probing methods exist. For example, the quasi-optical method using mirrors and a hemispherical lens in [72] can operate up to 750 GHz; however, the setup is complicated, and the insertion loss of the method is high. Furthermore, dielectric waveguide coupling methods are more efficient. The DWG probe in [33] is simple, low-cost, and performs well for DWG excitation. On the other hand, the DWG probe in [73] is a more sophisticated version of the previously mentioned DWG probe; however, it introduces more sources of measurement error and requires more complicated metallic packaging. The dielectric rod antenna probe in [1] relies on near-field coupling to a linear-tapered slot antenna, but its measured performance degrades after the V-band. Our work utilizes the DWG non-contact near-field coupling method to excite different transmission lines using high-quality transitions up to the THz.

2.3 THz Frequency Multiplier-Based Sources

Over the past few decades, the demand for terahertz technology in fields such as space exploration, astronomy, earth science, and others has driven advancements in terahertz

sources, detection, and systems. Terahertz technology has found use in satellites like the NASA Upper Atmosphere Research Satellite (UARS) and the European Space Agency's Rosetta for monitoring atmospheric and cosmic phenomena [71]. Terahertz technology also holds potential applications in imaging, biological science, high-speed communication, and more. Several organizations, including the Jet Propulsion Laboratory (JPL) in the US and Nippon Telegraph and Telephone in Japan, have developed terahertz-based imaging and communication systems [50] [74]. In [75], a long-distance terahertz wireless communication system is proposed based on 240 GHz, achieving high data rates. This section offers an overview of the frequency multiplier-based THz sources relevant to this study. The main objective of our device is to demonstrate the capabilities of the multi-band all-silicon EM-SSW integration technology in hosting a fully integrated THz system. Therefore, the following survey discusses the various THz GaAs Schottky diode-based multiplier sources from the perspective of integration/packaging complexity, technology cost, and system performance—emphasizing not only devices' performance regarding output power level enhancement but also design methodology and system architecture.

2.3.1 THz Schottky Diode Technologies

Schottky diodes are a well-established technology used in terahertz solid-state sources due to their high cutoff frequency, simple structure, and mature international technology of frequency multipliers. Terahertz frequency multipliers have made remarkable progress in various research institutions, including Virginia Diodes Inc., JPL, ACST, and Teratech. Compared to photonics and vacuum electronics, terahertz frequency multipliers have

gained popularity as a research field due to their compact structure, lightweight, low power consumption, and stable performance [76]. Schottky diodes used in terahertz frequencies are mainly based on GaAs or GaN materials, with an epitaxial layer of varying doping concentration. The cathode and metal form an ohmic contact, while the anode and metal form a Schottky contact with two types of structures: whisker-contacted diodes and planar Schottky diodes. Whisker-contacted Schottky diodes use a "honeycomb" combination for metal point contact, commonly used in the millimeter wave and low terahertz band to achieve good performance. However, they have several disadvantages, including poor reliability, complex and accurate modeling, and low physical strength, making integration and assembly challenging, thus limiting improvements in their operating frequency.

The development of planar Schottky diodes has led to easier fabrication and installation, yet their high parasitic capacitance presents a challenge to high-frequency performance. Surface channel planar Schottky diodes, air-bridged planar Schottky diodes, and Quasi-vertical planar Schottky diodes are the main types of planar diodes, offering significantly lower parasitic capacitance and finding widespread use in terahertz devices. [77] introduced a technique for producing low parasitic surface channel planar diodes using anisotropic etching of different GaAs lattice planes, as shown in Figure 2.3(a). These diodes demonstrated the first planar Schottky varactor diode at 180 GHz in 1993 and were subsequently developed into a commercial product line by Virginia Diodes, Inc. The surface channel design reduces the parasitic capacitance between the anode and cathode, and the distance between the ohmic contact and the anode can be controlled using photolithography [78].

The fabrication process of the air-bridged planar Schottky diode chip was developed at JPL to streamline assembly and enable the production of a larger number of chips using

3 to 4-inch wafer batch processing. The mesa structure is defined through reactive ion etching (RIE), which offers better control over mesa dimensions and sidewall profile and reduces parasitic resistance and capacitance. A significant advancement in this process was the creation of a robust air bridge, which is formed simultaneously with the anode to minimize misalignment and processing steps [2]. This technology allows for the creation of devices surrounded by frames that aid in handling and mounting within waveguide structures. Selective etch layers grown using molecular beam epitaxy (MBE) generated a substrate thickness of a few micrometers, reducing substrate effects and increasing the operating frequency. This process has produced some of the highest-frequency working mixers and multipliers with exceptional performance. The structure of the air-bridged planar Schottky diode is depicted in Figure 2.3(b).

The planar quasi-vertical diode, illustrated in Figure 2.3(c), was developed with the Schottky contact formed on the front side of the epilayer, and the cathode ohmic contact formed on the backside directly below the corresponding Schottky contact [79]. This design mitigates electric current crowding effects, reducing ohmic losses and enabling the backside ohmic metal to function more effectively as a heat spreader than a GaAs membrane. Despite its higher fabrication complexity, 664-GHz mixer diodes have been reported to perform competitively [80]. Integrating quasi-vertical diodes with RF circuitry could yield benefits. A quasi-vertical Schottky diode demonstrated 160-GHz quadrupling integrated with RF circuitry by bonding a GaAs substrate to a high-resistivity silicon-on-insulator (SOI) wafer with pre-formed RF features that were later etched [81]. While planar structures enable monolithic integration, they also possess drawbacks like additional parasitic capacitance and series resistance compared to whisker-contacted diodes. However, these

latter planar diode technologies compete in performance with whisker-contacted diodes [2].

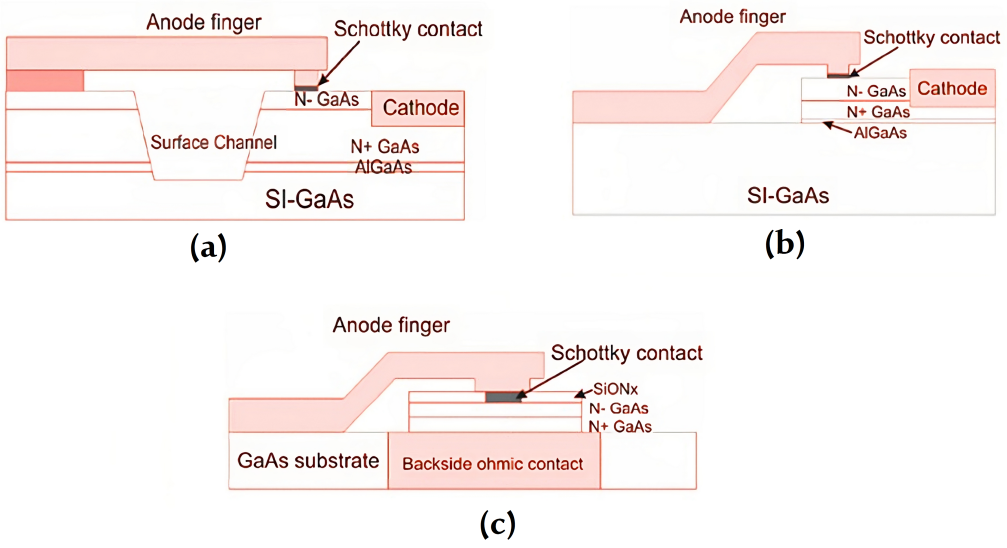


Figure 2.3: Different planar Schottky diode technologies (a) Surface channel planar Schottky diodes. (b) Air-bridged planar Schottky diodes. (c) Quasi-vertical planar Schottky diodes [2].

2.3.2 Schottky Diode-Based Frequency Multipliers

An overview of various terahertz sources is provided in this subsection, focusing on the hybrid integration of traditional terahertz solid-state devices with discrete diodes. These circuits are assembled on the conductive transmission lines of the circuit using Flip-chip packaging. Hybrid integrated circuits were initially utilized for lower terahertz frequencies due to their simple process, affordability, and relatively easy diode assembly. For terahertz sources based on Schottky diodes, doublers and triplers are standard components [82]. The

design of frequency doublers in terahertz technology is straightforward, involving independent input and output impedance matching, which simplifies the overall device design. Additionally, balanced multipliers result in significant rejection for undesired harmonics without requiring extra filtering. Creating terahertz triplers is more complex than doublers, as they require input and output filters to ensure proper isolation for even harmonics. While triplers have lower conversion efficiency than doublers, they are commonly used in cascading terahertz source systems due to their ability to produce a higher frequency third harmonic output [83]

In [84], researchers demonstrated a source that utilizes discrete Schottky diodes and operates at 270-320 GHz, providing up to 35 mW of power without power combining and using split-block technology. The doublers developed for the 135-160 GHz and 270-320 GHz ranges exhibit high power handling capabilities and state-of-the-art efficiencies. The doubler designed for 300 GHz achieves a conversion efficiency exceeding 25% within the band, peaking around 35%, which marks the highest reported efficiency using discrete diode technology at these frequencies. This enables the source to generate more than 30 mW with an input power of 100 mW. Furthermore, the source in [85] presents data for a fixed-tuned high-power Schottky diode frequency doubler operating at 180-200 GHz. The doubler was designed for input power ranging between 100-200 mW and demonstrated a peak efficiency surpassing 42.5% along with an output power exceeding 80 mW within the 185-195 GHz band. In [86], a high-power 220 GHz frequency tripler is presented based on a pair of GaN planar Schottky barrier diode chips arranged in a chain. Unlike traditional designs, the diodes are directly connected to a metal block to achieve improved heat dissipation. The proposed tripler can effectively operate under input power at the watt level due to the power

endurance capacity of GaN material. The pair of diode chips are mounted directly across the metal diaphragm, allowing the RF field to couple directly onto the diode chains. The output power of this frequency tripler is 17.5 mW at 219.5 GHz, with the best efficiency of 1.93%, achieved with an input power of 900 mW. In [87], an unbalanced tripler operating at 225 GHz is presented, utilizing a pair of parallel discrete Schottky varactor chips. The circuit is constructed on a 50 µm-thick quartz substrate. The output power exceeds seven dBm at 228 GHz, and at 224 GHz, the output power is 12.3 dBm when driven with 23.8 dBm of input power at room temperature. Table 2.2 provides a performance comparison of several examples of discrete-chip planar Schottky diode multipliers.

Table 2.2: Performance comparison of different types of hybrid-integrated THz multipliers

Type	Study	Efficiency %	Frequency [GHz]
Doubler (X2)	[84]	25-35	270-320
Doubler (X2)	[85]	45	180-200
Tripler (X3)	[86]	1.93	219.5
Tripler (X3)	[87]	7.3	215-228

Manual assembly of the circuit can lead to a degradation in performance. Furthermore, the use of hybrid integrated circuits is constrained by the performance of the diodes, which might not meet the actual requirements. As a result, achieving medium to high terahertz frequencies with hybrid integrated circuits proves challenging. With the development of new materials, traditional terahertz solid-state devices have undergone innovative changes. The direct growth of diodes on the circuit substrate through the semiconductor process eliminates the need for manual assembly and significantly enhances terahertz solid-state

device performance. Monolithic integrated circuits reduce errors stemming from manual assembly and uncertainties linked to circuitry. The fusion of monolithic technology and diode semiconductor technology propels terahertz solid-state circuit technology forward and enhances diode design.

In [88], a series of submillimeter-wave frequency multipliers has been developed for high-power operation. The frequency multiplier chips have been designed and fabricated in the range of 100 GHz to 1 THz, focusing on higher power operation. The results demonstrate that a single-chip 105-120 GHz tripler achieves efficiencies of approximately 30%, while a single-chip 170-200 GHz doubler achieves 25% efficiency when driven with 500 mW. By utilizing in-phase power-combining techniques, an 840-900 GHz frequency multiplier chain has been designed and fabricated in [89] to deliver over one mW of power at room temperature and up to 2 mW at 882 GHz when cooled to 120K. The chain comprises two cascaded frequency triplers driven by a power amplifier module, with the first stage utilizing four power-combined chips and the last stage using two.

The device in [90] is a continuous wave coherent source covering 2.48-2.75 THz, with over 10% instantaneous tuning bandwidth and 1-14 μW output power at room temperature. It utilizes a synthesizer, power amplifier, and three cascaded frequency triplers. Furthermore, the researchers in [91] present the design and performance of a 135-150 GHz frequency tripler that employs waveguide resonator filters for low-loss impedance matching. They use the resonator filters to combine the functionality of three component blocks: filters, matching, and waveguide-to-chip transitions. The device is bias-less, has a 15 GHz output bandwidth, and was measured to have a conversion loss of 13.1-14 dB across the band at an input power of 17 dBm. The design approach transfers most of the

tripler's matching networks from microstrip circuitry to lower-loss rectangular waveguide resonators, thus improving performance for sub-millimeter-wave and THz frequencies. Table 2.3 compares the performance of some examples of MMIC-based planar Schottky diode multipliers.

Figure 2.4 depicts a 1.5 THz source developed by JPL researchers. The MMIC amplifier is used to increase the pump signal power in the first stage. It's important to note that the dimensions of each stage decrease as the frequency increases, necessitating precise alignment between the stages and the two halves of the split blocks. The output power of the end stage of the THz source was reported for both room temperature and cryogenic cooling. The output power is approximately $10\mu W$ at 1.5 THz at room temperature, which increases to around $50\mu W$ at 120K.

Table 2.3: Performance comparison of different types of Monolithic-integrated THz multipliers

Type	Study	Efficiency %	Frequency [GHz]
Tripler (×3)	[88]	25-35	260-340
Tripler (×3)	[89]	2.6	840-900
Three Cascaded Triplers (×3 ×3 ×3)	[90]	1.7	2700
Tripler (×3)	[91]	7.3	135-150

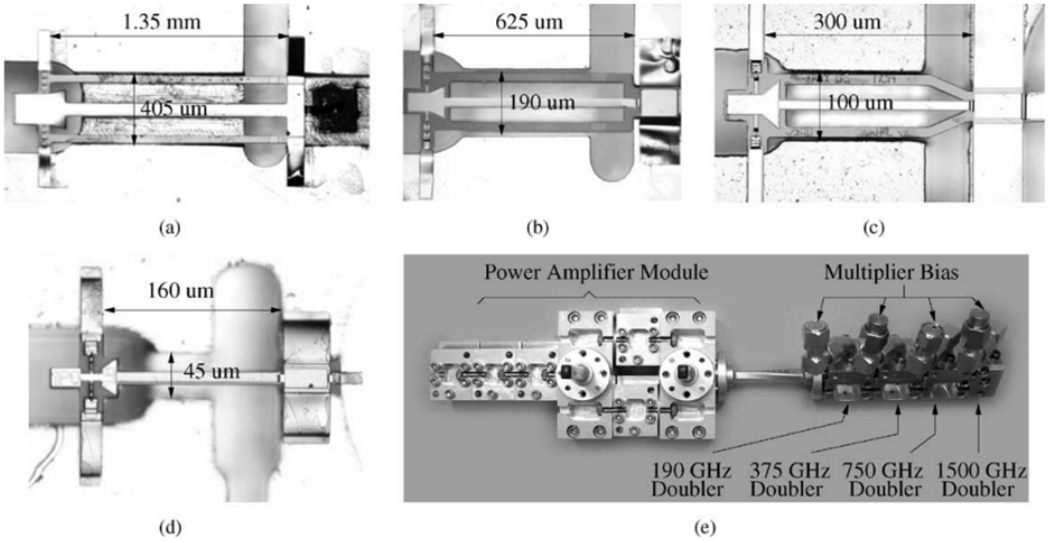


Figure 2.4: The fabricated 1.5 THz source by JPL (a) first stage doubler at 190 GHz (b) second doubler at 375 GHz (c) third stage doubler at 750 GHz (d) final doubler stage at 1.5 THz (e) the full module of the THz source [3].

Chapter 3

Multi-Band All-Silicon EM-Based Terahertz Integration Technology

This chapter introduces a multi-band integration technology that utilizes all-silicon components capable of efficient operation up to the THz range. The approach involves incorporating photonic crystal-like cylindrical holes within the silicon structure to achieve tunable effective materials. The fabrication process is then detailed, outlining the necessary steps to create waveguide sizes within a single wafer while minimizing mask usage for reduced process complexity. The modal behavior of guided channels is analyzed, and a straightforward design procedure for constructing waveguides at the desired frequencies is presented. To validate the effectiveness of the integration technology, a prototype waveguide at the V-band is designed and its measured results are provided. The subsequent sections of the chapter are organized as follows: Section II introduces the proposed effective medium-silicon suspended waveguide (EM-SSW) and explores the various operational

modes of photonic crystals at THz. In Section III, designs for PhC-based EM-SSW operating at the V-band and D-band are proposed, along with corresponding numerical results. Section IV outlines the concept of multi-band operation within the all-silicon PhC-based technology and explains the fabrication process. Finally, in Section V, conclusions drawn from the study are presented, and potential future extensions for operating beyond 1 THz are discussed.

3.1 Effective Medium-Suspended Silicon Waveguides

Combining the advantages of the two waveguide technologies with the best THz performance discussed in the literature: effective medium and suspended waveguides, we propose *photonic crystal-based effective medium-suspended silicon waveguides (EM-SSW)*. This design allows the planar representation of suspended waveguides while increasing the isolation of the guiding strip providing preparation steps for an efficient multi-band operation, which will be discussed in section III. The motive for using the EM operation for PhC structures is the increased bandwidth over the PBG operation. Additionally, the fabrication of a suitable PhC cell size is feasible at THz frequencies. On the other hand, the suspension of the waveguide channel provides a practical packaging solution for substrate-independent operation without the impact on field perturbation, i.e., the complete insulation of the guided mode allows the use of the EM-SSW on any packaging technology, e.g., all-silicon, SOG, substrate-less, etc.

3.1.1 EM-SSW Structure and Analysis

The structure of the EM-SSW, shown in Figure 3.1, consists of a guiding silicon strip of width "w" and height "h" suspended between two PhC grids functioning as effective media. The PhC lattice structure depends on the value of the desired effective dielectric constant required to achieve modal confinement in the waveguide channel. The height of the silicon wafer "h_s" depends on the fabrication technology and the limitations of the process in terms of the maximum aspect ratio achievable for the cylindrical holes; however, it needs to be sufficient for proper modal isolation. The substrate can utilize any hard material that is thermally compatible with silicon for easy bonding and has fair thermal conductivity for heat sinking; however, it is optional, and the EM-SSW can operate efficiently with all-silicon packaging. In our research, we were interested in the operation at three different frequency bands: V-band, D-band, and Y-band; these bands correspond to each frequency-tripler stage of the planned THz source.

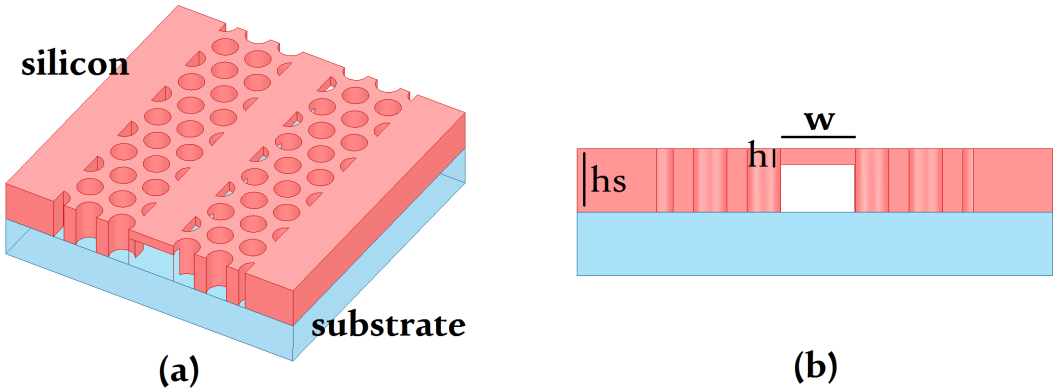


Figure 3.1: The structure and the cross-section of the effective medium suspended silicon waveguide (EM-SSW) on an optional substrate

Eigen-modal analysis using the COMSOL Multiphysics FEM electromagnetic solver is conducted to determine the single-mode bandwidth for the waveguides used in each stage. High-resistivity silicon is employed with a dielectric constant $\epsilon_r = 11.7$ and a loss tangent $tan\delta = 0.001$. The width w of the waveguides is $w_{V-band} = 1800\mu m$, $w_{D-band} = 1000\mu m$, and $w_{Y-band} = 200\mu m$, while the height h of the waveguides is $h_{V-band} = 500\mu m$, $h_{D-band} = 100\mu m$, and $h_{Y-band} = 100\mu m$. The height of the waveguides operating beyond 100 GHz is fixed at $100\mu m$ to simplify the fabrication process of the multi-band operation, which will be discussed in the next sections. The height of the silicon wafer h_s is set to $500\mu m$ for all waveguides without considering the thickness of the handle substrate since the goal of the all-silicon integration technology is to operate on a single wafer for all frequency bands. The effective medium is chosen to have a dielectric constant $\epsilon_r = 5$, a value that establishes a contrast between the guiding channel and the PhC.

Figure 3.2 exhibits the results of the modal analysis, i.e., the vector of the electric field distribution of the dominant mode is shown in the first column, and the second column presents the effective mode index β/k_0 of the first three propagating modes. The field graphs show the guided mode confinement in the silicon suspended strip for the three bands where the chosen effective dielectric constant of the cladding, $\epsilon_r = 5$, provides acceptable contrast with silicon.

It's worth noting that the V-band waveguide design is the ordinary EM-PhC-based waveguide without any elevation of the strip; this simplifies the upcoming fabrication steps by reducing mask count and overcomes a complex successive etching process. Furthermore, at the V-band, the effect of substrate interaction does not significantly degrade the performance. Single-mode bandwidth refers to a specific frequency range where only

one mode with the same polarization can be transmitted in a waveguide channel. The single-mode bandwidth, shown in Figure 3.2, is approximately 45%, 30%, and 40% for the V-band, D-band, and Y-band waveguides of operating frequencies 56 GHz, 168 GHz, and 498 GHz, respectively. The proposed D-band EM-SSW has a small strip aspect ratio which benefits the fabrication process despite the inconsiderable bandwidth reduction, especially in our case for building the THz source. The guided mode degradation is dominant by the dielectric loss caused by silicon's loss tangent; however, there are other sources of attenuation, such as radiation and substrate losses. The attenuation constant for the three waveguides is simulated to be $\alpha_{V-band} = 0.0052dB/mm$, $\alpha_{D-band} = 0.0043dB/mm$, and $\alpha_{Y-band} = 0.0062dB/mm$. Therefore, the simulated results prove the principle of operation of the EM-SSW and show the potential to proceed in the next steps of using the structure to build an all-silicon multi-band integration technology.

3.1.2 Photonic Crystal-Based Effective Medium Analysis

A Photonic Crystal (PhC) is a lattice of cylindrical holes that was primarily utilized in the optical wave region. The early principle of operation relies on creating a periodic arrangement of holes in silicon that generates a photonic band gap (PBG) and prohibits the propagation of modes within the silicon. Creating a line defect along the lattice provides guided wave operation within the silicon, known as PBG-based line-defect PhC waveguides.

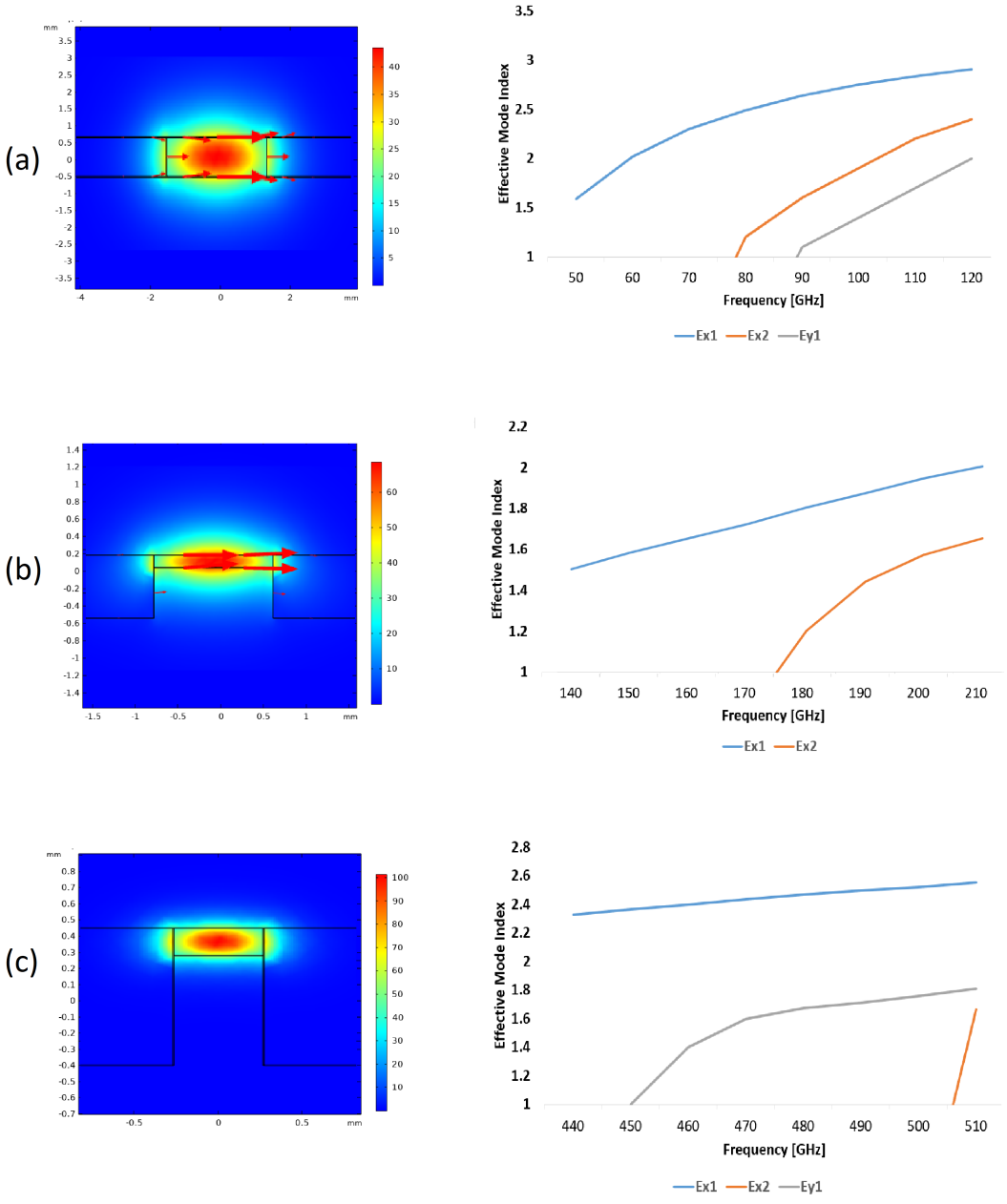


Figure 3.2: Electric field distribution and modal propagation for (a) V-band (b) D-band (c) Y band channels.

The PBG is produced when the size of the cylindrical holes is close to the wavelength λ of the propagating wave, leading to scattering and causing destructive interference for the propagating waves. However, when the size of the holes is considerably smaller than the operating wavelength, the periodic PhC behaves as an effective homogeneous medium with an effective dielectric constant range between air and silicon, depending on the structure of the lattice. An EM structure with larger holes will have an effective index more similar to that of air, while an EM structure with smaller holes will have an effective index more similar to that of silicon. Equivalent to PBG line-defect waveguides, creating a line defect of the high permittivity silicon in contrast with a low effective dielectric constant of the PhC lattice leads to guided propagation along the line but utilizes the mechanism of total internal reflection (TIR), called EM-PhC waveguides. The proposed lattice structure is the triangular periodic array shown in Figure 3.3. An approximation for the effective dielectric constant can be calculated by averaging; however, it depends on the polarization of the propagating mode. The Maxwell-Garnett approximation is given by equations 3.1 and 3.2 for perpendicular ($\perp$) and parallel ($\parallel$) modes of polarization. The dissimilarity in the relationships of the two modes being propagated is due to the boundary conditions at the vertical and horizontal interfaces.

$$\epsilon_{\perp} = \epsilon_{si}\frac{(\epsilon_0 + \epsilon_{si}) + (\epsilon_0 - \epsilon_{si})\zeta}{(\epsilon_0 + \epsilon_{si}) - (\epsilon_0 - \epsilon_{si})\zeta} \tag{3.1}$$

$$\epsilon_{\parallel} = \epsilon_{si} + (\epsilon_0 - \epsilon_{si})\zeta \tag{3.2}$$

Where $\epsilon_{\parallel}$ is the effective dielectric constant of horizontal modes, $\epsilon_{\perp}$ is the effective dielectric constant of vertical modes, ϵ_{si} is the permittivity of silicon, ϵ_0 is the permittivity of air,

and ζ is the filling factor of the lattice that depends on the structure of the PhC. Maxwell-Garnett averaging methodology can be applied to determine equations for the triangular PhC lattice. The periodicity of holes in horizontal Px and vertical Py directions of the triangular lattice are related by equation 3.3. In contrast, its filling factor is related to the volume of holes compared to the unit cell's volume by the equation 3.4.

$$P_x = P_y \ \sin\frac{\pi}{3} \tag{3.3}$$

$$\zeta = \frac{V_h}{V_c} = \frac{\pi R^2}{a^2 \ \sin\frac{\pi}{3}} \tag{3.4}$$

Where V_h is the volume of the cylindrical holes, V_c is the cell volume, R is the radius of each cylindrical cavity, and a is the lattice constant, i.e., the distance between the centers of two adjacent holes in the lattice.

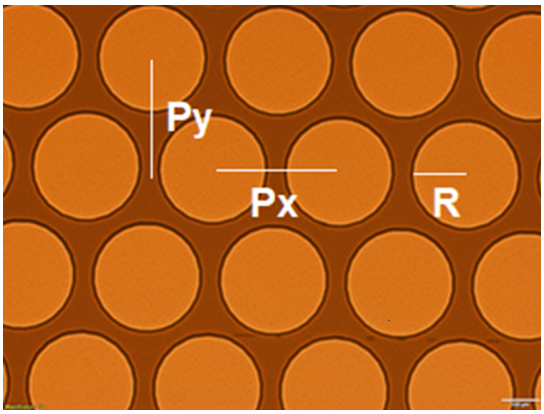


Figure 3.3: Triangular PhC structure under an optical microscope.

Next, it is necessary to determine the maximum effective dielectric constant of the EM-PhC cladding to provide proper modal confinement in the guiding channel. A core-clad

permittivity contrast analysis is performed by calculating the propagation of the substrate leakage modes and increasing the cladding's effective dielectric constant at the V-band. Figure 3.4 shows the variation of electric field confinement of the fundamental mode $E_{x_{11}}$ with changing the effective dielectric constant of the cladding. It is noticed that the field confinement is reasonable up to $\epsilon_{r_{clad}} \approx 5 - 7$. However, investigating the propagation of cladding modes provides a more accurate representation of the maximum acceptable required effective permittivity. The results of the modal analysis shown in Figure 3.5 indicate that the cladding modes start to propagate at $\epsilon_{r_{clad}} \approx 5$. Therefore, to achieve perfect core modal confinement, the effective permittivity of the cladding should be less than that value; however, it could be reasonable to operate at a higher effective permittivity if the substrate leakage lies within an acceptable range, i.e., with lower coupling of substrate modes.

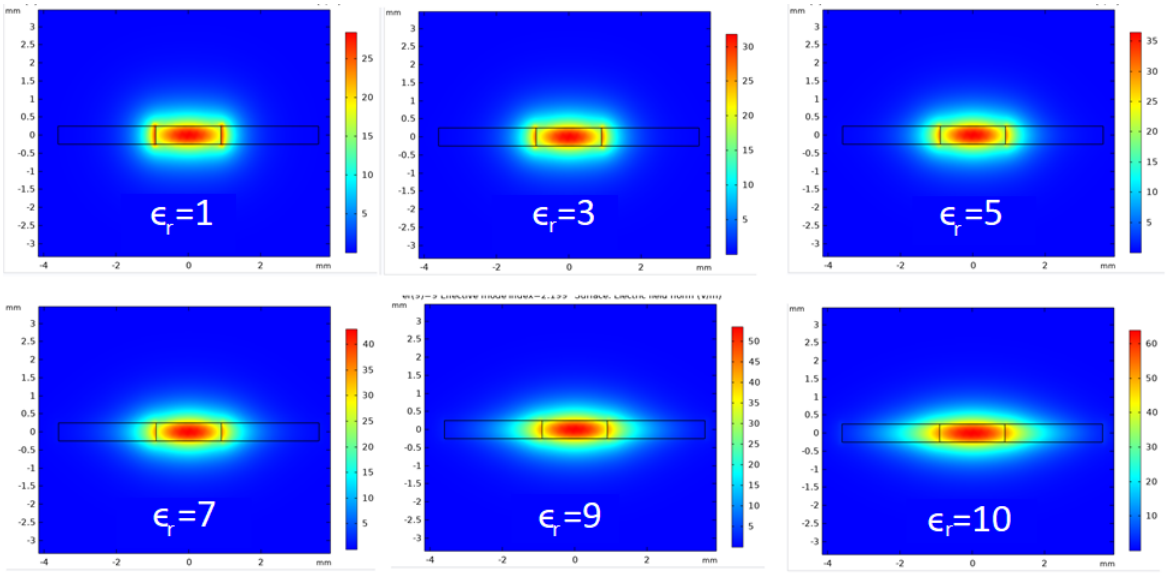


Figure 3.4: EM-SSW modal confinement with different clad effective permittivity values.

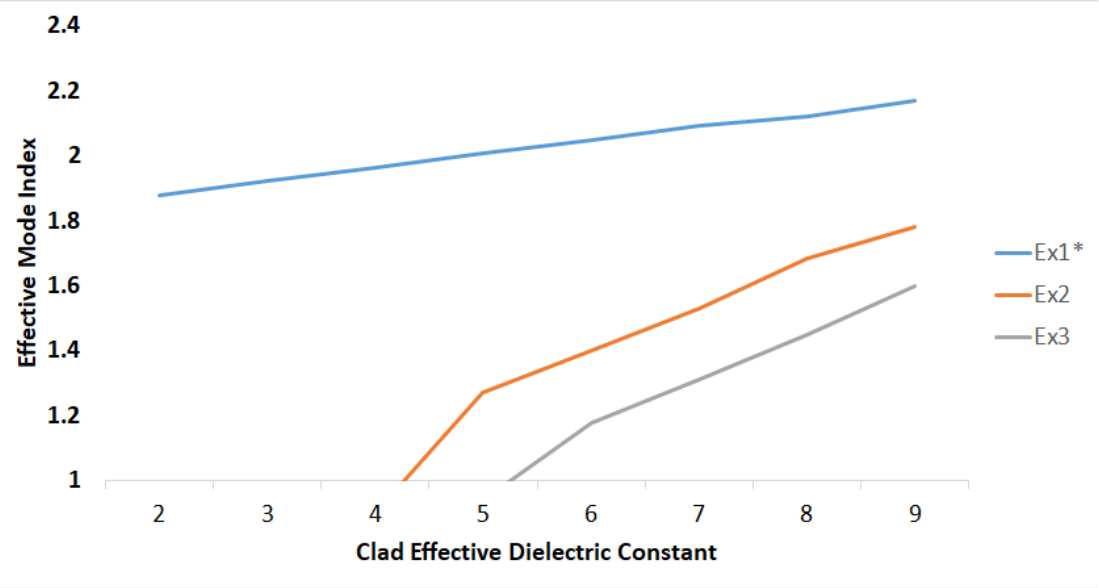


Figure 3.5: The propagation of clad modes vs. clad effective dielectric constant.

3.2 Simulation and Measurements of V-band, D-band and Y-band EM-SSW

After defining the EM-SSW and considering the results of the performed 2D modal analysis, 3D finite element analysis (FEA) becomes essential to determine the scattering matrix (S-parameters) and simulate the back-to-back measurement setup for determining proper waveguide excitation across the operational band. Furthermore, analyzing the electric field distribution in the axial direction provides a more accurate representation of the modal confinement within the core. This analysis aids in determining the operational margin beyond the cladding's effective dielectric constant, as calculated from the 2D modal analysis. The interest in operating at a higher effective dielectric constant for the cladding is to work with lower filling factors. A lower filling factor reduces the structure's fragility;

having mechanically stable cladding is crucial to prevent wafer damage during fabrication, packaging, and component assembly.

3.2.1 3D FEM Simulations of the EM-SSW

Ansys High-Frequency Simulation Software (HFSS) is used for the FEM modal-driven analysis. Figure 3.6 illustrates the EM-SSW with two ports for modal excitation. The PhC-like structure is constructed based on the formulation in the previous section to implement different effective materials. Continuing the contrast analysis to find the maximum acceptable filling factor, a 3D simulation was conducted by varying values of the effective dielectric constant, similar to the 2D modal contrast analysis we previously carried out. The cladding consists of three rows of unit cells, which have been proven to be sufficient for the EM behavior.

The wave propagation field, as shown in Figure 3.7, is simulated at different values of cladding effective permittivity at $168GHz$. Guided mode leakage in the cladding begins at $\epsilon_r \approx 5.5$; however, it becomes significant at $\epsilon_r \approx 6$, and the waveguide loses operation at $\epsilon_r \approx 7$. Moreover, Figure 3.8 illustrates the insertion loss versus cladding's effective permittivity values for the D-band EM-SSW waveguide. The response is equivalent for all structures with effective permittivity ϵ_r less than 5.5. Accordingly, the maximum filling ζ_{max} can be estimated from the effective permittivity. The waveguides can function with a filling factor value lower than ζ_{max}, depending on the fabrication process and the necessary mechanical strength. It is worth noting that the operation at $\epsilon_r = 1$ corresponds to the operation of a ribbon waveguide since the effective material is equivalent to air. There-

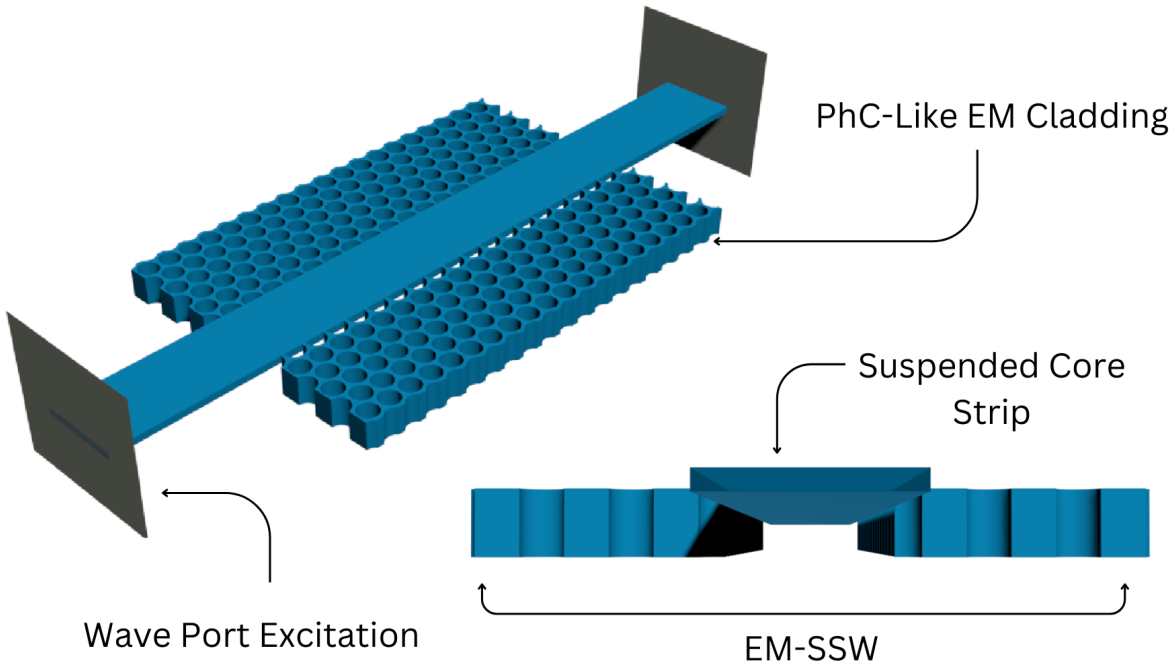


Figure 3.6: FEM simulation for EM-SSW showing wave ports excitation sections and PhC-like cladding.

fore, the operation below ζ_{max} is nearly identical in operation to the ideal operation with attenuation constants $\alpha_{\zeta_{max}} = 0.00435$ and $\alpha_{ribbon} = 0.0042$ at $168GHz$. In summary, the simulation results prove the operation of the EM-SSW and provide the basic guidelines for proper procedures. The next step is fabricating the EM-SSW and comparing the measured results to the simulated ones.

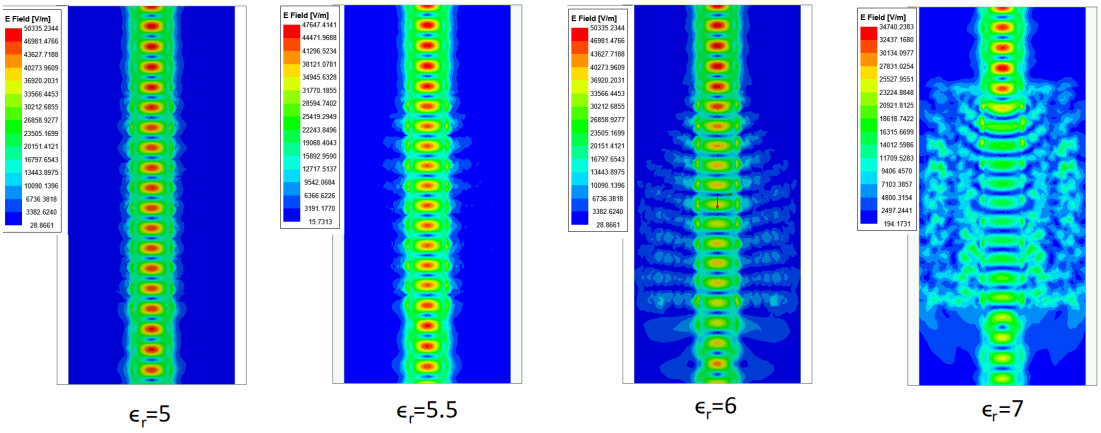


Figure 3.7: Electric field confinement with contrast analysis for D-Band EM-SSW.

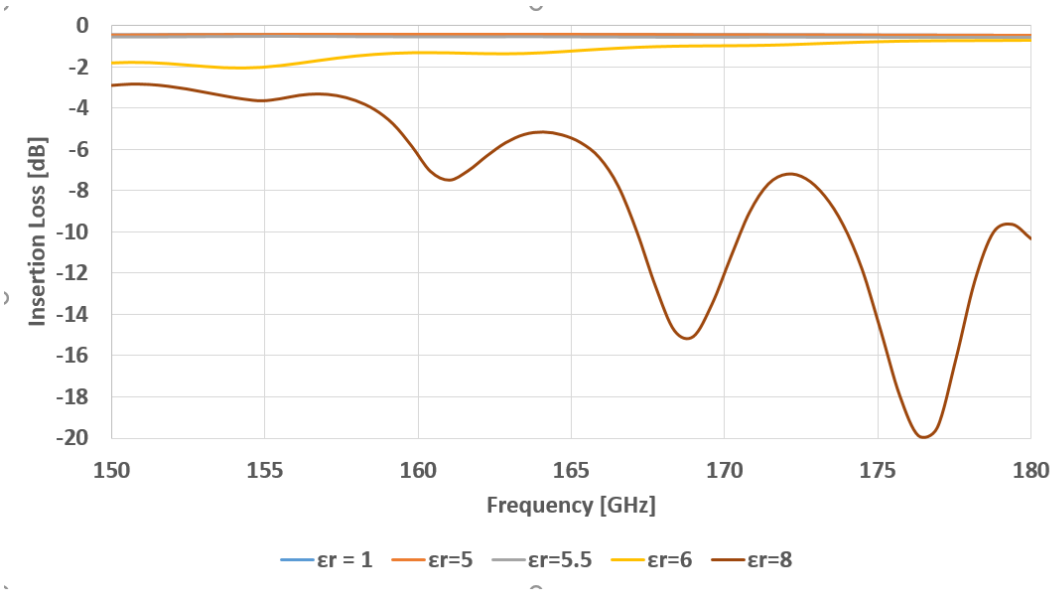


Figure 3.8: Simulated insertion loss with contrast analysis for D-Band EM-SSW.

3.2.2 Fabrication and Measurement of V-Band and D-Band EM-SSW

The final step in the design verification process of the EM-SSW involves physically testing fabricated waveguides to determine how well they align with the simulated results. The experimental setup used for testing the V-band and D-band EM-SSW is shown in Figure 3.9. Frequency mixers by OML Inc. are employed to extend the operating range of Keysight Technologies PNA-X into the V-band and D-band. The connectors of the frequency extenders are metallic waveguides, namely WR-15 for the V-band and WR-05 for the D-band. Silicon contactless probes, which will be discussed briefly in the next chapter, are utilized to excite the EM-SSW waveguides through taper transitions inserted in the metallic connectors. To ensure the precise alignment of the excitation probes with the waveguides, the two extenders are attached to movable stages that enable movement in all three principal coordinates.

Figure 3.10(a) displays the results of the V-band EM-SSW structure with a length of $L = 10mm$, effective cladding permittivity of $\epsilon_{r_{effective}} = 5.5$, and a hole radius of $r = 150\mu m$. 3.10(b) presents the Scanning Electron Microscope (SEM) image of the fabricated V-band EM-SSW. The waveguide is fabricated in the QNFCF at the University of Waterloo using a two-mask photo-lithography process and DRIE. The results compare the measured return and insertion losses to the simulated results. The measurement calibration is established at the metallic connectors to ensure it corresponds to the reference plane used in the simulations. The transmission response is flat across the V-band with $S_{21} < 1dB$ and the reflection $S_{11} < -15dB$. The attenuation constant is calculated af-

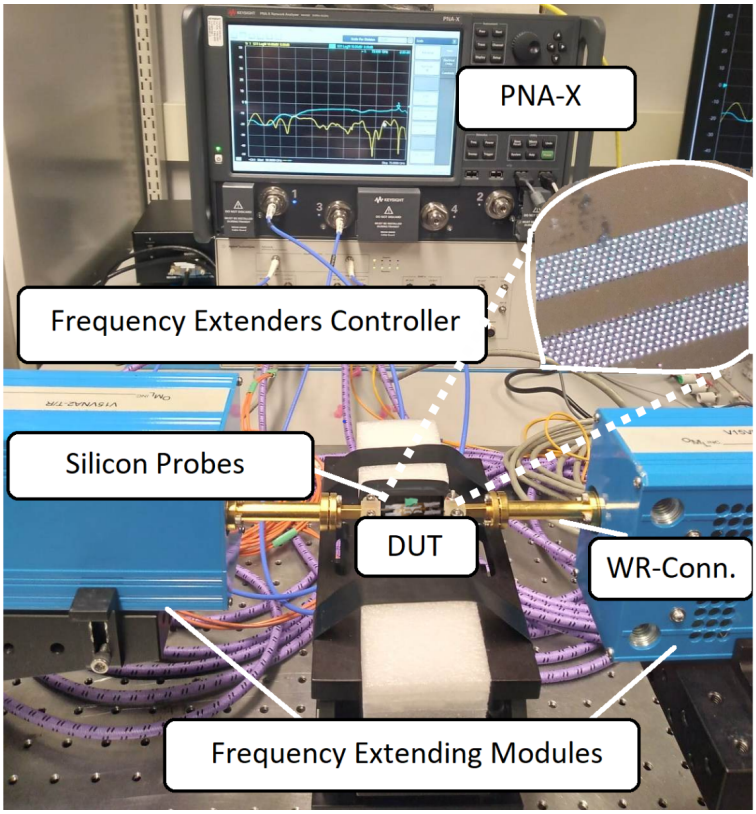
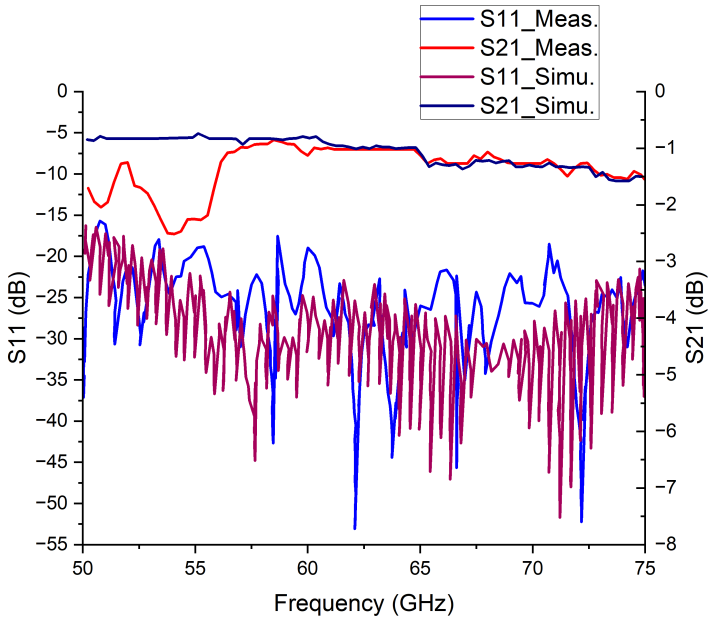


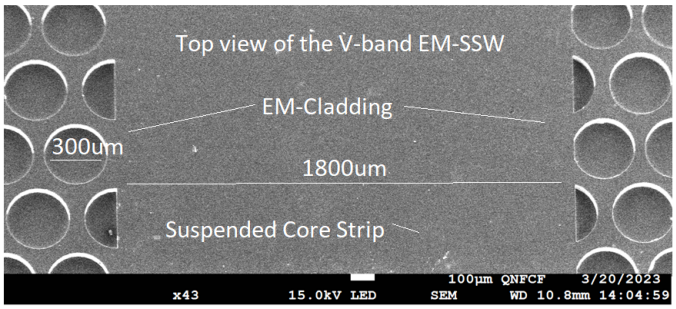
Figure 3.9: Experimental setup for EM-SSW measurements.

ter de-embedding the effect of the two dielectric probes to be $\alpha_{measured} = 0.0058dB/mm$, which is approximately equivalent to the simulated attenuation constant

On the other hand, the D-band EM-SSW, with a length of $L = 10mm$ and the same filling factor but a hole radius of $r = 120\mu m$, is similarly measured using the same setup. D-band frequency extenders with WR05 connectors are used along with novel contactless frequency probes for the measurements. Figure 3.11 presents an SEM picture of the fabricated D-band EM-SSW in (a) along with combined results of the simulated and measured S-parameters in (b). Similar to the results of the V-band waveguide, the transmission



(a)



(b)

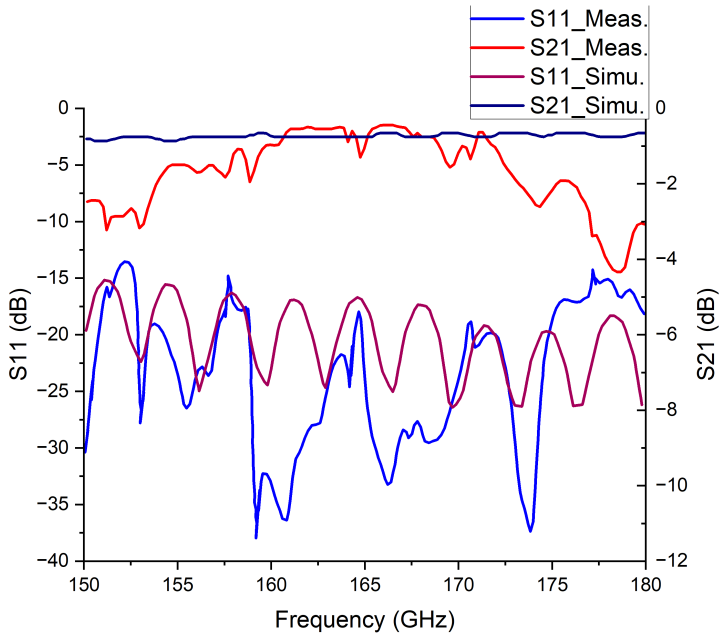
Figure 3.10: (a) Simulated and Measured S-parameters for V-band EM-SSW. (b) SEM picture for the fabricated V-band EM-SSW

curve is flat with $S_{21} > -1dB$, and the reflection is acceptably low with $S_{11} < -18dB$. The measured attenuation constant matches the simulated value at the D-band, with $\alpha_{measured} = 0.0051$. Therefore, the measurements confirm the excellent performance of

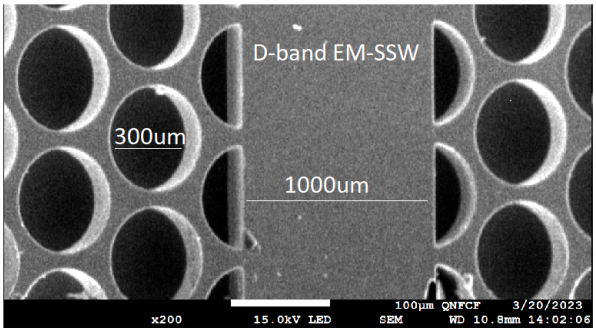
the EM-SSW at both the V-band and D-band. Moreover, the simulation of the Y-band EM-SSW in Figure 3.12 shows an insertion loss of less than $1dB$ and a return loss of less than $-20dB$.

3.3 Multi-Band THz Integration Based on EM-SSW

Multi-band operation is essential for frequency up-conversion harmonic-based THz sources. The dimensions of the system significantly decrease as the frequency doubles or triples. As mentioned earlier, the performance of planar PCB technology is limited to frequencies below 100 GHz. However, finding a substitute technology with equivalent characteristics at higher THz frequencies is more complex. Such features may include the planar integration of components, low-loss interconnects, and multi-band single-mode operation. At this point in our research, we proposed the low-loss, multi-band EM-SSW. Nevertheless, exploring methods for operating these multi-band waveguides on a single wafer is still required while achieving planar integration. Figure 3.13 presents the evolution of our proposed multi-band integration method; in (a), the differences in waveguide dimensions across three Tripler stages are shown. This configuration is necessary to produce THz power through a 50 GHz input signal. The suspension property of EM-SSW made it convenient to align all waveguides on a single planar level, as shown in Figure 3.13(b) and (c). However, the fabrication of such planar alignment requires multi-step etching on the same side of the wafer, i.e., three DRIE steps for the configuration in the figure. Multi-step etching presents a challenge as it involves a sequence of photo-lithography procedures, which can be impractical due to difficulties in achieving uniform photoresist (PR) material distribution



(a)



(b)

Figure 3.11: (a) Simulated and Measured S-parameters for D-band EM-SSW. (b) SEM picture for the top view of the fabricated D-band EM-SSW with 10 degrees tilt to show the depth of the sidewalls.

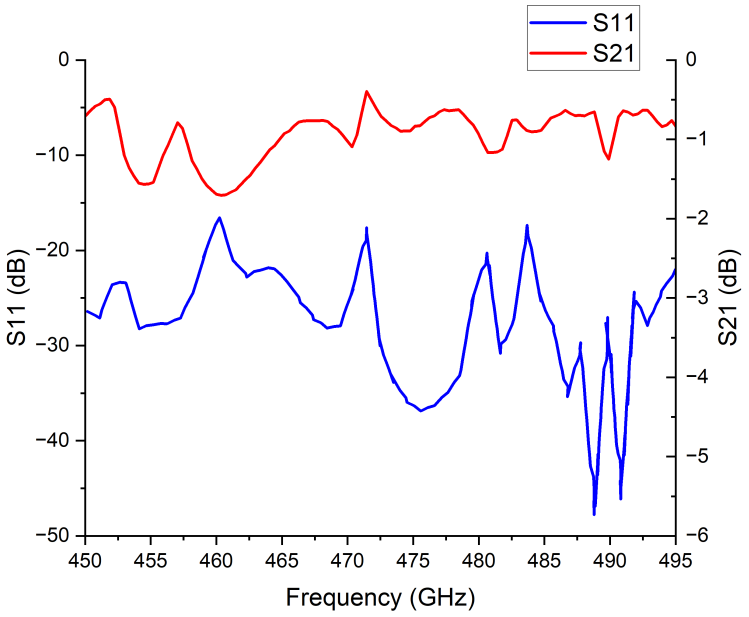


Figure 3.12: Simulated S-parameters for the back-to-back Y-band EM-SSW, including WR-2.2 connectors and Y-band probes excitation.

in the presence of patterned features.

To solve this issue, we address the problem by dividing the necessary etching levels between both sides of the wafer and utilizing double-sided lithography. Figure 3.13(b) illustrates the packaging using low-contrast substrate materials as a step towards all-silicon integration. The substrate under the EM-SSW is etched to isolate it from the operating V-band waveguides. On the other hand, in Figure 3.13(c), the packaging using high-contrast substrate materials is shown, such as Pyrex. Our research used the all-silicon EM-SSW packaging to design the THz triplers and sources.

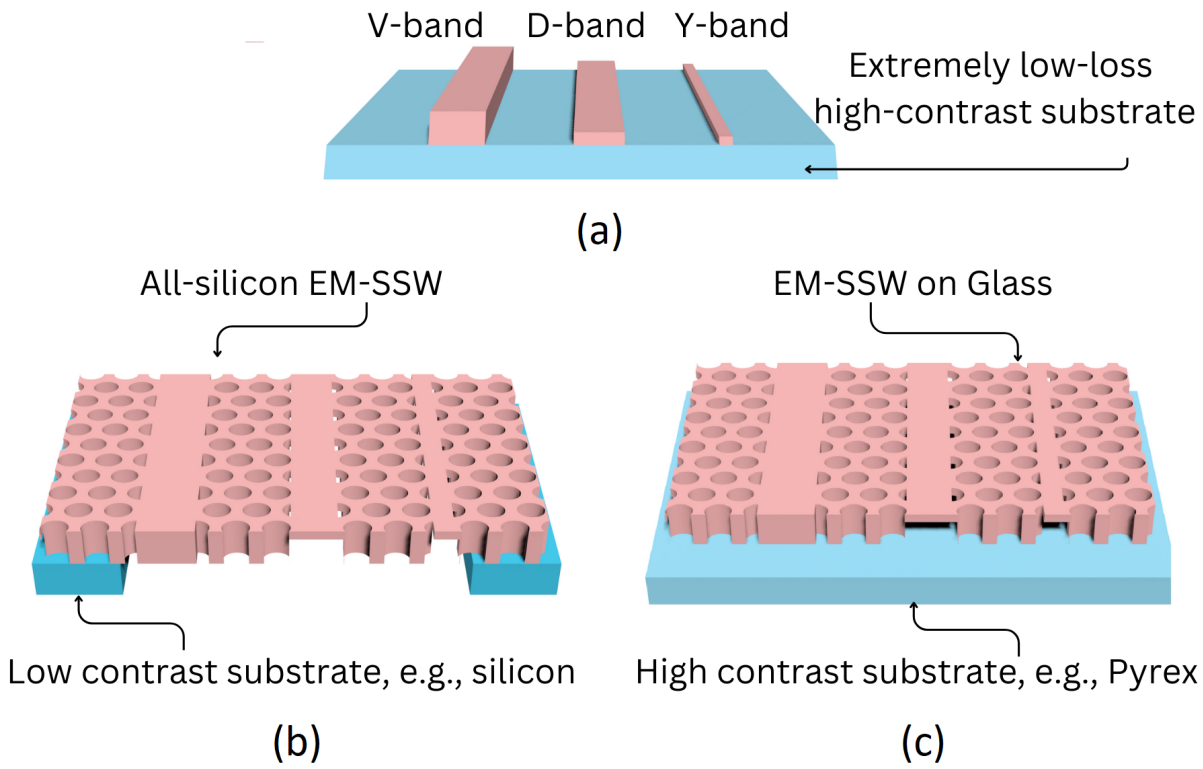


Figure 3.13: 3D models for (a) multi-band operation with non-planar waveguides integration (b) the proposed multi-band EM-SSW with all-silicon double-sided lithography. (c) the proposed multi-band EM-SSW bonded with glass and double-sided lithography.

3.3.1 Multi-Frequency Platform Fabrication Process

The fabrication of the previously discussed method of multi-band THz integration using the EM-SSW consists of three accurately tuned steps: Aluminum lift-off process, front photo-lithography, and back photo-lithography. The fabrication process was conducted in the QNFCF facility at the University of Waterloo. The steps are shown in Figure 3.14 and will be discussed in the following subsections.

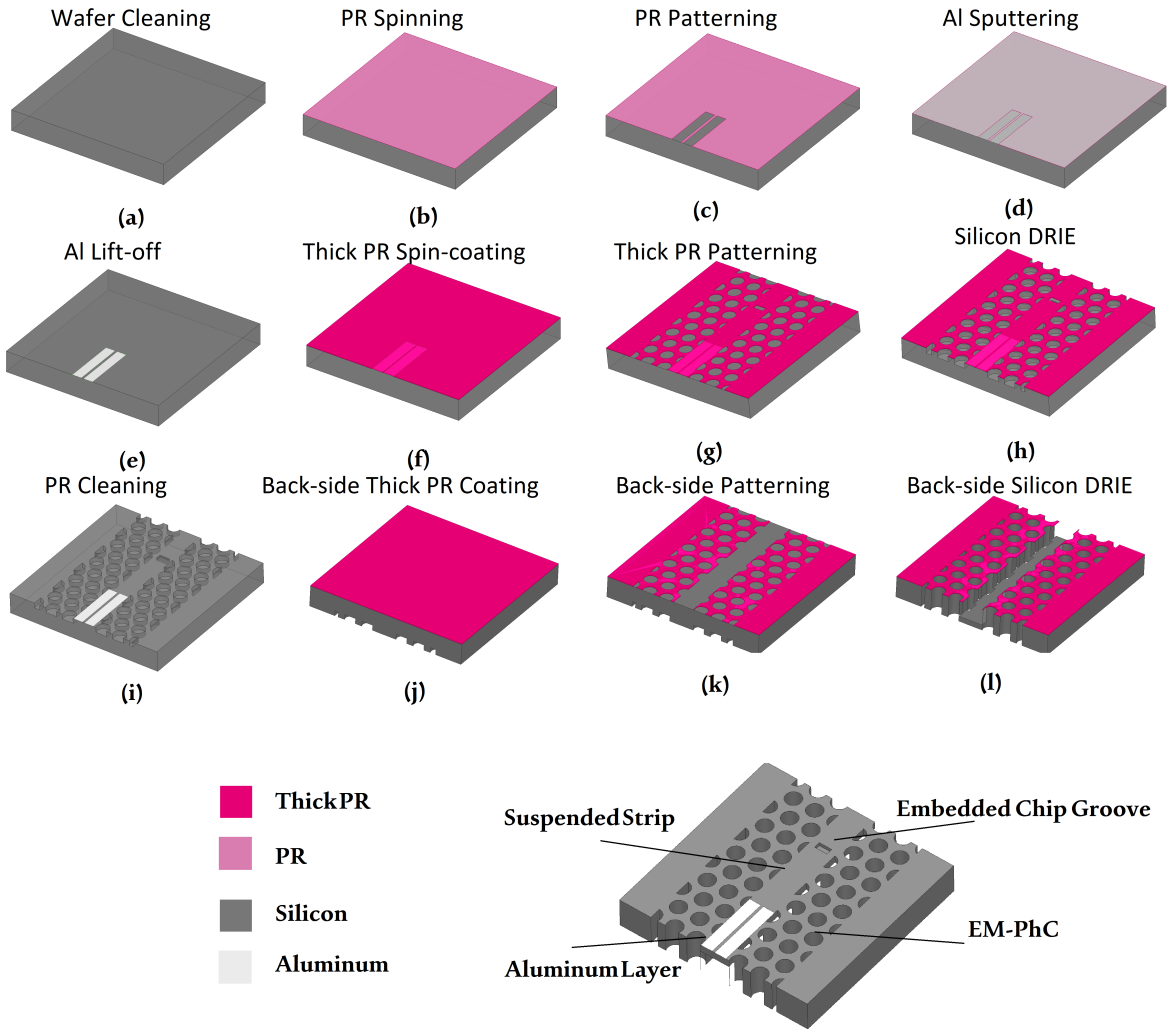


Figure 3.14: Fabrication process steps for the multi-band THz platform.

In micro and nanofabrication, the lift-off process is a widely used technique to deposit a pattern of a thin metal layer on silicon substrates. This process circumvents the use of hazardous acids for direct wet etching of metals. Our proposed integration technology employs the Aluminum layer to create metallic contact pads, facilitating the integration of

active devices through transitions and packaging techniques, such as Flip-chips and Wire bonding. The recommended pad thickness for wire bonding, the packaging technology discussed later in Chapter 4, is approximately $750nm$. Therefore, the steps in Figure 3.14 from (a) to (e) will discuss how to create a $1\mu m$ pattern of Aluminum layer on a $500\mu m$ HR-Si wafer. After completing the Aluminum patterning on the wafer, the next step involves etching $100\mu m$ of silicon, serving two purposes: creating the embedded grooves for the active chip integration and partially etching the thru cylindrical holes to avoid a lengthy DRIE run. The steps of the second mask are shown in Figure 3.14 from (f) to (i). The back-side process is essentially a long-run DRIE to create the thru cylindrical holes and remove $400\mu m$ of silicon to form the suspended waveguide strip. Since the silicon wafer is etched through, the wafer is bonded to a carrier wafer to ensure the uniformity of gas distribution and prevent damage to the device wafer. The steps of the last mask are presented in Figure 3.14 from (j) to (l).

a) The wafer is prepared and cleaned in Piranha solution, i.e., a mixture of sulphuric acid and hydrogen peroxide, to get rid of any particles and guarantee the purity of the wafer. A thin layer of Hexamethyldisilazane solution (HMDS) is deposited on the wafer to improve the adhesion of the PR.

b) A $4\mu m$ of ma-N 1400 series negative PR is spin-coated on the wafer.

c) The PR is patterned using Mask-less Aligner Heidelberg UV photo-lithography. A dose test was performed before the actual exposure to determine the suitable Defoc and Dose for the PR, i.e., $D = 350mJ/cm^2$ and $Defoc = -2$. After exposure, the PR is put in the developer to harden the unexposed patterns.

d) A $1\mu m$ layer of Aluminum is PVD sputtered on the patterned wafer using AJA Twin-coater sputtering.

e) The wafer is immersed in Remover PG, a solution used to remove the PR, 24 hours after Aluminum deposition. Then, it is subjected to ultrasonic agitation in a heated solution at a temperature of $80°C$ for 30 minutes. Finally, the wafer is cleaned with de-ionized water to remove any solution residues.

f) A $10\mu m$ of thick positive AZ4620 PR is spin-coated after depositing a layer of HMDS on the wafer.

g) The features of the holes and embedded grooves are patterned using UV photo-lithography after conducting a dose test to precisely adjust the dose and defocus, followed by developing for 5 minutes.

h) The first DRIE step to create vertical anisotropic grooves in silicon using the Bosch process. The selectivity to the PR was calculated to be $95:1$, and the etch rate was $2\frac{\mu m}{min}$.

i) The wafer is immersed in Remover PG and heated to $80°C$ for 30 minutes to remove the PR.

j) A $10\mu m$ of thick positive AZ4620 PR is spin-coated on the back-side of the wafer after depositing a layer of adhesive HMDS.

k) The features of the holes are patterned using UV photo-lithography after using the same dose parameters as the front-side lithography process. However, the alignment

marks are flipped horizontally to match the backward alignment camera. Then, the PR is developed for 5 minutes.

l) The final DRIE step is to create high aspect ratio side walls in silicon using the Bosch process.

m) The wafer is immersed in Remover PG and heated to $80°C$ for 30 minutes to remove the PR. Followed by washing in deionized water.

Finally, the device is ready for characterization, dicing, and packaging. It's worth noting that the fabrication process might require an additional mask if the device is operating beyond 1 THz. In this case, the back etching step will involve two successive lithography processes using two PR masks to achieve two etching levels. However, this is a complex process and requires precise tuning to achieve the necessary etching levels.

3.3.2 PhC Design Rules and Fabrication Consideration

The study of EM-PhC presented in the previous sections led to a design approach to determine the optimal filling factor required for successful EM-SSW functionality. However, when dealing with THz frequencies, the PhC unit cell size becomes significantly smaller to ensure operation outside the electromagnetic bandgap region. This condition is crucial for the PhC to function as an effective medium. From a nanofabrication standpoint, we aim to identify the smallest radius for the cylindrical holes that can be fabricated while maintaining a constant filling factor. Additionally, the DRIE rate should remain consistent for all PhC holes regardless of their radius. Figure 3.15 displays various PhC patterns

under an optical microscope. The characteristics remain distinguishable down to a radius of $25\mu m$. Figure 3.16 depicts a fabricated EM-PhC hole under depth investigation to confirm DRIE accuracy. For a targeted $100\mu m$ etching depth, the manufactured holes, including those with a radius as small as $25\mu m$, exhibited a consistent etching response. This outcome confirms the effective operation of the EM-SSW up to 1 THz; at 1 THz, the wavelength is $300\mu m$.

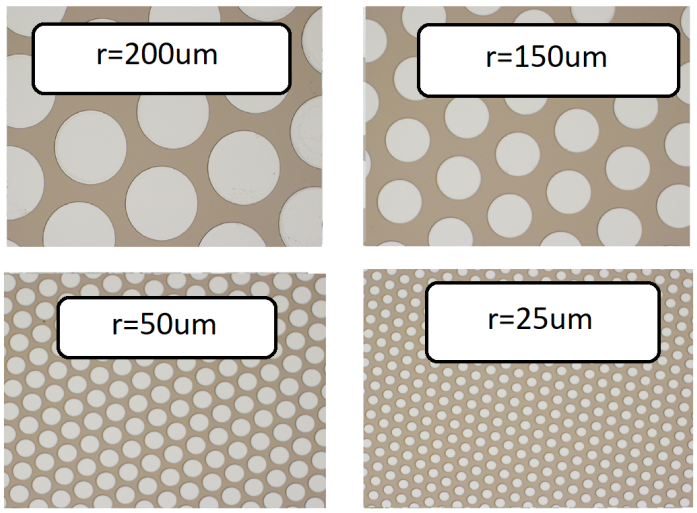


Figure 3.15: Different sizes of PhC with constant filling factor.

3.4 Summary

In this chapter, we proposed Effective Medium-Suspended Silicon Waveguides (EM-SSW) based on photonic crystal-like (PhC) structures. This waveguide technology offered excellent performance with a low attenuation constant and provided a feasible multi-band

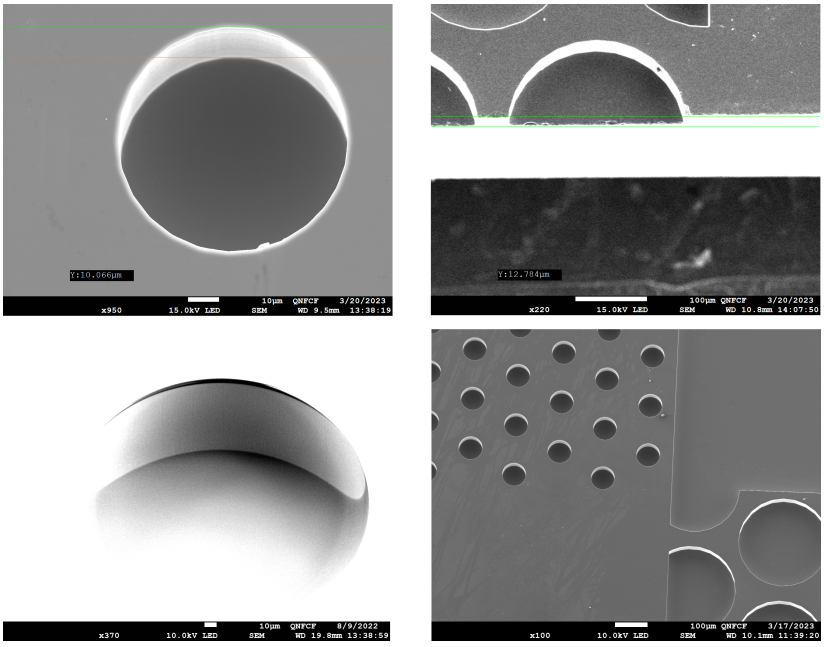


Figure 3.16: SEM pictures for fabricated $100\mu m$ deep holes.

integration solution for THz systems up to the THz range. We conducted a simulation-based modal analysis to study the conditions and limitations of proper single-mode guided operation. Additionally, we analyzed the required permittivity contrast between the core and PhC cladding to investigate the structure's functionality with different PhC filling factors. Subsequently, a 3D full-wave finite element analysis (FEA) was conducted to optimize the system and study modal transmission through structures of various filling factors. After fully understanding the operation of the EM-SSW and its advantages and limitations, V-band and D-band waveguides were fabricated using a design procedure based on the preceding studies. A 2-port network analysis was performed to measure the scattering parameters (S-Parameters) and attenuation constant of the fabricated structures, and the measurements accurately matched the simulated results. Thus, the proposed technology

paves the way for multi-band single-wafer THz integration. We discussed the proposed multi-band integration fabrication process in detail, including the three-mask steps for fabricating the THz platform and its potential for extension beyond 1 THz. Chapter 4 focuses on the silicon probe technology used in all THz measurements and proposes a novel contactless excitation technique for various widely used commercial technologies.

Chapter 4

Contactless Silicon DWG Probes for THz Measurements Advancements

In this chapter, we propose dielectric waveguide-based silicon probes for the contactless excitation of various types of transmission lines and waveguide technologies. This includes planar PCB technologies such as Microstrip lines (MS), Co-planar Waveguides (CPW), and Co-planar Striplines (CPS). Furthermore, we present excitation methods for metallic waveguides and dielectric waveguides using the principle of mode coupling. The waveguides are precisely fabricated using micro-machining HR-Si wafers. Additionally, their design includes a 3D-printed plastic fixture that wraps around the probes to ensure stability and proper positioning during measurements. The fixtures can contribute to the total probe loss, which is not a significant concern for measurements up to the W-band. However, they can negatively impact performance beyond 100 GHz. To mitigate this issue, a new type of probe was designed using all-silicon material, which eliminates the impact of the

plastic fixtures and can maintain good performance even at high THz frequencies. Figure 4.1 presents a 3D diagram of the different versions of silicon probes.

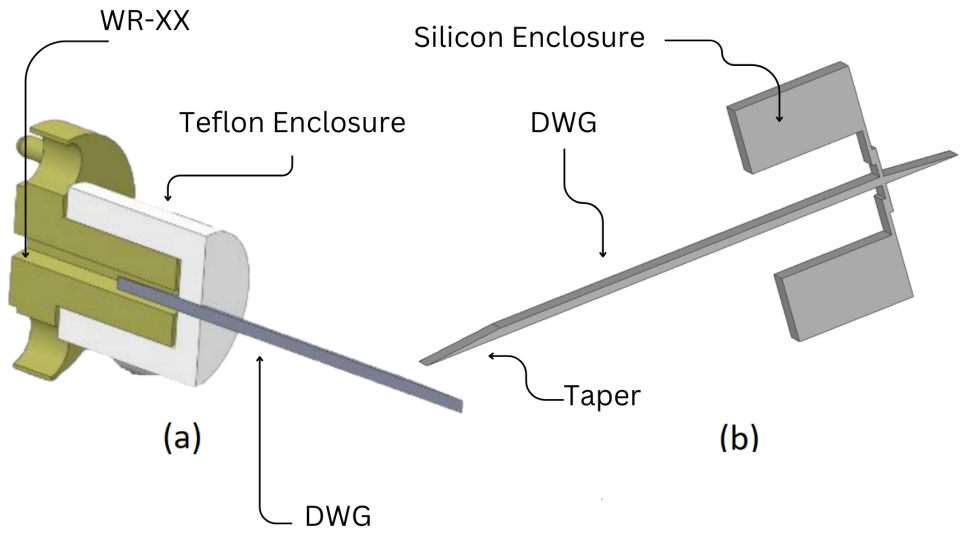


Figure 4.1: (a) The basic silicon probe with the Teflon fixture (b) The THz all-silicon novel version of the probe

4.1 Contactless Silicon Probes

In this section, we present the structure of the *Contactless Silicon Probes* used for all the measurements conducted in Chapter 3 and that will be used for the upcoming measurements in the following chapters. We analyze their operation and discuss different transitions that enable the excitation of multiple planar PCB technologies.

4.1.1 Dielectric Waveguides (DWG) Excitation

The dielectric probe is depicted in Figure 4.2 and consists of three primary components: a metallic waveguide connector, a high-resistivity Si dielectric waveguide, and a 3D-printed packaging enclosure. The required frequency band determines the metallic waveguide standard and the dimensions of the dielectric waveguide, including the cross-section dimensions and taper section length. This modified version of a tapered dielectric waveguide can couple the propagating power along it to a device under test on a wafer via near-field proximity. To create the metallic waveguides of the two probes, a 2-inch straight section of the WR10 waveguide is cut into two pieces using CNC machining. The Si dielectric waveguide is fabricated using Laser Milling on a 4-inch HR-Si wafer with a thickness of $500\mu m$. The 3D-printed enclosure is designed to consist of two parts that fit the Si dielectric waveguide and center it inside the metallic WR10 waveguide.

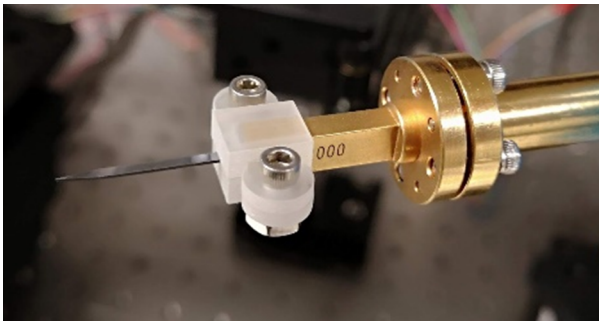


Figure 4.2: The fabricated contactless silicon probe at the V-band [4].

The W-band probe in Figure 4.2 has dimensions of $1200\mu m$ x $500\mu m$ that support the fundamental mode shown in Figure 4.3. The FEM modal analysis demonstrates the transmission of $E_{x_{11}}$ during single-mode operation. The attenuation constant of the waveguide

is $\alpha = 0.0046$, and the single-mode bandwidth covers the W-band.

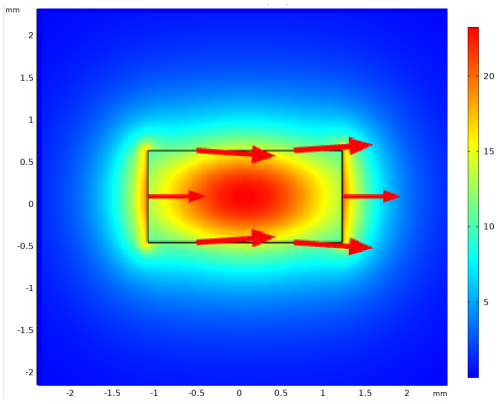


Figure 4.3: The electric field distribution of the $E_{x_{11}}$ mode of the silicon probe.

Furthermore, a 3D FEM modal-driven simulation is performed to optimize the taper sections and verify the probes' coupling in the DWG waveguides' excitation process. DWG excitation is similar in functionality to our proposed EM-SSW since the mode in the suspended strip is also $E_{x_{11}}$. The electric field in Figure 4.4 displays the near-field coupling between the back-to-back probes exciting DWG at a distance of $20\mu m$. The measurement setup includes W-band frequency extenders connected to the PNA-X, two W-band contactless silicon probes exciting a 30mm DWG. The results in Figure 4.5 depict the insertion and reflection loss of the measured probe-DUT-probe setup compared to the simulations. The transmission shows a flat response with an acceptable match to the simulated results. The average measured transmission $S_{21_{meas}}$ is more than -1.8 dB, while the average simulated $S_{21_{sim}}$ is approximately -0.7 dB. The return loss S_{21} is below -15 dB for both measured and simulated data. In summary, the contactless probes demonstrated their high performance in transmitting the fundamental mode of dielectric waveguides; therefore, they are suitable

for use in exciting DWG-based technologies, including the proposed EM-SSW technology.

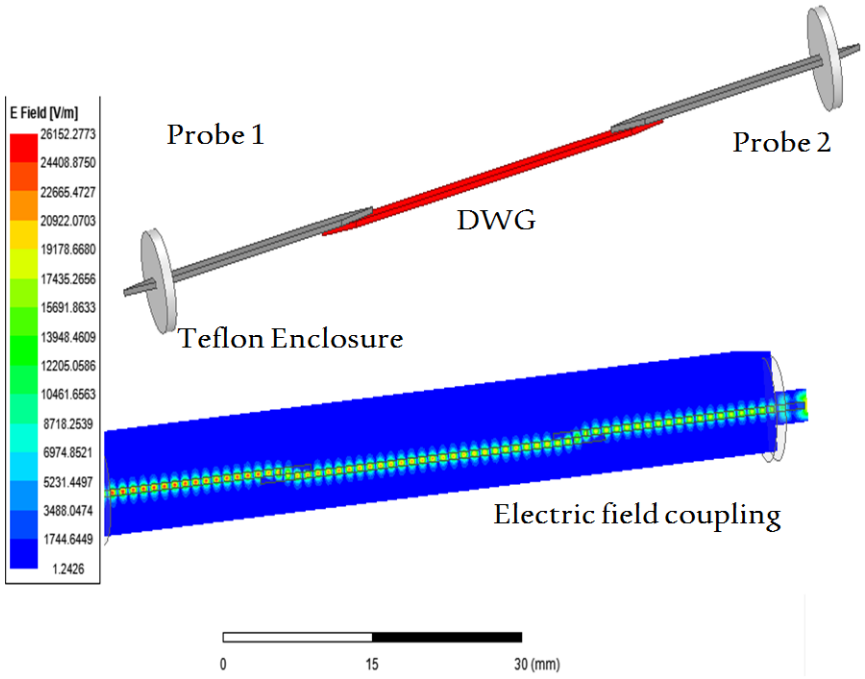


Figure 4.4: The electric field distribution of the $E_{x_{11}}$ mode of the silicon probe.

4.1.2 Co-planar Waveguides Excitation

The Coplanar Waveguide (CPW) is a commonly used transmission line at RF and mmW frequencies for terminating monolithic microwave integrated circuits (MMICs) and interconnects within and between chips on the board. The structure of the CPW consists of a signal strip of width w_s separated by a gap of distance s from two planar grounds, all mounted on top of a substrate of height h and permittivity ϵ_r. To achieve better near-field coupling between the CPW mode on top of the substrate and the dielectric probe mode

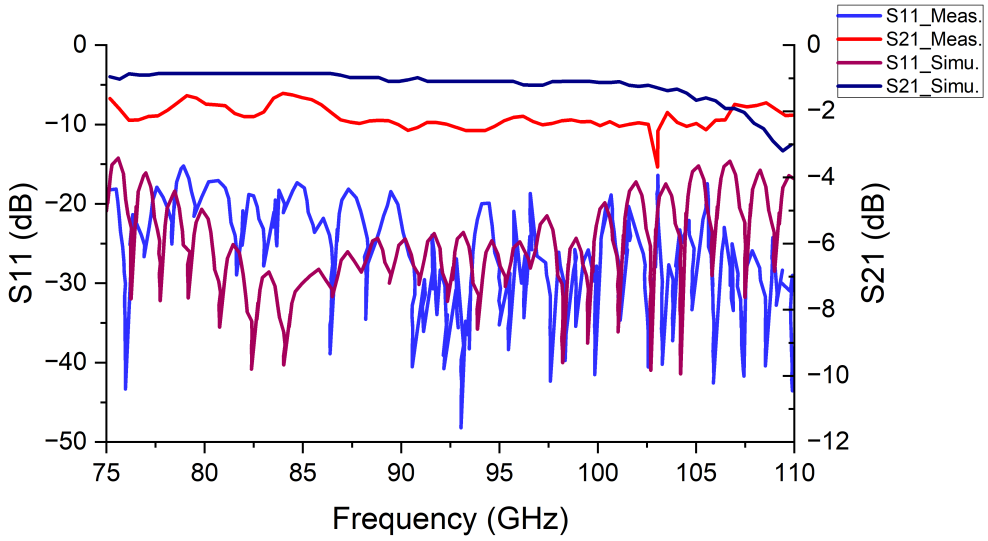


Figure 4.5: The S-parameters for the back-to-back probe to DWG excitation.

without physical contact between the probe and the board in the V-band, gradual tapering in the CPW grounds is used as the excitation methodology. The contactless silicon probe illustrated previously is utilized as the excitation probe for the CPW. The V-band probe has a WR15 metallic waveguide connector on the VNA side, and on the other side, it excites the CPW. The CPW termination used is a standard 50Ω with a $w_s = 50\mu m$ signal line and $s = 50\mu m$ ground gaps on a $10mil$ RO3003 substrate with $\frac{1}{4}Oz$ copper cladding. The silicon probe has dimensions of $1400\mu m$ x $500\mu m$ to support the fundamental $E_{x_{11}}$ mode and excite the odd-quasi TEM CPW mode [4].

A FEM simulation is conducted for the DWG probes to CPW transition presented in Figure 4.6(a) to analyze the transmission and return loss performance. The transition consists of gradually tapered cuts in the line's on-substrate grounds to match the modes of the probes and transmission lines. As shown in Figure 4.6(b), the probes are not in

contact with the CPW board, with a $20\mu m$ spacing. The field distribution, depicted in Figure 4.6(c), correlates excellently with the quasi-TEM odd CPW mode. Furthermore, the electric field shown in Figure 4.6(b) illustrates the confined coupling between the two modes.

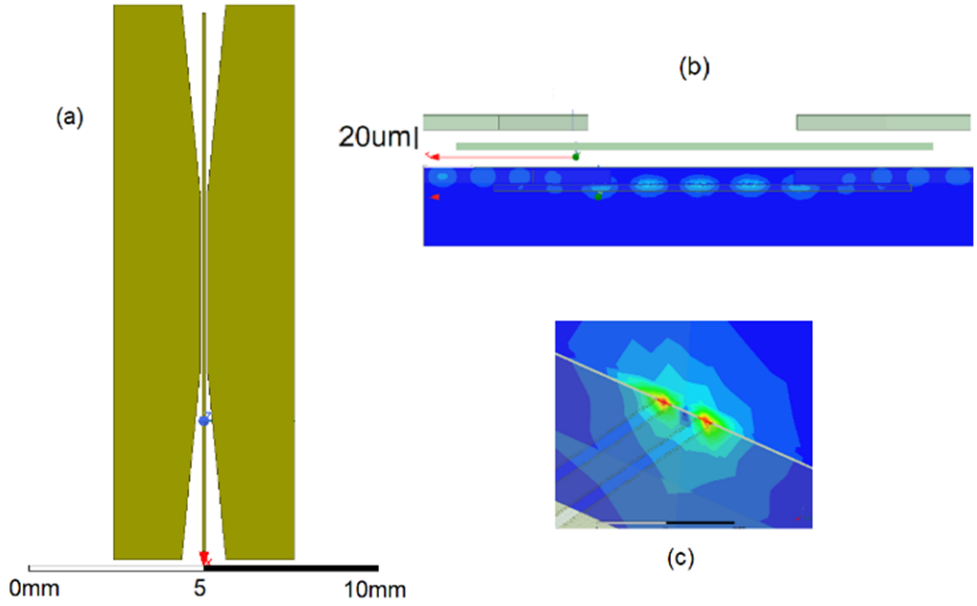


Figure 4.6: (a) a top view of the CPW transition. (b) a side view for the board excitation and field coupling. (c) Cross-sectional CPW mode after the transition.

The diagram in Figure 4.7 shows the DWG excited using a metallic WR15 waveguide at 60 GHz. A tapered section is employed to achieve the minimum coupling loss between the fundamental TE_{10} mode and the DWG mode. The insertion and return loss simulation results are displayed in Figure 4.8, with values of $-1.6dB$ and $-20dB$, respectively, at 65 GHz. It is important to note that multiple factors contribute to this loss, including matching losses between the WR15 and DWG, losses in the transition between the probes

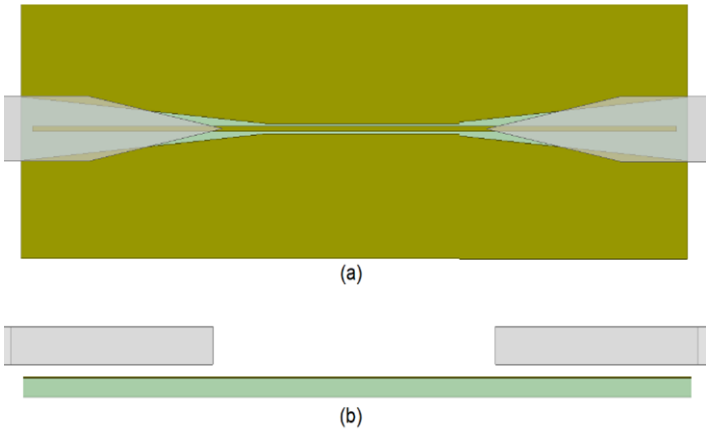


Figure 4.7: Schematics of the excitation for the CPW back-to-back transition using contactless dielectric probes. (a) Top view (b) Side view.

and CPW board, and ohmic losses, all of which are significant at such high frequencies. Furthermore, maintaining a fixed spacing of 20 um between the board and the probe during measurements is challenging. Therefore, a sensitivity analysis is conducted on the gap distance at 65 GHz, as demonstrated in Figure 4.9, indicating an acceptable level of divergence from the optimal value.

The board for the CPW transition is created with a laser machine and measures 5mm x 8mm. The Silicon probes are micro-machined in the QNFCF nanofabrication facility at the University of Waterloo, as shown in Figure 4.10. The probes are linked to the measurement system, which includes a VNA calibrated for the V-band, WR15 metallic waveguides, high-resolution motor stages to maintain probe alignment with the transition and a microscope. The board is fixed, and the probes are used to excite it with a consistent $20\mu m$ spacing between the probe and the board. The S-parameters are measured between the two ports, and the CPW under test produces a -3.4 dB insertion loss and a -15 dB return loss at

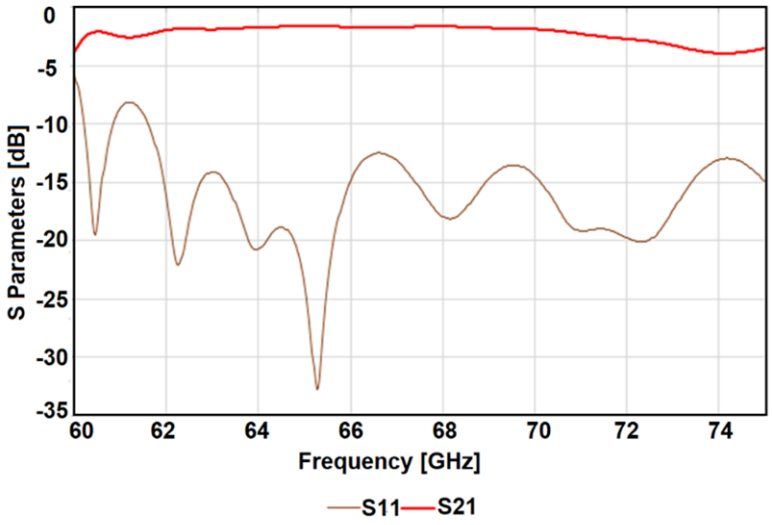


Figure 4.8: The simulated S-Parameters of the back-to-back WR excited DWG-CPW transition.

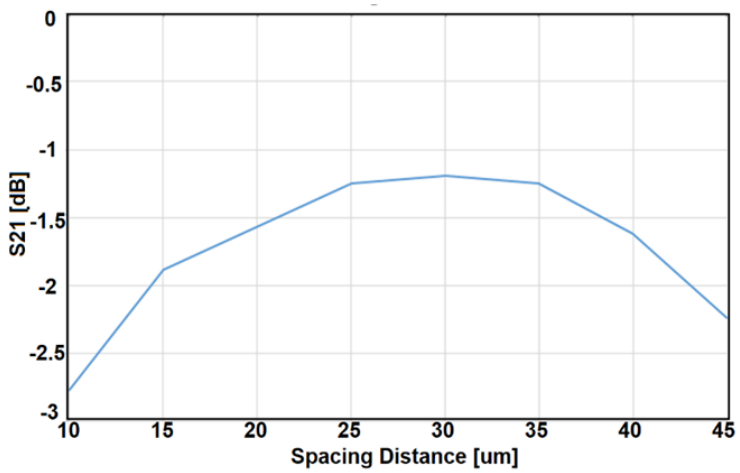


Figure 4.9: Sensitivity of spacing between probe and board and S_{21} at 65GHz.

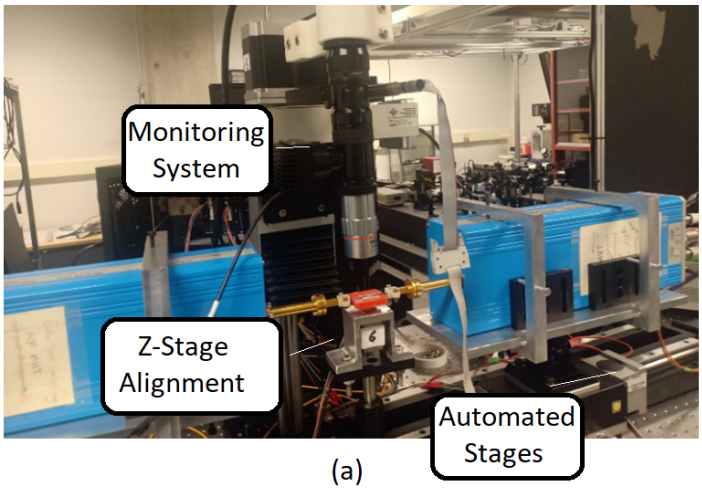
65 GHz, as shown in Figure 4.11. The simulated and measured results are reasonably consistent. However, a discrepancy of approximately -1 dB in the S_{21} measurement may be caused by probe misalignment with the board and non-uniform spacing between the probes and the board. Figure 4.12 shows the fabricated board under the microscope, revealing some substrate depth irregularities due to the laser machine fabrication process, which may contribute to the slight result mismatch, particularly at higher frequencies.

4.1.3 Microstrip Lines Excitation

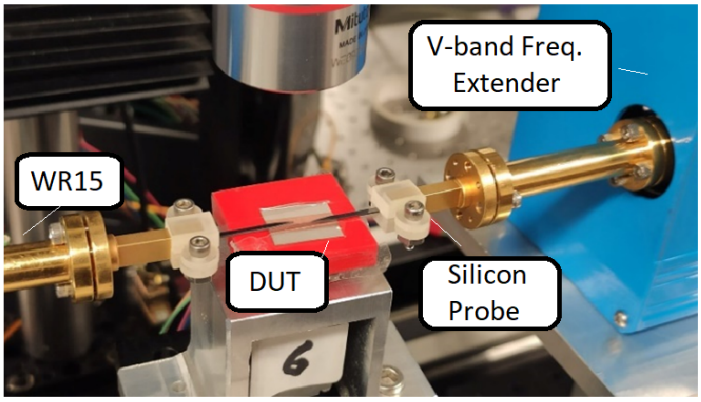
This section focuses on developing a contactless transition between silicon probes and Microstrip lines (MSL), commonly used for interconnects in MMICs and between chips on a board. MSL is a conductor strip of width w mounted on a grounded dielectric substrate of height h. The goal is to excite the single and differential quasi-TEM fundamental MSL mode. We present the differential excitation transition structure, followed by a modified version with a 180-degree phase shifter to excite a single MSL. The simulation of the back-to-back setup of the transition is discussed, and the experimental setup and measurements are presented.

Differential Microstrip Line Excitation

Differential MSL can be considered as two conductor strips with a 180 deg phase shift on top of a grounded dielectric substrate. The differential transition is designed for the V-band, and it relies on the coupling between the DWG's horizontally polarized mode and two MSLs located on the sides of the probe's taper tip without any contact between the



(a)



(b)

Figure 4.10: The experimental setup of the back-to-back CPW excitation using silicon probes in the V-band.

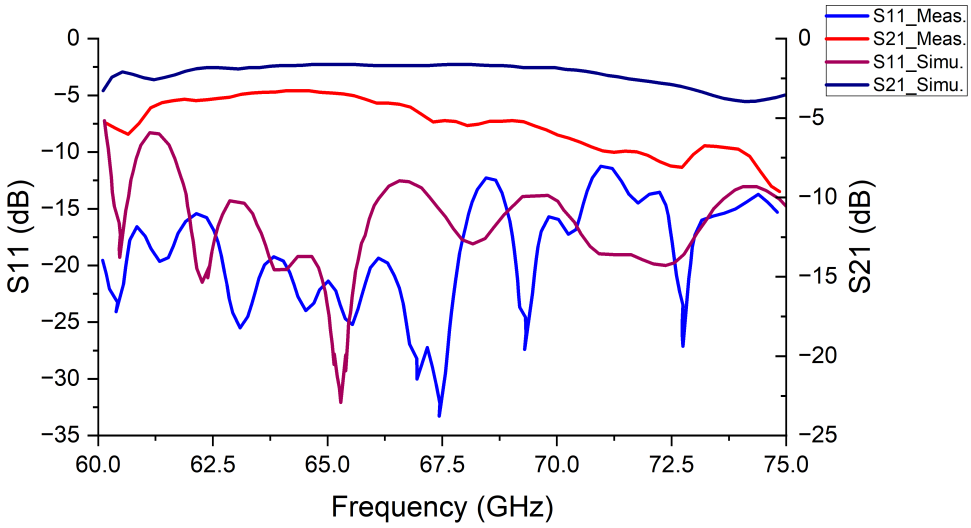


Figure 4.11: The measured S-Parameters of the back-to-back WR excited DWG-CPW transition by the VNA.

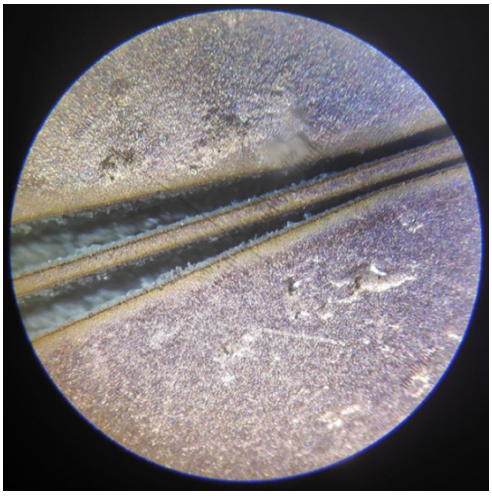


Figure 4.12: The fabricated CPW transition under the microscope.

probe and the board. The 50Ω, $0.63mm$ wide, two signal lines are patterned on top of a $10mil$ RO3003 substrate with $\frac{1}{4}Oz$ copper cladding. The same V-band silicon probe used in the previous section is utilized to excite the MS transitions. The coupling between the DWG probe mode and the Quasi-TEM MSL fundamental mode is performed in a contactless method by fixing the probe's tip at a $20\mu m$ distance from the MSL board, which is optimized for maximum power transfer from the taper section to the two MSLs. The schematic structure of the transition and the exciting DWG probe is shown in Figure 4.13. To evaluate the design and calculate the transmission and return loss of the transition, finite element simulation is performed using Ansys HFSS [92].

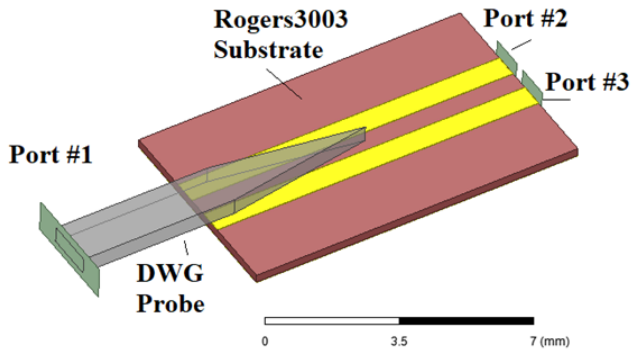


Figure 4.13: Schematic structure of the differential excitation for the MSLs using V-band Silicon DWG probe.

In the FEM study, the electric field distribution of the contactless transition between the silicon DWG probe and the differential MSL is presented in detail. Figure 4.14 shows the electric field distribution across the DWG probe and the differential MSL, respectively. It is observed that the probe excites the fundamental Quasi-TEM mode with a 180-degree phase shift between each line, as presented in Figure 4.14(c). Regarding performance, the

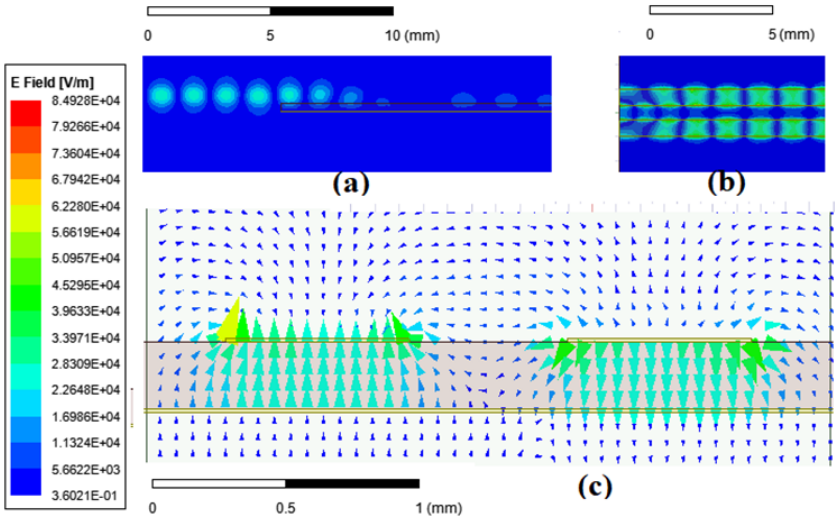
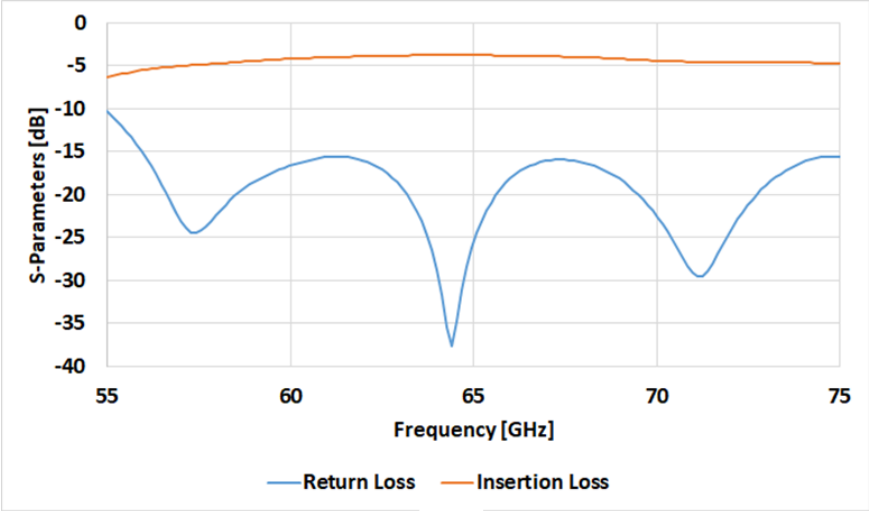
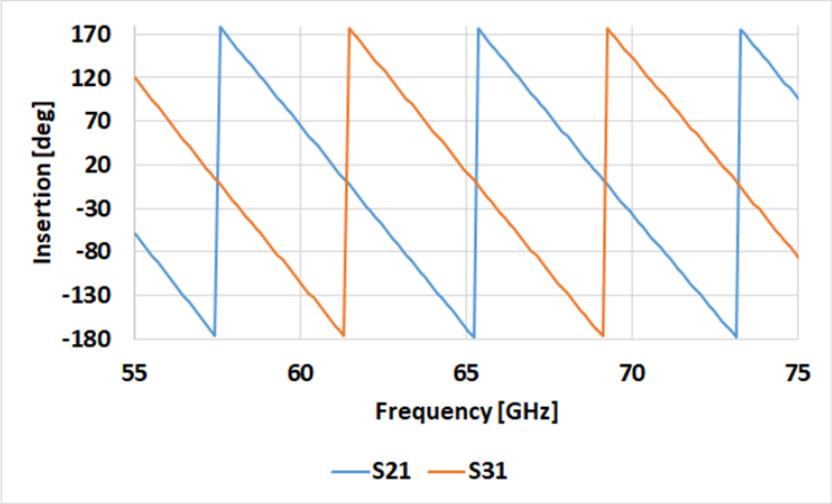


Figure 4.14: (a) the side view of the electric field distribution showing the coupling between the DWG and MSL modes at 65GHz. (b) The top view of the electric field distribution of the MSL at 65GHz. (c) The cross-sectional field distribution of the differential MSL at 65GHz.

insertion loss magnitude is evaluated and shown in Figure 4.15, indicating that it is 3.73 dB for each port at 65 GHz. Moreover, the phase difference between the differential MSL pair shows 180 degrees across the entire band, which is desirable for numerous applications. Additionally, the return loss for the V-band is evaluated to be less than 15 dB, indicating good matching between the two structures. In summary, these results demonstrate the feasibility and effectiveness of the proposed contactless differential excitation method using the transition between the silicon DWG probe and the MSL.



(a)



(b)

Figure 4.15: (a) Magnitude of insertion and return loss of the DWG probe to the differential MSL. (b) The phase of the differential MSL line.

Single Microstrip Line Excitation

Despite the advantages of differential excitation in a wide range of applications, such as exciting planar dipole antennas, there are certain circumstances in which it is advantageous to transmit power to a single MSL. This can be useful, for example, when testing single-feed MMICs with MSL input and output terminations. To achieve this objective, one method is modifying the differential transition to include an out-of-phase combiner in one of the MSL branches. This adds 180 degrees to the MSL and matches its phase with the other line. The modified transition is depicted in Figure 4.16 with the added bend combiner.

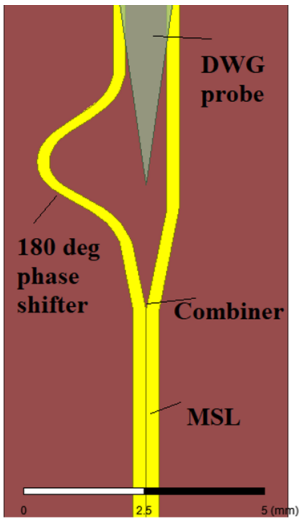


Figure 4.16: A schematic of the excitation for the single MSL transition using the contactless silicon probe.

Exciting the probe with a single 50Ω MSL transition is comparable to differential excitation. The transition can be adjusted to accommodate any signal line width by modifying matching parameters, but the signal line used in the simulation has a width of $0.63mm$ on a $10mil$ Rogers3003 substrate. The coupling distance is $20\mu m$, and the bend shifter

has a length of $0.9mm$. An analysis was performed on the sensitivity of the coupling distance, and it was found that it can tolerate up to 150% of the optimal spacing. Figure 4.17 demonstrates the field distribution on the board's top layer and at the cross-section of the MSL, showing the quasi-TEM mode confined in the substrate after coupling from the probe. According to the simulation results in Figure 4.18, the insertion loss is 0.86 dB, and the return loss is 17.5 dB at 65 GHz. The primary sources of degradation are the radiation from the probe's matching taper and the ohmic losses of the MSL.

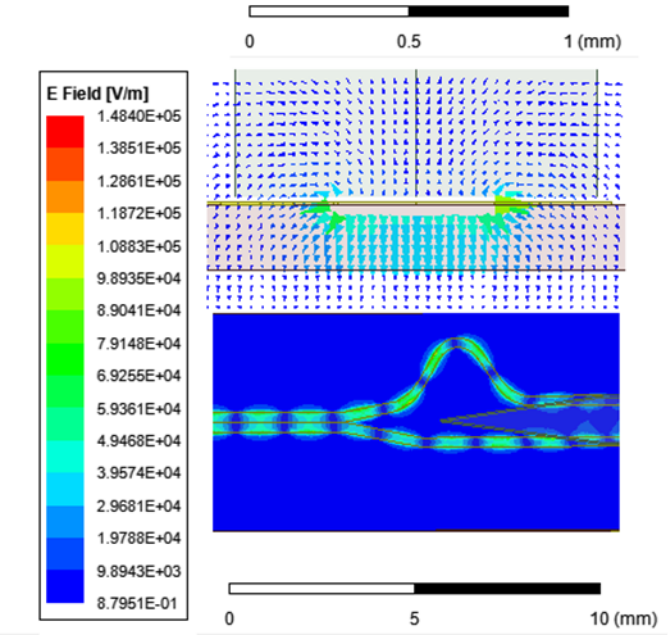


Figure 4.17: Field distribution at the cross-section and top layer of the MSL-DWG transition at 65GHz.

Experimental Setup and Measurements for the MSL transitions

The single and differential DWG-MSL transitions were fabricated on a single board utilizing a laser machine with dimensions of $20mm$ x $20mm$. The V-band silicon probes were used in the measurements. A schematic of the back-to-back structures is presented in Figure 4.19, which illustrates the board that houses the two transitions. The diagram displays the two MSL boards of the single and differential transitions stimulated by the DWG probes. The silicon probes are excited by metallic WR15 connectors linked to the measuring PNA-X, calibrated for the V-band using a calibration plane at the waveguide flange.

The positioning of the probes along the axial directions is determined by utilizing two printed pads on the top of the substrate, which serve as the initial reference points for the two probes. The two probes are alternately used to measure the two transitions at a contactless spacing of $20\mu m$. A movement stage is employed to secure the probes and reduce the tilt and offset detected at the alignment pads. The experimental setup, as depicted in Figure 4.20, is based on the schematic discussed earlier.

The measured S-parameters are then compared to the simulated back-to-back structure, and the results are presented in Figure 4.21(a). The comparison reveals an acceptable agreement, with an insertion loss of 2.8 dB and a return loss of 21 dB at 65 GHz for the single MSL transition. Conversely, the measured S-parameters for the differential MSL excitation, demonstrated in Figure 4.21(b), indicate an acceptable level of agreement with the simulated outcomes. The insertion loss is documented as 1.52 dB, and the return loss is lower than 15 dB at 65 GHz. The obtained experimental data confirms the simulated designs across the entire V-band frequency range. Consequently, the proposed transitions

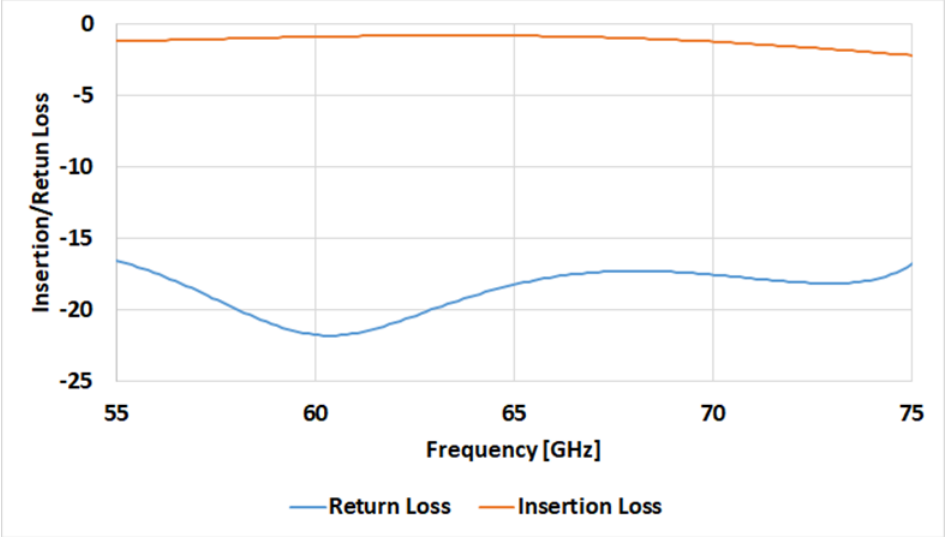


Figure 4.18: The DWG probe's simulated insertion/return loss to single MSL transition.

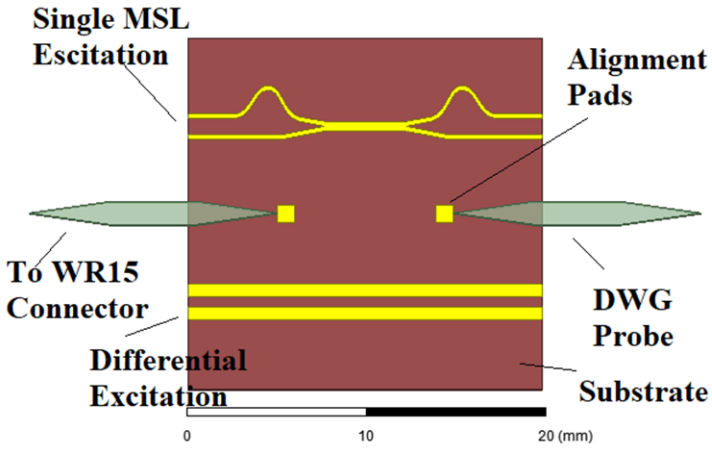
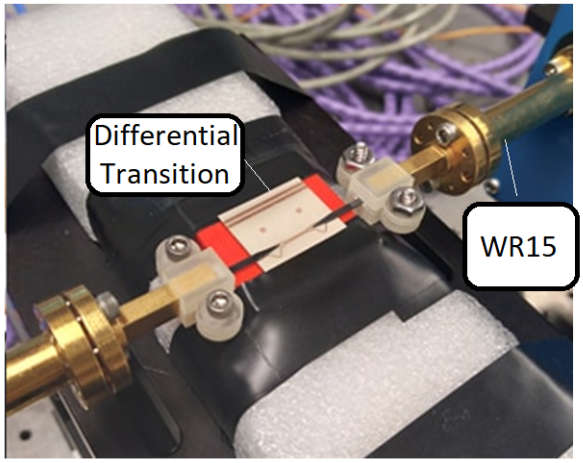
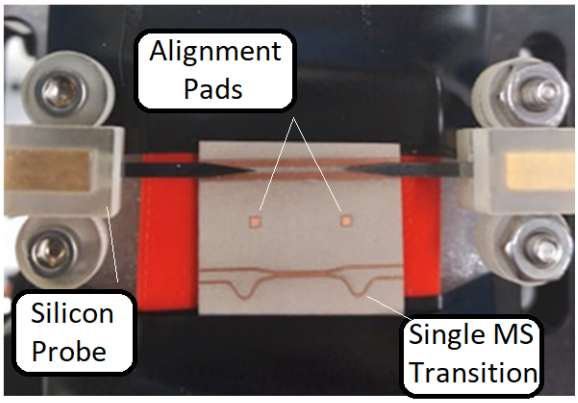


Figure 4.19: A schematic for the transition board, including the differential and the single MS excitation with the DWG probes.



(a)



(b)

Figure 4.20: The experimental setup of the back-to-back MSL transitions board excitation using DWG probes in the V-band for (a) the single MS transition and (b) the differential MS transition under test.

have successfully presented two distinct excitation methods for the MSL, and the results demonstrate their feasibility and high performance.

4.2 Characterization of Ultra-Short Wire Bonding-Based Embedded-EPIC Packaging using Silicon Probes

Electronic-photonic integrated circuits (EPICs) integrate both electronic and photonic components on a single chip, enabling high-speed, low-power, and low-cost data communication [93]. The packaging and interconnect technologies of EPICs play a significant role in their performance and reliability, with the packaging being a major contributor to the overall manufacturing cost [94]. Various packaging approaches have been proposed, including chip-scale packaging, fiber-to-chip coupling, and hybrid integration. EPIC hybrid integration using wire bonding presents challenges due to the different materials and geometries of the components, requiring high alignment accuracy and reliable electrical and optical interconnects. This section proposes a packaging method based on ultra-short wire bonding to minimize parasitic effects, validated by fabricating dummy chips on silicon wafers. The performance of the package and transitions in the V-band is presented and validated through simulations and experimental measurements. The proposed packaging method can be a good alternative for expensive and complex on-wafer testing.

The packaging technique involves placing chips in grooves on the silicon substrate to align the chip's surface with the substrate. This surface alignment enables the use of

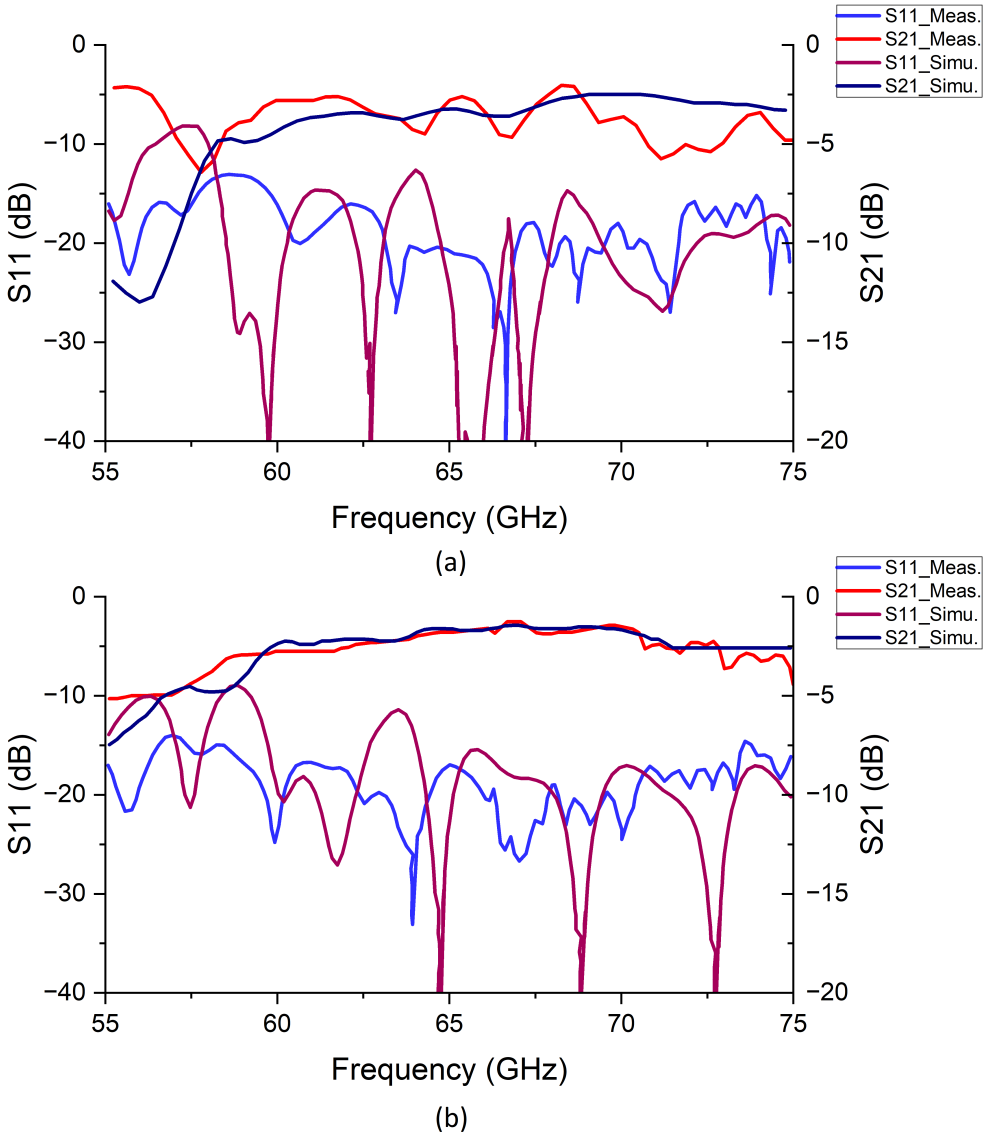


Figure 4.21: The measured and the simulated S-Parameters of the back-to-back WR15 excited DWG probe to-single MSL transition by the PNA.

ultra-short wire bonds with lengths of less than $100\mu m$. Such short wire bond lengths enhance electrical performance and improve matching between the chip and the substrate, especially at high frequencies exceeding 100 GHz. Dummy chips were fabricated on HR-Si wafers, featuring a $1\mu m$-thick layer of aluminum for patterning. The chip pattern included a through coplanar transmission line used to assess transmission through the package. The matching transition between the probing pads and the transmission line is illustrated in 4.22, demonstrating uniform and consistent bonds. Wire bonds with lengths of $80\mu m$ and heights of $100\mu m$ were utilized. Ansys Electronics was employed for finite element simulation to evaluate the design and determine the package's transmission and return loss.

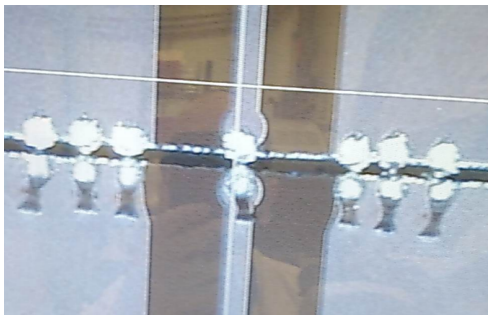


Figure 4.22: The ultra-short wire bonds connecting the wafer and an embedded dummy chip through GSG pads under the microscope.

The QNFCF facility at the University of Waterloo is utilized for micro-machining the chips. The chip fabrication process involves a single-mask lift-off process to pattern the sputtered aluminum layer, followed by wafer dicing into $3mm$ x $8mm$ chips. The grooves are prepared using a dicing machine, and the chips are subsequently inserted and secured with epoxy. Finally, ultra-short wedge wire bonds are connected in the QNFCF packaging

lab. Exciting the V-Band measurement is achieved using contactless silicon probes by fixing the probe's tip at a $20\mu m$ distance from the PCB. This distance is optimized for maximum power transfer from the taper section to the transition on the wafer, as discussed in previous sections. However, the probe excites a horizontally polarized $E_{x_{11}}$ wave mode. Therefore, the transition is designed in two stages: first, the probe to coplanar stripline (CPS) transition, and then a CPS to even-mode CPW transition as shown in Figure 4.23.

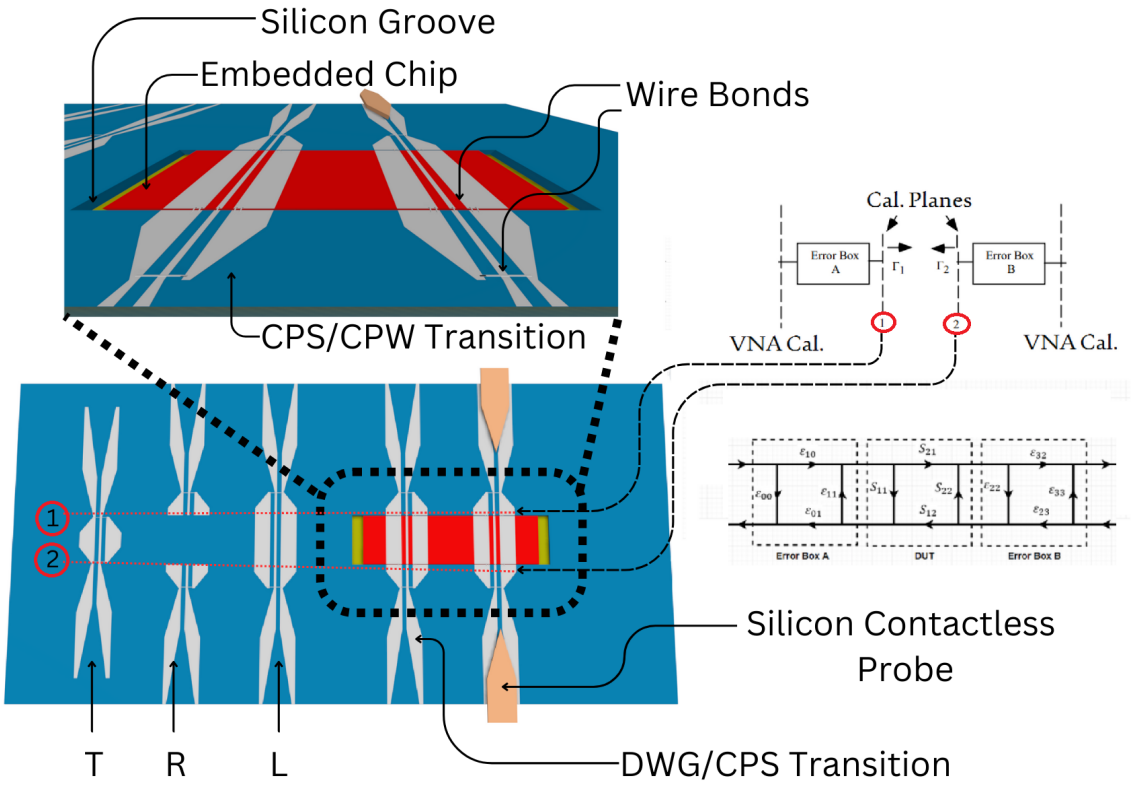


Figure 4.23: The 3D model of the package with the modified transition for contactless silicon probes, including a schematic for the calibration.

The objective of the measurement is to characterize the packaging method, including the on-wafer CPW to pad transitions and the wire bonds. The rest of the network is considered

error contributors. The VNA is calibrated at the WR15 flange plane using a three-step calibration approach: through, reflection, and line (TRL) calibration. The silicon probes, DWG to CPS transitions, and CPS to CPW transitions are treated as error boxes on each port side. These error parameters are extracted through post-measurement processing using TRL calibration structures on the wafer. Figure 4.24 illustrates the V-band silicon probe excitation for the embedded chip package. The measured S-parameters presented in Figure 4.25 show acceptable agreement with the simulated results. The insertion loss is recorded to be 2.59 dB, and the return loss is less than -15 dB at 65 GHz.

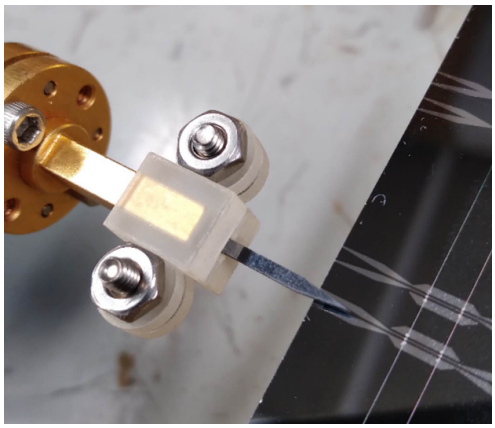


Figure 4.24: Contactless silicon probe excitation for the EPIC embedded package in the V-band.

In summary, embedding integrated chips within a groove of the silicon substrate and packaging them with ultra-short wire bonds has demonstrated its potential at high frequencies, exhibiting acceptable power transmission and matching. The performance of this method is comparable to more advanced packaging techniques, such as flip-chip packaging; however, it comes with a significantly less expensive process. Furthermore, the package was evaluated using V-band silicon contactless probes, which have demonstrated

their reliability in characterizing devices operating at high frequencies.

4.3 Novel THz All-Silicon DWG Probes

The extremely small dimensions of features at THz frequencies contribute to the fragility of conventional silicon DWG probes. The assembly process of inserting the waveguide into the Teflon-packaged metallic waveguide proves to be more complex compared to silicon probes operating at frequencies below 100 GHz, such as the V-band or W-band. Furthermore, handling the conventional probes can potentially damage the tapered probe tip, especially when the motorized stages are in motion. Therefore, this section proposes self-packaged all-silicon DWG probes. The modified probe design introduces support structures at the sides of the waveguides to facilitate handling. Additionally, the tapered tip is enclosed between thicker sections of silicon to simplify assembly with the metallic waveguide. Two modified versions of the probes are fabricated using laser machining: one for the D-band and another for the Y-band.

The D-band probe features cross-sectional dimensions of $500\mu m$ x $200\mu m$ for the DWG and a length of $L = 9mm$. A 500 μm thick HR-Si wafer is utilized to create the structure through laser patterning. Conversely, the Y-band probe has DWG cross-sectional dimensions of $200\mu m$ x $100\mu m$ and a length of $L = 5mm$. To fabricate this version, a $200\mu m$ thick HR-Si wafer is required. However, since wafers of such thinness are not readily available, a wafer-thinning process is employed. In this process, a $300\mu m$ thick HR-Si wafer undergoes etching to achieve a depth of $100\mu m$ in the wafer. Subsequently, the processed wafer is laser-milled to carve the probe pattern. The resulting configuration is depicted in

Figure 4.26(b), showcasing a few fabricated probes for both the D-band and the Y-band. Each wafer can yield numerous DWG probes. Additionally, Figure 4.26(a) illustrates the assembled probe within the WR5 metallic waveguide.

The performance of D-band coupling between two probes is measured to evaluate their efficacy. In Figure 4.26(c), the experimental setup featuring two D-band frequency extenders connected to the VNA is depicted. The D-band probes are inserted into the WR6.5 metallic waveguide, positioned with a gap distance of $20\mu m$ between their tapers. Figure 4.27(a) showcases the combined results of both simulated and measured S-parameters for the coupling between the two D-band probes. The outcomes demonstrate agreement with a minor variance, possibly attributed to misalignment during probe placement, misalignment between the two probes, or slight rotation of the probes from their horizontal positions. The simulated S-parameters exhibit an insertion loss of 0.54 dB and a return loss of less than -15 dB at 168 GHz. Meanwhile, the measured data reveals an insertion loss of 1.2 dB and a return loss of less than -15 dB at 168 GHz.

Conversely, the simulated coupling between Y-band probes is shown in Figure 4.27(b), indicating an insertion loss of 1.05 dB and a return loss of 20 dB at 495 GHz. The simulated electric field in Figure 4.27(c) portrays the effective coupling between the WR6.5 and the DWG for the D-band probe, while the probe-to-probe coupling at 168 GHz is illustrated in Figure 4.27(d) for the WR2.2 and DWG. These findings affirm the reliability of this excitation method, enabling high-quality modal stimulation above 100 GHz. This characteristic opens doors for its utilization in a wide array of applications.

4.4 Summary

In this chapter, we have presented a cost-effective and easily set up method for coplanar waveguide (CPW) excitation using micro-machined dielectric waveguide probes in the V frequency band. The transition design was fabricated using a laser machine, and the board's performance was evaluated using a VNA connected to the dielectric probes through metallic waveguides. The results demonstrate a close match between the measured data and the FEM-simulated design.

Furthermore, we have introduced two contactless silicon waveguide probe methods for exciting Microstrip lines (MSL). The first method involves exciting two MSLs with differential modes, while the second method employs a 180-degree bend combiner to excite a single MSL. These designs were simulated, fabricated, and measured, yielding promising outcomes that exhibit successful coupling of the DWG mode into the MSL modes. These methods provide a straightforward and economical solution for chip prototyping and debugging, with potential applications at higher frequencies up to the THz range.

Additionally, we have proposed a packaging design for electronic-photonic integrated circuits (EPICs) that employs ultra-short wire bonding to mitigate parasitic effects and enable high-speed data communication with RF signals up to 75 GHz. The design's validity was confirmed through the fabrication of dummy chips and subsequent measurements using contactless silicon probes, showing agreement with simulated designs. The proposed packaging design exhibited satisfactory performance, with an insertion loss of under 3.5 dB and a return loss of less than -12 dB. This enables high-performance EPICs for a wide range of applications and holds promise for even higher frequencies beyond 100 GHz.

Lastly, a modified version of the silicon probes displayed excellent power excitation at both the D-band and the Y-band. These new probes were successfully simulated and tested at the D-band to validate their operational concept. The results underscore their potential for THz probing applications.

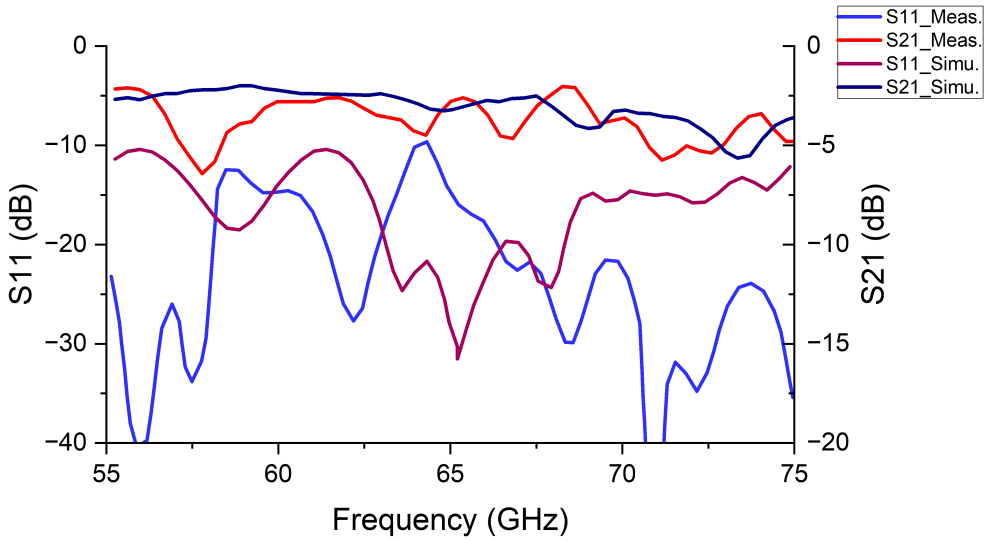


Figure 4.25: The measured and the simulated S-Parameters of the EPIC embedded package design by the PNA.

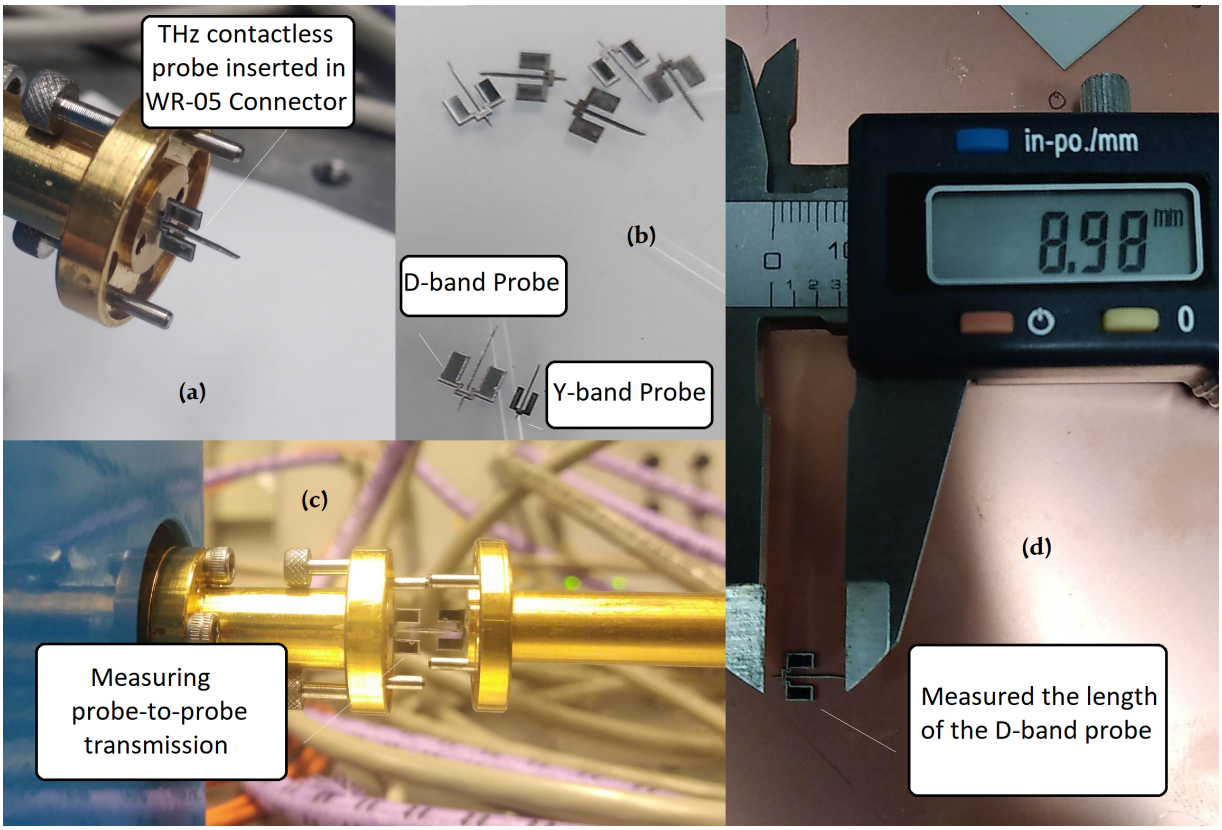


Figure 4.26: (a) The D-band probe inserted in the WR6.5 metallic waveguide. (b) A few fabricated D-band and Y-band probes. (c) The experimental setup for measuring the probe-to-probe coupling. (d) A length measurement for the D-band probe.

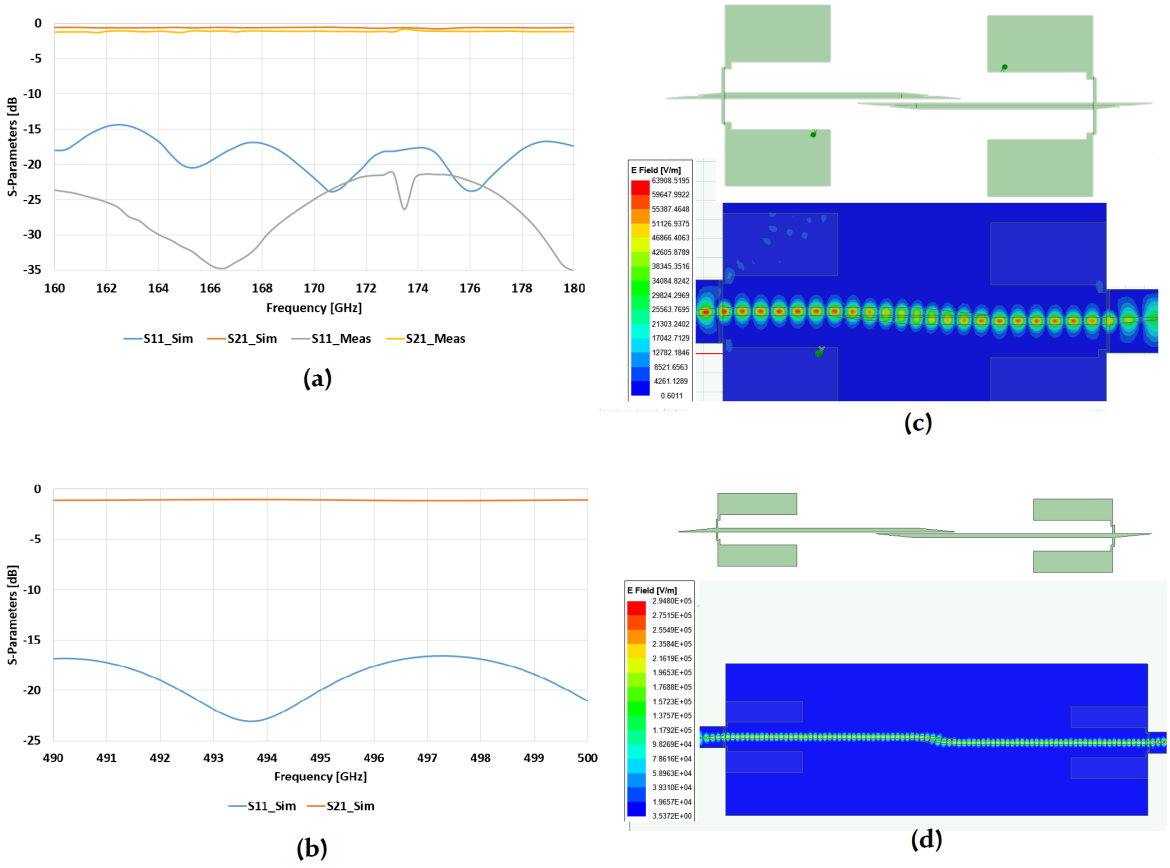


Figure 4.27: (a) The measured and simulated S-Parameters of the probe-to-probe D-band coupling. (b) The simulated S-Parameters of the probe-to-probe Y-band coupling. The electric field distribution in (c) the D-band probe and (d) the Y-band probe.

Chapter 5

THz Source Integration using EM-SSW Technology

In this chapter, we present a design for THz frequency multiplier sources utilizing planar GaAs Schottky diodes, employing the all-silicon EM-SSW technology introduced in Chapter 3. The proposed THz sources involve the hybrid integration of GaAs Schottky diodes, facilitated by the ultra-short wire bonding-based embedded chip packaging discussed in Chapter 4. We begin by introducing a single-stage frequency tripler operating within the V-band, specifically at 56 GHz. This tripler produces a third-harmonic output signal in the D-band. We elaborate on the tripler's circuit components, detail the system design approach, and analyze the fabricated prototype. The circuit components encompass PhC-based filters, low-loss modal transitions from DWG to metallic contact pads, and impedance-matching sections. Subsequently, we propose a prototype for the second-stage tripler operating in the D-band and generating a third-harmonic output sig-

nal at 500 GHz. Similar to the first stage, we outline the circuit components and provide a system analysis. We also discuss the experimental setup used to measure the output of both prototypes, employing contactless silicon probes. Lastly, we present a two-stage tripler design incorporating DWG power combiners to produce an output Y-band signal from a V-band pumped input. This final prototype primarily validates the operation of the proposed multi-band all-silicon integration technology. In the forthcoming sections, we will introduce three distinct THz sources based on the multi-band all-silicon EM-SSW integration technology discussed in Chapter 3, coupled with the embedded wire-bonded chip packaging proposed in Chapter 4. The first device is a single-stage tripler operating in the D-band, yielding an output power of 168 GHz. The second device is a single-stage tripler for the Y-band, producing an output signal at 500 GHz. The third device comprises two cascaded triplers stimulated with a Y-band input signal, generating output power at 500 GHz. This later device is designed to showcase the multi-frequency operation potential of the EM-SSW technology.

5.1 Proposed Hybrid-Integrated D-Band Source on EM-SSW All-Silicon Technology

This section presents the modeling schemes for analyzing Schottky diode-based triplers. We first begin with discussing the method used to explore all the triplers covered in this chapter. Next, we apply the proposed analysis method to design the D-band single-stage tripler. Finally, we delve into the fabrication of the D-band THz source prototype and

the necessary test setup to measure its performance, allowing for a comparison with the simulated design.

5.1.1 D-Band EM-SSW Tripler Modelling and Analysis

The tripler utilizes an EM-SSW technology design with a V-band waveguide for the input and a D-band waveguide for the output, as depicted in Figure 5.1. It is optimized for the maximum input power of our available source in the CIARS lab, i.e., 12 dBm, with a center frequency of 56 GHz. Typically, a conventional frequency multiplier setup includes components such as an input low-pass filter, an input-matching network, diodes (or other nonlinear semiconductor devices), an output-matching network, and an output high-pass filter. In balanced configuration designs, there is no need for an idler circuit since even harmonics are suppressed. In some cases, the output high-pass filtering is achieved through the cutoff of the output waveguide. However, the topology presented in this design integrates the matching networks and CPS transitions in one design block. The chip channel features an anti-parallel Schottky diode configuration to suppress the generation of even harmonics. In this approach, the Schottky diodes are coupled to waveguides using CPS transitions. The design procedure, shown in Figure 5.2, for this tripler is outlined in detail in the following steps.

1. The tripler model consists of three main components: a) the embedded diode chip and its groove housing; b) the input filter and matching block; and c) the output matching block. The Schottky diode chip, produced by VDI, was simulated using a comprehensive 3-D model incorporating internal ports at the anode terminals. This

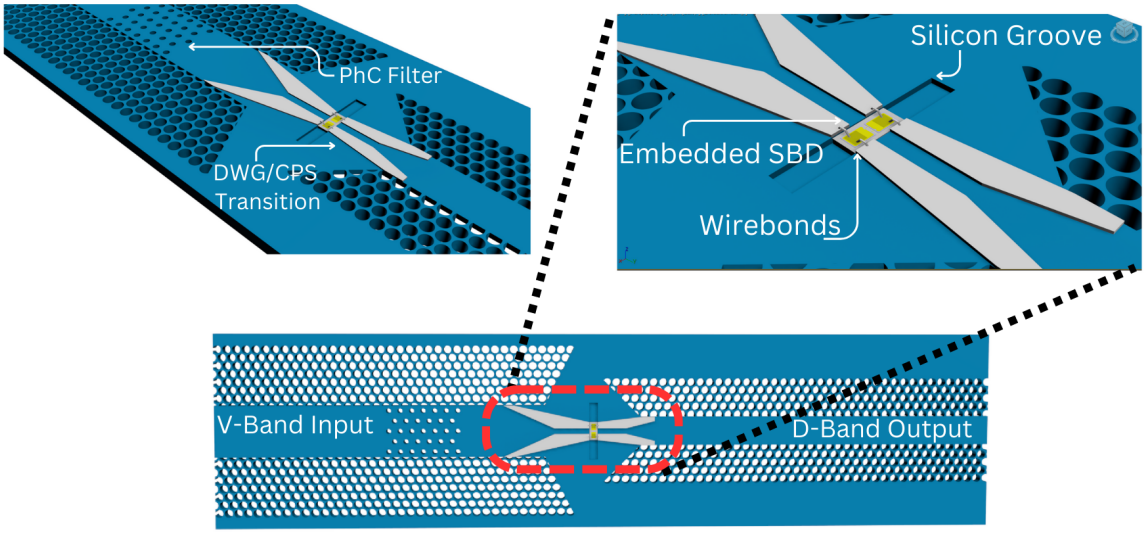


Figure 5.1: A 3D model for the D-band Tripler showing its components and the embedded SBD packaging.

modeling approach allowed for the accurate determination of the chip's S-parameters, including all parasitic elements. Obtaining precise S-parameters was crucial for accurately determining the input and output impedance;

2. To design the source, it is necessary to determine the embedding impedance (Z_{in} and Z_{out}) of the mounted diode chip at the input and output frequencies. Circuit simulation software, such as ADS, models the nonlinear Schottky junction and performs harmonic balance simulation on the structure. Key diode parameters, including series resistance, ideality factor, saturation current, and nonlinear junction capacitance at zero bias voltage, are defined within the ADS diode model. By optimizing the com-

plex source and load impedance at the fundamental and third-harmonic frequencies to achieve the desired incident power levels, the impedance can be obtained;

3. After obtaining the embedding impedance at the output and the input of the source, a passive EM simulation is used to design each block in the circuit, such as the filter and matching blocks, and obtain their S-parameters. The input and output matching blocks include the DWG/CPS transition at one terminal and match the other terminal to the embedding impedance of the diode;

4. Finally, a system circuit simulator, i.e., ADS, is used to perform a harmonic balance simulation for all system components, utilizing the extracted S-matrices for the passive system components and the nonlinear diode model to determine the desired output's third harmonic level.

The selection of circuit topology is a critical decision primarily influenced by the available technologies. Implementations of THz-wave circuits vary, ranging from more simple and cost-effective hybrid integration. This method typically utilizes low dielectric and low-loss materials like HR silicon, along with discrete diode components that are mounted or soldered onto the circuit using packaging technologies, such as Flip-chip or Wire-bonding [95]. On the other end, there are ultra-thin membrane MIC structures, which offer an array of circuit features such as beam leads, on-chip resistors and capacitors, and air bridges. Additionally, some MMICs are diced and mechanically thinned to fit the waveguide assembly [50]. In our design, we employ a hybrid topology, embedding anti-parallel diode chips inside silicon grooves using wire bonding. Figure 5.3(a) presents the chosen shunt-connected anti-parallel-diode bias-less topology.

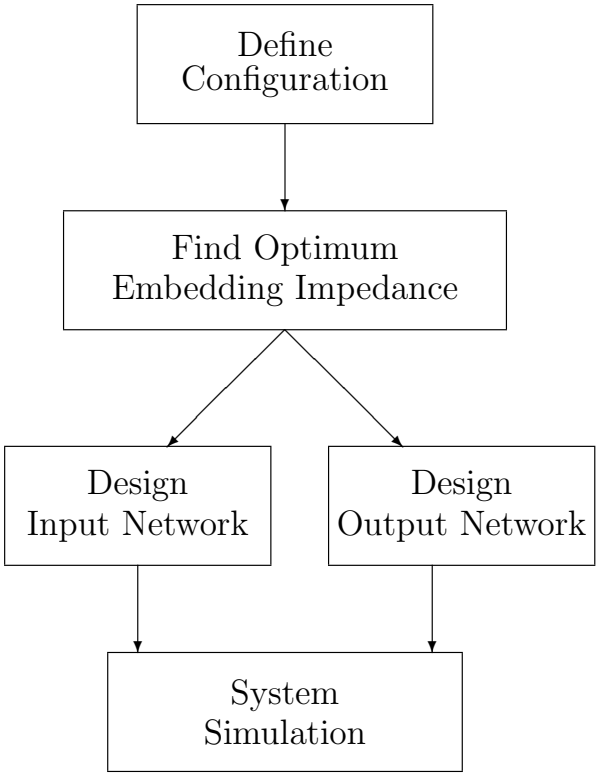


Figure 5.2: Flowchart for the design steps of the tripler

In order to accurately determine the optimal embedding impedance for the diode chip terminals, it is essential to conduct a comprehensive 3D electromagnetic (EM) simulation of the diode within its circuit environment. The 3D model of the diode package is depicted in Figure 5.3(c), constructed based on the information provided by the supplier. In the simulation, the diode pad interfaces are extended, and the reference plane of the CPS transmission line ports is later de-embedded to align with the diode reference planes and accurately extract the S-parameters of the diode. The active part of the diode is substituted with an internal lumped port, allowing for the separation of the diode barrier (the non-linear component) from the diode parasitics (the passive 3D portion). To ensure the correct anti-parallel configuration, Figure 5.3(b) illustrates the approach. The optimal embedding impedance for the diodes can be calculated using load-pull techniques and harmonic balance simulations.

The circuit model in Figure 5.3(d) implements the nonlinear diode model in ADS. The series resistance R_s, as shown in equation **??**, represents the total diode resistance, including the epitaxial layer resistance $R_{epitaxial}$, the spreading resistance R_{spread} in the highly doped layer, and the ohmic contact series resistance R_{ohmic}. The cutoff frequency of the diode in equation 5.5 depends on the series resistance and the junction capacitance C_j. For high-frequency operation, the junction capacitance needs to be minimal. This can be achieved by reducing the epitaxial layer doping concentration or opting for a smaller anode size; however, this increases the series resistance. The increase in series resistance elevates the conversion loss in varactors, and the nonlinear C-V characteristics lead to harmonic generation. The voltage-dependent junction capacitance $C_j(v)$ can be calculated using equation 5.4. The ideality factor n, as shown in equation 5.3, along with I_o and R_s,

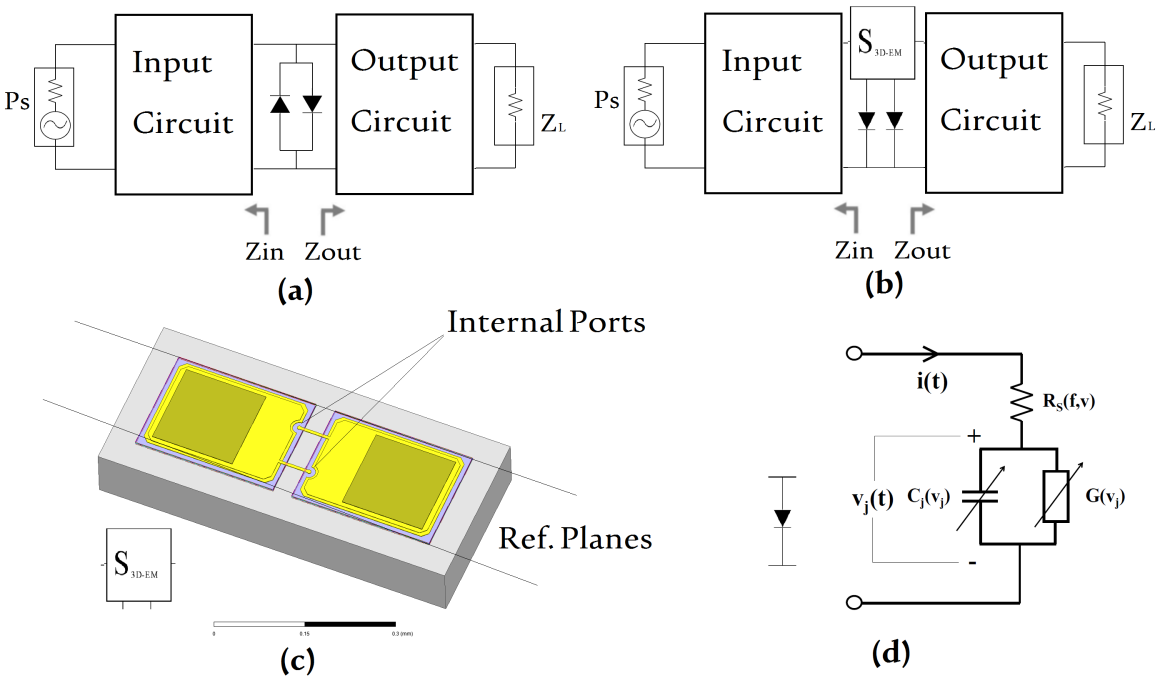


Figure 5.3: (a) Circuit model of the THz tripler (b) Equivalent circuit model of the tripler using co-simulation method (c) 3D EM-diode model used to extract diode's parasitic model. (d) Diode's simplified circuit nonlinear model.

can be obtained from the diode I-V characteristics. In our case, the diode supplier, VDI, in collaboration with Modelithics Inc., provides a precise diode circuit model. This model is imported into the ADS circuit simulator, incorporating all parameters provided by the supplier's product information sheet [96] [97].

$$I(v) = I_o(\exp(\frac{qv}{nk_BT}) - 1) \tag{5.1}$$

$$G(v) = \frac{dI}{dV} = \frac{q}{nk_BT} I_o \exp(\frac{qv}{nKT}) \tag{5.2}$$

$$n = q\Delta V \log(e)/k_BT = \frac{\Delta V}{0.05783} \tag{5.3}$$

$$C_j(v) = \frac{C_{jo}}{\sqrt{1 - \frac{v}{\phi_b}}} = w\sqrt{\frac{qN_d\epsilon_s}{2(\phi_b - v)}} \tag{5.4}$$

$$f_c = \frac{1}{2\pi R_s C_j(v)} \tag{5.5}$$

where k_B is Boltzmann's constant, T is the temperature, N_d is the epitaxial layer doping concentration, v is the voltage across the junction, ϕ_b the built-in junction potential, w is the depletion width, q is the electron charge, ϵ_s the dielectric permittivity of GaAs, and n is the ideality factor.

5.1.2 D-band Tripler Design Procedure

The analysis begins by determining the parasitic 4-port S-matrix for the diode model. The EM-simulation, shown in Figure 5.4, is conducted through 4-ports: two wave ports that excite the CPS transitions and two internal lumped ports at the diode anodes [98]. The impact of the CPS transitions is subsequently de-embedded since we have the S-parameters from a separate EM simulation. Following this, the 4-port matrix is incorporated into the ADS circuit simulator alongside the nonlinear diode circuit model provided by VDI

Inc. and Modelithics Inc. to perform the harmonic balance (HB) analysis needed for determining the optimal diode chip embedding impedance, as illustrated in the schematic of Figure 5.4. The HB simulation involves varying the impedance values at the diode circuit's input and output and calculating the third harmonic level. In our analysis, the optimal embedding impedance at the input and output are practical values that yield the highest third harmonic level for the given input power of 12 dBm. Table 5.1 presents the optimal values of the diode embedding impedance determined through the simulation study.

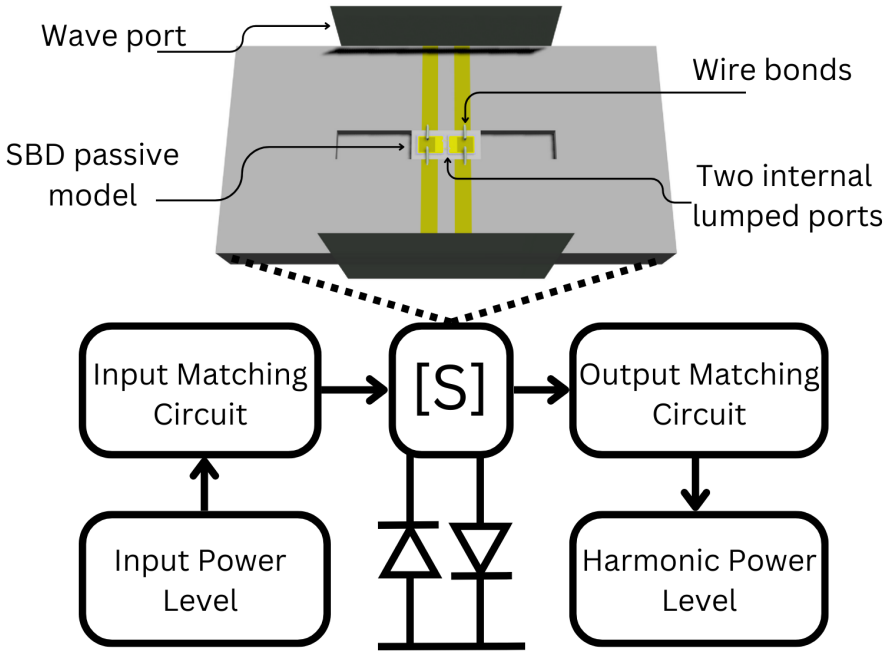


Figure 5.4: (a) A schematic for the analysis used to determine SBD's embedded impedance illustrating the harmonic balance simulation and the FEM analysis included for determining SBD's passive network.

Subsequently, each passive component is designed and simulated to extract the scatter-

Table 5.1: Input and output embedding impedance values of the diode chip for the D-band Tripler at an input of 56 GHz

Impedance	Value	Frequency	Power
Z_{in}	$21 + 67j$	Fundamental	12 dBm
Z_{out}	$36 + 42j$	Third Harmonic	12 dBm

ing matrix individually. For instance, this includes the EM-SSW input and output waveguides, the PhC filter, the CPS/DWG transitions, and the contactless excitation probes. In our design, we have combined the CPS/DWG transitions and the matching circuitry into a single block. Then, the matching blocks are optimized for maximum power transfer to a lumped port, using the same values of embedding impedance extracted in the previous step of the study. Figure 5.5(a) illustrates the EM simulation employed for optimizing the matching transition at the V-band, including the electric field in the CPS line. The results presented in Figure 5.5(c) demonstrate excellent matching across the V-band, with an insertion loss of $S_{21} = 0.67$ dB and a return loss of $S_{11} \approx 20$ dB at 56 GHz. Similarly, Figure 5.5(b) portrays the matching transition for the output D-band, and the outcomes in Figure 5.5(d) exhibit a low-loss matching spanning the D-band, featuring an insertion loss of $S_{21} = 0.73$ dB and a return loss of $S_{11} \approx 30$ dB at 168 GHz.

Photonic Crystal PBG Filter

After designing the CPS/DWG transitions for the input and output, the PhC PBG filter is developed to feature a rejection band at the third harmonic frequency while preserving low-loss transmission within the input pass band. The underlying concept of such filters

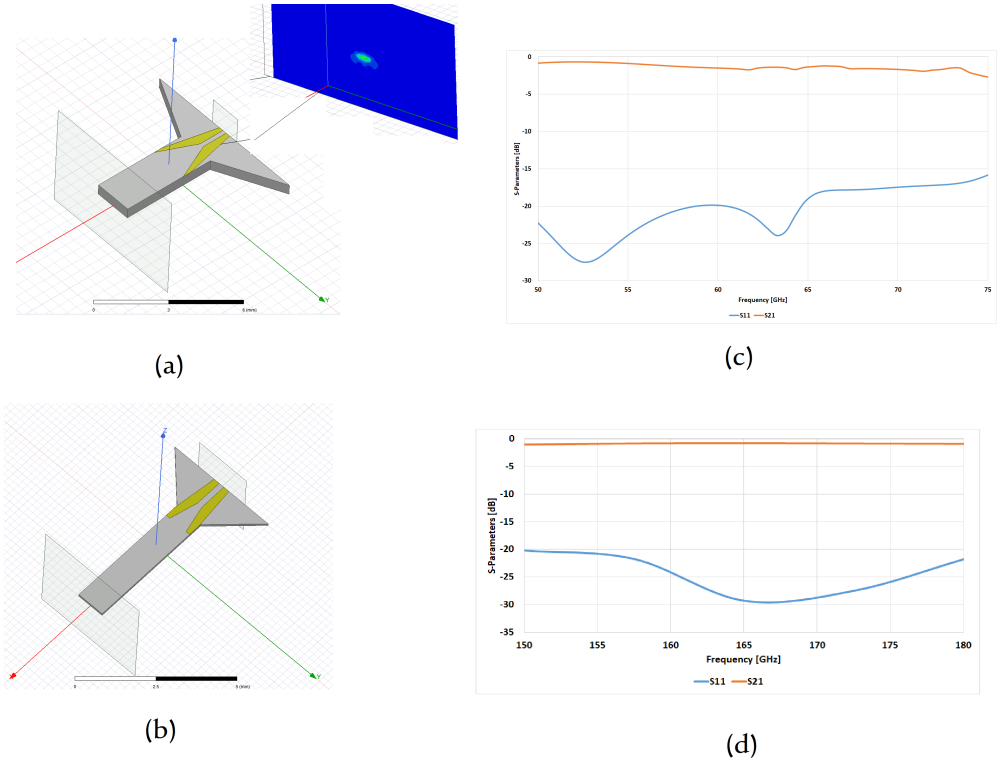


Figure 5.5: (a) DWG/CPS transition at V-band. (b) DWG/CPS transition at D-band. (c) Simulated S-parameters of the V-band transition. (d) Simulated S-parameters of the D-band transition.

revolves around creating a photonic bandgap that effectively inhibits modal propagation at the desired rejection frequencies. The PBG is fashioned by establishing a periodic arrangement of PhC unit cells. Figure 5.6(a) presents the schematic of the D-band PhC PBG filter. The implementation of this filter is executed on the V-band EM-SSW channel, employing a photonic crystal periodic structure with a lattice constant of $a = 400\mu m$ and a diameter of $d = 150\mu m$. A photograph of the fabricated filter is depicted in the SEM image presented in Figure 5.6(b). It is noteworthy that the fabricated structure possesses grooves

in the EM structures adjacent to the filter. This is because the PhC filter operates as an EM structure for signals within the pass band, which consequently results in a reduction in the contrast between the strip and the surrounding cladding. To design the band gap rejection band at the third harmonic for the output, an Eigenmode analysis is conducted on the unit cell of the PhC structure using CST Software. The dispersion diagram displayed in Figure 5.6(c) visually illustrates the creation of the desired band gap within the D-band. To validate the performance of the filter within both pass and stop bands, the S-parameters are simulated for two measurements, spanning the V-band and the D-band. As depicted in Figure 5.7, the measured S_{21} at 168 GHz is below -10 dB, while the measured insertion loss within the pass band, i.e., 56 GHz, is recorded as $S_{21} = 1.7dB$.

Subsequently, the PhC-PBG filter and the matching transition are unified within a single EM simulation, incorporating the silicon probe for achieving a match across the entire input circuitry to align with the input diode embedding impedance. Similarly, the output circuit, encompassing the matching transition, D-band EM-SSW, and the D-band contactless probe, is optimized to align with the output diode embedding impedance. The results of these two simulations yield two S-matrices for the input and output circuitries, which are then combined with the 4-port S-matrix of the diode model within the final harmonic balance simulator to estimate the system's conversion efficiency. Figure 5.8 elucidates the input and output final circuitry simulation adopted for extracting the input and output S-matrices. The simulated S-parameters for the input circuitry, post-optimization to conform with the diode's embedding impedance, demonstrate a total insertion loss of $S_{21} = -1.17dB$ and a return loss of $S_{11} \approx -15dB$ at 56 GHz. Conversely, the output circuitry displays $S_{21} = -1.4dB$ and $S_{11} \approx -20dB$ at 168 GHz. Figure 5.9 shows the

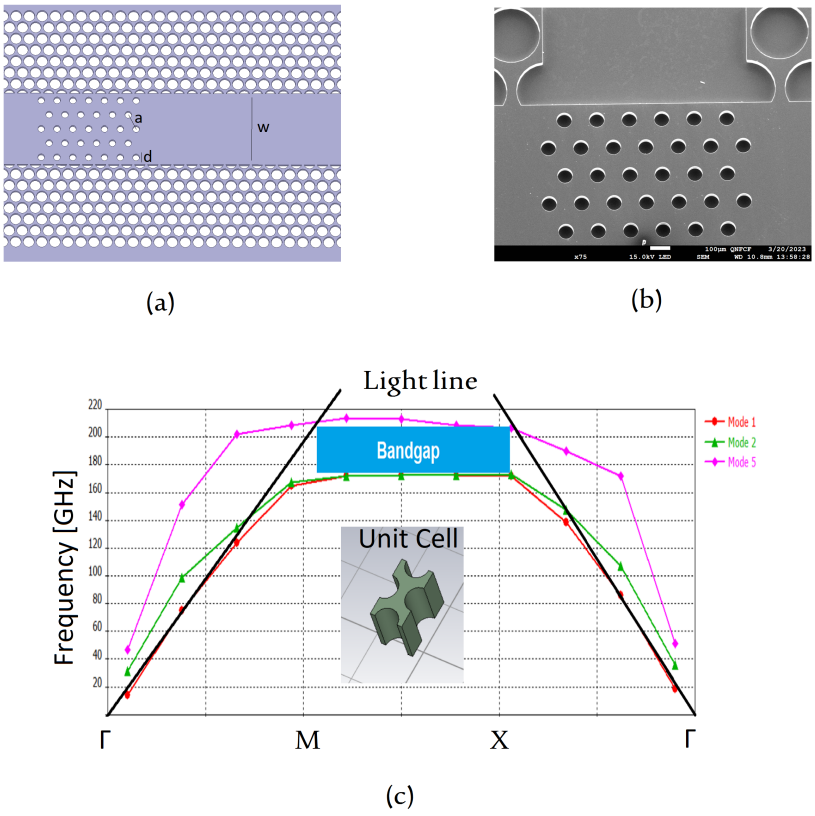
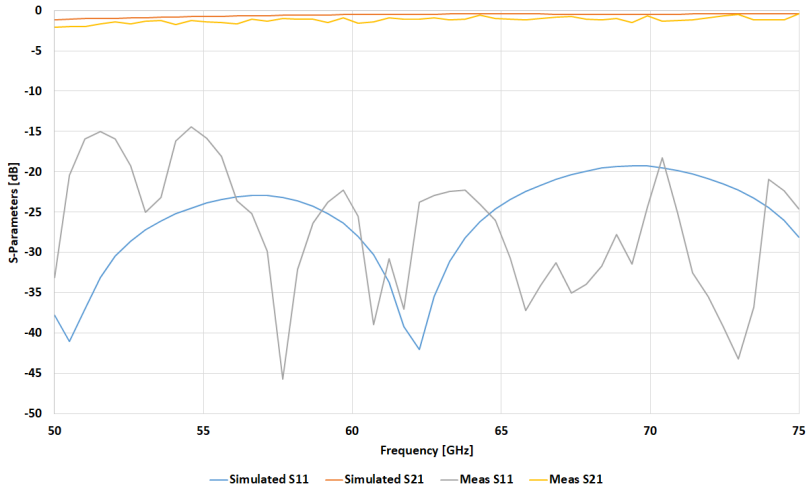
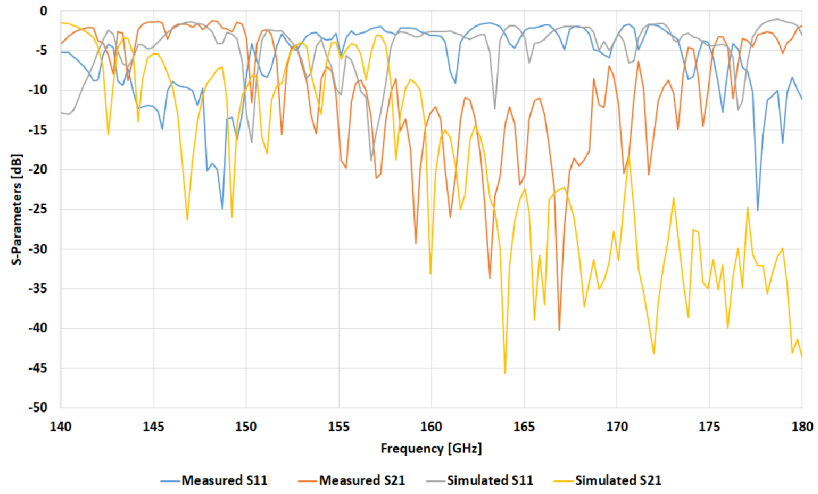


Figure 5.6: (a) A schematic for the D-band PhC-PBG filter. (b) SEM picture for the PhC-PBG filter. (c) The dispersion diagram for the periodic structures.

outcomes of the combined system harmonic balance simulation within ADS. The conversion loss, as defined in equation 5.6 denoting the ratio between the available source power $P_{in_{source}}$ and the output harmonic power $P_{out_{harmonic}}$, serves as a metric to characterize the harmonic power delivered to the load by the frequency multiplier. The input power level is set to 12 dBm to align with the rated output of the V-band OML extender output power. The simulated output third harmonic power stands at approximately $\approx 1.5dBm$, with a conversion loss of 10.5 dB.



(a)



(b)

Figure 5.7: (a) The simulated and measured S-parameters for the pass band of the D-band PhC PBG filter. (b) The simulated and measured S-parameters for the rejection band of the D-band PhC PBG filter.

$$CL = \frac{P_{in_{source}}}{P_{out_{harmonic}}} \tag{5.6}$$

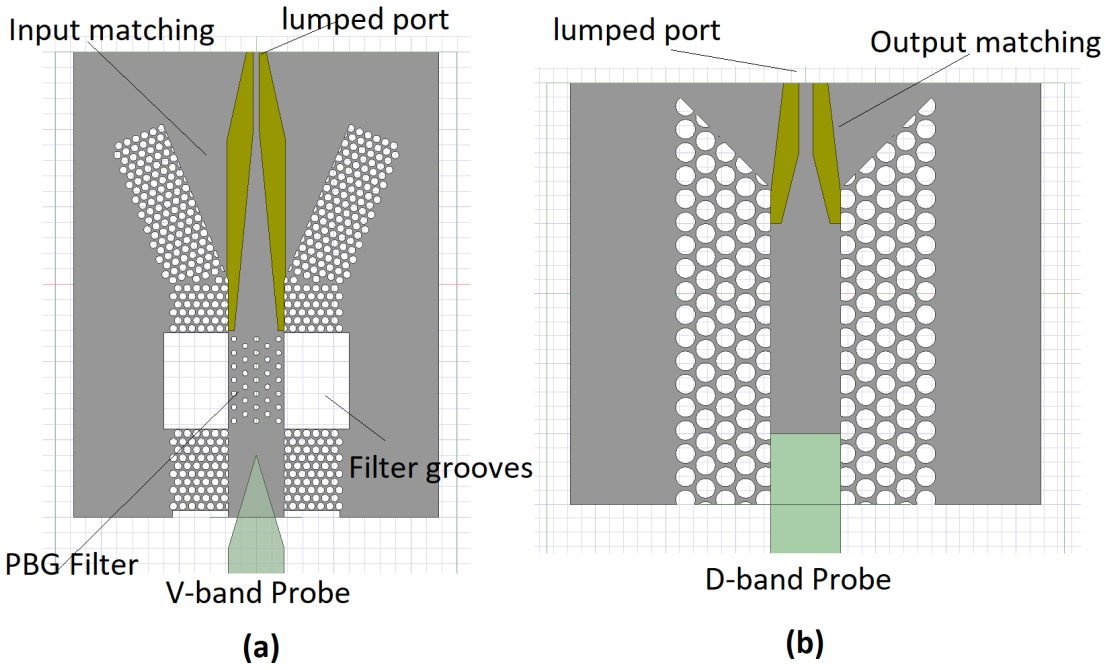


Figure 5.8: (a) The simulated input circuitry for final S-matrix extraction. (b) The simulated output circuitry for final S-matrix extraction.

5.1.3 D-band Tripler Fabrication and Experimental Measurements

The multi-band all-silicon EM-SSW integration technology is employed to fabricate the D-band tripler, as discussed in Chapter 3. This tripler operates across two distinct frequency bands: the V-band and the D-band. Consequently, a 500 μm HR-Si wafer is utilized to

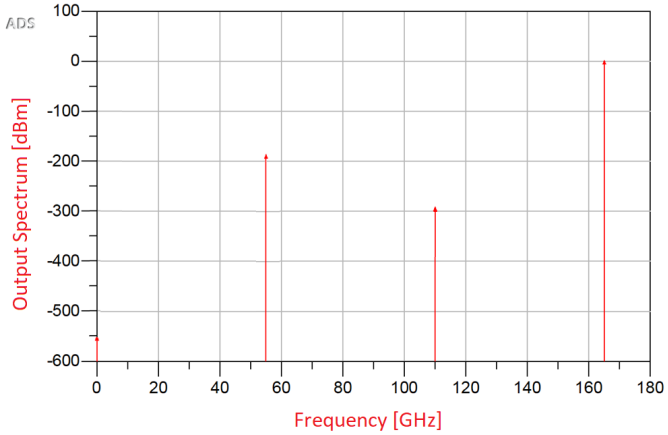


Figure 5.9: The simulated output harmonics of the D-band tripler with an input power of 12dBm.

implement the EM-SSW, featuring two different height levels; a full-thickness of 500 μm for the V-band and 100 μm for the D-band. The fabrication process involves the use of three masks: a front-side mask for depositing the metallic structures, another front-side mask for etching 100 μm into the silicon for chip groove patterning, and a back-side mask for etching 400 μm into the silicon to define the EM-SSW D-band strip. The fabrication steps closely mirror the process detailed in Chapter 3. After device fabrication, the wafer is diced into smaller pieces, each containing devices, to prepare for packaging and testing. Figure 5.10 visually outlines the pivotal fabrication stages under both optical and SEM microscopes. The first mask's wafer patterning is depicted in Figure 5.10(a), showcasing a 750nm deposition of the Aluminum layer. The second mask reveals the etching of 100μm deep chip grooves, displayed in Figure 5.10(b). The depth of the 100μm trenches is measured using a stylus profilometer to assess the accuracy of the DRIE process following the initial mask. The outcomes depicted in Figure 5.11 affirm the precision of the fabricated

depth. The assembly of the diode chip within the silicon groove entails applying a thin layer of epoxy to the back of the chip, followed by meticulous placement within the designated pocket to align with the CPS input and output lines, as visualized in Figure 5.10(c). Finally, the embedded chip is connected to the CPS input and output lines through wire bonding, facilitated by 25μm thick wedge Aluminum wires of ultra-short length and height, both measuring less than 100μm. Figure 5.10(d) presents an SEM image showcasing the final packaged chip.

The setup for testing the D-band tripler is illustrated in Figure 5.12. The configuration comprises an input power source operating at the V-band, specifically an OML frequency extender capable of delivering an output power of 12 dBm. Additionally, there is an output PM4 THz power meter by VDI, alongside motion stages that enable movement along the primary directions. The input source is linked to a V-band silicon contactless probe using a metallic WR-15 connector. In contrast, the output power meter is connected to a D-band silicon probe via a WR-6.5 connector. The positioning of the probes is established through the use of a Z-motion stage, ensuring a separation distance of 20μm for optimal modal coupling. The power meter is calibrated through direct through-connection with an external known power source, with internal calibration weights adjusted to facilitate precise power measurements. This arrangement mirrors the simulated harmonic balance analysis detailed in the preceding section. Given that the levels of other frequency components are anticipated to be significantly lower than the device's noise floor, the power meter is adept at accurately detecting the harmonic power level. Thus, this configuration is harnessed to determine the conversion loss of the tripler prototype.

A graph depicting the measured output power of the D-band tripler is presented in Fig-

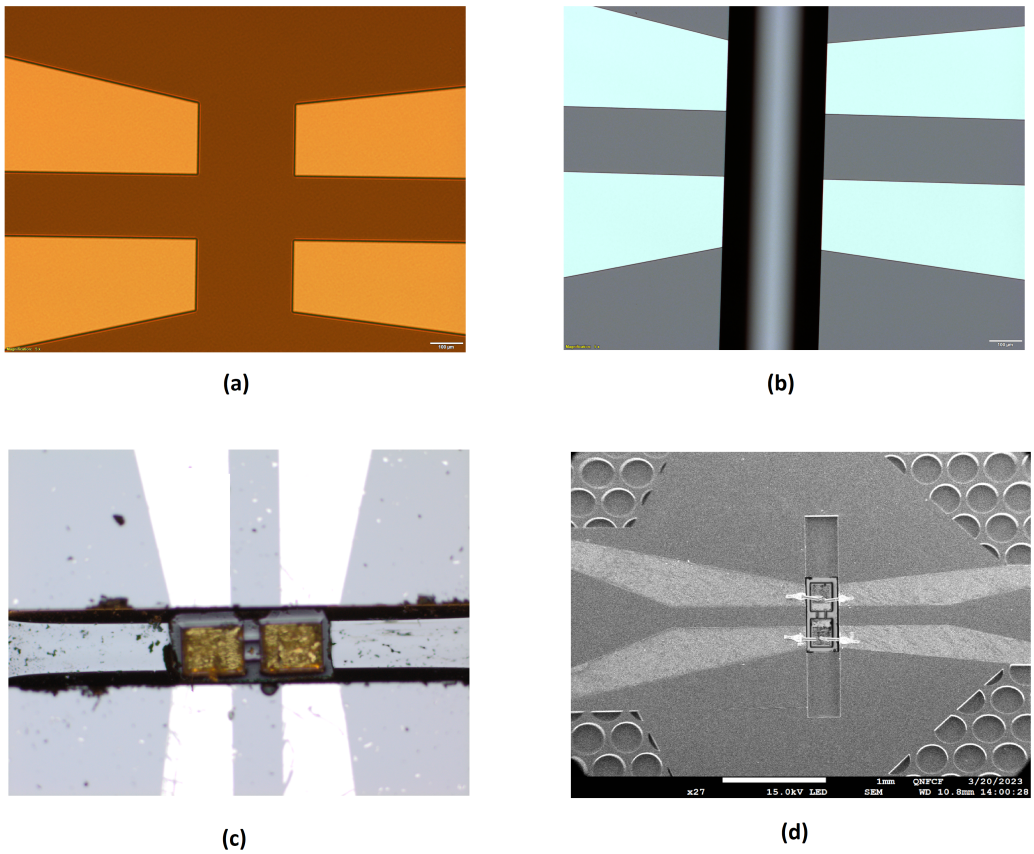


Figure 5.10: (a) The deposited Aluminum layer after the first mask. (b) The etched silicon groove after the second mask. (c) Chip assembly in the silicon pocket. (d) SEM picture for the packaged embedded chip in the silicon groove.

ure 5.13. The input power level was calibrated and approximated to be around 12.5 dBm. The highest achieved output power registers at approximately -0.67 dBm at 167 GHz, resulting in a conversion loss of about 13.17 dB. While discrepancies between the simulated results and the actual measurements are expected due to the model's nondeterministic parameters, particularly at THz frequencies, the reported results remain reasonable. Various

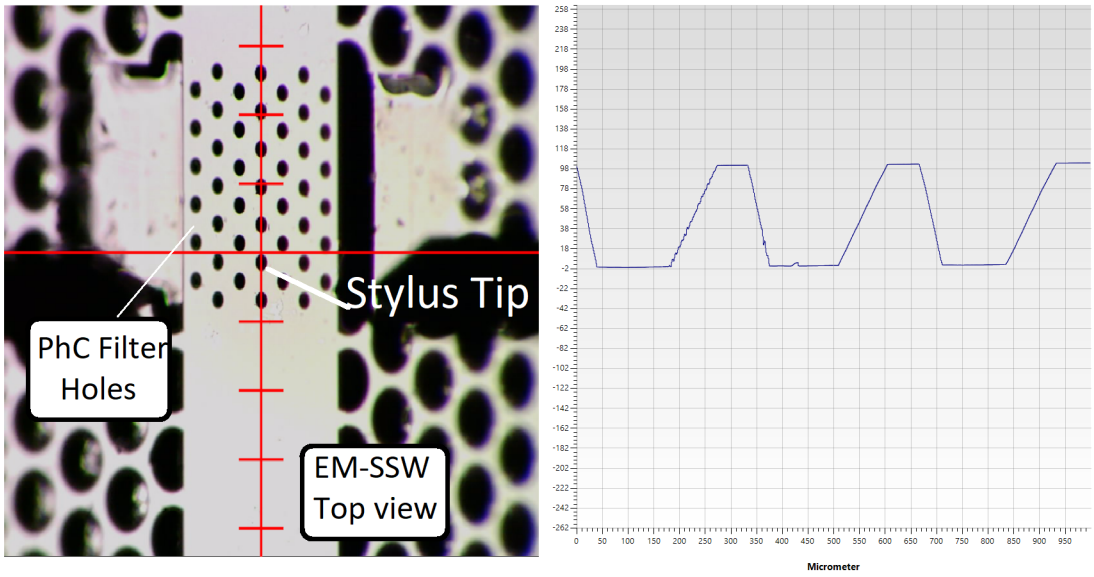


Figure 5.11: Measuring the depth of the $100\mu m$ trenches after the first mask DRIE process .

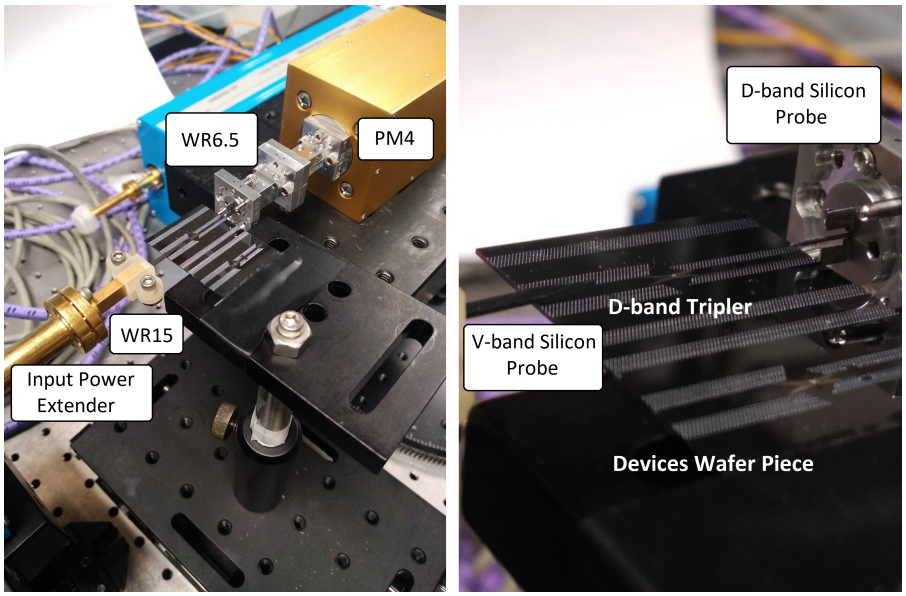


Figure 5.12: Test setup for the D-band Tripler.

random factors contribute to errors in the test setup, such as probe misalignment, tilts, inconsistencies in the chip back-epoxy, misalignment during chip assembly, and inaccuracies in wire bonding. These errors are likely to have an adverse impact on performance since the chip assembly is carried out manually during the prototyping phase.

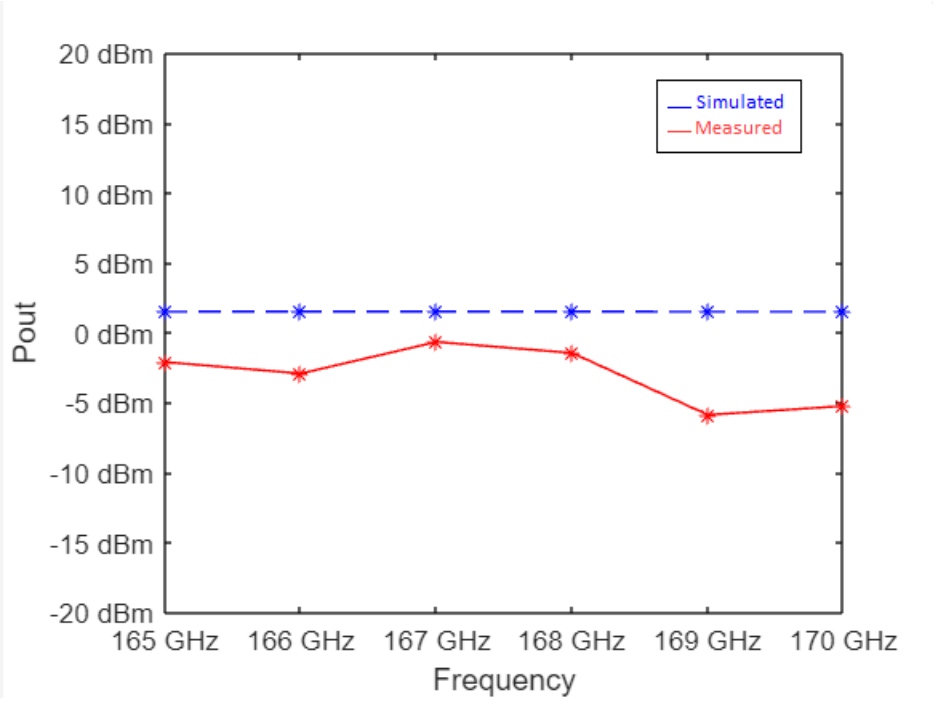


Figure 5.13: Simulated and measured output power level for the D-band tripler prototype.

5.2 Y-Band EM-SSW-Based Integrated THz Source

The same procedure discussed in the previous section for designing the D-band THz source is employed in the design of the Y-band tripler prototype. The tripler is constructed on the EM-SSW platform, featuring a D-band waveguide for the input and a Y-band

waveguide for the output, as illustrated in Figure 5.14. The device encompasses the same components outlined in the design of the D-band tripler, encompassing the DWG/CPS matching transitions, PhC filter, and EM-SSW waveguides. The 3D electromagnetic model is utilized to extract the S-matrix for the diode chip. With the assistance of the Modelithics Inc. diode model, the simulated diode S-matrix determines the diode embedding impedance values for both the input and output circuitry. The embedding impedance values for the input and output diode are tabulated in Table 5.2 and are derived using an input power level of 1.5 dBm, corresponding to the output of the D-band tripler. These values are then utilized in the subsequent steps, where the extracted S-matrices for each passive circuitry are matched for maximal harmonic generation in the harmonic balance simulation.

Table 5.2: Input and output embedding impedance values of the diode chip for the Y-band Tripler at an input of 168 GHz

Impedance	Value	Frequency	Power
Z_{in}	$34 - 22j$	Fundamental	1.5 dBm
Z_{out}	$30 + 62j$	Third Harmonic	1.5 dBm

The input circuit of the Y-band tripler in Figure 5.15(a) comprises the D-band EM-SSW waveguide featuring an embedded PhC-PBG filter in the suspended strip. Additionally, the DWG/CPS transition is optimized to match the diode's embedding impedance to the value defined within the lumped port. On the other hand, as depicted in Figure 5.15(b), the output circuit incorporates the output DWG/CPS matching transition on the Y-band EM-SSW, with dimensions $W_s = 200\mu m$ and $h_s = 100\mu m$. It is important to note that the height of the Y-band suspended strip remains consistent with that of the

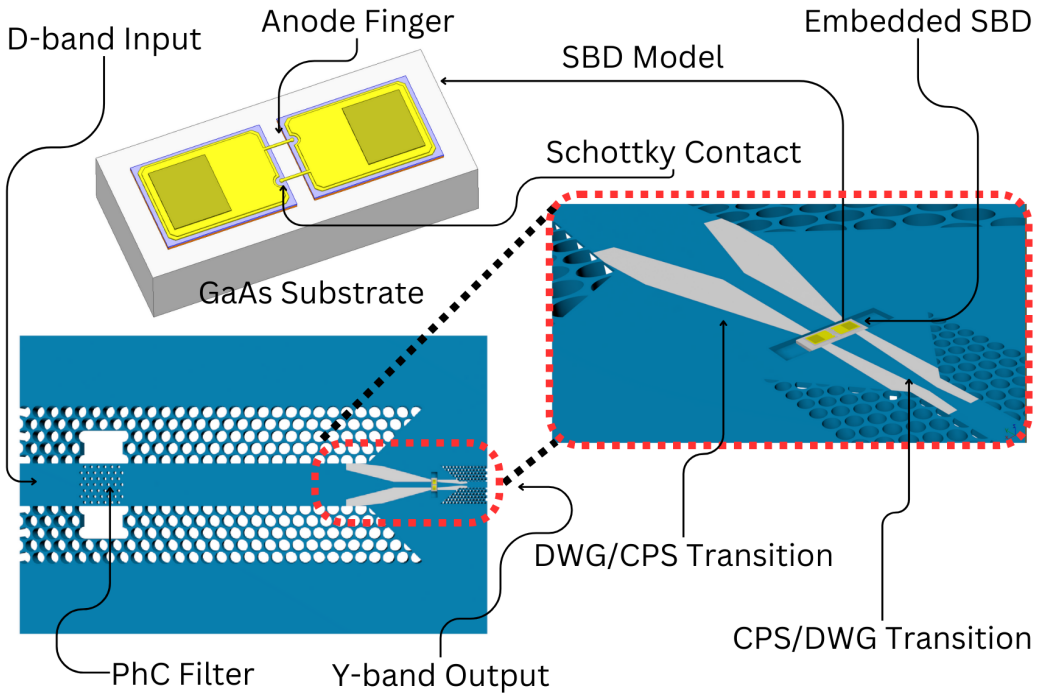


Figure 5.14: A 3D model for the Y-band tripler showing its components and the SBD embedded packaging.

D-band. Therefore, there is no requirement for additional masks in the process, which can accommodate the newly introduced Y-band.

Consequently, the S-parameters for the input and output circuitry were calculated using the 3D Ansys HFSS EM simulator. In Figures 5.16(a) and (b), the insertion loss and return loss for the pass band and the stop band of the PhC-PBG filter are shown, respectively. The PBG was tuned in the Y-band, specifically around a center frequency of 500 GHz. The insertion loss in the pass D-band is $S_{21} = 0.4dB$ and the return loss S_{11} is less than $-15dB$, while the insertion loss in the rejection Y-band is more than $20dB$ and the return loss is $-1dB$ at 500 GHz. It is important to emphasize that the filter is not 100% reflective

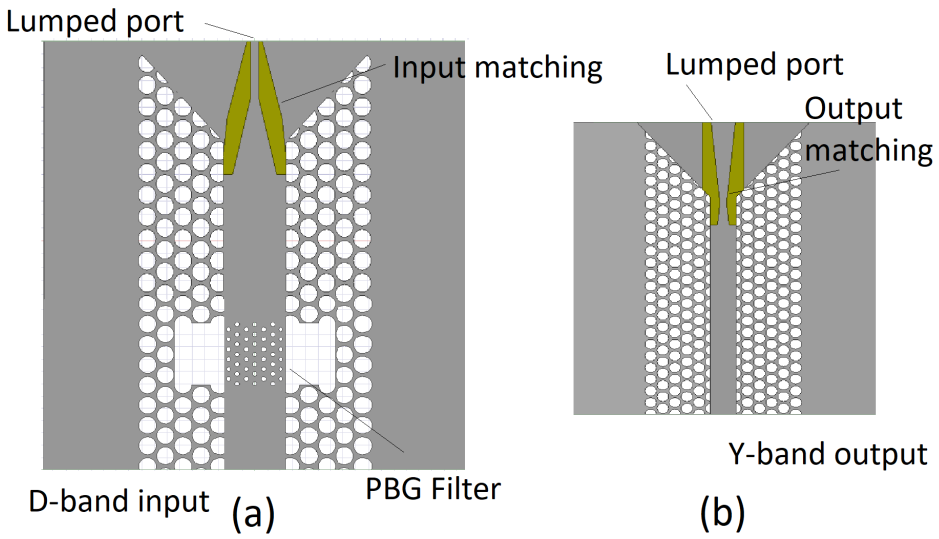


Figure 5.15: (a) The simulated input circuitry for the final Y-band tripler. (b) The simulated output circuitry for the final Y-band tripler.

due to the radiating nature of dielectric waveguides.

The S-parameters for the input passive circuitry are reported in Figure 5.16(c) to indicate excellent matching between the output DWG mode from the D-band tripler and the Y-band SBD embedding impedance. The insertion loss of the input circuit is $S_{21} \approx 1dB$ at $168GHz$ with a flat response in the D-band. On the other hand, the S-parameters of the output circuit, presented in Figure 5.16(d), show a flat matching of S_{11} less than $-25dB$ with a low insertion loss of $S_{21} \approx 1dB$ at 500 GHz. Table 5.3 presents the estimated insertion loss for the D-band and Y-band tripler components. Next, the harmonic balance simulation is conducted for the Y-band tripler, and the conversion loss is estimated to be 28 dB for an input power of 1.5 dBm. However, the estimated output power is close to the PM4 power meter's sensitivity limit. Figure 5.18 shows the tripler at the various fabrica-

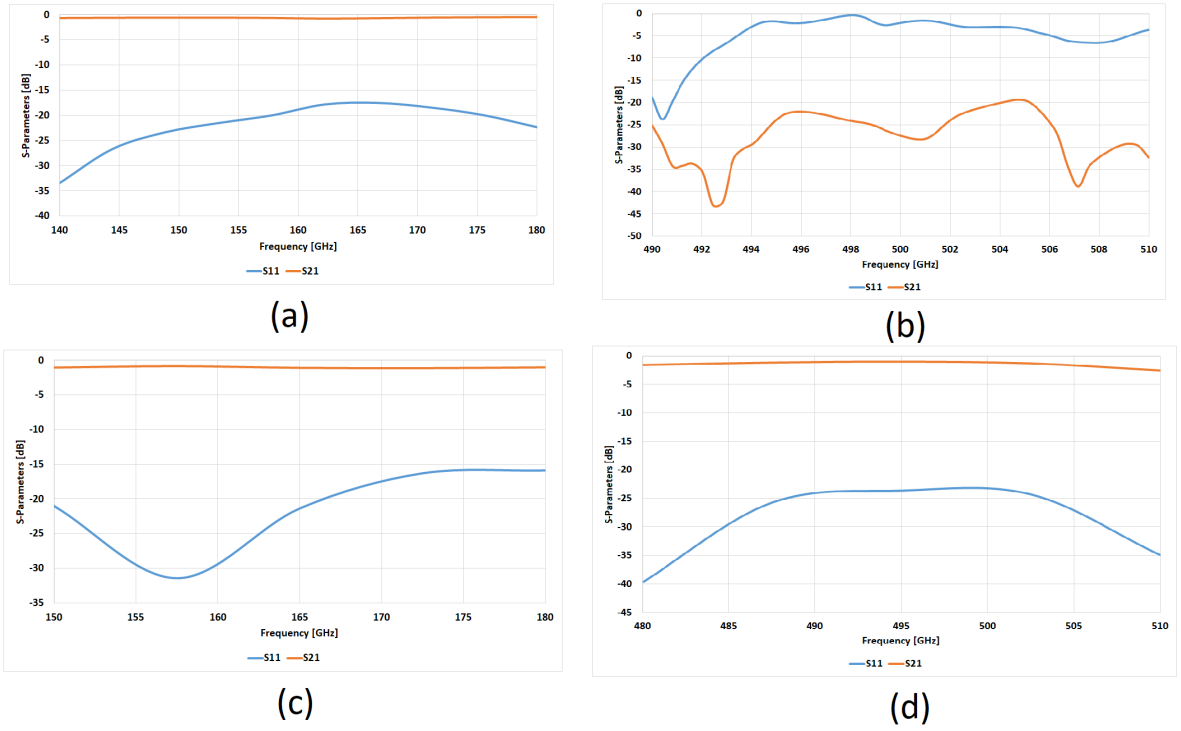


Figure 5.16: (a) Simulated S-parameters for the PBG filter pass band. (b) Simulated S-parameters for the PBG filter stop band. (c) Simulated S-parameters for Y-band input circuitry. (d) Simulated S-parameters for Y-band output circuitry.

tion stages under optical and scanning electron microscopes. The images in Figure 5.18(a), (b), and (c) illustrate the DWG/CPS transitions, the PBG filter, and the embedded chip pocket. Figure 5.18(d) shows the final assembled device, including the packaged embedded chip and the wire bonds. Due to the challenging assembly process of the 285 μm X 114μm sized die, the remains of the epoxy spread around the chip pocket, and the wires were not perfectly placed on the 50μm pads. This could lead to errors in the device's operation, especially at such high frequencies.

Figure 5.19 presents the fabricated Y-band source and its experimental setup. The

Table 5.3: List of the estimated system components' insertion loss for the proposed triplers

Components	**D-Band Tripler**	**Y-Band Tripler**
Input Circuitry	$0.88dB$	$1.13dB$
Output Circuitry	$0.34dB$	$1.05dB$
Wire Bonding	$1.24dB$	$1.77dB$
Probe Excitation	$0.59dB$	$0.74dB$
Diode Chip	$0.62dB$	$0.59dB$

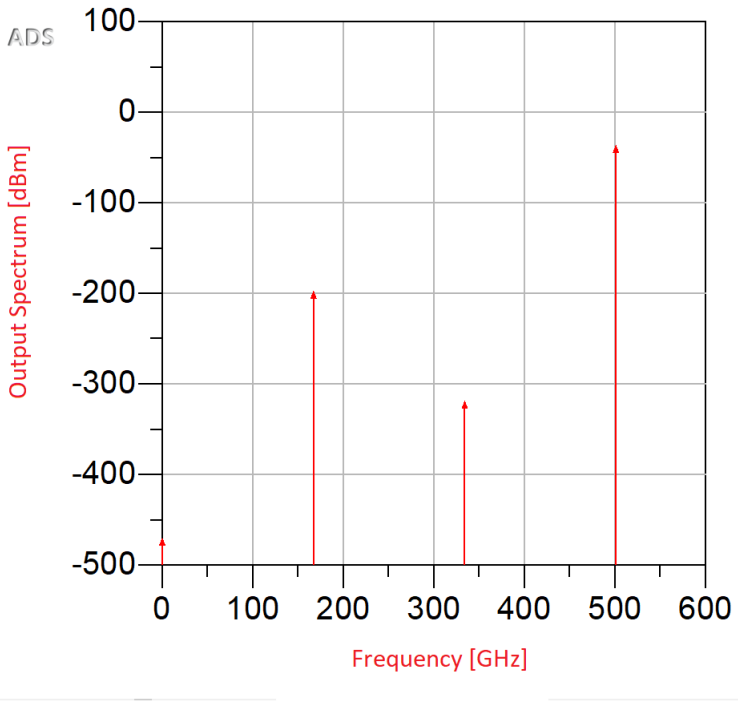


Figure 5.17: The simulated output harmonic level for the Y-band tripler at 500 GHz.

design includes an excitation V-band source of 12 dBm power, used in testing the previously discussed D-band tripler, contactless silicon probes at the V-band and Y-band, and a PM4

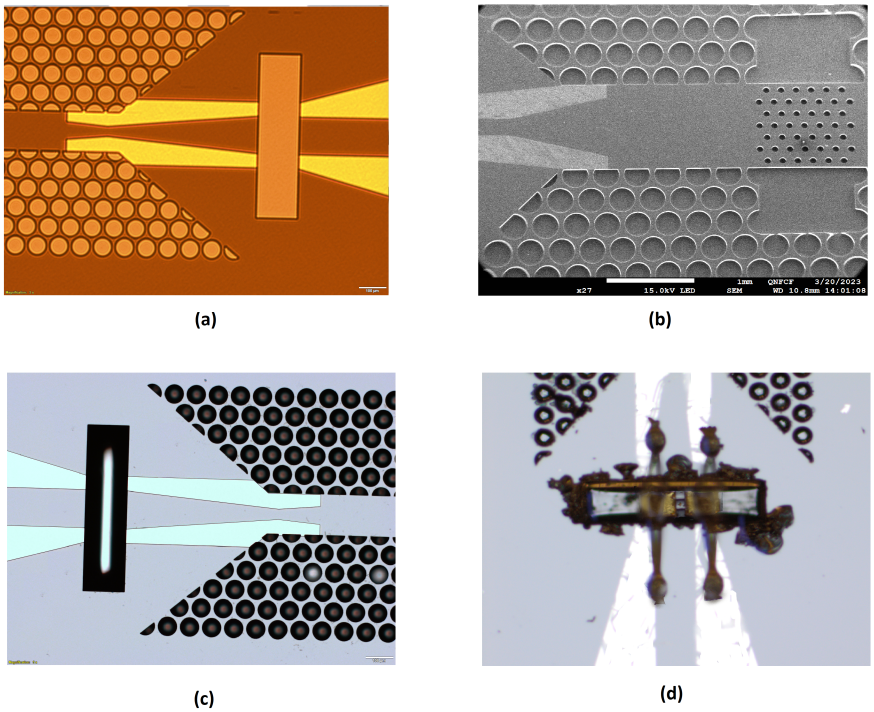


Figure 5.18: The fabricated and assembled Y-band tripler under microscopes at different stages.

power meter. The measured output power level couldn't be detected by the power meter. The sensitivity of the PM4 is $1\mu m$; this indicates that the output harmonic level is less than -30 dBm. This was expected since the simulated power level was -26.5 dBm and the causes of deviation from the measured device and the simulated model increase at high THz operation. Hence, it is necessary to make changes to the design structure to enhance the output harmonic level beyond the minimum detectable signal level offered by the PM4 power meter.

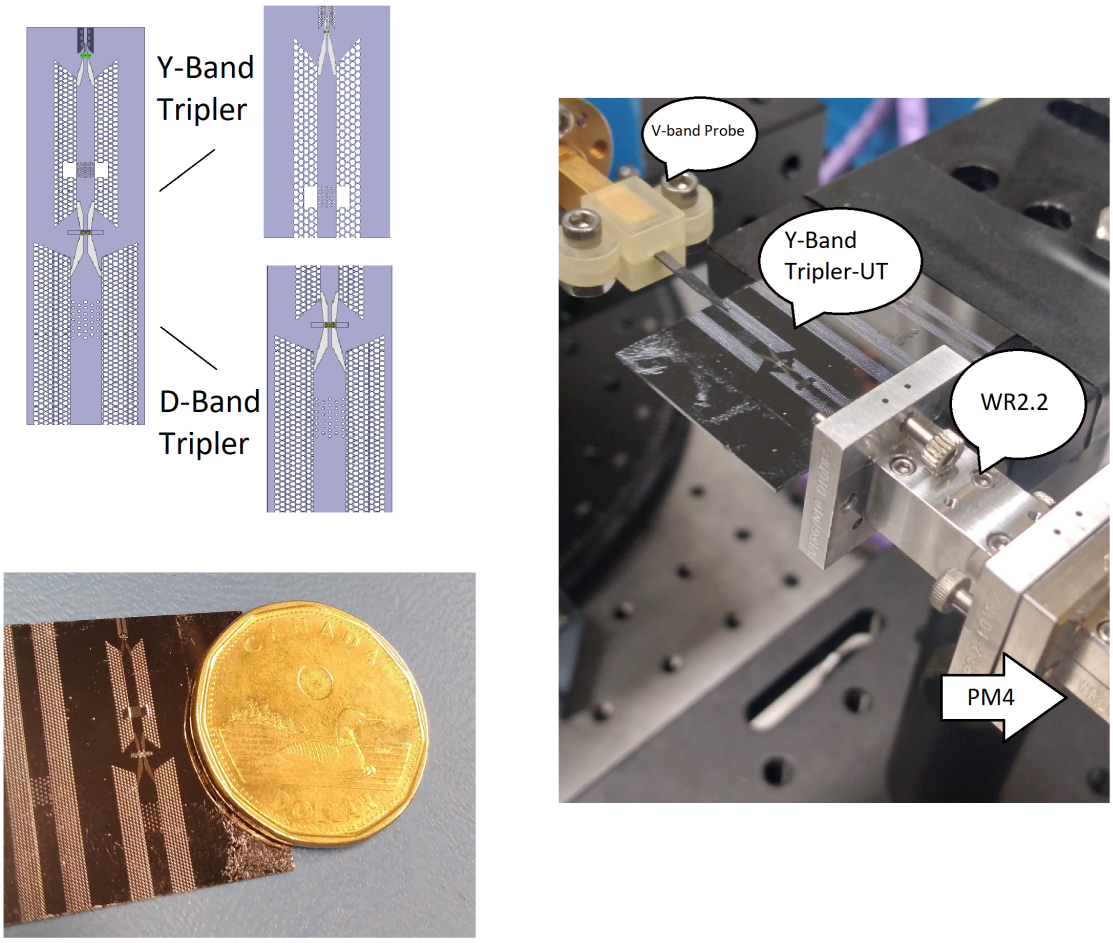


Figure 5.19: The fabricated Y-Band source and test setup.

5.3 Power Combined Y-Band EM-SSW THz Source

The objective is to increase the input power level for the second tripler stage. Increasing the input power to the diode significantly improves harmonic generation since we are operating in a bias-less topology. A power combining configuration is employed to roughly double

the input power applied to the initial tripler stage [76]. Figure 5.20 shows the schematic and the fabricated device of the Y-band power combined source. We must highlight that we have chosen the approach of consolidating the input power into a single pathway before directing it to the initial tripler stage. Another scheme could involve combining the output of two D-band tripler stages. However, this configuration would be beneficial for high-power operation as it enhances heat dissipation.

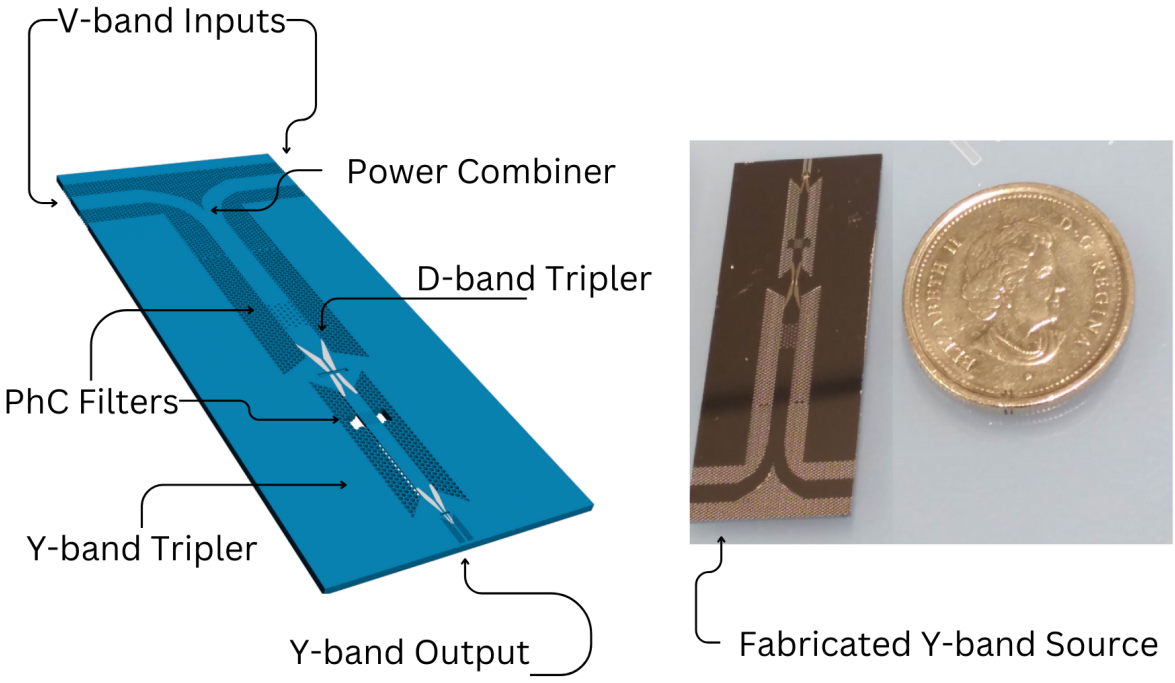


Figure 5.20: The power combined Y-band THz source.

The newly introduced EM-SSW T-junction maintains the same design as previously analyzed. The 3-Port S-matrix of the power combiner is calculated separately using Ansys

EM-simulator, as depicted in Figure 5.21. Next, the S-parameters are used in the ADS harmonic balance simulator to estimate the output harmonic level. The insertion loss for the outputs of the EM-SSW T-junction at 56 GHz is S_{21} and $S_{31} = 3.7dB$, and the return loss is less than -15 dB. The outcome of the harmonic balance analysis is shown in Figure 5.22. The conversion loss at 500 GHz is estimated to be $CL \approx 21dB$, which represents a significant improvement compared to the single-pumped THz source.

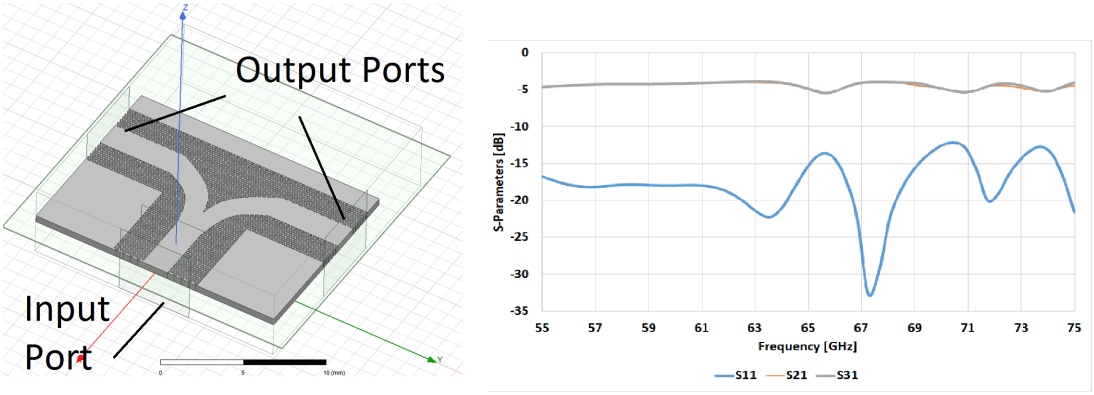


Figure 5.21: The S-parameters simulation for the EM-SSW T-junction.

The experimental setup for testing the power-combined Y-band THz source includes two V-band input signal generators connected to dielectric probes through WR15 connectors. Each generator produces an input power of approximately 12.5 dBm. The PM4 power meter, connected via a WR2.2 connector and using a Y-band contactless silicon probe, is used to measure the output. Figure 5.23 shows a picture of the setup, and the obtained data is presented in Figure 5.24. The PM4 power meter can detect the output power of the combined THz source in the Y-band. The maximum output power level is recorded to be $\approx -18dBm$ at $495GHz$, and the lowest detectable output signal is at $500GHz$ with

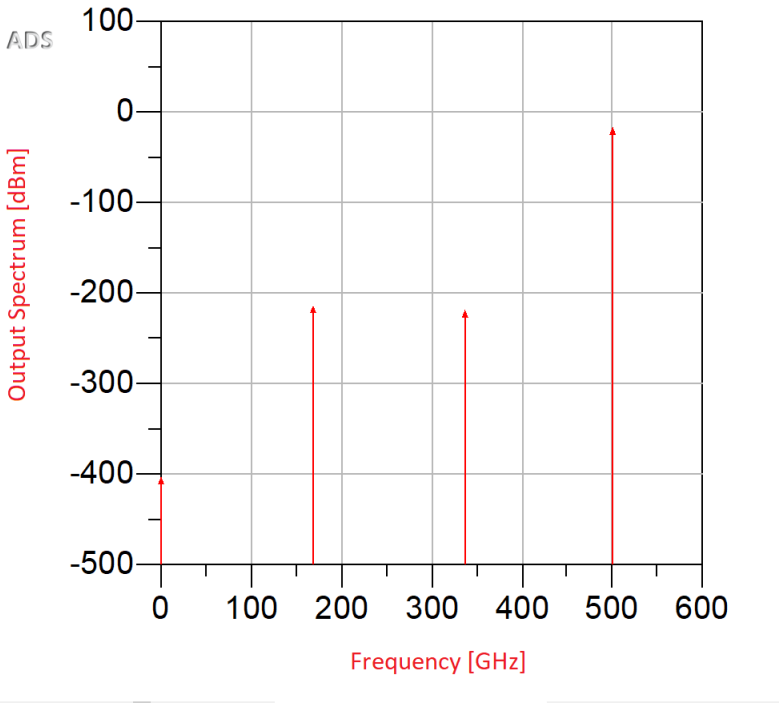


Figure 5.22: The simulated output harmonic level for the power combined Y-band source at 500 GHz.

$\approx -27dBm$. The overall maximum conversion loss of the system is $32dB$ at $495GHz$. This power level is significant for unbiased operation at the THz range despite the various non-deterministic practical factors introduced during the device fabrication processes.

Table 5.4 compares our work with related triplers in the literature. It is worth noting that the maximum overall conversion efficiency of the proposed D-band tripler is about 5%. When compared to unbiased triplers operating in the D-band, this conversion efficiency is considered high and demonstrates the excellent performance of the proposed integration technology. The work presented in [91] is the most similar in the literature in terms of source configuration and implementation. It utilized hybrid integration of unbiased GaAs

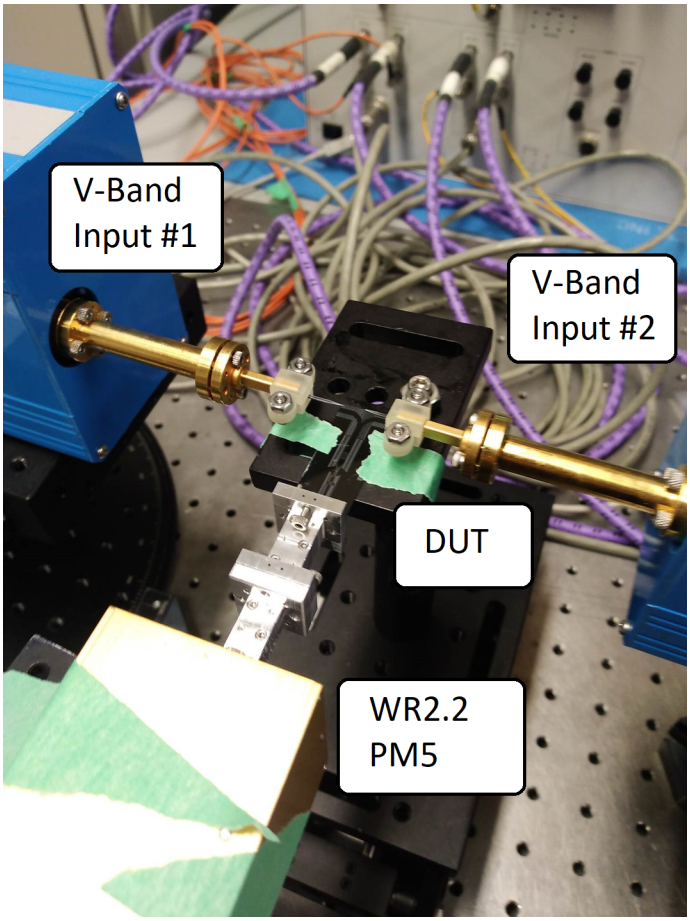


Figure 5.23: The test setup for the Y-band source.

diode chips on split-block metallic waveguide technology, using an input power of about 13 dBm. The design is based on coupled resonators to achieve matching to the diode's embedding impedance. The typical conversion efficiency is about 3.98%, demonstrating that our technology performs comparably to split-block waveguides. On the other hand, the conversion efficiency of our cascaded Y-band source is approximately 0.063 %, which is lower than triplers in the literature. However, most work at such high frequencies involves biased diode operation and much higher input power, making direct performance

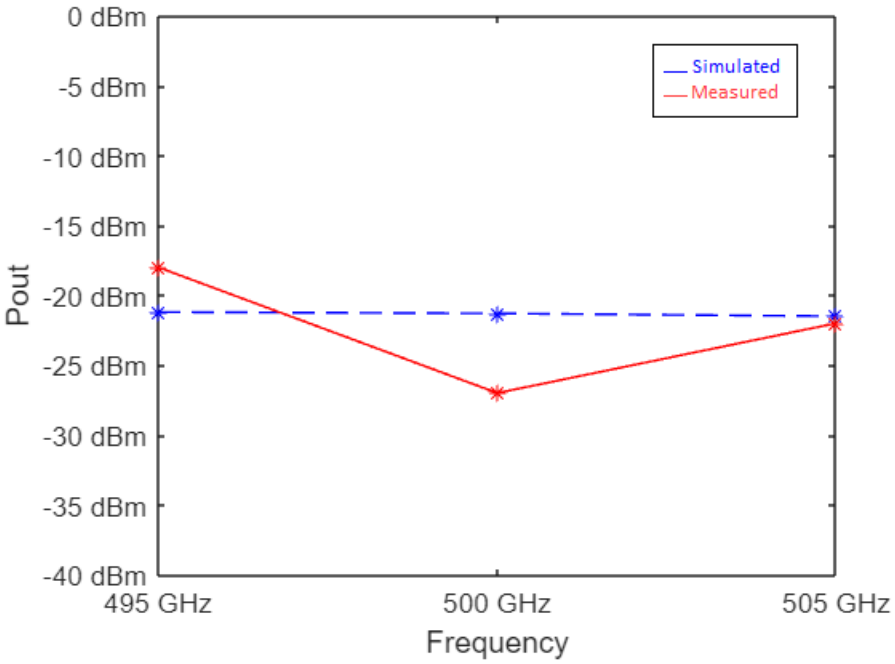


Figure 5.24: The simulated and measured output power for the power combined Y-band source.

comparison challenging. Moreover, the manual assembly of diodes and limitations in wire-bonding pad size introduced additional sources of degradation in our system. In summary, achieving such a power level using two cascaded unbiased triplers is considered satisfactory and underscores the potential of the proposed integration technology.

5.4 Summary

In this chapter, terahertz source prototypes were built based on the proposed EM-SSW technology. The objective was to develop functional prototypes with low power consump-

Table 5.4: Performance comparison of the proposed THz source with similar work in literature

Type	Study	Efficiency %	Frequency [GHz]
Tripler (Unbiased)	[99]	0.7–3.3	460–540
Tripler (Unbiased)	[100]	2-0.02	330–500
Tripler (Biased)	[101]	8-9	510-560
Tripler (Unbiased)	[91]	3.98	135-150
Tripler (Biased)	[102]	0.8–0.9	520–600
Tripler (Unbiased)	This Work	5.01	165-170
Triplers (Unbiased)	This Work	0.0631	495-505

tion using hybrid integration of GaAs Schottky Barrier Diode chips. Initially, we introduced the design process for the first stage D-band tripler, which involved EM-parasitic and non-linear diode models. We validated the tripler's operation through numerical simulations and discussed the device's fabrication. Experimental measurements of the D-band source exhibited promising results, demonstrating an output harmonic level with a conversion loss of 13 dB and paving the way for designing the subsequent tripler stage. The design procedure for the Y-band tripler followed a similar approach to the first stage. Although the simulations indicated successful operation, limitations in the measuring equipment prevented recording the output harmonic level. Consequently, a modified version of the THz source was developed, employing a power-combining topology at the input to enhance the power level at the first stage tripler. The measured data exhibited a system maximum conversion loss of 32 dB and generated a low-power signal at 495 GHz. These prototypes effectively demonstrated the functionality of the EM-SSW hybrid-integrated THz sources,

opening up opportunities for further investigation utilizing the same technology.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

Terahertz (THz) electronics are gaining more attention due to their expanding applications and distinctive advantages. With the advancement of millimeter-wave research and the evolution of 5G communication systems, the prospect of commercializing 6G communication systems hinges on addressing low-THz frequencies. The goal of this Ph.D. research is to devise solutions for integrating THz systems using a low-loss, compact, and cost-effective technology, employing hybrid off-chip integration. This work focuses on integrating frequency multiplier-based THz sources, utilizing GaAs Schottky diodes as an example to assess the performance of the proposed approach.

Firstly, Chapter 3 introduces the *Effective Medium-Suspended Silicon Waveguide (EM-SSW)*. This structure combines the advantages of suspended dielectric waveguides and EM

waveguides, providing efficient isolation of the guiding channel from the cladding and the handle structures. The design demonstrates a remarkably low attenuation constant for frequencies up to 0.5 THz. Additionally, the suspended channel enables the planarization of different frequency operating waveguides on a single level, offering multi-band integration. Our proposed EM-SSW technology is based on photonic crystal-like (PhC) EM structures. We conducted a simulation-based modal analysis to study guided operation conditions and limitations, examining the required permittivity contrast between the core and EM cladding at various filling factors. Using 3D full-wave finite element analysis (FEA), we optimized the structure's modal transmission by evaluating different filling factors. Subsequently, we fabricated V-band and D-band waveguides based on the presented studies, measuring the scattering parameters and attenuation constant using a 2-port network analysis. The experimental results closely matched the simulated outcomes, highlighting the potential of our proposed technology for multi-band single-wafer THz integration. Comprehensive discussions were held regarding the fabrication process, including the three-mask steps for constructing the THz platform and the potential for operation beyond 1 THz.

Next, chapter 4 focused on the silicon probe technology utilized in all THz measurements, introducing a novel contactless excitation technique compatible with various widely used commercial technologies. We presented a low-cost and easily set-up coplanar waveguide (CPW) excitation method using a micro-machined dielectric waveguide probe for the V frequency band. The transition design was fabricated using laser machining, and the board was tested with a Vector Network Analyzer (VNA) connected to the dielectric probes via metallic waveguides. The experimental results demonstrated agreement with the Finite Element Method (FEM) simulations. Furthermore, we introduced two contactless silicon

waveguide probe methods for exciting Microstrip lines (MSL). The first method involved the differential mode excitation of two MSLs, while the second method utilized a 180-degree bend combiner to excite a single MSL. These designs were simulated, fabricated, and measured, yielding promising results that showcased the successful coupling of the dielectric waveguide (DWG) mode into the MSL modes. This approach provided a cost-effective solution for chip prototyping and debugging, with the potential for utilization at higher frequencies, including the THz range. Additionally, we proposed a packaging design for electronic-photonic integrated circuits (EPICs), employing embedded chip ultra-short wire bonding to minimize parasitic effects and enable high-speed data communication with RF signals up to 75 GHz. The design's validity was confirmed by dummy chip fabrication and measurements using contactless silicon probes, which exhibited close agreement with the simulated results. The proposed packaging design proved effective, achieving an insertion loss of less than 3.5 dB and a return loss of less than -12 dB. This capability enables the operation of high-performance EPICs, suitable for diverse applications, with the potential for utilization at frequencies exceeding 100 GHz. Lastly, we introduced an enhanced version of the silicon probes designed for power excitation in the D-band and Y-band. The modified probe designs were successfully simulated and measured, validating their operational concept. The results highlighted their potential in THz probing applications, demonstrating excellent power excitation, specifically in the D-band and Y-band.

Finally, utilizing all-silicon multi-band EM-SSW hybrid technology, we investigated the integration of THz sources to develop energy-efficient prototypes. We presented a design for frequency multiplier THz sources based on planar GaAs Schottky diodes, utilizing the technology introduced in Chapter 3. The design incorporates the hybrid integration of

GaAs Schottky diodes using embedded chip packaging with ultra-short wire bonding, as explained at the end of Chapter 4. The proposed THz sources consist of multiple stages. First, we introduce a single-stage frequency tripler operating at the V-band (56 GHz), which generates a third-harmonic output signal at the D-band. We provide details on the circuit components, system design methodology, and analysis of the fabricated tripler prototype. These components include PhC-based filters, low-loss modal transitions from DWG to metallic contact pads, and impedance-matching sections. Moreover, we propose a prototype for the second-stage tripler operating in the D-band, producing a third-harmonic output signal at 500 GHz. Analogous to the first stage, we discuss the circuit components and provide a system analysis. We also describe the experimental setup for measuring the output of both prototypes using contactless silicon probes. Promising results were obtained for the D-band tripler, showcasing an output harmonic level with a 13 dB conversion loss and setting the stage for subsequent tripler design. The Y-band tripler followed a similar procedure, yielding successful simulations despite limitations in the measuring equipment. To overcome this, a modified THz source was created using power combining topology to enhance input power to the first tripler stage. Experimental data revealed a system conversion loss of up to 32 dB, generating a low-power signal at 495 GHz. These prototypes effectively demonstrated the potential of EM-SSW hybrid-integrated THz sources.

6.2 Future Research Directions

This Ph.D. research can be extended in several directions by enhancing open challenges. These enhancements can be summarized as follows:

- The proposed EM-SSW multi-band frequency technology in Chapter 3 covers single-wafer operation from the mmW frequency range up to the Y-band. The measured results were promising and paved the way for operation beyond 1 THz. However, extending the operation will require the introduction of more lithography masks to pattern the small features. More research is needed to investigate the fabrication process to include such extensive features for low-frequency bands and those at high THz bands. We have investigated novel concepts to address this issue, assisted by simulation analysis. For example, we introduced the idea of bonding two differently sized wafers for low and high-frequency band operation, and the preliminary simulations showed promising results. The transitions between the different levels of such a wafer-bonded method can be implemented using all-silicon vertical vias.

- Despite the excellent results obtained from the embedded chip packaging technique covered in Chapter 4, a more sophisticated method could enhance performance by utilizing Flip-chip technologies on the on-silicon metallic pads. This could allow for shorter metallic interconnects and increase the overall system efficiency.

- One of the advantages of the proposed EM-SSW technology is its high performance using all-silicon waveguides. This feature could be implemented with wafer MMIC diodes instead of hybrid chip integration for readily packaged GaAs diodes. Although this approach could pose challenges regarding cost and fabrication complexity, achieving such integration will potentially boost performance to a significant level.

- Enhancing the operation beyond the unbiased topology can enhance the conversion efficiency of the triplers, as proposed in Chapter 5, by introducing biasing circuitry

and more sophisticated topologies, including additional diode connections. Furthermore, employing a higher input power source can generate higher harmonics, aided by a power-combining topology. Additionally, biasing can significantly amplify the output THz power at higher frequencies, providing more possibilities for cascading more tripler stages to operate beyond 1 THz

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Appendix A

ADS Harmonic Balance Simulation and Fabricated Layouts

Figure A.1 presents a screenshot of the harmonic balance analysis performed in Keysight's ADS for the power-combined Y-band tripler. The figure consists of cascaded blocks for the S-parameters of the system's input and output passive networks connected to the diode's nonlinear model. The S-matrices are extracted by EM simulation using Ansys HFSS for the following circuits:

- The V-band probe with the input WR15 metallic waveguide and the output EM-SSW V-band waveguide.
- The V-band EM-SSW T-junction power combiner.
- The input circuitry for both tripler stages including the PhC-PBG filters and DWG to CPS transitions.

- The output circuitry for both tripler stages including DWG/CPS transitions.
- 4-port networks for both SBDs including the parasitic models and attached to the diodes nonlinear models.
- The Y-band probe with the output WR2.2 metallic waveguide and the output EM-SSW Y-band waveguide.

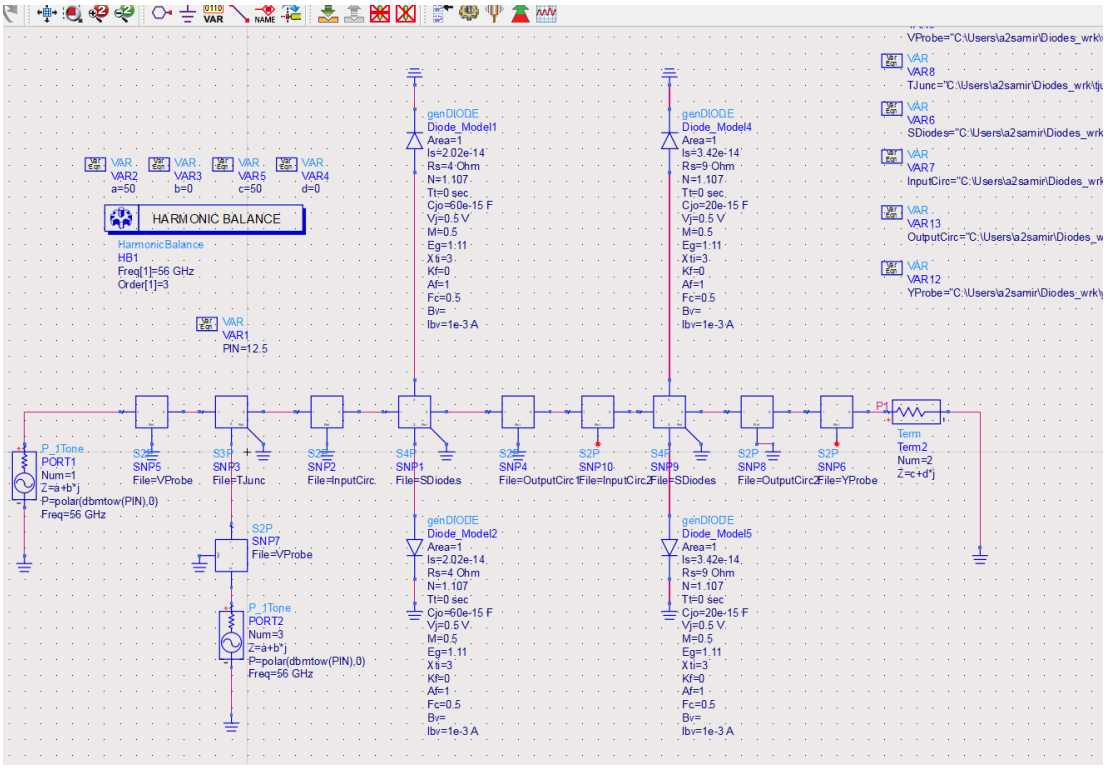


Figure A.1: Harmonic balance simulation in ADS for the power combined Y-Band tripler.

Figure A.2 shows the layout of the masks used in the fabrication process of the EM-SSW all-silicon technology for the tripler devices. The masks include three layers for each version used in the rapid prototyping process. The layers are for patterning the Aluminum

layer, front silicon DRIE, and back-side silicon DRIE. The layout is created by K-layout software.

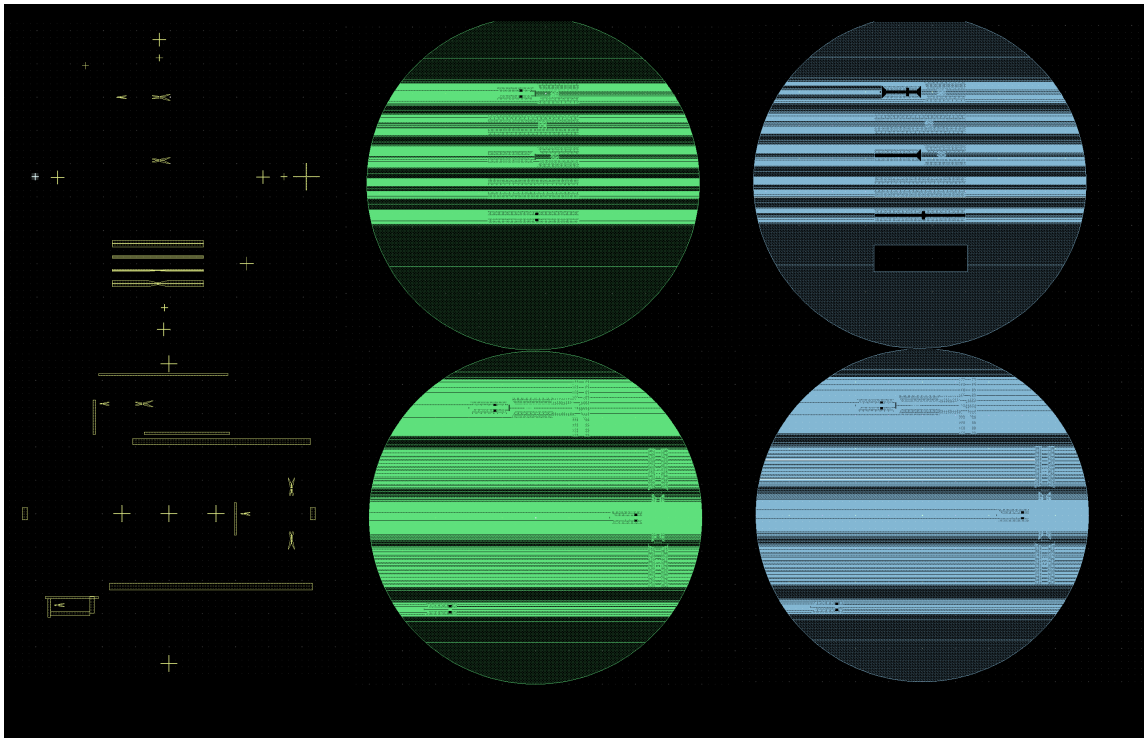


Figure A.2: The masks used in the fabrication of all devices in the proposed research.