Reconfigurable Microwave/Millimeter-Wave Devices Using Liquid Crystal Technology

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

In recent years, microwave liquid crystal (LC) technology has attracted significant attention from researchers due to its tunability and low-loss characteristics, extending up to terahertz frequencies. However, existing state-of-the-art LC-based devices face limitations in fabrication processes, resulting in relatively large sizes compared to other available tunable technologies. This thesis seeks to address this challenge by proposing a fabrication process for chip-scale and miniaturized LC-integrated devices. To achieve this goal, an alignment method is adopted for silicon micromachined devices, along with a comprehensive fabrication process for chip capacitors, reflective loads, and reflective-type phase shifters. Additionally, a tunable waveguide filter is designed and fabricated based on a control mechanism using a static magnetic field.

The design and fabrication of silicon-micromachined variable capacitors are presented, utilizing nematic LC technology: shunt and series capacitors with and without integrated bias lines. The LC material enables electronic control over its dielectric properties, offering versatility across a broad spectrum of RF reconfigurable applications that require analog tuning. Measurement and simulation results for the chip LC shunt variable capacitor reveal a measured quality factor ranging from 44 to 123 at 1 GHz. With a biasing control voltage from 0 V to 40 V, the fabricated micromachined capacitor demonstrates an 18% capacitance shift. The LC-based series capacitor, demonstrated with an integrated bias line, isolates voltage control from RF terminals, serving a pivotal role in devices where series capacitors are essential. With a 21% shift in capacitance and a quality factor of up to 45 at 1 GHz, the capacitor's performance is evaluated comprehensively through measurement and simulation. LC-integrated series capacitors tailored for applications without isolating bias voltage from RF terminals are demonstrated, yielding a notable 24% shift in capacitance and achieving a quality factor of up to 105 at 1 GHz. The demonstrated series capacitors feature a 10 µm thin layer of LC material, contributing to lower control voltage requirements and faster response times. These devices are manufactured through an in-house multi-layer microfabrication process.

The thesis introduces a tunable waveguide filter that integrates LC material within quartz glass tubes, actuated by a static magnetic field. This innovative filter demonstrates a 7% tuning range with minimal bandwidth variation. Experimental validation for a 7.5 GHz filter with a 2.5% bandwidth confirms the concept's viability. The quality factor of this filter varies between 108 and 288 in the fabricated sample. Tuning of the filter is first demonstrated using both a pair of rotating magnets; then, a pair of coil magnets is used to eliminate moving parts.

Finally, two monolithically integrated reflective loads and two reflective-type phase shifters are presented, employing LC material as a reconfigurable element. The LC material is confined within a micromachined space, and its dielectric properties are controlled through an applied bias voltage. The tunable reflective loads find applicability in RTPSs. Operating at frequencies of 28 GHz and 62 GHz, the reflective loads exhibit phase variations of 113° and 118°, respectively, as the bias voltage ranges from 0 V to 25 V. The 28 GHz and 62 GHz devices demonstrate reflective insertion losses of 3.9 dB and 4.3 dB, respectively, indicating figures of merit of 29°/dB and 27.5°/dB, respectively. Employing tandem hybrids at the operating frequency alongside two identical reflective loads has led to two reflective-type phase shifters at 28 GHz and 62 GHz. While the phase shift remains the same as the corresponding reflective loads, the insertion loss increases due to the use of hybrids. The insertion loss is measured at 5.95 dB and 7 dB for the 28 GHz and 62 GHz samples, respectively. Fabrication of these devices is conducted in-house using a multi-layer microfabrication process. To the best of our knowledge, this marks the first time a fully silicon-made, chip-level LC integrated reflective load and RTPS phase shifter is presented.

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Dedication

To my beloved parents

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List of Abbreviations

3D 3-Dimensional xiii–xvii, 13, 32, 33, 39, 40, 43, 48, 51, 58, 59, 73, 79, 81, 82, 86, 87

5G Fifth Generation 1, 2, 66, 92

AFM Atomic Force Microscope xiii, 28, 29

BiCMOS Bipolar CMOS 2

BST Barium Strontium Titanate 2, 5, 6, 30, 56

CMOS Complementary Metal-Oxide Semiconductor 2

CPW CoPlanar Waveguide xvii, 32, 50, 69, 71, 79–83, 86, 94, 95

CPWG CoPlanar Waveguide with Ground 12

CRLH Composite Right/Left Hand 1, 7, 8, 16

DC Direct Current 30, 31, 42, 45, 53, 93, 94

DRIE Deep Reactive Ion Etching xiii, xiv, xvi, 33, 34, 39–41, 49, 53, 71, 72

DSE Dispersion Sensitivity Enhancement 7

EM ElectroMagnetic 51

FOM Figure of Merit 68, 74, 75, 77, 86, 90, 91, 93

FSS Frequency Selective Surface 94

GaN Gallium Nitride 78

GeTe Germanium Telluride 78

GSG Ground-Signal-Ground 45, 76, 82, 85, 86, 88

HMCSIW Half-Mode Corrugated Substrate Integrated Waveguide 15

IBFD In-Band Full-Duplex 1

IBI Ion Beam Irradiation xiii, 23, 25, 26, 29, 31, 34, 42, 53, 68, 71

LTCC Low-Temperature Co-fired Ceramic 12

LWA Leaky-Wave Antenna 1, 7, 8, 16

MEMS Micro-ElectroMechanical System 2, 5, 30, 56, 67, 78, 90

mm-Wave Millimeter Wave xix, 1–4, 7, 9, 16, 19, 66, 67, 78, 79, 91–95

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor 78

PA PolyAmide 19, 23, 26, 35

PCB Printed Circuit Board 11

PCM Phase Change Material 2, 5, 30, 67, 78

PECVD Plasma-Enhanced Chemical Vapor Deposition xvi, 25, 71, 72, 85

PI PolyImide xiii, xiv, xvi, 15, 16, 19–21, 23–26, 28, 34, 35, 45, 49, 50, 71, 72

PIN Positive-Intrinsic-Negative 5, 56

PR PhotoResist xiii, xiv, xvi, 33, 34, 41, 42, 49, 71, 72

PVA PolyVinyl Alcohol 7–9

RF Radio Frequency 2, 3, 5, 17, 30, 32, 33, 36, 38, 39, 45, 47, 54, 55, 67, 92

RTPS Reflective Type Phase Shifter xvii, 4, 68, 69, 71, 77, 78, 82–91, 93

SIW Substrate Integrated Waveguide 10, 11, 24

SMA SubMiniature version A 59

SPDT Single Pole Double Throw 12

UV UltraViolet 36

VNA Vector Network Analyzer 53, 76

Chapter 1

Introduction

The expansion of wireless communication systems has experienced remarkable growth over the past few decades. Microwave devices and antennas, crucial components of communication system front-ends, significantly influence the definition of system specifications, performance metrics, and limitations. The rise of technologies like Fifth Generation (5G) requires features such as beam steering and In-Band Full-Duplex (IBFD) transceivers in the mm-Wave frequency band. Beam steering can be achieved through the mechanical movement of the antenna; however, this proves impractical for high-frequency 5G networks. The prevalent approach involves utilizing a phased array antenna, necessitating the integration of phase shifters. Alternatively, reconfigurable Composite Right/Left Hand (CRLH) Leaky-Wave Antenna (LWA)s stand out as potential candidates. The 5G communications network operates across diverse frequency bands, necessitating the deployment of frequency-reconfigurable filters and tunable impedance matching networks.

1.1 Motivation

In recent years, significant progress has been made in the development of satellite and 5G communication systems and their architectures, prioritizing high capacity, reliability, expanded coverage, efficient spectrum utilization, and high data rates with minimal latency. Among these advancements, a key driver is the demand for higher data rates to accommodate a growing number of users within the network. Consequently, there has been an increased utilization of multiple frequency bands, driving the adoption of mm-Wave ranges where substantial unused spectrum is available.

While satellite communication relies on high-gain parabolic reflector antennas due to the long distances and fixed link direction, short-range communication applications like 5G, which involve moving users, present a challenge for such solutions. In these scenarios, antennas must be dynamically steered to provide network coverage as users change position. Therefore, a more efficient solution lies in the use of phased array antenna systems, where the beam direction can be steered by controlling the signals delivered to the array elements. However, implementing smart antennas in the mm-Wave range can be challenging and complex. Currently, various approaches aim to introduce cost-effective and low-profile beam steering antennas with the assistance of emerging technologies.

In addition to beam steering antennas, achieving optimal performance and addressing other challenges in communication systems require each device to avoid interference and select the best modulation and operating frequency. However, these maneuvers necessitate reconfigurable components in the Radio Frequency (RF) frontend, including tunable filters, phase shifters, and adaptive impedance tuners. These reconfigurable components can be realized using different materials and technologies that fall into three main categories: semiconductor technologies such as Complementary Metal-Oxide Semiconductor (CMOS) and Bipolar CMOS (BiCMOS), which offer suitable performance at an acceptable cost; Micro-ElectroMechanical System (MEMS) technology, known for its high performance across a broad range of frequencies; and functional materials such as Phase Change Material (PCM), Barium Strontium Titanate (BST), and microwave Liquid Crystal technology.

While semiconductor technology offers highly miniaturized devices in the form of integrated circuits with fast response times, they suffer from considerable loss at high frequencies and limited linearity. PCM and MEMS-based devices provide improvements in linearity and high-frequency performance; however, they offer only a limited number of states of control over their tuning range, which reduces their maximum practical performance. While BSTs offer a good range of tuning, they suffer from considerable loss at high frequencies. LC materials, on the other hand, provide high linearity, good power handling, and low-loss characteristics while offering analog tuning capability.

Since the introduction of the first LC material specifically developed for microwave applications in 2002, numerous innovative designs have introduced a wide range of high-performance LC-integrated components for RF and microwave applications. These include planar devices such as filters, antennas, and delay lines, as well as dielectric and metallic waveguide phase shifters, tunable resonators and filters, tunable metamaterial structures and frequency-selective surfaces, and reconfigurable beam steering antennas. However, many state-of-the-art LC-based devices are relatively large in size due to limitations in the processes required for their fabrication. One of the most crucial processes for planar devices is the treatment of the pre-alignment surface, traditionally done using a rubbing

machine. This limitation restricts the structure and dimensions of the proposed devices. Consequently, most currently available LC-integrated devices are not suitable for integration with other RF frontend components due to these issues.

1.2 Objectives

This research primarily aims to address the limitations associated with fabricating small and miniaturized LC-based devices. It specifically focuses on utilizing silicon microfabrication processes, which can streamline the integration of proposed devices with existing RF and mm-Wave devices like phased array systems. By reducing size and dimensions, the proposed devices hold the potential for significant miniaturization. Thinner LC material in planar devices is anticipated to contribute to faster response times, depending on material type and biasing voltage. The summarized objectives of this research regarding miniaturized RF and mm-Wave devices are as follows:

1. Introduction of an adopted pre-alignment surface treatment method
2. Complete fabrication process for silicon micromachined devices
3. Analog tunable LC-based capacitors
4. mm-Wave tunable reflective loads
5. mm-Wave phase shifters

Moreover, the utilization of a static magnetic field for tuning purposes is constrained in much of the existing research. This work stands out by presenting an LC-based tunable metallic waveguide filter that is reconfigured solely through the application of a magnetic field.

1.3 Thesis Organization

This thesis commences with a survey of previous works in which LC materials have been utilized, outlined in Chapter 2. This chapter presents state-of-the-art examples of both LC-based antennas and microwave devices, concluding with a summary of available publications and their limitations.Chapter 3 introduces LC materials in tunable microwave

devices, starting with an explanation of their operational principles. Various alignment methods for LC materials and their respective use cases are detailed. At the chapter's conclusion, the adopted pre-alignment treatment method, compatible with small, multi-surface, and microfabricated devices, is explained.

Chapter 4 delves into LC-integrated chip capacitors, comprising three different types: shunt capacitors, series capacitors with integrated bias lines, and series capacitors. Each capacitor type is explored in detail, covering design, fabrication, simulation, measurement results, and summarization. In Chapter 5, an LC-integrated metal waveguide filter operating in the C band is presented. This filter is tuned using a static magnetic field, and the chapter provides insights into its design, simulation, and measurement.

Chapter 6 focuses on LC-based mm-Wave tunable reflective loads operating at 28 GHz and 62 GHz, followed by two RTPS at those frequencies. The chapter elaborates on the design of each reflective load and RTPS, along with the hybrid coupler. Simulation and measurement results for these devices are presented in each section.

Finally, Chapter 7 concludes the thesis with an overview of future work and contributions provided by this research. A list of references is provided later in the manuscript.

Chapter 2

Survey of Previous Works Using Liquid Crystal Materials

Tunable devices play a crucial role in modern RF and microwave systems, including cognitive and software-defined radios. Meeting the demands of today's communication systems, such as efficient spectrum usage, smart antenna solutions, and cost reduction, necessitates the use of tunable devices. Tunable filters [10, 11, 12, 13] enhance spectrum usage efficiency by enabling the reconfiguration of communication systems, while low-loss phase shifters and impedance tuners facilitate phased array antenna solutions [14, 15, 16]. The variable capacitor serves as a fundamental component of most microwave devices, making the development of high-quality factor variable capacitors essential for the advancement of efficient and advanced communication systems. Various technologies, such as MEMS, semiconductors, BST, Positive-Intrinsic-Negative (PIN) diodes, PCM, graphene, and LC materials, can be employed to achieve tunability.

MEMS-based devices [17, 18, 19, 20, 21] and PCM-based devices [22, 23, 24, 25, 26] are commonly utilized for fabricating switched capacitors. These technologies offer advantages such as a small footprint and low insertion loss. However, they have limitations in discrete tuning capabilities, fabrication cost, lifetime, and reliability. Diodes offer fast switching times but suffer from increased loss at higher frequencies, limiting their usage in mm-Wave applications [27, 28]. Semiconductor analog and switched capacitors have potential for mm-Wave frequencies [29, 30, 31], but they encounter challenges such as poor linearity, low quality factor, and high power consumption. Although BST-based devices offer higher power handling, lower loss, and better linearity, their complex fabrication process and lossy behavior at higher frequencies are considered disadvantages [32, 33, 34, 35]. Liquid crystals [36, 37] and graphene [38, 39, 40, 41] have demonstrated promising performance overall.

Microwave liquid crystals with a low loss tangent at high frequencies have the potential to mitigate issues related to linearity, reliability, loss, power consumption, and lifetime through continuous tuning [42, 43]. All planar LC-based devices exhibit nearly zero power consumption since bias voltage is solely required to generate a static electric field. Recent studies indicate that certain LC materials can sustain their performance up to the W band and THz [44, 45]. Nevertheless, LC-based tunable devices represent an attractive research area, as evidenced by numerous publications in recent years [46, 47, 48]. Notably, publications in this area often offer comprehensive explorations due to the growing interest in LC-based technologies. Devices in these studies tend to be relatively bulky due to limitations in fabrication and packaging. Depending on the application, these materials can facilitate changes in operating frequency, antenna beam direction, load impedance, filter bandwidth, and phase shift. This section will explore several state-of-the-art LC-integrated antennas, focusing on their diverse functionalities in microwave and mm-Wave applications.

Table 2.1: Comparison of continuous tunable technologies available for microwave and millimeter wave applications.

Feature	Semiconductor	BST	LC
Size	Small	Medium	Large
Tunability	High	Medium	Low
Tuning Speed	Fast	Fast	Slow
Fabrication Complexity	High	High	Moderate
Fabrication cost	High	Moderate	Moderate
Frequency Range	Microwave	Microwave	Microwave/mm-Wave
Quality Factor	Low	Medium	High
Linearity	Very Low	Moderate	High
Power Handling	Low	High	High
Power Usage	Moderate	Low	Negligible

Table 2.1 provides a comparative summary of continuous tuning technologies. While LC materials exhibit inherent limitations in tuning range and speed due to their molecular physics, LC-integrated devices remain larger than those based on BST or semiconductor technologies. However, despite similar fabrication complexity and costs, microwave LC materials offer several advantages, including superior linearity, power handling, and reduced power consumption. Importantly, as discussed earlier, the loss tangent of microwave LC materials remains stable at higher frequencies, leading to improved quality factors, especially at millimeter-wave frequencies.

2.1 Tunable LC-Based Antennas

LC materials hold the potential to function as tunable mediums in microwave and mm-Wave antennas, facilitating their reconfiguration. Depending on the application, these materials can be employed to adjust the operating frequency, beam direction, or both simultaneously. This section will delve into several state-of-the-art LC-integrated antennas, highlighting their diverse functionalities.

Composite right/left-hand leaky wave antennas exhibit frequency-based beam steering, where the main beam rotates over the working frequency band. Nonetheless, the incorporation of LC materials empowers CRLH LWAs to achieve beam steering at a fixed frequency [49, 2].

In reference [1], a CRLH metamaterial is fabricated on Rogers RO4350B substrate, characterized by a relative permittivity of 3.48, a thickness of 0.762 mm, and a loss tangent of 0.004. The antenna radiators are printed on identical substrate material, excluding the ground, and are positioned above a CRLH structure. Within the two layers of RO4350B, the LC material is introduced and sealed (utilizing a sticky film) at a height of 0.25 mm. Both the top and bottom structures undergo coating with PolyVinyl Alcohol (PVA), followed by rubbing to facilitate pre-alignment along the y-direction. The LC material CDZL-016, supplied by LuQuan Company Ltd, possesses a relative permittivity ranging from 2.7 to 3.25. The 3D structure with multiple layers is depicted in Figure 2.1a.

The biasing network, as depicted in Figure 2.1b, is designed to convey the applied voltage to the radiator pads, which function as electrodes in this configuration. Variations in the biasing voltage induce a shift in the dispersion diagram, consequently causing the antenna beam to steer. The corresponding dispersion diagram shift is illustrated in Figure 2.1c. It is noteworthy that the application of bias voltage results in a leftward shift of the dispersion diagram. A frequency beam scanning capability of 115° was successfully achieved within the frequency range of 11.8 GHz to 12.9 GHz. Specifically, at 12.4 GHz, the adjustment of bias voltage effectively steers the beam direction, resulting in a maximum scanning range of 35°.

An additional instance of the CRLH leaky-wave antenna is presented in reference [3]. This implementation utilizes a planar structure situated above an LC layer, with Rogers RO4350B serving as the substrate material. CRLH and Dispersion Sensitivity Enhancement (DSE) units are printed on one side, with the feeding transmission line located on the opposite side. The LC material employed is of CDZSL-018 type, featuring a thickness of 0.25 mm, a relative permittivity ranging from 2.46 to 2.95, and a loss tangent of 0.037. Nevertheless, as they did not incorporate multiple electrode configurations, pre-alignment

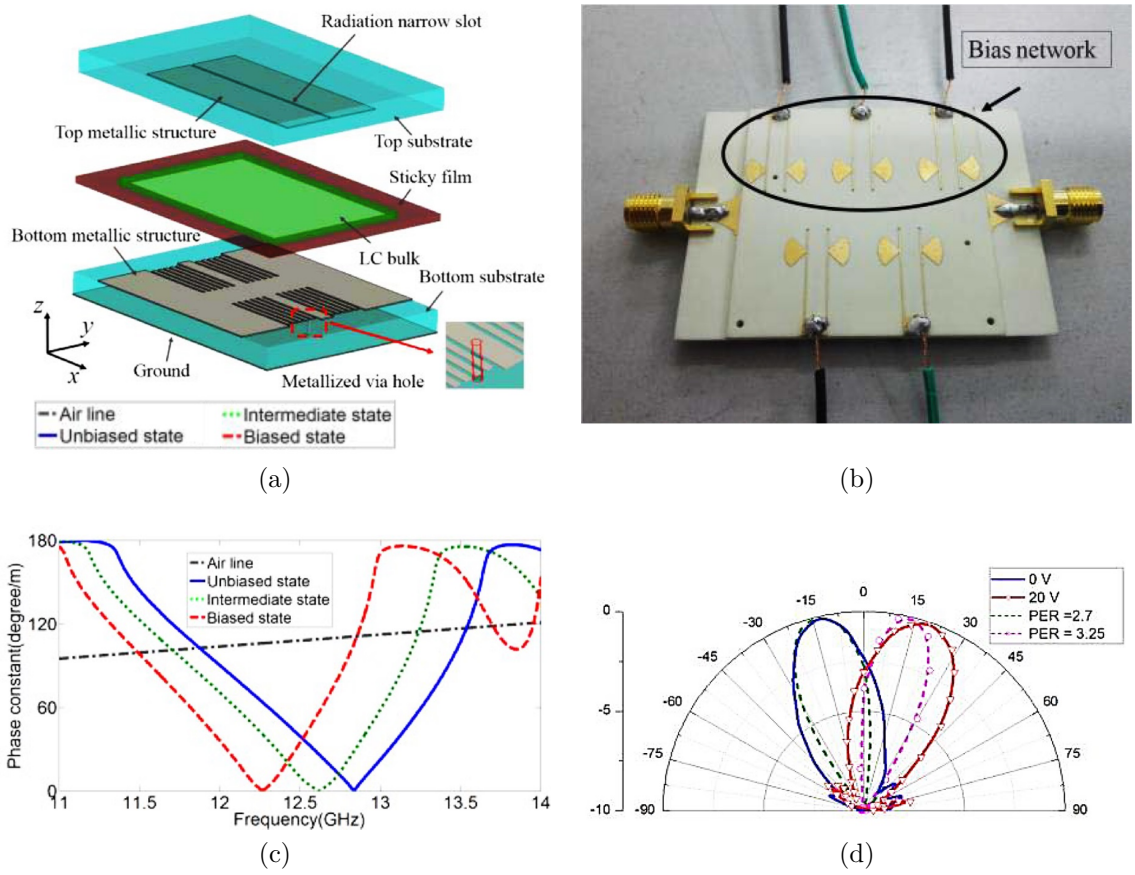
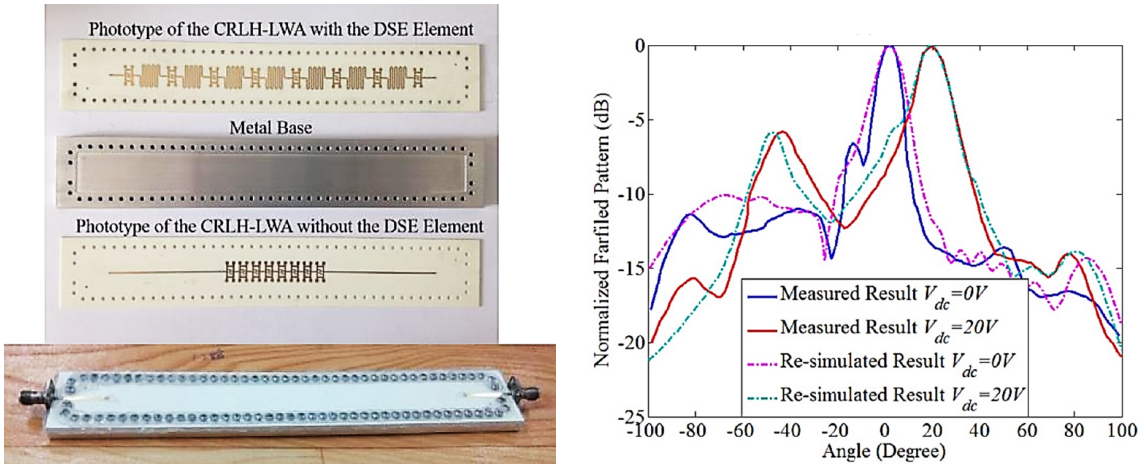


Figure 2.1: (a) 3D layer view of CRLH unit, (b) fabricated antenna with biasing network, (c) dispersion diagram under different biasing voltage (min, intermediate, and max permittivity), and (d) fixed frequency beam scanning performance at 12.4. [1].

was necessary. This was achieved by applying PVA on the printed layout and ground plate, followed by rubbing to align the LC material in the y-direction. Figure 2.2a depicts both the individual layers and the fully assembled fabricated sample.

To facilitate the injection of LC material, two holes were strategically designed, and the material was introduced after securely tightening all screws. The observed radiation pattern results demonstrate a 20° beam scanning capability achieved by modulating the bias voltage within the range of 0 V to 20 V as shown in Figure 2.2b.

Leveraging LC material in antenna designs extends beyond the confines of the CRLH LWA antenna, as planar array antennas also exhibit tunable characteristics. Figure 2.3a



(a) (b)

Figure 2.2: Tunable CRLH leaky-wave antenna: (a) fabricated antenna (with and without DSE) and (b) radiation pattern results [2].

illustrates both the top and cross-sectional views of the proposed array antenna, detailed in [3], operating at 12.5 GHz. The substrate employed is Rogers RO4350B with a thickness of 0.762 mm. The LC material utilized is CDZSL-014, supplied by BAYI Space LCD, featuring a relative permittivity ranging from 2.54 to 3.15 and a loss tangent of 0.015. A 0.25 mm cavity is precision-milled into the ground plate, designed to accommodate inserted dielectric slabs (refer to Figure 2.3b). The antenna's input and output ports are printed on the rear side of the substrate and connected to the antenna layout through vias. Positioned between every two patches is a phase shifter, adjusting the phase shift through variations in bias voltage, attributed to changes in the LC material.

Due to its uncomplicated structure, the ground plate and the upper surface of the substrate undergo coating with PVA and rubbing to achieve pre-alignment of the LC in the y-direction. Remarkably, a 41° beam steering is attained at 12.5 GHz, with a return loss exceeding 13 dB across the entire range of biasing voltage.

2.2 Tunable LC-Based Microwave Devices

The integration of LC materials in microwave and mm-Wave devices provides the advantage of reconfigurability. In certain devices, such as filters, this reconfigurability manifests as adjustments in frequency tuning, while in others, like phase shifters and impedance tuners,

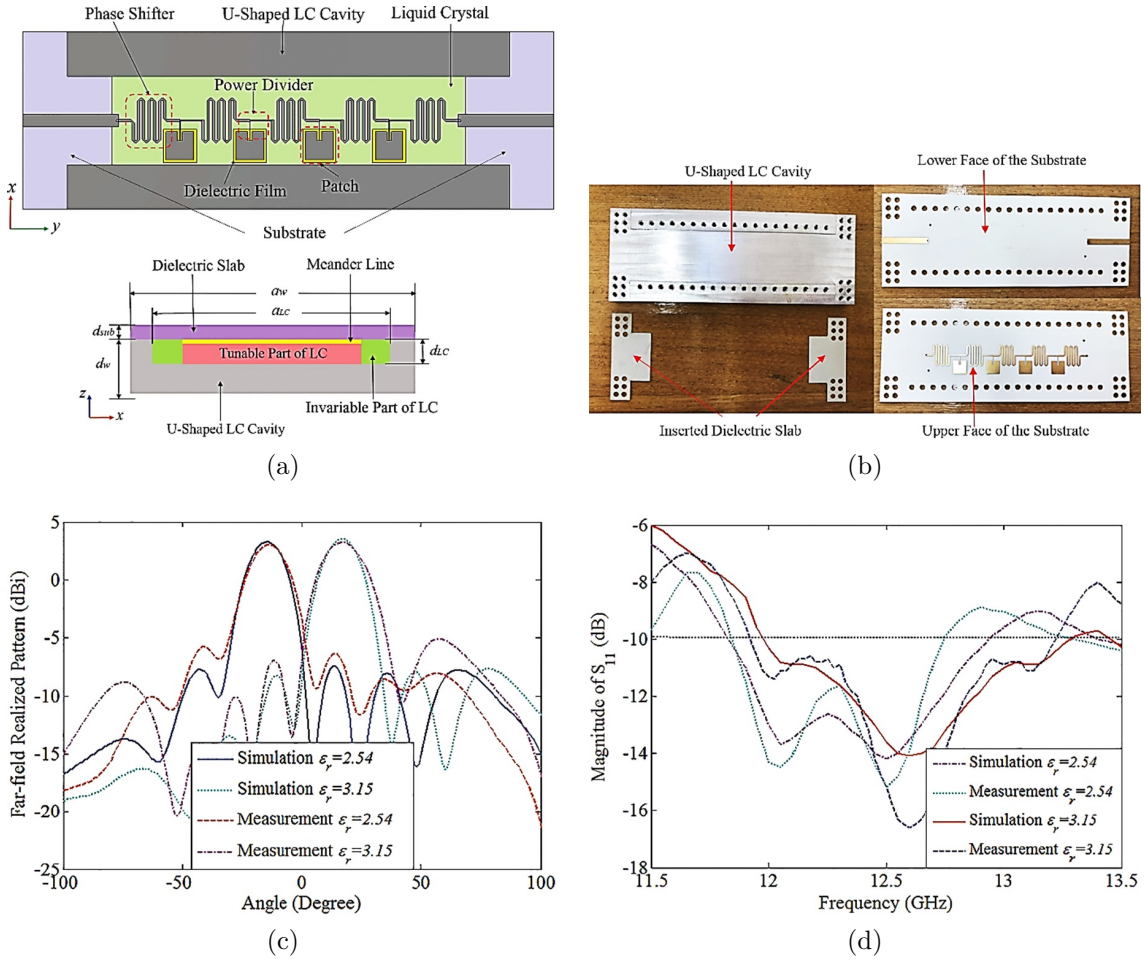


Figure 2.3: Tunable planar array antenna with LC: (a) top and cross-section view, (b) fabricated layers, (c) measured and simulated radiation pattern, and (d) measured and simulated return loss [3].

it leads to modifications in specifications. LC materials have been applied to various structures and devices in the past, and this section will explore a few illustrative examples.

LC-based tunable phase shifters are introduced in references [4] and [50], where permittivity tuning imparts the capability to alter the electrical length of a transmission line. In [4], a tunable phase shifter at 20 GHz is presented, employing a Substrate Integrated Waveguide (SIW) transmission line integrated with LC. The alignment of LC is controlled through the utilization of four electrodes, as depicted in Figure 2.4a.

The SIW transmission line is implemented using Rogers substrate RO4003, characterized by a relative permittivity of 3.38 and a height of 0.5 mm. Continuous tuning is accomplished by varying the voltage applied to the electrodes, specifically, just two of them, within the range of ±200 V. As all alignment states are achieved through the applied voltage to the electrodes (electric field), there is no requirement for a pre-alignment layer treated by the rubbing method. The LC cavity dimensions measure 2 mm in width, 0.5 mm in height, and 31 mm in length. To ensure isolation between the SIW ground and biasing electrodes, a thin layer of silicon nitride is positioned over the ground plane, accompanied by an additional thin layer of silicon nitride between the electrodes and LC.

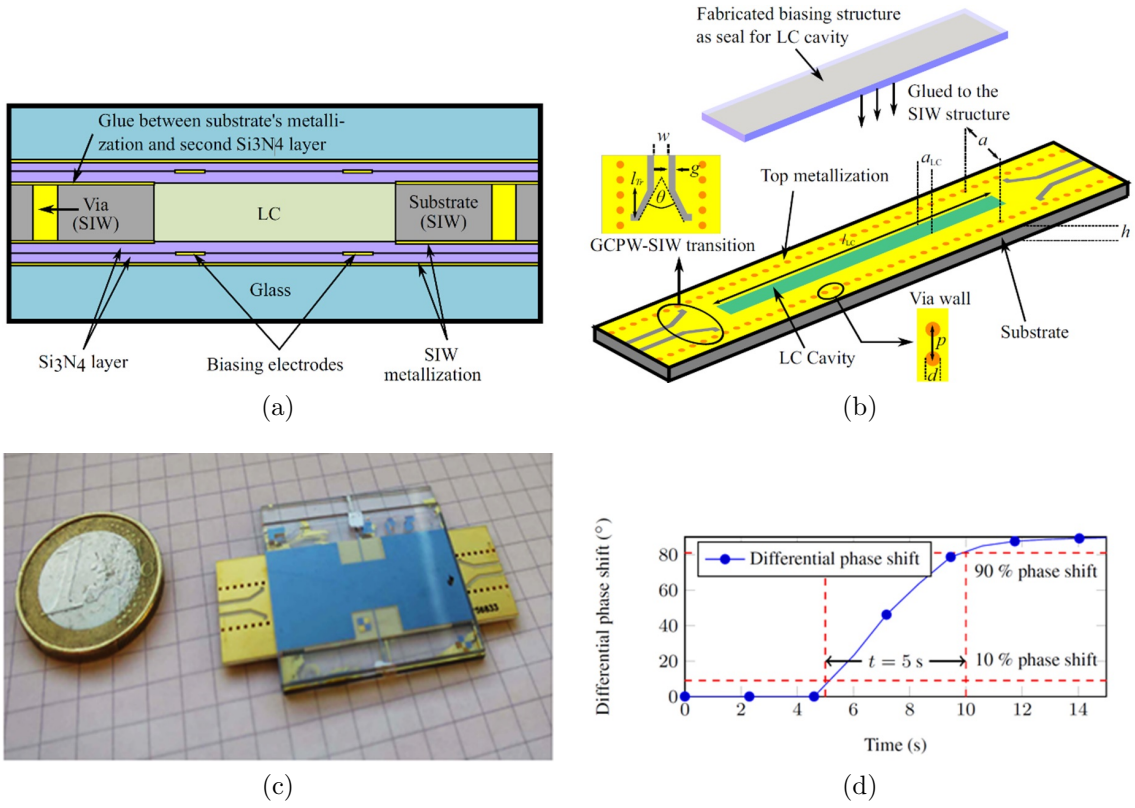


Figure 2.4: (a) Cross-section view of structure, (b) layers of structure, (c) perpendicular state, (d) intermediate state, and (e) parallel state [4].

Given that the SIW is printed on a Printed Circuit Board (PCB), the fabrication process solely involves the deposition of the ground plane and the patterning of electrode lines. Notably, GT3-23001 LC material with $\varepsilon_{\perp}$=2.46, $\varepsilon_{\parallel}$=3.28, $tan\delta_{\perp}$=0.0143, and $tan\delta_{\parallel}$=0.0038,

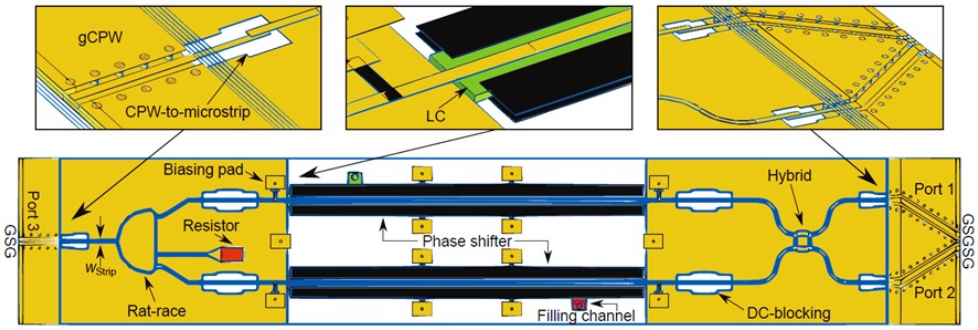
provided by Merck KGaA, has been employed. At 20 GHz, the insertion loss is 4 dB, indicating a 1 dB difference between parallel and perpendicular states, and a return loss exceeding 10 dB. Contrary to the anticipated 94° phase shift based on simulation results, the fabricated phase shifter achieved an 88° shift. Figure 2.4d illustrates the measured response time in the fastest scenario, where the phase shift increases continuously. Intriguingly, the reported response time for the phase shift from 10% to 90% is 5 seconds.

A phase shifter can also serve as the basis for realizing a Single Pole Double Throw (SPDT) switch [5, 51]. The integration of LC material with Low-Temperature Co-fired Ceramic (LTCC) technology is exemplified in [5], functioning within the frequency range of 27 GHz to 33 GHz. The 3D view and details of this work is shown in Figure 2.5a. By incorporating a 90° hybrid and two tunable phase shifters capable of toggling between 0° and 90°, an SPDT switch can be constructed. Electrode pads are designed to govern both parallel and perpendicular states, eliminating the need for the pre-alignment of LC. Electrodes and biasing states are depicted in Figure 2.5b.

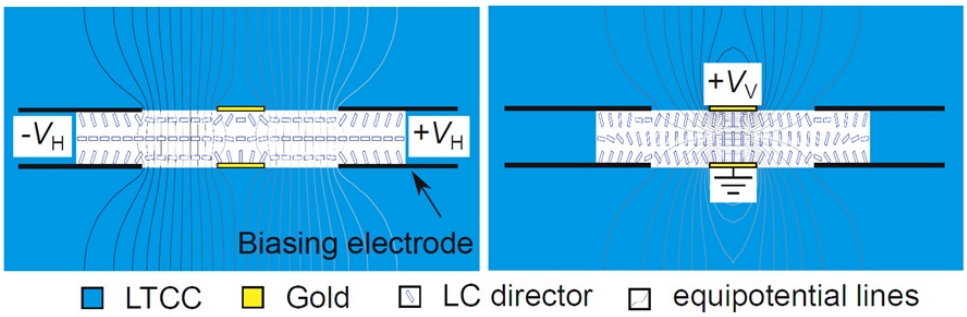
The input and outputs are implemented using CoPlanar Waveguide with Ground (CPWG) transmission lines, while the Wilkinson power divider, phase shifters, and hybrid are fabricated over a microstrip. A DuPont 9k7 LTCC with a relative permittivity of 7.1, loss tangent of 0.001, and a thickness of 107 μm was employed. GT3-23001 LC material, provided by Merck KGaA, was utilized, featuring a relative permittivity ranging from 2.47 to 3.16 and a loss tangent of 0.009. Two filling channels were established, one for each phase shifter. The reflection coefficient was documented as superior to 10 dB, albeit with a 9 dB insertion loss. In the quest for optimal biasing conditions, every conceivable voltage combination for electrodes was tested, ultimately settling on applied voltages of 5.5 V and 9 V. Similar to most other state of the are devices, this SPDT switch is relatively large as illustrated in Figure 2.5c.

Another SPDT switch utilizing an LC-based phase shifter in a dielectric waveguide is detailed in [51]. In this study, a dielectric waveguide was constructed with an internal cavity for LC insertion. Given its dielectric nature, the biasing electrode configuration is relatively straightforward – four electrodes, one for each side of the dielectric. The electrode configuration, depicting both biasing states, is illustrated in Figure 2.6a. Notably, the maximum biasing voltage is relatively high ($\pm$550), attributed to the electrode distance and dielectric material.

Figure 2.6b showcases a fabricated SPDT switch constructed on the dielectric waveguide with biasing electrodes. Figure 2.6c illustrates the fabricated phase shifter featuring a tapering section, necessitating electrodes and biasing voltages. Given its operation in the W band (93-100 GHz), the fabricated device has a relatively large footprint.



(a)



(b)



(c)

Figure 2.5: (a) Overall structure of the SPDT switch with zoom in input port, output port and LC part, (b) electrodes and biasing states, and (c) fabricated SPDT switch with sealed injection holes.[5]

A tunable filter utilizing LC materials is proposed in [6], employing dielectric resonators. GT3-23001 LC material with dielectric properties of $\varepsilon_{\perp}$=2.41, $\varepsilon_{\parallel}$=3.18, $tan\delta_{\perp}$=0.0141, and $tan\delta_{\parallel}$=0.0037 is utilized within a Rexolite 1422 (ε_r=2.53) waveguide filter. LC material is filled into a hole inside each resonator; however, due to the small size of the device, capillary force retains the LC material, obviating the need for sealing. A 3D view of the

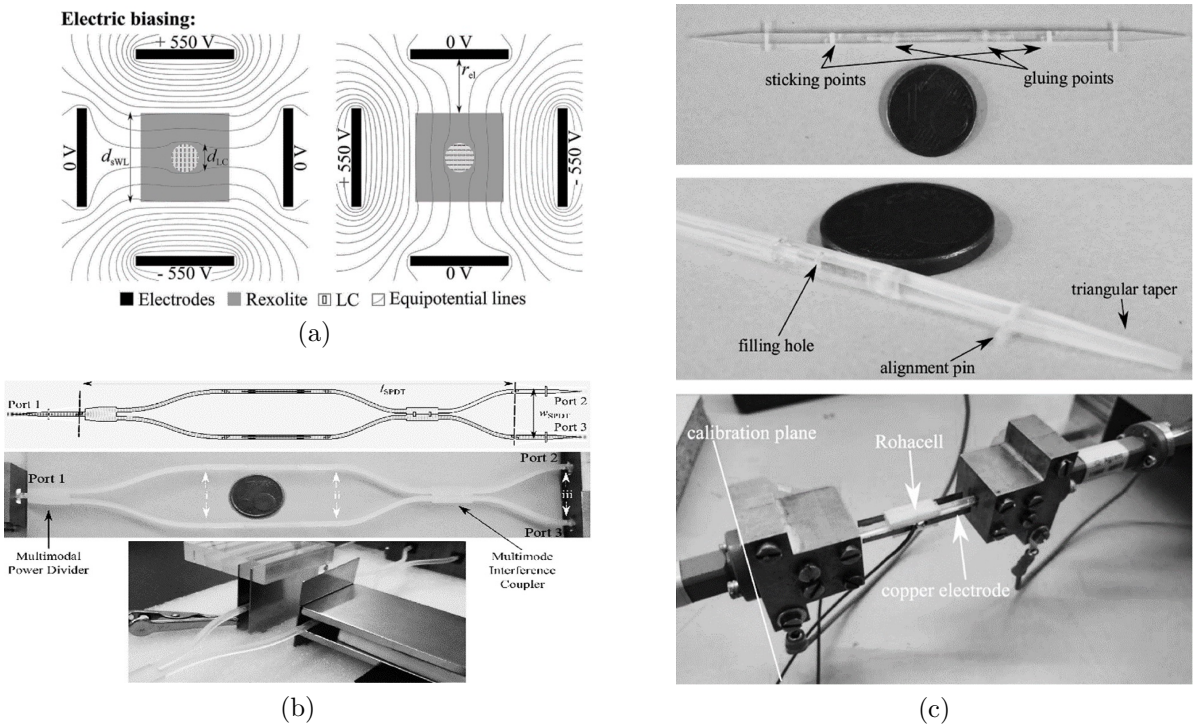


Figure 2.6: (a) Biasing electrodes configuration, (b) complete fabricated structure, and (c) phase shifter part with taper only .

tunable dielectric waveguide is depicted in Figure 2.7a. Given the challenge of achieving pre-alignment in this structure using the rubbing technique, there is a necessity to design electrode configurations that enable control of both states (parallel and perpendicular) through the electric field created by applied biasing voltages. The electrode configuration and layout are displayed in Figure 2.7b.

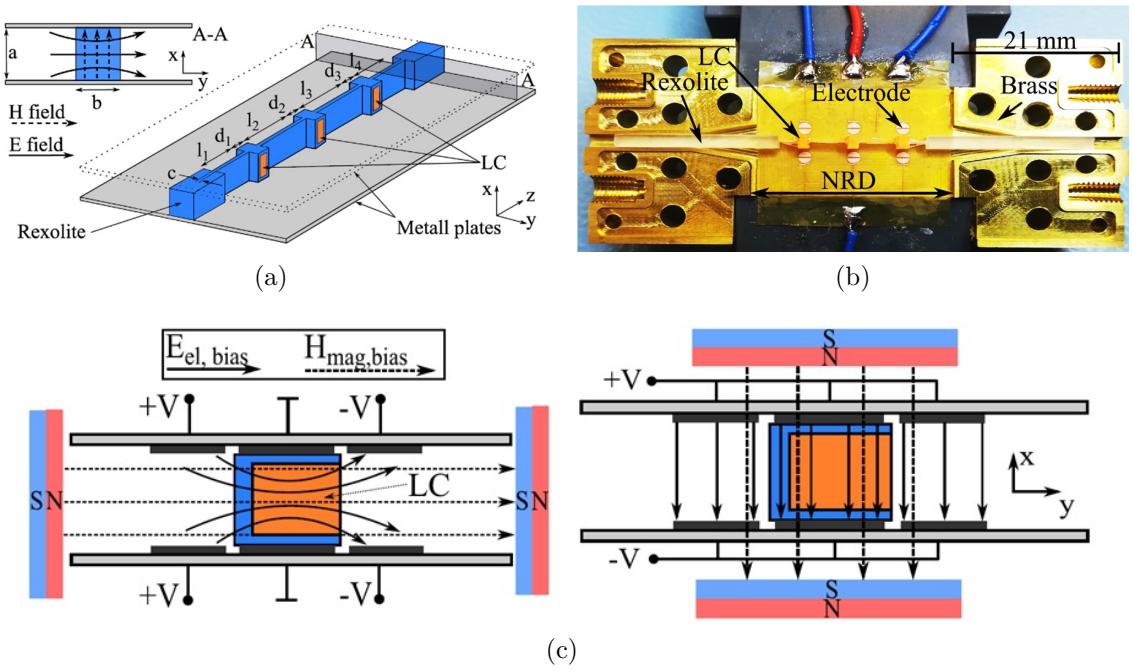
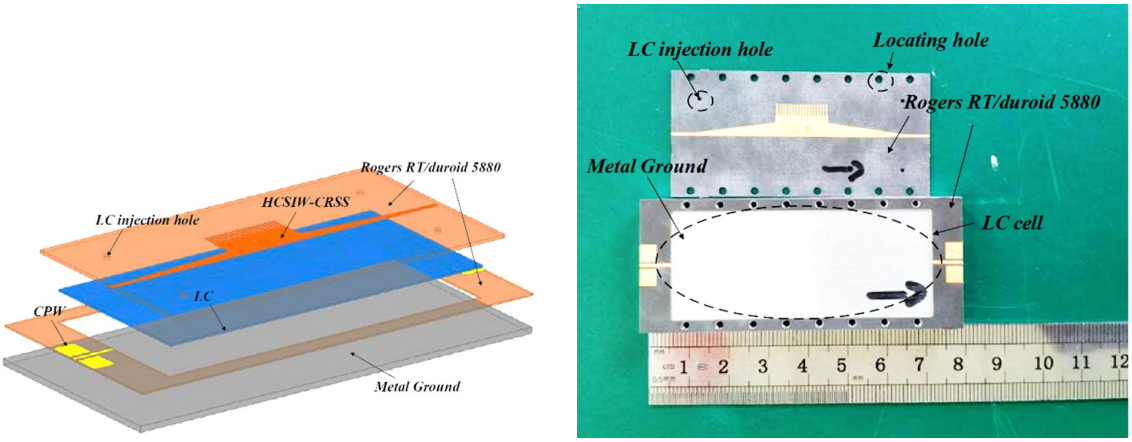


Figure 2.7: (a) 3D view of dielectric waveguide filter with LC filled resonators, (b) fabricated filter without top plate, (c) electrode configuration and biasing conditions [6].

Electrodes are printed on a 12 μm Pyralux PI laminate and positioned over ground plates. A biasing voltage of $\pm$200 V is necessary to attain both the parallel and perpendicular states, and it is applied as illustrated in Figure 2.7c. At 60 GHz, a tuning range of 3% and a bandwidth of 1% are achieved, accompanied by an insertion loss ranging from 4.9 dB to 6.2 dB and a return loss exceeding 10 dB.

LC materials can be incorporated into planar filters to attain tunability, as demonstrated in [7]. Figure 2.8a presents layers of this planar filter, which is a Half-Mode Corrugated Substrate Integrated Waveguide (HMCSIW) operating at 17 GHz. To enhance the band-stop feature of the filter, a split-ring resonator has been integrated into the layout. Employing Rogers RT/Duroid 5880, an LC cavity is formed over a metal ground at a

height of 0.254 mm. A thin layer of PI has been deposited on both the metal ground and the printed layout, facilitating the pre-alignment process through the friction orientation method using a rubbing machine. Figure 2.8b displays the LC cavity and printed filter with a substrate featuring four holes, facilitating the injection of LC material after the two substrates are glued together. The relative permittivity of the utilized LC material can vary from 2.4 to 2.8, considering cavity dimensions of 26×65 mm^2.



(a) (b)

Figure 2.8: (a) Layer view of filter with HMCSIW structure, (b) fabricated filter [7].

The biasing voltage is adjusted within the range of 2 V to 22 V to transition the LC state from a perpendicular to a parallel orientation. The measured return loss is documented as better than 10 dB, and the insertion loss is recorded at 3.4 dB within the frequency range of 16.41 GHz to 17.06 GHz.

2.3 Summary

This chapter delved into the integration of LC materials for tuning microwave and mm-Wave devices, covering CRLH LWAs, filters, switches, and antennas. While LC materials have been utilized in high-frequency devices, their overall dimensions remain relatively large, primarily due to fabrication limitations that necessitate a layer-by-layer assembly process. However, there is significant untapped potential in LC materials when paired with microfabrication techniques. This synergy could yield chip-scale devices character-

ized by lower loss, reduced bias voltage requirements, faster response times, and seamless integration with other RF frontend components.

Chapter 3

Liquid Crystal Materials in Microwave Tunable Devices

This chapter encompasses fundamental aspects of LC materials, encompassing operational principles and alignment techniques. Initially, the fundamental principles governing the behavior and functionality of LC materials will be elucidated through a few examples. Subsequently, the alignment techniques employed in previous LC-integrated devices will be discussed. Finally, a detailed explanation of the adopted pre-alignment treatment method will be provided.

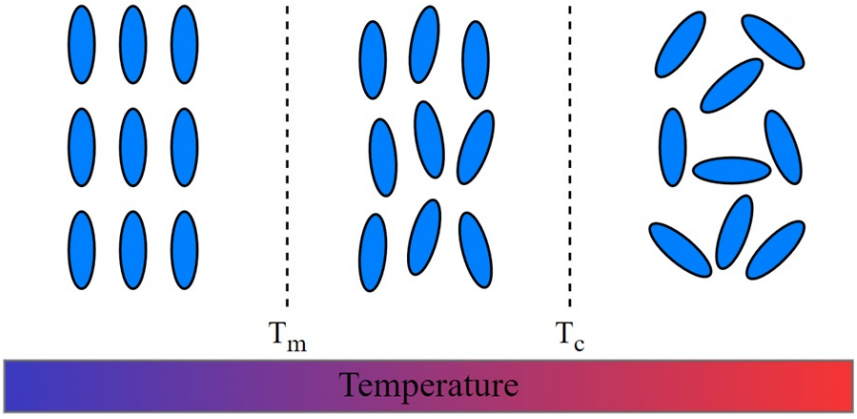
3.1 LC Material Operation Principle

Liquid Crystal technology finds extensive use in display applications, leveraging the birefringence properties of LC materials within the optical domain. The inception of using LC dates back to the 1960s, where it was initially employed as a light filter. In the realm of microwave engineering, birefringence is termed anisotropy and is characterized by a permittivity tensor:

$$\tilde{\varepsilon} = \begin{bmatrix} \varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz} \\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz} \end{bmatrix} .\varepsilon_0 \tag{3.1}$$

within the material's coordinate system (xyz). In optical applications, applying an electrical field will alter the polarization of the light passing through LC, whereas in the microwave domain, the effective permittivity, ε_{eff}, will undergo variation instead.

Figure 3.1 illustrates various phases of liquid crystal materials as a function of temperature. In the solid phase, each crystal unit is isotropic and exists in powder form. Although it can be anisotropic, it is not regarded as a tunable element in this phase, as the molecules are bonded in a crystalline structure and are not free to move or change direction. If the temperature surpasses the clear point, the LC material transitions into a completely clear liquid phase. In this phase, LC molecules are isotropic but not tunable. The clear point temperature is highly dependent on the specific material and the compounds used in its composition.



(a)

Figure 3.1: Different phases of liquid crystal separated by melting point (Tm) and clear point (Tc) temperatures.

Between the melting and clearing points, a Nematic phase is present at specific temperatures for each LC material. The anisotropic behavior of LC materials in the nematic phase presents the potential for their application in tunable microwave and mm-Wave devices. The dielectric properties of LC materials are characterized by a tensor that varies between two states: perpendicular and parallel. In the nematic phase, the molecules of LC materials can align along an applied static electromagnetic field due to the bipolar nature of their molecules.

An illustrative example can help clarify the alignment of LC molecules with more detail. Please refer to Figure 3.2, which presents a cross-section of an LC-integrated planar structure. In Figure 3.2a, LC molecules are uniformly oriented horizontally, a state referred to as perpendicular. In such planar structures, this state is achieved by employing a polymer layer (either PI or PolyAmide (PA)) coated on both top and bottom metal layers. In [52], polyvinyl alcohol is employed as the pre-alignment layer. However, for enhanced

effectiveness, it traditionally undergoes treatment using a rubbing machine.

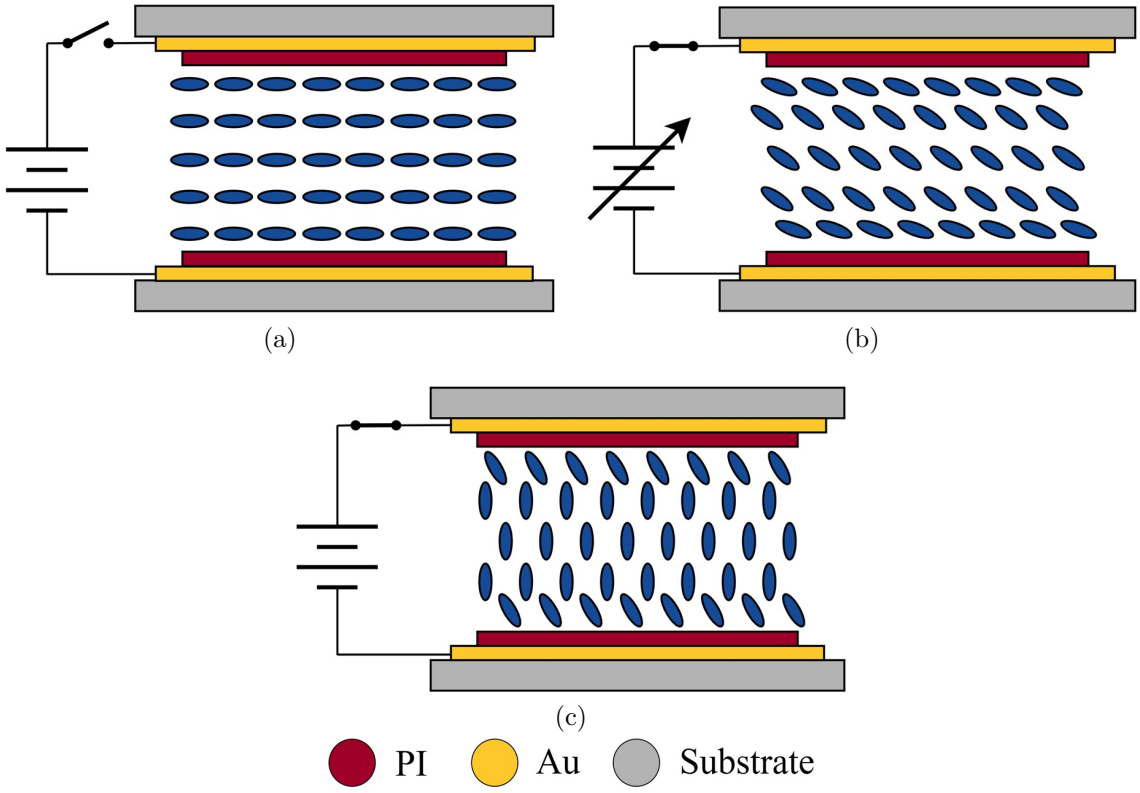


Figure 3.2: Cross section of different liquid crystal molecules orientation in a planar structure, (a) perpendicular orientation, (b) middle state, (c) parallel orientation.

As depicted in Figure 3.2b, applying voltage to the top patch induces the reorientation of LC molecules. It is crucial to note that the surface force created by the PI layer remains in place. However, elevating the voltage strengthens the electric field, exerting a more significant impact on the LC material. Under these conditions, setting a specific voltage can yield the desired permittivity and, consequently, the expected performance from the device.

As the voltage increases, more LC molecules align with the applied field. However, at specific points where the saturation voltage is reached, a further increase in applied voltage (field) does not induce any change in effective permittivity. In such cases, the utilized LC material is in the parallel state. A careful examination of Figure 3.2d reveals that despite the majority of LC molecules between the two plates aligning vertically, some molecules

are not. Those molecules in close proximity to the top and bottom plates, influenced by the treated PI layer, orient themselves halfway between perpendicular and parallel states. Molecules not directly situated between the plates are more influenced by the surface anchoring force of the pre-alignment layer. Moreover, the applied electric field converges in non-vertical lines in those areas.

In recent publications, a variety of microwave LC materials have been utilized, as summarized in Table 3.1, showcasing their properties at room temperature across specific frequencies. The table illustrates a progressive increase in variation percentage, with K15 exhibiting the least tunability and GT7-29001 emerging as the most tunable LC material. The evolution of LC materials over the past decade has resulted in enhanced tunability, reduced loss tangent, and expanded maximum operating temperature, particularly by elevating the clear point. Although this study employed GT3-23001, a high-performance LC material, exploring superior materials in similar device configurations holds promise for improved outcomes. For instance, adopting GT5-28004 could significantly reduce loss and enhance the quality factor, while integrating GT7-29001 would expand the tuning range.

Table 3.1: Properties of microwave liquid crystals at room temperature, at the specified operating frequency.

LC	Frequency	$\varepsilon_\perp$	$\varepsilon_\parallel$	$tan\delta_\perp$	$tan\delta_\parallel$	$\Delta\varepsilon$	τ_ε	Tc	Reference
K15	10 GHz	2.72	2.9	0.03	0.03	0.18	6.2	38°	[53]
BL037	10 GHz	2.35	2.61	0.06	0.06	0.26	10	-	[53]
E7	5 GHz	2.72	3.17	0.12	0.02	0.45	14.2	58°	[54]
BL006	4.8 GHz	2.62	3.11	0.0191	0.0069	0.5	16.1	118.5°	[55]
CDZSL-018	4 GHz	2.46	2.95	0.037	0.037	0.49	16.6	-	[2]
CDZSL-016	12 GHz	2.7	3.25	-	-	0.55	16.9	-	[1]
BMW29	38 GHz	2.44	3.22	0.0122	0.0039	0.78	24.2	-	[56]
GT3-23001	19 GHz	2.5	3.3	0.0143	0.0038	0.8	24.2	173.5°	[53]
GT3-24002	10 GHz	2.5	3.3	0.0123	0.0032	0.8	24.2	173.5°	[57]
GT5-26001	19 GHz	2.39	3.27	0.007	0.0022	0.88	26.9	146°	[58]
GT5-28004	19 GHz	2.4	3.32	0.0043	0.0014	0.92	27.7	151°	[59]
TUD-566	19 GHz	2.41	3.34	0.006	0.0027	0.93	27.8	105.5°	[58]
GT7-29001	19 GHz	2.46	3.53	0.0116	0.0064	1.07	30.3	124°	[60]

While simulating the LC-based devices using Ansys Electronics Desktop software (i.e., HFSS), defining the dielectric properties of the LC material accurately is crucial for obtaining reliable results. To ensure this, the LC material should be defined as a tensor for each specific state. Table 3.2 provides the values for the dielectric constant, ε, and loss tangent, $tan\delta$ used in the simulations. These values are distributed linearly within the

specified range. These tensor values account for the orientation-dependent behavior of the LC molecules of GT3-23001 material.

Table 3.2: Tensor representative of used LC material.

	State 1 (perpendicular)	State 2	State 3	State 4	State 5 (Parallel)
$\boldsymbol{\varepsilon}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 3.3 & 0 \\ 0 & 0 & 2.5 \end{bmatrix}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 3.1 & 0 \\ 0 & 0 & 2.7 \end{bmatrix}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 2.9 & 0 \\ 0 & 0 & 2.9 \end{bmatrix}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 2.7 & 0 \\ 0 & 0 & 3.1 \end{bmatrix}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 2.5 & 0 \\ 0 & 0 & 3.3 \end{bmatrix}$
$\boldsymbol{tan\delta} \times \mathbf{10^3}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 3.8 & 0 \\ 0 & 0 & 14.3 \end{bmatrix}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 6.4 & 0 \\ 0 & 0 & 11.7 \end{bmatrix}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 9.1 & 0 \\ 0 & 0 & 9.1 \end{bmatrix}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 11.7 & 0 \\ 0 & 0 & 6.4 \end{bmatrix}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 14.3 & 0 \\ 0 & 0 & 3.8 \end{bmatrix}$

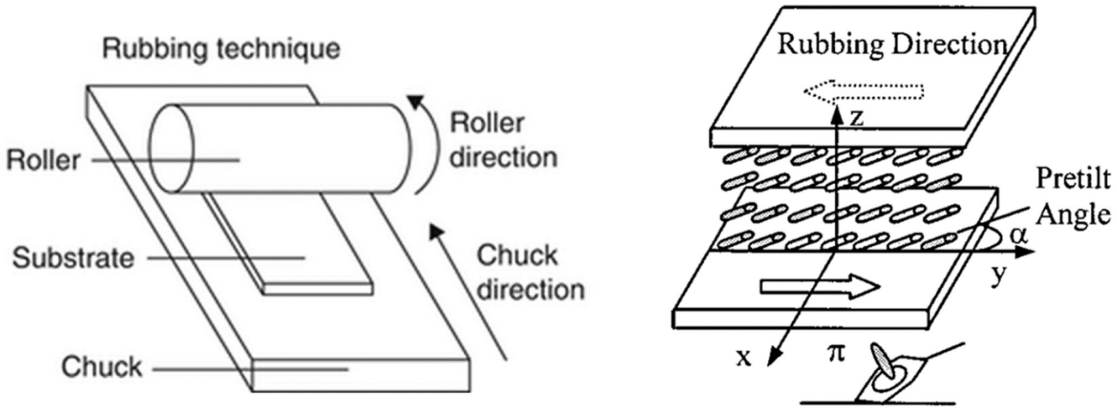
It is important to acknowledge that in state 1, the LC molecules are oriented along the Y-axis, while in state 5, they align with the Z-axis. In states 2 to 4, there is a gradual rotation of the LC molecules towards alignment with the Z-axis. However, it is noteworthy that the properties along the X-axis remain constant since the LC rotation is assumed to occur exclusively within the Y-Z plane.

3.2 Alignment Techniques in LC-Integrated Devices

As previously explained, LC molecules possess a bipolar form, and they respond to applied electromagnetic fields. This concept forms the foundation of alignment methods utilized in all LC-based devices, including displays, microwave, and mm-wave applications. There are three primary methods for aligning LC materials: static electric field, static magnetic field, and surface anchoring.

The application of a static electric field influences the alignment of affected LC molecules. Electromagnetic fields can realign LC molecules in the same direction as the field itself. It should be noted that while creating the static electric field, a wide distance between two plates will necessitate a very high applied voltage. With some state-of-the-art examples in mind from Chapter 2, for an LC thickness of 200 μm, there might be a requirement of $100 - 200$V. Conversely, an LC thickness of 10 μm may only require a bias voltage as small as $10 - 15$V. Regarding the use of magnetic fields, the rule of thumb holds true, but magnetic fields are generated either using coil magnets or permanent magnets. Thus, a specific voltage (for coil magnets) or magnet strength cannot be ruled out.

As for the surface anchoring method, it is possible to align LC molecules in a specific direction using treated PI, PA, or a diamond-like carbon film. When using PI, it should be spin-coated and cured over the desired surface [61, 62, 63]. Conversely, diamond-like carbon can be deposited onto the surface using Plasma-Assisted Chemical Vapor Deposition (PACVD) as a thin film [64, 65]. PI film can be treated either by a rubbing machine with a roller covered in velvet cloth [66, 56, 67] or through exposure to low-intensity IBI [68, 9, 69]. Both treatment methods create micro-grooves on the surface of the pre-alignment layer. Consequently, the major axis of polar LC molecules will orientate in the same direction as the micro-grooves upon exposure. Since the molecules in the vicinity of the surface are aligned horizontally, the remaining molecules within the volume of the LC will follow the same pattern.



(a) (b)

Figure 3.3: Creation of micro-grooves using rubbing machine, (a) the overall setup including substrate, roller, chuck and direction of movement [8], (b) Placement of rubbed surfaces with PI coating showing rubbing direction [9].

The crucial details of the rubbing technique are depicted in Figure 3.3a, including the rotation of the roller and the movement directions of the chuck. It is important to note that the roller should be covered with velvet cloth containing lint to rub the surface of the coated PI on the substrate. Upon completing the rubbing process on both the top and bottom substrates, they should be positioned according to the setup illustrated in Figure 3.3b. If the substrates are asymmetrical, this placement should be taken into account during the rubbing process.

However, in practice, a combination of different alignment techniques is often employed

to fine-tune the state of LC molecules. Table 3.3 illustrates the possible combinations of alignment techniques in LC-based devices.

Table 3.3: Summary of combinations of different alignment methods in microwave applications.

		Forces Used for State II		
		Magnetic Field	Electric Field	Surface Anchoring
Forces Used for State I	Magnetic Field	Waveguide devices	Dielectric Waveguides	Not used
	Electric Field	Dielectric Waveguides	SIWs and Dielectric Waveguides	Planar devices
	Surface Anchoring	Not used	Planar devices	Not tunable

For metallic waveguide devices, only a magnetic field will be effective, as placing electrodes inside a completely sealed metallic structure could be challenging. Since both states are achieved using a magnetic field, it can involve one of the following setups: movable permanent magnets, a combination of permanent and coil magnets, or two coil magnets. The first and last combinations have been utilized in this research, and further details are presented in Chapter 5.

A combination of electric and magnetic fields is often employed in dielectric waveguides. The primary advantage of this approach is that biasing electrodes can be positioned to surround the waveguide without impacting the transmission of the wave. Meanwhile, permanent magnets can facilitate the initial alignment in the absence of an electric field. Any state in between can be achieved by tuning the strength of the electric field, controlled by bias voltage.

Relying solely on an electric field for all states is feasible only when the encapsulated LC is considerably small. This scenario is typically observed in SIWs and dielectric waveguides. It is important to note that since all states of LC material should be controlled by the electric field, the placement of electrodes requires special attention. Figure 2.5 and Figure 2-6 illustrate some examples of fully electrically controlled LC-integrated SIWs with at least 4 electrodes.

The surface anchoring force is effective only in close proximity, limiting its application to planar devices with relatively small LC cavity dimensions. This method's effectiveness is enhanced when combined with an electric field, as surface anchoring is not variable and is fixed based on surface features of a polar material such as PI. However, when combined with an electric field, it can add tunability. The use of a magnetic field along with surface

anchoring is not common since the small planar structures are not suitable for the presence of a static magnetic field to control the state of LC molecules.

3.3 Adopted treatment technique for LC-integrated Silicon-based chip devices

The traditional method to treat the pre-alignment layer involves a rubbing machine equipped with a roller. To utilize this method effectively, the surface containing the pre-alignment layer should be flat. However, all proposed devices in this work are based on micromachined silicon and have at least two surfaces. Figure 3.4 illustrates the side view of a rubbing machine's roller over a device with a multi-level surface.

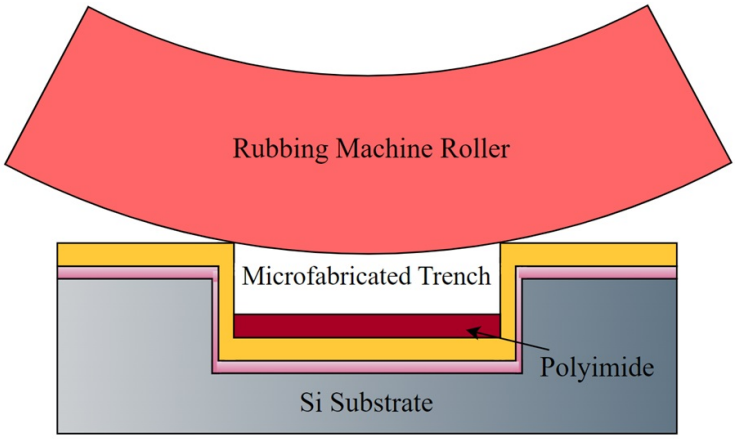


Figure 3.4: Side view of a rubbing machine's roller in contact with a multi-level surface of microfabricated device.

As depicted in Figure 3.4, treating the PI layer using the rubbing technique is not feasible. Therefore, an alternative method of IBI is required. As explained in section 3.2, diamond-like carbon is primarily used in this method. The preference for diamond-like carbon stems from its desirability in the display industry, where a more transparent film is advantageous, as it blocks as little light as possible. However, applying diamond-like carbon film presents challenges for us, mainly due to the lack of availability of this material in our PECVD chambers and the absence of a reliable method to properly pattern it.

In this research, the IBI technique has been adopted for silicon microfabricated devices with a small footprint. The process begins with the preparation of the PI solution. In

this study, Nylon-6 is dissolved in Trichloroethanol (Organic ethanol) to enable application to small structures and create a thin layer. The exact proportions of Nylon-6 and Trichloroethanol are available in Table 3.4.

Table 3.4: Substances used for pre-alignment layer solution.

SUBSTANCES	CHEMICAL NOTATION	AMOUNT
NYLON 6	$[NH\text{-}(CH_2)_5\text{-}CO]_n$	3 g
TRICHLORETHANOL	$C_2H_3Cl_3O$	100 g

The uniformity of the PI layer is crucial, especially in large devices where thickness discrepancies can vary significantly. To address this, after applying the PI solution, the device undergoes a spin-coating process to achieve a uniform and smooth layer. The latest spin profile is presented in Table 3.5.

Table 3.5: Spin-coating profile for Nylon 6 solution.

STEP	SPEED (RPM)	DURATION (SECOND)
STEP 1	500	5
STEP 2	1000	10
STEP 3	2000	30
STEP 4	1000	10
STEP 5	500	5

The thickness of the PI layer will be below 100nm when the above-mentioned spin profile is used. To prepare the layer for surface treatment, it should be cured at a high temperature to ensure all solvents evaporate. This process should be conducted with care, as sharp increases or decreases in temperature could result in separated or damaged PI layers. The temperature steps and timing for the curing process are presented in Table 3.6.

The curing process takes approximately 5 hours to complete, resulting in a hard, thin layer of PI ready for further treatment processes. The IBI technique necessitates a directed Ar ion beam hitting the PI surface. The available equipment in clean room facilities is the Ion Milling system. The Intlvac Nanoquest Pico Ion-Milling System is available at the CIRFE lab, as shown in Figure 3.5.

This tool is a dry etching system primarily used for etching metals, PIs, and PA. The etching profiles typically require a high voltage beam and long etching durations to complete. However, surface treatment necessitates relatively lower voltage and shorter

Table 3.6: Baking profile of coated device with thin layer of Nylon 6.

STEPS	TEMPERATURE (° C)	DURATION (MINUTES)
STEP 1	0 – 90	30
STEP 2	90	60
STEP 3	90 – 180	30
STEP 4	180	60
STEP 5	180 - 0	120



Figure 3.5: Intlvac Nanoquest Pico Ion-Milling System available at CIRFE lab.

exposure times. According to research, the optimal angle for ions to impact the surface is 45°, resulting in maximum surface anchoring force. An essential setting to consider is substrate rotation, which should be turned off during the process.

The required direction of ion beams that hit both substrates of a device is illustrated in Figure 3.6. The impact angle of ions is crucial, and failure to adhere to this configuration could result in poor performance and minimal variation of LC material's properties. To ensure this, the correct placement of both sides of a chip capacitor is depicted in Figure 3.7, and any device using this technique should follow the same setup.

Considering Figure 3.7, after the surface treatment procedure, points A and B will align with points A' and B'. This placement ensures the proper setup required for this technique, as depicted in Figure 3.6. The optimized parameters used in the Ion Milling system are 200V for beam voltage for a duration of 40 seconds at a 45° angle. The impact of this treatment is on a nanoscale, thus, to verify the treatment's physical effect, the surface

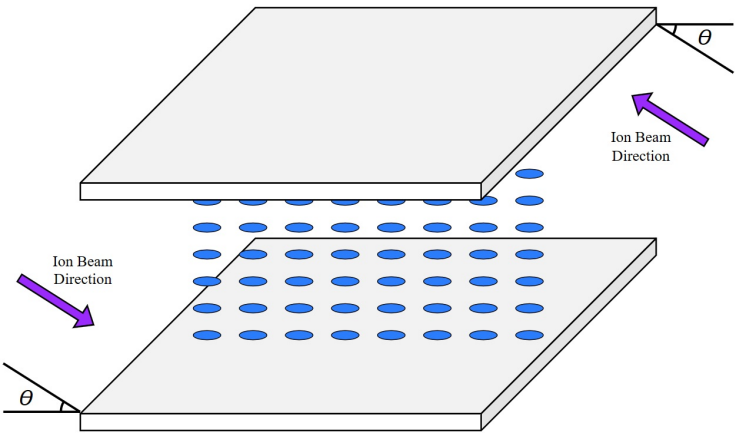


Figure 3.6: Ion beam impact angle to both substrates of a planar device.

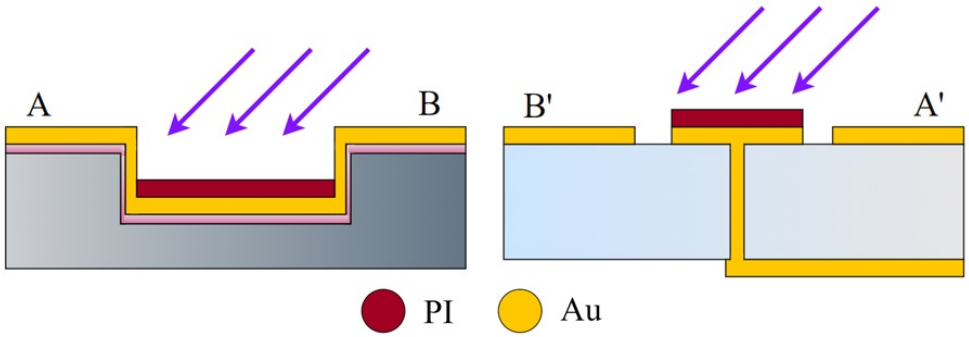
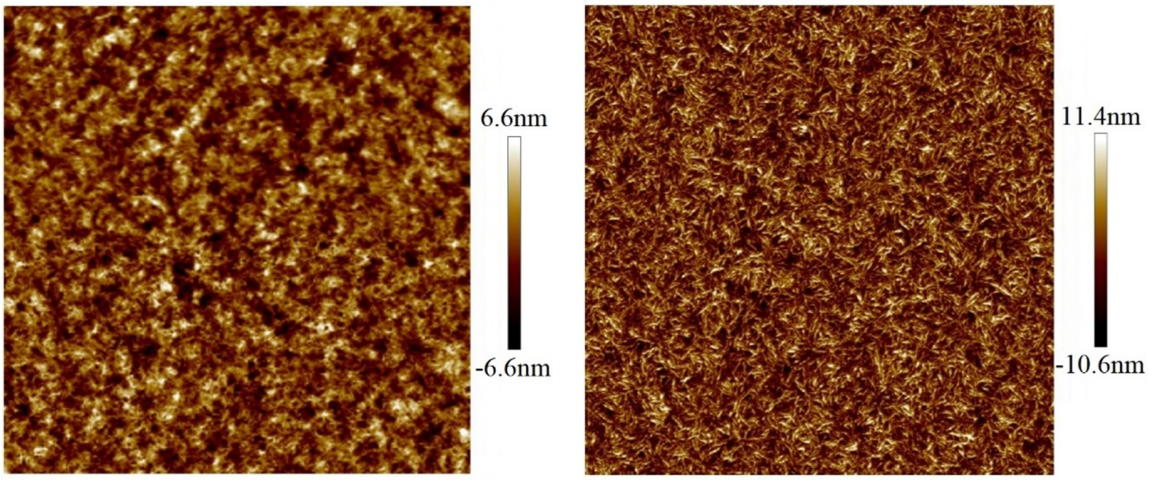


Figure 3.7: Placement of both substrates of a chip capacitor inside the Ion Milling system's chamber.

should be inspected at a nanoscale. For this purpose, an atomic force microscope is used on both untreated and treated surfaces of PI, as shown in Figure 3.8.

AFM images reveal the change in morphology of the surface, showcasing deeper features. It should be noted that the AFM sensor can only detect the vertical features of the surface, while the surface treatment leaves angled cones and edges. Therefore, it is expected that AFM images cannot thoroughly investigate all changes. Overall, the surface roughness is almost doubled using this treatment technique. The real efficacy of this method will be evaluated by measurement results of proposed chip devices.



(a) (b)

Figure 3.8: AFM image of the PI surface over area of 5x5 um, (a) before and, (b) after Ion Milling system treatment.

3.4 Summary

This chapter explores the operational principles of LC materials in microwave devices, highlighting their tunability in the nematic phase. Temperature fluctuations significantly impact the tuning range, leading to a clear point where the material becomes isotropic. For planar structures, biasing voltage via two plates and a pre-alignment layer are necessary for dielectric property control. Notably, ion beam treatment, a more effective alternative for silicon microfabricated devices, replaces conventional rubbing machine techniques. The process involves careful pre-alignment layer preparation and IBI, as clarified through the Intlvac Nanoquest Pico Ion-Milling Systems. AFM analysis validates the method's efficacy by confirming physical changes post-treatment, providing compelling evidence of its effectiveness.

Chapter 4

Single-Chip Liquid Crystal Variable Capacitors

The variable capacitor serves as a fundamental component in a wide range of RF applications and finds utility in various tunable devices, including but not limited to tunable filters, phase shifters, and impedance tuners [70, 71, 72]. Both semiconductor analog and switched-capacitor technologies are readily accessible in the market, offered by numerous manufacturers. Over the last two decades, numerous publications have addressed the advancements in switched-capacitor technologies incorporating MEMS and PCM. However, these capacitors often provide only a limited number of states, which restricts their applicability in various applications that demand analog tuning capabilities.

On the other hand, semiconductor analog capacitors exhibit nonlinearity, low Q values, and high Direct Current (DC) power consumption. BST based devices, while offering better Q and power handling, come with the drawbacks of complex fabrication processes, limited frequency coverage, and only slightly improved linearity [73]. In contrast, LC technology holds the potential to achieve analog variable capacitors with higher Q values. Moreover, thanks to the primary role of biasing voltage in creating an electric field, LC-based devices maintain consistently low DC power consumption, regardless of the biasing state. Additionally, LC materials can operate effectively up to 100 GHz [74], accompanied by a simpler and more cost-effective fabrication process. A comparison of analog tunable materials is presented in Table 4.1.

In recent years, several papers have been published focusing on LC-based tunable devices [75, 76, 6]. However, in these studies, the LC was integrated with bulky RF structures to simplify handling and pre-alignment procedures. This research presents miniature chip-

Table 4.1: Comparison of continuous tunable medias

	Semiconductor	***BST***	***LC***
Size	Small	Medium	Large
Quality factor	Low	Medium	High
Frequency (up to)	C band	Ka band	W band
Tunability	High	Medium	Low
Linearity	Very Low	Moderate	High
Power Handling	Low	High	High
Tunning Speed	Fast	Fast	Slow
Power Usage	Moderate	Low	Negligible
Fab Complexity	High	High	Moderate
Fab Cost	High	Moderate	Moderate

scale variable capacitors achieved through a clean room fabrication process that employs silicon-micromachining technology and an IBI procedure for pre-alignment.

While Figure 4.1a depicts the shunt capacitor, Figure 4.1b and Figure 4.1c showcase the advanced developed capacitor configurations. The utilization of two series capacitors in configuration b leads to an enhancement in power handling capability [52]. This is a result of power being evenly distributed over the two capacitors, with double the capacity of the required single capacitor. Furthermore, it provides a dedicated bias pad, which serves to isolate the DC applied voltage from the input lines.

In the subsequent subsections, the structure of each chip capacitors is described, and the proposed fabrication process for each capacitor is presented in detail. This chapter further includes the presentation of simulation and measurement results obtained from prototype units constructed to validate the proposed concept. The chapter ends with the summary of proposed single chip variable capacitors.

4.1 Shunt Capacitor

This section details the design and fabrication of a silicon-micromachined shunt variable capacitor utilizing nematic LC technology. The LC material is enclosed within a thin micromachined housing, offering electronic control over its dielectric properties. The chip

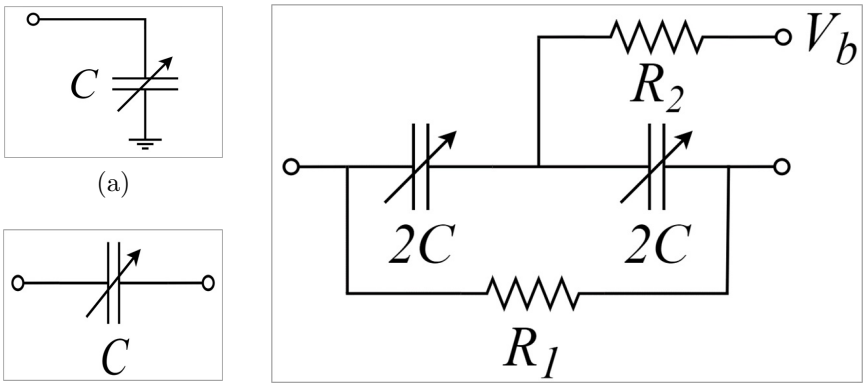


Figure 4.1: Fabricated variable capacitors' schematic in different configurations: (a) single port shunt capacitor, (b) two-port series capacitor with an integrated bias line, and (c) two-port series capacitor.

capacitor demonstrates versatility across a broad spectrum of RF reconfigurable applications requiring analog tuning. The measurement and simulation outcomes for the chip LC variable capacitor is presented, showcasing a measured quality factor ranging from 44 to 123 at 1 GHz. Biasing voltage, adjustable from 0 V to 40 V, induces a measured capacitance shift of 18% in the fabricated micromachined capacitor. The devices are manufactured through an in-house multi-layer microfabrication process.

4.1.1 Design Concept

The shunt capacitor comprises two main components: a silicon-micromachined housing designed for LC encapsulation and a substrate. Figure 4.2 provides a top view of the substrate, the housing, and their integration, offering a comprehensive understanding of their arrangement.

On the other hand, Figure 4.3 presents a 3D view of the integrated chip capacitor. The capacitor is constructed with two plates, with one plate positioned within the trench, and the other plate printed on the underside of the substrate. The top surface of the substrate features a CPW line, facilitating the testing and characterization of the capacitor.

In the fabrication process, holes are created in the substrate to facilitate the injection of LC material into the trench. The shunt capacitor plate has dimensions of $1.1 \times 1.1\ mm^2$. To ensure proper isolation of the plate from the metalized micromachined sidewalls, additional

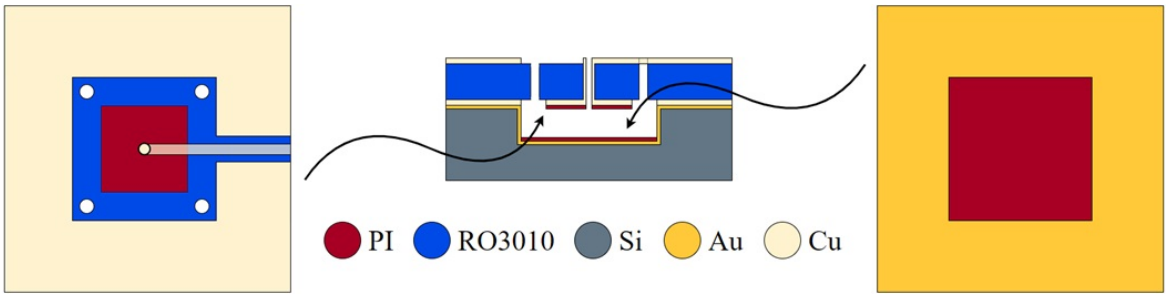


Figure 4.2: Design of the proposed LC-integrated variable shunt capacitor, side view (not to scale) and top view of two parts from LC material standpoint.

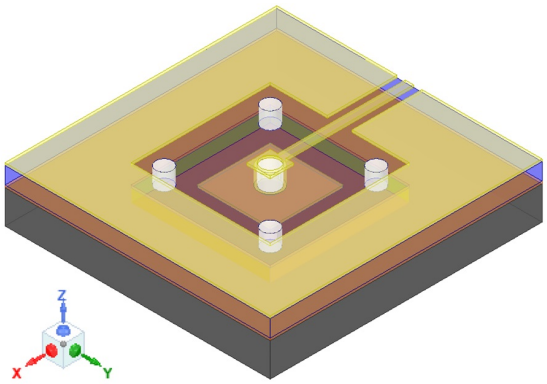


Figure 4.3: 3D view of the proposed shunt capacitor in Ansys Electronics Desktop software.

spacing is added on both sides. Furthermore, a grounding area is incorporated to simplify the packaging process. Although the actual size of the LC variable shunt capacitor as a standalone chip can be 1.6×1.6 mm^2, the overall dimensions of the prototype unit in this research are 5.2×5.2 mm^2. This larger size allows for RF probing and laboratory testing requirements.

4.1.2 Fabrication Process

The key fabrication steps are depicted in Figure 4.4. The fabrication process commences with a 450 μm intrinsic silicon wafer. A layer of positive PR is spin-coated onto the wafer, which is subsequently subjected to photolithography and development steps. The photoresist is subsequently removed selectively from the trench area, preparing it for a dry etching process executed through a DRIE system, achieving a depth of 100 μm with 90°

sidewalls. This etching requires 192 cycles in an Oxford silicon DRIE system. Its cleanly etched sidewalls are of significant importance for the subsequent required metallization. Following the removal of the PR layer, a plasma clean process is performed as a preparation step prior to the deposition of metal layers.

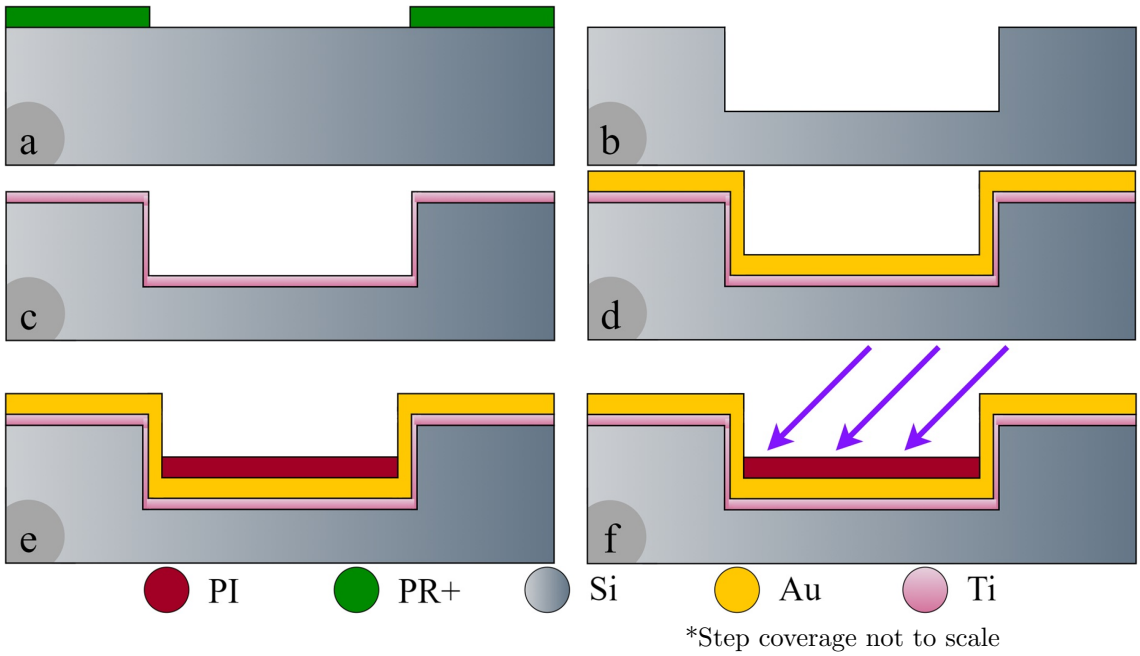


Figure 4.4: Fabrication process flow for developing LC-integrated micromachined shunt capacitor: (a) spin coating, photolithography, and development of positive PR, (b) dry etch using DRIE, (c) plasma clean and sputtering of Ti as adhesion layer, (d) Au sputtering as seed layer, then electroplating, (e) PI coating and curing, (f) introducing PI layer to IBI system.

To ensure proper adhesion of the gold layer, it is essential to utilize an adhesion layer. In this case, a thin layer of titanium with a thickness of 20 nm is sputtered first, followed by the sputtering of a gold seed layer with a thickness of 60 nm. It is crucial that these two steps are performed in the same chamber without venting. The reason for this is that titanium immediately oxidizes upon exposure to air (specifically, oxygen), which prevents the gold seed layer from bonding to the titanium.

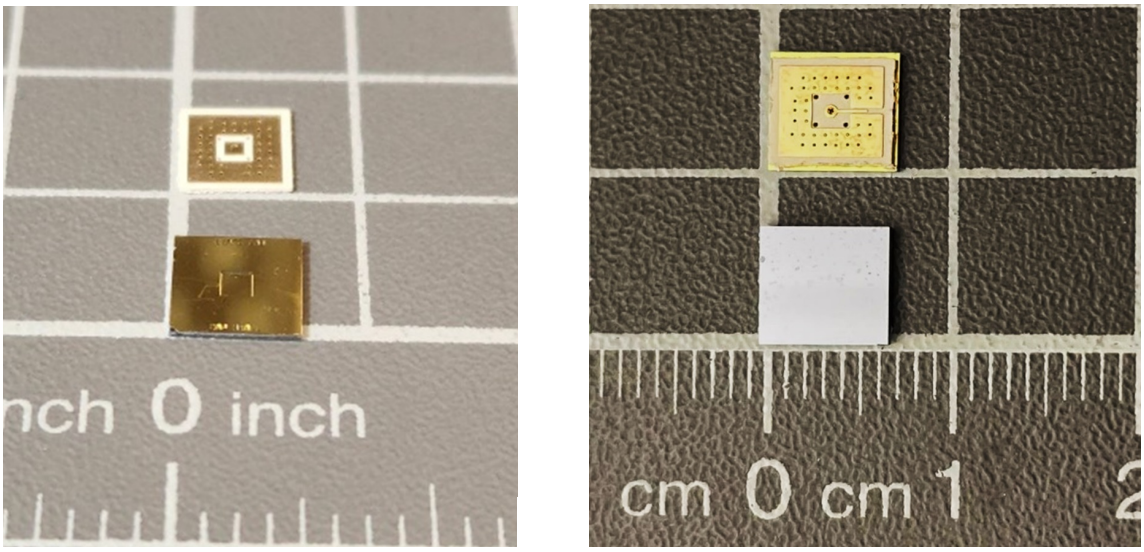
The use of a sputtering system is necessary as it provides a vacuum environment, ensuring uniform metal deposition and effective coverage of the deep sidewalls of the trench. This coverage ensures the grounding of the bottom of the trenches, which acts as the second

capacitor's plate. Moreover, it aids in the creation of a static electric field for alignment purposes.

To serve as the pre-alignment layer, a 100 nm thick PI layer is created. This thickness is chosen to minimize its impact on the performance while optimizing its effectiveness as a pre-alignment layer. The curing process involves subjecting the PA layer to a smooth temperature curve, reaching up to 180°C. This process eliminates any remaining solvents in the PI layer, resulting in a solid and stable surface for further treatment.

4.1.3 Fabricated Device

Figure 4.5a shows two parts of the chip capacitor and Figure 4.5b illustrates the packaged device from both top and bottom. LC filling holes are visible on the top part as shown in the side view in Figure 4.2. The LC material is injected into the encapsulated trench using a 10 μL syringe with a needle.



(a) (b)

Figure 4.5: LC-based capacitor, (a) top and bottom sections before packaging and (b) two chip capacitor sample.

It is important to note that the PI coating, curing, and surface treatment should also be applied to the plate printed on the bottom surface of the substrate. After the surface

treatment is completed, the substrate and the silicon-micromachined housing are assembled together using a die bonder. A low-temperature bonding process conducted at 118°C to ensure proper bonding between the components. Finally, to seal all the holes, a special adhesive that does not mix with the LC material is used. In this work, NOA/UVS 91 adhesive is employed. After applying the adhesive, the package is exposed to UltraViolet (UV) light to initiate the curing process and solidify the adhesive.

4.1.4 Results

In Figure 4.6, the capacitance simulation result is depicted as a function of frequency for different states of the LC material. As the LC material transitions from a perpendicular state to a parallel state, the simulation reveals a 24% change in the capacitance value specifically at 1 GHz as the capacitance changes from 0.59 pF to 0.73 pF. The tuning range increases as the frequency goes higher because it gets closer to the resonance frequency.

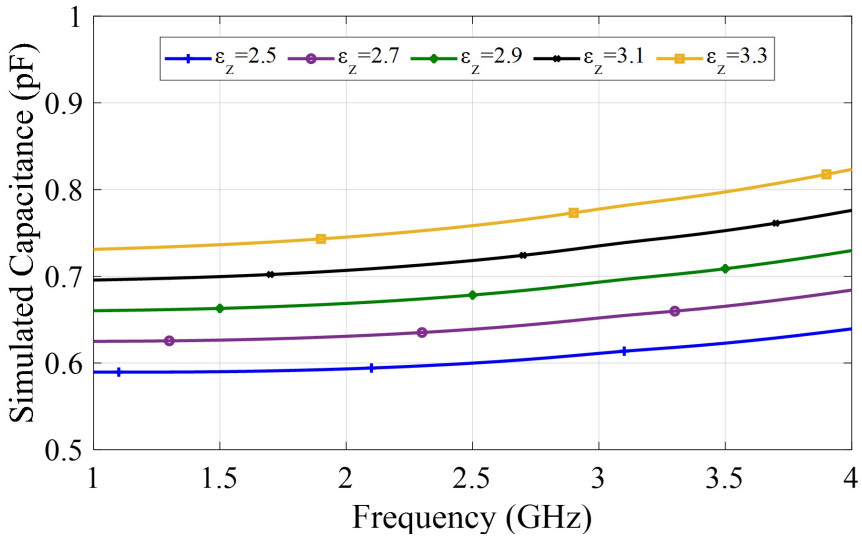


Figure 4.6: Simulation results of shunt capacitor, capacitance vs frequency.

The quality factor undergoes variation as well. When permittivity is the lowest, it is equal to 65, and it increases with the variation of dielectric properties. Eventually, it reaches over 150 at 1 GHz and peaks around 2 GHz. Figure 4.7 shows the decrease in Q as the frequency increases, as it should reach zero at the resonant frequency.

The measurements were conducted using a 250 μm pitch probe on an RF probe station, as depicted in Figure 4.8. The results of these measurements indicate an 18% shift in

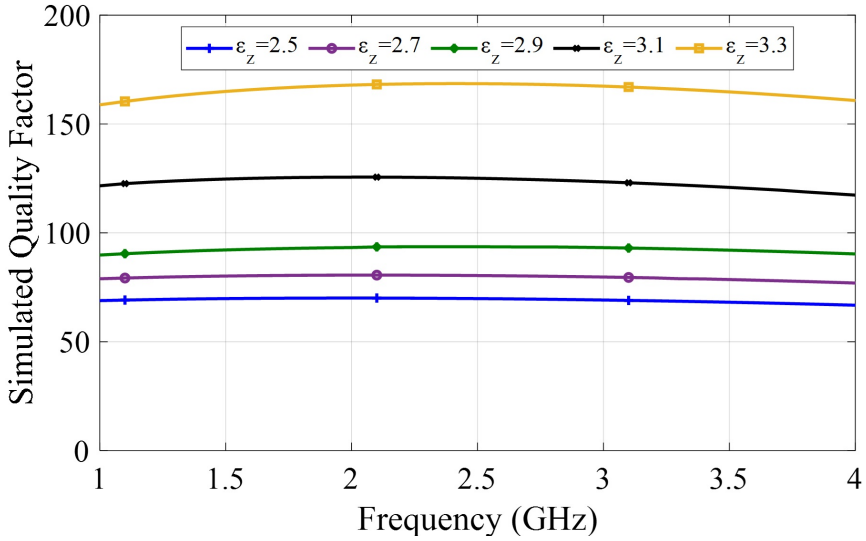


Figure 4.7: Simulation results of shunt capacitor, Q factor vs frequency.

capacitance at 1 GHz when the bias voltage is increased from 0 V to 40 V. Specifically, the capacitance changes from 0.62 pF to 0.73 pF at the said frequency. It is worth noting that as the biasing voltage increases further, the change in capacitance becomes less noticeable.

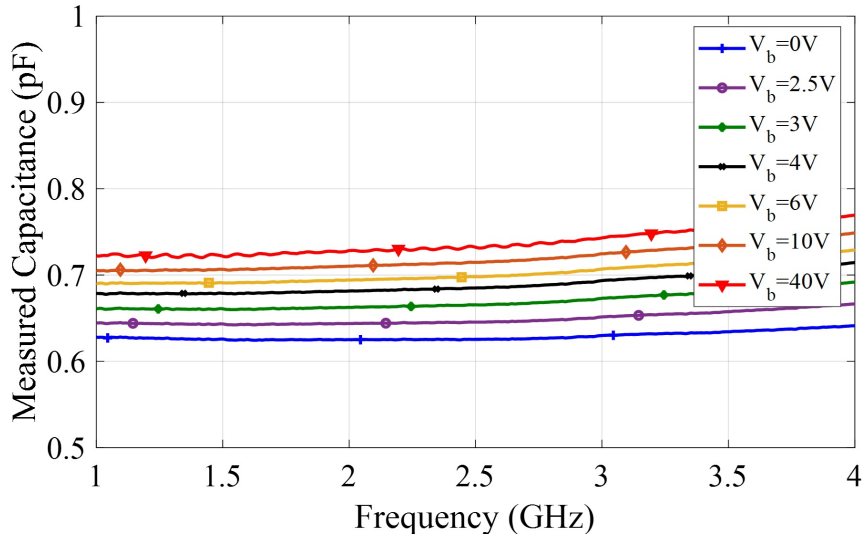


Figure 4.8: Measurement results of shunt capacitor, capacitance vs frequency.

When there is no bias voltage, the quality factor is equal to 44, and it increases with

the variation of dielectric properties. Eventually, it reaches over 123 at 1 GHz, where it is at its peak. Figure 4.9 shows the decrease in Q as the frequency increases, as it should reach zero at the resonant frequency.

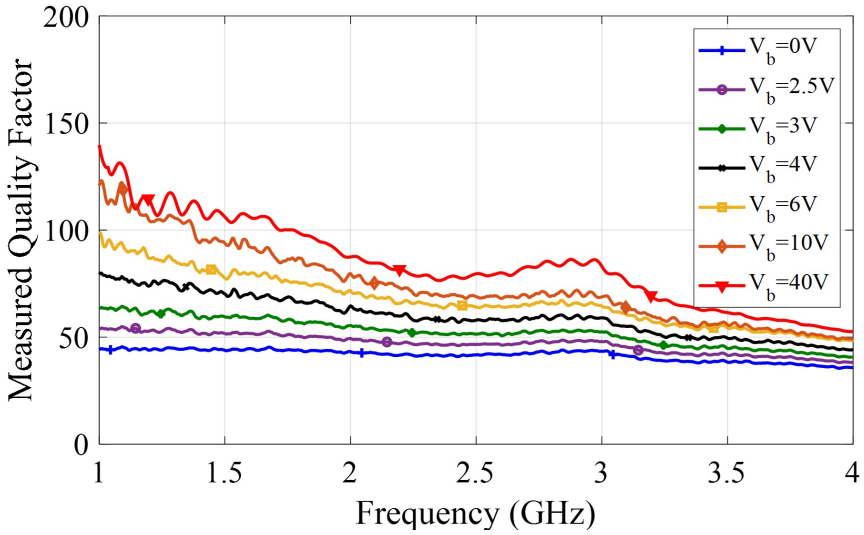


Figure 4.9: Measurement results of shunt capacitor, Q factor vs frequency.

The shunt prototype unit exhibits certain limitations that impact the achievable capacitance tuning range. Firstly, the presence of the input transmission line, via hole, and RF testing pads can introduce parasitic effects and interfere with the LC capacitor. Furthermore, the fabrication tolerance of the top Rogers RO3010 substrate, which is used in this prototype unit can also affect the accuracy of the obtained measurements. Fabrication tolerances introduce variations in the physical dimensions and characteristics of the device, which in turn can influence the measured capacitance values. It is important to consider these limitations when interpreting the results and understanding the achievable performance of the shunt capacitor prototype unit.

4.2 Series Capacitor with Integrated Bias Line

This section details the design and fabrication of an LC-based series capacitor featuring an integrated bias line, strategically aimed at isolating voltage control from RF terminals. The capacitor serves a pivotal role in devices where series capacitors are essential. Demonstrating a 21% shift in capacitance and achieving a quality factor of up to 45 at 1 GHz,

the capacitors' performance was thoroughly assessed through measurement and simulation. The incorporation of a dedicated bias line ensures precise voltage control while preserving RF signal integrity. Unlike the previous capacitor, this capacitor features a 10 μm thin layer of LC material, which contributes to lower control voltage requirements and faster response times.

4.2.1 Design Concept

The series capacitor with a bias line consists of two distinct parts: the top part, made of micromachined silicon, and the bottom part, made of Alumina. Figure 4.10 showcases a side view, the LC material perspective of this device. The top micromachined silicon part has a single plate in the trench that is shared between the two series connected capacitor (as shown in Figure 4.1b) along with the LC filling holes. The bottom Alumina substrate has the input and output lines, capacitor plates, two resistors (R_1 and R_2 in Figure 4.1b), and the bias line. Together, these components contribute to the functionality of the series capacitor with an integrated bias line.

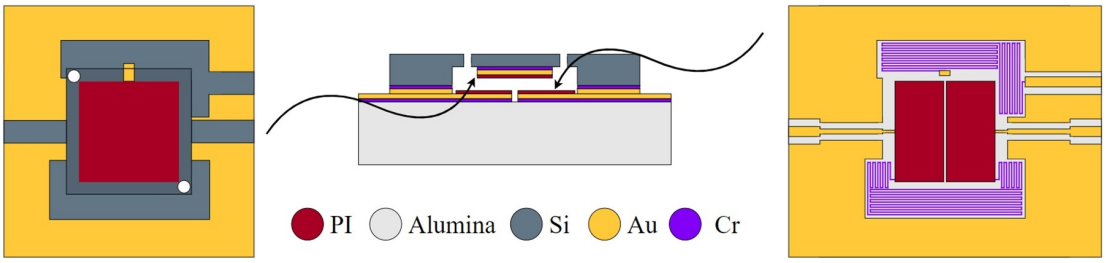


Figure 4.10: Design of the proposed LC-integrated series variable capacitor with an integrated bias line, side view (not to scale) and top view of two parts from LC material standpoint.

For full-wave simulation purposes, this device is modeled in Ansys Electronics Desktop software with all details included. The 3D view of the design is shown in Figure 4.11. The resistors were verified in a separate simulation and later added to the final capacitor design.

4.2.2 Fabrication Process

The fabrication process flow, as depicted in Figure 4.12, commences with photolithography to create patterns for the filling holes. Subsequently, DRIE is employed to etch through the

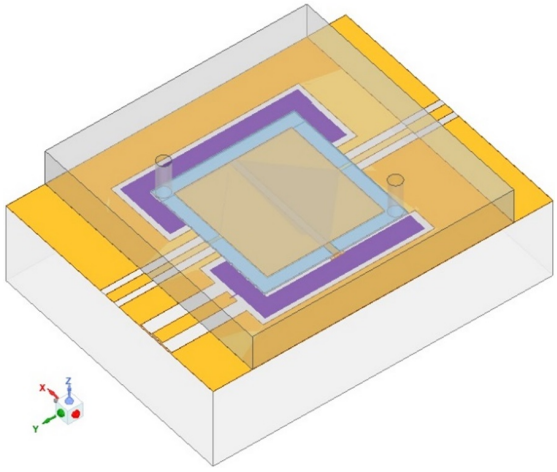


Figure 4.11: 3D view of the proposed series variable capacitor with an integrated bias line in Ansys Electronics Desktop software.

silicon, resulting in long and straight holes with a diameter of 100 μm. After the cleaning process, a second round of photolithography is necessary to create the housing for the LC material. The Oxford DRIE system is employed once more, this time for 22 etching cycles to produce a trench with a depth of 10 μm. Following this, metallization is deposited on both substrates. Considering the requirement for an adhesion layer and the need to fabricate resistors on alumina, it is prudent to use a metal that can be easily patterned in later steps. In this case, chromium is employed as the adhesion layer with a thickness of 40 nm, followed by a 150 nm thick layer of gold as the seed layer for the electroplating process. The use of a sputtering system is essential to ensure proper metal coverage, especially on the sidewalls of the trench. It is important to note that the common plate located at the bottom of the trench needs to be connected to the bias line. To achieve this, a narrow line is brought to the top surface, which will be connected to a small, patterned metallization. This metallization will subsequently be connected to the bias pad using a resistor fabricated in a later step.

It is important to highlight that introducing resistors by depositing metal significantly complicates the fabrication process. The complexity arises from the requirement of E-Beam evaporation deposition for metal lift-off. However, this method fails to establish a connection with the existing capacitor plates and pads. In such a scenario, utilizing a sputtering system would address the electrical connection issue, but it would pose challenges in achieving well-defined features due to uniform coverage over the photoresist. Consequently, the decision was made to employ the adhesion layer as the base layer for patterning the

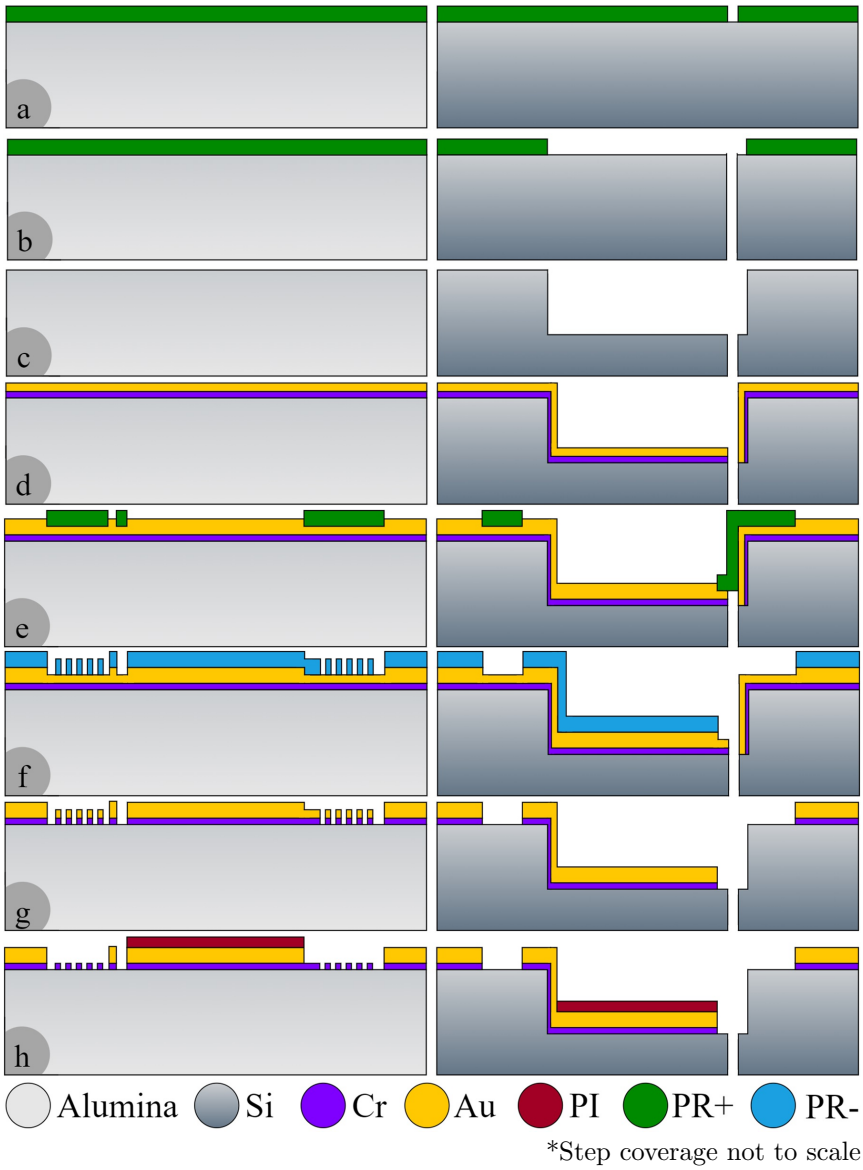


Figure 4.12: Fabrication process flow for developing LC-integrated micromachined series capacitor with an integrated bias line: (a) photolithography of positive PR, (b) etching through using DRIE, photolithography of positive PR, (c) etching 10 μm using DRIE and cleaning. (d) Sputtering chromium and Au. (e) Photolithography of positive PR, electroplating Au, (f) removing positive PR, photolithography of negative PR, (g) dry etch Au and Cr using Ion Milling system, cleaning, (h) wet etch Au, adding DRIE to capacitors' plates.

resistors.

In the subsequent photolithography step, areas that are not intended to be metallized in the final stage are covered with a PR layer. This ensures that only the desired areas will undergo electroplating, resulting in a thickness of 2 μm for the desired metallization.

Following this, the unwanted metallization is removed, and resistors are created. The resistors are designed as meander lines with a width of 4 μm, requiring precise photolithography. A negative PR is used in the photolithography process to form the meander lines and expose the areas where unwanted metallization is present. Subsequently, a dry etching process utilizing an Ion Milling system is employed to remove both the 150 nm of gold and the 40 nm of chromium. Cleaning the PR leaves a patterned metallization on the wafers.

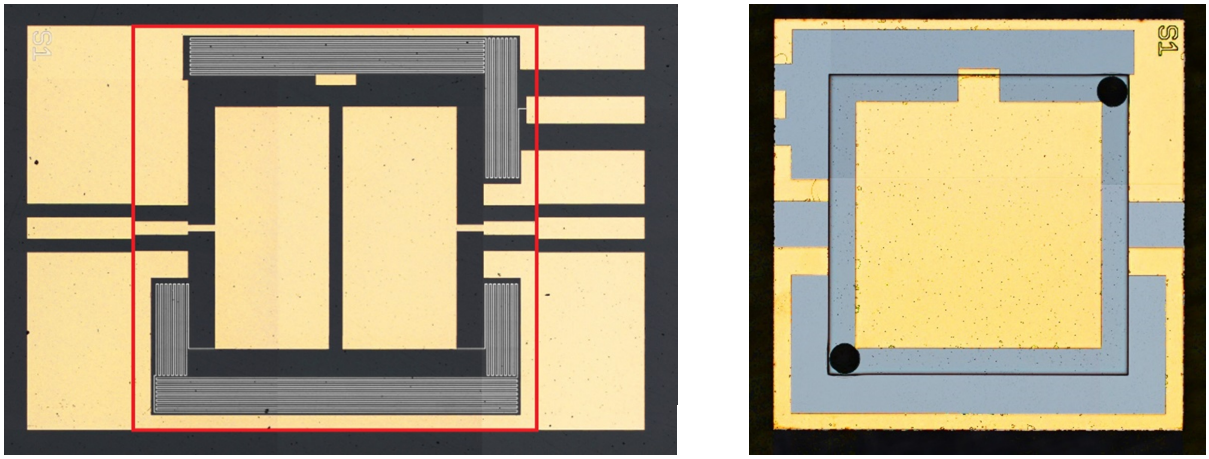
Since the meander lines are initially covered with sputtered gold, a timed wet etching process is utilized to remove the gold layer, leaving only the chromium-made resistors. After this step, a layer of nylon-6 is deposited on the capacitors' plates and cured with a smooth temperature curve. The samples are then ready for the dicing and pre-alignment treatment. The pre-alignment treatment is followed as explained in chapter 3 and configuration shown in Figure 3.7.

Subsequently, the two sides of the capacitor will be bonded together. While Au-Au bonding typically requires high temperature and pressure, the plasma cleaning, and IBI processes utilized in the previous steps simplify the bonding process [77, 78]. The bonding is achieved using a die-bonding machine, with a temperature of 235°C and a force of 10 kg applied for 10 minutes. This results in a strong and accurate bond between the two substrates.

4.2.3 Fabricated Device

Figure 4.13a illustrates the fabricated bottom part of the device, which is made on alumina. The two plates are interconnected by the meander resistor (R_1 in Figure 4.1b), which has a measured resistance of 220 kΩ. This configuration ensures that if either the input or output is grounded in terms of DC, the other will follow suit. In the top area of the image, another meander line resistor (R_2) is visible, measured 180 kΩ using 5μm DC probes. This resistor connects the bias line to a rectangular pad. This rectangular pad serves as a bridge to connect the bias line to the common plate located within the trench.

Figure 4.13b depicts the top part of the device, where the substrate is made of micromachined silicon. In the center, the 10 μm deep trench is clearly visible, with dimensions of 1.1×1.1 mm^2. Two filling holes are also situated at the far end corners of the trench.



(a) (b)

Figure 4.13: Microscope images of the LC-based series capacitor with an integrated bias line, (a) bottom part made on alumina and (b) top part made on high resistivity silicon.

An important feature to note is the narrow line extending from the top of the common plate, which has metalized sidewalls and is connected to the rectangular gold structure on the upper surface. It is worth mentioning that the top part folds back onto the bottom substrate over the indicated red square area. This bonding ensures proper alignment and connection between the top and bottom parts of the device.

Figure 4.14 provides a zoomed-in view of the left side of R_1, offering more detailed insights into its structure that allows for a closer inspection of the device's features and characteristics. On the other hand, Figure 4.15 presents a 3D view of the final packaged device. This view provides a comprehensive illustration of the device's overall structure and appearance, showcasing its completed and assembled form.

Due to the small dimensions of the device ($1.5\times1.9\ mm^2$) and the 100 μm filling holes, it is not feasible to fill the LC material using a syringe. Therefore, an alternative filling approach is adopted, which is suitable for such small devices. In this method, the packaged device is placed upside down in a pool of LC material. The device, along with the LC material, is then positioned in a vacuum chamber and the pressure is reduced to 10^{-6} mTorr. This vacuum environment ensures that all air is drawn out of the LC housing within the packaged capacitor. Subsequently, the pressure is increased, and since there is a vacuum inside the cavity, the LC material is forced into it. This filling process ensures complete and bubble-free filling of the housing, maximizing the performance of the device.

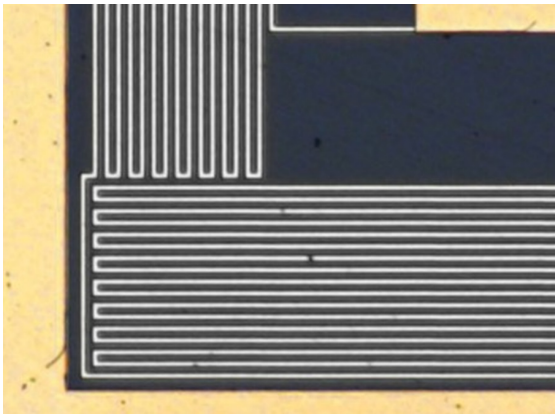


Figure 4.14: Zoomed image of the meander line resistor.

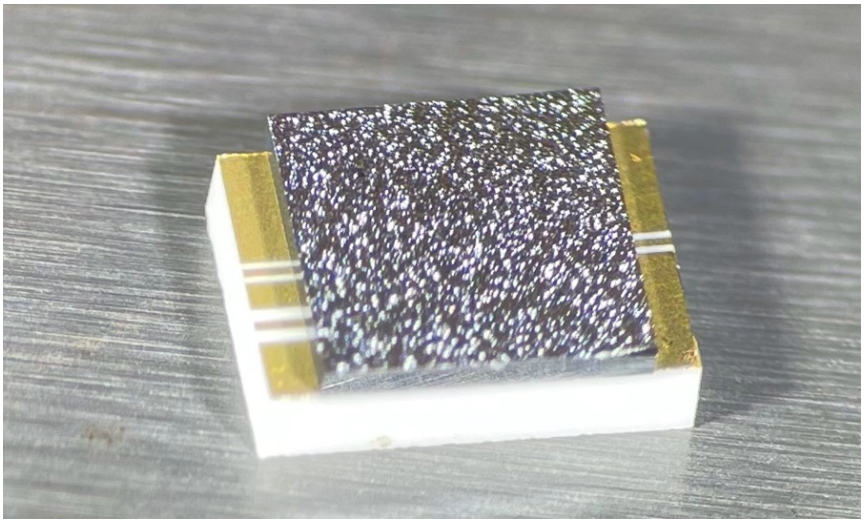


Figure 4.15: Packaged series capacitor with extended input, output, and bias line.

4.2.4 Results

In Figure 4.16, the simulation results of the series capacitor with an integrated bias line are presented. These simulations were performed using the tensor values provided in Table 3.2. The simulation results reveal a 24% variation in capacitance value, ranging from 0.74 pF to 0.92 pF.

Additionally, the quality factor exhibits variations, ranging from peak values of 30 to 59, shown in Figure 4.17. It is worth noting that the presence of resistors in this

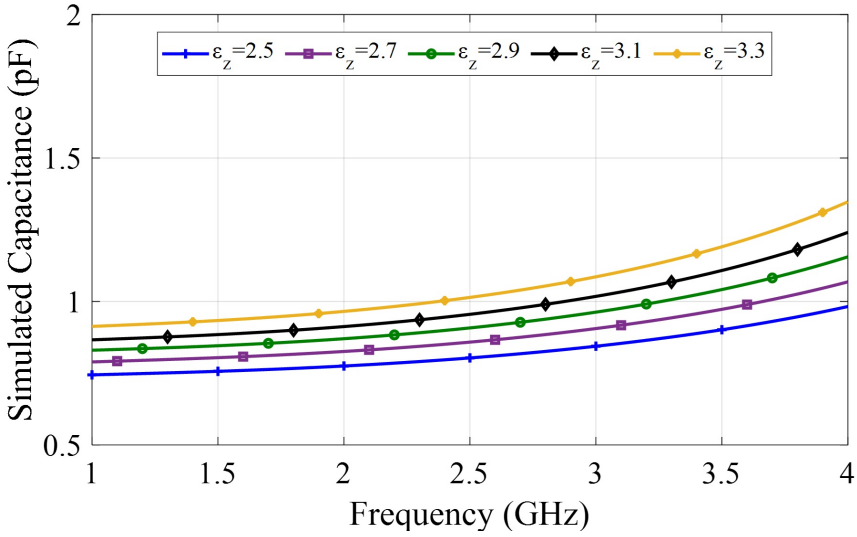


Figure 4.16: Simulation results of series capacitor with integrated bias line, capacitance vs frequency.

configuration impacts both the maximum achievable quality factor and the capacitance variation. These resistors introduce additional losses and affect the overall performance of the series capacitor. However, they help in isolating PI from RF and make it easy to integrate the capacitor in RF tunable applications that require the use of a series-connected variable capacitors.

In this design, the LC material used is much thinner compared to the previous shunt capacitor. As a result, the intensity of the electric field required to control the orientation of the LC molecules is higher for the same applied voltage. In the measurements, this has led to a lower bias voltage ranging from 0 V to 15 V. To accommodate the smaller footprint of the series capacitors, the measurements were conducted using 150 μm pitch Ground-Signal-Ground (GSG) probes. The input lines were grounded DC, while the bias voltage was connected using a 5 μm DC probe.

Figure 4.18 presents the measurement results of the series capacitor with the integrated bias line. The measurements demonstrate that the capacitance of the capacitor varies between 0.79 pF and 0.96 pF as the applied bias voltage is increased, which accounts for a shift of 21%. The quality factor of the capacitor reaches a peak value of 45 at 1.25 GHz, illustrated in Figure 4.19.

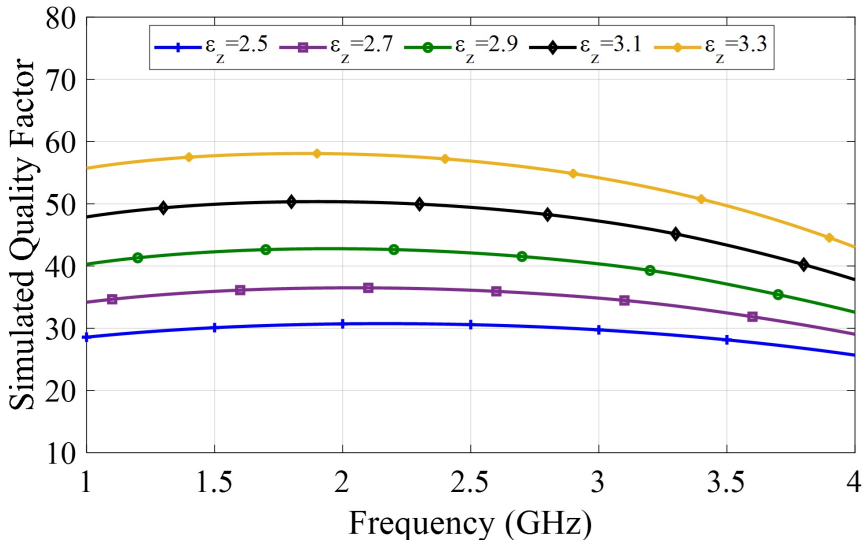


Figure 4.17: Simulation results of series capacitor with integrated bias line, quality factor vs frequency.

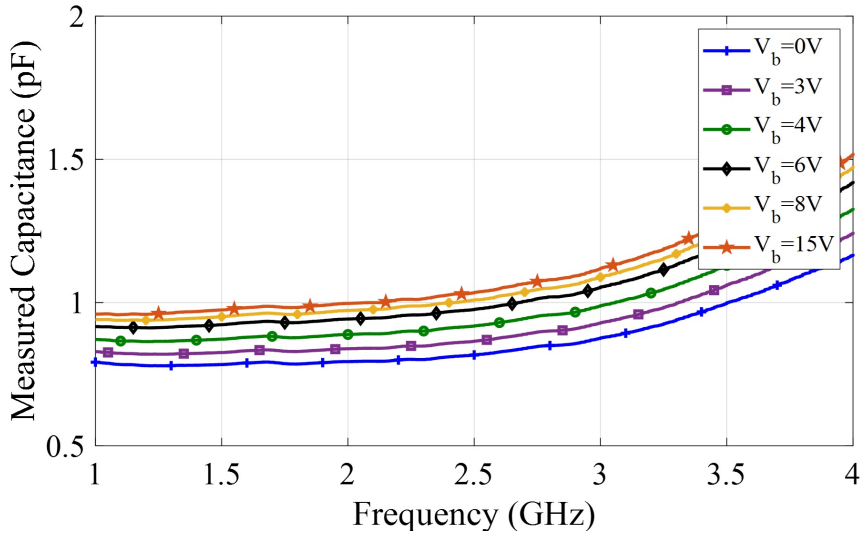


Figure 4.18: Measurement results of series capacitor with integrated bias line, capacitance vs frequency.

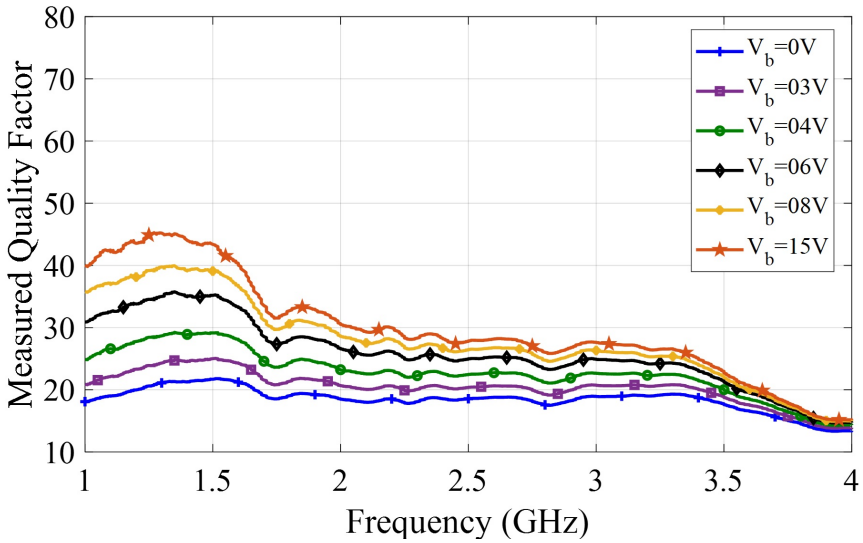


Figure 4.19: Measurement results of series capacitor with integrated bias line, quality factor vs frequency.

4.3 Series Capacitor

This section details the design and fabrication process of an LC-integrated series capacitor, tailored for applications where a series capacitor is indispensable, albeit without the necessity of isolating bias voltage from RF terminals. This capacitor assumes a crucial role in devices requiring series capacitors with high-quality factors. Demonstrating a notable 24% shift in capacitance and achieving a quality factor of up to 105 at 1 GHz, the capacitor's performance underwent comprehensive evaluation through measurement and simulation. Additionally, the capacitor features a 10 μm thin layer of LC material, contributing to lower control voltage requirements and faster response times.

4.3.1 Design Concept

The third device is a simple series capacitor fabricated entirely on high-resistivity silicon. Unlike the previous sample, the capacitance of this capacitor is controlled by grounding one pad and applying a bias voltage to the other pad. The design of this device is simpler compared to the previous one. Figure 4.20 presents a side view as well as a top view of both substrates, focusing on the perspective of the LC material.

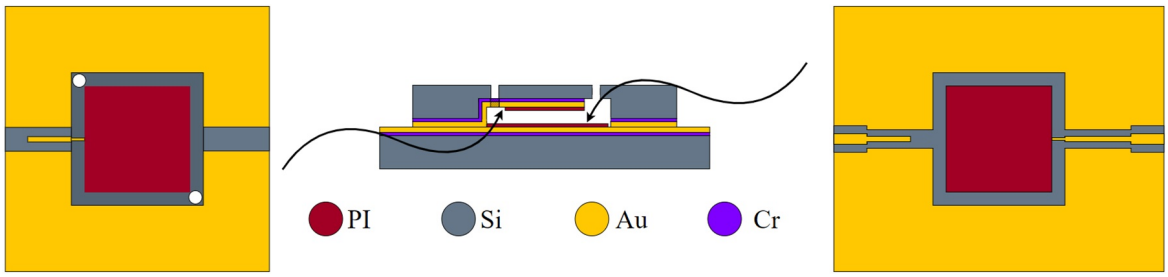


Figure 4.20: Design of the proposed LC-integrated simple series capacitor, side view (not to scale) and top view of two parts from LC material standpoint.

Upon closer inspection, it is indeed observed that the left input line is not directly connected to any plate. However, during the packaging step, this left input line will be connected to the transmission line patterned on the top substrate through an Au-Au bonding process. This bonding process ensures the proper electrical connection between the left input line and the corresponding plate in the device. In addition, Figure 4.21 offers a 3D view of this series capacitor.

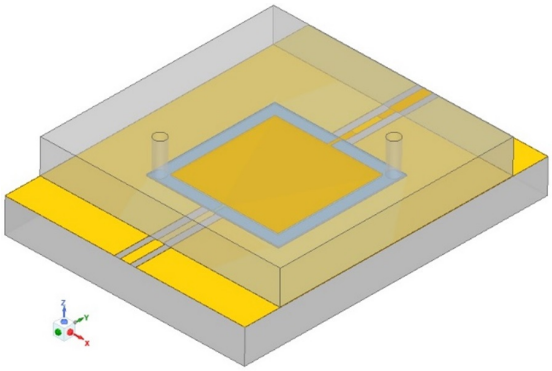


Figure 4.21: 3D view of the proposed simple series capacitor in Ansys Electronics Desktop software.

Compared to the shunt capacitor, this device has a smaller footprint. Additionally, this sample is fully silicon-made, fabricated in available clean room facilities.

4.3.2 Fabrication Process

As shown in Figure 4.22, the fabrication process for this device begins with photolithography and DRIE to create the filling holes. Another round of photolithography is required before DRIE etch of 10 μm and form the LC housing. After the cleaning process, a complete sputtering of chromium and gold is performed as the adhesion and seed layer, respectively, with thicknesses of 40 nm and 150 nm. It is important to note that one of the main transmission lines should be connected to the bottom surface of the created trench, making sidewall coverage crucial during the metallization process.

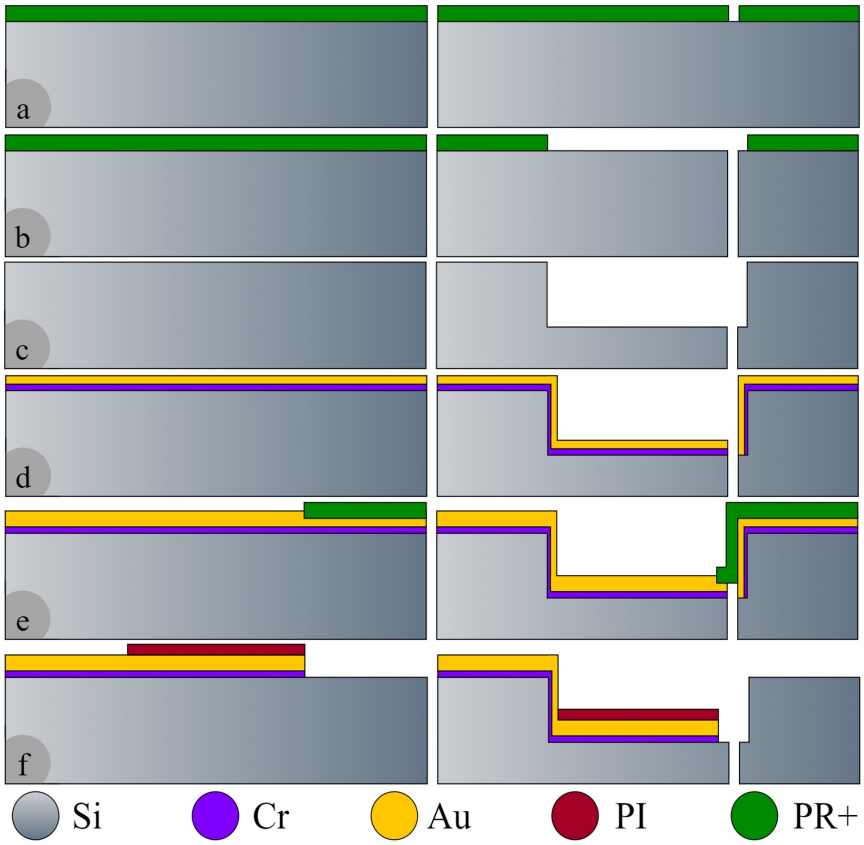
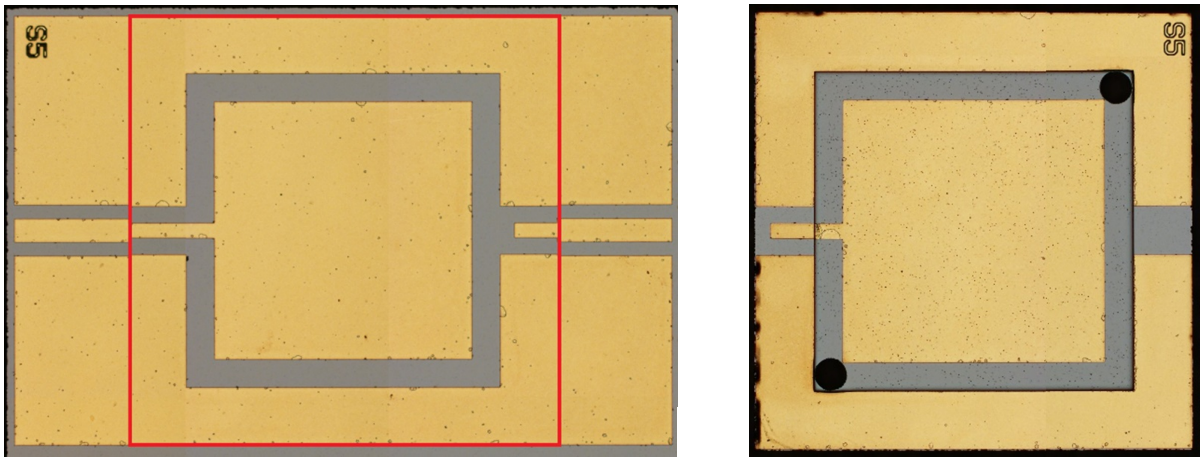


Figure 4.22: Fabrication process flow for developing LC-integrated micromachined series capacitor: (a) photolithography of positive PR, (b) etching through using DRIE, photolithography of positive PR, (c) etching 10 μm using DRIE and cleaning, (d) sputtering Cr and Au, (e) photolithography of positive PR, electroplating Au, (f) removing PR, Au and Cr wet etch, adding PI.



(a) (b)

Figure 4.23: Microscope images of the fully silicon made LC-based series capacitor, (a) bottom part and (b) top part.

Next, a photolithography process is carried out to cover the undesired areas before the gold electroplating. This ensures that the gold layer remains thin, allowing for its easy removal through a short wet-etching process. Electroplating is then conducted to increase the thickness of the gold layer to 2 μm. Since there are no sensitive structures like meander resistor lines, isotropic etch processes such as wet etching can be employed. Initially, a gold etch is performed to remove the gold seed layer, followed by a chromium wet etch to eliminate the adhesion layer from the undesired areas. Subsequently, a thin layer of PI is added to cover the capacitor's plates. This layer requires a curing process to remove any remaining solvent. At this stage, the samples are ready to be diced and undergo the surface treatment process as explained earlier.

4.3.3 Fabricated Device

Figure 4.23a provides a microscope image of the fabricated bottom part of the device. Both transmission lines are extended as CPWs for measurement purposes. However, in this substrate, only one input line is directly connected to the plate. The other one will be connected to the transmission line visible in Figure 4.23b. This image shows the top part of the device, where there is a square trench with dimensions of 1×1 mm^2. The capacitor plate is placed within this etched trench, measuring 0.8×0.8 mm^2. A narrow line

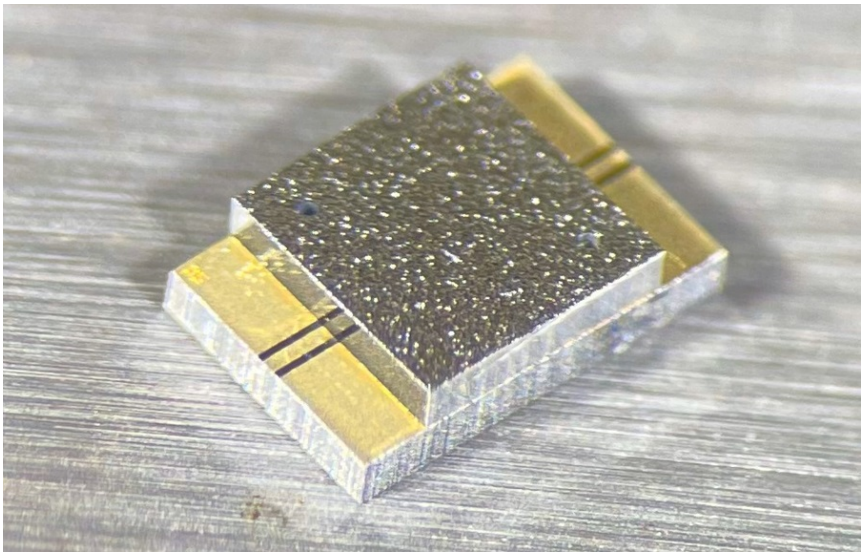


Figure 4.24: Microscope image of the fully silicon made LC-based series capacitor with extended input.

extends from this plate and connects it through the sidewall to the other surface where the connection transmission line is situated. The filling holes can also be observed in the two far end corners of the housing. The red square drawn on the diagram indicates the area where the top part sits on the bottom part during the packaging process.

The device is packaged using a similar process to that used for the capacitor with the integrated bias line. Figure 4.24 showcases the final packaged device, providing a comprehensive 3D perspective of the fabricated device. The overall dimensions of this device, including the extension transmission lines, are 1.4×1.9 mm^2. Since this device is made on high-resistivity silicon, its height is noticeably shorter, measuring 0.562 mm.

4.3.4 Results

Since the plates of this capacitor have a larger area compared to the previous capacitor with the integrated bias line, it is expected that the capacitance would be larger. The ElectroMagnetic (EM) simulation results presented in Figure 4.25 align with this expectation, as the capacitance varies between 2.03 pF and 2.59 pF, representing an approximate 27% variation.

The quality factor increases with permittivity, as expected based on the LC material's

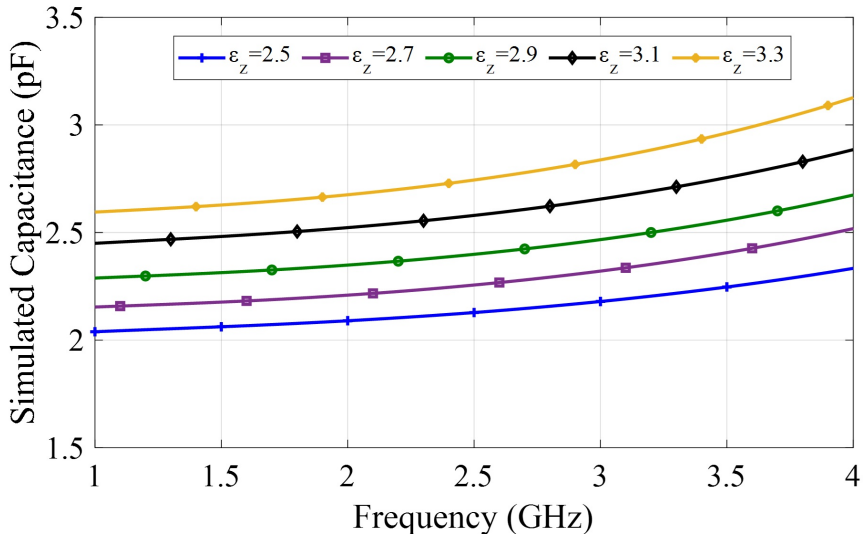


Figure 4.25: Simulation results of series capacitor, capacitance vs frequency.

behavior, presented in Figure 4.26. It peaks at 115 at 1.5 GHz when the permittivity is at its highest. The quality factor also declines as the frequency increases and eventually reaches zero at the resonant frequency.

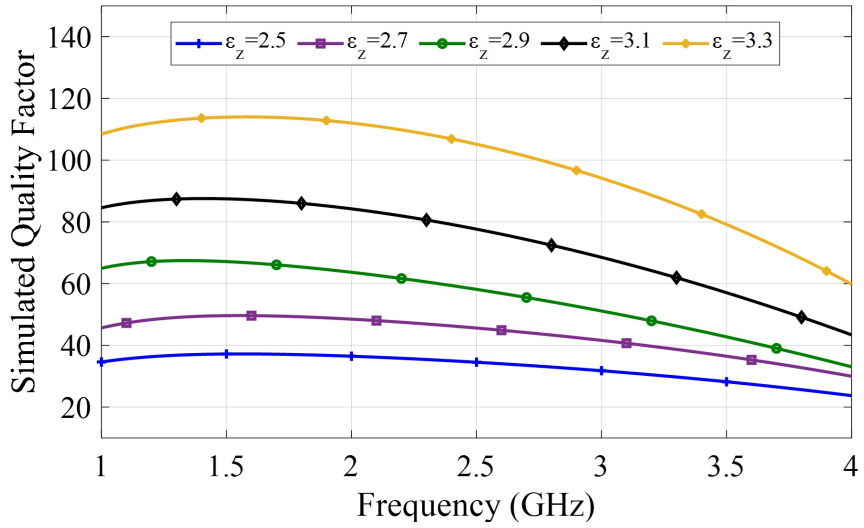


Figure 4.26: Simulation results of series capacitor, Q factor vs frequency.

The measurements of the simple series capacitors were conducted using two 150 μm

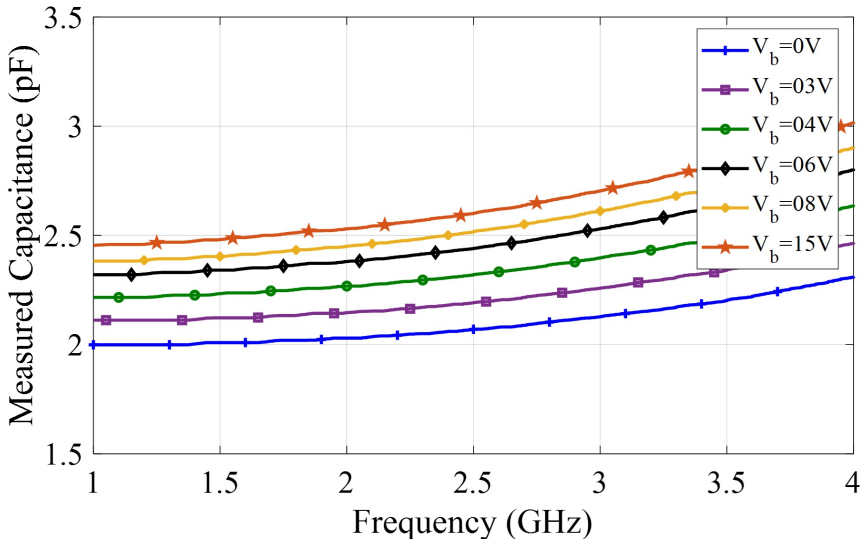


Figure 4.27: Measurement results of series capacitor, capacitance vs frequency.

pitch probes and bias tees on both terminals of the Vector Network Analyzer (VNA). One input line was grounded DC, while the bias voltage was applied to the other input. The measurement results shown in Figure 4.27 indicate that changing the bias voltage from 0 V to 15 V results in a corresponding change in capacitance from 1.99 pF to 2.45 pF, representing a 23% variation.

Additionally, the quality factor exhibits changes with the applied bias voltage in Figure 4.28. At 0 V bias, it reaches a value of 22, while at the maximum applied voltage of 15V, it peaks at 105. The overall behavior follows the simulation results.

4.4 Summary

This chapter presents a comprehensive investigation into the design, fabrication, simulation, and measurement of single-chip silicon micromachined variable capacitors utilizing nematic LC. The study focuses on three distinct capacitor configurations: a shunt capacitor, a series capacitor with an integrated bias line, and a series capacitor.

The entire fabrication process was conducted in-house utilizing meticulous techniques such as multiple photolithography steps, multiple DRIE processes, sputtering deposition, Ion Milling dry etching, metal wet etching, electroplating, and thorough cleaning procedures. A significant aspect of the process involved the utilization of an IBI system for

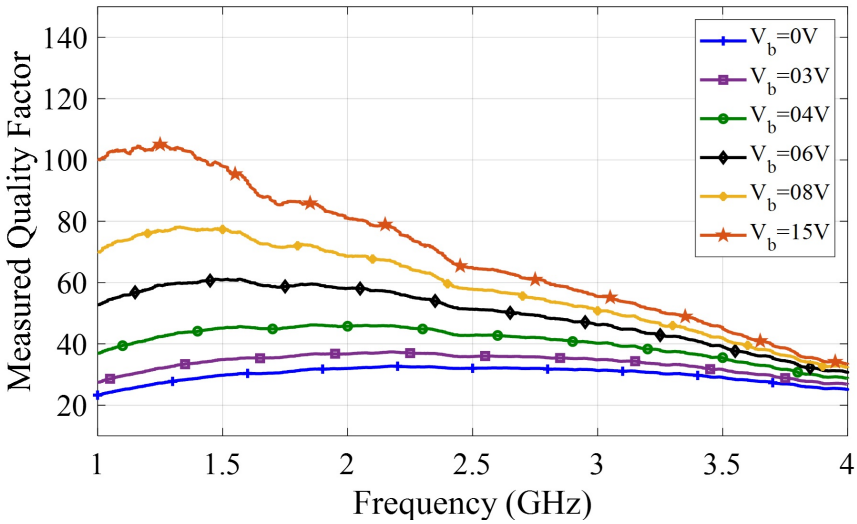


Figure 4.28: Measurement results of series capacitor, Q factor vs frequency.

precise surface treatment of the pre-alignment layer, which is essential when dealing with highly miniature LC-based devices. Furthermore, a meticulous die bonding process was employed, ensuring low-temperature Au-Au bonding and resulting in the production of robust and reliable final devices.

This research involved the fabrication and measurement of more than 20 samples, consistently yielding reliable results. The experimental results clearly demonstrate the effectiveness of the designed silicon-micromachined variable capacitors in achieving reasonably good high-quality factor tunable capacitors at the chip level. The shunt capacitor exhibited an 18% shift in capacitance with a variable quality factor ranging from 44 to 123. The series capacitor, which features an integrated bias line for ease of integration with RF circuits, further improved the variable range to 21% and demonstrated a quality factor ranging from 22 to 45. In the case of the other series capacitor, a 23% variation in capacitance was observed with a quality factor ranging from 32 to 105. It is noteworthy that these two series capacitors incorporate a 10 times thinner LC material, which offers advantages in terms of reducing the maximum applied voltage required for tuning. It is important to highlight that these variable capacitors exhibit almost zero power consumption, as the creation of an electric field between the capacitor plates does not draw any current.

In conclusion, the fabricated silicon-micromachined LC-based variable capacitors have the potential for use in various RF applications that demand analog tuning, particularly in scenarios where low power consumption is crucial, including but not limited to tunable

filters, phase shifters, impedance tuners, and tunable matching networks. The achieved performance improvements, as demonstrated through the experimental results, provide new opportunities for the development of new devices with enhanced performance and increased flexibility. These variable capacitors offer promising solutions for achieving precise tuning and optimization in RF circuits, paving the way for advancements in wireless communication systems, RF front-end modules, and other RF applications. Their ability to deliver high-quality factor and low power consumption makes them highly desirable for next-generation wireless communication technologies. The presented fabrication process can be carried-out on large wafer of size 8" or 12" to produce thousands of single-chip variable capacitors using a single fabrication run. Using the proposed fabrication process, a single-chip capacitor operating at millimeter-wave frequencies can be constructed. However, the dimensions and input measurement lines must be significantly reduced; otherwise, the resonance frequency may degrade the performance of these capacitors. These capacitors are integrated into mm-Wave tunable reflective loads, as discussed in Chapter 6. To our knowledge, this is the first-time miniature single-chip LC-based variable capacitors are ever reported.

Chapter 5

Liquid Crystal Integrated Waveguide Tunable Filter

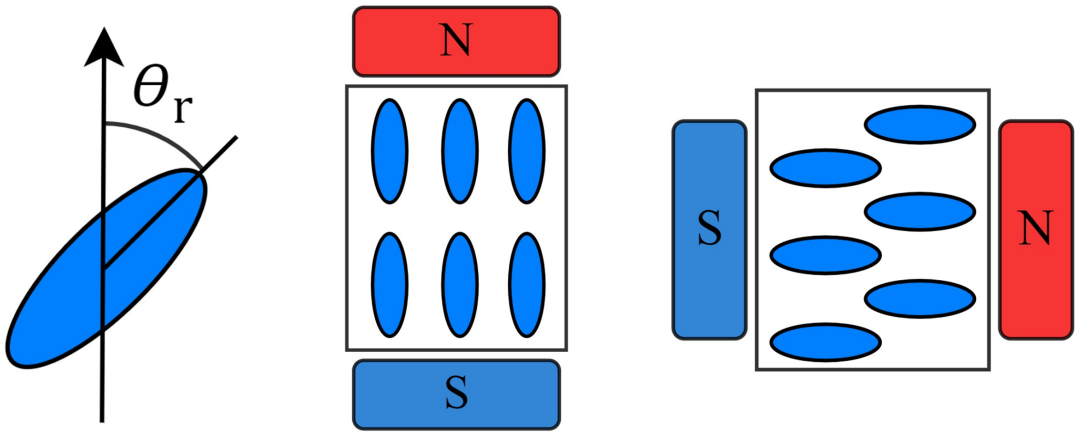
Modern communication systems, including systems such as cognitive radios and software-defined radios, require highly efficient usage of the frequency spectrum. Tunable filters play a crucial role in achieving this efficiency by allowing for the reconfiguration of communication systems. To achieve tunability, various technologies such as MEMSs, semiconductors, BST, PIN diode, graphene, and liquid crystals can be employed.

Although MEMS-based tunable filters offer a small size and low insertion loss, their reliability, lifetime, and cost pose significant limitations [79, 80, 81, 82, 83, 84]. In addition, MEMS only provides discrete tunability. On the other hand, diodes offer fast switching times, but their excessive loss in higher frequencies is a drawback [85, 86]. Liquid crystals [87, 48] and graphene [88, 89], have shown promising performance in higher frequency ranges compared to diodes and BST [90, 91, 92]. Using a liquid crystal that exhibits a low loss tangent in reconfigurable devices such as filters can help address issues related to nonlinearity, reliability, high loss, and lifetime while having analog tunability [59]. However, despite the potential advantages of liquid crystals, their development and optimization for use in tunable devices is still an active research area. To enable their practical applications in wireless communication systems, key challenges include quality factor and size reduction need to be addressed.

This chapter presents the development of a tunable waveguide filter utilizing LC material integrated within quartz glass tubes where the LC material is actuated by a static magnetic field. The proposed filter demonstrates a 7% tuning range with a minimal bandwidth variation. Experimental results are presented for a 7.5 GHz filter with a bandwidth

of 2.5%, confirming the viability of the concept. The filter incorporates a single tuning element employing only one pair of magnets to reduce tuning complexity and improve reliability.

5.1 Operation Concept



(a) (b) (c)

Figure 5.1: Liquid crystal molecules orientation in nematic phase, (a) axial angle, (b) parallel state, and (c) perpendicular state.

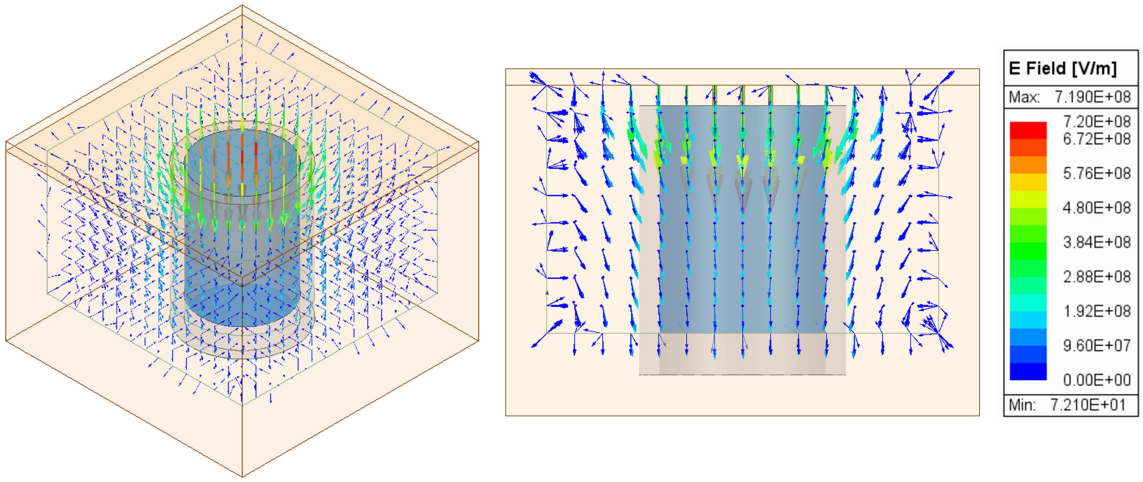
The anisotropic behavior of LC materials in the nematic phase offers the potential for their utilization in tunable devices. Specifically, the uniaxial anisotropy of LC molecules generates different electromagnetic properties along distinct axes. Along the long axis of LC molecules, these materials display $\varepsilon_{\parallel}$ and $tan\delta_{\parallel}$, whereas along the other two axes, they exhibit $\varepsilon_{\perp}$ and $tan\delta_{\perp}$. It is important to note that the tensor representing the dielectric properties of LC materials is orientation-dependent. Notably, a distinctive characteristic of LC materials is their lowest loss when they exhibit their highest dielectric constant. In the present study, we employ GT3-23001 LC material with properties of $\varepsilon_{\perp}$=2.5, $tan\delta_{\perp}$=0.0138, $\varepsilon_{\parallel}$=3.3, and $tan\delta_{\parallel}$=0.0038.

In Figure 5.1a, a detailed view of an LC molecule is presented. For the sake of clarity and reference later in this chapter, the angle difference between the Z-axis and the long axis of the LC molecules is denoted by θ_r. To manipulate the orientation of LC molecules, a static electric or magnetic field must be applied. In the presence of such a field, LC

molecules align themselves along its direction, and altering the direction of the applied field would subsequently alter the dielectric properties of the material.

5.2 Device Design

Since the electrical field is concentrated in the center, confining the LC material within the central region of the resonator would yield the maximum possible variation in resonance frequency. This is evident by the observation of electrical field distribution inside the resonator as depicted in Figure 5.2. To accomplish this confinement, a material with a low dielectric constant and loss tangent must be employed. For this purpose, a quartz glass (also known as fused silica) tube is utilized in this study, with a dielectric constant of 3.77 and a loss tangent of 0.0001 at 10 GHz.



(a) (b)

Figure 5.2: Simulated electric field distribution inside the resonator that includes LC and quartz tube, (a) 3D view, (b) side view.

A 2 mm deep notch is incorporated into the cavity bottom wall to stabilize the tubes, with an additional 1 mm gap at the top for ease of assembly. It is important to highlight that volume of the LC material used significantly impacts the Q factor, due to its higher loss factor in comparison to air. Increasing the volume of LC material extends the tuning range at the expense of a lower Q factor. Therefore, a trade-off must be made between the tuning range and the Q factor.

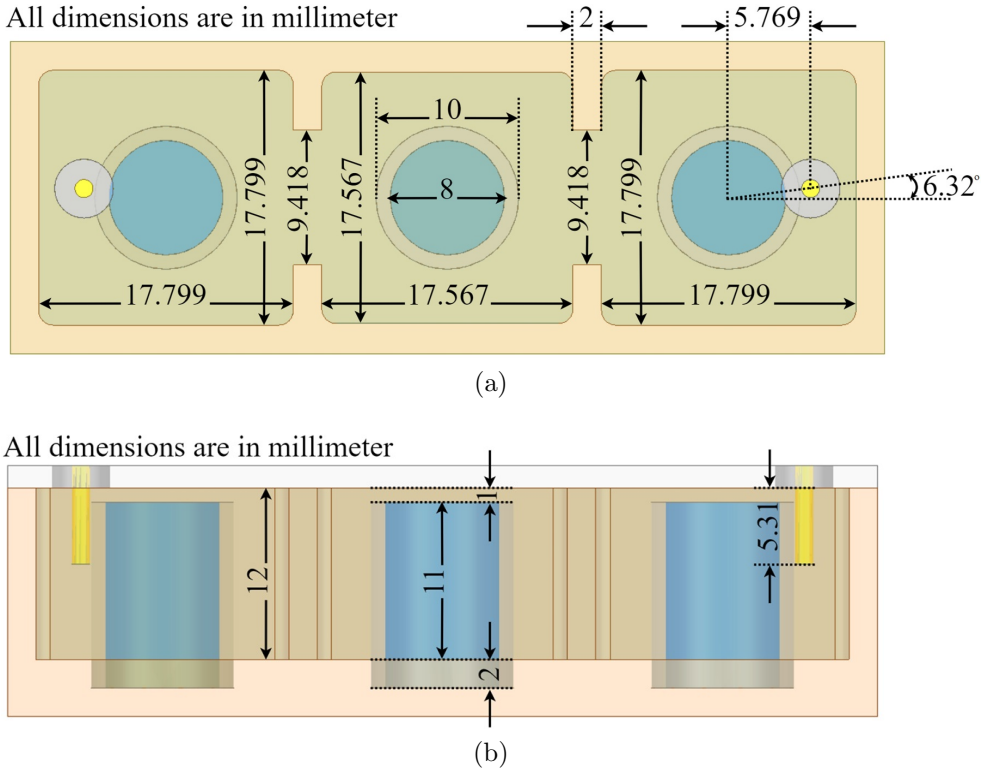


Figure 5.3: Designed tunable filter with dimensions, (a) top view and (b) side view.

The design of this filter follows the coupling matrix method [68], which involves determining the appropriate cavity dimensions, followed by calculating the corresponding coupling factor, $k_{i,j}$, to determine the iris width between resonators. Each resonator must then be adjusted after the placement of the adjacent resonator with an open iris to match the center frequency. Figure 5.3 depicts the designed filter in top, side, and 3D views, with detailed dimensions of the filter's resonators, quartz glass, and probes. An important consideration during the design process to maintain a constant absolute bandwidth over the tuning range, is ensuring that the product of the physical inter-resonator coupling factor and the center frequency $k_{1,2} \times f_r$ exhibits a minimal variation over the tuning range. Figure 5.4 displays the simulated $k_{1,2} \times f_r$ versus frequency for different LC orientations.

Input/output coupling in this filter is achieved through the use of an SubMiniature version A (SMA) probe. For constant absolute bandwidth, it is also important for the reflected group delay of the first and last resonators to remain constant over the tuning range. The employed input/output coupling mechanism, as depicted in Figure 5.3a-b, has

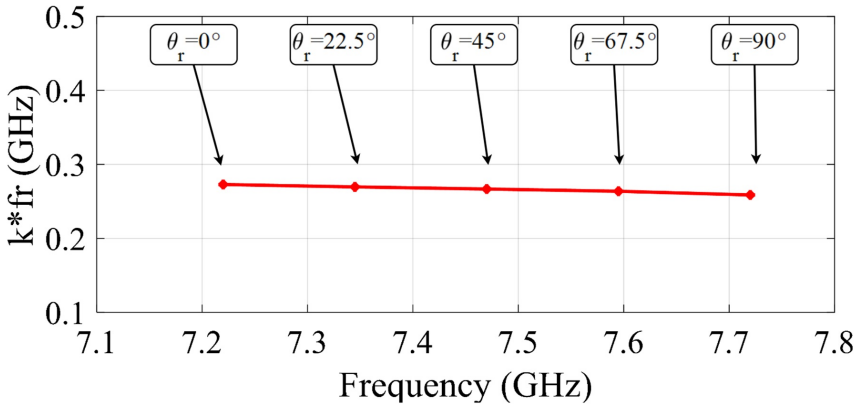


Figure 5.4: Iris coupling with constant $k_{12} \times f_r$ over the tuning range.

three degrees of freedom: pin length, distance from the center of the quartz glass tube, and rotation around the center of the tube. Simulated group delay versus different LC material orientations shows variation between 1.8 ns to 2.2 ns, presented in Figure 5.5.

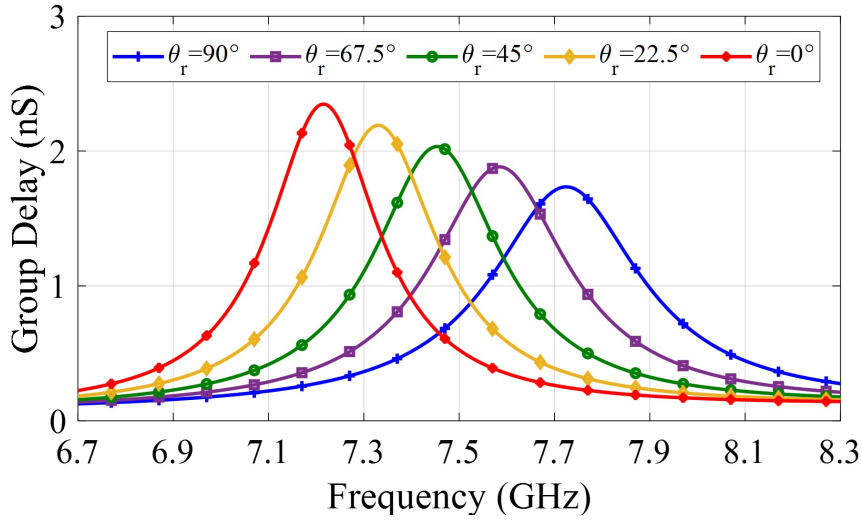


Figure 5.5: Simulated input group delay of the resonator in different states of the utilized LC.

To enable tuning of the filter, it should be constructed from a magnetic field penetrable material, such as copper. This will allow for the use of a static magnetic field to change the orientation of the LC molecule (θ_r). If the magnetic field is applied from the sides, the LC material will align horizontally, resulting in the maximum achievable frequency.

Conversely, applying the field from the top and bottom will result in the vertical alignment of LC molecules and the minimum resonance frequency.

Table 5.1: Tensor representation of employed LC material, used in simulations, along with u assuming lossless and lossy LC.

	θ_r=90° (perpendicular)	θ_r=67.5°	θ_r=45°	θ_r=22.5°	θ_r=0° (Parallel)
ε	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 3.3 & 0 \\ 0 & 0 & 2.5 \end{bmatrix}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 3.1 & 0 \\ 0 & 0 & 2.7 \end{bmatrix}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 2.9 & 0 \\ 0 & 0 & 2.9 \end{bmatrix}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 2.7 & 0 \\ 0 & 0 & 3.1 \end{bmatrix}$	$\begin{bmatrix} 2.5 & 0 & 0 \\ 0 & 2.5 & 0 \\ 0 & 0 & 3.3 \end{bmatrix}$
$tan\delta \times 10^3$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 3.8 & 0 \\ 0 & 0 & 14.3 \end{bmatrix}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 6.4 & 0 \\ 0 & 0 & 11.7 \end{bmatrix}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 9.1 & 0 \\ 0 & 0 & 9.1 \end{bmatrix}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 11.7 & 0 \\ 0 & 0 & 6.4 \end{bmatrix}$	$\begin{bmatrix} 14.3 & 0 & 0 \\ 0 & 14.3 & 0 \\ 0 & 0 & 3.8 \end{bmatrix}$
Lossless LC Q_u	5484	5516	5544	5569	5580
Lossy LC Q_u	135	160	199	271	430

To accurately simulate this filter in Ansys Electronics Desktop software, rotating the LC material tensor for each state is essential. This rotation leads to the utilization of five different dielectric constant and loss tangent tensors based on θ_r (see Figure 5.1a) for presented results. Table 5.1 represents the exact tensor values of dielectric constant and loss tangent that has been used in simulations for each state. This is necessary because the effect of the uniaxial properties of the LC material depends on field orientation. The insertion of the quartz tube and LC material reduces the filter's overall volume by 61%. This reduction in size comes with a trade-off, resulting in a decrease in the unloaded Q factor from 7000 to a range between 430 and 135. Please note that if the LC material is assumed to be lossless, the quality factor would be approximately 5500. However, the addition of $tan\delta$ significantly reduces the quality factor, as shown in Table 5.1.

Figure 5.6 depicts the simulated response of the proposed LC-integrated tunable filter with respect to varying axial angles of the LC molecules inside the quartz tube. Additionally, simulation results in Figure 5.7 ensure small variation of both bandwidth and insertion loss with respect to the center frequency. The bandwidth variation is observed to be 10% while insertion loss varies from 0.98 dB to 2.5 dB over the range of 7.22 GHz to 7.72 GHz.

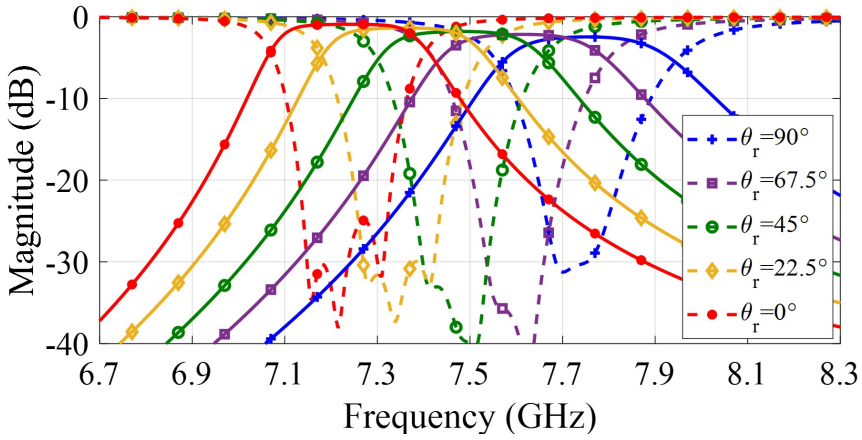


Figure 5.6: Simulated frequency response of the filter, including reflection coefficient (S11), and transmission coefficient (S21).

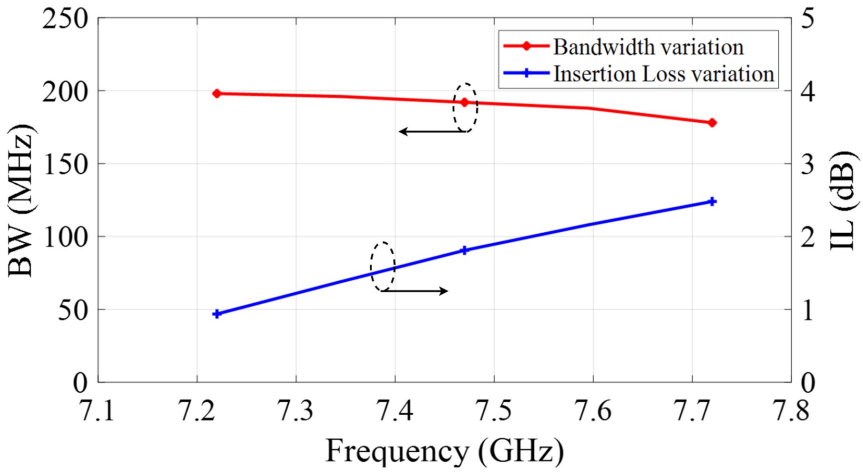
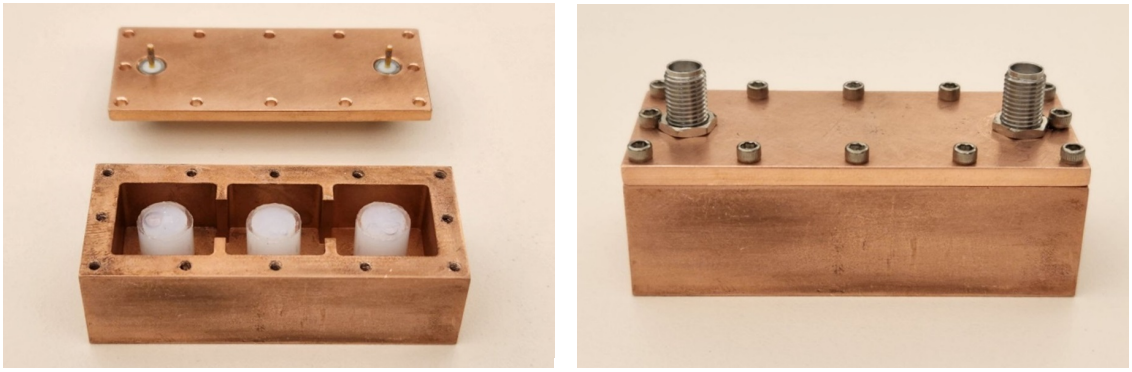


Figure 5.7: Simulated bandwidth and insertion loss variation versus center frequency.

5.3 Measurement Results

Figure 5.8 presents photographs of the prototype unit that was fabricated to validate the proposed design, with overall dimensions of $67\times27\times17$ mm^3. The main housing is made of copper to allow for magnetic field penetration. For the top part, a copper sheet is also utilized, where the input/output probes are screwed in a threaded hole to enable fine tuning of the input.



(a) (b)

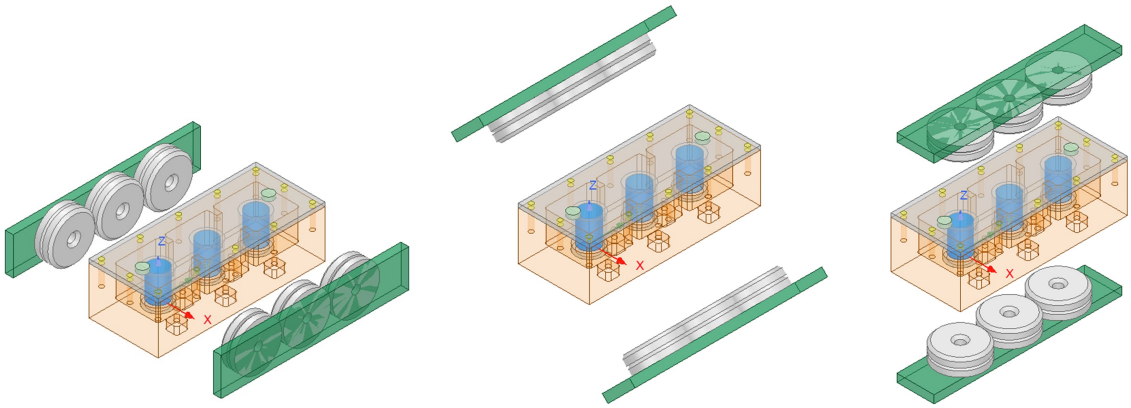
Figure 5.8: Fabricated prototype filter, (a) 3 fused silica tubes filled with LC and (b) complete packaged device.

The primary method employed to tune this filter involved the utilization of a pair of permanent magnets. Each set comprised 9 rare-earth magnets arranged in a 3 by 3 configuration. This arrangement served dual purposes: firstly, to impact all three resonators simultaneously, and secondly, to enhance the static magnetic field intensity. During the measurement process, the magnet pair was rotated around the fabricated sample. Figure 5.9 illustrates the positioning of this pair.

To achieve a state where $\theta_r = 90°$, signifying the maximum center frequency, the pair of magnets is positioned on the sides of the filter (Figure 5.9a). Conversely, to attain the minimum center frequency, the pair should be placed on the top and bottom of the filter. This configuration aligns the LC molecules with $\theta_r = 0°$ (Figure 5.9c). Intermediate states are achieved by rotating the pair of magnets around the filter. For instance, Figure 5.9b illustrates the $\theta_r = 45°$ state.

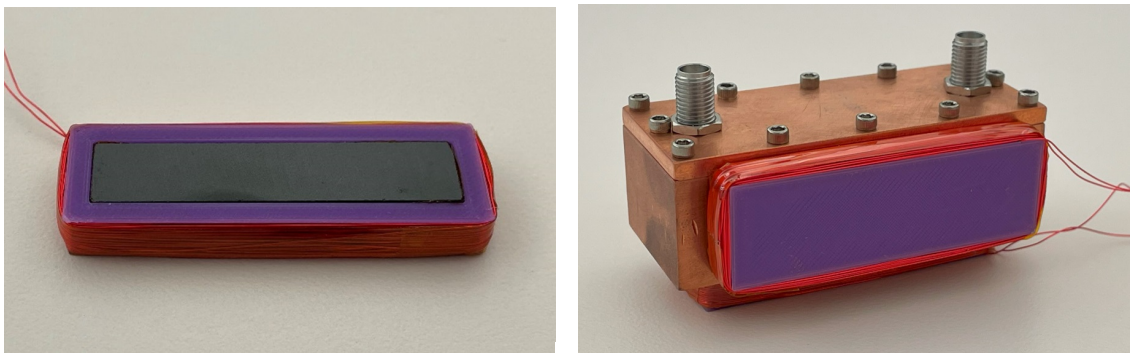
An alternative approach involves employing two coil magnets affixed to the bottom and sides of the filter. These coil magnets measure $12{\times}12{\times}65\ mm^3$, with a hollow space created to accommodate a ferrite magnet, as depicted in Figure 5.10a. The inclusion of a ferrite core enhances the magnetic flux density, thereby improving the effectiveness of the coil magnets. The coils consist of over 300 rounds wound with insulated wire measuring 0.098 inches in diameter.

For tuning purposes, activating the side coil magnets aligns the LC molecules in the Y direction, corresponding to state 1 in Table 5.1, which results in the highest center frequency when a perpendicular state is required. Conversely, activating the bottom coil while



(a) (b) (c)

Figure 5.9: Three different configurations of one pair of permanent magnets that has been used for measurement purposes, (a) $\theta_r = 90°$, (b) $\theta_r = 45°$, and (c) $\theta_r = 0°$.



(a) (b)

Figure 5.10: Tuning with coil magnets, (a) a single coil magnet with ferrite core and (b) fabricated filter with a pair of coil magnet attached to side and bottom.

disconnecting the side one reduces the resonance frequency to its lowest within the tuning range, representing state 5 in Table 5.1, when a parallel state is desired. To achieve states between these extremes, the applied current to each coil must be meticulously adjusted to establish a net static magnetic field along the desired direction. Figure 5.10b presents an image of the fabricated coil magnets attached to the proposed filter. It is important to note, however, that the tuning speed of these coil magnets is slower compared to that of a pair of permanent magnets.

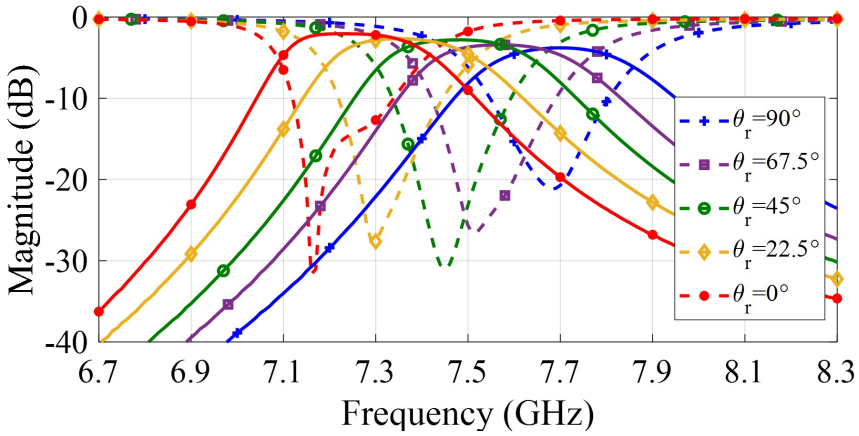


Figure 5.11: Measured frequency response of the filter, including reflection coefficient (S_{11}), and transmission coefficient (S_{21}).

Figure 5.11 shows the measured S-parameters of the prototype unit in five different states of the LC material. The tuning range measured is from 7.21GHz to 7.69 GHz, (i.e., 7%). Insertion loss varies between 2 dB at the start of the tuning range to 3.7 dB at the very end. The increased insertion loss is due to the surface roughness and possible fabrication precision. The measured quality factor varies from 115 to 288 with a resonator volume of 3703 mm^3.

Table 5.2: Summary of state-of-the-art liquid crystal integrated tunable band pass filters.

Work	Technology	Tuning Mech.	f(GHz)	FBW	τ_{f_c}	Order	IL(dB)	Q
[48]	GGW	E&M field	30	1%	3.4%	2	1.65-1.95	Up to 300
[93]	Microstrip	SA&E field	33	10%	5.7%	3	4.5	NA
[94]	Waveguide	E field	20	1%	2.3%	3	7.5	170–256
[95]	Microstrip	SA&E field	5	16.6%	13.4%	2	3-5	NA
[96]	SIW	M Field	22	3.18%	2.8%	3	6	73–75
[7]	HMCSIW	SA&E field	16.5	3.9%	3.8%	2	3.4	NA
[6]	NRD	E field	60	1%	2.9%	3	4.2-6.2	96–141
[97]	Waveguide	E field	30	1%	3%	2	3.5-4.2	NA
This work	Waveguide	M field	7.5	2.6%	7%	3	2-3.7	115–288

Table 5.2 shows a comparison of various state-of-the-art band pass LC-based filters employing different LC actuation technologies. The main advantage of current filter is wide tuning range of center frequency (7%) maintaining a relatively low insertion over a small bandwidth of (2.5%). In [8], a higher tuning range is achieved, but insertion loss is high considering the wide fractional bandwidth in that design.

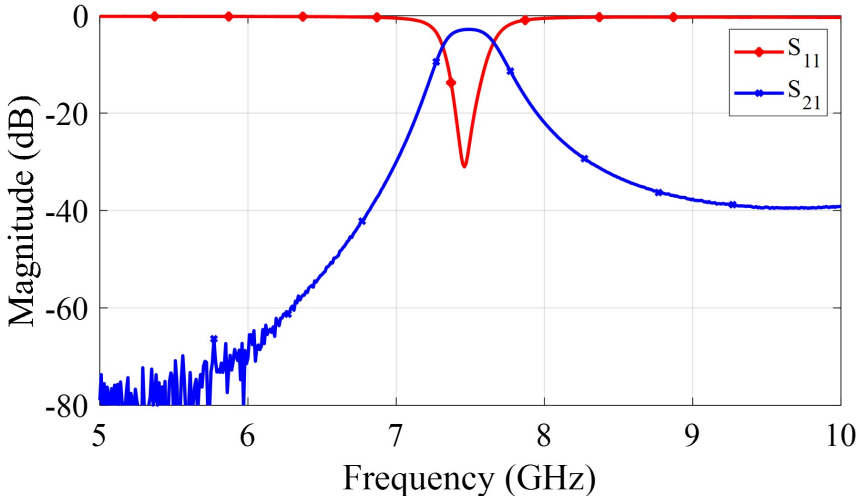


Figure 5.12: Measured frequency response of the filter over a wide span.

Confirming the effectiveness of the filter involves ensuring a clean wide-span response devoid of any unintended transmissions. This validation guarantees the prevention of unwanted signals in actual communication systems utilizing this filter. Figure 5.12 illustrates precisely such a clean wide-span frequency response spanning from 5 GHz to 10 GHz.

5.4 Summary

This chapter has presented the design, simulation, fabrication, and measurement results of an LC-integrated tunable waveguide filter operating at 7.5 GHz. The filter is tunable by controlling the orientation and properties of the LC material using a static magnetic field. The simulation and measurement results show a reasonably constant bandwidth over the tuning range, and the fabrication results are within a good margin of the simulation.

The methodology proposed in this study, which involves utilizing a magnetic field to manipulate the orientation of the LC material and enclosing the tunable material within a fused silica tube, can be utilized to design tunable filters for a diverse range of frequencies and applications with the same accuracy and performance. In particular, this approach is well-suited for applications involving 5G mm-Wave base stations using micromachining technologies. The results of this investigation can be leveraged to enhance the design and performance of future LC-based tunable filters.

Chapter 6

Liquid Crystal Integrated Millimeter Wave Devices

Tunable components constitute essential elements in a wide range of microwave and mm-Wave applications. In recent times, there has been a notable increase in the demand for phase shifters, particularly within the mm-Wave frequency band. These phase shifters play a crucial role as fundamental building blocks in communication systems, especially in phase array systems. To achieve excellence, phase shifters must demonstrate essential attributes such as minimal insertion loss, an extensive tuning range, elevated linearity, and a compact physical footprint. The incorporation of analog tunability could offer an additional advantage, ensuring optimal performance and precision in communication systems. The integration of these features is expected to lead to a significant reduction in the complexity of communication systems.

Both semiconductor analog and switched capacitors are viable options for integration into tunable mm-Wave devices [98, 99]. While extensive research has been conducted over the past two decades on the development of switched capacitors using MEMS [71, 100, 101] and PCM technologies [102, 103, 104], these capacitors present a constraint in terms of available states. This limitation restricts their applicability in various contexts where analog tuning is essential for optimal performance.

In recent years, a considerable number of papers have been published, centering on LC-based tunable devices [6, 75, 76]. However, within these studies, the integration of LC frequently included sizeable RF structures, aiming to facilitate handling and the pre-alignment procedures of liquid crystal. Results of Chapter 5 which was published recently showcased the performance of LC-based chip capacitors using silicon micromachin-

ing techniques. This chapter introduces a compact chip-scale tunable reflective load and a complete RTPS achieved through a cleanroom fabrication process that utilizes silicon-micromachining technology and incorporates an IBI procedure for pre-alignment.

6.1 LC-Based Reflective Loads

This section introduces two monolithically integrated reflective load employing liquid crystal material as a reconfigurable element for phase shifter applications. The LC material is confined within a micromachined space, and its dielectric properties are controlled through an applied bias voltage. These tunable reflective loads finds applicability in RTPSs. Operating at a frequency of 28 GHz and 62 GHz, the reflective loads exhibits a phase variation of 113° and 118°, respectively, as the bias voltage ranges from 0V to 25V. The 28 GHz and 62 GHz devices demonstrate a reflective insertion loss of 3.9 dB and 4.3 dB, indicating a Figure of Merit (FOM) of 29°/dB and 27.5°/dB, respectively. Fabrication of these devices is conducted in-house using a multi-layer microfabrication process. To the best of our knowledge, this marks the first time a fully silicon-made, chip-level LC integrated reflective load is presented.

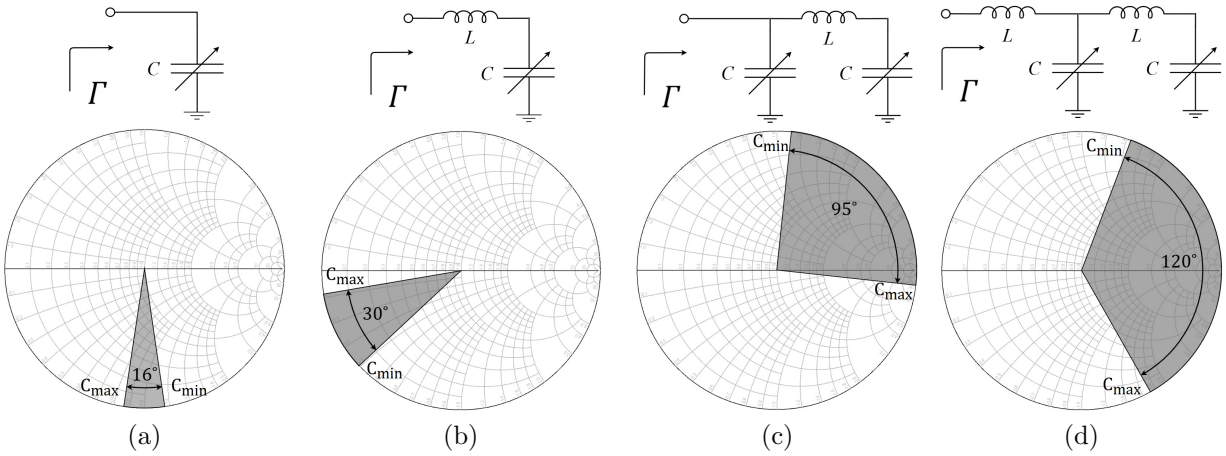


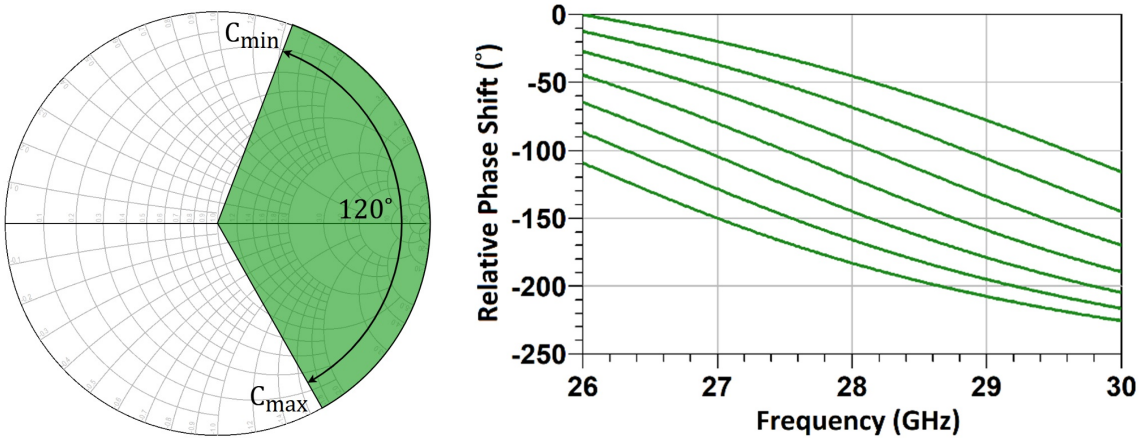
Figure 6.1: Comparison of the simulated reflective loads for different configurations, Smith charts are at 28 GHz, (a) single capacitor, (b) inductor and capacitor connected in series, (c) two shunt capacitors and a series inductor in π configuration, and (d) an inductor in series with π configuration.

6.1.1 Design Principle

The LC-based capacitor holds promise for application in a RTPS. In this configuration, the load comprises an LC-based capacitor and a length of high-impedance CPW transmission line acting as an inductor. To ascertain the optimal loading configuration, four distinct types of reflective loads, comprising shunt capacitors and series inductors, underwent investigation at 28 GHz. The obtained results serve as valuable insights for designing similarly structured devices operating at 62 GHz. The incorporation of shunt capacitors simplifies the biasing scheme and potentially yields higher Q values, thereby facilitating the creation of simpler and lower-loss devices. The results of this analysis are depicted in Figure 6.1, taking into account a 30% tuning range of the LC-based capacitor.

Figure 6.1a illustrates the basic reflective load comprising only a variable capacitor. The tuning range is notably limited, reaching 28 GHz with a phase shift $\Delta\theta$ of 16°. Introducing an inductor in series and a shunt capacitor, as depicted in Figure 6.1b and Figure 6.1c, extends the phase shift range to 30° and 95°, respectively. While these configurations exhibit higher phase shifts than a single capacitor, they still require improvement. The proposed configuration, shown in Figure 6.1d, achieves a maximum phase shift of 120° at 28 GHz, with a consistent phase shift across the bandwidth.

Utilizing the topology as depicted in Figure 6.1d, a circuit simulation of the proposed phase shifter is presented in Figure 6.2. This simulation utilizes L1 = 50 pH, C1 = 75 fF



(a) (b)

Figure 6.2: Phase shift performance of the proposed reflective load, (a) reflection coefficient on Smith chart at 28 GHz and (b) relative phase shift over the frequency band.

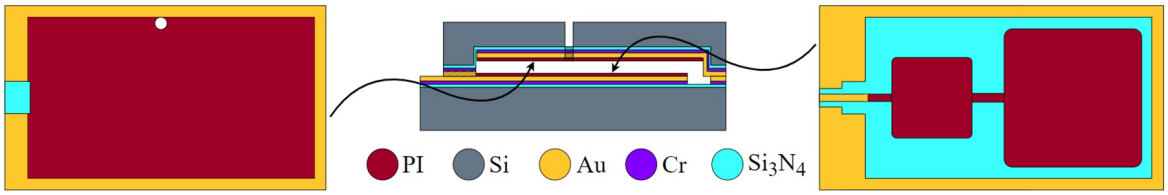


Figure 6.3: Structure of the proposed LC-based chip tunable reflective load at 28 GHz, top, side, and bottom view.

to 95 fF, L2 = 140 pH, C2 = 145 fF to 180 fF. The results reveal a maximum phase shift inconsistency of 12°, with a 120° phase shift observed at 28 GHz.

Various perspectives of the proposed 28 GHz device are depicted in Figure 6.3. The bottom substrate incorporates the inductors, input line, and one plate of each capacitor. The top substrate contains the housing for the LC material, which has been etched into the silicon. The encapsulation area is formed through a flip-chip process that joins the two substrates together. The filling hole with a diameter of 100 μm is carefully placed in the top substrate within the LC trench area. This will facilitate the filling process using vacuum chamber and avoids any leak of LC material before sealing of filling hole.

The reflective load operating at 62 GHz follows a design procedure similar to that of the 28 GHz counterpart. While maintaining a similar structure, the device employs different capacitor and inductor values to meet the specifications required for the higher frequency. Following parameters can be determined for the 62 GHz reflective load: L1 = 270 pH, C1 = 67 fF to 85 fF, L2 = 180 pH, C2 = 53 fF to 68 fF. Figure 6.4 provides a view of the top substrate, side view, and bottom substrate from the perspective of the LC material in the 62 GHz reflective load.

It is important to note that the overall dimensions of the reflective load at 62 GHz are smaller than those at 28 GHz. Consequently, while the filling hole in both devices has the same diameter, it appears smaller in the lower frequency device. For reference, despite the

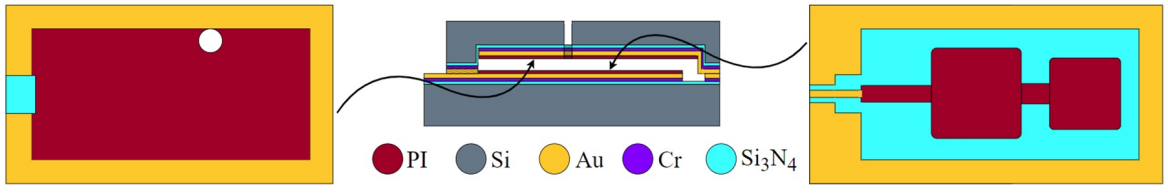


Figure 6.4: Structure of the proposed LC-based chip tunable reflective load at 62 GHz, top, side, and bottom view.

visual impression, the borders around the LC material's trench measure 150 μm and 100 μm in the 28 GHz and 62 GHz devices, respectively.

The designed reflective load at 28 GHz has overall dimensions of 2.7×1.4×0.56 mm^3 including the input CPW line and grounding around the LC housing cavity. The device operating ast 62 GHz has overall dimensions of 1.6×0.8×0.56 mm^3 which is considerably smaller. The CPW input is necessary for testing of this device, however, it can be removed to reduce area while the reflective loads are being integrated into an RTPS device. Grounding borders are also crucial for the bonding process of two substrates.

6.1.2 Fabrication Process

It is important to emphasize that both reflective loads adhere to the same fabrication process and have been manufactured on a single piece of silicon through a unified fabrication run. The fabrication process commences with the cleaning of a 280 μm thick high-resistivity silicon wafer. It is important to note that in Figure 6.5, two substrates, the top and bottom sides, are presented on the right and left, respectively. To create filling holes, a layer of photoresist is spin-coated, followed by photolithography. The resulting pattern exposes the desired areas for the filling holes, each with a diameter of 100 μm. Subsequently, DRIE is employed for the etching-through process to create these holes.

Following this, a cleaning process is conducted, and another round of photolithography is carried out to expose areas designated for the LC material housing. The etching process, using DRIE, is then executed with a depth of 20 μm. Despite the use of high-resistivity silicon, some conductivity between isolated metal pads may occur. To mitigate this issue, a 500 nm thick Si_3N_4 layer is deposited using PECVD.

In the metallization process, the presence of an adhesion layer is crucial for bonding gold to silicon nitride. It is essential to deposit gold immediately afterward in the same chamber to prevent oxidation. To achieve this, a 50 nm layer of chromium followed by a 150 nm layer of gold is deposited using a sputtering system. It is noteworthy that the utilization of this system is critical, ensuring metal coverage over the sidewalls of the trench. The subsequent step involves establishing the desired metallization pattern using a PR and a photolithography step, thereby preparing the sample for electroplating. This electroplating process enables the thickening of the sputtered gold seed layer to 2 μm.

Metallization patterns become evident after the wet etching of gold and chromium. Subsequently, the sample is prepared for dicing into separate top and bottom pieces. To facilitate pre-alignment, a thin layer of PI (100 nm) is applied over areas within the LC cavity. The IBI surface treatment method is then implemented, with ions striking the PI

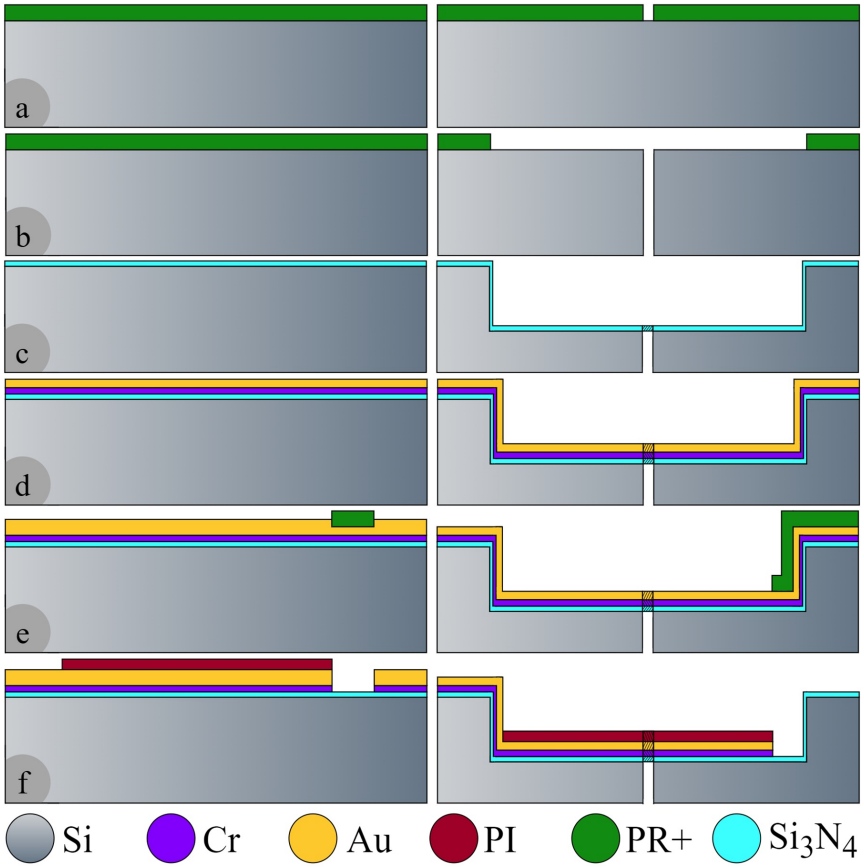


Figure 6.5: Fabrication process flow for developing LC integrated fully silicon made tunable reflective load: (a) photolithography of positive PR, (b) etching through using DRIE, photolithography of positive PR, (c) etching 10 μm using DRIE and cleaning, depositing Si_3N_4 using PECVD, (d) sputtering Cr and Au, (e) photolithography of positive PR, electroplating Au, (f) removing PR, Au and Cr wet etch, adding PI.

surface at a 45° angle for a brief period. This step enhances the tuning range of the LC material in a planar structure. The final step involves utilizing a die bonder to perform a low-temperature Au-Au bonding process with precise alignment.

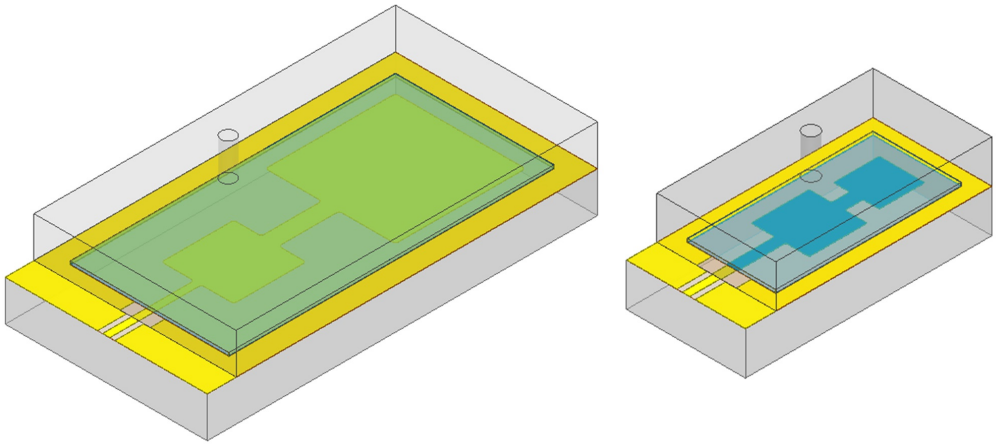
To introduce the LC material into the created cavity, the packaged device will be submerged into the LC material. Subsequently, the entire LC container will be placed inside a vacuum chamber to evacuate any air while keeping the device below the LC level. Following this, an increase in pressure will prompt the surrounding LC material to enter

the vacuumed cavity. This process may be repeated multiple times to ensure the formation of a bubble-free LC-filled cavity. Finally, the LC filling holes will be sealed with glue to ensure isolated encapsulation.

6.1.3 Simulation Results

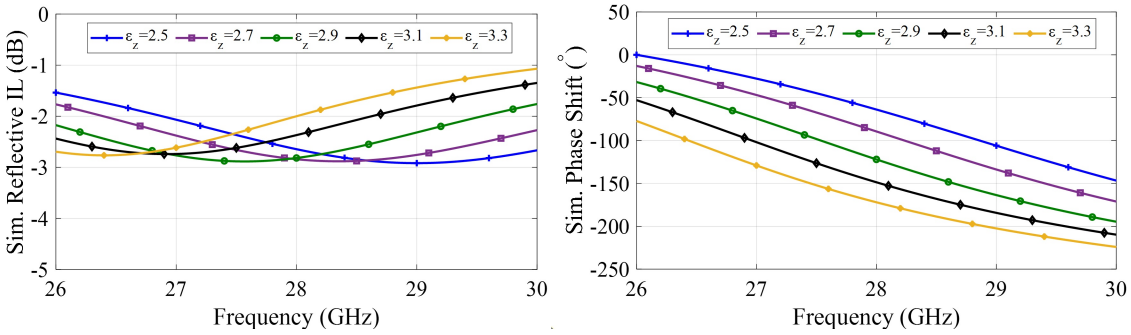
The design and simulation were carried out using Ansys Electronics Desktop software, assuming a full tensor representation of the LC material as detailed in Chapter 2. All layers discussed in the design and fabrication section were meticulously drawn in the simulation software, including metallization and silicon nitride layers. Figure 6.6a and Figure 6.6b depict the 3D view of the 28 GHz and 62 GHz reflective loads in the Ansys Electronics Desktop software, respectively.

For simulation purposes, five reflective loads with different LC materials inside were simulated to analyze the impact of variation in dielectric properties. This resulted in five different curves for both reflective insertion loss and phase shift. In Figure 6.7a, the simulated reflective insertion loss of the 28 GHz device is illustrated, revealing a maximum of 2.95 dB across the frequency band among all variation states. It shows that the maximum reflective insertion loss occurs when the dielectric constant along the Z-axis is at its minimum (state 1 in Table 3.2). Despite seeming odd, this is mainly due to the fact that the



(a) (b)

Figure 6.6: 3D view of the structure of the proposed LC-based chip tunable reflective loads operating at: (a) 28 GHz and (b) 62 GHz (dimensions are to scale).



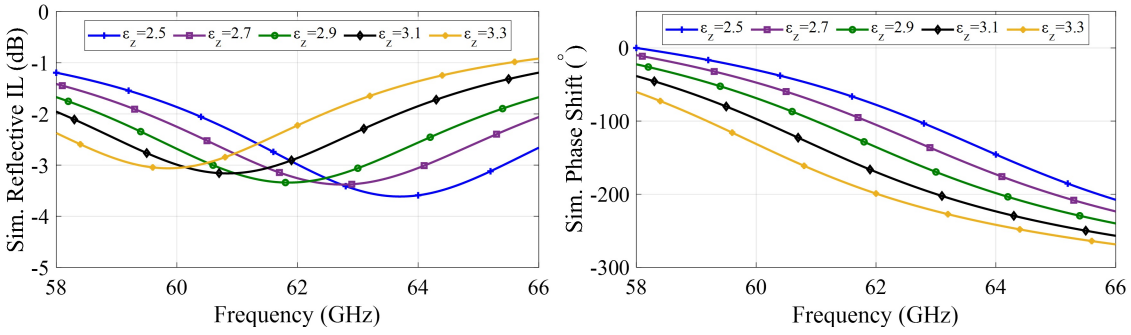
(a) (b)

Figure 6.7: Simulation results of the 28 GHz sample: (a) reflective insertion loss and (b) reflective phase shift

loss tangent is highest in this state, resulting in slightly higher loss.

Observing the reflection coefficient at the input port, its phase variation is the actual result. As the dielectric constant increases, the reflected signal experiences a higher shift in its phase. Figure 6.7b presents the simulated phase shift of the input reflection for different LC states, showcasing a 117° phase variation. This makes the FOM equals to 39.7°/dB.

Similar to the previous design, the reflective load operating at 62 GHz should be modeled in Ansys Electronics Desktop software in 5 different devices, each with varying states of LC material. This allows observation of the changes in reflective insertion loss and phase



(a) (b)

Figure 6.8: Simulation results of the 62 GHz sample: (a) reflective insertion loss and (b) reflective phase shift

shift as the LC material properties vary. The simulated reflective insertion loss of the 62 GHz device is depicted in Figure 6.8a, showing a maximum of 3.6 dB across the frequency band among all different states. The maximum reflective insertion loss occurs in state 1 when the dielectric properties of the LC material are at their lowest, similar to the 28 GHz sample.

The reflective phase shift of this sample exhibits the same behavior as the 28 GHz counterpart, phase shift increases with the increment in Z-axis dielectric permittivity as shown in Figure 6.8b. The simulated design reveals a maximum phase shift of 122° at 62 GHz, corresponding to a FOM of 33.8°/dB in full-wave simulation. In the next section, the results of the fabricated reflective loads will be presented.

6.1.4 Measurement Results

The entire fabrication process is identical for both devices, thus their designs will be integrated onto a single piece of silicon. Figure 6.9 provides an overview of the silicon piece containing both designs, including the top and bottom substrates. Each individual substrate piece must be diced to facilitate the assembly of the final devices.

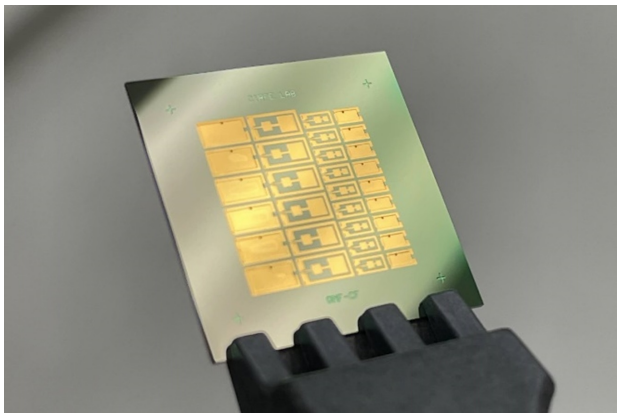
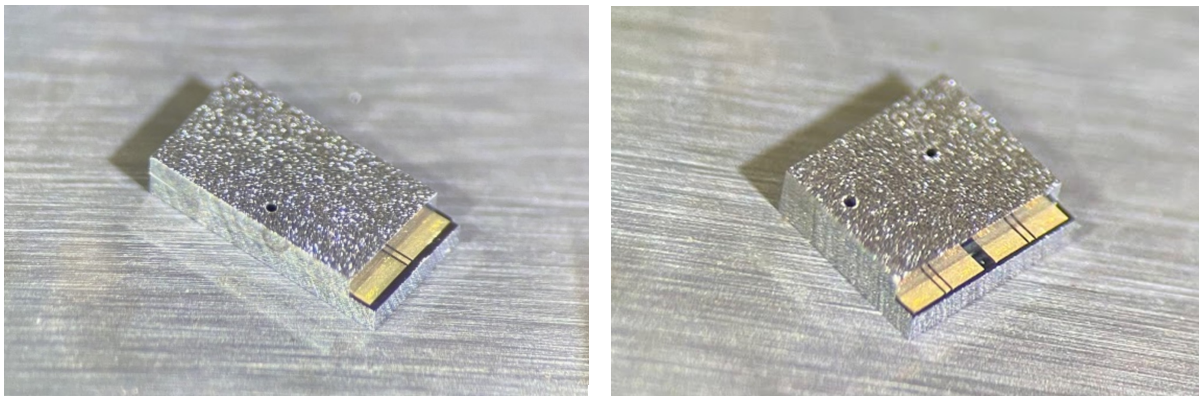


Figure 6.9: Fabricated sample that includes top and bottom sides of both 28 GHz and 62 GHz devices on a single piece of silicon.

The dimensions of the 28 GHz sample measure 2.7×1.4×0.56 mm^3, making it suitable for processing using the available die bonder machine (TreSky Diebonder). However, the 62 GHz design, with dimensions of 1.4×0.8×0.56 mm^3, is significantly smaller. It is so compact that it can be drawn into the vacuum holder of the tool, rendering it impossible to package a single 62 GHz reflective load sample. Consequently, for measurement purposes,

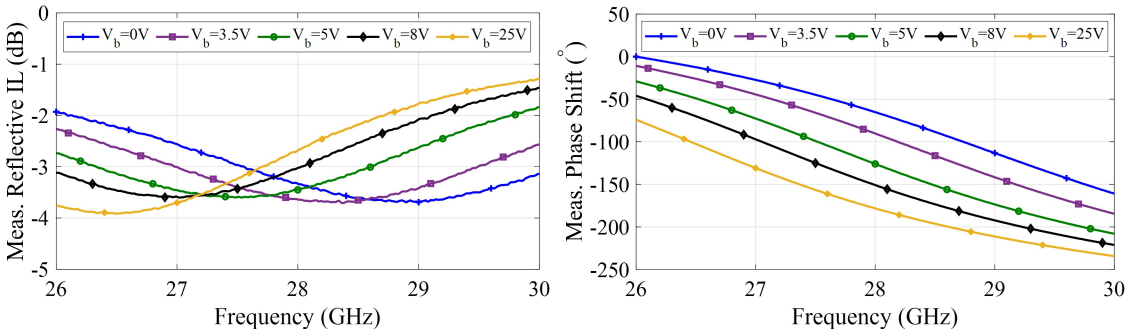


(a) (b)

Figure 6.10: Fabricated samples operating at: (a) 28 GHz and (b) 62 GHZ (two devices).

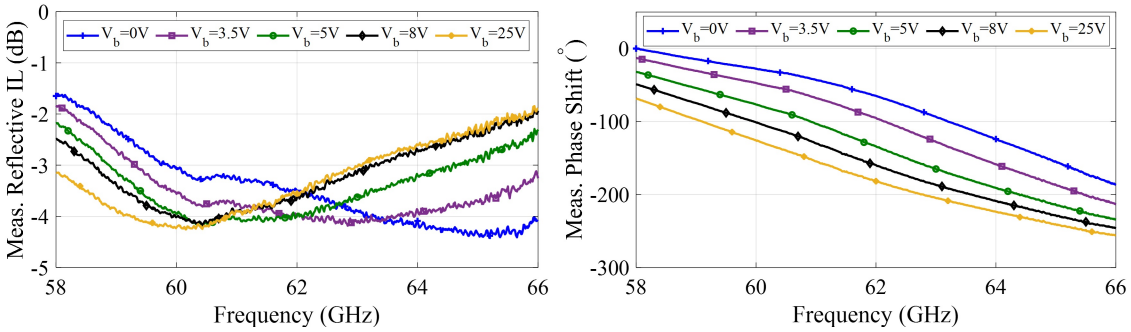
two 62 GHz reflective loads are being packaged side by side. Both of these devices are depicted in Figure 6.10.

The measurements were conducted using 150 μm pitch GSG probes and a 67 GHz Keysight VNA. The bias voltage was applied through the input port using a bias tee. The response of the reflective loads began to change at around 2.6 V to 2.8 V and reached saturation at 25 V. It is important to note that while there may be slight changes in the response if the bias voltage exceeds 25 V, the variation in phase shift appears to be negligible.



(a) (b)

Figure 6.11: Measurement results of the 28 GHz sample: (a) reflective insertion loss and (b) reflective phase shift



(a) (b)

Figure 6.12: Measurement results of the 62 GHz sample: (a) reflective insertion loss and (b) reflective phase shift

With no applied voltage, the maximum reflective insertion loss is measured at 3.5 dB, as shown in Figure 6.11a. While the overall pattern of measurement follows the simulation up to a bias voltage of 8 V, the loss increases as the voltage increases. Consequently, the maximum reflective insertion loss occurs at 25 V, which equals 3.9 dB.

Phase shift measurement results are consistent with the simulation, showing an expected increase in phase shift with higher bias voltages, demonstrated in Figure 6.11b. The maximum phase shift measures 113° at 28 GHz with 25 V of applied voltage. This results in an FOM of 29°/dB, which is slightly lower than the simulation result. It's important to note that both the simulated and measured phase shift responses are normalized to a maximum of 0° at the start of the reported frequency band.

The measured reflective insertion loss, shown in Figure 6.12a, exhibits a similar pattern to the simulations, with slight differences in magnitudes. The maximum reflective insertion loss of 4.3 dB occurs when the bias voltage is 0 V and the LC material is in state 1. As the applied voltage increases, the frequency of maximum reflective insertion loss decreases.

As expected, measurements reveal a maximum of 118° phase shift at 62 GHz, as shown in Figure 6.12b. With a maximum reflective insertion loss of 4.3 dB, the FOM equals 27.5°/dB over the presented frequency band. These measurement results proved the feasibility of such reflective loads at those frequencies. As a result, the design of RTPS devices using the designed loads could be followed in the next step.

6.2 Millimeter Wave Reflective Type Phase Shifters

RTPS represent a popular choice in monolithically integrated phased array systems for microwave and mm-Wave applications. These phase shifters rely on a variable reflective load that enables controlled phase shift variation. Typically, a RTPS consists of an LC load and a 3 dB hybrid, such as Lange, broadside, or hybrid coupler.

Compact phase shifters have been realized using Gallium Nitride (GaN), Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) technology, and PCM Germanium Telluride (GeTe). While PCM technology offers a small footprint and non-volatile functionality, it may compromise linearity and power handling capability. Both GaN and PCM technologies are limited to discrete tuning steps. MEMS technology, on the other hand, offers better linearity and power handling capability, with an analog tuning mechanism. However, reducing the footprint of MEMS-based devices in high frequencies presents a significant challenge.

Chip-level LC-based devices emerge as promising candidates in such scenarios. They provide high linearity, power handling capability, and continuous tuning, while their size can be smaller than that of MEMS-based devices in higher frequencies. In this section, new chip-level monolithically integrated RTPS phase shifters will be introduced using previously designed and fabricated mm-Wave LC-based reflective loads.

6.2.1 Design Principle

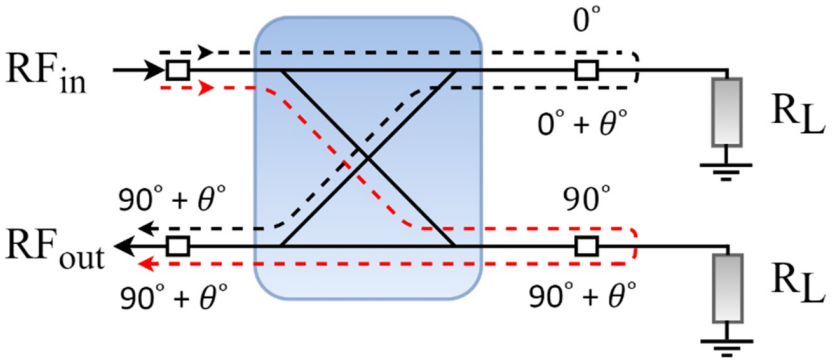


Figure 6.13: Schematic of the proposed phase shifter which includes two identical LC-based tunable loads and a quadrature hybrid coupler.

The schematic of the proposed mm-Wave LC-based phase shifter includes a quadrature Hybrid and two identical reflective tunable loads, as shown in Figure 6.13.

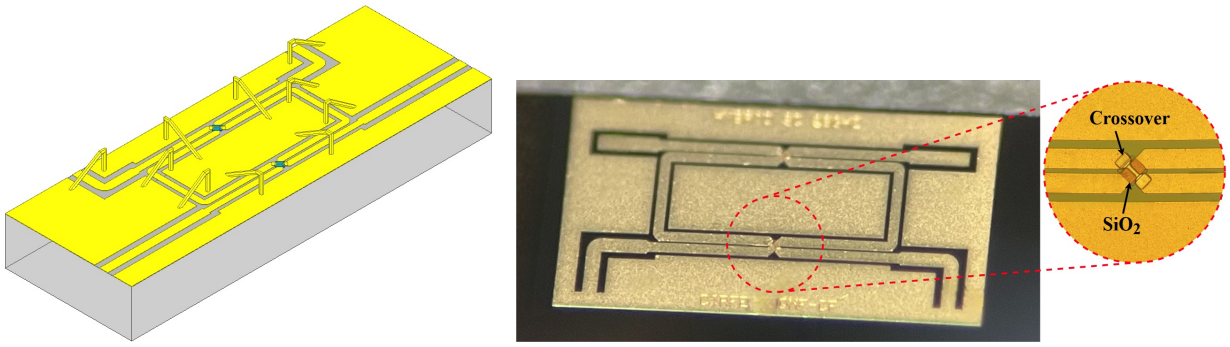
In a lossless scenario, the phase shift of the output port is solely determined by the reactance of the reflective load X_L. Assuming that the reactance of the reflective load varies within the range from X_{Lmin} to X_{Lmax}, the total phase shift of the device can be calculated using equation (6.1).

$$\Delta\theta = \theta_{max} - \theta_{min} = 2\left[tan^{-1}\left(\frac{X_L^{max}}{Z_0}\right) - tan^{-1}\left(\frac{X_L^{min}}{Z_0}\right)\right]. \tag{6.1}$$

Where Z_0 represents the characteristic impedance of the quadrature hybrid. Traditional hybrid coupler uses think signal line and gap results in challenging wire bonding procedure.

6.2.2 28 GHz Hybrid

In this study, a 3 dB tandem coupler was selected for its broadband response and compact size. Constructing such a coupler involves combining two 8.3 dB CPW couplers. An additional metal layer with an insulating dielectric deposition is necessary to connect the signal lines at the crossovers. The length of the coupling side is determined by the broadside coupling effect, resulting in smaller than $\lambda/4$. Given the dimensions of the designed reflective load in the preceding section and the compact nature of a tandem 3 dB coupler, it is necessary to extend two CPW lines that connect to the reflective loads. These ports feature



(a) (b)

Figure 6.14: 3 dB tandem coupler at 28 GHz: (a) 3D view in simulation software, (b) fabricated sample.

a 90° bend to facilitate the connection to the reflective loads, as illustrated in Figure 6.14 for a 28 GHz designed coupler.

The dimensions of the CPW coupler at 28 GHz are originally $1\times0.5\ mm^2$, but with the extension arms depicted in Figure 6.14a, they reach $1.7\times0.75\ mm^2$. The use of wire bonding is essential to ensure uniform ground across the hybrid. The form of the wire bonds is assumed to be realized in both ball-wedge and wedge-wedge configurations, consistent with the capability of available equipment. Two dumbbell-shaped junctions connect the signal lines at the crossovers, shown in Figure 6.14b. Additionally, ten wire bonds contribute to establishing a unified ground for all CPW lines.

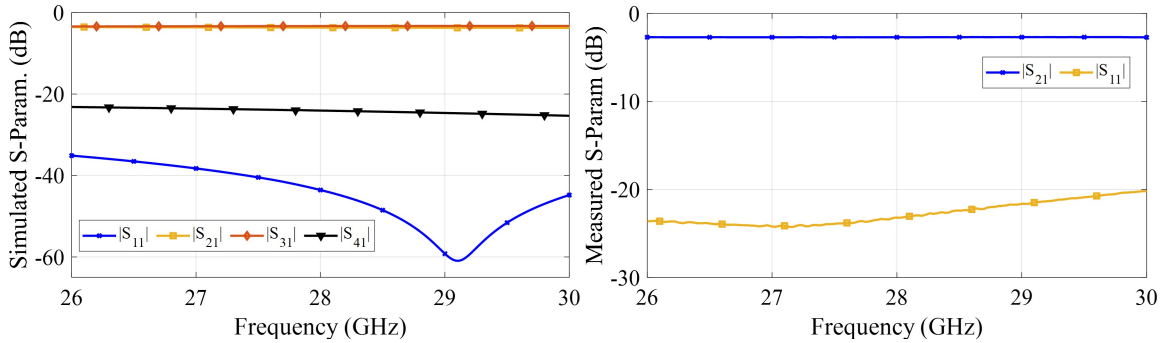
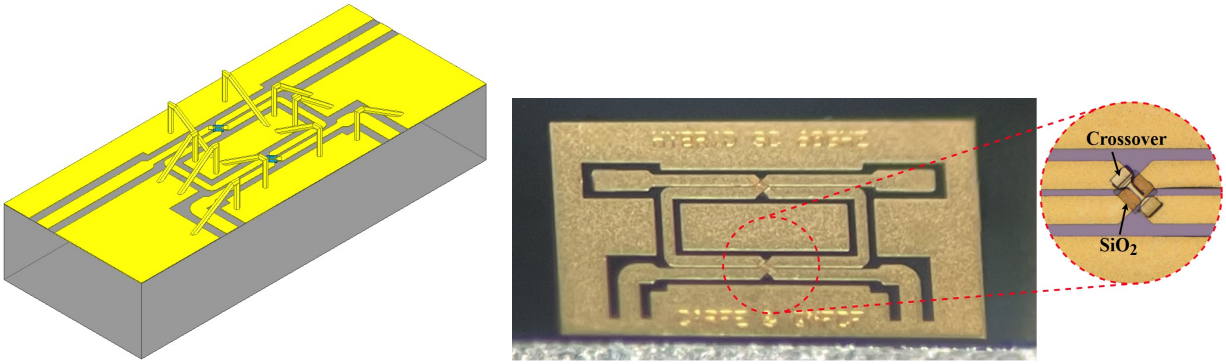


Figure 6.15: Result of the 28 GHz 3dB CPW coupler, (a) simulation results of 4-port device, (b) measurement results of a 2-port device.

Simulation results of the 4-port hybrid at 28 GHz are presented in Figure 6.15a. The return loss in the simulation exceeds 30 dB across the frequency band, while the isolation performance of this coupler is better than 23 dB. The transmission and coupling vary within the range of 3.27 dB to 3.75 dB over the presented frequency band. This should result in a maximum of 0.9 dB insertion loss when combined with any reflective load operating at the same frequency. Since the available measurement setup is a two-port probe station, ports 2 and 3 were terminated in short circuits. This resulted in a two-port network, allowing for the observation of insertion loss and return loss. Figure 6.15b shows a return loss better than 20 dB and an insertion loss of up to 2.4 dB over the frequency range. While the insertion loss is higher than the simulation result, this discrepancy could be attributed to the effective length of the short-circuit stubs placed at the ends of ports 2 and 3.

6.2.3 62 GHz Hybrid

Similarly, another coupler has been designed to operate at 62 GHz, tailored to match the reflective load's requirements. While having a similar structure, the dimensions are considerably smaller at 0.56×0.37 mm^2. The overall dimensions of the device, visible in Figure 6.16a, are 1.1×0.59 mm^2, including extended input CPW lines and ground planes. It is noteworthy that the silicon nitride layer is present on top of the silicon substrate in both hybrids. A top view of the fabricated hybrid is shown in Figure 6.16b, highlighting the dummbbel shaped crossover. The Si_3N_4 layer is visible in non-metalized areas with purple color.



(a) (b)

Figure 6.16: 3 dB tandem coupler at 62 GHz: (a) 3D view in simulation software (b) fabricated sample.

As depicted in Figure 6.17a, the return loss of this hybrid is better than 27 dB, while its isolation exceeds 24 dB over the frequency band. The transmission and coupling range between 2.6 dB and 4.5 dB, with a phase deviation of less than ±0.25° over the working frequency range, which results in insertion loss of 1.1 dB when connected to identical loads.

Due to limitations in the available measurement setup, which is a two-port probe station, ports 2 and 3 were terminated in short circuits. This resulted in a two-port network, allowing for the observation of insertion loss and return loss. Figure 6.17b shows a return loss better than 16 dB and an insertion loss of up to 3.2 dB over the frequency range. While the insertion loss is higher than the simulation results, this discrepancy could be attributed to the effective length of the short-circuit stubs placed at the ends of ports 2 and 3.

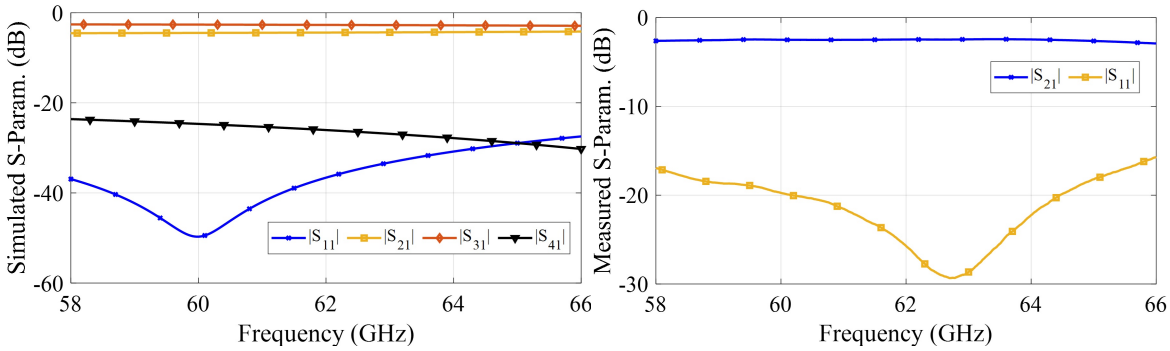


Figure 6.17: Result of the 62 GHz 3dB CPW coupler, (a) simulation results of 4-port device, (b) measurement results of a 2-port device.

6.2.4 Simulation Results of 28 GHz RTPS

With the utilization of the previously designed reflective load and hybrid at 28 GHz, a comprehensive RTPS can be assembled. The complete unit is illustrated in both top and 3D views in Figure 6.18. For simulation purposes, the input and output CPW lines are extended sideways, which is also necessary for measurement procedures involving GSG

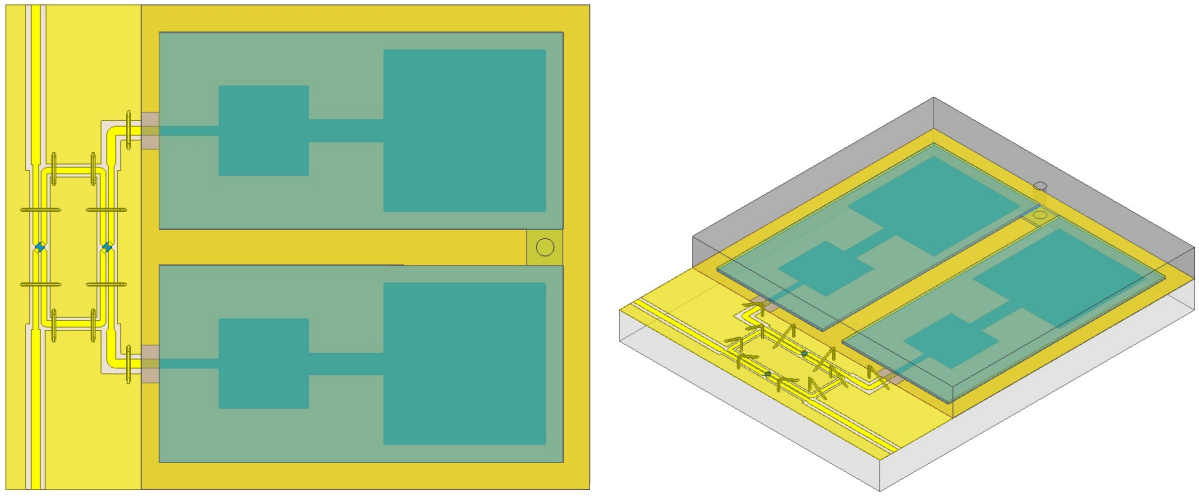


Figure 6.18: Complete RTPS at 28 GHz: (a) top view and (b) 3D view.

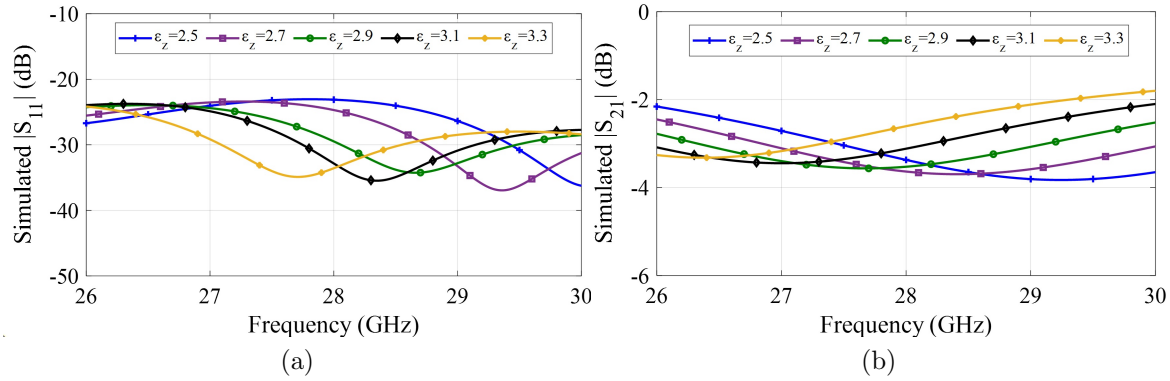


Figure 6.19: Complete RTPS simulation results at 28 GHz: (a) $|S_{11}|$ and (b) $|S_{21}|$.

probes. However, in an actual unit, such constraints do not exist, and both CPW lines can be drawn from the left side of Figure 6.18a. The substrate of the hybrid and the bottom substrate of the reflective loads are unified in simulation, as they will be fabricated on the same high-resistivity silicon wafer.

The addition of reflective loads alters the S-parameter response of the hybrid. Although the return loss worsens compared to the initial result, it remains better than 23 dB over the 26-30 GHz frequency band across different states of the LC material, as shown in Figure 6.19a. As anticipated, the insertion loss increases in comparison to the reflective insertion

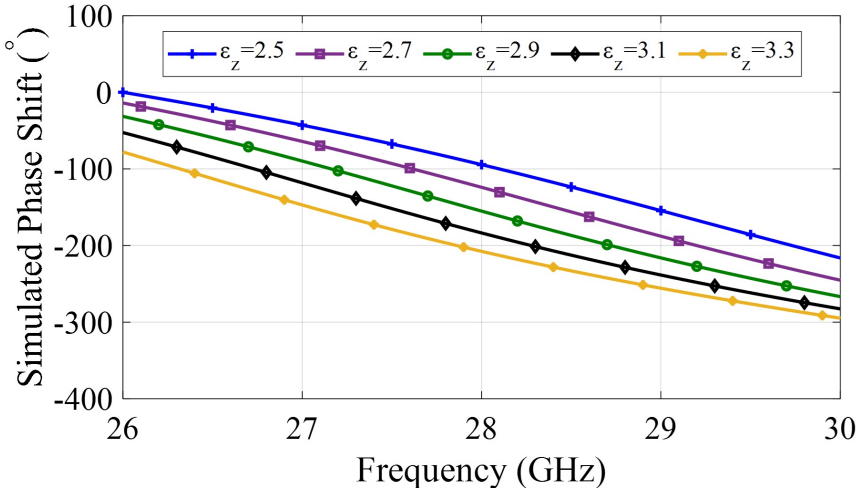


Figure 6.20: Simulated phase shift of RTPS at 28 GHz.

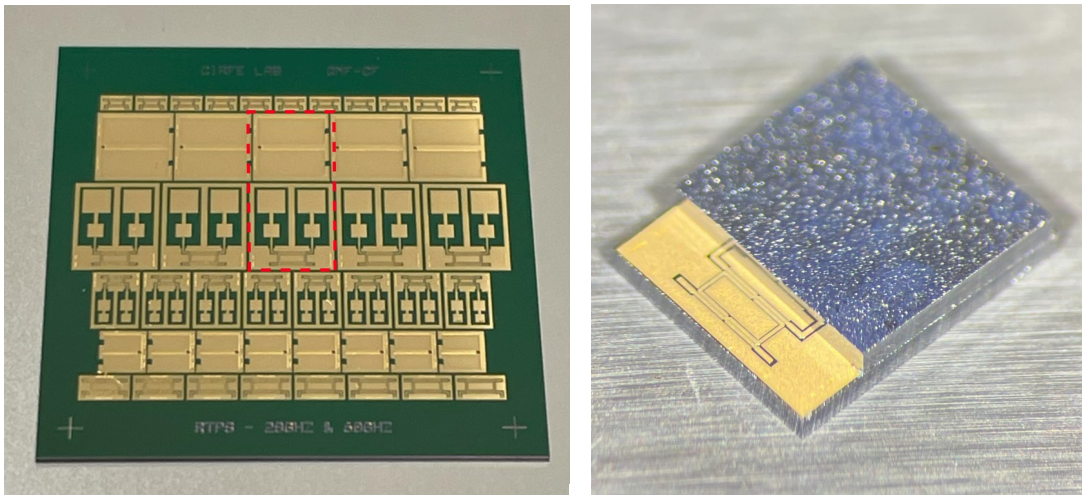
loss of the reflective load.

The maximum insertion loss reaches 3.85 dB, which is 0.95 dB higher than that of the reflective load, due to the addition from the hybrid. The insertion loss over the frequency band in different states of the LC material is shown in Figure 6.19b. The variation in insertion loss depends on the operating frequency and ranges from 0.6 dB to 1.8 dB.

The phase shift response of the RTPS unit at 28 GHz is illustrated in Figure 6.20, showing a maximum phase shift of 114° at 28 GHz. As expected, it closely follows the performance of the reflective load, with minimal changes resulting from the insertion of the hybrid.

6.2.5 Measurement Results of 28 GHz RTPS

After completing the fabrication process, including the pre-alignment surface treatment, the top and bottom substrates need to be packaged together. The microscopic image of the fully assembled RTPS unit operating at 28 GHz is shown in Figure 6.21a. The overall dimensions of this unit are $3.3 \times 2.7 \times 0.564\ mm^3$. Due to the small width of the coupling traces in the hybrid and the short distance where cross-connection is required, placing wire



(a) (b)

Figure 6.21: Microscopic image of fabricated 28 GHz RTPS: (a) before dicing on a piece of silicon with the highlighted 28 GHz top and bottom parts, and (b) complete packaged unit with dimensions of $3.3 \times 2.7 \times 0.564\ mm^3$.

bonds was challenging. To address this, an alternative method was designed and fabricated using two additional layers. The first layer is a square patch that covers the middle line using silicon dioxide (SiO_2). Next, a metal layer is patterned in a dumbbell shape to create the connection instead of using wire bonds, as shown in Figure 6.21b.

The SiO_2 layer is deposited using a sputtering system to avoid the high temperatures associated with PECVD systems. This allows for a smooth lift-off process to form the dielectric layer with a thickness of $1.5\mu m$. The metal layer is also deposited using the sputtering method because the height of the traces ($2\mu m$) and the SiO_2layer is too high for other deposition methods to ensure a continuous connection. The dumbbell-shaped metal layer has a thickness of $1\mu m$ and is primarily composed of copper, except for the adhesion layer at the very bottom and the protective layer at the top, which are made of chromium (Cr) and gold (Au), respectively. The junction width is measured at $3.5\mu m$, while the patch width is $40\mu m$.

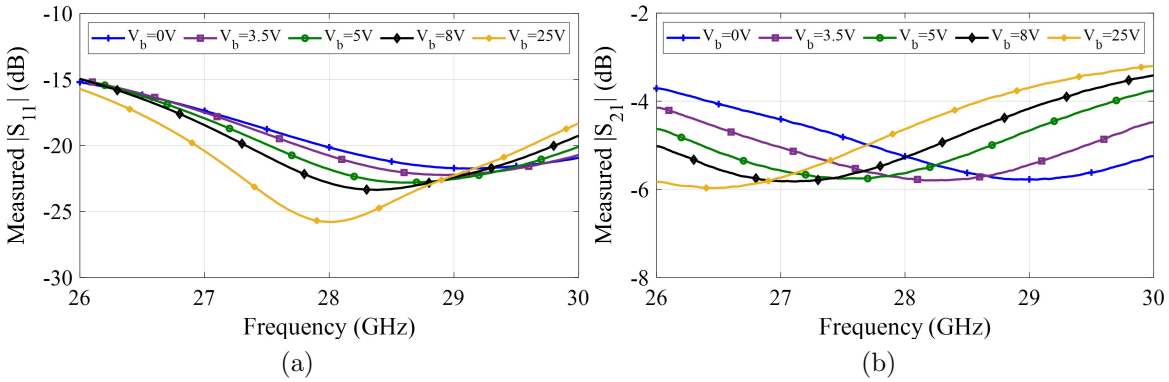


Figure 6.22: Complete RTPS measurement results at 28 GHz: (a) $|S_{11}|$ and (b) $|S_{21}|$.

The measurement process was conducted using $150\mu m$ pitch GSG probes, cables, and bias tees, along with a Keysight network analyzer, all rated to operate up to 67 GHz. The bias voltage range and values remained consistent with those used for the reflective loads since they were integrated into this RTPS without any structural changes. Figure 6.22a illustrates the return loss variation across different bias voltages over the operating frequency band. Minimal changes in return loss are observed with varying bias voltage, maintaining a performance of better than 15 dB. The insertion loss versus applied voltage within the range of 26-30 GHz is depicted in Figure 6.22b. At the start of the band, the maximum insertion loss reaches 5.95 dB when the maximum bias voltage is applied. The insertion loss variation ranges from 0.9 dB to 2.2 dB at 28 GHz and 29.4 GHz, respectively.

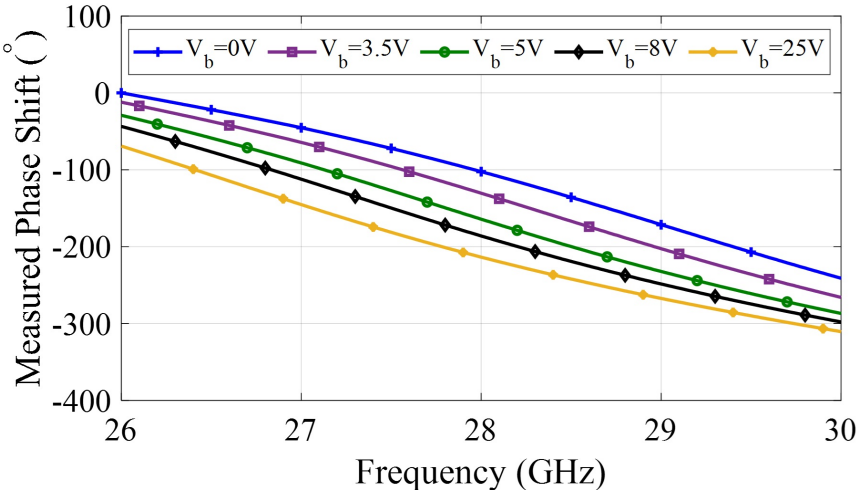


Figure 6.23: Measured phase shift of RTPS at 28 GHz.

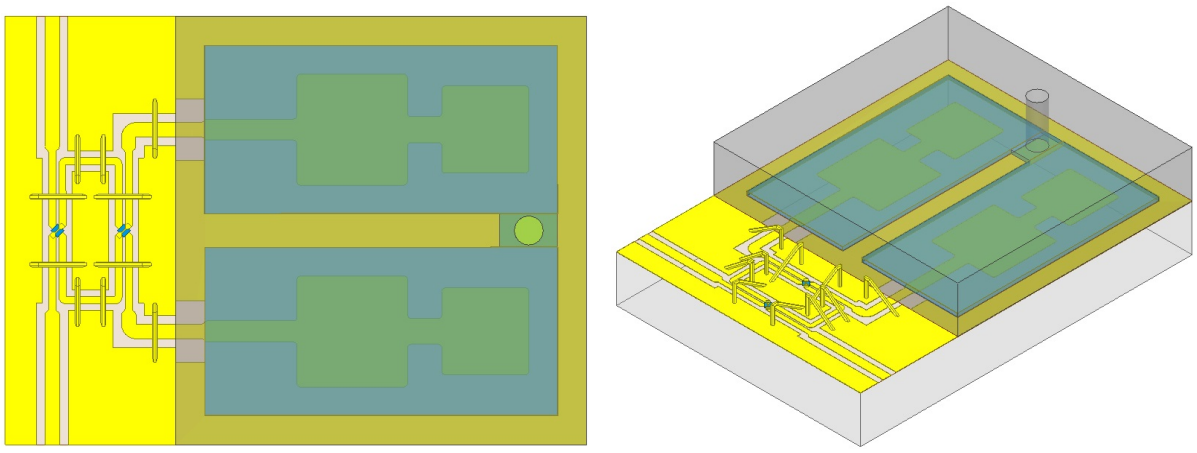
The phase shift of this RTPS is illustrated in Figure 6.23 versus different applied voltages. At 28 GHz, this device provides a phase shift of 115°, aligning well with the simulation results. Calculating the FOM based on the maximum insertion loss yields a value of 19.16°/dB.

6.2.6 Simulation Results of 62 GHz RTPS

Using the designed reflective load in Section 6.1.3 and hybrid operating at 62 GHz, a monolithic RTPS can be created. The complete RTPS device is depicted in both top and 3D views in Figure 6.24. For simulation purposes, the input and output CPW lines are extended sideways, a necessity for measurement procedures involving GSG probes. However, in an actual unit, such constraints do not exist, and both CPW lines can be drawn from the left side of Figure 6.24a. The substrate of the hybrid and the bottom substrate of the reflective loads are unified in simulation, as they will be fabricated on the same high-resistivity silicon wafer.

The simulated return loss of the complete RTPS operating at 62 GHz is depicted in Figure 6.25a. The change in return loss is minimal across all variations of LC material, indicating that the response is not significantly impacted by changes in the load. As expected, the return loss deteriorated compared to the short circuit response of the hybrid, with the return loss being better than 18 dB.

The insertion loss remains better than 4.8 dB over the frequency band for all states

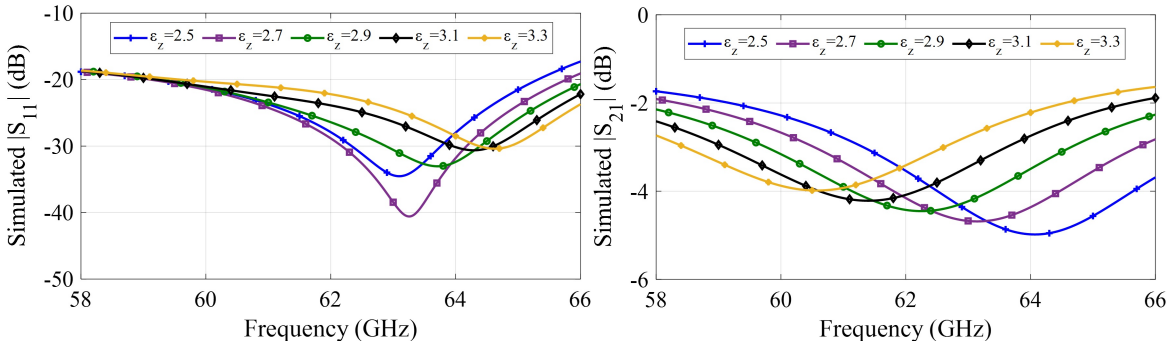


(a) (b)

Figure 6.24: Complete RTPS at 62 GHz: (a) top view and (b) 3D view.

of LC material. This indicates a notable increase in insertion loss compared to the single reflective load discussed in Section 6.1.3.

The phase shift of the simulated RTPS is depicted in Figure 6.26 as the dielectric properties of the LC material were altered. This resulted in a phase shift of 118°. The simulation results of the RTPS device exhibit an expected difference from those of the designed reflective load. Consequently, the fabrication process is followed to produce this device.



(a) (b)

Figure 6.25: Complete RTPS simulation results at 62 GHz: (a) $|S_{11}|$ and (b) $|S_{21}|$.

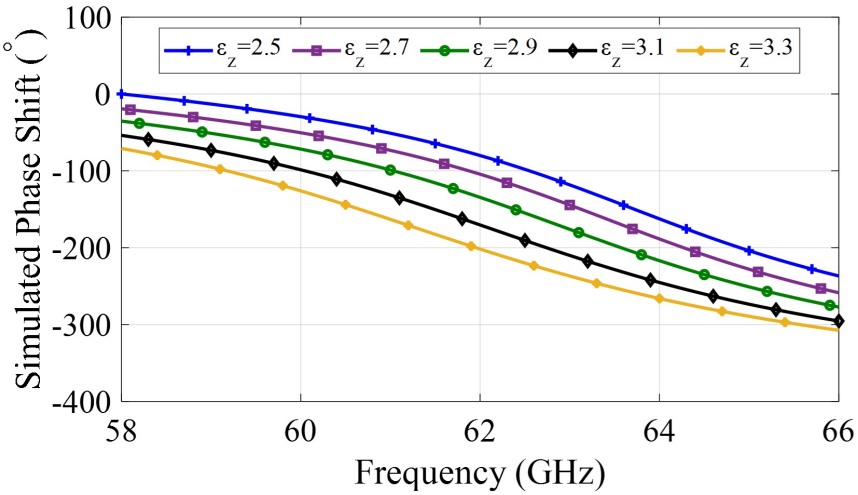


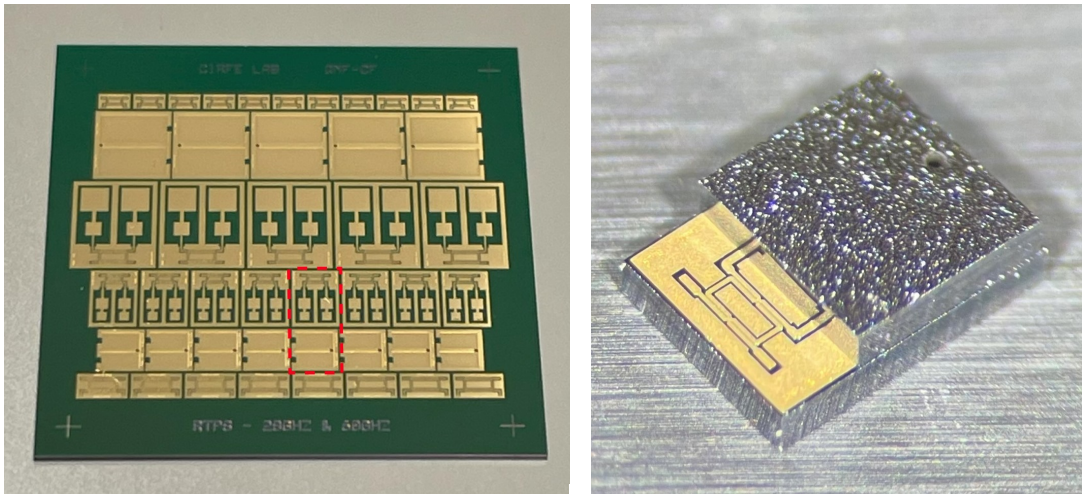
Figure 6.26: Simulated phase shift of RTPS at 62 GHz.

6.2.7 Measurement Results of 62 GHz RTPS

The top and bottom substrates of the 62 GHz RTPS need to be assembled together to form a monolithic device. This process is carried out using a Tre-Sky die bonder with a low-temperature Au-Au bond recipe. The recipe requires a temperature of $228°C$, a pressure of 10 kg, and a duration of 10 minutes, ensuring a flawless bond between the gold layers of both substrates. The microscopic image of the complete RTPS device operating at 62 GHz is shown in Figure 6.27a. The overall dimensions of this device measure at $2.05 \times 1.48 \times 0.564\ mm^3$. While the thickness of this device is the same as the 28 GHz sample, it appears thicker due to its smaller footprint.

Figure 6.27b presents a magnified microscopic image of the cross-over junction in the 62 GHz hybrid. The layer composition and metal thickness of the junction are similar to what was mentioned in section 6.2.5, except for the dimensions of the dumbbell. While the width of the square patch is $30\mu m$, the width of the junction measures only $3.3\mu m$. The measurement process is conducted using $150\mu m$ pitch GSG probes, cables, and bias tees, along with a Keysight network analyzer, all capable of operating up to 67 GHz. The applied voltage ranges are similar to those of the reflective loads, as they have been used in this RTPS with no change in the structure.

The measurement results reveal a return loss better than 13.7 dB in all cases of applied voltage. As shown in Figure 6.28a, the overall return loss response appears reasonable for such a high-frequency range. The measured insertion loss, illustrated in Figure 6.28b,

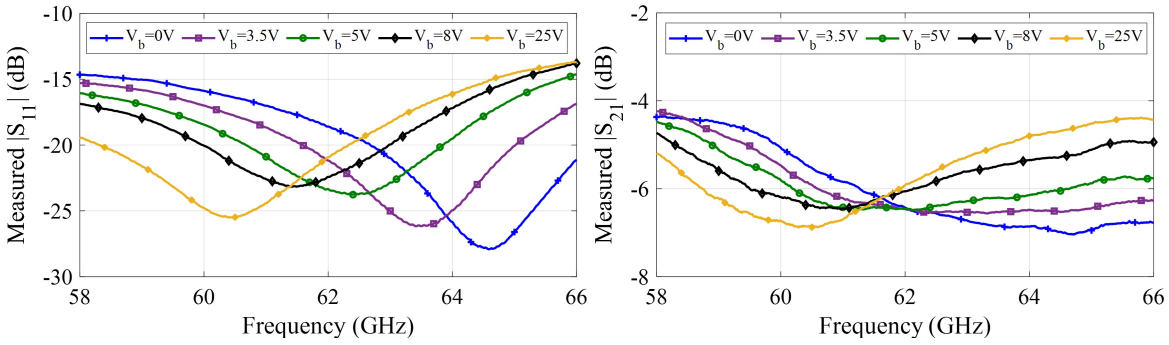


(a) (b)

Figure 6.27: Fabricated 62 GHz RTPS: (a) before dicing on a piece of silicon with the highlighted 62 GHz top and bottom parts, and (b) complete packaged unit with dimensions of $2.05 \times 1.48 \times 0.564\ mm^3$.

demonstrates a performance better than 7 dB in all cases of bias voltage over the frequency range of 58 GHz to 66 GHz. The insertion loss variation ranges from 0.23 dB to 2.4 dB over the presented frequency range as the applied voltage changes from 0V to 25V.

Finally, the measured phase shift of this unit is presented in Figure 6.29. This device



(a) (b)

Figure 6.28: Complete RTPS measurement results at 62 GHz: (a) $|S_{11}|$ and (b) $|S_{21}|$.

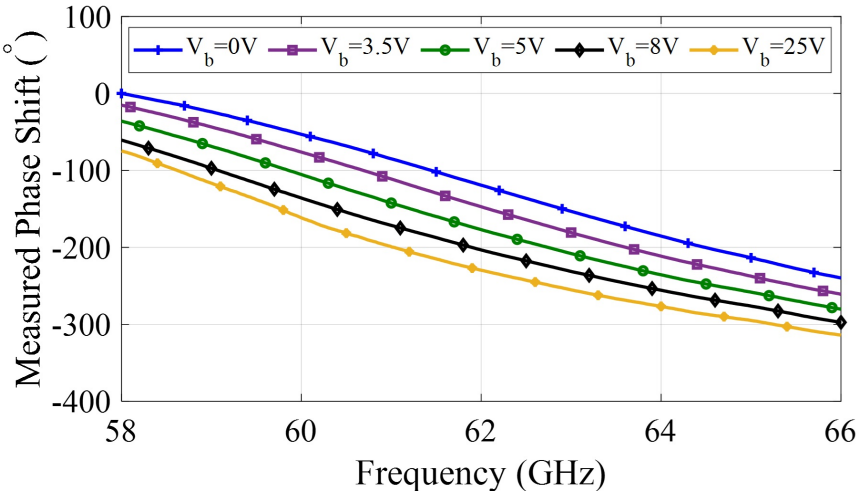


Figure 6.29: Measured phase shift of RTPS at 62 GHz.

exhibits a phase shift of 117° at 62 GHz, providing a FOM of $16.71°/dB$.

6.3 Result Comparison

To compare the proposed devices with state-of-the-art phase shifters, Table 6.1 is summarized. Most phase shifters in the literature are switched type or semiconductor-based, with a few LC-integrated devices. The 28 GHz sample is smaller in dimensions compared to MEMS-based analog phase shifters while achieving a similar FOM. The primary goal of this research was to significantly reduce the dimensions of LC-integrated devices. For instance, in contrast to [105], which has an area of 540 mm^2 and an FOM of $6.32°/dB$, the proposed device at 28 GHz has an area of only 8.9 mm^2 and an FOM of $19.16°/dB$. The slow-wave LC-based phase shifter in [42] demonstrates excellent performance with a compact footprint at 45 GHz. However, a fair comparison at 28 GHz reveals a lower phase shift of 162° and an insertion loss of 4.6 dB.

However, at higher frequencies, this research provides even more valuable results. Compared to MEMS-based and LC-integrated devices, the proposed 62 GHz sample has a significantly smaller footprint. For instance, the device in [108] has twice the area of the proposed device while providing a similar phase shift. LC-integrated devices utilizing slow-wave membrane structures may offer an improved FOM, but this often comes at the expense of a larger footprint and more complex fabrication requirements [112]. The FOM

Table 6.1: Summary of state-of-the-art mm-Wave phase shifters.

Work	$f(GHz)$	Tech	Tuning	A (mm^2)	PS (°)	Precis. (°)	IL (dB)	RL (dB)	V_b (V)
28 GHz	26-30	LC*	Analog	8.91	117	Cont.	5.95	15	25
[70]	26-30	MEMS*	Analog	10.4	120	Cont.	5.95	15	8
[106]	10-35	MEMS	3-bit	13.3	315	45	4.8	7	60
[103]	26-34	PCM	3-bit	1.4	173	22.5	4.9	14	12
[24]	26-30	PCM	8-bit	0.89	280	50‡	6	14.2	18
[107]	20-30	CMOS	Digital	0.48	360	5.6	13.5	13.3	NA
[105]	20-40	LC*	Analog	540	60	Cont.	9.5	14	100
[42]	30-45†	LC*	Analog	0.38	275	Cont.	5.35	10	20
62 GHz	58-66	LC*	Analog	3.03	115	Cont.	7	13.7	25
[108]	dc-60	MEMS	20-bit	5.7	126	6.3	3.21	16	45
[109]	60	MEMS	3-bit	22	360	45	5.51	9	30
[110]	10-50	SiGe	Analog	0.65	80	Cont.	18	12	2.8
[111]	40-67	LC*	Analog	23	89	Cont.	2.4	10	40
[112]	5-60	LC*	Analog	6.48	116	Cont.	1.7	10	10
[113]	61	LC*	Analog	32.84	170	Cont.	14	10	11
[114]	59.5	LC*	Analog	5.58	188	Cont.	11	8	NA

* Phase shifter has analog tunning capability.

† Reported measurements are at 45 GHz.

‡ The minimum initial step is 50°, it reduces as the required phase shift increases.

of the proposed device at 62 GHz is better than the LC-based devices presented in [113] and [114].

6.4 Summary

In this chapter, two LC-based reflective loads operating at 28 GHz and 62 GHz were designed and fabricated. The measurement results were promising, prompting the subsequent design and fabrication of RTPS devices. This entailed the creation of a low-loss compact hybrid, for which a tandem hybrid was selected. The overall performance of these RTPS phase shifters is notable, with FOM of $19.16°/dB$ and $16.71°/dB$ for 28 GHz and 62 GHz, respectively. The insertion loss variation of these samples is below 2.4 dB, which can be compensated for using either an active or passive solution. Depending on the type of system, a variable gain amplifier or variable attenuator can help maintain a constant insertion loss.

Chapter 7

Conclusion

7.1 Contributions

The research contributes significantly to the advancement of RF applications through the design, fabrication, simulation, and measurement of single-chip silicon micromachined variable capacitors utilizing nematic liquid crystal [115, 116]. The study explores three distinct capacitor configurations: shunt capacitor, series capacitor with an integrated bias line, and series capacitor. Fabricated through an in-house process employing meticulous techniques, including ion beam irradiation for precise pre-alignment layer treatment, the capacitors exhibit robust and reliable performance. With more than 20 samples fabricated and measured, the experimental results showcase the effectiveness of these capacitors at the chip level. The achieved improvements open new avenues for applications in tunable filters, phase shifters, impedance tuners, and matching networks, particularly in scenarios where low power consumption is crucial. The presented fabrication process allows for large-scale production on 8" or 12" wafers, marking the first reported instance of miniature single-chip LC-based variable capacitors.

Next, the research introduces the design, simulation, fabrication, and measurement of an LC-integrated tunable waveguide filter operating at 7.5 GHz [117]. The filter's tunability, controlled by manipulating the LC material's orientation through a static magnetic field, is a key innovation. The methodology proposed, involving the use of a magnetic field and a fused silica tube, offers accuracy and performance in designing tunable filters for diverse frequencies and applications. Particularly suited for 5G mm-Wave base stations, the results of this investigation provide insights that can enhance the design and performance of future LC-based tunable filters.

This research extends the contribution with the design and fabrication of two LC-integrated mm-Wave tunable reflective loads using a microfabrication process. Featuring a small footprint and multi-level surfaces, the pre-alignment layer is treated with an ion beam irradiation system. The applied voltage variation from 0 V to 25 V results in a remarkable 113° and 118° shift in reflected phase for 28 GHz [118] and 62 GHz devices, respectively. These devices exhibit a maximum reflective insertion loss of 3.9 dB and 4.3 dB, leading to FOM of 29°/dB and 27.5°/dB, respectively. The analog tuning mechanism, coupled with virtually nonexistent power consumption, positions these mm-Wave tunable reflective loads as ideal candidates for mm-Wave phase shifter applications with critical low-power DC consumption requirements. The incorporation of a single-chip tuning element that can be integrated with a hybrid monolithically adds versatility to their applications, especially in scenarios requiring heightened sensitivity.

This research advanced by utilizing the designed reflective loads in RTPS phase shifters [119]. This required the design and fabrication of low-loss tandem hybrids at 28 GHz and 62 GHz. Combining two reflective loads with a hybrid, two RTPS devices were designed and fabricated. With similar applied voltages to the reflective loads, phase shifts of 115° and 117° were achieved in the 28 GHz and 62 GHz samples, respectively. The return losses of these devices are 15 dB and 13.75 dB over their operating frequency bands. The insertion losses, however, reach 5.95 dB for the 28 GHz sample and 7 dB for the 62 GHz sample. While the 28 GHz RTPS shows a FOM of $19.16°/dB$, the 62 GHz RTPS exhibits a FOM of $16.71°/dB$. These devices provide analog tunability, with low power consumption and monolithic integration with a hybrid, making them suitable for high precision and mobile applications.

7.2 Future Work

This research has uncovered a unique opportunity to advance the field of microwave and mm-Wave devices. Its primary contribution lies in the capabilities of microfabrication and compact design, paving the way for future research endeavors to explore the development of more sophisticated components. Building upon the insights obtained from this study, researchers can explore various directions to create advanced structures, including impedance tuners, filters, antennas, metamaterial surfaces, and frequency-selective surfaces, utilizing the outlined fabrication process. In the subsequent sections, we will succinctly outline the advantages and fabrication processes associated with each potential future endeavor.

While LC materials have demonstrated excellent performance in reflective loads and RTPS phase shifters at mm-Wave frequencies, there is potential for integrating such mate-

rials into impedance tuners within a similar frequency range. With a modest enhancement in the fabrication process outlined in Chapter 6, it becomes feasible to realize mm-Wave impedance tuners. However, a significant challenge arises in achieving independent control over the variable capacitors, which is essential for impedance tuning. In cases where multiple capacitors are involved, separating the biasing voltage from the signal line becomes necessary. This necessitates the incorporation of biasing electrodes dedicated to each tunable element. To accomplish this, a thin layer of metal must be interposed between the two plates of LC-based capacitors to enable the manipulation of LC molecules via an electric field. Careful attention must be paid to both the design and fabrication processes to mitigate any potential adverse effects on the variable capacitors.

Using a process similar to that required for an impedance tuner, it is possible to construct planar tunable filters based on established guidelines for designing microstrip resonators and filters. Without modifying the existing process, filters such as interdigital, combline, and shunt stub filters can be designed and implemented. A common feature among these filter types is that the resonators are grounded DC-wise, allowing for the incorporation of biasing electrodes to facilitate tuning. Unlike with the impedance tuner, there is no requirement for an independent biasing scheme; thus, a single unified electrode can be employed to tune the entire filter. Such a filter would offer analog tuning capability within a compact form factor, operating effectively within the mm-Wave frequency range.

Since all microfabricated devices utilize silicon substrates, which are unsuitable for antenna design due to their high dielectric constant, a solution must be devised. One approach involves replacing one substrate with a thin layer of fused silica to facilitate radiation with minimal reduction in antenna efficiency. In contrast to the provided samples, the LC material's trench should be situated in the bottom substrate, while the input terminal must be patterned on the same substrate. Meanwhile, the antenna radiators need to be positioned on the quartz glass substrate. The connection between the input CPW and the antenna printed on fused silica would resemble what was presented in section 4.3, necessitating an Au-Au bonding process performed using either a wafer bonder (for large devices) or die bonder. Filling holes must be incorporated in the bottom silicon-made substrate. It is important to note that such an antenna cannot exhibit omnidirectional radiation patterns; however, directional beam patterns are achievable.

Frequency Selective Surface (FSS) and metamaterials are integral components in modern communication systems, offering unique capabilities for signal manipulation and control. The fabrication process for FSS and metamaterials closely mirrors that of antennas, employing a dual-substrate approach with one substrate composed of silicon and the other of fused silica. A critical consideration in designing FSS and metamaterials lies in the grounding of all elements in the structure, ensuring that the biasing scheme relies solely

on electrodes accommodated at the bottom of the LC material's trench. The number and arrangement of independent biasing electrodes are determined based on the specific design requirements of the application. These electrodes can either be unified, as seen in planar filter configurations, or distributed across multiple square zones to enable precise control over surface reflection properties.

Utilizing a similar approach, a reflect array antenna can be actualized within the mm-Wave range using a combination of silicon wafer and fused silica substrate. This fabrication method can be scaled up for industry-level production, accommodating 8 or 12-inch wafers. Given the absence of CPW lines, the necessity for high resistivity silicon wafers diminishes, consequently reducing overall costs. The biasing scheme necessitates independently controlled zones to manipulate the phase of the reflected wave in the desired pattern. The bonding process can be facilitated using available wafer bonders capable of handling wafers up to 4 inches, which aligns with the maximum acceptable size for most equipment in the facilities at the University of Waterloo. For larger antenna requirements, multiple such antennas can be arranged side by side, akin to a tile pattern, offering scalability and flexibility in antenna design and implementation.

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APPENDICES

Appendix A

Photolithography

A.1 Sample Preparation

Cleaning the silicon wafer or substrate before initiating the microfabrication process is a critical step. Additionally, before each lithography stage, a cleaning process is necessary to remove photoresist residues and any unwanted remnants from prior steps. While some of these cleaning procedures are non-destructive, others can potentially damage the device and should be applied only to bare silicon wafers or substrates at the beginning of the fabrication process.

A.1.1 RCA Cleaning

This process was developed by Werner Kern in 1965 while working at the Radio Corporation of America (RCA). RCA cleaning has since become a standard procedure for preparing wafers for microfabrication, effectively eliminating contaminants from the samples. In this thesis, only silicon and alumina wafers were used, but other substrates, such as glass and sapphire, can also be cleaned using this method. It is essential to wear proper personal protective equipment (PPE) when performing this cleaning method. The standard RCA cleaning process consists of the following three steps.

Step 1 targets organic and particle cleaning and is commonly referred to as RCA-1 or SC-1. This process involves preparing a solution by mixing Deionized (DI) water (H_2O), hydrogen peroxide (H_2O_2), and ammonium hydroxide (NH_4OH) in a 5:1:1 ratio (the ratio used in this research). The solution is heated to 70° before immersing the wafers into the

beaker. At around 65° to 70°, the solution begins to form bubbles, indicating the activation of the cleaning agents. Samples should be immersed for 20 minutes, followed by rinsing with DI water and drying with a nitrogen gun.

Step 2, the oxide strip, is optional and can be omitted when working with new wafers. This step involves immersing the samples in hydrofluoric acid at room temperature to remove any oxide contamination. In this study, this step was skipped as it was deemed unnecessary for new prime wafers.

Step 3 focuses on ionic cleaning, commonly referred to as RCA-2 or SC-2. The cleaning solution is prepared by mixing DI water, hydrogen peroxide, and hydrochloric acid (HCl) in a ratio of 6:1:1. The solution should be heated to 75° before immersing the wafers in the beaker for 10 minutes. This process is designed to remove any metallic contaminants from the wafer surface.

Finally, the samples should be thoroughly rinsed with running DI water and then dried using a nitrogen gun. This final step is crucial to prevent any contamination just before utilizing the prepared samples.

A.1.2 Piranha Cleaning

This cleaning method is aptly named after the Piranha fish because of its ability to aggressively dissolve and consume organic material through a vigorous chemical reaction. The solution used in this method is extremely potent and can cause significant damage, including severe chemical burns, if it comes into contact with skin or fabric. Due to its highly corrosive nature and powerful oxidizing properties, it is crucial to meticulously follow the steps for preparing the solution. Proper PPE is essential when performing this cleaning procedure to ensure safety. The wet bench to perform this cleaning recipe is shown in Figure A.1.

The solution is composed of four parts sulfuric acid (98%, H_2SO_4) and one part hydrogen peroxide. It is crucial to emphasize that the preparation of this solution must begin with the addition of sulfuric acid, followed by the careful addition of hydrogen peroxide. Reversing this order could trigger a hazardous chemical reaction. The sample should be gently immersed into the solution, which will begin to bubble vigorously as it reacts with and consumes organic materials.

The samples should then be immersed in DI water, followed by a thorough rinse with running DI water for several minutes. The drying process should be carried out using nitrogen blows to ensure no water streaks remain on the sample.

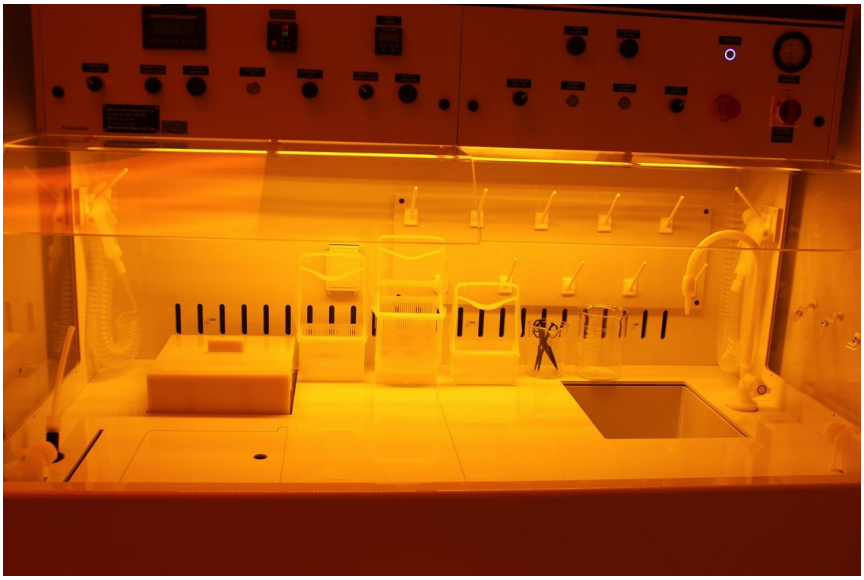


Figure A.1: Piranha wetbench at Quantom Nano Fabrication and Characterization Facility (QNFCF) clean room.

A.1.3 Acetone and Isopropyl Alcohol

The most commonly used cleaning process involves the use of acetone and isopropyl alcohol (IPA). This method is efficient and effective for removing residual photoresist. Acetone is not water-soluble, while IPA is miscible with water, which influences the cleaning sequence. Therefore, the process begins with acetone cleaning. If the photoresist on the sample is thick and covers a large area, immersion in a beaker of acetone is recommended. Alternatively, for thinner layers, pouring acetone from a wash bottle spray should suffice. This process is performed using solvent wet bench shown in Figure A.2.

Cleaning with IPA should immediately follow acetone cleaning to prevent the evaporation of acetone. The IPA should be applied uniformly over the entire sample, either by immersing the wafer in a beaker or by spraying it directly. This step is then followed by rinsing the sample with running DI water. The drying process is completed using a nitrogen gun to eliminate any water streaks on the wafer.

If the photoresist has been hard baked or subjected to a high-temperature process (such as DRIE), it may not be effectively removed using standard cleaning methods. In such cases, the sample should be submerged in a beaker of acetone and placed in an ultrasonic cleaning bath. It is important to note that the acetone solvent should not be heated due

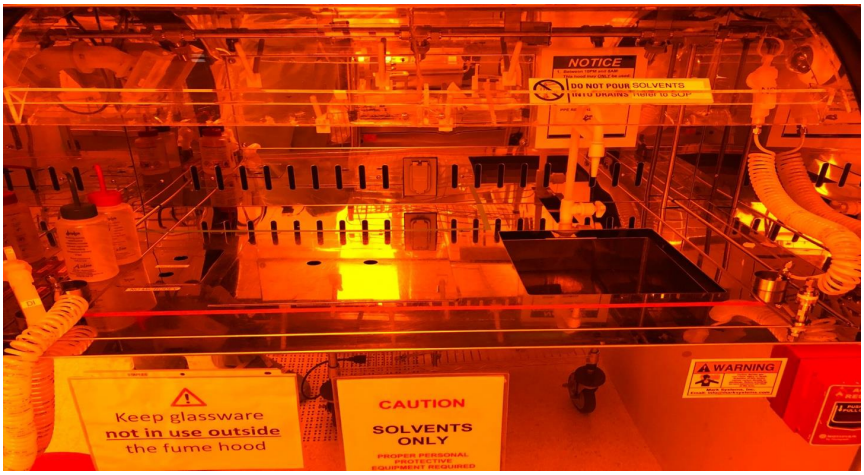


Figure A.2: Solvent wet bench where IPA and acetone should be used for cleaning purposes.

to its highly flammable nature. The ultrasonic power setting should be adjusted based on the features of the sample. If the sample does not have any fragile features, the ultrasonic power can be set to maximum. However, high power may cause significant damage to sensitive features and metallization. For instance, metalized sidewalls can be particularly vulnerable to high-power ultrasonic baths, depending on the characteristics of the sidewall features resulting from the DRIE process.

A.1.4 Remover PG

Another effective cleaning method for photoresist removal involves using a stripper known as Remover PG. This solvent is capable of efficiently removing PMGI, SU-8, and various other photoresist films from substrates such as silicon, silicon dioxide, gallium arsenide, and many others.

Remover PG is particularly effective on hardened resist films when used in conjunction with other accelerating factors such as heating, ultrasonic baths, and extended exposure times. A picture of a wet bench with a hotplate and ultrasonic bath is shown in Figure A.3. Heating the stripper to up to 80° on a hotplate or within an ultrasonic bath significantly enhances its effectiveness. For particularly stubborn resist, the sample can be immersed overnight to soften the photoresist. Following this, an ultrasonic bath—either heated or at room temperature—can be employed to effectively eliminate any remaining resist remnants.

It is important to handle this solution exclusively in a wet bench equipped with an

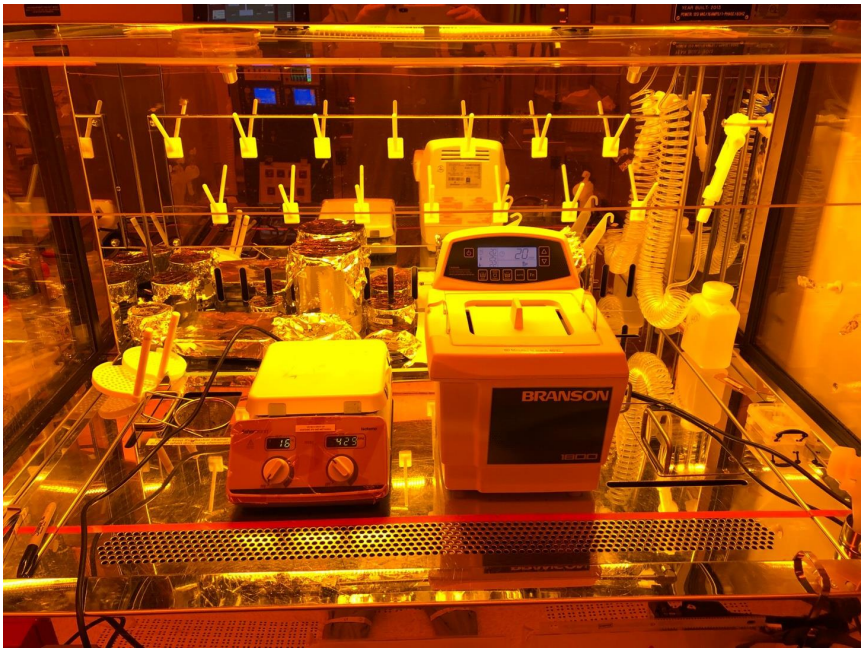


Figure A.3: Solvent wet bench with hot plate and ultrasonic bath for Remover PG use.

active fume hood, particularly when heated. After the photoresist is removed, the sample should be thoroughly rinsed with running DI water and then dried using a nitrogen blow to eliminate any residual moisture.

A.1.5 Plasma Clean

All the cleaning methods discussed thus far are wet processes. In contrast, a dry etch process known as O_2 plasma cleaning is employed for sample cleaning. This method is effective for removing polyimide and organic residues, performing photoresist descum, and activating surfaces prior to direct bonding.

For this process, the YES-CV200RFS O_2 plasma asher system is utilized, shown in Figure A.4. Within its chamber, gas atoms are excited to higher energy states and ionized, creating a plasma that consists of atoms, molecules, ions, electrons, free radicals, metastables, and photons. This mixture interacts with any sample placed inside the chamber, effectively cleaning and removing most organic contaminants and surface residues.

The Yes Asher tool features several preset recipes tailored for different cleaning scenarios. The most aggressive recipe operates at 1000 W RF power, with a sample temperature



Figure A.4: Yes Asher, a plasma cleaning tool at the QNFCF lab.

of 180°, a base pressure of 0.001 torr, and an O_2 flow rate of 20 SCCM for a duration of 10 minutes. This recipe is effective for hard-baked photoresists; however, if the resist layer exceeds $> 15\mu m$ in thickness, it may not achieve optimal cleaning results. In such cases, it is advisable to use heated Remover PG with an extended exposure time. Additionally, low-temperature and shorter-duration recipes can be employed following the removal of photoresist using acetone and IPA to ensure a thoroughly cleaned sample.

A.2 Spin Coating, Exposure, and Development

After thorough cleaning, the wafer or sample must undergo a dehydration process. This involves heating it on a hotplate at 110° for 5 minutes to completely eliminate any residual water. Failing to perform this step may result in the sliding of photoresist features during subsequent processing. The spin coating profiles and exposure parameters vary depending on the specific resists and thicknesses used. Therefore, the details of the photolithography process for the photoresists predominantly utilized in this research are presented in the following sections. For spin coating and baking process, the Brewer Science Spin Coater and Hotplate is used, shown in Figure

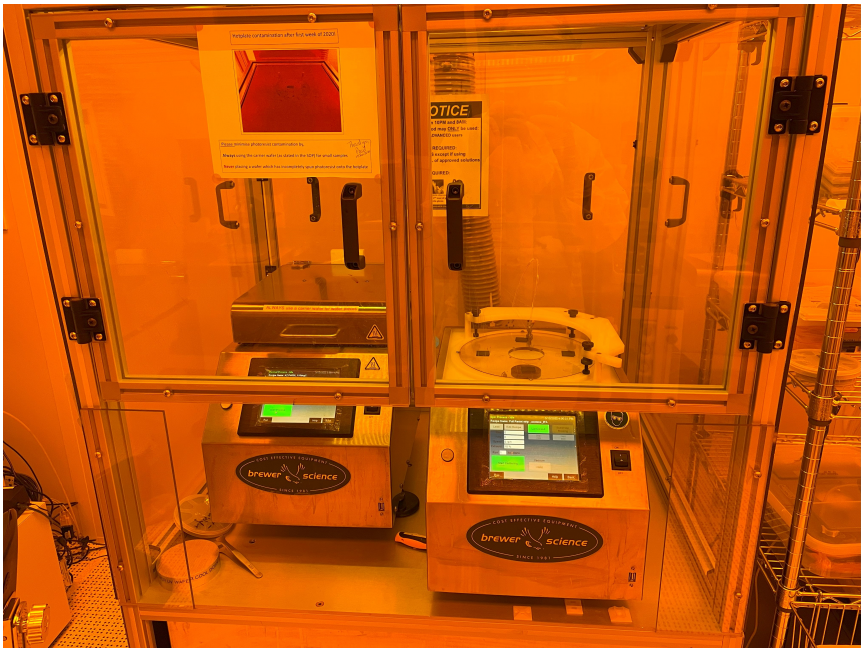


Figure A.5: Brewer Science Spin Coater and Hotplate at the QNFCF lab.

A.2.1 AZ P4620 - Positive Photoresist

This photoresist is a positive resist known for two primary characteristics. First, it exhibits excellent adhesion to a wide range of substrates, enhancing stability during wet etching or plating processes. Second, it features a lower concentration of photoactive compounds, enabling the formation of thick films up to $30\mu m$. This makes the photoresist particularly

suitable for applications such as DRIE etching, electroplating, and thick metallization lift-off processes.

This resist has been utilized in this research with varying thicknesses, ranging from $6\mu m$ to $22\mu m$. To achieve a thick resist film, a slower spin coating speed is necessary. However, this approach can lead to the formation of a thick edge bead, which presents several challenges, including wasted area around the edges and bubbling issues during the DRIE process. Conversely, increasing the spin speed while reducing film thickness results in a thinner and narrower edge bead. It is important to note that effective etching through the wafer using DRIE requires a sufficiently thick photoresist film.

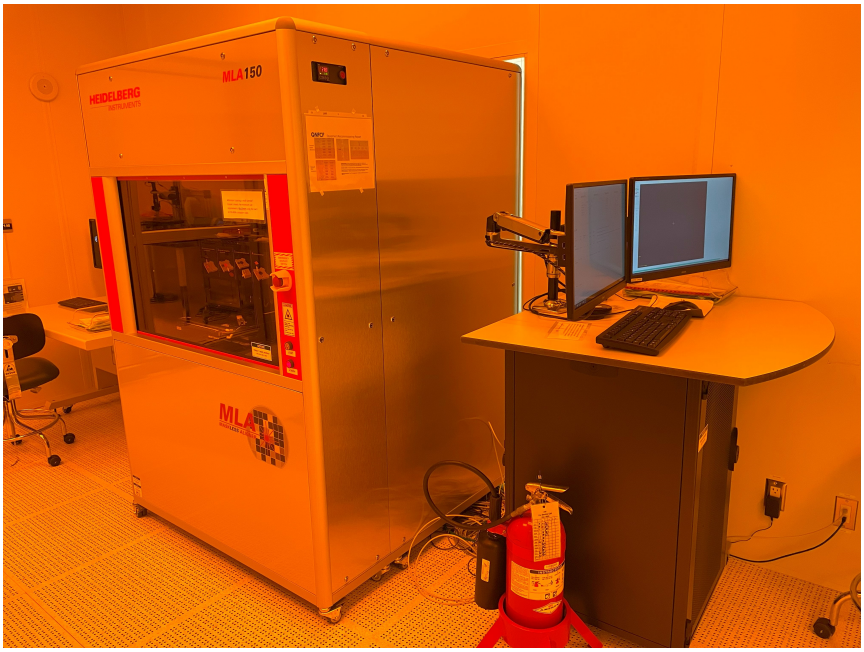


Figure A.6: Heidelberg MLA150 Maskless Aligner used for exposure.

After conducting several photolithography and DRIE etch processes, it was concluded that thicker films could be more effectively produced by applying multiple layers of a thinner photoresist. This approach results in thinner and narrower edge beads while still achieving the desired overall thickness. The spin coating and pre-bake profiles for this resist are detailed in Table A.1. To attain a photoresist thickness of 22-24μm, the second profile must be repeated four times.

In this study, the Heidelburg MLA 150 maskless aligner is employed to expose the desired patterns on the photoresists. This tool is shown in Figure A.6 inside the QNFCF

Table A.1: Spin coating parameters for AZ P4620 photoresist at two thicknesses

Step	14-16 μm Thickness			6-7 μm Thickness		
	Speed (RPM)	temp (°)	Time (s)	Speed (RPM)	Temp (°)	Time (s)
Spin 1	200	20	2	500	20	2
Spin 2	500	20	5	1000	20	5
Spin 3	1000	20	60	6000	20	60
Spin 4	500	20	5	500	20	5
Pre-Bake	NA	110	80	NA	110	80

lab. The light parameters, including exposure dose and defocus, are adjusted according to the thickness of the photoresist. A summary of the exposure parameters is provided in Table A.2.

Table A.2: MLA 150 Exposure Parameters for AZ P4620.

Parameter	6-7 μm	14-16 μm	22-24 μm
Light (nm)	405	405	405
dose (mJ/cm^2)	300	600	800
defocus	0	1	2

It is important to note that as the thickness of the photoresist increases, the minimum achievable feature size also increases. Based on the findings of this research, feature sizes as small as $5\mu m$ can be achieved with the thinnest resist; however, the exact exposure parameters may need to be fine-tuned by the user for optimal results. Figure A.7 shows a spin-coated and exposed sample before development.

The development of this photoresist is carried out using AZ-400K MIF in a 4:1 solution. It is observed that the development time increases with the thickness of the photoresist. A brief summary of the development times for various photoresist thicknesses is provided in Table A.3

Table A.3: AZ P4620 Development Time.

Resist Thickness	6-7 μm	14-16 μm	22-24 μm
Development time	120s	270s	360s

As a special consideration, incorporating a thin layer of aluminum beneath the photoresist layer can enhance the quality of the etched features. While it might appear simpler to use only an aluminum hard mask, this approach can lead to micro-masking, negatively affecting the quality of the silicon wafer for subsequent layers. Conversely, relying solely

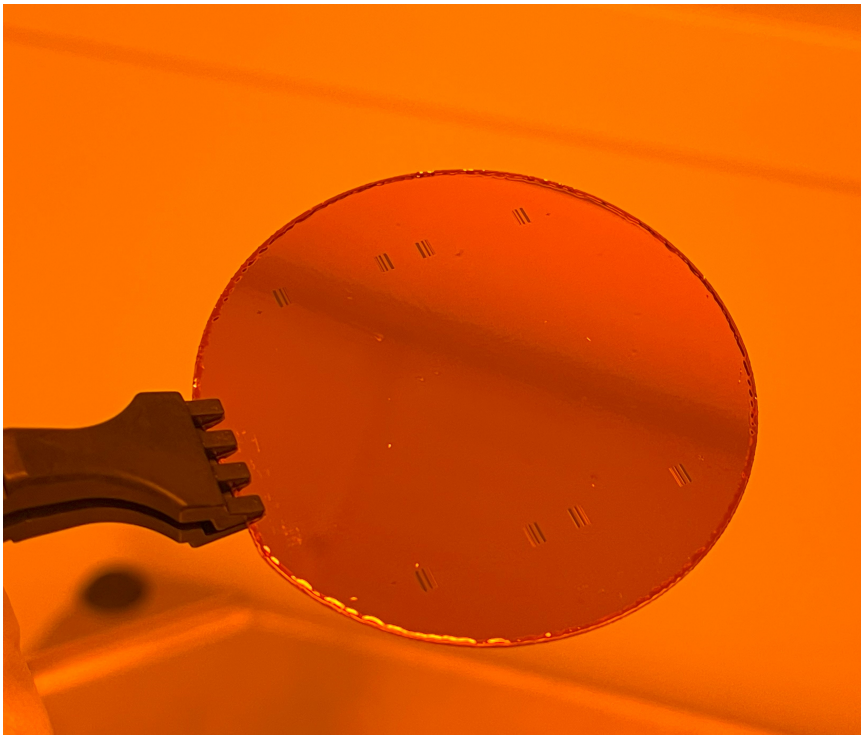


Figure A.7: A sample with spin-coated AZ-P4620 after exposure, before development.

on photoresist can result in distorted shapes due to the high temperatures involved in the Deep Reactive Ion Etching (DRIE) process. This distortion is particularly problematic because the etching cycle required to fully penetrate a silicon wafer typically ranges from 800 to 1000 cycles.

A.2.2 AZ nlof2035 - Negative Photoresist

This photoresist is a negative resist, typically applied at a thickness of 3.5 μm. A key characteristic of negative resists is their ability to create undercuts, making them particularly suitable for lift-off processes. This specific resist supports the fabrication of high aspect ratio features, enabling the creation of small, intricate patterns. Additionally, it possesses excellent thermal stability, ensuring that the features remain unaffected during high-temperature processing.

In this research, this photoresist was utilized to fabricate small feature sizes, achieving dimensions as small as 2 μm. Figure A.8 shows a sample with meander lines with 3μm fea-

ture size. The recipe employed for this purpose is detailed in Table A.4, which summarizes the spin coating parameters for this resist.

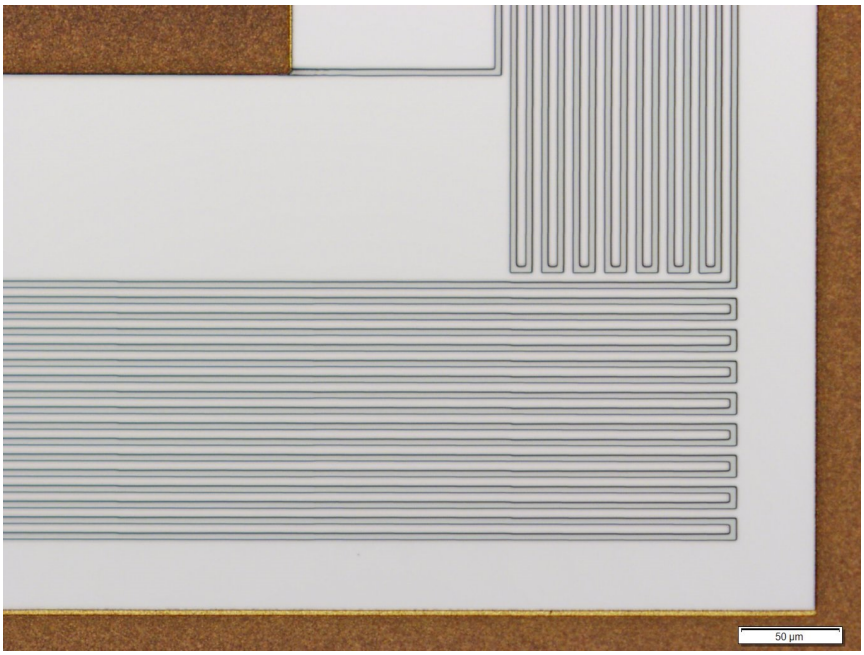


Figure A.8: Small feature sizes of $3\mu m$ achieved using AZ-nlof2035 negative photoresist.

Table A.4: Spincoating parameters for AZ nlof2035 photoresist.

Step	2.5 μm Thickness		
	Speed (RPM)	temp (°)	Time (s)
Spin 1	500	20	2
Spin 2	1000	20	5
Spin 3	5000	20	60
Spin 4	500	20	5
Pre-Bake	NA	110	60
Post-Bake	NA	110	60

It is important to emphasize that a post-exposure bake is essential for this photoresist. Neglecting this step can lead to the complete removal of the photoresist layer. The cross-linking process begins during exposure but is not fully completed until the post-exposure bake is performed. Extending the baking time, increasing the temperature, or using a combination of both can result in a hardened photoresist, making the removal process more challenging and potentially damaging to previously defined features on the sample.

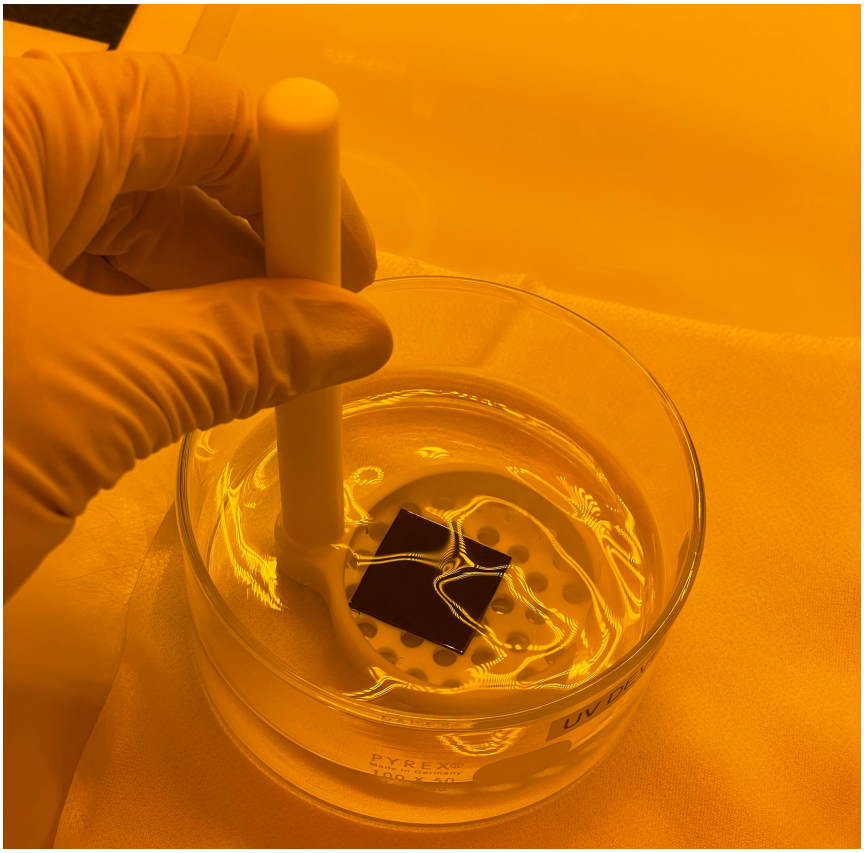


Figure A.9: A sample in a developer beaker during the development process.

Table A.5: MLA 150 Exposure Parameters for AZ nlof2035.

Parameter	2.5 μm thickness
Light (nm)	375
dose (mJ/cm^2)	350
defocus	-2

The parameters utilized in the MLA 150 tool are detailed in Table A.5. While these parameters served as a foundation for this research, they can be adjusted and refined according to specific design requirements. The development of this resist is carried out using the AZ 300MIF developer in a 3:1 dilution, shown in Figure A.9. The standard development time is typically 120 seconds. However, for a more conservative approach, immersion in the developer for 90 seconds is recommended. If further development is necessary due to rough or inadequately developed features, an additional 30 seconds may

be applied.

A.3 Lift-Off Process

The lift-off process is a technique used to pattern a deposited layer on a substrate. This method is considered additive, as opposed to traditional subtractive techniques such as etching. In this context, the photoresist acts as a sacrificial layer to create the desired pattern. One of the primary advantages of the lift-off method is that it eliminates the need for etchants, whether they are wet etchants like acids or dry etchants such as ion beam milling or metal reactive ion etching (RIE). In certain situations, the use of etchants may be impractical or detrimental to the sample. For instance, when gold is present on the sample, employing a metal RIE tool is prohibited. Similarly, when chromium is on the sample and a new layer of chromium is needed, using a wet etching process for patterning the new layer can be destructive.

Negative photoresists are ideally suited for the lift-off process due to their undercut profile. Although positive photoresists can also be used and have occasionally been paired with the lift-off method, they tend to yield lower success rates in thicker depositions. The inherent undercut of negative photoresists provides better adhesion and pattern fidelity, making them more effective for this application.

The lift-off process necessitates inverse pattern photolithography, meaning that the pattern created with the photoresist is the inverse of the desired final pattern. Deposition of the material can be achieved using either electron beam (E-Beam) evaporation or sputtering methods. Among these, E-Beam evaporation is generally considered the most effective for lift-off, as it minimizes sidewall coverage. This characteristic allows for easier removal of the deposited material from the photoresist, separating it from the substrate. However, in cases where large steps exceed the thickness of the deposited layer and sidewall coverage is critical, employing a sputtering system becomes essential.

After completing the photolithography and depositing the desired layer, the next step is to remove the photoresist along with any unwanted deposited material. This involves immersing the sample in a solution that gradually dissolves the photoresist. It is crucial to note that using acetone for the lift-off process can lead to unwanted overlays. This issue arises because acetone dissolves the photoresist quickly but unevenly, which can cause portions of the deposited material to fold back onto other areas of the sample. To mitigate this problem, it is advisable to use heated Remover PG instead. Depending on the temperature of the deposition process, the sample may need to be left in the Remover

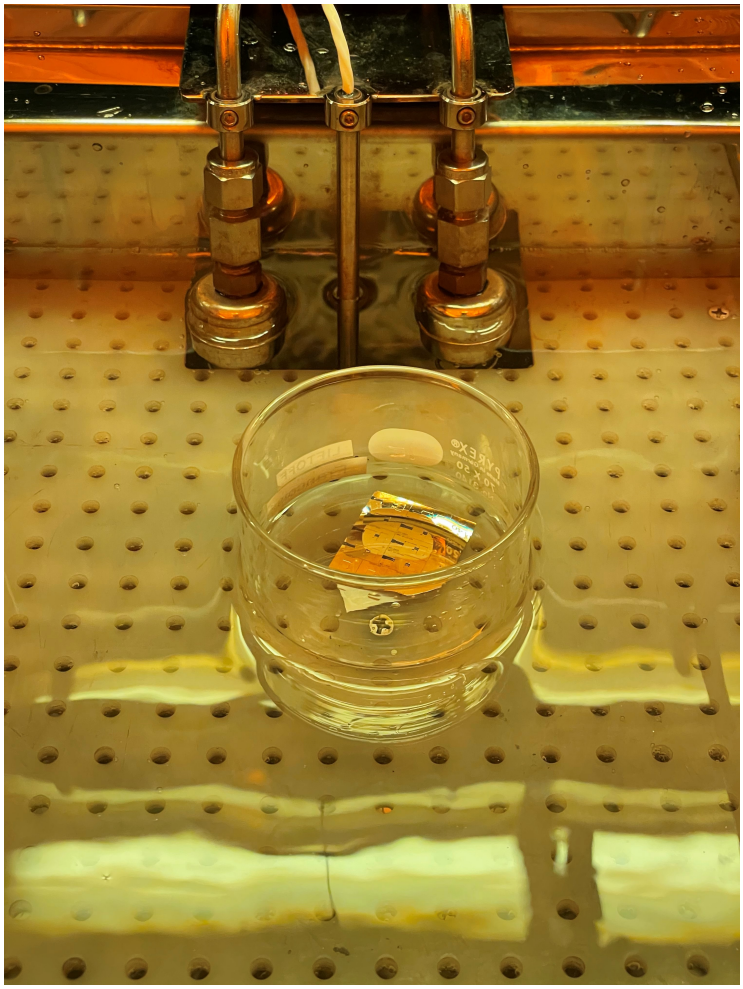


Figure A.10: Using ultrasonic bath to accelerate lift-off process.

PG solution overnight or with the help of an ultrasonic bath, as shown in Figure A.10 to ensure complete lift-off. A close photo of the lift-off process in Figure A.11 reveals the separation of an unwanted deposited metal layer inside the remover PG beaker.

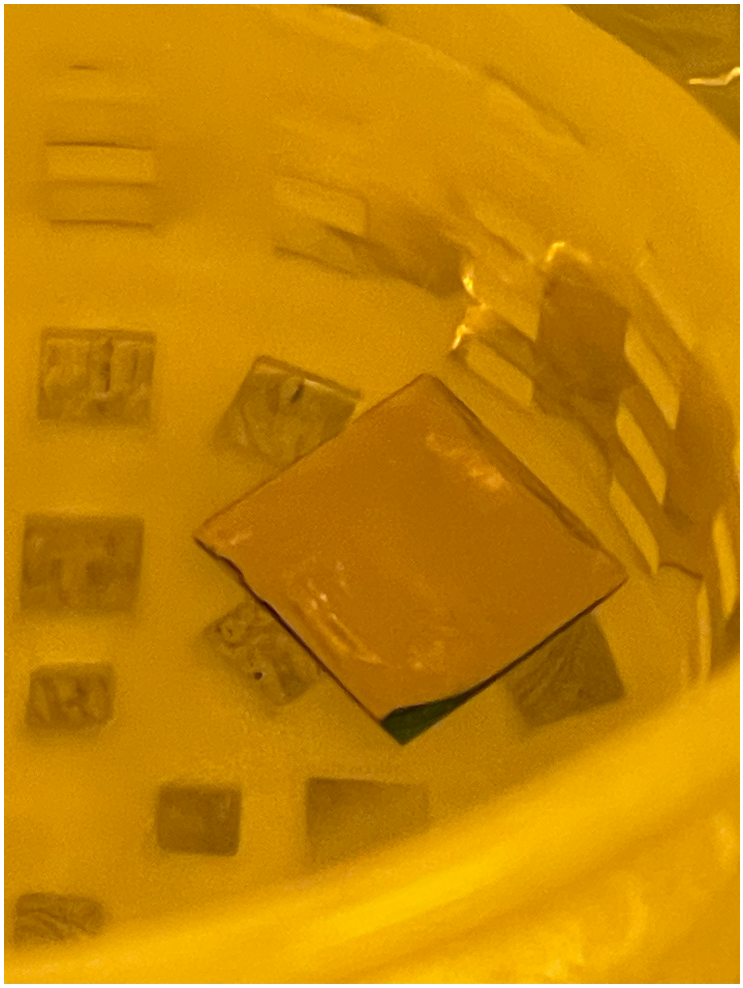


Figure A.11: A sample in Remover PG beaker during lift-off process.

Appendix B

LC Filling Procedure

Filling micromachined devices with LC material is a process that should be executed carefully to ensure optimal performance. Depending on the size of the fabricated device, one of the methods described in the following sections can be employed.

B.1 Large Samples

Since handling large devices is easier, they can be filled using a microsyringe. The main advantage of this method is that the waste of LC material is kept to a minimum compared to other filling techniques. However, this comes at the cost of filling each sample individually, which may be time-consuming and inefficient.

The syringe used for this purpose should have a needle diameter smaller than the filling holes on the fabricated devices. The volume of the syringe should also be very small, as the LC-based micromachined devices utilize a small amount of LC material. This will make it easier to inject the required volume of LC into each device while avoiding spills or overfills. It is important to note that to use this filling method, the fabricated device should incorporate at least two filling holes. Otherwise, the injected LC material will not enter the designed cavity.

The initial devices in this research were filled using a 10 μL syringe. The needle attached to the syringe had a diameter of 200 μm, which was smaller than the filling hole diameter of the devices at 250 μm. To ease the filling procedure, the first set of devices had five filling holes, as shown in Figure B.1. Considering the square shape of the LC

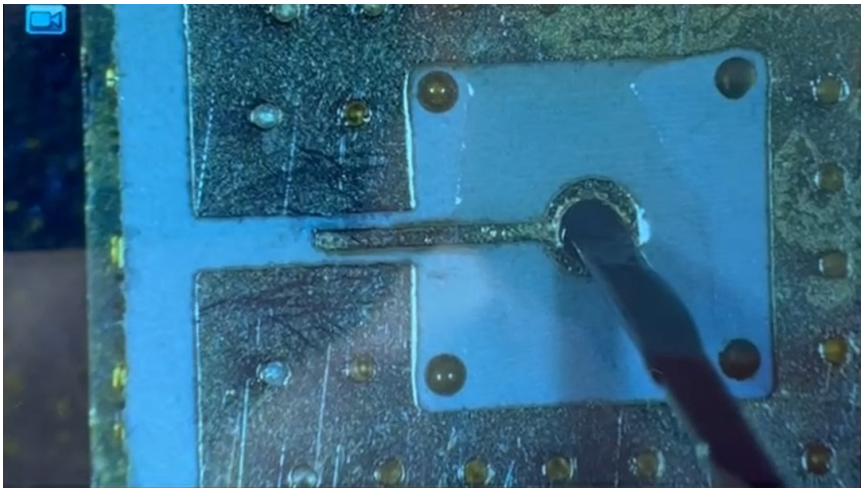


Figure B.1: Filling a $5.5 \times 5.5mm^2$ sample using μsyringe.

cavity footprint, four holes were placed at the corners, and one hole was positioned in the middle, incorporated by the metalized via.

The exact amount of required LC should be injected into the middle hole. The LC cavity of the initial shunt capacitor, for example, had dimensions of $1.6 \times 1.6 \times 0.1mm^3$. The volume of this cavity is only $0.256\mu L$. Considering filling all holes to the top, that device could have used $0.413\mu L$ of LC material.

After injecting the LC material, the filled devices should undergo low-pressure vacuum conditions to avoid any bubbles inside the cavity. Any air and bubbles will be drawn out of the LC cavity when the device is placed in the vacuum chamber. However, another LC injection may be required to ensure that all areas previously occupied by air are filled with LC material. This process can be repeated multiple times until no air emerges from the filling holes during vacuum conditions.

B.2 Small Samples

When dealing with small devices where the filling holes are also extremely small, the use of a microsyringe may not be applicable. Firstly, the LC volume used in such devices is very small and cannot be handled with microsyringes. In addition, finding a properly sized needle that fits the small filling holes can be challenging. As a result, another method should be employed to fill small devices more effectively.

To fill the small-sized packaged devices, they should be immersed in LC material. For this purpose, the LC material should be poured into a container that is deep enough with a small cross-section. It should be able to contain the LC material to a height of 5 to 10 times the height of the packaged device to avoid filling issues. A smaller cross-section reduces the waste of LC material after the filling process. The phase shifter at 62 GHz, for example, had dimensions of $2.05 \times 1.48 \times 0.56 mm^2$, and the filling hole diameters were only $100 \mu m$. For this process, a beaker with a base diameter of 20 mm and a height of 30 mm was used; however, the LC was only filled to a height of 4 mm.

To begin, the fabricated chips should be placed at the bottom of the beaker. Then, the LC material should be filled to an appropriate level to provide enough headroom above the chips. The beaker will then be placed in a vacuum chamber. As the pressure decreases, the trapped air inside the cavities of the devices will start to bubble out. It may be necessary to reach a pressure of 1×10^{-6} and maintain this condition for 10 minutes. This process will create a vacuum inside the cavities while the filling holes remain covered with LC material. After venting the chamber, the increased pressure will force the LC material into the evacuated LC cavity. This process can be repeated several times to ensure a bubble-free LC cavity.

Besides handling small devices, this method can fill multiple devices at once, reducing the overall time required to fill many chips. However, most of the LC material used is wasted, as the overall used LC volume is very limited. The 62 GHz phase shifter, for instance, has two cavities with dimensions of $0.6 \times 1.3 \times 0.02 mm^3$, which equals $0.0156 \mu L$. Considering the total LC material used in the beaker is $1257 \mu L$, even filling 50 devices at once may consume only 0.12%, leaving 99.88% of the LC material wasted. Therefore, this method is best employed with as many devices as possible in a single run to minimize LC material usage.

B.3 Sealing holes

Filling holes should be sealed after the cavity is filled with LC material to avoid evaporation and loss of performance over time. To facilitate this, the filling holes should be as small as possible to minimize challenges during the sealing process. The holes can be plugged using various types of adhesives; however, it is advisable to use a special type of glue designed for LC-based devices. The main feature of such glue is that it will not mix with the LC material and remains separated in liquid form before it hardens. For this purpose, the NOA/UVS 91 adhesive made by Norland is used. This glue is in a soft liquid form and requires UV light for the curing process.