Frequency Multiplier-Based RF Beamforming Front-End for Vector Modulated Signal Transmission

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

In the rapidly evolving era of wireless communications, the advent of sixth-generation (6G) technology promises unprecedented advancements in terms of high data rates and ultra-low latency, which will lead to significant improvement in different applications such as internet-of-things, autonomous driving, and virtual/augmented reality. The key enabler for these advancements lies in exploiting the untapped spectrum bands at millimeter-wave (mm-wave) and sub-terahertz (sub-THz) frequency bands to meet the new stringent data rate and latency requirements. Nevertheless, generating highly-efficient vector modulated signals at these elevated frequency bands face different challenges. For example, the increased free-space path loss and the degradation of the RF performance of most semiconductor technologies at these bands hinder the generation of high-quality signals with sufficient output power. Additionally, vector modulated signals suffer from a high peak-to-average-power ratio, necessitating more strict linearity requirements. Therefore, in light of these challenges, the development of transmitter front-ends capable of surmounting these obstacles becomes imperative to meet the stringent demands of high data rates and ultra-low latency of future wireless communication.

Existing front-end solutions in the literature faced different limitations hindering their applicability to generate signals at the targeted frequencies that satisfy the stringent requirements. The aim of this thesis is to develop a frequency multiplier-based RF beamforming front-end suitable for vector modulated signal transmission and to design frequency doublers capable of generating vector modulated signals with adequate output power, power efficiency, and linearity.

This thesis begins with proposing a new design methodology for designing high-efficiency frequency doublers with improved phase distortion characteristics (AM-PM). The proposed methodology defines the current and voltage waveforms at the output of the transistor to guide the selection of harmonic load impedance terminations that can maintain consistent output power and power efficiency over the designated bandwidth. Then, it formulates the AM-PM characteristics of the frequency doublers, taking into account the transistor parasitic input capacitance, to explore the optimum choice of the harmonic source impedance termination that minimizes the AM-PM nonlinearity. Using the proposed methodology, frequency doublers targeting the V-band frequency range (50-75 GHz) were designed. Their measurement results showed promising RF performance in terms of output power, power efficiency, and conversion gain. Moreover, by employing digital pre-distortion (DPD) linearization technique, the fabricated frequency doublers were able to generate vector modulated signals with acceptable error vector magnitude (EVM) and average efficiency.

Next, the thesis delves into the design considerations of the phase shifters in the context of frequency multiplier-based front-end. A comprehensive study of the different reflective-type phase shifter (RTPS) topologies is conducted to guide the selection of the optimum topology that would meet the pre-defined design constraints. Accordingly, an RTPS tailored for a frequency multiplier-based front-end was designed, and its performance was validated experimentally. Subsequently, a proof-of-concept demonstration of a V-band RF beamforming front-end module was developed, consisting of a cascade of phase shifter, driver amplifier, and frequency doubler. The RF beamforming demonstration showed the ability to cover a 360° phase tuning range with high gain and phase accuracy. Also, it effectively generated a vector modulated signal with a flat EVM across the full 360°. To the best of our knowledge, this thesis represents the first reported phase measurements of a frequency doubler.

Lastly, this work advances to even higher frequencies by designing frequency doublers targeting the D-band frequency range (110-170 GHz). The transition to higher frequency evolved different design challenges. Hence, a novel design approach for designing frequency doublers was developed. This approach explores a solution for the harmonic source impedance termination that is practically realizable at such elevated frequencies. The proposed approach was applied to the design of two frequency doubler prototypes targeting an output frequency of 120 GHz. The first prototype was a stand-alone frequency doubler while the second one used a pre-driver amplifier in cascade with the frequency doubler to enhance the overall gain. These prototypes were validated experimentally, reporting promising output power and power efficiency at the D-band frequency range. Also, by utilizing the DPD linearization technique, they successfully generated vector modulated signals with acceptable performance metrics at this elevated frequency range.

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Dedication

To my family and friends.

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Nomenclature

3GPP	Third Generation Partnership Project
5G	Fifth Generation
6G	Sixth Generation
ACPR	Adjacent Channel Power Ratio
ADCs	Analog-to-Digital Converters
AWG	Arbitrary Waveform Generator
CG	Conversion Gain
CMOS	Complementary Metal-Oxide Semiconductor
CPW	Co-Planar Waveguide
CW	Continuous-Wave
DPD	Digital Pre-Distortion
DUT	Device-Under-Test
EIRP	Effective Isotropic Radiated Power
EM	Electromagnetic
EVM	Error Vector Magnitude
FM	Frequency Multiplier
FMCW	Frequency-Modulated Continuous-Wave

FSPL	Free-Space Pass Loss
GHz	gigahertz
IF	Intermediate Frequency
IL	Insertion Loss
InP	Indium Phosphide
IoT	Internet-of-Things
LO	Local Oscillator
LUT	Look-Up-Table
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
NVNA	Nonlinear Vector Network Analyzer
OFDM	Orthogonal Frequency Division Multiplexing
OOK	On-Off-Keying
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PS	Phase Shifter
PSD	Power Spectrum Density
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMS	Root-Mean-Square
RTPS	Reflective-Type Phase Shifter
SC	Switched-Controlled
SOI	Silicon-on-Insulator

STPS	Switched-Type Phase Shifter
THz	terahertz
TL	Transmission Line
Tx	Transmitter
VNA	Vector Network Analyzer
VR/AR	Virtual/Augmented Reality

Chapter 1

Introduction

1.1 Motivation

The successful deployment of the fifth generation (5G) of wireless mobile communication in realizing ultra-reliable low-latency communication and enhanced system capacity has spurred significant research interest to investigate more solutions for improvements. Hence, the sixth generation (6G) of wireless communication, considered the future successor of 5G, is currently under development and is expected to provide higher data rates and reduced latency that will lead to significant improvements in different applications such as internet-of-things (IoT), autonomous driving, and virtual/augmented reality (VR/AR). The transition to the emerging 6G mobile communication calls for greater data bandwidth to meet the strict data rates and latency requirements. However, such bandwidth can't be achieved using the crowded sub-6 GHz frequency bands. This motivated the expansion to the untapped spectrum bands at millimeter-wave (mm-wave) and sub-terahertz (sub-THz) frequency bands (24-300 GHz) since they can offer several gigahertz (GHz) of bandwidth compared to the lower frequency bands. Figure 1.1 shows the anticipated 6G spectrum grouping [1]. It emphasizes the shift towards mm-wave and sub-THz frequency bands, showing their substantially expanded bandwidth in contrast to lower frequency bands. This expansion facilitates the realization of high data rates (up to 1 terabit per second (Tb/s)) and ultra-low latency which enables the provision of ultra-fast wireless communication. Nevertheless, Figure 1.1 also shows the limited coverage at high-frequency bands which is due to the significant challenges facing the generation of a high-quality signal with sufficient output power at these frequency bands. The challenges are mainly caused by: (i) the increased free-space pass loss (FSPL) and (ii) the degradation of the radio

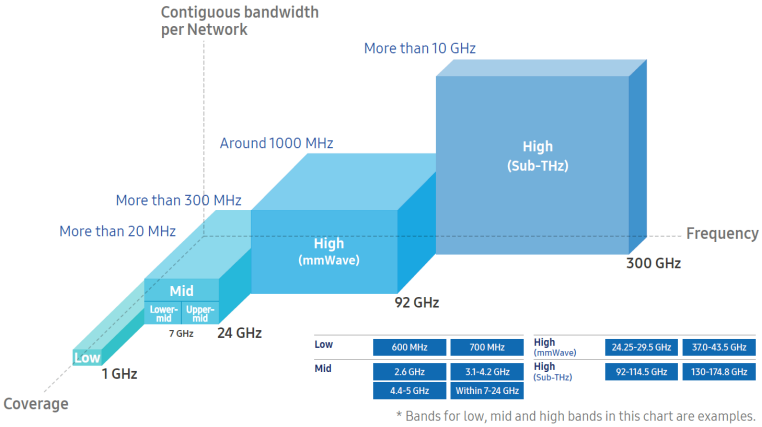
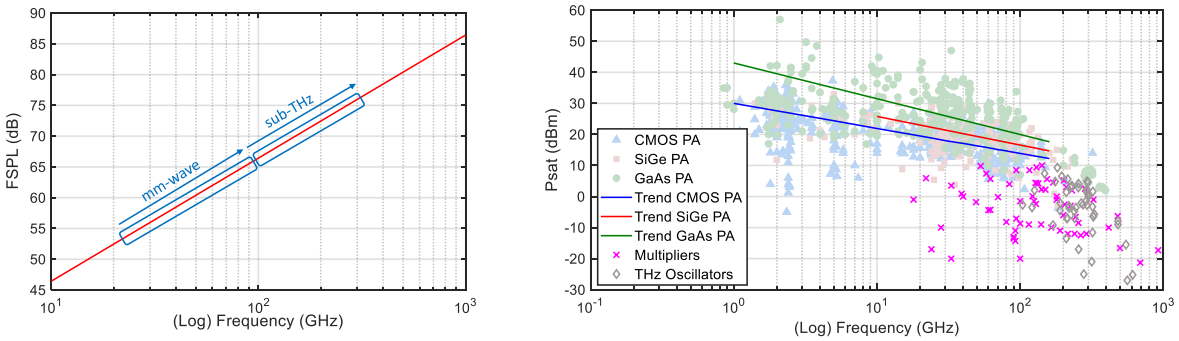


Figure 1.1: Three dimensions of 6G spectrum grouping [1].



(a) Free-space pass loss.

(b) Saturated output power [2].

Figure 1.2: Challenges imposed by the transition to high-frequency bands.

frequency (RF) performance (i.e., output power, power efficiency, and gain) of most semiconductor technologies as the operating frequency increases approaching the maximum oscillation frequency (f_{max}) of the transistor. Figure 1.2 depicts graphically these two challenges. Figure 1.2a highlights the increased FSPL as we move to mm-wave and sub-THz frequency bands. While Figure 1.2b shows the saturated output power of different transmitter building blocks and confirms the significant performance degradation with the transition to these frequency bands [2].

Another essential criterion for maximizing the data rate and system throughput of wireless mobile communication is to generate signals with high spectral efficiency. Such signals can be obtained using high-order vector modulation schemes, such as 64-quadrature ampli-

tude modulation (64-QAM) and 256-QAM, and multi-carrier schemes, such as orthogonal frequency division multiplexing (OFDM). However, spectrally efficient signals suffer from a high peak-to-average power ratio (PAPR). As a result, the transmitter front-end (e.g., the power amplifier (PA)) has to operate at large power back-off levels. Unfortunately, the power efficiency of a typical PA drops significantly as the output power is backed-off from its peak value. Figure 1.3 shows the drain efficiency of an ideal Class-B PA versus the normalized output power. It demonstrates that the efficiency drops from 78.5% at peak power to 24.8% at 10-dBm output power back-off. Thus, the high PAPR of spectrally efficient signals imposes strict linearity requirements on the design of the transmitter front-end.

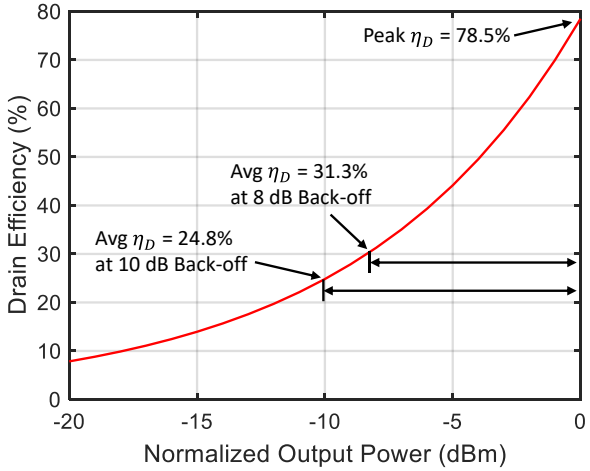


Figure 1.3: Drain efficiency of ideal Class-B PA versus the normalized output power.

1.2 Problem Statement

As discussed in Section 1.1, while the future 6G wireless mobile communication offers significant improvements in terms of the system capacity and quality of service, the resulting data rates, latency, and linearity requirements impose new challenges to the design of the transmitter. Hence, there is a need to design a highly-efficient transmitter front-end that is suitable for high-frequency vector modulated signal transmission. To generate a high-frequency signal, different front-end architectures have been investigated in the literature. The most commonly-used architecture utilizes a PA as a last stage [3]. The maximum operating frequency of the PA should be significantly lower than the maximum oscillation

frequency of the technology to ensure acceptable RF performance. As the operating frequency increases, designing a high-power PA with acceptable power efficiency and linearity represents a bottleneck that restricts the use of this architecture to generate low-order modulated signals. Using III-V technology, it is possible to overcome some of the challenges; however, the associated cost overhead limits its applicability to large-scale antenna-array systems. It is, hence, important to explore alternate complementary metal-oxide semiconductor (CMOS)-based front-end architectures. One proposed solution in the literature is to use a nonlinear harmonic mixer at the front-end output [4]. This architecture allows for high-frequency operation close to f_{max} of the technology. Nevertheless, it suffers from significant spurious frequencies which will require lossy high-order filters to attenuate the spurious signals near the targeted frequency band. The limitations of the previous two front-end architectures motivated the use of frequency multipliers as a last stage for frequency up-conversion [5]. In such architecture, all stages preceding the frequency multiplier will operate at an intermediate frequency lower than the targeted operation frequency, resulting in improved RF performance. However, the strong nonlinearity exhibited by the frequency multiplier restricts its application to generating constant-envelope signals with low output power and power efficiency.

This thesis presents the design of a frequency multiplier-based front-end suitable for high-frequency vector modulated signal transmission. It presents novel design methodologies for designing frequency doublers capable of generating vector modulated signals with high output power and power efficiency while maintaining acceptable bandwidth. To address the challenges of increased FSPL and performance degradation at the mm-wave and sub-THz frequency bands, advancements are required at the device, circuit, and system design levels of RF technologies. At the device and circuit levels, choosing a semiconductor fabrication process with improved active and passive components and developing new circuit techniques with improved RF performance will reduce parasitic losses and consequently provide high output power. At the radio system design level, beamforming architectures (e.g., RF, hybrid, and digital) have been adopted by literature to enable directed radiation that maximizes the output power and mitigates the impact of increased FSPL with the operating frequency. Amongst these, RF beamforming architectures have gained significant traction at the mm-wave and sub-THz frequency bands due to their low complexity and cost compared to their counterparts. Hence, this thesis proposes incorporating the frequency multiplier-based front-end in an RF beamforming structure. Moreover, to address the frequency multiplier nonlinearity and to tackle the problem of high PAPR of vector modulated signals, this thesis uses a digital pre-distortion (DPD) linearization technique to improve the linearity of the targeted front-end design and generate high-order vector modulated signals.

1.3 Thesis Outline

This thesis is organized as follows. Chapter 2 presents a general overview of the front-end architectures employed for high-frequency signal generation. This is followed by a survey on the power-combining techniques that boost the front-end's output power. Building upon these discussions, the thesis will focus on the integration of frequency multipliers into an RF beamforming structure, exploring the various circuit-level designs for frequency multipliers and phase shifters.

Chapter 3 proposes a novel methodology for designing frequency doublers that provide high output power and power efficiency over a designated bandwidth. A waveform engineering technique is utilized to guide the selection of the harmonic load impedance terminations across frequencies. Moreover, to support the generation of vector modulated signals, the proposed methodology addresses the phase distortion characteristics (AM-PM) of frequency doublers through formulation to define the optimum harmonic source impedance terminations. This methodology will guide the design of frequency doublers targeting the D-band frequency range (50-75 GHz).

Chapter 4 presents the design considerations of the phase shifters in the context of frequency doubler-based RF beamforming front-end. Accordingly, an extensive study on the different topologies used to implement a reflective-type phase shifter (RTPS) is detailed and an RTPS design is developed based on this study. Additionally, a proof-of-concept demonstration of a 60-GHz frequency doubler-based RF beamforming front-end module is designed which consists of a phase shifter, driver amplifier, and frequency doubler.

Chapter 5 proceeds one step further in frequency by addressing frequency doublers targeting the D-band frequency range (110-170 GHz). Due to the design challenges at this frequency range, the chapter proposes a new design approach that guides the choice of the harmonic source impedance terminations to more realistic solutions that can be realized practically. Accordingly, frequency doublers operating around an output frequency of 120 GHz are developed to validate the proposed design approach.

The contribution of this work to the field is summarized in Chapter 6. Besides, possible directions for future research work on this topic are discussed.

Chapter 2

Front-End Architectures for High-Frequency Signal Generation

2.1 Introduction

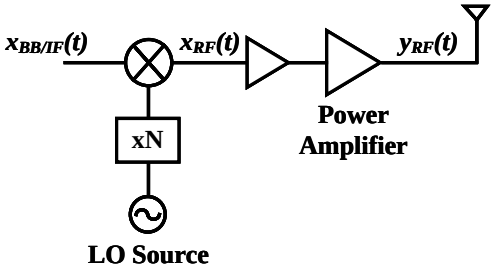
As mentioned in Chapter 1, future 6G wireless mobile communication has been experiencing stringent requirements of high data rate and ultra-low latency leading to the transition to mm-wave and sub-THz frequency bands since they can offer several GHz of bandwidth compared to the lower frequency bands. However, generating a high-quality signal with sufficient output power at these frequency bands faces significant challenges due to the increased FSPL and the low performance of silicon-based technologies. It is possible to overcome some of these challenges using expensive III-V technologies; however, their associated cost limits their applicability to large-scale antenna-array systems. This motivated the investigation of novel CMOS-based front-end architectures to efficiently generate high-power and wideband vector modulated signals. This chapter presents a review of the existing architectures together with a summary of relevant recent publications. In addition, the power combining techniques used to enhance the front-end's output power are discussed to tackle the increased FSPL at high frequencies. This is followed by an extensive literature review on the circuit-level designs of the key building blocks of frequency multiplier-based RF beamforming front-end that will guide us in designing a high-performance architecture.

2.2 High-Frequency Signal Generation

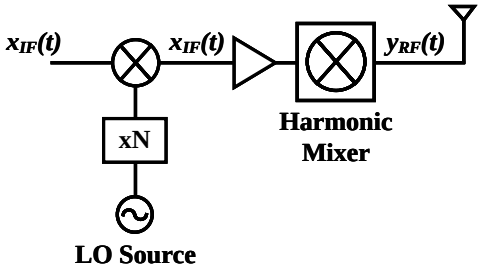
Figure 2.1 shows the three front-end architectures adopted by literature for high-frequency signal generation. They are classified into: i) power amplifier-based (PA-based) architecture which uses a PA as a last stage, ii) harmonic mixer-based architecture, and iii) frequency multiplier-based architecture utilizing a frequency multiplier as a last stage for frequency up-conversion.

Figure 2.1a depicts the conventionally-used PA-based front-end architecture. In this architecture, the frequency up-conversion is performed using a mixer driven by a high-frequency local oscillator (LO) signal generated using a cascade of frequency multipliers and a low phase-noise LO source. The PA is utilized as a last stage for signal transmission and consequently has to operate at the targeted mm-wave/sub-THz frequency ranges. This brings the challenge of building high-power PA stages with acceptable power efficiency and linearity. Hence, the limited PA performance restricted the application of this architecture to generating low-order modulation schemes with either constant envelope signals or low envelope variation signals [3, 6–12]. For instance, the authors in [8] and [9] deployed the architecture in Figure 2.1a to design a transmitter (Tx) front-end centered at an operating frequency of 240 GHz and 300 GHz, respectively. However, the demonstrated results were limited to generating low-order modulated signals such as quadrature phase shift keying (QPSK). On the other hand, the authors in [10] and [11] proposed ultra-wideband Tx architectures that successfully generated 16-QAM vector modulated signals at a data rate of 120 Gb/s and 100 Gb/s, respectively. Nevertheless, the former showed a quite low output power of -1.6 dBm across a 70-105 GHz frequency range while the latter suffered from a high error vector magnitude (EVM) of 17% at an operating frequency of 230 GHz. More interestingly, the work in [12] was able to generate a 64-QAM signal with a reasonable output power level at the D-band frequency range (i.e., 110-170 GHz). However, they relied on an expensive III-V technology (i.e., indium phosphide (InP)). Therefore, the PA stage in the front-end architecture shown in Figure 2.1a represents a bottleneck as the maximum operating frequency of the underlying transistor should be significantly lower than f_{max} of the technology to ensure acceptable performance. This limitation motivated the research to investigate other front-end solutions that can achieve a high frequency of operation without resorting to more expensive technologies.

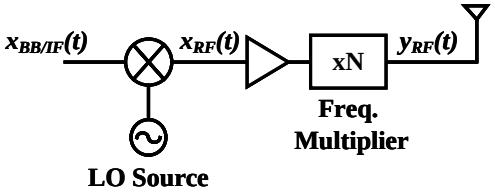
An alternate front-end architecture is shown in Figure 2.1b. This architecture starts with an intermediate-frequency (IF) modulated signal that feeds an up-conversion mixer. The mixer output is further up-converted using a nonlinear harmonic mixer to generate a high-frequency modulated signal. Hence, this architecture allows the frequency upper-bound to approach f_{max} of the transistor. It has been adopted by [4, 13] to generate



(a)



(b)



(c)

Figure 2.1: Front-end architectures used for high-frequency signal generation: (a) with last stage power amplifier, (b) with last stage nonlinear harmonic mixer, and (c) with last stage frequency multiplier.

high-order modulated signals. The authors in [4] demonstrated a 300 GHz Tx capable of generating a 32-QAM signal. They utilized a cubic mixer which is essentially a tripler but receives a two-tone-like signal. However, the reported Tx output power was limited to -14.5 dBm. Similarly, the authors in [13] used a doubler-based mixer, called a square mixer, to generate high-order modulation signals (32-QAM and 128-QAM) centered at an operating frequency of 300 GHz. Since the metal oxide semiconductor field effect transistor (MOSFET) quadratic nonlinearity is stronger than its cubic counterpart, they were able to achieve higher peak output power (i.e., -5.5 dBm) compared to the work in [4]. Nevertheless, the process of nonlinear mixing results in non-negligible images and spurious signals close to the targeted frequency band. Hence, the harmonic mixer-based front-end architecture, shown in Figure 2.1b, requires lossy high-order filters after the up-conversion or/and additional signal processing.

The challenges of the previous two front-end architectures triggered the research to devise the frequency multiplier-based front-end architecture depicted in Figure 2.1c. In such architecture, the frequency multiplier is used as the last stage for frequency up-conversion. Hence, all stages preceding the frequency multiplier operate at an IF lower than the targeted operating frequency. This enables the design of low-loss passives and high-gain actives, ultimately improving the RF performance. Nevertheless, due to the frequency multipliers' nonlinearity, they are typically used to generate constant envelope or phase modulated signals [5, 14, 15]. For example, the authors in [14] and [15] developed linear frequency-modulated continuous-wave (FMCW) transmitters at a center frequency of 77 GHz for automotive radar applications. While the authors in [5] demonstrated a QPSK Tx centered at an operating frequency of 240 GHz for future wireless chip-to-chip communication. Thus, the inherent nonlinearity of frequency multipliers limited their application to generating amplitude and phase modulated signals.

To address this issue, the architecture in Figure 2.1c is augmented with an outphasing technique that utilizes nonlinear frequency multipliers for signal generation [16–18]. In the outphasing technique, the amplitude-varying input signal is decomposed into two phase modulated signals which are passed through two parallel chains of frequency multipliers. Since these two signals have a constant envelope, the nonlinearity of the frequency multiplier won't cause any distortion at the output of the chain. The signals from the two parallel chains are then combined to generate a high-frequency vector modulated signal. Using this technique, the authors in [17] and [18] presented Tx architectures centered at frequencies of 216 GHz and 390 GHz, respectively. They were able to generate 16-QAM modulated signals. However, limited data rates of 20 Mb/s and 6 Gb/s were reported. Hence, the outphasing technique failed to generate ultra-wideband signals with acceptable data rates that meet the strict requirements of future wireless communication. Moreover,

another limitation of the outphasing technique is that it is very sensitive to the phase and amplitude imbalance between the two paths which would require additional calibration steps to correct this imbalance. Thus, while solving the issue of frequency multipliers' nonlinearity, the outphasing technique suffered from its own design limitations. This motivated the authors in [19–22] to propose the use of a DPD linearization technique to mitigate the strong nonlinearity exhibited by frequency multipliers in Figure 2.1c when driven by spectrally-efficient signals having high PAPR. They were inspired by the DPD schemes that are commonly used to linearize PAs and investigated how to tailor these schemes to linearize frequency multipliers. Hence, by applying DPD, the authors in [21] and [22] were able to successfully generate up to 400 MHz OFDM signals with sub-carriers modulated using 256-QAM at a center frequency of 63 GHz.

Based on the discussion in this section, the frequency multiplier-based front-end architecture, shown in Figure 2.1c, represents a promising solution for high-frequency signal generation. Recent publications showed the potential of this architecture to generate vector modulated signals by applying DPD linearization technique to solve the issue of frequency multipliers' nonlinearity. However, the achieved output power was quite low. In the next section, we will investigate various solutions to enhance the front-end's output power.

2.3 Beamforming Front-End Architectures

Despite the large bandwidth offered by the transition to mm-wave and sub-THz frequency bands, generating a high-quality signal with sufficient output power faces significant challenges due to the increased FSPL and the degradation of RF performance in most semiconductor technologies. These challenges call for advancements at the device, circuit, and system design levels of RF technologies. Focusing on the system design levels, power-combining techniques are commonly employed to boost the front-end's output power. They are classified into fixed power combining and free-space (over-the-air) combining. Both techniques utilize multiple transmit elements to generate high-frequency signals; however, the key difference lies in the way of signal combining at the transmit elements' outputs. The fixed power combining technique utilizes an on-chip power combiner to generate a high-power output signal [23, 24]. For instance, the authors in [24] developed a four-way power-combining frequency multiplier where the outputs from four transmit elements are combined using a reactive power-combining network. They achieved an 8 dBm output power at 215 GHz and > 5 dBm over a 200-230 GHz frequency range. Although showing promising output power, by increasing the number of transmit elements, larger on-chip power combiners will be required which would result in high loss and large area. Conse-

quently, this limits its scalability to large-scale antenna array systems.

To overcome this limitation, most of the research adopted the free-space power combing technique [25, 26]. In this technique, multiple transmit elements are utilized to transmit signals which are combined over the air to achieve a certain effective isotropic radiated power (EIRP). For example, authors in [25] demonstrated a 260 GHz on-off-keying (OOK) transceiver for short-range chip-to-chip communication applications. They designed two Tx/Rx elements with on-chip antennas achieving an EIRP of 5 dBm. While authors in [26] developed an 8-way amplifier-quadrupler array centered at 420 GHz. The measurement results showed an EIRP of 3 dBm.

One common architecture of coherent over-the-air combining is the beamforming architecture. This architecture utilizes beamformers in the Tx paths to enable directed radiation in a desired direction and to steer the beam in different directions serving multiple users. The beamformer's key component is the phase shifter which is responsible for directing the beam and beam steering. Also, amplitude-varying stages (e.g., variable attenuators and/or variable gain amplifiers) are utilized in the beamformer for additional tapering. Generally, RF, digital, and hybrid beamforming architectures have been utilized to enable directed radiation as well as to mitigate the impact of the increased FSPL with the carrier frequency [27–29]. Digital and hybrid beamforming techniques are not practical at mm-wave and sub-THz frequency bands due to the high sampling rate requirements of analog-to-digital converters (ADCs) which consume a significant amount of DC power. Hence, the RF beamforming architecture is widely adopted at these frequency bands for its low DC power, complexity, and cost compared to its counterparts [30].

Figure 2.2a shows the typical PA-based RF beamforming front-end architecture which is inspired by the architecture previously shown in Figure 2.1a. In this architecture, the frequency multiplier serves as the key component of the local oscillator which is needed to up-convert the modulated signal around an IF frequency, $x(t)$, to a desired mm-wave/sub-THz carrier frequency, f_{RF}. The resulting high-frequency signal feeds a mm-wave/sub-THz front-end composed of multiple cascades of RF beamformers and PAs before being radiated using a large-scale antenna-array system. As f_{RF} increases, the design of the mm-wave/sub-THz front-end module and the signal distribution network encounters significant challenges due to the constraints and limitations imposed by the underpinning semiconductor technologies. For instance, the limited breakdown voltage and high level of parasitics of the active devices and high losses of the passive devices in nano-scale semiconductor technologies significantly compromise the achievable performance of the PA stage, especially as the carrier frequency approaches the f_{max} frequency. Accordingly, the PA-based RF beamforming architecture shown in Figure 2.1a is widely utilized for generating vector modulated signals up to 80 GHz [31–33]. Nevertheless, attempts in [34] and [35] to deploy

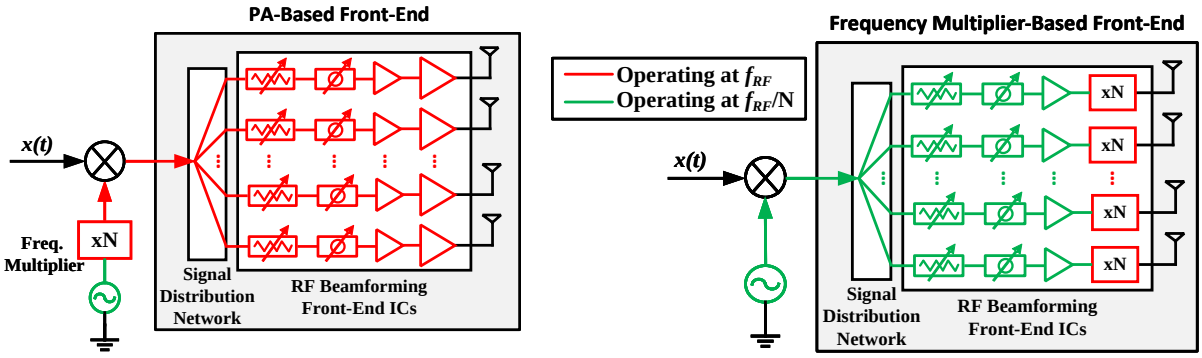


Figure 2.2: (a) Typical PA-based RF beamforming front-end. (b) Frequency multiplier-based RF beamforming front-end utilizing a frequency multiplier as a last stage for frequency up-conversion.

this architecture at 110 GHz and 150 GHz carrier frequencies, respectively, were limited to generating an amplitude-modulated (AM) signal [34] and a QPSK modulated signal [35].

To address the challenges of the PA-based RF beamforming architecture, alternative approaches were proposed in [36] and [37]. In these works, the authors developed front-end architectures where the RF beamformers are placed in the LO and IF paths, respectively, before the up-conversion mixer. Hence, the phase shifters and the signal distribution network operate at a lower frequency with high-gain actives and low-loss passives. The authors in [36] successfully generated a QPSK modulated signal with an output power limited to -6.8 dBm at an operating frequency of 258 GHz. While the authors in [37] demonstrated promising results, generating up to 64-QAM modulated signals with decent power levels centered at a carrier frequency of 140 GHz. However, challenges persisted, such as LO leakage and a low image rejection ratio, as the up-conversion mixer still had to operate at a high frequency. Moreover, the PA stage faced performance limitations due to the need to operate at such high frequency.

The limitations of the RF beamforming architectures discussed earlier have spurred research into alternate solutions. Building upon the architecture shown in Figure 2.1c, the integration of frequency multipliers into RF beamforming structures has been explored [38, 39]. Figure 2.2b depicts the frequency multiplier-based RF beamforming front-end architecture where the frequency up-conversion operation is deferred to the last stage and is carried out using frequency multipliers. This architecture allows the up-conversion mixer, the signal distribution network, and the preceding front-end components (i.e., RF

beamformers) to operate at a lower frequency (f_{RF}/N), resulting in improved RF performance. For example, authors in [38] deployed the frequency multiplier-based RF beamforming structure, incorporating a frequency quadrupler at the front-end's output. This work reported a proof-of-concept prototype that was used to transmit AM signals at 400 GHz carrier frequency. Moreover, authors in [39] developed a 320 GHz frequency multiplier-based Tx with an EIRP of 10.6 dBm, albeit limited to generating frequency-modulated signal. Hence, the generalization of the frequency multiplier-based RF beamforming front-end, depicted in Figure 2.2b, to the generation of vector modulated signals has been hindered by the nonlinearity exhibited by the frequency multipliers. Nevertheless, recent attempts to linearize frequency multiplier-based RF beamforming front-ends using the DPD linearization technique, mentioned in Section 2.2, have demonstrated promising results in generating OFDM vector modulated signals [40]. Furthermore, another interesting feature offered by the frequency multiplier-based RF beamforming architecture is its resiliency to active load modulation induced by antenna cross-coupling in the array [41]. The study in [41] revealed that the frequency multiplier-based RF beamforming arrays exhibit reduced sensitivity to load modulation when compared to last-stage PA arrays (i.e., PA-based front-end shown in 2.2a).

Given the insights from this section, the frequency multiplier-based RF beamforming front-end, illustrated in Figure 2.2b, will be adopted in this work. However, its viable deployment relies on the development of frequency multipliers capable of generating vector modulated signals with adequate output power levels and power efficiency. It also depends on the design of RF beamformer (i.e., phase shifters) that is tailored to meet the specifications of the frequency multiplier-based front-end. Consequently, the next section will delve into the investigation of various circuit-level techniques for designing frequency multipliers and phase shifters.

2.4 Frequency Multiplier-Based RF Beamforming Front-End

In this section, a detailed literature review on the circuit-level techniques to design frequency multipliers and phase shifters is investigated to understand the trade-off between the different configurations. This will help us design high-performance components that will contribute to enhancing the RF performance of our targeted frequency multiplier-based RF beamforming front-end.

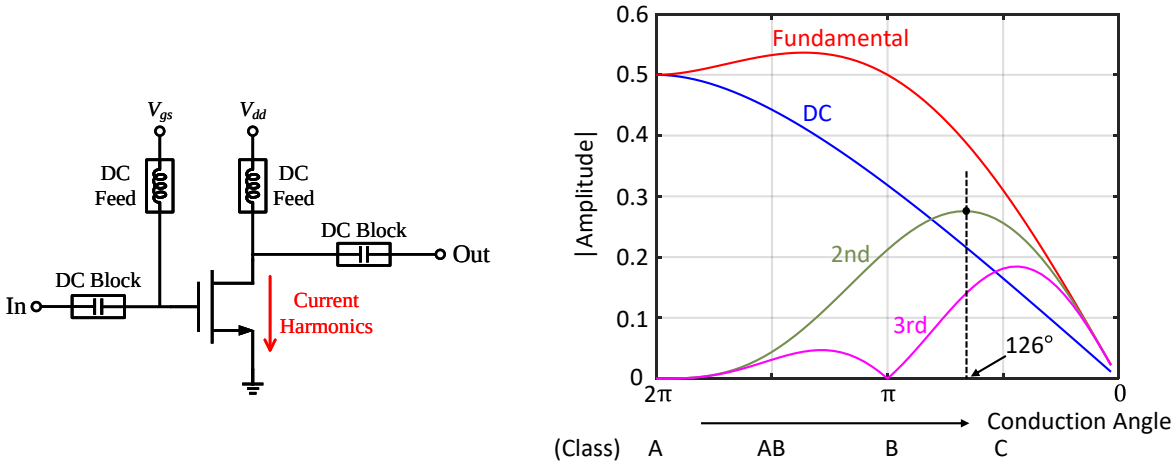
2.4.1 Frequency Multipliers

Frequency multipliers represent a promising solution for signal generation at mm-wave and sub-THz frequency bands. Their key performance metrics include output power, power efficiency, conversion gain (CG), bandwidth, area, and fundamental rejection. Frequency multipliers can be classified into two categories: passive and active. Passive frequency multipliers are typically implemented using diodes [42–44]. They can achieve good fundamental suppression and wide RF bandwidth but suffer from high conversion loss. In contrast, active frequency multipliers allow to have a conversion gain and higher output power that makes them an attractive candidate compared to their passive counterparts. Various circuit topologies have been proposed in the literature for the realization of active frequency multipliers (e.g., frequency doublers and triplers). In this thesis, we will focus on the design of active frequency doublers.

Frequency Doublers in Literature

Existing works on frequency doublers have explored various approaches. For instance, works such as [45–47] proposed Gilbert-cell mixer-based topologies. These schemes achieve frequency doubling by injecting the same input signal into the mixer's LO and RF paths. In [45] and [46], frequency doublers targeting a carrier frequency around 60 GHz are developed, demonstrating high CG and good fundamental rejection but at the expense of low power efficiency. In an effort to enhance the power efficiency of the mixer-based topology, the authors in [47] proposed replacing the transconductance stage of the conventional Gilbert-cell with a passive trifilar transformer. They were able to achieve a 14% efficiency at an operating frequency of 58 GHz. However, the reported output power was quite low. While mixer-based frequency doublers offer high CG and fundamental suppression, their elevated power consumption significantly limits their power efficiency, rendering them unsuitable for integration with RF beamforming front-end structures.

Recently, frequency doublers exploiting the nonlinearity of active device have gained significant attention in the literature for their enhanced power efficiency compared to mixer-based counterparts [48–60]. These schemes leverage the transistor transconductance nonlinearity to generate current components at different harmonics at the transistor's output. For instance, Figure 2.3 depicts the normalized amplitudes of the DC and the first three harmonics of the transistor's output current as a function of the conduction angle [61]. For optimum frequency doubling operation, a Class-C bias for the transistor must be selected with a conduction angle of 126°. This bias can be maintained by adjusting the transistor's gate-source voltage, V_{gs}, shown in Figure 2.3a. Building upon that approach, the



(a) (b)

Figure 2.3: (a) MOSFET transistor. (b) Normalized amplitudes of the transistor's output current harmonics versus the conduction angle.

authors in [48] and [49] developed frequency doublers using a single transistor at various frequencies, incorporating an additional filtering stage at the transistor's output to suppress undesired harmonics. Despite compact size and low power consumption, the use of filtering stages introduced losses, impacting the output power and CG.

Alternatively, the authors in [51–55] proposed frequency doubler topologies employing two transistors connected in a push-push configuration. In this configuration, the drains of the two differentially-fed transistors are connected together resulting in broadband cancellation of the fundamental and odd harmonics at the output and eliminating the need for lossy filtering stages. Some works [52–54] introduced an amplifier stage after the push-push-based frequency doubler to increase the output power. However, these prototypes exhibited either low CG [52] or narrow bandwidth [53, 54]. Alternatively, the authors in [55] incorporated a second harmonic feedback network into the push-push-based frequency doubler to enhance the CG. Although their demonstrated result showed a peak CG of 1.2 dB at an output frequency of 56 GHz, their design experienced low power efficiency. Moreover, the authors in [56] and [57] proposed using current-reuse and neutralization techniques, respectively, to improve the CG at low input power. However, these techniques were found to yield limited output power and peak CG. To enhance the power efficiency of the push-push-based frequency doubler, the authors in [60] utilized a transistor multi-port waveform shaping technique, where the gates and sources of the push-push configuration were driven

by 180° out-of-phase signals. This approach achieved a high efficiency of 25% and output power of 7.4 dBm at an output frequency of 60 GHz but at the expense of a low CG.

The success of the push-push configuration at lower frequencies prompted its adoption at frequencies above 100 GHz [62–72]. For example, the authors in [66] developed a push-push frequency doubler, achieving an output power of 4.1 dBm and an efficiency of 11.8% at 134 GHz output frequency. To maximize the second harmonic power generation, the authors in [68] proposed a Class-F frequency doubler where they optimized the fundamental and third harmonic load impedance. They created a square output voltage waveform inspired by the well-known Class-F PA. The demonstrated results in [68] showed an output power above 5 dBm from 112 GHz to 125 GHz. A critical issue in the push-push frequency doublers is that the output current flows back to the input due to the transistors' Miller capacitances, creating an in-phase second harmonic voltage swing at both gates of the push-push pair. This in-phase voltage swing causes distortion to the input voltage waveform which affects the output drain current and consequently alters the RF performance of the frequency doubler. A well-known solution to this issue is to short-circuit the second harmonic input impedance. However, creating a short-circuit impedance at high frequencies is challenging due to the inherent high losses at these frequencies; hence, most of the literature tends not to design for it when targeting high operation frequency. Nevertheless, to address this issue, [70], [71], and [72] successfully implemented this solution at frequencies 120 GHz, 204 GHz, and 130 GHz, respectively. The authors in [70] and [71] used a custom-designed capacitor with enhanced quality factor and an open stub input harmonic reflector at the second harmonic, respectively. Meanwhile, the authors in [72] developed a triaxial balun to create the second harmonic input short, achieving an improved output power of 9.4 dBm at 130 GHz output frequency.

It is important to highlight that while the works mentioned above have shown promising results, their performance under vector modulated signal stimuli and applicability for frequency multiplier-based front-end have yet to be validated.

Higher Multiplication Order

While the preceding discussion delved into frequency doubler designs, the generation of high frequencies from relatively low frequencies necessitates high-order multiplication. This can be achieved through either a single high-order frequency multiplier, such as a frequency quadrupler, or cascading multiple stages of low-order frequency multipliers, such as frequency doublers and triplers. However, the use of a single frequency quadrupler stage encounters challenges, including limited CG, since the transistor has to be biased in very

deep Class-C to extract the 4^{th} harmonic [73, 74]. Consequently, research efforts have predominantly embraced the concept of a frequency multiplier chain (FMC), realized through a cascade of frequency doublers and/or triplers [75–80]. For instance, the works in [78–80] employed a cascade of two push-push frequency doublers to design a frequency quadrupler. Specifically, the authors in [78] demonstrated a 140 GHz frequency quadrupler featuring good RF bandwidth but suffered from very low gain. In contrast, the authors in [79] introduced an interstage bandpass filter in the FMC to reject undesired harmonics, compensating for filter loss with an intermediate amplifier. Their demonstrated results showed excellent harmonic rejection across a bandwidth of 70-115 GHz but at the expense of limited output power and high power consumption. Additionally, the authors in [80] developed a 2-stage push-push frequency doubler with optimized second harmonic reflectors to improve the output power. They also used an intermediate driver amplifier to provide the last-stage doubler with sufficient power. The prototype in [80] achieved an output power of 5.5 dBm with a 3-dB bandwidth from 212 GHz to 260 GHz, albeit with limited efficiency.

In conclusion, an extensive literature review has explored diverse techniques for designing frequency doublers, a critical block in the envisioned RF beamforming front-end design. The subsequent section will delve into the circuit-level techniques proposed in the literature for designing phase shifters.

2.4.2 Phase Shifters

The phase shifter (PS) serves as a pivotal component in the realization of an RF beamforming structure capable of precisely directing and steering the beam in different directions. Hence, an effective PS design must exhibit low insertion loss (IL), high phase accuracy, and enhanced linearity while minimizing IL-variation over the phase shift settings. Existing PS designs are broadly categorized into two types: active and passive. Active PSs, namely vector-sum PSs, allow for simultaneous control of the gain and phase; however, they suffer from poor linearity and high power consumption [81–83]. Passive PSs are commonly preferred for large-scale RF beamforming realization due to their zero power consumption and improved linearity compared to their active counterparts. They can be classified into three main configurations: i) switched-type PS (STPS) [84–86], ii) loaded transmission line PS [87, 88], and iii) reflective-type PS (RTPS) [89–95].

The STPS is implemented by cascading phase-shifting stages, designed using low-pass/high-pass filters, to achieve discrete phase shift (e.g., 180°, 90°, and 45°). However, increasing the bit resolution leads to adding more stages with smaller phase shifts (e.g., 22.5° and 11.25°), which results in excessive chip area due to bulky passive components.

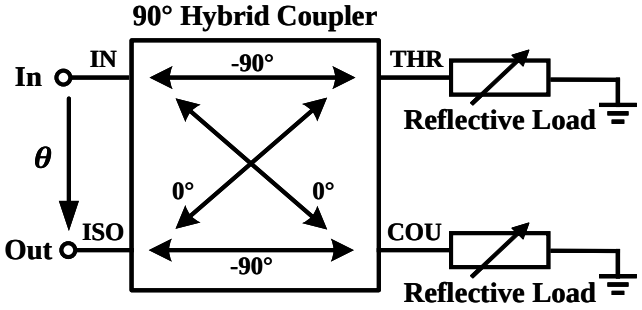


Figure 2.4: Reflective-type phase shifter design.

Also, the STPS configuration suffers from high IL and IL-variation [84–86]. Alternatively, the authors in [87] and [88] introduced the loaded transmission line PS. In this design, the phase tuning is done by manipulating the electromagnetic properties of an artificially constructed transmission line. Although the authors in [88] were able to achieve a sub-degree phase precision, their design suffered from high IL of 9.3 dB and limited phase shift range of 190° at an operating frequency of 28 GHz.

The limitations of the STPS and loaded transmission line PS configurations triggered most of the research to extensively investigate the RTPS solution. Figure 2.4 shows the block diagram of the RTPS which consists of a 90° hybrid coupler and two tunable reflective loads at the coupler's coupled and through ports. The phase shift is achieved through tuning the reflective load. Various circuit arrangements have been proposed to improve the phase shift range of the RTPS. For instance, the authors in [89] proposed a cascade of three RTPS stages that utilize simple varactor-based reflective loads to achieve a 180° phase shift range. However, their prototype suffered from a high IL-variation of ±1.6 dB versus the phase settings.

Alternatively, single-stage RTPS arrangements that incorporate more complicated tunable reflective loads, including LC- [90–92], CLC- [93], and transformer-based [94], allow for extended phase shift range and reduced size. For instance, the authors in [90] and [91] designed a single RTPS stage with reflective loads implemented by parallel-LC and series-LC networks, respectively. While achieving acceptable IL, these designs exhibited high IL-variation and limited phase shift range ($< 150°$). Additionally, the authors in [92] utilized series-LC reflective loads with improved inductor design to alleviate the issue of quality factor. They achieved a 190° phase range but at the expense of high IL of 9.3 dB. To maximize the phase shift range, the authors in [93] developed complex CLC-based reflective loads (having two resonance points) to design a single-stage 5-bit RTPS at a carrier frequency of 28 GHz. Although the CLC network couldn't achieve a full 360°, leveraging asymmetry

between the two reflective loads maintained a 360° phase range. However, this comes at the cost of increased IL. Alternatively, the authors in [94] proposed a transformer-based reflective load network that has a triple resonance point, demonstrating low IL-variation and a 367° phase range with $< 5°$ phase resolution. But, the IL was quite high. Moreover, the authors in [95] introduced triple-resonance reflective loads, implemented by a parallel combination of two series-LC networks. They developed a single-stage RTPS with a phase range of 379° and IL-variation of $\pm$ 0.2 dB operating at a frequency of 29 GHz. However, their fabricated prototype suffered from a limited phase resolution of 22.5°. Therefore, while single-stage RTPS arrangements offer increased phase shift range, the limited quality factor of on-silicon passive components used to implement the reflective loads engenders relatively high IL and often limits the achievable RF bandwidth.

2.5 Vision of The Proposed Front-End Architecture

Based on the literature discussed in this chapter, the frequency multiplier-based front-end will be adopted for high-frequency signal generation. Furthermore, to boost the front-end's output power, an RF beamforming structure will be employed. Using the frequency multiplier in the RF beamforming structure imposes additional design constraints. For example, the phase shifter must meet more strict requirements in terms of the gain accuracy and phase resolution. Hence, for the phase shifter design, the RTPS will be adopted due to its low insertion loss, minimal insertion loss variation, and high phase resolution compared to other phase shifter configurations.

In this work, the primary focus will be on frequency doublers with the flexibility to increase the multiplication factor, N, by cascading multiple frequency doubling stages. We are targeting an output frequency, f_{out}, at the D-band frequency range (i.e., around 120 GHz). The choice of the input frequency, f_{in}, is crucial and depends on the availability of signal sources, at such input frequency, capable of generating vector modulated signals with acceptable EVM and adjacent channel power ratio (ACPR) that meet the requirements of the future 6G wireless systems. Such signal sources can be obtained at a carrier frequency of 30 GHz. Thus, while aiming for an f_{out} of 120 GHz, we will select an f_{in} of 30 GHz and employ a cascade of two frequency doublers (i.e., N = 4) to realize the desired output frequency. Note, the use of a much lower input frequency (i.e., higher N) is avoided as the phase noise of the input signal source will be multiplied by N at the front-end output. Moreover, the ultimate goal of this research is to generate vector modulated signals at frequencies above 200 GHz by adding a frequency doubler/tripler at the output. This will allow us to generate signals close to f_{max} of the transistor which can not be achieved

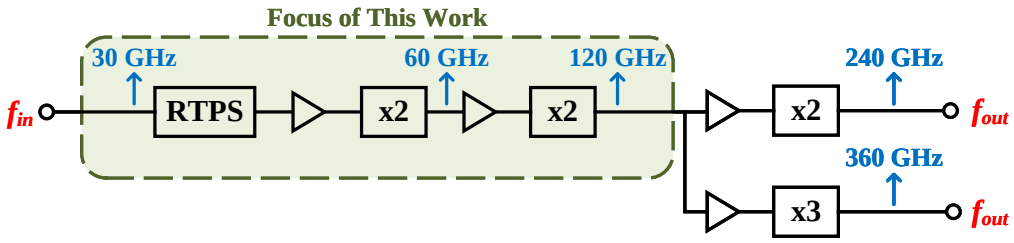


Figure 2.5: Proposed frequency multiplier-based RF beamforming front-end architecture.

using the PA-based RF beamforming front-end. Figure 2.5 depicts the block diagram of the proposed frequency multiplier-based RF beamforming front-end architecture.

2.6 Conclusion

In this chapter, the different front-end architectures used to generate high-frequency signals have been presented. While PA-based and mixer-based architectures have been employed, the frequency multiplier-based front-end has emerged as a promising alternative for high-frequency signal generation. However, the main challenges of this architecture lie in the frequency multiplier's nonlinearity and limited output power. Recent research efforts have shown advancements in linearizing frequency multipliers through DPD linearization technique, enabling the generation of vector modulated signals. To address the issue of limited output power, the RF beamforming front-end architecture will be adopted which depends on coherent over-the-air combining and utilizes phase shifters to enable directed radiation.

The efficient design of frequency multiplier-based RF beamforming front-end architecture hinges on the performance of its constituent building blocks. This thesis will primarily focus on the design of frequency multipliers and phase shifters. To provide a comprehensive foundation for these designs, an extensive literature review on the various circuit-level implementations has been presented. Notably, RTPS represents a promising candidate for PS design as it exhibits improved IL and IL-variation compared to other PS configurations. For the frequency multiplier, cascading frequency doubler stages will be considered in this work to avoid the issues associated with implementing a high-order multiplication stage. Among the diverse frequency doubler designs, the push-push configuration has demonstrated superior performance, forming the basis for further exploration in this thesis. The next chapter will delve into a detailed analysis of the push-push frequency doubler to provide insights that will guide the design of frequency doublers capable of generating vector modulated signals with optimal output power and power efficiency.

Chapter 3

V-Band Frequency Doubler With Enhanced Efficiency and AM-PM Characteristic

3.1 Introduction

As discussed previously, the employment of frequency multiplier-based front-ends holds considerable promise for high-frequency signal generation. Nonetheless, the inherent strong nonlinearity of frequency multipliers restricts its application to signals with a constant envelope. Remarkably, recent research has demonstrated the potential of frequency multipliers to generate vector modulated signals through the application of DPD linearization techniques [96]. However, the successful deployment of frequency multiplier-based front-ends hinges on the development of frequency multipliers capable of generating vector modulated signals with adequate output power levels, power efficiency, and linearity. Various circuit topologies have been proposed in the literature to realize frequency doublers and triplers, with higher frequency multiplication factors achieved through cascading. This chapter addresses the design of a 60-GHz frequency doubler which is the first frequency doubler in the proposed frequency multiplier-based RF beamforming front-end module as highlighted in Figure 3.1. It presents a novel methodology for designing push-push-based frequency doublers, offering high output power and power efficiency over a designated bandwidth. Furthermore, to support the generation of vector modulated signals, this methodology proposes a new design strategy aimed at enhancing the phase distortion characteristics (AM-PM) of the push-push configuration.

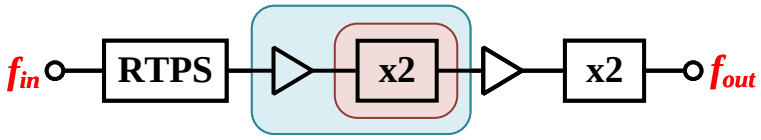


Figure 3.1: Proposed frequency multiplier-based RF beamforming front-end module, highlighting the focus of this chapter.

In this chapter, Section 3.2 begins by discussing the utilization of waveform engineering techniques to identify the optimal harmonic load impedance terminations that maintain consistent output power and power efficiency over a designated bandwidth. It then proceeds to formulate the AM-PM characteristics of the frequency doubler while considering the impact of transistor parasitic input capacitance. This finding plays a crucial role in determining the most suitable second harmonic source impedance. In Section 3.3, the proposed methodology is applied to design a V-band (50-75 GHz) frequency doubler within a 45-nm silicon-on-insulator (SOI)-CMOS process. Moving forward, Section 3.4 presents the measurement results obtained under continuous-wave (CW) and modulated signal stimuli. Finally, in Section 3.5, a summary of the work undertaken in this chapter is provided.

3.2 On the Selection of Harmonic Load and Source Terminations for Maximizing Frequency Doubler Performance

In this section, we propose the use of waveform engineering techniques to determine the harmonic load impedances that optimize the output power and power efficiency of frequency doublers over a designated bandwidth. Additionally, we formulate the phase of the frequency doubler's CG, taking into account the transistor parasitic input capacitance, to investigate how we can minimize the AM-PM nonlinearity.

3.2.1 Continuous Harmonic Load Termination Design Space

Figure 3.2 shows the schematic of the push-push core of the frequency doubler. In this configuration, the drains of the differential transistors, M_1 and M_2, are directly connected, resulting in the constructive addition of the even harmonics and the broadband cancellation

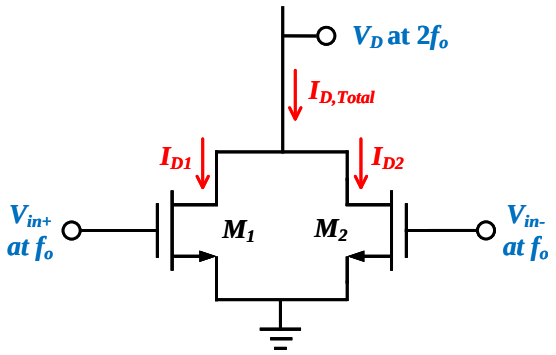


Figure 3.2: Schematic of the frequency doubler push-push core.

of the fundamental and odd harmonics. Hence, the total output current and voltage, $I_{D,Total}$ and V_D, contain only even harmonics. The transistors, M_1 and M_2, are biased in deep Class-C mode with a conduction angle of 126° [97] to maximize the magnitude of the output current at the 2^{nd} harmonic. In the following analysis, the transistors are modeled as ideal voltage-controlled current sources with a knee voltage of zero.

The drain currents, $I_{D1}(\theta)$ and $I_{D2}(\theta)$, of transistors, M_1 and M_2, can be represented as a function of the angular phase θ by:

$$\begin{aligned} I_{D1}(\theta) &= I_{dc} + I_1 cos(\theta) + I_2 cos(2\theta) + I_3 cos(3\theta) + ... \\ &= I_{dc}\big[1 + 1.78 cos(\theta) + 1.23 cos(2\theta) + 0.57 cos(3\theta) + ...\big], \end{aligned} \tag{3.1}$$

$$\begin{aligned} I_{D2}(\theta) &= I_{dc} - I_1 cos(\theta) + I_2 cos(2\theta) - I_3 cos(3\theta) + ... \\ &= I_{dc}\big[1 - 1.78 cos(\theta) + 1.23 cos(2\theta) - 0.57 cos(3\theta) + ...\big], \end{aligned} \tag{3.2}$$

where I_{dc} denotes the DC current and I_n represent the Fourier coefficients at the n^{th} harmonic of the current. They are calculated based on the following equation [97],

$$\begin{aligned} I_{dc} &= I_{max} \frac{2t_o}{\pi T} \\ I_n &= I_{max} \frac{4to}{\pi T} \left| \frac{cos(n\pi t_o/T)}{1 - (2nt_o/T)^2} \right| \text{ for } n \geq 1, \end{aligned} \tag{3.3}$$

given that I_{max} is the maximum drain current of the transistor and t_o/T is the duty cycle of the push-push frequency doubler and is equal to 0.35 (i.e., equivalent to a conduction angle of 126°).

Based on (3.1) and (3.2), the total output current of the push-push core can be found by:

$$I_{D,Total}(\theta) = I_{D1}(\theta) + I_{D2}(\theta) = 2I_{dc}\big[1 + 1.23cos(2\theta) + 0.09cos(4\theta) + ...\big]. \tag{3.4}$$

Assuming that the push-push core is terminated with non-zero harmonic load terminations at the even harmonics, the output drain voltage waveform can be expressed as:

$$V_D(\theta) = V_{dc} - V_{2r}cos(2\theta) + V_{2q}sin(2\theta) + \sum_{\substack{\text{n even} \\ n>2}} V_{nq}sin(n\theta), \tag{3.5}$$

where V_{dc} represents the DC supply voltage, V_{2r} and V_{2q} are the in-phase and quadrature voltage coefficients at the 2^{nd} harmonic, and V_{nq} are the quadrature voltage coefficients at the n^{th} harmonic.

To avoid voltage clipping, the output voltage waveform $V_D(\theta)$ must satisfy the condition $V_D(\theta) \geq 0$. Assuming control over the harmonic terminations up to the 4^{th} harmonic, (3.5) can be re-written as:

$$\begin{aligned} V_D(\theta) &= V_{dc}\big(1 - \beta cos(2\theta)\big)\big(1 - \alpha sin(2\theta)\big) \\ &= V_{dc}\big(1 - \beta cos(2\theta) - \alpha sin(2\theta) + 0.5\alpha\beta sin(4\theta)\big) \end{aligned} \tag{3.6}$$

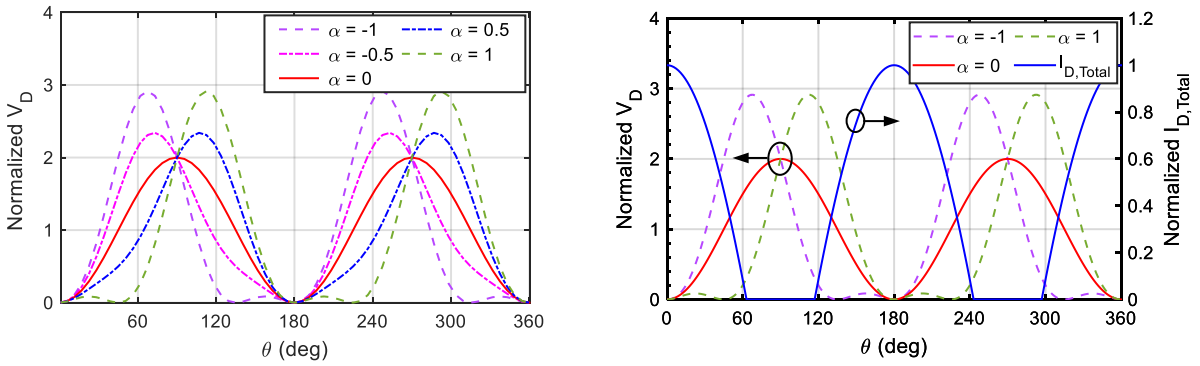
where $\alpha \in [-1, 1]$ and $\beta \in [0, 1]$ are two design parameters introduced to engineer the waveform of $V_D(\theta)$ such that the condition $V_D(\theta) \geq 0$ is satisfied. Figure 3.3a shows the output voltage waveforms corresponding to different values of α with $\beta = 1$. These plots represent a subset of a continuous design space for a push-push frequency doubler that satisfies the condition $V_D(\theta) \geq 0$. It should be noted that $\beta = 1$ (i.e., $V_{2r} = V_{dc}$) and $\alpha = 0$ define the output power and power efficiency of the frequency doubler. By varying the value of α within the range $[-1, 1]$ while maintaining constant output power and power efficiency, one can explore the design space.

The current and voltage expressions in (3.4) and (3.6) can be used to derive the 2^{nd} harmonic load impedance, $Z_{L,2}$, and 4^{th} harmonic load impedance, $Z_{L,4}$, for each value of α as follows:

$$Z_{L,2} = \frac{V_{dc}(-1 - j\alpha)}{-2I_2} = R_{opt}(1 + j\alpha) \tag{3.7}$$

$$Z_{L,4} = \frac{j0.5\alpha V_{dc}}{-2I_4} = -j\frac{13\pi}{6}\alpha R_{opt}, \tag{3.8}$$

where $-1 < \alpha < 1$ and R_{opt} $(= V_{dc}/2I_2)$ represents the optimum 2^{nd} harmonic load impedance. Given that the push-push core cancels the odd harmonics at the common drain



(a) (b)

Figure 3.3: The output voltage and current waveforms of the push-push core corresponding to a subset of continuous design space: (a) the normalized output voltage waveform for different values of α with $\beta = 1$, and (b) the normalized output voltage and current waveforms for $\alpha = \{-1, 0, 1\}$ and $\beta = 1$.

node, the fundamental and odd harmonic load impedance terminations are assumed to be short circuits. Figure 3.3b shows the normalized output voltage and current waveforms for the cases of $\alpha = [-1, 0, 1]$. It should be noted that for $\alpha = 0$, $Z_{L,2} = R_{opt}$ and $Z_{L,4} = 0$.

Equations (3.7) and (3.8) define a continuous design space for $Z_{L,2}$ and $Z_{L,4}$ that allows for the same output power and power efficiency as a conventional push-push frequency doubler terminated with $Z_{L,2} = R_{opt}$ and $Z_{L,4} = 0$. Figure 3.4 graphically depicts the design space defined by (3.7) and (3.8). The proposed continuous design space offers a relaxation of the harmonic termination design, accommodating the constraints and limitations imposed by implementation technologies. It eliminates the need for pure real load termination at the 2^{nd} harmonic and short circuit termination at the 4^{th} harmonic, which are difficult to achieve in practice, especially at higher output frequencies. Furthermore, the design space provides valuable degrees of freedom for designing frequency doublers with constant output power and power efficiency over a designated bandwidth. This can be achieved through a careful selection of $Z_{L,2}$ and $Z_{L,4}$ values at each frequency on the design space specified in Figure 3.4.

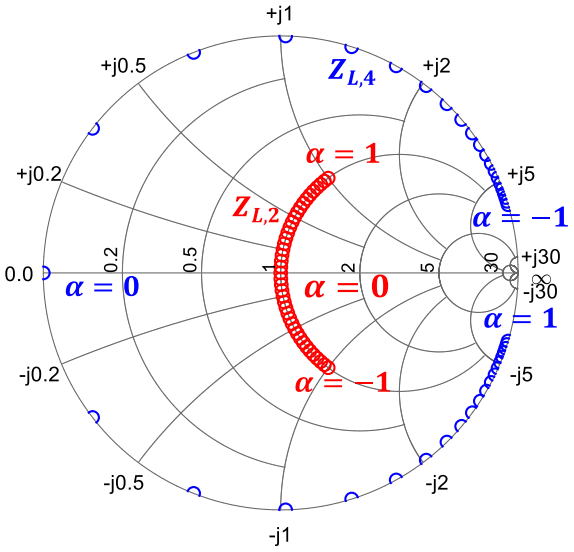


Figure 3.4: 2^{nd} and 4^{th} harmonic load impedances (normalized to R_{opt}) corresponding to the proposed continuous design space for different values of α with $\beta = 1$.

3.2.2 Harmonic Source Termination Design Choice For Linearity Enhancement

This section exploits the potential solutions for selecting the 2^{nd} harmonic source impedance, $Z_s(2\omega_o)$, to enhance the phase distortion characteristics (AM-PM) of the frequency doubler. Hence, the subsequent analysis formulates the frequency doubler's AM-PM (i.e., $\angle$CG) in an attempt to define these potential solutions. It also takes into consideration the impact of the transistor parasitic input capacitance. Figure 3.5 depicts a simplified half-circuit model of the push-push core, which serves as the basis for determining the strategy to identify the desired source termination. It is important to note that the drain-source parasitic capacitance, C_{ds}, is absorbed in the load impedance.

The drain current, $i_{ds}(t)$, in the half-circuit model shown in Figure 3.5, can be expressed in terms of the gate voltage, $v_{gs}(t)$, as:

$$i_{ds}(t) = g_{m,1}v_{gs}(t) + g_{m,2}v_{gs}^2(t) + g_{m,3}v_{gs}^3(t) + ..., \tag{3.9}$$

where $g_{m,n}$ represent the transistor transconductance at the n^{th} harmonic. It is assumed that $g_{m,2}$ is significantly higher than $g_{m,n}$ with $n > 2$, as the push-push core is biased in a deep Class-C conduction angle that maximizes the CG at the 2^{nd} harmonic. Also, $g_{m,1}$ is

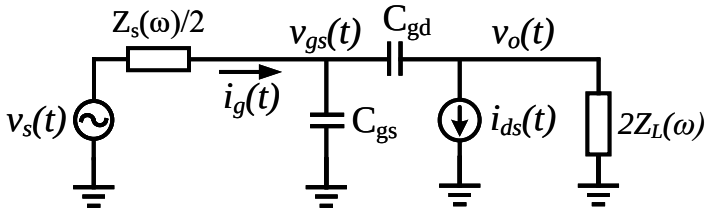


Figure 3.5: Simplified half-circuit small-signal model of the push-push core where C_{gs}, C_{gd}, and C_{ds} designate the transistor parasitic capacitances with C_{ds} absorbed in the load impedance.

neglected since the push-push configuration cancels the fundamental current component at the output. Based on (3.9), the fundamental and the 2^{nd} harmonic drain current, $I_{ds}(\omega_o)$ and $I_{ds}(2\omega_o)$, can be written in the phasor form as:

$$I_{ds}(\omega_o) = g_{m,2} V_{gs}(2\omega_o) V_{gs}^*(\omega_o) \tag{3.10}$$

$$I_{ds}(2\omega_o) = g_{m,2} V_{gs}^2(\omega_o) \tag{3.11}$$

where $V_{gs}(\omega_o)$ and $V_{gs}(2\omega_o)$ designate the fundamental and the 2^{nd} harmonic phasors of the gate voltage. Accordingly, the frequency doubler's output voltage can be defined in the phasor form as:

$$V_o(\omega_o) = -2Z_L(\omega_o) I_{ds}(\omega_o) = -2Z_L(\omega_o) g_{m,2} V_{gs}(2\omega_o) V_{gs}^*(\omega_o) \tag{3.12}$$

$$V_o(2\omega_o) = -2Z_L(2\omega_o) I_{ds}(2\omega_o) = -2Z_L(2\omega_o) g_{m,2} V_{gs}^2(\omega_o) \tag{3.13}$$

where $Z_L(\omega_o)$ and $Z_L(2\omega_o)$ denote the load impedance of the push-push core at the fundamental and 2^{nd} harmonic, respectively.

Assuming $V_{gs}(\omega_o) = V_{gs1} e^{j\phi_{gs1}}$ and $V_{gs}(2\omega_o) = V_{gs2} e^{j\phi_{gs2}}$, the CG of the push-push core can be expressed as:

$$\text{CG} = \frac{V_o(2\omega_o)}{V_s(\omega_o)} = -2Z_L(2\omega_o) g_{m,2} \frac{V_{gs1}^2}{V_s} e^{j2\phi_{gs1}}, \tag{3.14}$$

where $V_s(\omega_o)$ is the source voltage phasor at the fundamental frequency and given by V_s. Thus, the AM-PM of the frequency doubler can be determined as:

$$\angle\text{CG} = 180 + \angle Z_L(2\omega_o) + \angle g_{m,2} + 2\phi_{gs1}. \tag{3.15}$$

Next, the phase of the fundamental gate voltage phasor, ϕ_{gs1}, should be formulated to fully characterize the $\angle$CG given in (3.15). Based on Figure 3.5, the gate current, $i_g(t)$, can be expressed as a function of the transistor parasitic capacitances, C_{gs} and C_{gd}, as follows:

$$i_g(t) = C_{gd}\frac{d\big(v_{gs}(t) - v_o(t)\big)}{dt} + C_{gs}\frac{d\big(v_{gs}(t)\big)}{dt}. \tag{3.16}$$

Hence, (3.16) can be re-written in the phasor form at the fundamental and the 2^{nd} harmonic as follows:

$$\begin{aligned} I_g(\omega_o) &= j\omega_o C_{gd}\big[V_{gs}(\omega_o) - V_o(\omega_o)\big] + j\omega_o C_{gs}V_{gs}(\omega_o) \\ &= j\omega_o C_g V_{gs}(\omega_o) + j\omega_o C_{gd}2Z_L(\omega_o)g_{m,2}V_{gs}(2\omega_o)V_{gs}^*(\omega_o) \end{aligned} \tag{3.17}$$

$$\begin{aligned} I_g(2\omega_o) &= j2\omega_o C_{gd}\big[V_{gs}(2\omega_o) - V_o(2\omega_o)\big] + j2\omega_o C_{gs}V_{gs}(2\omega_o) \\ &= j2\omega_o C_g V_{gs}(2\omega_o) + j2\omega_o C_{gd}2Z_L(2\omega_o)g_{m,2}V_{gs}^2(\omega_o) \end{aligned} \tag{3.18}$$

where $C_g = C_{gs} + C_{gd}$. Moreover, the fundamental and the 2^{nd} harmonic gate voltage phasors, $V_{gs}(\omega_o)$ and $V_{gs}(2\omega_o)$, can be expressed in terms of the source voltage phasor as follows:

$$V_{gs}(\omega_o) = V_s(\omega_o) - \frac{Z_s(\omega_o)}{2}I_g(\omega_o) \tag{3.19}$$

$$V_{gs}(2\omega_o) = 0 - \frac{Z_s(2\omega_o)}{2}I_g(2\omega_o) \tag{3.20}$$

where $Z_s(\omega_o)$ and $Z_s(2\omega_o)$ represent the fundamental and the 2^{nd} harmonic source impedance, respectively. Note, the source voltage phasor has only one component at the input frequency (i.e., the fundamental frequency).

By substituting (3.17) into (3.19), $V_{gs}(\omega_o)$ can be expressed as:

$$V_{gs1}e^{j\phi_{gs1}} = \frac{2V_sY_s(\omega_o)}{2Y_s(\omega_o) + j\omega_o C_g + j\omega_o C_{gd}2Z_L(\omega_o)g_{m,2}V_{gs2}e^{j(\phi_{gs2}-2\phi_{gs1})}} \tag{3.21}$$

where $Y_s(\omega_o) = G_s(\omega_o) + jB_s(\omega_o)$ is the fundamental source admittance. To maximize the input power transfer, $B_s(\omega_o)$ is chosen to resonate with the total input capacitance such that:

$$2B_s(\omega_o) = -\omega_o C_g = -\omega_o(C_{gd} + C_{gs}). \tag{3.22}$$

Accordingly, (3.21) can be re-written as:

$$V_{gs1}e^{j\phi_{gs1}} = \frac{2V_sY_s(\omega_o)}{2G_s(\omega_o) + j\omega_o C_{gd}2Z_L(\omega_o)g_{m,2}V_{gs2}e^{j(\phi_{gs2}-2\phi_{gs1})}}. \tag{3.23}$$

It is worth noting that (3.23) is a function of the gate voltage phasor at the 2^{nd} harmonic which needs to be defined.

Using (3.18), $V_{gs}(2\omega_o)$ in (3.20) can be simplified to:

$$V_{gs2}e^{j\phi_{gs2}} = \frac{-j2\omega_o C_{gd}2Z_L(2\omega_o)g_{m,2}V_{gs1}^2 e^{j2\phi_{gs1}}}{2Y_s(2\omega_o)+j2\omega_o C_o} = \frac{-j2\omega_o C_{gd}2Z_L(2\omega_o)g_{m,2}V_{gs1}^2 e^{j2\phi_{gs1}}}{2Y_s(2\omega_o)-j4B_s(\omega_o)}. \tag{3.24}$$

Note, $Y_s(2\omega_o) = G_s(2\omega_o) + jB_s(2\omega_o)$ is the source admittance at the 2^{nd} harmonic. By substituting (3.24) back into (3.23), (3.23) can be re-written as:

$$V_{gs1}e^{j\phi_{gs1}} = \frac{2V_s Y_s(\omega_o)}{2G_s(\omega_o) + \frac{\left(\omega_o C_{gd}2Z_L(\omega_o)g_{m,2}\right)\left(2\omega_o C_{gd}2Z_L(2\omega_o)g_{m,2}\right)}{2Y_s(2\omega_o)-j4B_s(\omega_o)}V_{gs1}^2}. \tag{3.25}$$

Re-arranging the terms in (3.25), the gate voltage phasor at the fundamental frequency can be defined by:

$$V_{gs1}e^{j\phi_{gs1}} = \frac{2V_s\big(G_s(\omega_o)+jB_s(\omega_o)\big)}{2G_s(\omega_o)+A(\omega_o,2\omega_o)V_s^2+jB(\omega_o,2\omega_o)V_{gs1}^2}, \tag{3.26}$$

where

$$A(\omega_o,2\omega_o) = \frac{\left(\omega_o C_{gd}2Z_L(\omega_o)g_{m,2}\right)\left(2\omega_o C_{gd}2Z_L(2\omega_o)g_{m,2}\right)(2G_s(\omega_o))}{4G_s^2(2\omega_o)+\left[2B_s(2\omega_o)-4B_s(\omega_o)\right]^2} \tag{3.27}$$

$$B(\omega_o,2\omega_o) = \frac{\left(\omega_o C_{gd}2Z_L(\omega_o)g_{m,2}\right)\left(2\omega_o C_{gd}2Z_L(2\omega_o)g_{m,2}\right)\left(-2B_s(2\omega_o)+4B_s(\omega_o)\right)}{4G_s^2(2\omega_o)+\left[2B_s(2\omega_o)-4B_s(\omega_o)\right]^2}. \tag{3.28}$$

Thus, a closed-form for the phase of the fundamental gate voltage phasor, ϕ_{gs1}, can be extracted by:

$$\phi_{gs1} = tan^{-1}\left(\frac{B_s(\omega_o)}{G_s(\omega_o)}\right) - tan^{-1}\left(\frac{B(\omega_o,2\omega_o)V_{gs1}^2}{2G_s(\omega_o)+A(\omega_o,2\omega_o)V_{gs1}^2}\right). \tag{3.29}$$

Using (3.29), the AM-PM in (3.15) can be fully defined by:

$$\begin{aligned}\angle\text{CG} = 180 + \angle Z_L(2\omega_o) + \angle g_{m,2} + 2tan^{-1}\left(\frac{B_s(\omega_o)}{G_s(\omega_o)}\right) \\ - 2tan^{-1}\left(\frac{B(\omega_o,2\omega_o)V_{gs1}^2}{2G_s(\omega_o)+A(\omega_o,2\omega_o)V_{gs1}^2}\right).\end{aligned} \tag{3.30}$$

Equation (3.30) shows that the first four terms of the AM-PM are independent of V_{gs1} and add a constant phase, which does not affect the AM-PM characteristics. However, the last term in (3.30) is a nonlinear function of the input gate voltage, V_{gs1}. Consequently, it introduces a power-dependent phase shift that engenders AM-PM distortions. To cancel the last term in (3.30), $B(\omega_o, 2\omega_o)$ should be equal to zero. Hence, using (3.28), the following condition needs to be satisfied:

$$\frac{\big(-2B_s(2\omega_o)+4B_s(\omega_o)\big)}{4G_s^2(2\omega_o)+\big[2B_s(2\omega_o)-4B_s(\omega_o)\big]^2}=0. \tag{3.31}$$

It is important to note that the condition in (3.31) is a function of the 2^{nd} harmonic source impedance, $Z_s(2\omega_o)$. This adds a degree of freedom to control the AM-PM characteristics. Accordingly, based on (3.31), there are two potential solutions for the choice of $Z_s(2\omega_o)$ that eliminates the AM-PM distortions. The first solution is to short circuit $Z_s(2\omega_o)$; hence, $G_s(2\omega_o)$ satisfies

$$G_s(2\omega_o)=\infty. \tag{3.32}$$

The second solution is to choose $Z_s(2\omega_o)$ such that

$$B_s(2\omega_o)=2B_s(\omega_o), \tag{3.33}$$

which makes the numerator of (3.31) equal to zero. Simulation results showing the impact of these two solutions on the AM-PM characteristics will be further discussed in Section 3.3.2.

3.3 Implementation of V-Band Stacked Push-Push Frequency Doubler

The previous section presented a novel methodology that defines the design space for selecting the optimum load and source harmonic impedance terminations, which maintain consistent output power and power efficiency over the designated bandwidth while improving the AM-PM characteristics. In this section, we will implement the discussed methodology for the design of the frequency doubler. As a proof-of-concept demonstration, a cascade of a buffer stage followed by a frequency doubler is implemented using the GlobalFoundries' 45-nm SOI-CMOS process, operating at an output frequency of 60 GHz. The complete schematic of the proposed design is shown in Figure 3.6.

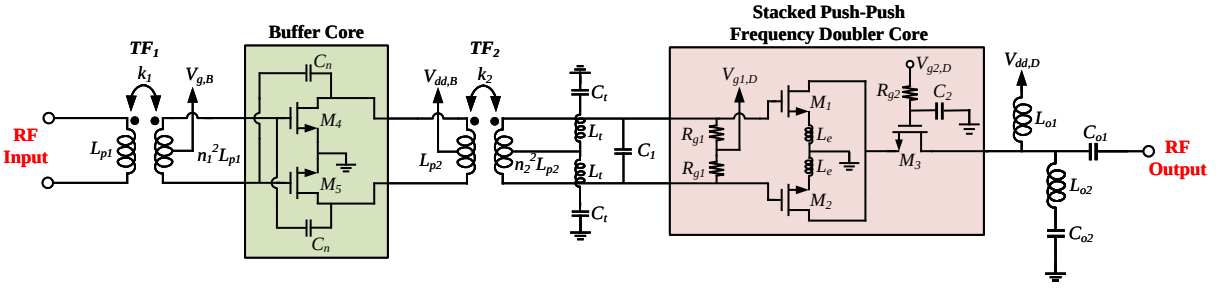


Figure 3.6: Complete schematic of the cascade of a buffer stage and the proposed frequency doubler.

3.3.1 Frequency Doubler Core

Figure 3.6 depicts the schematic of the frequency doubler core, which utilizes the push-push topology. An input differential signal is applied to the transistors, M_1 and M_2, which have a common drain node to extract the 2^{nd} harmonic current component. This push-push configuration of the frequency doubler core enables broadband cancellation of the fundamental and odd harmonics. To boost the output power of the frequency doubler, a simple common-gate amplifier, M_3, is added on top of M_1 and M_2 since it has lower input parasitic capacitances compared to using a common-source amplifier at the frequency doubler output. The sizes of the transistors are chosen to optimize the trade-off between output power and CG, as larger transistors yield higher output power at the expense of lower CG. Hence, the size of M_1 and M_2 are equal to 60 μm each, and the size of M_3 is set to 120 μm. Additionally, M_1 and M_2 are biased in deep Class-C mode with a gate bias, $V_{g1,D}$, set to -0.2 V. The gate bias, $V_{g2,D}$, and gate capacitor, C_2, of the stacked transistor, M_3, are carefully determined to ensure equal voltage swing among the push-push core and the stacked transistor. Given that the same current is passing through the push-push core and the stacked transistor and both of them have the same voltage swing, the 2^{nd} harmonic load impedance seen across the stacked transistor is assumed to be equal to that of the push-push core and is found by $Z_{L,2}$. Hence, the 2^{nd} harmonic load impedance seen at the output of the designed stacked push-push core, $Z_{o,2}$, can be seen as two impedances in series given by,

$$Z_{o,2} = 2Z_{L,2}. \tag{3.34}$$

Furthermore, a small degeneration source inductor, L_e, (equals to 12 pH) is employed to increase the real part of the fundamental source impedance, reducing the loss and complexity of the inter-stage matching network. It is important to note that the use of a stacked transistor introduces additional parasitic capacitances, which affect the bandwidth

of the frequency doubler.

3.3.2 Choice of Harmonic Load and Source Terminations

Harmonic Load Termination

As discussed in Section 3.2.1, the selection of $Z_{L,2}$ and $Z_{L,4}$ at each frequency within the designated bandwidth is crucial to maintain constant output power and power efficiency. Nevertheless, designing a high-order matching network practically poses significant challenges. Therefore, it is essential to study the sensitivity of the push-push core to the mismatch of 2^{nd} and 4^{th} harmonic terminations. This will help us to define an acceptable range for $Z_{L,2}$ and $Z_{L,4}$ that yields very low variation of the RF performance in terms of output power and power efficiency while relaxing the requirements on the matching network design.

To begin, we define the output power, $P_{L,2}$, and power efficiency, η_D, of the push-push core using the expressions of the current, $I_{D,Total}$, and voltage, V_D, in Section 3.2.1 as:

$$P_{L,2} = \frac{1}{2}(2I_{dc} * 1.23)V_{dc}, \tag{3.35}$$

$$\eta_D = \frac{P_{L,2}}{P_{dc}}, \tag{3.36}$$

where $P_{dc} = 2I_{dc}V_{dc}$. Note, from (3.36), an ideal push-push frequency doubler can achieve a maximum η_D of 61.5%. Figure 3.7 illustrates $P_{L,2}$ and η_D of the push-push core as functions of the normalized reactive part of $Z_{L,2}$ and $Z_{L,4}$ (i.e., $X_{L,2}$ and $X_{L,4}$), with α in (3.7) and (3.8) varied independently and V_k assumed to be zero. It can be observed that the design can tolerate some impedance mismatch without significantly degrading the RF performance. This defines a design space (the yellow region in Figure 3.7) for the choice of $X_{L,2}$ and $X_{L,4}$ on the reactance plane. Additionally, Figure 3.7 shows that, at a fixed $X_{L,4}$, $X_{L,2}$ can be varied within the yellow region while maintaining the same output power and power efficiency. This flexibility allows for careful variation of $Z_{L,2}$ across frequency, ensuring that the output power and power efficiency are consistent over the designated bandwidth. Consequently, it enables a more relaxed design of the output matching network over frequency.

For example, assuming $Z_{L,4}$ is short-circuited, $X_{L,2}/R_{opt}$ (i.e., α) can be chosen to vary linearly from -0.4 to 0.4 (as shown in Figure 3.7) across the frequency range of 54-66 GHz.

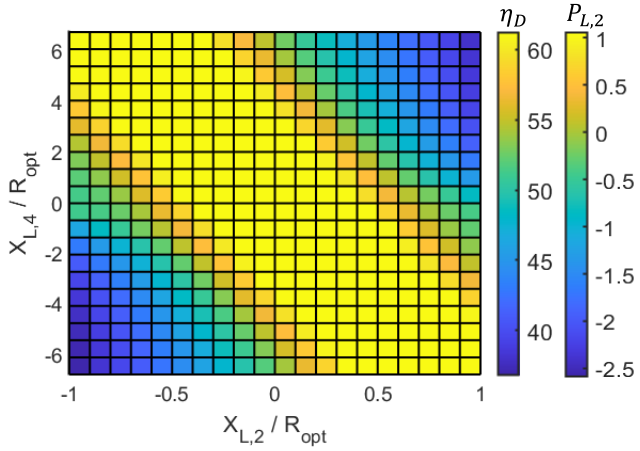


Figure 3.7: Sensitivity analysis of the push-push frequency doublers' output power and power efficiency to the harmonic impedance mismatch when $X_{L,2}$ and $X_{L,4}$ are varied independently and are normalized to R_{opt}.

Accordingly, the value of $Z_{L,2}$ at each frequency can be obtained using (3.7) and the value of $Z_{o,2}$ can be calculated using (3.34).

Figure 3.8 depicts the selected $Z_{o,2}$ (in circle) for design and the theoretical $Z_{o,2}$ (in triangle) based on (3.34) and (3.7) when α varies linearly from -0.4 to 0.4 over the frequency range of 54-66 GHz. The selected $Z_{o,2}$ for design slightly deviate from the theoretical values and were obtained by performing a load-pull simulation around the theoretical values so as to maximize the power efficiency. Note that the fundamental source impedance, $Z_{s,1}$, is maintained as a conjugate match at each frequency, while the other higher-order source harmonics are assumed to be short.

Next, we investigate the choice of the 4^{th} harmonic load impedance, $Z_{L,4}$. Ideally, the value of $Z_{L,4}$ is calculated using (3.8) based on the selected choice of α at each frequency. Similar to (3.34), the 4^{th} harmonic load impedance seen at the output of the designed stacked push-push core, $Z_{o,4}$, is defined by $Z_{o,4} = 2Z_{L,4}$. However, designing a 4^{th} harmonic matching network is challenging due to significant loss and low passive efficiency, which would impact the overall RF performance of the frequency doubler. Therefore, sensitivity analysis on the stacked push-push frequency doubler core is performed to determine the values of $Z_{o,4}$ that achieve acceptable power efficiency. Figure 3.9 illustrates the drain efficiency of the frequency doubler core when the real and imaginary parts of $Z_{o,4}$ (i.e., $R_{o,4}$ and $X_{o,4}$) are independently varied across the entire Smith Chart for different frequencies: (a) at 54 GHz, (b) at 60 GHz, and (c) at 66 GHz. It can be observed that the drain efficiency

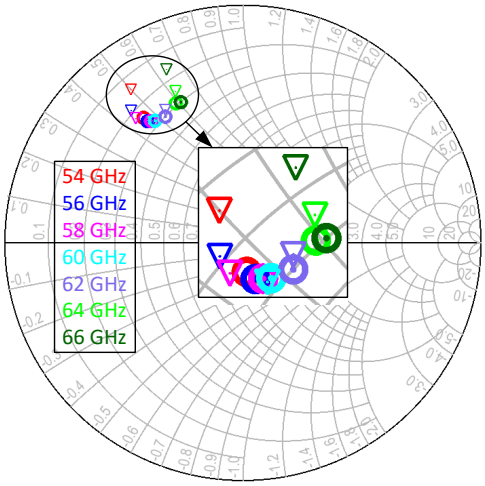
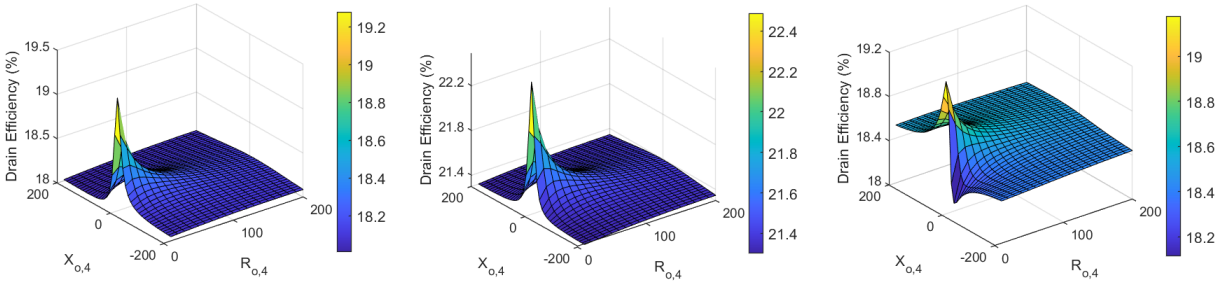


Figure 3.8: 2^{nd} harmonic load impedance of the designed frequency doubler core showing the selected one for design (in circle) and the theoretical one based on the proposed formulation (in triangle).



(a) At 54 GHz. (b) At 60 GHz. (c) At 66 GHz.

Figure 3.9: Drain efficiency of the frequency doubler core when the real and imaginary parts of $Z_{o,4}$ are varied independently across the entire Smith Chart at different frequencies.

experiences low sensitivity (around 1%) to the variation of $Z_{o,4}$ across frequencies. Note, this resiliency in the efficiency to the variation to the 4^{th} harmonic impedance can be explained by the fact that the 4^{th} harmonic current component at a conduction angle of 126° is significantly lower than the 2^{nd} harmonic current component. Therefore, we choose to design an output matching network that precisely achieves the selected $Z_{o,2}$ for design at each frequency, while monitoring $Z_{o,4}$ to ensure it resides in a relatively high-efficiency region. This relaxed the design of the output matching network, allowing for improved passive efficiency.

Harmonic Source Termination

Moving on to the selection of the 2^{nd} harmonic source impedance, $Z_{s,2}$, in light of the formulations discussed in Section 3.2.2, the AM-PM nonlinearity can be mitigated by satisfying the condition outlined in (3.31). This consideration leads to two potential approaches for addressing the AM-PM nonlinearity. The first approach involves directly short-circuiting $Z_{s,2}$. While the second approach entails designing $Z_{s,2}$ to fulfill the condition detailed in (3.33). Figure 3.10 shows the AM-PM of the designed frequency doubler where the 2^{nd} harmonic source impedance is either: i) not designed for, ii) short-circuited, or iii) terminated with the impedance that satisfies (3.33). Figure 3.10 shows the effectiveness of these two solutions in reducing the AM-PM nonlinearity where the phase distortion was reduced by around 9° compared to leaving $Z_{s,2}$ not designed for. These results are in line with the theory presented in Section 3.2.2. In this work, we opt for the first solution by short-circuiting $Z_{s,2}$ as this solution achieves a higher output power compared to the solution in (3.33). Also, it offers wideband elimination of the AM-PM nonlinearity compared to the other solution.

Furthermore, recognizing that achieving a perfect short circuit might be challenging in certain scenarios, we address the potential impact of a non-ideal $Z_{s,2}$ short on AM-PM nonlinearity. To simulate such conditions, we introduce variations in the real component of $Z_{s,2}$, denoted as $R_{s,2}$, (shown in Figure 3.11a) to represent different levels of short-circuit imperfection and their impact on the AM-PM behavior (shown in Figure 3.11b). The results in Figure 3.11b confirm that the AM-PM nonlinearity is more pronounced with weaker short-circuiting of $Z_{s,2}$. Hence, in scenarios where achieving a reasonable short circuit for $Z_{s,2}$ is not feasible (e.g., at frequencies higher than 100 GHz), one can choose $Z_{s,2}$ to satisfy the solution in (3.33) instead of short-circuiting $Z_{s,2}$ as to improve the AM-PM. An example of such impedance for this design is shown in Figure 3.11a.

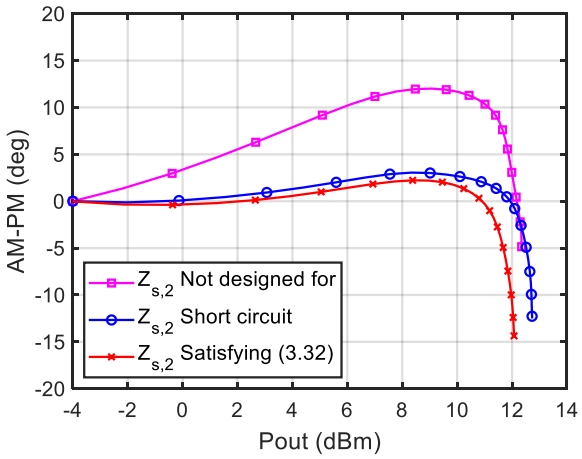
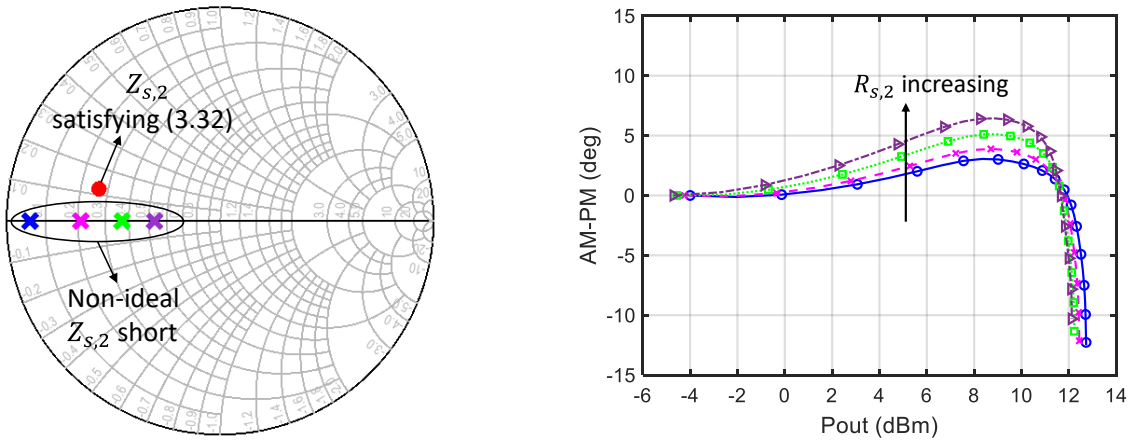


Figure 3.10: Simulated AM-PM of the designed frequency doubler for different termination conditions of $Z_{s,2}$.



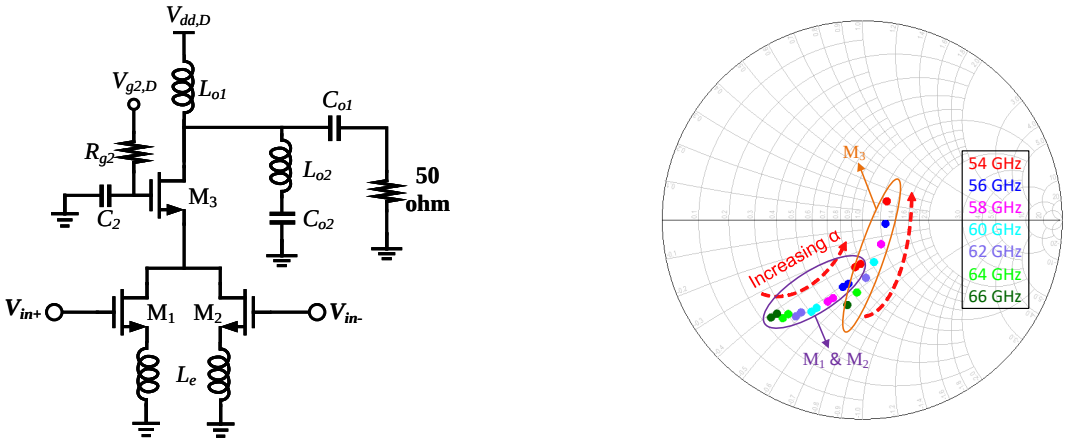
(a) (b)

Figure 3.11: (a) 2^{nd} harmonic input impedance of the frequency doubler corresponding to different termination conditions. (b) Sensitivity of the frequency doubler's AM-PM to a non-ideal $Z_{s,2}$ short.

3.3.3 Matching Networks Design

Output Matching Network

Various configurations can be employed to implement the output matching network in a frequency doubler. Examples of such configurations are transformers, transmission lines, and simple LC networks. Given the limited passive efficiency of transformers and the single-ended nature of the frequency doubler's output, a transformer-based matching network is avoided. Moreover, at the targeted frequency of operation, a transmission line-based matching network is avoided due to the large area occupied by the transmission line. Consequently, in this work, a simple LC matching network is chosen.



(a) (b)

Figure 3.12: Proposed frequency doubler core with the designed output matching network: (a) schematic and (b) the 2^{nd} harmonic load impedance seen by the common-source and common-gate transistors (normalized to 50 ohm).

Figure 3.12a illustrates the schematic of the proposed frequency doubler core, including the designed output matching network. The matching network is comprised of inductors (L_{o1} and L_{o2}) and capacitors (C_{o1} and C_{o2}), which achieve impedance transformation from the selected $Z_{o,2}$ defined in Section 3.3.2 to a 50-ohm output termination. To enhance the fundamental rejection, a fundamental short is implemented by resonating L_{o2} and C_{o2} at the fundamental frequency, f_o. Moreover, the supply voltage, $V_{dd,D}$, is biased through inductor L_{o1}, while capacitor C_{o1} provides DC decoupling.

Figure 3.12b illustrates the 2^{nd} harmonic load impedance seen by each transistor across different frequencies. It shows that the 2^{nd} harmonic load impedances encompass both re-

sistive and reactive components, effectively utilizing the continuous design space proposed in Section 3.2.1. Furthermore, their values vary across the frequency range ensuring consistent output power and power efficiency over the designated bandwidth, as discussed in Section 3.3.2. Note, the value of $Z_{o,4}$ is found by $50 + j70$. The designed output matching network achieves a passive efficiency of 89.5%.

Multi-Harmonic Inter-stage Matching Network

To address the issue of low CG in frequency doublers, a buffer stage is incorporated before the proposed frequency doubler to enhance the overall CG. While ensuring a conjugate match at the fundamental input impedance of the frequency doubler, an inter-stage load-pull simulation is performed to determine the optimal load impedance of the buffer that maximizes the overall efficiency across frequencies. Consequently, a transformer-based multi-harmonic inter-stage matching network is designed.

Figure 3.13a presents the circuit model of the designed inter-stage matching network, which comprises transformer TF_2, capacitor C_1, and a pair of L_t and C_t at the center-tap of the secondary coil. Figure 3.13b depicts the differential-mode half-circuit model of the inter-stage matching network. Since the drain of the input differential transistors of the push-push topology is assumed to be a virtual ground at f_o, the total input capacitance seen by the designed frequency doubler can be expressed as:

$$C_{in} = C_{gd} + \frac{C_{gs}}{1 - \omega_o^2 C_{gs} L_e} \tag{3.37}$$

The value of $\left(1 - \omega_o^2 C_{gs} L_e\right)$ is calculated to be close to 1. Hence, at the fundamental frequency, the transformer, TF_2, is designed such that its differential half-circuit inductance, $L_{dm,2}$, together with $2C_1$ provides the required matching to the inductively degenerated push-push transistor pair $\big($i.e., $L_{dm,2}$ resonates with $(2C_1 + C_{in})\big)$. This configuration ensures a robust match between the buffer stage and the frequency doubler at f_o.

As discussed in Section 3.3.2, $Z_{s,2}$ is selected to be short-circuited to minimize the AM-PM nonlinearity. Accordingly, the 2^{nd} harmonic short at the frequency doubler input is implemented using two pairs of L_t and C_t $\big($as shown in Figure 3.13a$\big)$. The common-mode half-circuit model of the inter-stage matching network is depicted in Figure 3.13c, where the common-mode inductance of TF_2, $L_{cm,2}$, resonates with L_t and C_t at $2f_o$ to create a 2^{nd} harmonic short. The symmetric structure of L_t and C_t is employed to improve the balance of the 2^{nd} harmonic input impedances seen by the frequency doubler's input differential transistors, $Z_{s,2}^{+}$ and $Z_{s,2}^{-}$. This allows for enhanced output power and CG. Figure 3.13d

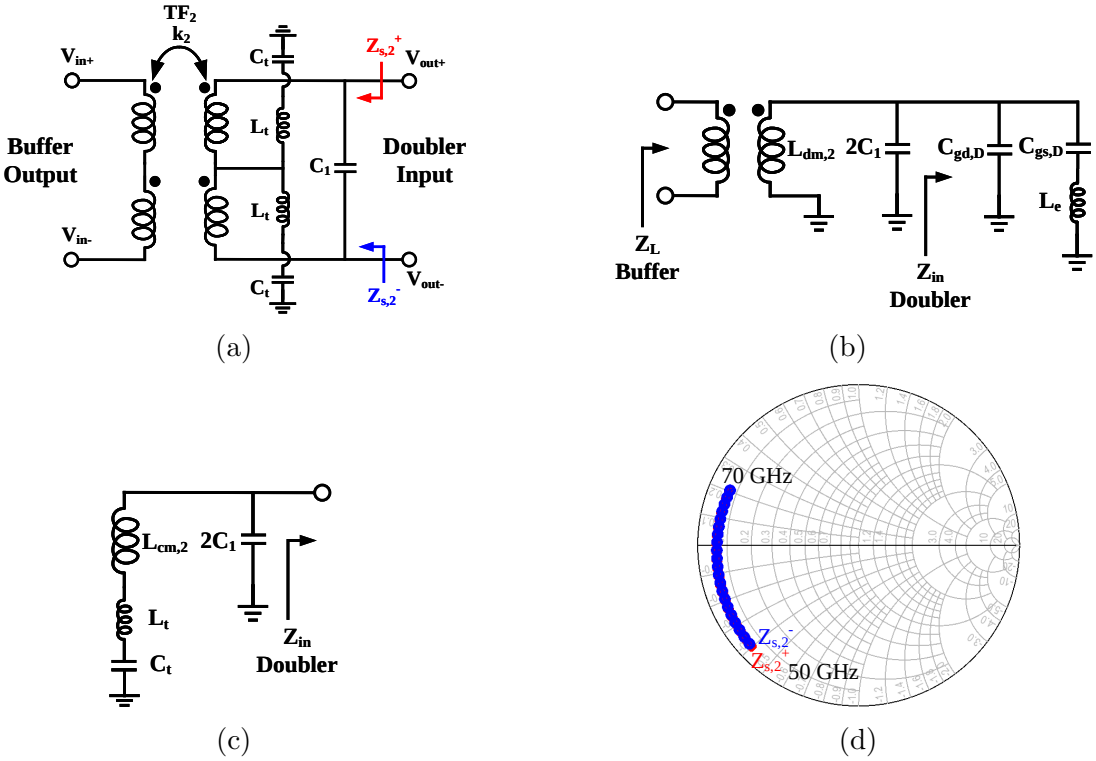


Figure 3.13: The designed inter-stage matching network: (a) complete circuit model and (b) differential-mode and (c) common-mode half-circuit models. (d) The 2^{nd} harmonic impedance seen by the input of the frequency doubler.

shows graphically $Z_{s,2}^{+}$ and $Z_{s,2}^{-}$ versus frequency, highlighting their good balance. Also, Figure 3.13d confirms the ability to achieve a 2^{nd} harmonic input impedance close to a short circuit which minimizes the AM-PM nonlinearity of the frequency doubler.

Figure 3.14 illustrates the synthesized multi-harmonic inter-stage matching network. The transformer is designed using a stacked topology where a primary coil is overlaid on a secondary coil. Two copper layers, OA and OB, are used to realize the coils where each of the layers has a metal thickness of 4 μm. The choice of metal thickness helps to reduce the Ohmic losses in the transformer windings while achieving the required mutual inductance. To realize the targeted impedance transformation, the value of the parallel capacitor, C_1, was chosen equal to 39.5 fF, while the primary inductance (L_{P2}), coupling coefficient (k_{m2}), and turn ratio (n_2) of the inter-stage transformer were deduced equal to 336 pH, 0.38, and 1.55, respectively. The designed transformer achieves a quality factor of 17.6. Additionally, L_t and C_t are determined to be 33 pH and 39.5 fF, respectively.

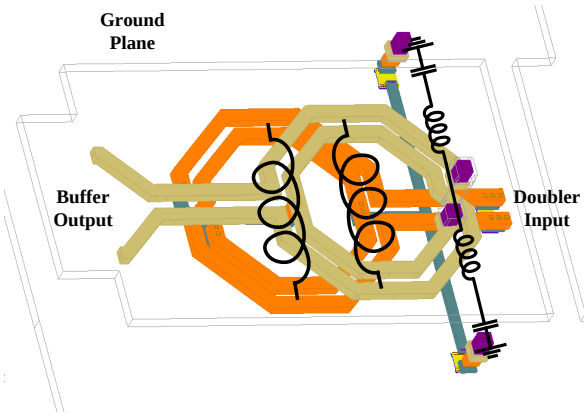


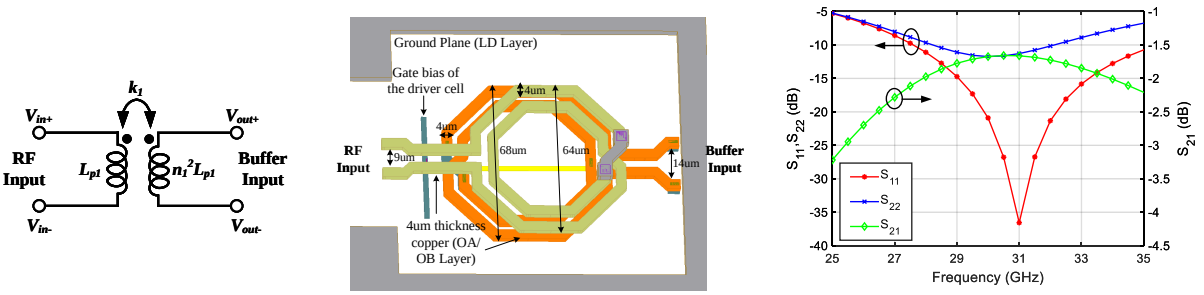
Figure 3.14: Layout structure of the multi-harmonic inter-stage matching network incorporating balanced 2^{nd} harmonic trap.

3.3.4 Buffer Design

The buffer stage is implemented using neutralized differential common-source transistors, as illustrated in Figure 3.6. The transistors' width is chosen as 120 μm, which has been determined to generate the desired input power for the frequency doubler. To mitigate the effect of transistor Miller capacitance $C_{gd,B}$, the neutralization capacitor is set to 31 fF. The supply voltage, $V_{dd,B}$, is selected as 1 V and biased through the center-tap of the primary

coil of the inter-stage matching network. Through simulation, the input impedance of the buffer, $Z_{in,B}$, that achieves conjugate match was determined to be $8.1 - j63$.

Figures 3.15a and 3.15b depict the circuit model and layout structure of the designed input matching network. A single transformer, TF_1, is utilized to transform $Z_{in,B}$ to a 100-ohm termination. The parameters of TF_1 are determined as follows: $L_{P1} = 317$ pH, $k_{m1} = 0.63$, and $n_1 = 1.07$. Figure 3.15c presents the S-parameters of the EM-simulated input matching network, demonstrating an insertion loss of approximately 1.67 dB with good input and output matching at the targeted 30 GHz input frequency.

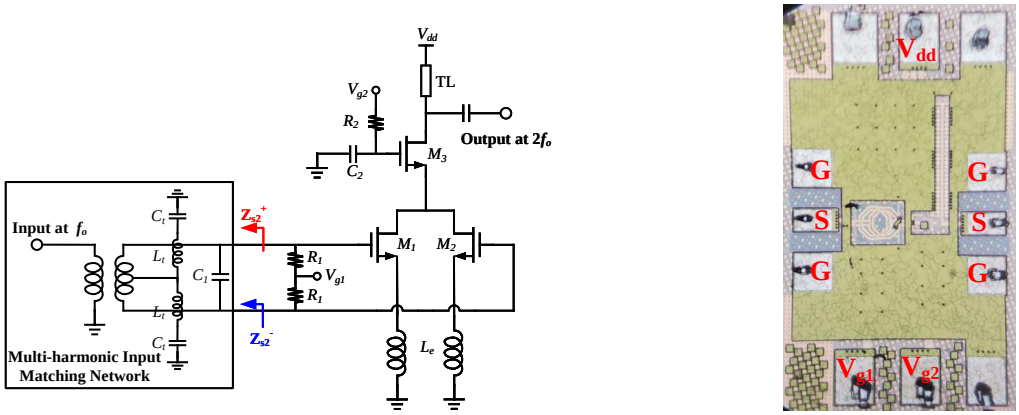


(a) Circuit model. (b) Layout structure. (c) Simulated S-parameters.

Figure 3.15: The designed input matching network.

3.4 Measurement Results

Before going to the design and fabrication of the cascade of buffer stage and frequency doubler discussed earlier, an initial prototype of a stand-alone frequency doubler is fabricated and validated experimentally. This initial prototype aims to evaluate the RF performance of the frequency doubler core, ensuring its intended functionality. Subsequently, building upon the success of the initial prototype, the second prototype is developed. This advanced iteration features the cascaded configuration of the buffer stage followed by the frequency doubler. It also aligns with the analysis and design framework detailed in Sections 3.2 and 3.3, contributing to the refinement of the overall design. The two frequency doublers' prototypes are fabricated using GlobalFoundries' 45-nm SOI-CMOS process. Their measurement results will be discussed in this section.



(a) Schematic. (b) Chip micrograph.

Figure 3.16: The fabricated stand-alone frequency doubler.

3.4.1 Stand-alone Frequency Doubler

Figures 3.16a and 3.16b depict the schematic model and chip micrograph of the fabricated stand-alone frequency doubler design. It occupies an area of 0.4×0.73 mm^2 (including pads). The design employs the same core architecture outlined in Section 3.3.1. Extensive load-pull simulation is conducted to deduce the optimal load impedance for maximum efficiency. Subsequently, a simple co-planar waveguide (CPW) transmission line (TL) is used to implement the output matching network. Furthermore, a multi-harmonic input matching network is utilized to match the frequency doubler's input impedance to a 50-Ω termination. It is implemented using a similar topology to the inter-stage matching network discussed in Section 3.3.3. The frequency doubler is biased in a Class-C mode, with a gate voltage, V_{g1}, of -0.2 V and a supply voltage of 2 V. Figure 3.17 shows the measured and simulated input reflection coefficients, highlighting achieved matching of better than -10 dB from 29.7 GHz to 33.7 GHz.

For the large-signal measurements, a signal generator (Keysight MXG-N5183B) was used to feed the input of the doubler, and a power meter augmented with a WR-15 filter was connected to the output. Figure 3.18a displays the measured CG, drain efficiency (η_D), and DC-to-RF efficiency (η_{out}) versus the output power at an output frequency of 60 GHz. η_D is determined by P_{out}/P_{dc} and η_{out} is defined as $P_{out}/(P_{in}+P_{dc})$. It reveals a peak CG, η_D, and η_{out} of 2.1 dB, 23.2%, and 20.3%, respectively. Furthermore, the η_D of about 15.5% measured at 6-dB output power back-off is very advantageous, particularly in the context of generating vector modulated signals.

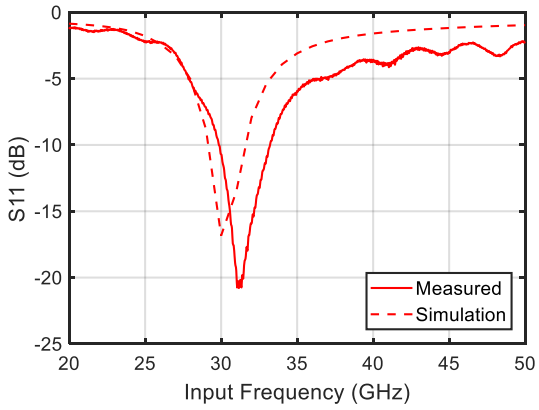
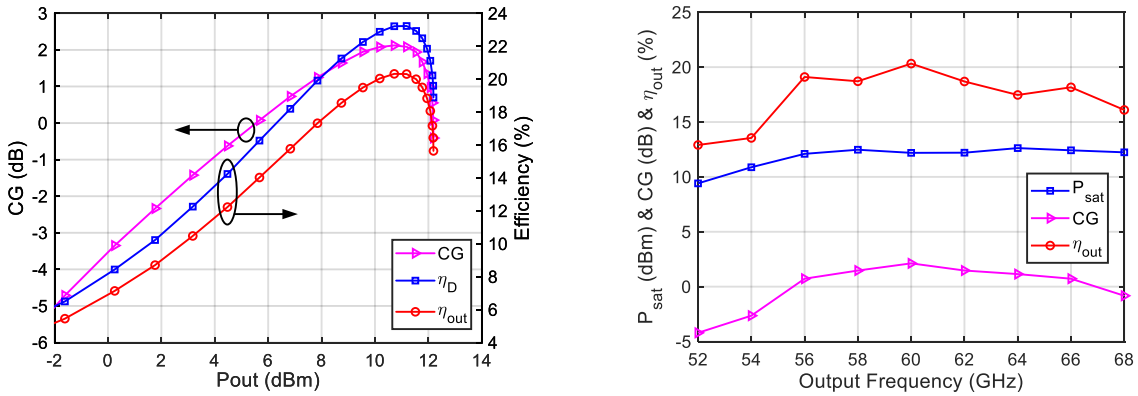


Figure 3.17: Measured and simulated input reflection coefficient of the stand-alone frequency doubler.



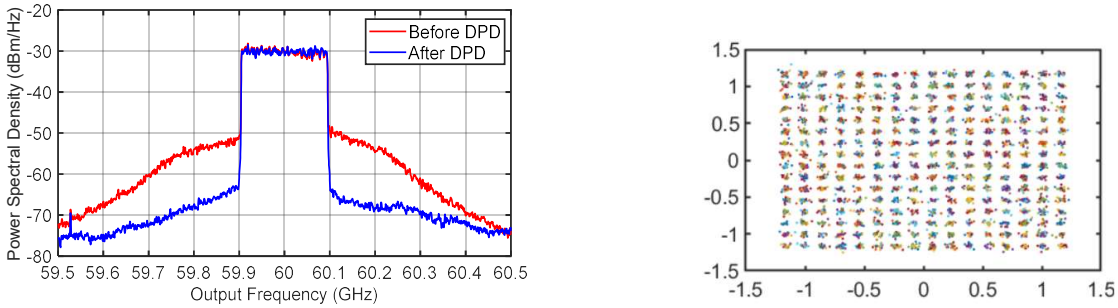
(a) (b)

Figure 3.18: (a) Measured CG and efficiency of proposed doubler versus output power at 60 GHz. (b) Measured P_{sat}, CG, and efficiency across frequency.

Figure 3.18b shows the measured saturated output power, P_{sat}, of the frequency doubler versus frequency. It reveals a high peak output power of 12.5 dBm and a 1-dB P_{sat} fractional bandwidth of 21.6% (55 to 68 GHz) without needing to resort to power-hungry output buffers as traditionally used in frequency doubler designs. Figure 3.18b also depicts the measured peak CG and η_{out} versus frequency. It highlights the measured peak CG, η_D, and η_{out} of $>$ 0dB, $>$ 20%, and $>$ 16% respectively, from 55 GHz to 68 GHz.

The designed frequency doubler was evaluated under modulated signal excitation using a 200-MHz OFDM test signal modulated using 256-QAM. The test signal was generated using an arbitrary waveform generator (Keysight M8190A), before being up-converted to 30 GHz and fed to the input of the frequency doubler. The output signal of the frequency doubler was then down-converted from 60 GHz to an IF of 2 GHz. Finally, the IF signal was digitized using a high-speed scope (Keysight MSOS804A). The experimental setup used for the modulated signal measurements will be further discussed in details in Section 3.4.2.

The linearization of the frequency doubler was performed using the low-complexity DPD function reported in [40] with a total of 94 coefficients. Figure 3.19 depicts the measured spectrum and 256-QAM constellation at the output of the frequency doubler before DPD and after DPD. Based on Figure 3.19, the ACPR and EVM were improved from 24 dBc and 11.9% before DPD, to 37.5 dBc and 2.9% after DPD. These results were reported at an average η_D of 12% and with an average power of 4.5 dBm.



(a) (b)

Figure 3.19: (a) Measured frequency doubler output spectrum before and after DPD. (b) 256-QAM constellation after DPD at an output frequency of 60 GHz.

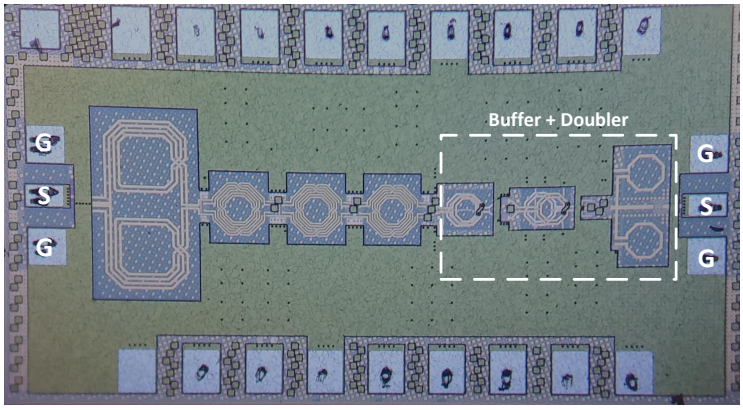


Figure 3.20: Micrograph of the fabricated chip where the white-dashed box highlights the proposed frequency doubler (i.e., the device under test in the following measurements).

3.4.2 Cascade of Buffer and Frequency Doubler

In this section, the performance of the proposed V-Band frequency doubler design (i.e., second prototype) is experimentally validated under CW and modulated signal excitations. Figure 3.20 depicts the micrograph of the fabricated chip, where the proposed design occupies a core area of $0.49 \times 0.52\ mm^2$. Note, the chip shows additional stages before the indented design of the buffer and doubler cascade. These stages are a phase shifter which will be discussed in detail in the next chapter. In this measurement, we are de-embedding the loss of the phase shifter and focusing on the intended frequency doubler design.

Continuous-Wave (CW) Measurements

The small-signal S-parameters of the cascaded buffer and frequency doubler design are measured using a linear vector network analyzer. Figure 3.21 presents the measured and simulated input reflection coefficient of the proposed design, showing a measured input return loss better than -13 dB from 27 GHz to 40 GHz. It should be noted that the slight frequency shift observed in the measurement compared to the simulation is attributed to simulation errors arising from the inaccuracies in the transistor model when biased in deep Class-C mode.

For the large-signal measurements, a non-linear vector network analyzer (Keysight N5247A) and a comb generator are employed. This is necessary to enable phase measurements and accurate amplitude readings of the device-under-test (DUT), considering that its input and output signals are centered at two different frequencies. The detailed

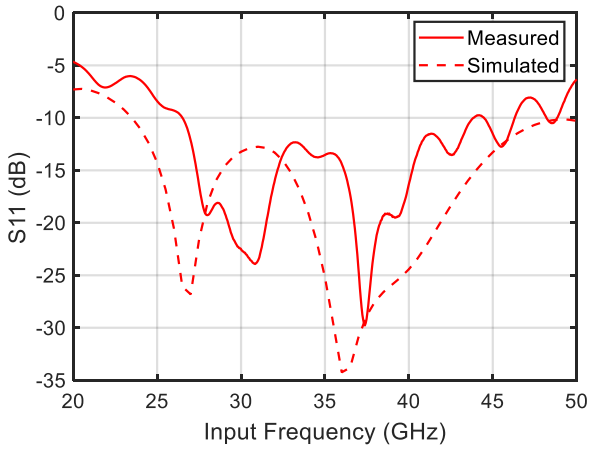
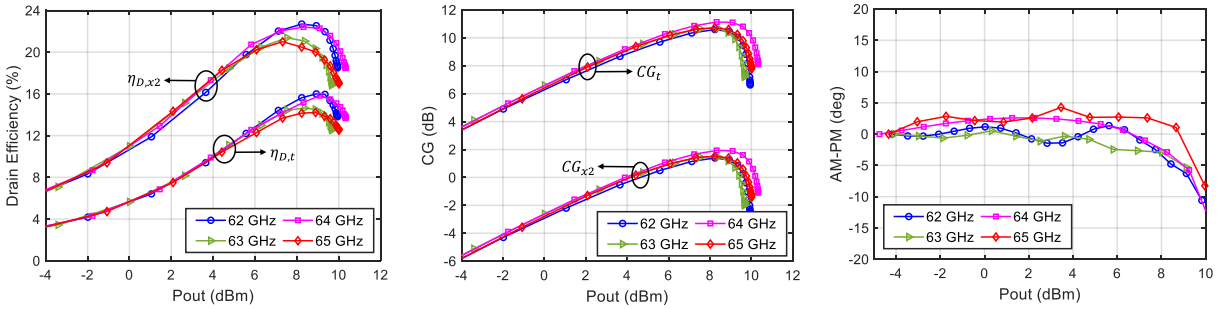


Figure 3.21: Measured and simulated input reflection coefficient of the proposed frequency doubler.

phase measurement technique will be presented in the next chapter (Section 4.6.1). Figures 3.22a and 3.22b show the measured RF performance versus output power for various frequencies. At an output frequency of 64 GHz, a total drain efficiency, $\eta_{D,t}$, of 16%, a doubler drain efficiency, $\eta_{D,\text{x2}}$, of 22.4%, and a total peak CG of 11.1 dB are measured. It is evident from Figures 3.22a and 3.22b that the proposed design maintains good performance from 62 GHz to 65 GHz, exhibiting less than 2% and 0.5 dB variation in $\eta_{D,t}$ and total CG, respectively. Hence, it validates the proposed theory presented in Section 3.2.1. Furthermore, at 6-dB output power back-off, a high $\eta_{D,\text{x2}}$ of 17.3% is obtained. After de-embedding the driver gain using simulation results, the frequency doubler achieves a peak CG of 2 dB.

To validate the impact of short-circuiting the 2^{nd} harmonic source impedance on phase linearity, the AM-PM of the proposed design is measured against the output power, as shown in Figure 3.22c for different frequencies. It can be observed that an AM-PM of less than 5.8° is achieved at 1-dB output power back-off for various frequencies. These results align with the proposed theory discussed in Section 3.2.2 and are consistent with the simulated results presented in Figure 3.10.

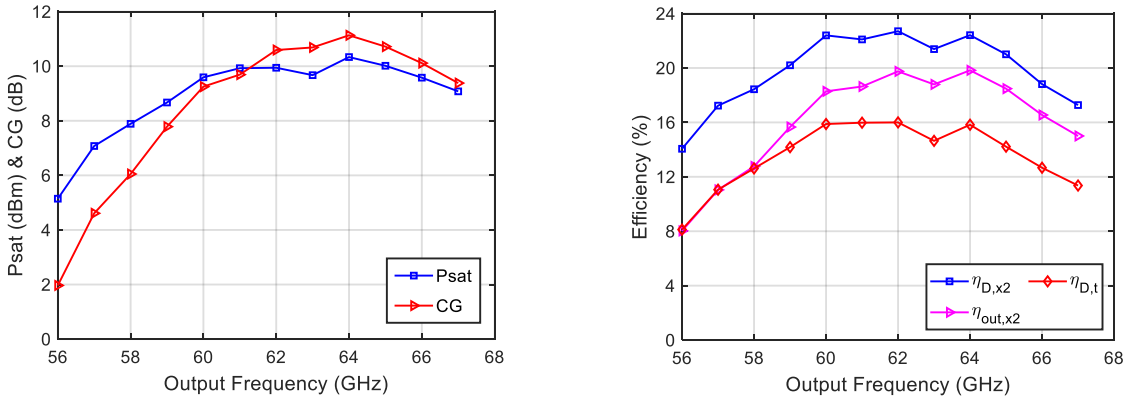
Figure 3.23 illustrates the measured RF performance of the proposed design across the output frequency range. The DC-to-RF efficiency of the frequency doubler, $\eta_{out,\text{x2}}$, is defined as $P_{out}/(P_{in,\text{x2}} + P_{dc,\text{x2}})$, where $P_{in,\text{x2}}$ and $P_{dc,\text{x2}}$ represent the input power and DC power consumption of the frequency doubler, respectively. As shown in Figure 3.23a, the fabricated frequency doubler exhibits a relatively high P_{sat} of 10.3 dBm, along with a 1-dB



(a) Drain efficiency. (b) CG. (c) AM-PM.

Figure 3.22: Measured RF performance of the proposed frequency doubler versus the output power for different frequencies.

P_{sat} bandwidth, BW_{1dB}, ranging from 59.5 GHz to 67 GHz. Across the BW_{1dB}, the design consistently maintains $\eta_{D,\text{x2}}$, $\eta_{out,\text{x2}}$, $\eta_{D,t}$, and total CG values greater than 17.3%, 15%, 11.5%, and 8.5 dB, respectively, as shown in Figure 3.23. It is important to note that the measurements were limited to frequencies up to 67 GHz due to the constraints of the test setup. Therefore, the design has not been evaluated above this frequency. Nevertheless, these results demonstrate the effectiveness of the proposed methodology in enhancing the output power and power efficiency over the designated bandwidth.



(a) Saturated output power and CG. (b) Efficiency.

Figure 3.23: Measured RF performance of the proposed frequency doubler versus the output frequency.

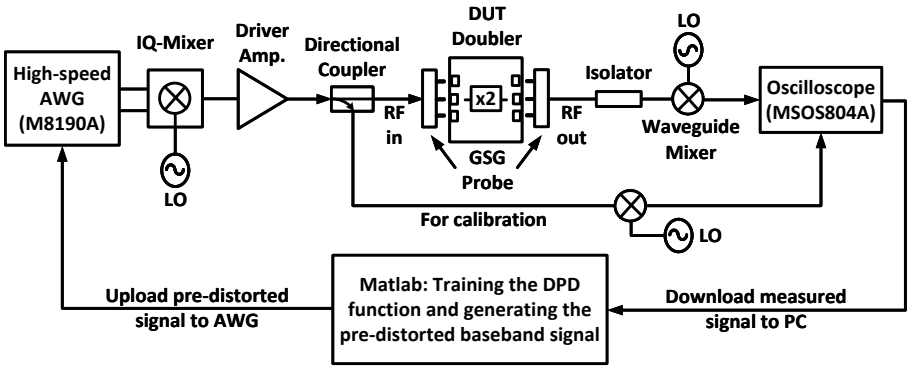


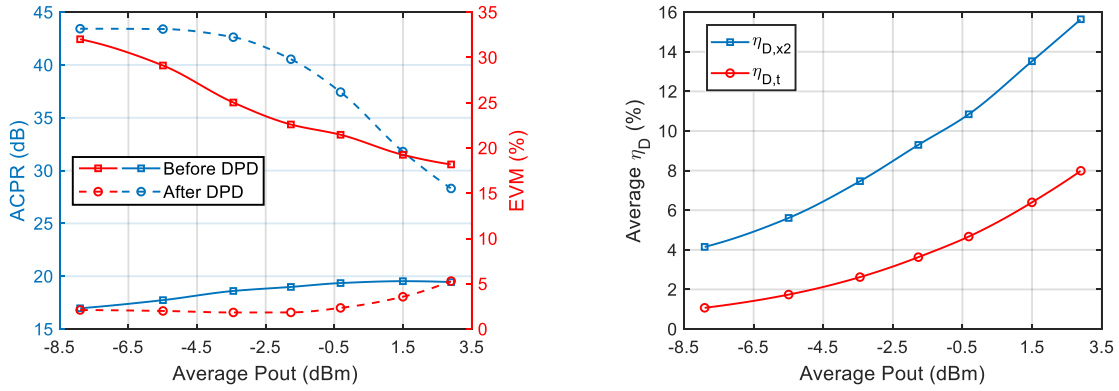
Figure 3.24: Experimental setup for the modulated signal measurements.

Modulated Signal Measurements

Figure 3.24 illustrates the measurement setup used for the modulated signal measurements. An arbitrary waveform generator (AWG) (Keysight M8190A) was utilized to generate an OFDM signal centered at 2 GHz. This signal was up-converted to a center frequency of 31 GHz using an IQ mixer (ADMV-1013) and amplified by a driver amplifier (HMC-1131) before being fed to the DUT. The DUT was mounted on a probe station, and GSG RF probes (67 GHz, infinity probes from FormFactor) were employed to access the DUT's input and output ports. The DUT output was connected to a waveguide isolator (Quinstar QIF-V00000), and the RF signal was down-converted using a WR-15 balanced mixer (Sage SFB-15-N1-M). A directional coupler was used to sample the driver output signal and provide feedback during transmitter calibration. The DUT's input and output signals were sampled using a 10-bit, 20 GS/s, 8 GHz analog bandwidth oscilloscope (Keysight MSOS804A). LO sources (Keysight MXG-N5183B and Hittite Microwave HMC-T2270) were employed to drive the up-conversion and down-conversion mixers in the setup.

The OFDM test signals used in the experiment had their subcarriers modulated using 256-QAM, with a subcarrier spacing of 120 kHz. These signals were characterized by a PAPR of 9 dB. To compensate for signal generator nonidealities and ensure error-free signals at the DUT, a linear source correction was performed using a multi-tone signal with a frequency spacing of 5 MHz and a modulation bandwidth of 3 GHz. The procedure outlined in [98] was followed for this purpose.

Figure 3.25 presents the modulated signal performance of the proposed frequency doubler versus the average output power at a $2f_o$ of 62 GHz when driven by a 400 MHz OFDM signal before and after DPD. The DPD used in this work is based on [22], where the nonlinearity order, nonlinear memory depth, and linear memory depth were set to 21,

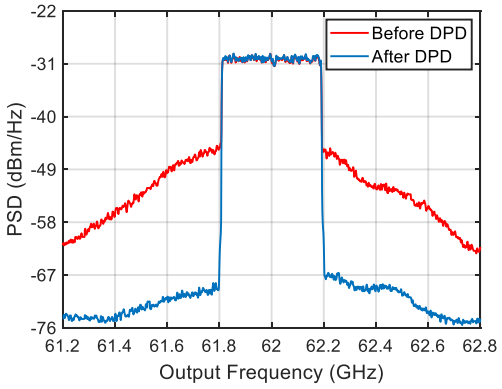


(a) (b)

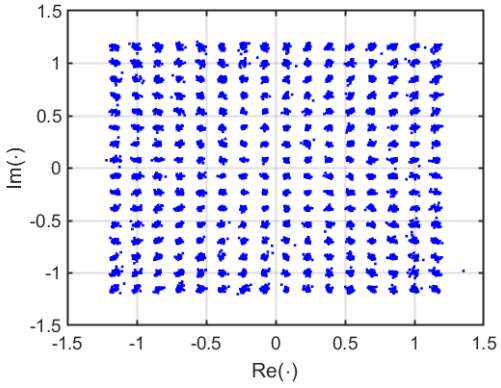
Figure 3.25: Measured (a) ACPR and EVM, and (b) average drain efficiency versus the average output power without DPD and with low-complexity DPD using 256-QAM OFDM signal with 400 MHz modulation bandwidth at a carrier frequency of 62 GHz.

3, and 10, respectively, resulting in a total of 65 coefficients. From Figure 3.25, it can be observed that when DPD is applied, the proposed frequency doubler achieved an output of up to 1.5 dBm average power, with an average $\eta_{D,\text{x2}}$ of 13.5% and an average $\eta_{D,t}$ of 6.4%. These results satisfy the 3GPP requirement for 256-QAM OFDM signals, with ACPR and EVM maintained below 31.8 dBc and 3.5%, respectively. Figure 3.26 depicts the power spectrum density (PSD), constellation plot, gain distortion, and AM-PM at the frequency doubler output, with the average power set to -1.8 dBm and average $\eta_{D,\text{x2}}$ and $\eta_{D,t}$ values of 9.3% and 3.6%, respectively, in the PSD and constellation plots. From Figure 3.26a, the ACPR and EVM improved from 19 dBc and 22.6% before DPD to 40.6 dBc and 1.8% after DPD, respectively. Moreover, Figure 3.26b, 3.26c, and 3.26d demonstrate a clean EVM constellation plot, flat gain response, and flat AM-PM after applying DPD to the proposed frequency doubler design, respectively. These results confirm the capacity of the proposed frequency doubler to generate vector modulated signals with high signal fidelity.

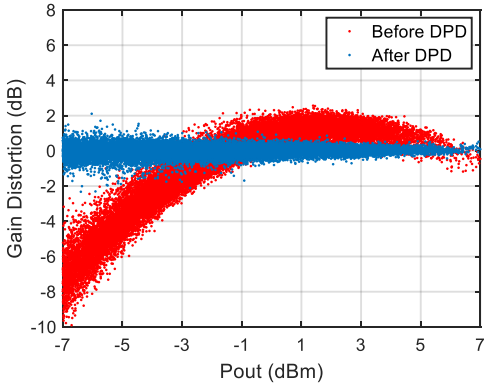
Table 3.1 provides a comparison of the CW performance of the proposed frequency doubler with state-of-the-art frequency doublers. Note, the values of CG and $\eta_{D,\text{x2}}$ are peak values. The proposed design achieves high output power and CG while maintaining good efficiency over the designated bandwidth. Additionally, this work presents the first reported AM-PM performance for a frequency doubler, achieving an AM-PM of less than 5.8° at 1-dB output power back-off. It should be noted that the inclusion of an additional buffer stage affects the overall bandwidth compared to a stand-alone frequency doubler design.



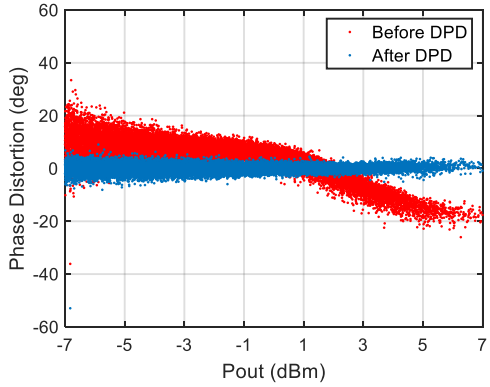
(a) Power spectrum density.



(b) Constellation.



(c) Gain distortion.



(d) Phase distortion.

Figure 3.26: Measured performance at the frequency doubler output with and without DPD using 256-QAM OFDM signal with 400 MHz modulation bandwidth at a carrier frequency of 62 GHz.

Table 3.1: CW Performance Comparison with State-Of-The-Art Frequency Doublers

Ref.	Technology	Topology	BW[a] (GHz)	P_{sat} (dBm)	CG (dB)	$\eta_{D,x2}$ (%)	AM-PM(°)	Area (mm^2)
[57]	90nm SiGe	x2	85-89[b]	4	0.7	16	–	0.6
[53]	65nm CMOS	x2+Buffer	58-64	5.7	0.8	–	–	0.33
[54]	65nm CMOS	Buffer+x2 +Buffer	58-61	5.6	9.1	–	–	0.62
[51]	65nm CMOS	x2	74[c]	2.5	-2.5	11.5	–	0.25
[56]	65nm CMOS	x2	77[c]	0	0.8	7.4	–	0.23
[55]	28nm CMOS	x2	50-60	5	1.2	12.6	–	0.17
[59]	28nm SOI CMOS	x2	79[c]	4.5	-1.4	24	–	0.1
[60]	45nm SOI CMOS	x2	50-83	7.4	-4.3	25(> 17.5,BW)	–	0.11[d]
This work	45nm SOI CMOS	x2+Buffer	59.5-67	10.3	11.1	22.4(> 17.3,BW)	5.8	0.25[d]

[a] 1-dB P_{sat} BW [b] Estimated from plot [c] Center Frequency [d] Excluding pads

Table 3.2 presents the modulated signal performance, which has not been evaluated in previous literature for frequency doublers.

3.5 Conclusion

This chapter presents a methodology for designing a high-power and high-efficiency mm-wave frequency doubler with improved AM-PM characteristics for vector modulated signal generation. First, the waveform engineering technique is applied to the push-push frequency doubler to determine the optimal harmonic load terminations. The sensitivity to harmonic impedance mismatch is carefully studied to reduce losses and complexity in the output matching network, while still maintaining acceptable output power and power efficiency across the designated bandwidth. Second, a theoretical formulation is derived to investigate the AM-PM characteristics of the frequency doubler taking into account the impact of parasitic input capacitance. This formulation provides insights into the potential

Table 3.2: Performance Summary of Frequency Doubler Under Modulated Signal Stimuli

Ref.	freq. (GHz)	Mod. Scheme	Technique	Mod. BW	ACPR (dBc)	EVM (%)	$P_{avg}{}^{a}$ (dBm)	$\eta_{D,x2}{}^{a}$ (%)	$\eta_{D,t}{}^{a}$ (%)
This work	62	256-QAM	DPD	400 MHz	40.6	1.8	-1.8	9.3	3.6
This work	62	256-QAM	DPD	400 MHz	32	3.5	1.5	13.5	6.4

[a] @ the reported EVM

solutions for selecting the second harmonic source impedance. A second harmonic input short is used to cancel the AM-PM nonlinearity of the frequency doubler. Measurement results demonstrate the effectiveness of the proposed design methodology.

Two frequency doubler prototypes operating at an output frequency of around 60 GHz have been successfully fabricated and evaluated. The first prototype is a stand-alone doubler that uses a stacked push-push configuration. It attains noteworthy performance metrics, yielding an output power of 12 dBm, a DC-to-RF efficiency of 20%, and a peak CG of 2.1 dB. Based on the success of the first prototype, the second prototype, consisting of a cascade of a buffer stage followed by the frequency doubler, is implemented. It achieved a doubler drain efficiency of 22.4%, a total drain efficiency of 16%, and a peak total CG of 11.1 dB at 64 GHz. Additionally, the AM-PM measurement yielded a result of less than 5.8° at 1-dB output power back-off for different frequencies. The proposed design attained a saturated output power of 10.3 dBm. Finally, by applying linearization techniques, the proposed frequency doubler is able to generate a 400 MHz vector modulated signal with an EVM of 3.5% and an average efficiency of 13%. It is worth noting that this thesis represents the first reported AM-PM measurements of a frequency doubler. Overall, the presented methodology enables the design of high-performance mm-wave frequency doublers with enhanced efficiency and AM-PM characteristics. The proposed design approach contributes to the advancement of frequency doubler technology, opening up possibilities for various applications in the mm-wave and sub-THz frequency bands.

Chapter 4

Frequency Doubler-Based RF Beamforming Front-End Module

4.1 Introduction

Unlike the conventional RF beamforming front-end architecture that uses a PA as a last stage, this work proposes a frequency multiplier-based RF beamforming front-end architecture that utilizes a frequency multiplier as a last stage for frequency up-conversion. However, to tailor a beamformer (e.g., phase shifter) for such frequency multiplier-based front-end, it is crucial to understand the design constraints imposed by the frequency multiplier on the beamformer design. This chapter starts with investigating the design considerations of the phase shifter in the context of a frequency multiplier-based front-end. Based on these considerations, an extensive study of the different RTPS topologies is conducted to guide the selection of the optimum topology that meets the pre-defined design constraints. Accordingly, an RTPS prototype is designed and validated experimentally. Subsequently, the RTPS is integrated with the frequency doubler design proposed in Chapter 3 to design a V-band frequency doubler-based RF beamforming front-end module. Figure 4.1 highlights the targeted building blocks that will be discussed in this chapter.

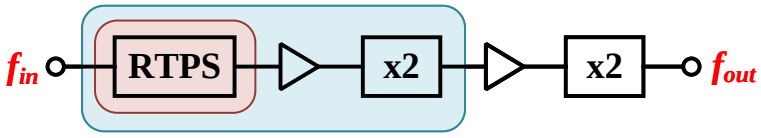


Figure 4.1: Proposed frequency multiplier-based RF beamforming front-end module, highlighting the focus of this chapter.

4.2 Design Considerations of Phase Shifter in Frequency Multiplier-Based RF Beamforming Front-End

The multiplication nature of the frequency multiplier-based RF beamforming front-end module imposes some design considerations on the PS. For instance, to achieve a full 360° phase range at the output of the front-end, the required phase tuning range of the PS, $\Delta\theta$, is determined by the frequency multiplier multiplication factor, N, and is given by,

$$\Delta\theta \in \left[0, \frac{360^\circ}{\mathrm{N}}\right]. \tag{4.1}$$

Similarly, the PS phase resolution, $\Delta\theta$, has to satisfy,

$$\Delta\theta_{res} = \frac{\Delta\theta_{res}^{ref}}{\mathrm{N}}, \tag{4.2}$$

where $\Delta\theta_{res}^{ref}$ is the desired phase resolution at the front-end output. While (4.1) shows that using frequency multiplier relaxes the required phase tuning range of the PS, (4.2) shows that it imposes more strict requirement on the phase error and, consequently, the required phase resolution of the PS. For instance, in the case of frequency doubler-based front-end (N = 2), the required tuning range of the PS is reduced to 180° based on (4.1). However, to achieve a 7-bit phase resolution at the front-end output, an 8-bit PS is required. Moreover, the magnitude variation of the PS will be multiplied by N at the front-end output; hence, this results in a higher requirement in terms of the PS CG variation which can be quantified as,

$$\Delta\mathrm{CG} = \frac{\Delta\mathrm{CG}^{ref}}{\mathrm{N}}, \tag{4.3}$$

where $\Delta\mathrm{CG}^{ref}$ is the desired magnitude variation at the front-end output. Thus, the frequency multiplier-based RF beamforming front-end puts more stringent requirements on the PS phase resolution and gain accuracy, despite allowing for a lower tuning range.

4.3 Choice of Phase Shifter Type

The choice of the PS type that meets the above-mentioned design constraints in Section 4.2 is crucial. The PS needs to exhibit low IL and high phase accuracy while minimizing the IL variation and group delay versus the phase shift. Based on the literature review of the PS presented in Section 2.4.2, the two major types of PS can be categorized into active and passive. Passive PSs are commonly preferred for large-scale phased-array realization as they offer zero power consumption and improved linearity over active PSs. The three main types of passive PSs discussed in the literature are the switched-type (STPS), the reflective-type (RTPS), and the loaded transmission line. The RTPS offers several advantages including compact size, moderate IL, low IL variation, and high phase resolution. Thus, it can be an excellent candidate that meets the strict requirements imposed by the frequency multiplier-based front-end module. In this work, RTPS is chosen to implement the PS. In the next section, we will go through the analysis and design of the implemented RTPS in detail.

4.4 Reflective-Type Phase Shifter (RTPS)

4.4.1 Basic Theory

Figure 4.2 depicts the RTPS block diagram which consists of a 90° hybrid coupler and two identical reflective loads at the coupled and through ports of the hybrid coupler. The input signal is split into two signals with 90° phase difference, which are then reflected by the two reflective loads at the coupled and through ports. Then, the reflected signals are combined in-phase at the RTPS output (i.e., the isolated port of the coupler) generating the desired output phase shift while canceling each other at the RTPS input (i.e., the input port of the coupler). The output phase shift of the RTPS can be varied by tuning the load impedance, Z_L, of the two reflective loads. Assuming the hybrid coupler has an IL of ξ, the output signal of the RTPS can be written as,

$$V_{out} = -j\Gamma_L \xi^2 V_{in}, \tag{4.4}$$

where V_{in} denotes the input signal to the RTPS and Γ_L designates the reflection coefficient of the reflective load. Accordingly, the output phase shift, θ, and the total insertion loss, IL_{RTPS}, of the RTPS are defined by,

$$\theta(^\circ) = -90^\circ + \angle\Gamma_L \tag{4.5}$$

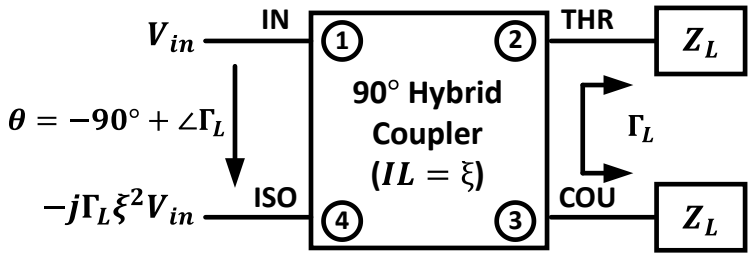


Figure 4.2: Block diagram of the reflective-type phase shifter (RTPS).

$$IL_{RTPS}(dB) = -20log(|\Gamma_L|) + 2\xi_{dB}. \tag{4.6}$$

Assuming that $\angle\Gamma_L$ can be tuned from a minimum value of $\angle\Gamma_{L,min}$ to a maximum value of $\angle\Gamma_{L,max}$, then the maximum achievable phase shift range, $\Delta\theta_m$, of the RTPS can be found using (4.5) by,

$$\Delta\theta_m(^\circ) = \angle\Gamma_{L,max} - \angle\Gamma_{L,min}. \tag{4.7}$$

It is to note that the design of the reflective load is crucial and affects the RTPS performance for different reasons. First, the accuracy of $\angle\Gamma_L$ directly determines the PS phase resolution as indicated by (4.5). Second, the IL and IL variation of the reflective load impacts IL_{RTPS} as given in (4.6). Lastly, the reflective-load tuning range defines the maximum achievable phase shift range as highlighted in (4.7). Hence, different topologies of the reflective load are commonly adopted. The key trade-off between them lies in the achievable phase shift range, IL, IL variation, and design complexity. Therefore, we need to investigate the performance of the different topologies to determine the optimum one that can be utilized to design an RTPS meeting the requirements of the frequency multiplier-based front-end defined in Section 4.2.

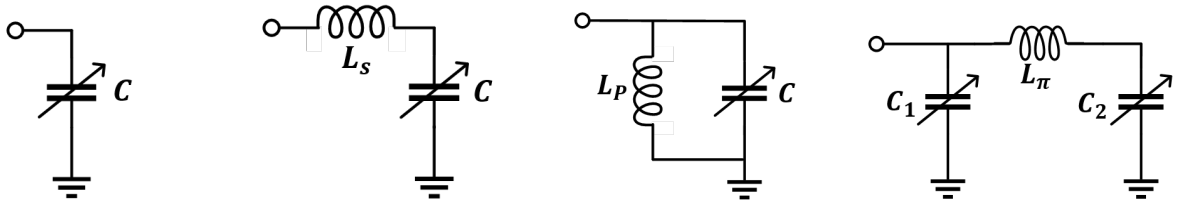
4.4.2 Analysis of Reflective-Load Topologies

Based on the PS literature in Section 2.4.2, four common topologies of the reflective load, shown in Figure 4.3, are considered which are capacitive, series LC, parallel LC, and CLC loads. In the following, a detailed theoretical analysis of each topology is carried out to determine the optimum topology for the RTPS design. The analysis procedure is as follows:

1. Formulate Z_L and Γ_L of the reflective load.
2. Define $|\Gamma_L|$ to study the IL and IL variation of each topology.

3. Define the phase shift range, $\Delta\theta$, for each topology.
4. Calculate the optimum L and C values to maximize the phase tuning range.
5. Formulate $\Delta\theta_m$ to determine the maximum achievable phase shift range of each topology.

This procedure is initially performed for the case of lossless reflective loads and is then extended to lossy loads to investigate the effect of reflective-load IL on $|\Gamma_L|$ and $\Delta\theta_m$. Also, the analysis is supported with schematic simulations to confirm the theory and to include the effect of components' parasitics.



(a) Capacitive load. (b) Series LC load. (c) Parallel LC load. (d) CLC load.

Figure 4.3: Common topologies of the RTPS reflective load.

Capacitive Reflective Load

For Lossless Load

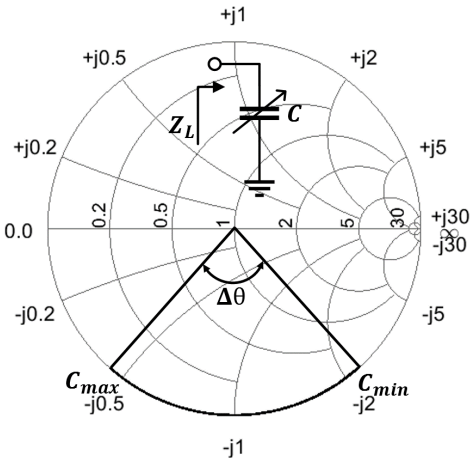
In capacitive reflective load, a variable capacitor is used to achieve the desired phase shift range. Ideally, 180° phase shift range can be obtained when the variable capacitor has $C_{max}/C_{min} = \infty$ (where C_{max} and C_{min} denote the maximum and minimum capacitance of the reflective load). However, this ratio is not practically conceivable, and only a finite value of C_{max}/C_{min} is realizable; consequently, yielding a phase shift range significantly lower than 180°. Figure 4.4a depicts graphically the impedance range of an ideal lossless capacitive load when the variable capacitor is tuned from C_{min} to C_{max}.

For lossless load, the load impedance of the capacitive load, $Z_{L,C}$, is given by,

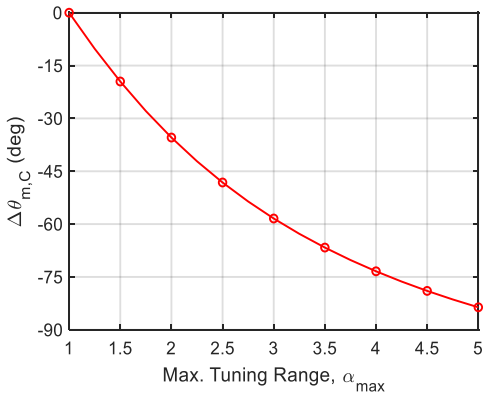
$$Z_{L,C} = jX_c = -1/\omega_o C, \tag{4.8}$$

where C denotes the capacitance value and ω_o designates the operating frequency. Accordingly, the reflection coefficient, $\Gamma_{L,C}$, can be expressed as,

$$\Gamma_{L,C} = \frac{Z_{L,C} - Z_o}{Z_{L,C} + Z_o} = \frac{1 - j\omega_o Z_o C}{1 + j\omega_o Z_o C}, \tag{4.9}$$



(a) Impedance tuning range.



(b) Maximum phase shift range versus α_{max}.

Figure 4.4: Performance of the lossless capacitive reflective-load topology.

where Z_o is the characteristic impedance. Let $k_c = Z_o/X_c$, $\Gamma_{L,C}$ can be re-written as,

$$\Gamma_{L,C} = \frac{1 - k_c^2 + 2jk_c}{1 + k_c^2}. \tag{4.10}$$

Based on (4.10), the magnitude of $\Gamma_{L,C}$ is equal to 1 as expected for the lossless load. While the phase of $\Gamma_{L,C}$ can be derived by

$$\angle\Gamma_{L,C} = tan^{-1}\left(\frac{2k_c}{1 - k_c^2}\right). \tag{4.11}$$

To find the achievable phase shift range, assume that the capacitor tuning range is equal to α where $1 \leq \alpha \leq \alpha_{max} = C_{max}/C_{min}$. Then, k_c can be varied such that

$$\begin{aligned} k_{c,min} &= Z_o/X_{c,min} = -Z_o\omega_o C_{min} \\ k_c &= Z_o/X_c = -Z_o\omega_o \alpha C_{min} = \alpha k_{c,min}. \end{aligned} \tag{4.12}$$

Using (4.11) and (4.12), the phase shift range of the capacitive load, $\Delta\theta_C$, is found by,

$$\begin{aligned} \Delta\theta_C &= \angle\Gamma_{L,C} - \angle\Gamma_{L,C,min} = tan^{-1}\left(\frac{2k_c}{1 - k_c^2}\right) - tan^{-1}\left(\frac{2k_{c,min}}{1 - k_{c,min}^2}\right) \\ &= tan^{-1}\left(\frac{2\alpha k_{c,min}}{1 - \alpha^2 k_{c,min}^2}\right) - tan^{-1}\left(\frac{2k_{c,min}}{1 - k_{c,min}^2}\right). \end{aligned} \tag{4.13}$$

Using the trigonometric identity,

$$tan^{-1}(u) \pm tan^{-1}(v) = tan^{-1}\left(\frac{u \pm v}{1 \mp uv}\right), \tag{4.14}$$

(4.13) can be re-written as,

$$\Delta\theta_C = tan^{-1}\left(\frac{2k_{c,min}(\alpha-1)(1+\alpha k_{c,min}^2)}{1-k_{c,min}^2(1+\alpha^2-4\alpha)+\alpha^2 k_{c,min}^4}\right). \tag{4.15}$$

Note, $\Delta\theta_C$ is a function of α and $k_{c,min}$ where α is limited by the capacitor tuning range allowed by the technology and $k_{c,min}$ is a design parameter depending on C_{min}.

To find the maximum phase shift range of the capacitive reflective load, $\Delta\theta_{m,C}$, for a specific α_{max}, the optimum C_{min} is derived by differentiating (4.15) with respect to C_{min} and equating to zero. Accordingly, the optimum C_{min} is found to be

$$C_{min,opt} = \frac{1}{\omega_o Z_o \sqrt{\alpha_{max}}}. \tag{4.16}$$

Hence, $\Delta\theta_{m,C}$ is found by

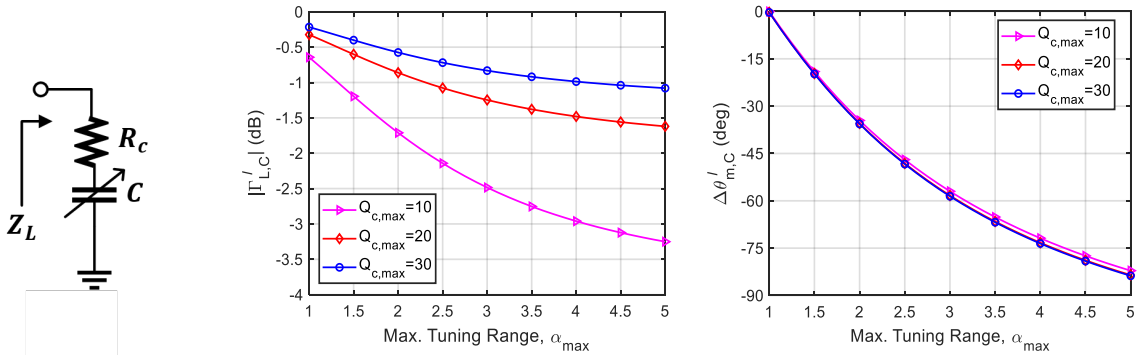
$$\Delta\theta_{m,C} = tan^{-1}\left(\frac{4\sqrt{\alpha_{max}}(\alpha_{max}-1)}{\alpha_{max}^2-6\alpha_{max}+1}\right). \tag{4.17}$$

Using (4.17), one can estimate the maximum achievable phase shift range of any capacitive reflective-load design for a given capacitance ratio of C_{max}/C_{min}. Figure 4.4b shows $\Delta\theta_{m,C}$ versus the maximum tuning range. For instance, a $\Delta\theta_{m,C}$ of 83.6° can be achieved when the load has an α_{max} of 5. Nevertheless, in reality, the variable capacitor suffers from a passive loss that affects IL and IL variation of the reflective load. Hence, the next step is to study the effect of the reflective-load loss on the $|\Gamma_{L,C}|$ and $\Delta\theta_{m,C}$.

For Lossy Load

Figure 4.5a depicts the schematic model of the lossy capacitive reflective load. R_c represents the series loss resistance of the variable capacitor and is defined as $R_c = 1/(\omega_o Q_c C)$ where Q_c denotes the capacitor quality factor. For the lossy load, the load impedance, $Z_{L,C}^l$, can be expressed as,

$$Z_{L,C}^l = R_c + jX_c = \frac{1}{\omega_o Q_c C} + \frac{1}{j\omega_o C}. \tag{4.18}$$



(a) (b) (c)

Figure 4.5: Lossy capacitive reflective-load topology: (a) schematic model, and (b) magnitude of the reflection coefficient and (c) maximum phase shift range versus α_{max}.

Using (4.18), the reflection coefficient, $\Gamma^l_{L,C}$, is found by,

$$\Gamma^l_{L,C} = \frac{1 + Q_c^2\left(1 - k_c^2\right) + 2jk_cQ_c^2}{1 + Q_c^2\left(1 + k_c^2\right) - 2k_cQ_c}. \tag{4.19}$$

Accordingly, its magnitude and phase can be separated into,

$$|\Gamma^l_{L,C}| = \frac{\sqrt{1 + Q_c^4\left(1 + k_c^2\right) + 2Q_c^2\left(1 - k_c^2\right)}}{1 + Q_c^2\left(1 + k_c^2\right) - 2k_cQ_c} \tag{4.20}$$

$$\angle\Gamma^l_{L,C} = tan^{-1}\left(\frac{2k_cQ_c^2}{1 + Q_c^2\left(1 - k_c^2\right)}\right). \tag{4.21}$$

Since Q_c will vary across the capacitor tuning range, one can define α_Q that will designate a range when Q_c is varied from a minimum value of $Q_{c,min}$ (occurs at $C = C_{max}$) to a maximum value of $Q_{c,max}$ (occurs at $C = C_{min}$). Hence, the range of α_Q can be written as,

$$1 \leq \alpha_Q \leq \alpha_{Q,max} = Q_{c,max}/Q_{c,min}. \tag{4.22}$$

Note, when $\alpha_Q = \alpha$, R_c will be a fixed resistance given by $R_c = 1/(\omega_o Q_{c,max} C)$ (i.e.,

function of $Q_{c,max}$). Then, using (4.21), the phase shift range, $\Delta\theta^l_C$, can be derived as

$$\begin{aligned}\Delta\theta^l_C &= \angle\Gamma^l_{L,C} - \angle\Gamma^l_{L,C,min} = tan^{-1}\left(\frac{2k_cQ_c^2}{1+Q_c^2(1-k_c^2)}\right) - tan^{-1}\left(\frac{2k_{c,min}Q_{c,max}^2}{1+Q_{c,max}^2(1-k_{c,min}^2)}\right)\\ &= tan^{-1}\left(\frac{2\alpha k_{c,min}Q_{c,max}^2/\alpha_Q^2}{1+\frac{Q_{c,max}^2}{\alpha_Q^2}(1-\alpha^2k_{c,min}^2)}\right) - tan^{-1}\left(\frac{2k_{c,min}Q_{c,max}^2}{1+Q_{c,max}^2(1-k_{c,min}^2)}\right).\end{aligned} \tag{4.23}$$

Equation (4.23) can be simplified using (4.14) to

$$\Delta\theta^l_C = tan^{-1}\left(\frac{2k_{c,min}Q_{c,max}^2\left[\alpha-\alpha_Q^2+Q_{c,max}^2(\alpha-1)(1+\alpha k_{c,min}^2)\right]}{\alpha_Q^2+Q_{c,max}^2\left[1+\alpha_Q^2-k_{c,min}^2(\alpha^2+\alpha_Q^2)\right]+Q_{c,max}^4\left[1-k_{c,min}^2(1-4\alpha+\alpha^2)+\alpha^2k_{c,min}^4\right]}\right) \tag{4.24}$$

Finally, for $\alpha = \alpha_{max}$, $\alpha_Q = \alpha_{Q,max}$, and $C_{min} = C_{min,opt}$, the maximum phase shift range for the lossy capacitive reflective load, $\Delta\theta^l_{m,C}$, can be formulated by,

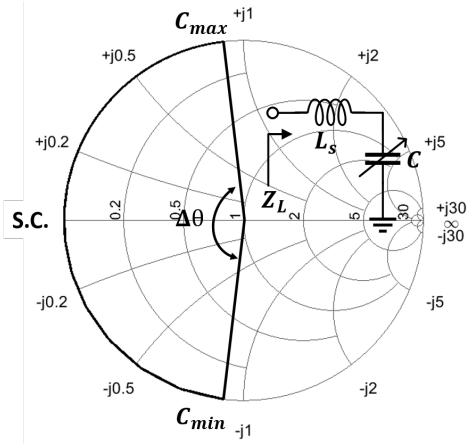
$$\Delta\theta^l_{m,C} = tan^{-1}\left(\frac{2Q_{c,max}^2\left[\alpha_{Q,max}^2-\alpha_{max}+2Q_{c,max}^2(1-\alpha_{max})\right]/\sqrt{\alpha_{max}}}{\alpha_{Q,max}^2+Q_{c,max}^2\left(1-\alpha_{max}\right)\left(1-\frac{\alpha_{Q,max}^2}{\alpha_{max}}\right)+Q_{c,max}^4\left(6-\frac{1+\alpha_{max}^2}{\alpha_{max}}\right)}\right). \tag{4.25}$$

Based on (4.20) and (4.25), Figures 4.5b and 4.5c depict the $|\Gamma^l_{L,C}|$ and $\Delta\theta^l_{m,C}$ of the lossy capacitive load versus the maximum tuning range for $Q_{c,max} = \{10, 20, 30\}$ at 30 GHz. From Figure 4.5b, the finite quality factor of the variable capacitor directly impacts $|\Gamma^l_{L,C}|$ and consequently affects the IL and IL variation of the reflective load. For instance, an average $|\Gamma^l_{L,C}|$ of -1.2 dB is obtained with a variation of $\pm$0.65 dB at $Q_{c,max} = 20$. On the other hand, Figure 4.5c shows that the finite quality factor of the variable capacitor doesn't affect the maximum achievable phase shift range compared to the lossless-load case.

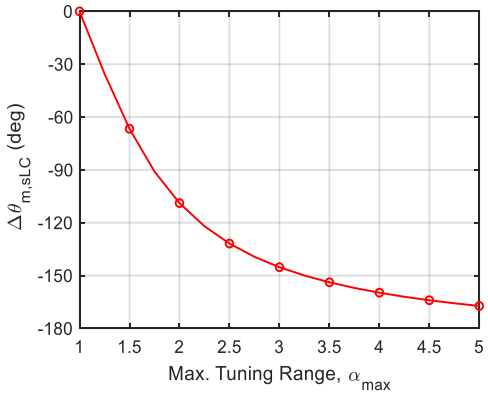
Series LC Reflective Load

For Lossless Load

More complex loads are investigated to achieve a higher phase shift range compared to the simple capacitive load. Figure 4.6a depicts the schematic model of a series LC reflective load topology which uses the variable capacitor in series with an inductor, L_s. Also, Figure 4.6a shows graphically the impedance range of that topology when the variable capacitor is tuned. At the resonance frequency, a short-circuit (S.C.) load is achieved while increasing C results in a more inductive load, and decreasing C moves the impedance to the capacitive region. Hence, depending on the capacitor tuning ratio, a specific phase shift range can be achieved.



(a) Impedance tuning range.



(b) Maximum phase shift range versus α_{max}.

Figure 4.6: Performance of the lossless series LC reflective-load topology.

For lossless load, the load impedance of the series LC load, $Z_{L,sLC}$, is given by,

$$Z_{L,sLC} = j(X_s + X_c) \tag{4.26}$$

where $X_s = \omega_o L_s$. Hence, the reflection coefficient, $\Gamma_{L,sLC}$, can be calculated by,

$$\Gamma_{L,sLC} = \frac{\left(1-\omega_s^2\right)^2 - k_c^2 + 2jk_c\left(1-\omega_s^2\right)}{\left(1-\omega_s^2\right)^2 + k_c^2} \tag{4.27}$$

where $\omega_s = \omega_o/\omega_{s,res}$ and $\omega_{s,res}$ is the resonance frequency and equals to $1/\sqrt{L_s C}$. From (4.27), the phase of $\Gamma_{L,sLC}$ can be extracted by,

$$\angle\Gamma_{L,sLC} = tan^{-1}\left(\frac{2k_c\left(1-\omega_s^2\right)}{\left(1-\omega_s^2\right)^2 - k_c^2}\right). \tag{4.28}$$

For a capacitor tuning range of α, ω_s will be varied such that,

$$\omega_s = \omega_o\sqrt{L_sC} = \sqrt{\alpha}\omega_{s,min} \tag{4.29}$$

where $\omega_{s,min} = \omega_o\sqrt{L_sC_{min}}$. Following the same procedure of the capacitive reflective load, the phase shift range of the series LC load, $\Delta\theta_{sLC}$, can be simplified to,

$$\Delta\theta_{sLC} = tan^{-1}\left(\frac{2k_{c,min}\Big[x_s\big(1-\omega_{s,min}^2\big) - \alpha y_s\big(1-\alpha\omega_{s,min}^2\big)\Big]}{x_sy_s + 4\alpha k_{c,min}^2\big(1-\omega_{s,min}^2\big)\big(1-\alpha\omega_{s,min}^2\big)}\right) \tag{4.30}$$

where

$$\begin{aligned} x_s &= \alpha^2\big(k_{c,min}^2 - \omega_{s,min}^4\big) + 2\alpha\omega_{s,min}^2 - 1 \\ y_s &= k_{c,min}^2 - \omega_{s,min}^4 + 2\omega_{s,min}^2 - 1. \end{aligned} \tag{4.31}$$

To formulate the maximum phase shift range, $\Delta\theta_{m,sLC}$, at a given $\alpha = \alpha_{max}$, the optimum L_s is calculated by differentiating (4.30) with respect to L_s and equating to zero. Accordingly, it is found to be:

$$L_{s,opt} = \frac{\alpha_{max}+1}{2\alpha_{max}C_{min}\omega_o^2}. \tag{4.32}$$

Using $C_{min,opt}$ obtained from (4.16) along with $L_{s,opt}$, $\Delta\theta_{m,sLC}$ of the lossless series LC load is defined by,

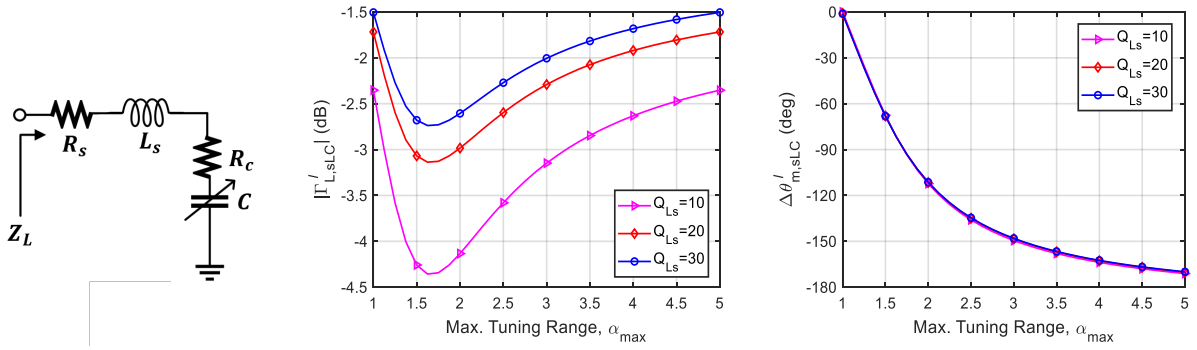
$$\Delta\theta_{m,sLC} = tan^{-1}\left(\frac{\sqrt{\alpha_{max}}(1-\alpha_{max})\big[8\alpha_{max} - (\alpha_{max}+1)^2\big]}{8\alpha_{max}^2 - 4\alpha_{max}(\alpha_{max}^2+1) + (\alpha_{max}+1)^4/8}\right). \tag{4.33}$$

The previous equation can be used to study the applicability of the series LC load to achieve a specific phase shift range for a given α_{max}. Figure 4.6b depicts $\Delta\theta_{m,sLC}$ versus the maximum tuning range. For $\alpha_{max} = 5$, one can maintain a $\Delta\theta_{m,sLC}$ of 167.2°. Hence, the series LC reflective load offers a better phase shift range compared to the capacitive one. Yet, the effect of its loss must be investigated to come to a precise conclusion.

For Lossy Load

Figure 4.7a shows the schematic used to model a lossy series LC reflective load where R_s and R_c designate the series loss resistance of L_s and C, respectively. From Figure 4.7a, the load impedance, $Z_{L,sLC}^l$, can be defined by,

$$Z_{L,sLC}^l = \big(R_s + R_c\big) + j\big(X_s + X_c\big) = \frac{X_s}{Q_{Ls}} - \frac{X_c}{Q_c} + j\big(X_s + X_c\big) \tag{4.34}$$



(a) (b) (c)

Figure 4.7: Lossy series LC reflective-load topology: (a) schematic model, and (b) magnitude of the reflection coefficient and (c) maximum phase shift range versus α_{max}.

where $R_s = (\omega_o L_s)/Q_{Ls}$ and Q_{Ls} is the quality factor of the inductor. Accordingly, the reflection coefficient of the lossy series LC load, $\Gamma^l_{L,sLC}$, is derived by,

$$\Gamma^l_{L,sLC} = \frac{Q_s^2\left[(1-\omega_s^2)^2 - k_c^2\right] + (\omega_s^2 Q_c + Q_{Ls})^2 + 2jk_c Q_s^2(1-\omega_s^2)}{(1-\omega_s^2)^2 Q_s^2 + (\omega_s^2 Q_c + Q_{Ls} - k_c Q_s)^2} \tag{4.35}$$

where $Q_s = Q_{Ls}Q_c$. From (4.35), $\Gamma^l_{L,sLC}$ magnitude and phase can be separated into

$$|\Gamma^l_{L,sLC}| = \sqrt{\frac{Q_s^4\left[(1-\omega_s^2)^2 + k_c^2\right]^2 + (\omega_s^2 Q_c + Q_{Ls})^4\left[(\omega_s^2 Q_c + Q_{Ls})^2 + 2Q_s^2((1-\omega_s^2)^2 - k_c^2\right]}{Q_s^4(1-\omega_s^2)^4 + (\omega_s^2 Q_c + Q_{Ls} - k_c Q_s)^2\left[(\omega_s^2 Q_c + Q_{Ls} - k_c Q_s)^2 + 2Q_s^2(1-\omega_s^2)^2\right]}} \tag{4.36}$$

$$\angle\Gamma^l_{L,sLC} = tan^{-1}\left(\frac{2k_c Q_s^2(1-\omega_n^2)}{(1-\omega_n^2)^2 Q_s^2 + (\omega_n^2 Q_c + Q_{Ls})^2 - k_c^2 Q_s^2}\right). \tag{4.37}$$

Similar to the procedure of the lossy capacitive load, by tuning the variable capacitor, α_Q will be varied such that $1 \le \alpha_Q \le \alpha_{Q,max}$. Hence, Q_s can be defined using α_Q as,

$$Q_s = Q_{Ls}Q_{c,max}/\alpha_Q = Q_{s,max}/\alpha_Q. \tag{4.38}$$

Based on (4.37), the phase shift range, $\Delta\theta^l_{sLC}$, can be found by,

$$\Delta\theta^l_{sLC} = tan^{-1}\left(\frac{2k_{c,min}Q^2_{s,max}\left[x'_s(\omega^2_{s,min}-1) - y'_s(\alpha/\alpha_Q^2)(\alpha\omega^2_{s,min}-1)\right]}{x'_s y'_s + 4k^2_{c,min}Q^4_{s,max}(\alpha/\alpha_Q^2)(\omega^2_{s,min}-1)(\alpha\omega^2_{s,min}-1)}\right) \tag{4.39}$$

where

$$x_s^{'} = \frac{Q_{s,max}^2}{\alpha_Q^2}\Big[\big(\alpha\omega_{s,min}^2 - 1\big)^2 - \big(\alpha k_{c,min}\big)^2\Big] + \big(\alpha\omega_{s,min}^2\frac{Q_{c,max}}{\alpha_Q} + Q_{Ls}\big)^2$$
$$y_s^{'} = Q_{s,max}^2\Big[\big(\omega_{s,min}^2 - 1\big)^2 - k_{c,min}^2\Big] + \big(\omega_{s,min}^2 Q_{c,max} + Q_{Ls}\big)^2. \tag{4.40}$$

Then, by substituting $L_{s,opt}$ and $C_{min,opt}$ in (4.39), the maximum phase shift range of the lossy series LC load, $\Delta\theta_{m,sLC}^l$, at a certain α_{max} and $\alpha_{Q,max}$ can be formulated as,

$$\Delta\theta_{m,sLC}^l = tan^{-1}\left(\frac{Q_{s,max}^2\big(\alpha_{max}-1\big)\big(\alpha_{Q,max}^2 x_s^{''} + \alpha_{max}^2 y_s^{''}\big)/\sqrt{\alpha_{max}}}{\alpha_{max}\alpha_{Q,max}^2 x_s^{''} y_s^{''} - Q_{s,max}^4\big(\alpha_{max}-1\big)^2}\right) \tag{4.41}$$

where

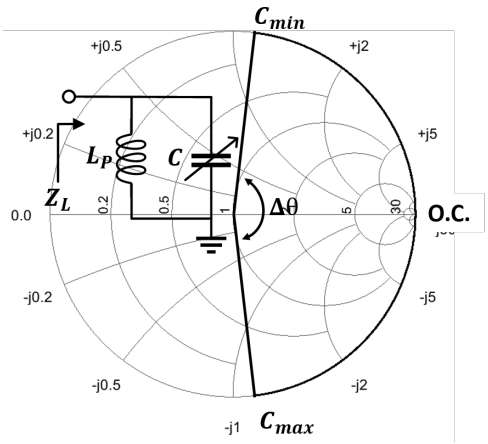
$$x_s^{''} = \frac{Q_{s,max}^2}{4\alpha_{Q,max}^2}\Big[\big(\alpha_{max}-1\big)^2 - 4\alpha_{max}\Big] + \big(Q_{c,max}\frac{\alpha_{max}+1}{2\alpha_{Q,max}} + Q_{Ls}\big)^2$$
$$y_s^{''} = \frac{Q_{s,max}^2}{4\alpha_{max}^2}\Big[\big(\alpha_{max}-1\big)^2 - 4\alpha_{max}\Big] + \big(Q_{c,max}\frac{\alpha_{max}+1}{2\alpha_{max}} + Q_{Ls}\big)^2. \tag{4.42}$$

Figures 4.7b and 4.7c depict $|\Gamma_{L,sLC}^l|$ and $\Delta\theta_{m,sLC}^l$ of the lossy series LC load versus α_{max} when $Q_{c,max} = 20$ and $Q_{Ls} = \{10, 20, 30\}$. An average $|\Gamma_{L,sLC}^l|$ of -2.4 dB is achieved with a variation of $\pm$0.7 dB when $Q_{Ls} = 20$. Also, as we get from Figure 4.7b, the magnitude variation of the reflective-load reflection coefficient can be enhanced by designing high-Q passive components. Moreover, similar to the lossy capacitive load, the finite quality factors of L_s and C do not affect the phase shift range as we can get from Figure 4.7c.

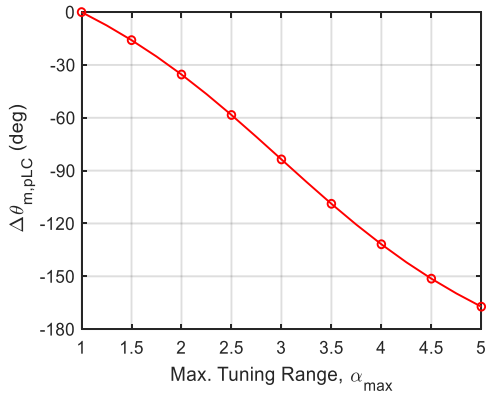
Parallel LC Reflective Load

For Lossless Load

The third reflective-load topology is the parallel LC where an inductor, L_p, is connected in parallel with the variable capacitor. Figure 4.8a shows the impedance tuning range of the parallel LC load. It has a single resonance where an open-circuit (O.C.) load impedance is achieved at resonance contrary to the series LC load which has a S.C. load termination at resonance. From Figure 4.8a, increasing C moves the load impedance to the capacitive region until it reaches its maximum value, C_{max}, and decreasing C moves the impedance to the inductive region until it reaches its minimum value, C_{min}. Hence, the parallel LC load can achieve a phase shift range close to that of the series LC load.



(a) Impedance tuning range.



(b) Maximum phase shift range versus α_{max}.

Figure 4.8: Performance of the lossless parallel LC reflective-load topology.

Assuming lossless load, the load impedance of the parallel LC load, $Z_{L,pLC}$, is given by,

$$Z_{L,pLC} = j(X_p//X_c) = j\frac{\omega_o L_p}{1-\omega_o^2 L_p C} \tag{4.43}$$

where $X_p = \omega_o L_p$. Hence, the load reflection coefficient, $\Gamma_{L,pLC}$, can be expressed as,

$$\Gamma_{L,pLC} = \frac{X_p^2 - Z_o^2\left(1-\omega_p^2\right)^2 + 2jX_pZ_o\left(1-\omega_p^2\right)}{X_p^2 + Z_o^2\left(1-\omega_p^2\right)^2} \tag{4.44}$$

where $\omega_p = \omega_o/\omega_{p,res}$ and $\omega_{p,res}$ is the resonance frequency given by $1/\sqrt{L_pC}$. Based on (4.44), $\Gamma_{L,pLC}$ phase is found by,

$$\angle\Gamma_{L,pLC} = tan^{-1}\left(\frac{2X_pZ_o\left(1-\omega_p^2\right)}{X_p^2 - Z_o^2\left(1-\omega_p^2\right)^2}\right). \tag{4.45}$$

A similar procedure as in the previous sessions is followed to formulate the phase shift range of the parallel LC load, $\Delta\theta_{pLC}$, as a function of $k_{c,min}$ and α. ω_p will be expressed in terms of α as follows,

$$\omega_p = \sqrt{\alpha}\omega_{p,min} \tag{4.46}$$

where $\omega_{p,min} = \omega_o\sqrt{L_pC_{min}}$. Accordingly, $\Delta\theta_{pLC}$ can be derived using (4.45) as,

$$\Delta\theta_{pLC} = tan^{-1}\left(\frac{2X_pZ_o\left[y_p(\alpha\omega_{p,min}^2 - 1) - x_p(\omega_{p,min}^2 - 1)\right]}{x_py_p + (2X_pZ_o)^2(\omega_{p,min}^2 - 1)(\alpha\omega_{p,min}^2 - 1)}\right) \tag{4.47}$$

where

$$x_p = Z_o^2\left(\alpha\omega_{p,min}^2 - 1\right)^2 - X_p^2$$
$$y_p = Z_o^2\left(\omega_{p,min}^2 - 1\right)^2 - X_p^2. \tag{4.48}$$

To find the maximum phase shift range, $\Delta\theta_{m,pLC}$, at a given α_{max}, the optimum L_p is calculated by differentiating (4.47) with respect to L_p and equating to zero; hence, it is found by,

$$L_{p,opt} = \frac{2}{(\alpha_{max}+1)C_{min}\omega_o^2}. \tag{4.49}$$

Using (4.16) for the value of $C_{min,opt}$, $\Delta\theta_{m,pLC}$ is formulated by

$$\Delta\theta_{m,pLC} = tan^{-1}\left(\frac{8\sqrt{\alpha_{max}}(\alpha_{max}-1)\left[(\alpha_{max}-1)^2 - 4\alpha_{max}\right]}{(\alpha_{max}-1)^4 - 24\alpha_{max}(\alpha_{max}-1)^2 + 16\alpha_{max}^2}\right). \tag{4.50}$$

Equation (4.50) is used to estimate the maximum achievable phase shift range of the lossless parallel LC load for a given tuning range of the variable capacitor. Hence, Figure 4.8b shows $\Delta\theta_{m,pLC}$ versus the tuning range α_{max}. A $\Delta\theta_{m,pLC}$ of 167.2° can be achieved for α_{max} of 5, which is similar to the lossless series LC topology.

For Lossy Load

Figure 4.9a depicts the schematic model of the lossy parallel LC reflective load where R_p designates the series loss resistance of L_p. From Figure 4.9a, the load impedance, $Z_{L,pLC}^l$, can be defined by,

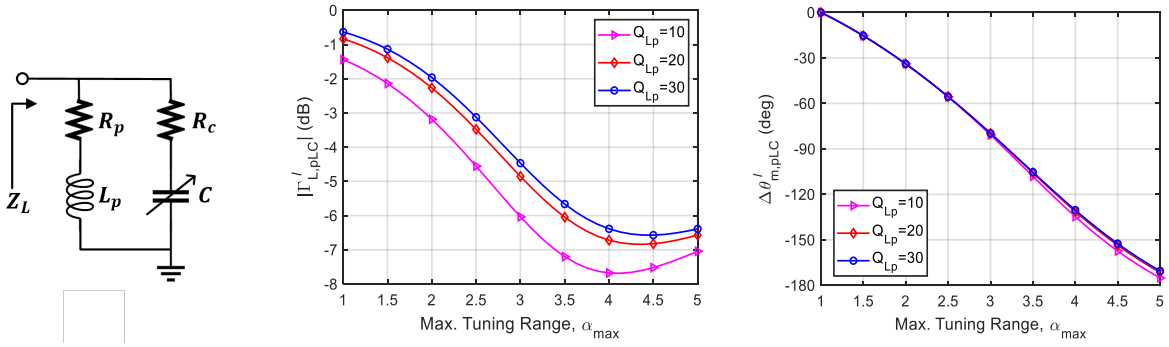
$$Z_{L,pLC}^l = (R_p + jX_p)//(R_c + jX_c) = \frac{-X_pX_c\left(1+jQ_{Lp}\right)\left(1-jQ_c\right)}{X_pQ_c\left(1+jQ_{Lp}\right) - X_cQ_{Lp}\left(1-jQ_c\right)} \tag{4.51}$$

where $R_p = (\omega_o L_p)/Q_{Lp}$ and Q_{Lp} is the quality factor of L_p. Hence, the load reflection coefficient, $\Gamma_{L,pLC}^l$, is derived by,

$$\Gamma_{L,pLC}^l = \frac{1+Q_p-Q_k+j\left[Q_L-Q_c+Q_p(k_c+k_L)\right]}{1+Q_p+Q_k+j\left[Q_L-Q_c-Q_p(k_c+k_L)\right]} \tag{4.52}$$

where $k_L = Z_o/X_p$, $k_c = Z_o/X_c$, $Q_p = Q_{Lp}Q_c$, and $Q_k = k_LQ_{Lp} - k_cQ_c$. Based on (4.52), the magnitude and phase of $\Gamma_{L,pLC}^l$ are extracted by,

$$|\Gamma_{L,pLC}^l| = \sqrt{\frac{\left[(1+Q_p)^2 - Q_k^2 + (Q_{Lp}-Q_c)^2 - Q_p^2k^2\right]^2 + \left[2Q_pk(1+Q_p) + 2Q_k(Q_{Lp}-Q_c)\right]^2}{\left[Q_p+Q_k+1\right]^2 + \left[Q_{Lp}-Q_c-kQ_p\right]^2}} \tag{4.53}$$



(a) (b) (c)

Figure 4.9: Lossy parallel LC reflective-load topology: (a) schematic model, and (b) magnitude of the reflection coefficient and (c) maximum phase shift range versus α_{max}.

$$\angle\Gamma^{l}_{L,pLC} = tan^{-1}\left(\frac{2Q_p k\left(1+Q_p\right)+2Q_k\left(Q_{Lp}-Q_c\right)}{\left(1+Q_p\right)^2-Q_k^2+\left(Q_{Lp}-Q_c\right)^2-Q_p^2k^2}\right) \tag{4.54}$$

where $k = k_c + k_L$.

By tuning the variable capacitor, Q_p will be varied such that

$$Q_p = Q_{Lp}Q_{c,max}/\alpha_Q = Q_{p,max}/\alpha_Q. \tag{4.55}$$

Note, $\alpha_Q = [1, \alpha_{Q,max}]$ denotes the tuning range of Q_c. Accordingly, the phase shift range, $\Delta\theta^{l}_{pLC}$, can be defined using (4.54) by,

$$\begin{aligned}\Delta\theta^{l}_{pLC} = &tan^{-1}\left(\frac{2Q'_{p,max}\left(1+Q'_{p,max}\right)\left(\alpha k_{c,min}+k_L\right)+2Q_k\left(Q_{Lp}-Q'_{c,max}\right)}{\left(1+Q'_{p,max}\right)^2-Q_k^2+\left(Q_{Lp}-Q'_{c,max}\right)^2-\left(Q'_{p,max}(\alpha k_{c,min}+k_L)\right)^2}\right)\\ &-tan^{-1}\left(\frac{2Q_{p,max}\left(1+Q_{p,max}\right)\left(k_{c,min}+k_L\right)+2Q_{k,min}\left(Q_{Lp}-Q_{c,max}\right)}{\left(1+Q_{p,max}\right)^2-Q_{k,min}^2+\left(Q_{Lp}-Q_{c,max}\right)^2-Q_{p,max}^2\left(k_{c,min}+k_L\right)^2}\right)\end{aligned} \tag{4.56}$$

where $Q'_{p,max} = Q_{p,max}/\alpha_Q$, $Q'_{c,max} = Q_{c,max}/\alpha_Q$, and $Q_{k,min} = k_{c,min}Q_{c,max} - k_L Q_{Lp}$. Then, by substituting $L_{p,opt}$ and $C_{min,opt}$ in (4.56), the maximum phase shift range of the

lossy parallel LC load, $\Delta\theta^{l}_{m,pLC}$, is simplified to,

$$\Delta\theta^{l}_{m,pLC} = tan^{-1}$$
$$\left(\frac{\left[\frac{Q_{p,max}(1-\alpha_{max})}{\alpha_{Q,max}}\left(1+\frac{Q_{p,max}}{\alpha_{Q,max}}\right) + \left(Q_{Lp} - \frac{Q_{c,max}}{\alpha_{Q,max}}\right)\left(2\alpha_{max}\frac{Q_{c,max}}{\alpha_{Q,max}} + (\alpha_{max}+1)Q_{Lp}\right)\right]/\sqrt{\alpha_{max}}}{(1+\frac{Q_{p,max}}{\alpha_{Q,max}})^2 - (\frac{\sqrt{\alpha_{max}}Q_{c,max}}{\alpha_{Q,max}} + \frac{\alpha_{max}+1}{2\sqrt{\alpha_{max}}}Q_{Lp})^2 + (Q_{Lp} - \frac{Q_{c,max}}{\alpha_{Q,max}})^2 - (\frac{Q_{p,max}(\alpha_{max}-1)}{2\alpha_{Q,max}\sqrt{\alpha_{max}}})^2} \right)$$
$$- tan^{-1}$$
$$\left(\frac{[Q_{p,max}(\alpha_{max}-1)(1+Q_{p,max}) + (Q_{Lp} - Q_{c,max})(2Q_{c,max} + (\alpha_{max}+1)Q_{Lp})]/\sqrt{\alpha_{max}}}{(1+Q_{p,max})^2 - (\frac{Q_{c,max}}{\sqrt{\alpha_{max}}} + \frac{\alpha_{max}+1}{2\sqrt{\alpha_{max}}}Q_{Lp})^2 + (Q_{Lp} - Q_{c,max})^2 - (\frac{Q_{p,max}(\alpha_{max}-1)}{2\sqrt{\alpha_{max}}})^2} \right). \tag{4.57}$$

From (4.53) and (4.57), Figures 4.9b and 4.9c show $|\Gamma^{l}_{L,pLC}|$ and $\Delta\theta^{l}_{m,pLC}$ of the lossy parallel LC load versus α_{max} when $Q_{c,max} = 20$ and $Q_{Lp} = \{10, 20, 30\}$. Figure 4.9b highlights an achieved average $|\Gamma^{l}_{L,pLC}|$ of -3.8 dB with a variation of $\pm$3 dB at $Q_{Lp} = 20$. It is important to note that the IL and its variation of the parallel LC load is much higher than that of the series LC load despite having a similar maximum phase shift range. From Figure 4.9c, the finite quality factors of the passive components do not affect the maximum achievable phase shift range.

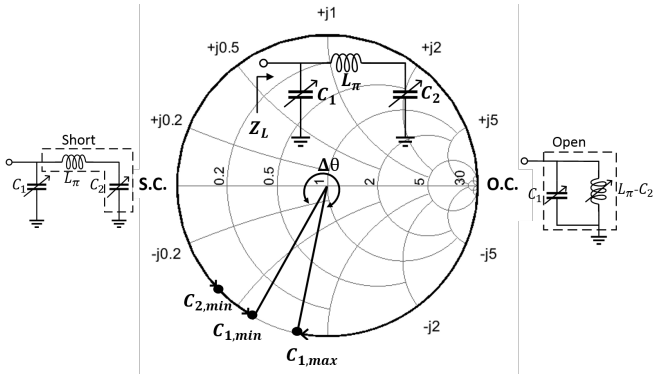
CLC (π-network) Reflective Load

For Lossless Load

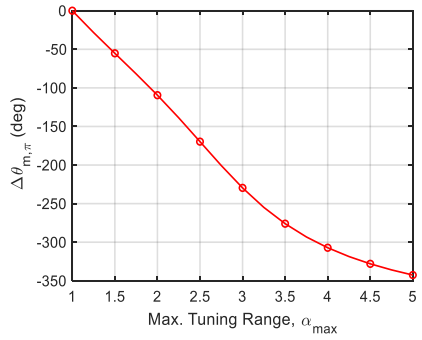
To maintain a higher phase shift range compared to the other topologies, a multi-resonance CLC reflective load is deployed which consists of two variable capacitors, C_1 and C_2, and an inductor, L_π, so that dual resonance is achieved. As shown in Figure 4.10a, for a certain C_1, L_π and C_2 form a series resonance (at S.C. point on Smith chart) where decreasing C_2 results in a capacitive load. Then, C_1 can be reduced to further extend the load trajectory in the capacitive region until $C_{1,min}$. On the other hand, increasing C_2 makes the equivalent of L_π-C_2 more inductive. Then, with tuning C_1, a parallel resonance between $(L_\pi - C_2)$ and C_1 is achieved at the O.C. point on Smith chart where increasing C_1 makes the load more capacitive resulting in an extended phase shift range until $C_{1,max}$.

For lossless load, the load impedance of the CLC load, $Z_{L,\pi}$, is given by,

$$Z_{L,\pi} = jX_{c1}//(jX_\pi + jX_{c2}) = j\frac{1-\omega_o^2 C_2 L_\pi}{\omega_o^3 C_1 C_2 L_\pi - \omega_o(C_1+C_2)} \tag{4.58}$$



(a) Impedance tuning range.



(b) Maximum phase shift range versus α_{max}.

Figure 4.10: Performance of the lossless CLC (π-network) reflective-load topology.

where $X_\pi = \omega_o L_\pi$, $X_{c1} = -1/\omega_o C_1$, and $X_{c2} = -1/\omega_o C_2$. Knowing that $\Gamma_L = (Z_L - Z_o)/(Z_L + Z_o)$, the reflection coefficient, $\Gamma_{L,\pi}$, is simplified to,

$$\Gamma_{L,\pi} = \frac{\left(\omega_\pi^2 - 1\right)^2 - \left(Z_o \omega_o C_{eq}\right)^2 - 2jZ_o\omega_o C_{eq}\left(\omega_\pi^2 - 1\right)}{\left(\omega_\pi^2 - 1\right)^2 + \left(Z_o \omega_o C_{eq}\right)^2} \tag{4.59}$$

where $\omega_\pi = \omega_o\sqrt{L_\pi C_2}$ and $C_{eq} = \omega_\pi^2 C_1 - C_1 - C_2$. Hence, $\Gamma_{L,\pi}$ phase can be extracted by,

$$\angle\Gamma_{L,\pi} = tan^{-1}\left(\frac{-2Z_o\omega_o C_{eq}\left(\omega_\pi^2 - 1\right)}{\left(\omega_\pi^2 - 1\right)^2 + \left(Z_o \omega_o C_{eq}\right)^2}\right). \tag{4.60}$$

For simplicity, we will assume that the two variable capacitors have the same $\alpha \in [1, \alpha_{max}]$ and that the ratio between them is β such that,

$$\begin{aligned} \alpha_{max} &= C_{1,max}/C_{1,min} = C_{2,max}/C_{2,min} \\ C_2 &= \alpha C_{2,min} \\ C_1 &= \beta C_2 = \beta\alpha C_{2,min}. \end{aligned} \tag{4.61}$$

Accordingly, the phase shift range of the CLC load, $\Delta\theta_\pi$, can be formulated by,

$$\begin{aligned} \Delta\theta_\pi = &tan^{-1}\left(\frac{2\alpha k_{c2,min}\left(\alpha\omega_{\pi,min}^2 - 1\right)\left(\alpha\beta\omega_{\pi,min}^2 - \beta - 1\right)}{\left(\alpha\omega_{\pi,min}^2 - 1\right)^2 - \alpha^2 k_{c2,min}^2\left(\alpha\beta\omega_{\pi,min}^2 - \beta - 1\right)^2}\right) \\ &- tan^{-1}\left(\frac{2k_{c2,min}\left(\omega_{\pi,min}^2 - 1\right)\left(\beta\omega_{\pi,min}^2 - \beta - 1\right)}{\left(\omega_{\pi,min}^2 - 1\right)^2 - k_{c2,min}^2\left(\beta\omega_{\pi,min}^2 - \beta - 1\right)^2}\right) \end{aligned} \tag{4.62}$$

where $k_{c2} = -Z_o\omega_o C_{2,min}$ and $\omega_{\pi,min} = \omega_\pi/\sqrt{\alpha}$.

To find the maximum phase shift range of the CLC load, $\Delta\theta_{m,\pi}$, for a certain $\alpha = \alpha_{max}$, the optimum L_π is derived from (4.62) and is found by,

$$L_{\pi,opt} = \frac{\sqrt{\beta k_{c2,min}^2[\beta\alpha_{max}^2(k_{c2,min}^2(\beta+1)^2+1)+\beta-2\alpha_{max}]+1}+\alpha_{max}\beta(\beta+1)k_{c2,min}^2-1}{\alpha_{max}(\alpha_{max}+1)C_{2,min}(\omega_o\beta k_{c2,min})^2} \tag{4.63}$$

Using $C_{2,min,opt} = 1/(\omega_o Z_o\sqrt{\alpha_{max}})$ as in (4.16), $\Delta\theta_{\pi,m}$ is derived by,

$$\begin{aligned}\Delta\theta_{m,\pi} = tan^{-1}&\left(\frac{2\sqrt{\alpha_{max}}\left(\alpha_{max}\beta\omega_{\pi,min,opt}^2-\beta-1\right)\left(\alpha_{max}\omega_{\pi,min,opt}^2-1\right)}{\alpha_{max}\left(\alpha_{max}\beta\omega_{\pi,min,opt}^2-\beta-1\right)^2-\left(\alpha_{max}\omega_{\pi,min,opt}^2-1\right)^2}\right)\\ -tan^{-1}&\left(\frac{2\sqrt{\alpha_{max}}\left(\beta\omega_{\pi,min,opt}^2-\beta-1\right)\left(\omega_{\pi,min,opt}^2-1\right)}{\left(\beta\omega_{\pi,min,opt}^2-\beta-1\right)^2-\alpha_{max}\left(\omega_{\pi,min,opt}^2-1\right)^2}\right)\end{aligned} \tag{4.64}$$

where

$$\omega_{\pi,min,opt}^2 = \frac{\sqrt{\frac{\beta}{\alpha}\left[\beta\alpha^2(\frac{(\beta+1)^2}{\alpha}+1)+\beta-2\alpha\right]+1}+\beta(\beta+1)-1}{\beta^2(\alpha_{max}+1)} \tag{4.65}$$

Figure 4.10b shows $\Delta\theta_{m,\pi}$ versus the maximum tuning range for $\beta = 1$. At $\alpha_{max} = 5$, a $\Delta\theta_{m,\pi}$ of 342.6° is achieved This shows the potential of the CLC reflective load to cover close to 360° phase shift range by choosing different α_{max} for the two variable capacitors and/or varying the ratio between them.

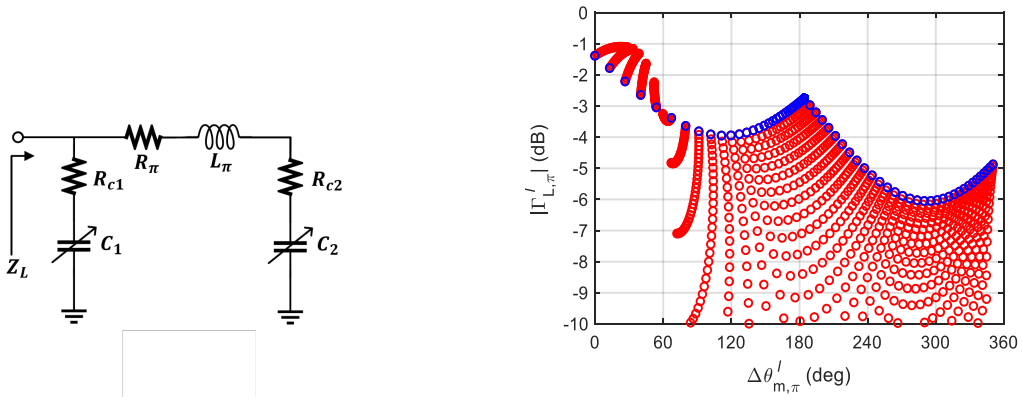
For Lossy Load

Figure 4.11a depicts the schematic model of the lossy CLC load where R_π, R_{c1}, and R_{c2} designate the series loss resistance of L_π, C_1, and C_2, respectively. Accordingly, the load impedance, $Z_{L,\pi}^l$, is found by,

$$Z_{L,\pi}^l = \left(R_{c1}+\frac{1}{j\omega C_1}\right)//\left(R_{eq}+j\omega L_{eq}\right) = \frac{R_{eq}-\omega^2 R_{c1}L_{eq}C_1+j\omega(L_{eq}+C_1R_{c1}R_{eq})}{1-\omega^2L_{eq}C_1+j\omega R_tC_1} \tag{4.66}$$

where

$$\begin{aligned}R_{eq} &= R_\pi + R_{c2}\\ R_t &= R_\pi + R_{c2} + R_{c1}\\ L_{eq} &= L_\pi - \frac{1}{\omega^2 C_2}.\end{aligned} \tag{4.67}$$



(a) (b)

Figure 4.11: Lossy CLC reflective-load topology: (a) schematic model, and (b) magnitude of the reflection coefficient, $\Gamma^l_{L,\pi}$, versus the maximum phase shift range for different α_{max} (in red) and for the selected points that achieve minimum $|\Gamma^l_{L,\pi}|$ variation (in blue).

It is important to note that the detailed theoretical analysis for the lossy CLC load is not included since the equations are so long that we can not make a concert conclusion. Alternatively, its schematic model, shown in Figure 4.11a, is simulated. Figure 4.11b shows the magnitude of the lossy CLC load reflection coefficient, $|\Gamma^l_{L,\pi}|$, versus its maximum phase shift range, $\Delta\theta^l_{m,pLC}$, when α_{max} of C_1 and C_2 is varied independently (in red) and when the points that achieve minimum $|\Gamma^l_{L,\pi}|$ variation are selected (in blue). Note, the passives' quality factors are set to 20. As per Figure 4.11b, an average $|\Gamma^l_{L,pLC}|$ of -3.8 dB is maintained with a variation of $\pm$2.4 dB is achieved.

Comparison and Conclusion

Since the previous analysis is based on ideal L and C components, we need to extend it by investigating the effect of components' parasitics on the behavior of different reflective load topologies. Hence, schematic simulations for the four topologies are carried out using non-ideal L and C components provided by the 45-nm CMOS-SOI process. A real varactor is utilized having $C_{min} = C_{min,opt} = 55fF$, $\alpha_{max} = 4.27$, and $Q_{c,max} = 15.8$. Also, the inductors' optimum values are calculated based on the derived equations such that

- For series LC topology: $L_{s,opt} = 363$ pH, $R_s = 2.3\ \Omega$
- For parallel LC topology: $L_{p,opt} = 223.5$ pH, $R_p = 1.72\ \Omega$

- For CLC (π-network) topology: $L_{\pi,opt} = 417.4$ pH, $R_{\pi} = 2.54\ \Omega$

Figure 4.12 depicts the simulated IL of the different RTPS reflective-load topologies versus the phase shift range, $\Delta\theta$, at 30 GHz. Note, IL is equal to $20log\big(|\Gamma_L|\big)$. The capacitive load has minimum IL and IL variation, but it suffers from a limited phase shift range. On the other hand, CLC reflective load can achieve a large phase shift range at the expense of more losses. Also, parallel LC topology shows significant IL variation compared to series LC topology despite having very close $\Delta\theta_m$. Additionally, Figure 4.13 shows the IL and group delay, GD, of the different topologies across frequency at zero phase shift. The capacitive load experiences the lowest IL variation and has an almost flat group delay. Table 4.1 summarizes the performance of the four analyzed reflective load topologies taking into account the components' parasitics.

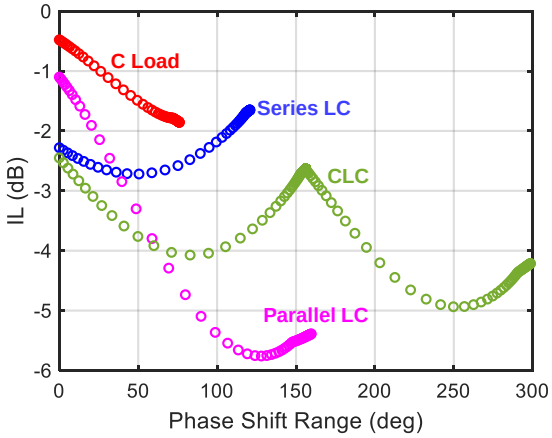
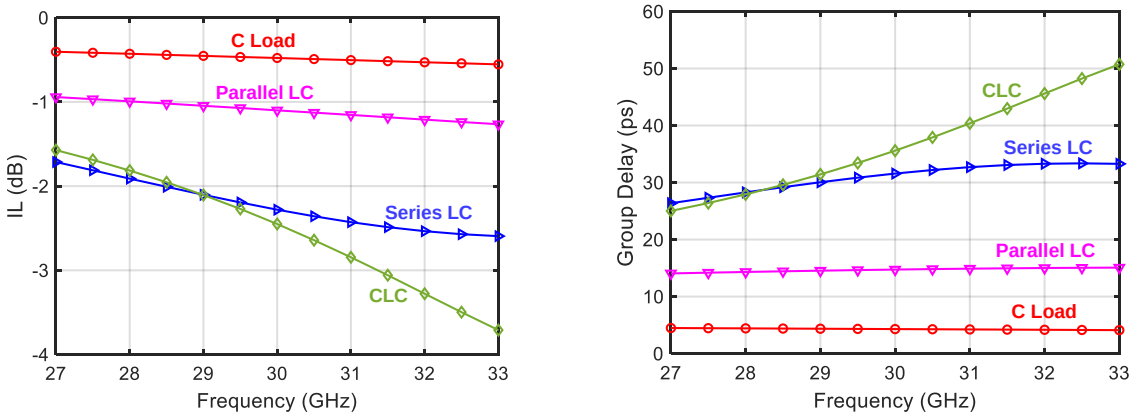


Figure 4.12: Simulated IL of the RTPS reflective load for different load topologies versus the phase shift range.

As a conclusion, Table 4.1 highlights that capacitive and series LC reflective loads yield the lowest IL and IL variation with phase setting as well as low variation across frequency compared to complex CLC load. However, they allow for a reduced phase tuning range. Based on the design considerations for the FM-based front-end module discussed in Section 4.2, capacitive and series LC loads are, hence, good candidates since the required PS tuning range is only 180°. In this work, a capacitive reflective load is adopted for the RTPS design as it has a better performance across frequency compared to the series LC load. The main limitation of the capacitive load is that it has a limited tuning range so multiple stages should be utilized to achieve a full 180°. In the next section, we will discuss the implementation of the capacitive reflective load.



(a) (b)

Figure 4.13: Simulated (a) IL and (b) Group delay of the RTPS reflective load for different load topologies versus frequency at zero phase shift.

Table 4.1: Performance comparison of the different RTPS reflective-load topologies

Reflective Load	Capacitive	Series LC	Parallel LC	CLC (β=1)
$\Delta\theta_m$	76°	120.8°	160.7°	289.5°
Avg. IL (dB)	-1.3	-2.35	-4	-4
ΔIL (versus $\Delta\theta$) (dB)	$\pm$0.69	$\pm$0.53	$\pm$2.3	$\pm$1.28
ΔIL at 0° (27-33 GHz) (dB)	$\pm$0.07	$\pm$0.45	$\pm$0.17	$\pm$1.07
ΔGD at 0° (27-33 GHz) (ps)	$\pm$0.19	$\pm$3.46	$\pm$0.51	$\pm$12.86

4.4.3 Implementation of RTPS Reflective Load

Based on the previous section, capacitive reflective-load topology is chosen for the RTPS design. A varactor-based tunable capacitor can be used to implement the variable capacitor. However, it would require bipolar tuning and typically exhibits relatively large IL variation versus the tuning value [99]. Alternatively, in this work, a switched-controlled (SC) capacitor bank that utilizes a new compensation technique is deployed to implement the variable capacitor. The proposed SC capacitor bank is also controlled digitally which minimizes the IL variation and complexity required for integration compared to the analog-controlled variable capacitor.

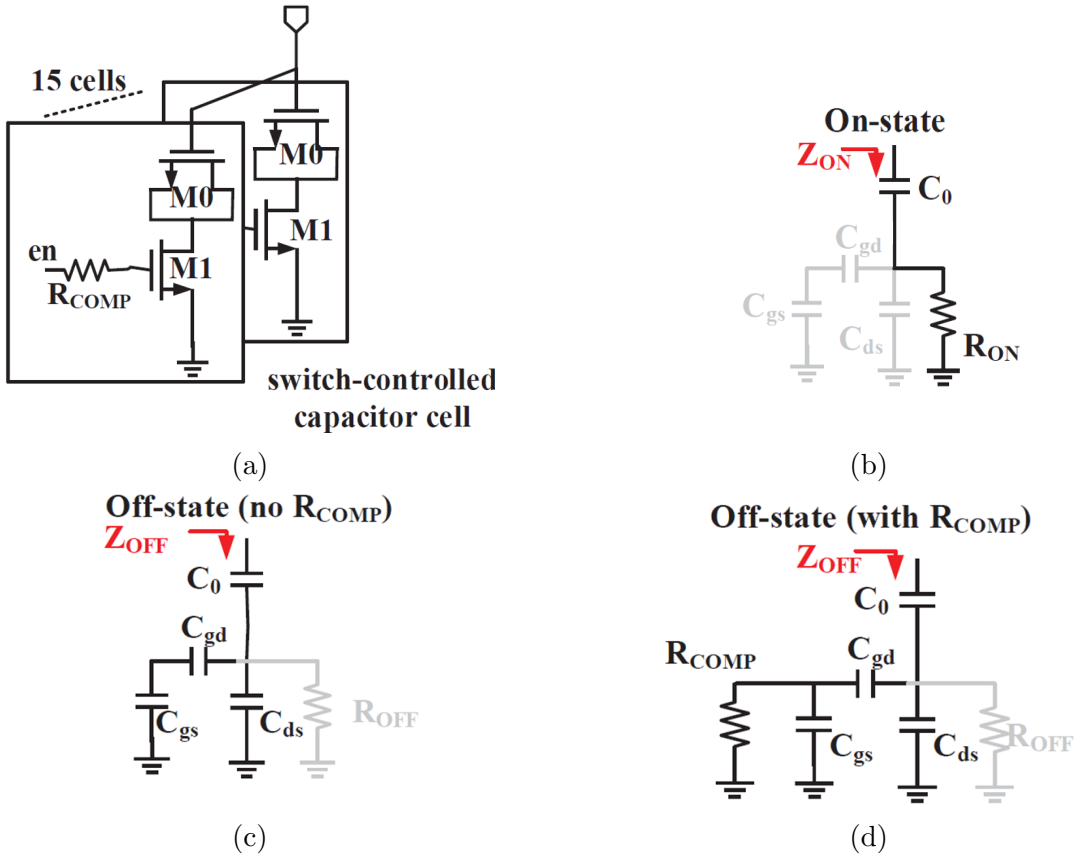


Figure 4.14: (a) Schematic of the proposed compensated SC capacitor bank with its equivalent small-signal model at (b) ON state, (c) OFF state without the compensation resistor R_{COMP}, and (d) OFF state with R_{COMP}.

Figure 4.14a shows the schematic of the proposed SC capacitive load. It consists of 15 identical cells controlled using a 4-bit digital code word. Each cell is implemented using a MOS capacitor (M0) and a transistor M1 that serves as an enabling/disabling switch. Figure 4.14b and Figure 4.14c show the equivalent small-signal circuit of a unit cell when the switch is turned ON and OFF, where Z_{ON} and Z_{OFF} denote the respective input impedance. During the ON state, the imaginary and real parts of Z_{ON} are determined by the MOS capacitor and R_{ON} of the switch, respectively. During the OFF state, Z_{OFF} is dominated by the parasitic capacitance of M1 and includes a negligible resistive component. The difference between Z_{ON} and Z_{OFF} of the different cells in the reflective load engenders a significant variation of $|\Gamma_L|$ with the code word and consequently leads to large IL variation across the phase shift range. To alleviate this problem, a compensation resistor, R_{COMP}, is added to the gate of transistors (i.e., M1 in each cell) as shown in Figure 4.14d. Its value is chosen according to the following constraints:

$$R_{ON} \leqslant R_{COMP} \leqslant R_{OFF} \tag{4.68}$$

where R_{ON} and R_{OFF} denote the resistance of the switch on its ON and OFF states, respectively. Figure 4.15 shows the magnitude of the reflection coefficient (in dB) as a function of the code word with and without R_{COMP}, obtained using post-layout simulation results. It confirms the minimization of $|\Gamma_L|$ variation over the code word range while maintaining similar capacitance values. The equivalent capacitance of the proposed topology is designed to have $C_{max}/C_{min} = 113fF/35fF = 3.1$. Given that this capacitance range would allow for a phase tuning of around 60°, three RTPS stages would be required to achieve 180°.

4.4.4 RTPS Design and Measurement Results

Figure 4.16 shows the block diagram of the proposed digitally-assisted RTPS (DA-RTPS) design which includes three 60° RTPS stages. For each stage, the reflective loads are designed using the 4-bit SC capacitor bank with compensation resistors, as discussed in Section 4.4.3. To minimize the overall IL of the three-stage RTPS, it is imperative to reduce the IL of the hybrid coupler, ξ. To accomplish this, a transformer-based coupler was chosen. Based on the transformer reported in [100], Figure 4.16 depicts the layout of the transformer-based differential hybrid coupler used to realize the proposed DA-RTPS. With a size of 120 by 120 μm, the EM-based optimization of the line width, spacing, and coil dimension choice yields a low IL of 0.45 dB and a phase mismatch of <1 at 30 GHz. Furthermore, for completeness of this PS design, a 1-bit 180° phase inverting stage is utilized at the RTPS output to achieve a full phase shift range of 360°.

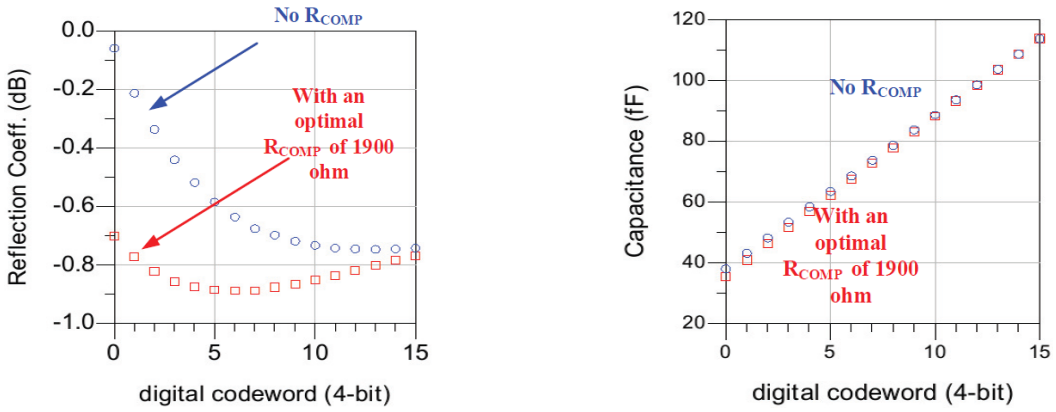


Figure 4.15: Post-layout simulation results of the proposed SC cell with and without R_{COMP} at 30 GHz.

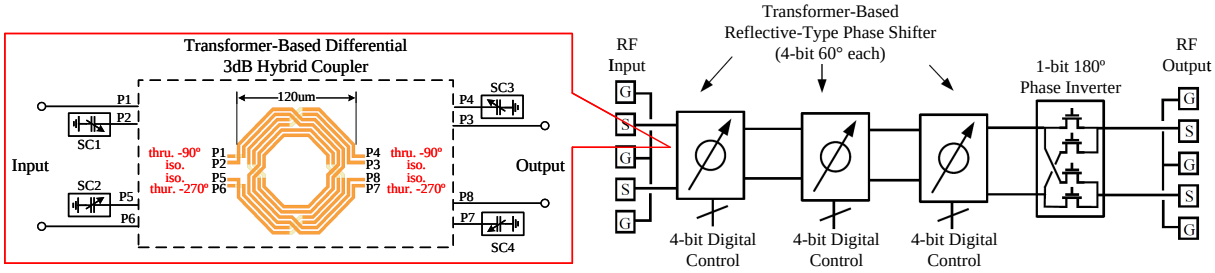


Figure 4.16: Block diagram of the DA-RTPS.

The proposed DA-RTPS is fabricated using GlobalFoundries' 45-nm SOI-CMOS process where a microphotograph of the fabricated prototype is shown in Figure 4.17a. A vector network analyzer (Keysight N5247A) was used to measure its performance. The digital code words were fed to the fabricated chip using an SPI-interface device (NI USB-8452). The DA-RTPS has a total of 13 control bits (i.e., 4-bits for each of the three RTPS stages and 1-bit for the phase inverter). To deduce the optimal code word, a pre-characterization step was conducted which sweeps all code word combinations. Figure 4.17b shows the corresponding phase shifts and IL obtained at 29 GHz. The proposed RTPS achieves a phase shift range of 360°, an excellent IL variation of ±0.4 dB regardless of the code word. Based on the pre-characterization results, a look-up-table (LUT) with 64 entries was constructed using the optimal code words needed to achieve a phase shift over 360° in a step of 5.6° while minimizing the IL variation. The DA-RTPS performance at 29 GHz with these

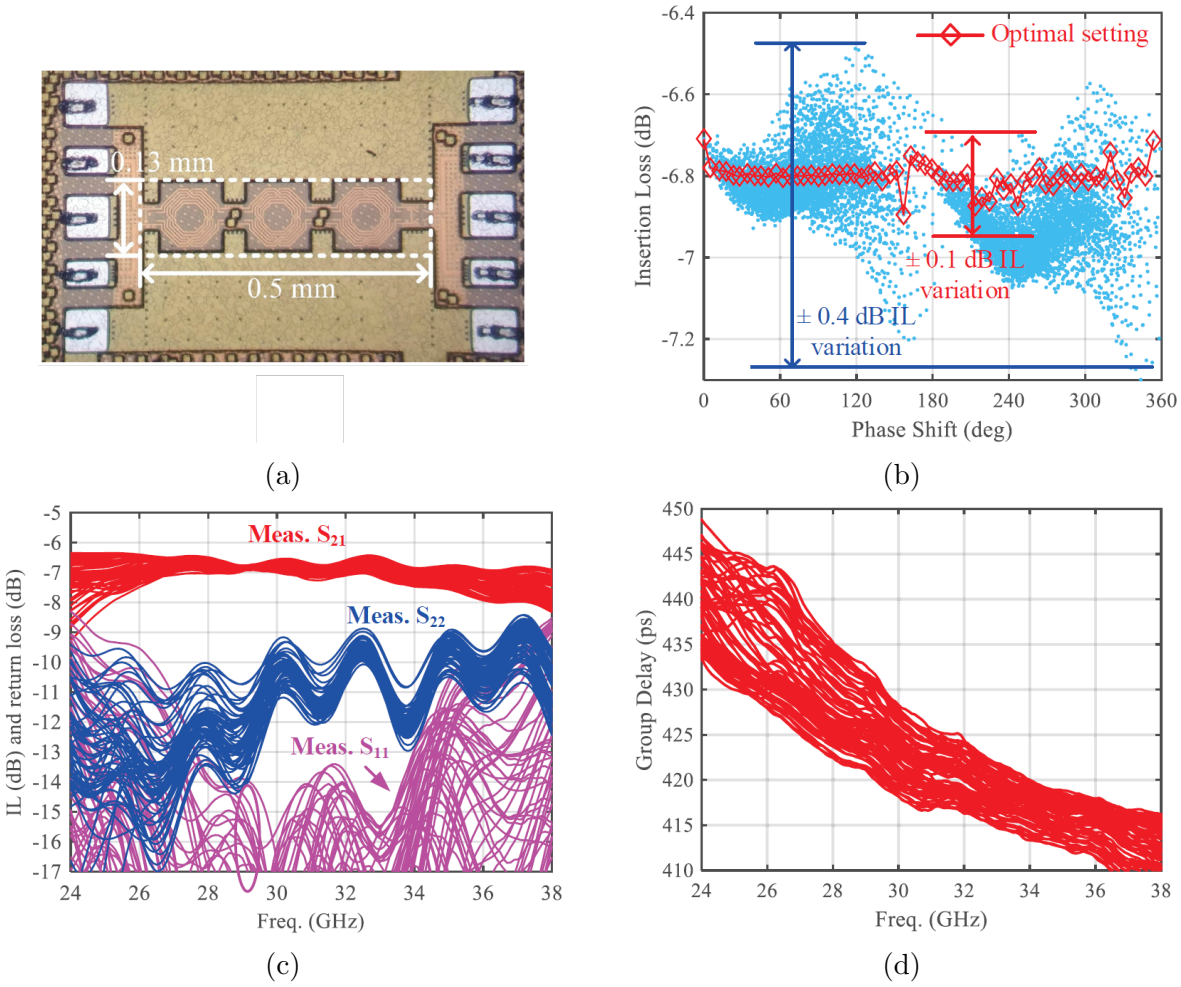
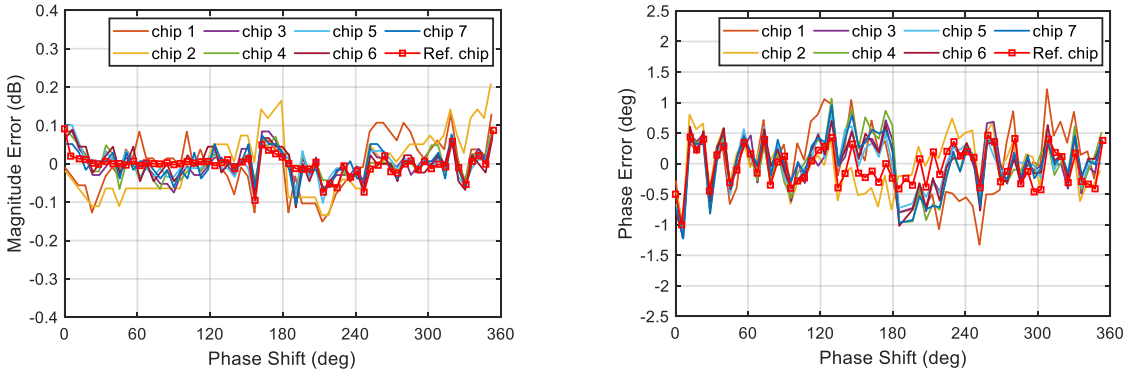


Figure 4.17: (a) Chip microphotograph of the fabricated DA-RTPS. Measured performance of the DA-RTPS: (a) phase shift versus IL using all code words (blue) and the selected optimal code words (red) that achieve optimal performances, (b) S-parameters using the optimal code words, and (c) group delay using the optimal code words.

optimal code words is highlighted in Figure 4.17b (in red) and demonstrates an IL variation of ±0.1 dB. Figure 4.17c shows measured small-signal performances corresponding to the 64 LUT entries. According to Figure 4.17c, an average IL of -6.8 dB is maintained within 1 dB of magnitude variation between 27 - 33 GHz (20% bandwidth). The measured input and output return losses were below -13.5 dB and -9 dB, respectively, in this bandwidth. Also, the measured group delay is shown in Figure 4.17d. A relatively constant group delay (±12 ps between 27 - 33 GHz) was achieved over 360° phase shift range.

To assess the process variation on the DA-RTPS, seven additional fabricated samples were measured using the same optimal code words, which were calculated from the pre-characterization results of one reference chip at 29 GHz. According to Figure 4.18, these seven chips maintained similar magnitude and phase error compared to the reference chip. Also, Table 4.2 highlights the numerical values of the IL variation and phase error for the different samples. The results demonstrate the potential of the proposed DA-RTPS for attaining high accuracy without requiring pre-characterization on every chip.



(a) Magnitude error.

(b) Phase error.

Figure 4.18: Measured performance of the DA-RTPS for different samples.

Table 4.2: IL variation and RMS phase error obtained from different samples.

	Ref. chip	chip 1	chip 2	chip 3	chip 4	chip 5	chip 6	chip 7
IL variation (dB)	±0.1	±0.12	±0.15	±0.08	±0.1	±0.1	±0.1	±0.09
RMS phase error (°)	0.3	0.58	0.41	0.43	0.5	0.39	0.44	0.46

Table 4.3 summarizes the measured performance of the fabricated DA-RTPS and compares it to the recently reported passive PSs at their best-reported frequency point. According to Table 4.3, the proposed DA-RTPS demonstrated the best root-mean-square (RMS) phase errors (0.3°), the lowest IL (-6.8±0.1 dB), and occupied the smallest area.

Table 4.3: Comparison of Recent Passive Phase Shifters

	This work	[93]	[95]	[89]	[99]
CMOS Tech.	45nm SOI	65nm	65nm	130nm SiGe	130nm SiGe
Topology	DA-RTPS	RTPS	RTPS	RTPS	DA-TL
Freq. (GHz)	29	28	29	62	28
Avg. IL (dB)	-6.8	-7.7	-8.3	-10	-9.3
IL variation (dB)	±0.1	±0.3	±0.2	±0.35	±0.25
Phase Range (°)	360	360	360	147	190
RMS phase error (°)	0.3[a]	0.3[a]	–	–	0.6[b]
Phase resolution (°)	5.6	11.25	22.5[c]	–	4.75
Area (mm^2)	0.065	0.16	0.076	0.16	0.18
Control Signal	Digital	Analog	Analog	Analog	Digital
FOM^d	52.1	45	42.3	35.5	19.9

[a] over 360° phase shift [b] over 190° phase shift [c] Estimated from plot [d] $FOM = \frac{\text{total phase shift (deg)}}{\text{max IL (dB)}}$

4.4.5 Conclusion

In this section, we investigated the design of RTPS reflective load to define the trade-offs between its different topologies. Based on this analysis, the capacitive reflective load is defined as the best candidate to meet the design constraints of the frequency multiplier-based front-end in terms of the IL, IL variation, phase shift range, phase accuracy, and group delay variation. Accordingly, we proposed a 3-stage RTPS design utilizing a capacitive reflective load which is implemented using a compensated SC-capacitor bank technique to improve the gain and phase accuracy. The fabricated RTPS chip showed an average IL of 6.8 dB, an IL variation of ±0.1 dB, and an RMS phase error of 0.3° at 29 GHz. Also, it demonstrated a 1-dB RF bandwidth spanning from 27 GHz to 33 GHz with a group delay below ±12 ps. In the next section, the proposed RTPS will be incorporated into the design of an RF beamforming chip.

4.5 Design of Frequency Doubler-Based RF Beamforming Front-End Module

Figure 4.19 shows the complete schematic of the proposed frequency doubler-based front-end module which consists of a cascade of a phase shifter, driver amplifier, and frequency doubler. For the phase shifter, the RTPS design discussed in Section 4.4.4 is utilized. It uses a capacitive reflective load implemented using a resistor-compensated SC-capacitor bank to minimize the IL variation across the phase shift range. For the front-end module having N = 2, the required phase tuning range of the RTPS is limited to 180°. Hence, a three-stage RTPS design is utilized with 60° tuning range per stage. Note, for N > 2, a subset of these stages can be utilized. The total number of control bits is 12 (4 bits*3) where each phase shift can be achieved using multiple settings of the digital code word. This allows for high bit resolution and gain accuracy by carefully selecting the optimum code words that minimize the IL variation across the phase shift range. The main challenge of using multiple stages is that the loss is multiplied by the number of stages; however, this can be mitigated by minimizing the loss per stage. Accordingly, a hybrid coupler with a low loss of 0.45 dB is designed.

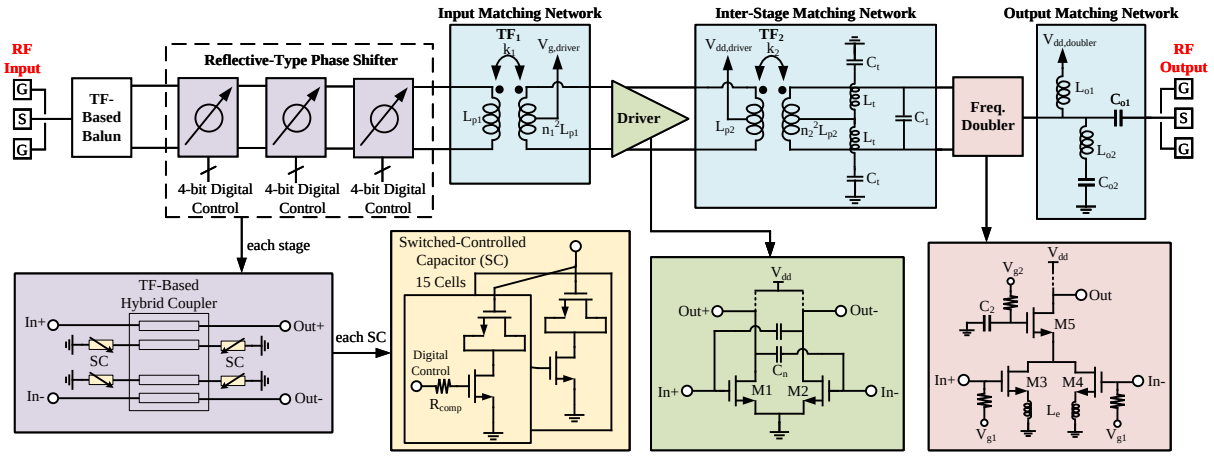


Figure 4.19: Complete schematic of the proposed frequency doubler-based RF beamforming front-end module.

To compensate for the losses incurred by the phase shifter and ensure adequate input power to the frequency doubler, a driver amplifier is added. Note, the driver is designed to operate at a lower frequency as it is located before the frequency doubler; hence, it can provide higher gain and better performance using 45-nm SOI CMOS. Figure 4.19 shows

the driver schematic, implemented using neutralized common-source transistors with a width of 120 μm. An input matching network (MN) is designed to match the driver source impedance to a 100-Ω termination at the RTPS output. It is implemented using a single transformer, TF_1, with the driver gate bias fed through the center-tap of the secondary coil. The designed input MN achieves an IL of 1.67 dB with good input and output match around 30 GHz.

For the frequency doubler, the stacked push-push topology discussed in Chapter 3 is utilized in this design and is also shown in Figure 4.19. This topology provides good fundamental suppression and has improved output power and efficiency compared to non-stacked designs. The bias of the stacked transistor and its gate capacitor, C_2, are chosen for equal voltage division between the two transistors. To reduce the front-end area and maximize its efficiency, the driver amplifier and the frequency doubler are co-designed where an inter-stage MN (comprised of TF_2 and C_1) is used to match the source impedance of the frequency doubler to the driver optimal load impedance. The driver V_{dd} is fed through the center-tap of the primary coil of TF_2. The center-tap of the secondary coil of TF_2 is used to provide a balanced second harmonic short at the frequency doubler input as it was found (in Section 3.2.2) to improve the AM-PM characteristics of the frequency doubler. Since the frequency doubler has a single-ended output, a simple LC network is utilized for the output MN design, converting the optimal 2^{nd} harmonic load impedance to 50 Ω. A fundamental short implemented using L_{o2} and C_{o2} is also added at the frequency doubler output to improve the fundamental rejection. The designed output matching achieves a passive efficiency of 89.5%.

4.6 Measurements of the Frequency Doubler-Based RF Beamforming Front-End Module

The performance validation of the proposed frequency doubler-based RF beamforming front-end module requires knowledge of both the magnitude and phase at the front-end's output. However, the phase measurement of the frequency doubler (i.e., a frequency multiplier) faces some challenges since its input and output ports operate at different frequencies. Hence, Section 4.6.1 summarizes these challenges and proposes a phase measurement technique for frequency multipliers. This technique will be utilized to measure the phase at front-end's output. Subsequently, Section 4.6.2 presents the full measurement results of the proposed frequency doubler-based RF beamforming front-end module.

4.6.1 Phase Measurement Technique for Frequency Multipliers

Challenges

As discussed in the previous chapters, in order to generate vector modulated signals at mm-wave and sub-THz frequency bands, frequency-converting devices are required to translate signals from an IF frequency to RF frequency. Conventionally, mixer-based frequency converters and high-frequency LO signals generated using a cascade of frequency multipliers and low phase-noise LO sources have been used for this purpose [101]. Alternatively, this thesis proposes frequency multiplier-based frequency converters, which incorporate frequency multipliers in the signal's main path for vector signal generation at mm-wave and sub-THz frequency bands. However, the successful deployment of vector signal generation using frequency converters requires the characterization of frequency-converting devices' magnitude and phase.

Measuring the phase of frequency converters is more challenging compared to non-frequency converting devices (e.g., power amplifiers and phase shifters) due to the frequency offset between input and output ports. Various phase measurement techniques have been proposed in the literature. One common approach involving a pair-wise measurement of three mixers, also known as the three mixer method, was proposed in [102–104]. This method requires two test mixers in addition to the mixer-under-test. One of the three frequency converter devices must provide reciprocal frequency response characteristics and all three frequency converter devices must be able to be operated as up- and down-converters. Alternatively, the Down/Up-conversion method can be used to measure the phase response of frequency converters using conventional S-parameter measurements with port de-embedding applied, if a "golden" reference mixer is provided, as discussed in [105, 106]. However, both of these methods are not suitable for measuring the phase distortion due to the required series connection between the mixers [106]. Moreover, these methods cannot be applied to frequency multipliers given that frequency multipliers are not reciprocal, do not have an LO port, and/or cannot be used as down-converters. Another approach proposed in [107] is to insert a reference frequency converter in the DUT's incident wave reference receiver path, which allows the received signal at the reference receiver to be at the same frequency as the DUT's output signal. However, this approach requires a reference frequency converter with known vector response versus frequency, which may not be always practical.

While these methods are effective for characterizing the phase distortion in mixer-based converters, they are not applicable to frequency multiplier-based converters because frequency multipliers are inherently nonlinear. In the next section, a new nonlinear vector

network analyzer (NVNA)-based technique is proposed to characterize the phase in frequency multipliers under CW excitation.

Proposed NVNA-Based Phase Measurement Technique

This section presents the theory of NVNA-based phase characterization in frequency multipliers under CW excitation. We consider the system shown in Figure 4.20, where a frequency multiplier of order N, is used as a DUT. For notation convenience, the analysis is carried out in the complex passband time domain. The incident wave at the frequency multiplier's input $a_1(t)$ can be expressed as follows,

$$a_1(t) = A_1 e^{j\omega_i t}, \tag{4.69}$$

where A_1 is the complex-valued coefficient of the incident wave, ω_i is the angular frequency of the multiplier input, and j is the imaginary unit. Assuming that the frequency multiplier output is matched, the transmitted wave around $N\omega_i$ at the frequency multiplier output, $b_2(t)$, can then be expressed as,

$$b_2(t) = SC_{21} A_1^N e^{jN\omega_i t}, \tag{4.70}$$

where SC_{21} is the complex-valued conversion gain of the frequency multiplier. Note that the ratio between (4.70) and (4.69) is not a constant and varies over time which is not the case in non-frequency conversion devices.

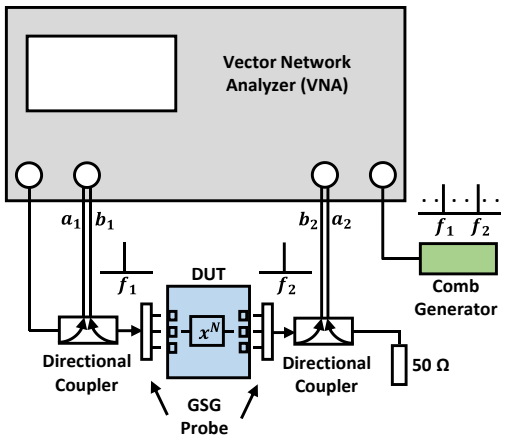


Figure 4.20: Block diagram of the proposed NVNA-based phase measurement technique for frequency multipliers.

To measure the phase response of the frequency multiplier conversion gain, $\angle SC_{21}$, a comb-generator that has a known phase relation between its tones can be used to act as a precise phase reference. The comb-generator output, denoted as $CG(t,\omega)$, can be expressed as,

$$CG(t,\omega) = C(\omega)e^{j\omega t}, \tag{4.71}$$

where $C(\omega)$ is the known complex coefficient of the comb-generator at angular frequency ω. Let Ω be the comb-generator frequency grid, i.e., $C(\omega) = 0$ for $\omega \notin \Omega$. Consequently, for $\omega_i \in \Omega$, we have $N\omega_i \in \Omega$, and the phase response of the frequency multiplier conversion gain can then be measured as follows,

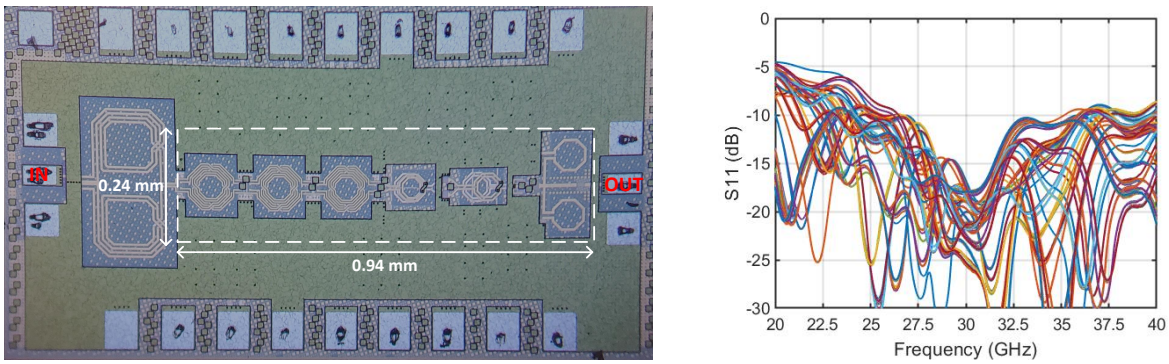
$$\angle SC_{21} = \angle\left[b_2(t) \cdot \frac{C(N\omega_i)}{CG(t,N\omega_i)}\right] - \angle\left[a_1(t) \cdot \frac{C(\omega_i)}{CG(t,\omega_i)}\right]^N. \tag{4.72}$$

Accordingly, the AM-PM of the frequency multiplier can be obtained using (4.72) by sweeping the incident wave power, allowing for the phase characterization of frequency multipliers under CW excitation.

4.6.2 Measurement Results of the Proposed Front-End Module

The proposed frequency doubler-based RF beamforming front-end module is fabricated using GlobalFoundries' 45-nm SOI-CMOS process. A micrograph of the fabricated chip is shown in Figure 4.21a where the core area is 0.94×0.24 mm^2. An on-chip balun is used for single-ended measurements. The digital code words are fed to the front-end using an SPI-interface device (NI USB-8452) to sweep the PS states. The losses of the probes and the on-chip balun are de-embedded from the measurements. Figure 4.21b shows the measured input reflection coefficient of the fabricated front-end when the digital code words are swept across all the phase states. It shows an input return loss of better than -10 dB from 27 GHz to 35 GHz across all the phase states.

A non-linear vector network analyzer (Keysight N5247A) and a comb-generator are used for large-signal measurements following the procedure described in Section 4.6.1. Since the RTPS has 12 control bits (4096 states), a pre-characterization step is performed where all the code words are varied and the optimal code words that achieve minimum CG variation across 360° phase range are selected. Figure 4.22 shows the measured peak CG and efficiency of the front-end for all the code words (in blue) and the optimal code words (in red) at different frequencies. Based on the pre-characterization step, the optimal code words are selected to cover 360° in a step of 2.8° while minimizing the CG variation; hence, a 7-bit phase resolution is achieved at the front-end output. This confirms the

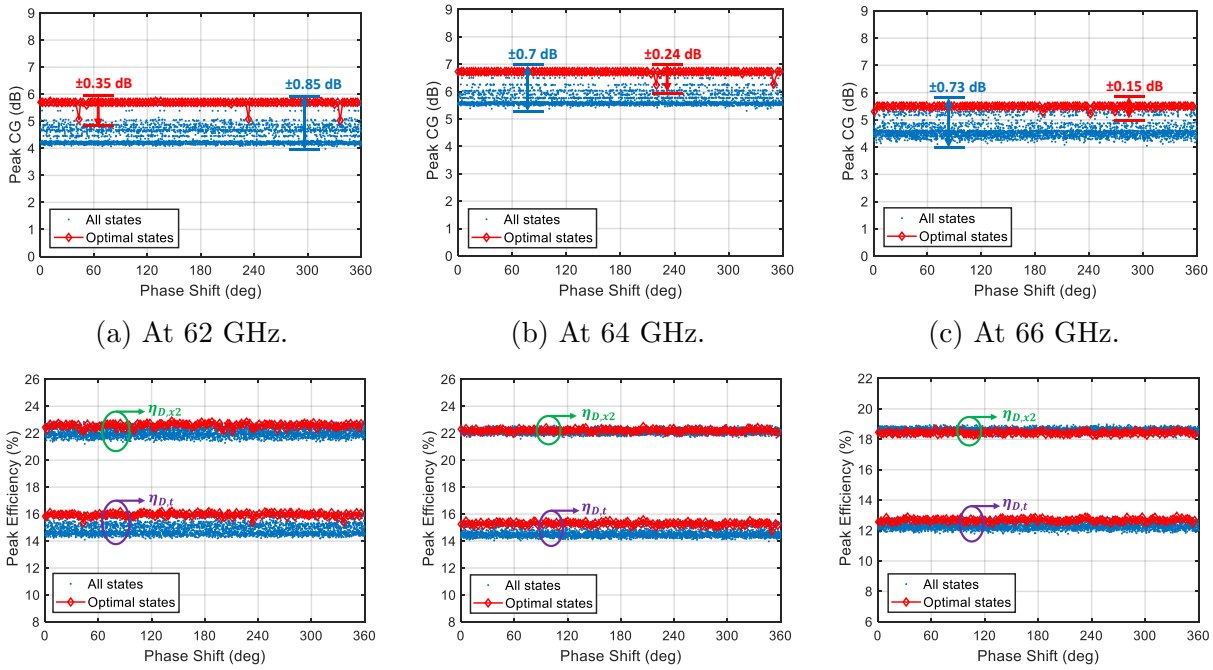


(a) (b)

Figure 4.21: (a) Micrograph of the fabricated frequency doubler-based RF beamforming front-end module. (b) Measured S11 of the front-end module for all the phase states.

advantage of having more stages in the PS design to achieve high phase and gain accuracy by carefully selecting the optimal code words among different phase settings. For instance, from Figure 4.22a, the proposed front-end has an average CG of 5.7 dB at 62 GHz output frequency with a low of ±0.35 dB variation and an RMS phase error of 0.57°. Note, the simulated gain of the driver amplifier is 9 dB at the output 1-dB compression, and the simulated peak CG of the doubler is 1.5 dB. Also, from Figure 4.22d, a doubler drain efficiency, $\eta_{D,\text{x2}}$, of 22.7% and a front-end drain efficiency, $\eta_{D,t}$, of 16% are achieved at 62 GHz output frequency with a variation of ±0.35% and ±0.4%, respectively, across full 360° phase tuning with a step of 2.8°. These results are maintained versus frequency as depicted in Figure 4.22. Moreover, the proposed front-end achieves a saturated output power of 10.3 dBm.

Figure 4.23a shows the absolute error of the front-ends' peak CG and $\eta_{D,t}$ versus the phase error. It highlights the major trade-off between the gain and phase accuracy, where a low CG error of ±0.06 dB can be obtained if the phase error requirement is relaxed to 1.4° for the 7-bit front-end's phase resolution. Hence, the proposed front-end allows for optimizing the trade-off between CG and phase errors depending on the application requirements. Furthermore, for applications targeting different front-end phase resolutions (i.e., 6-bit), the choice of the optimal states can be tailored to meet the required phase resolution with acceptable gain and phase accuracy. For example, an output phase resolution of 6-bit can be achieved with an almost zero CG error and an $\eta_{D,t}$ absolute error less than ±0.28% across the full 360°. Figures 4.23b and 4.23c show the measured CG and total efficiency of the front-end module across the measured phase shifts using 6-bit



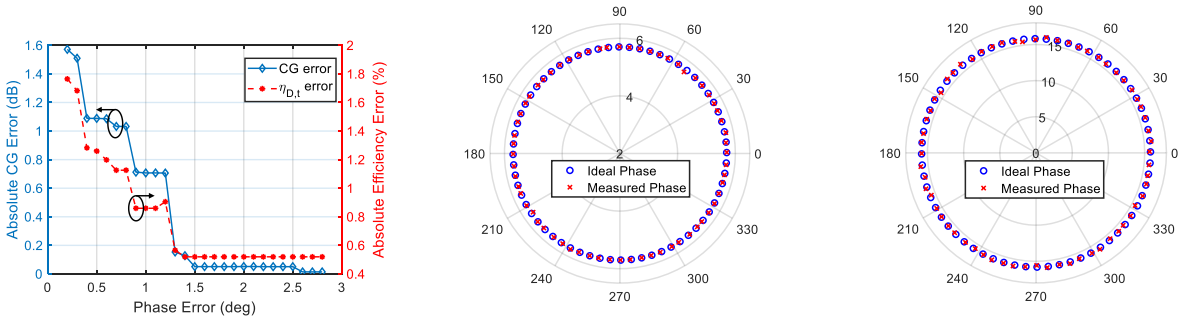
(a) At 62 GHz. (b) At 64 GHz. (c) At 66 GHz.

(d) At 62 GHz. (e) At 64 GHz. (f) At 66 GHz.

Figure 4.22: Measured (a)-(c) peak CG and (d)-(e) peak efficiency of the front-end module versus the measured phase shifts using all code words (in blue) and selected code words (in red) at different output frequencies.

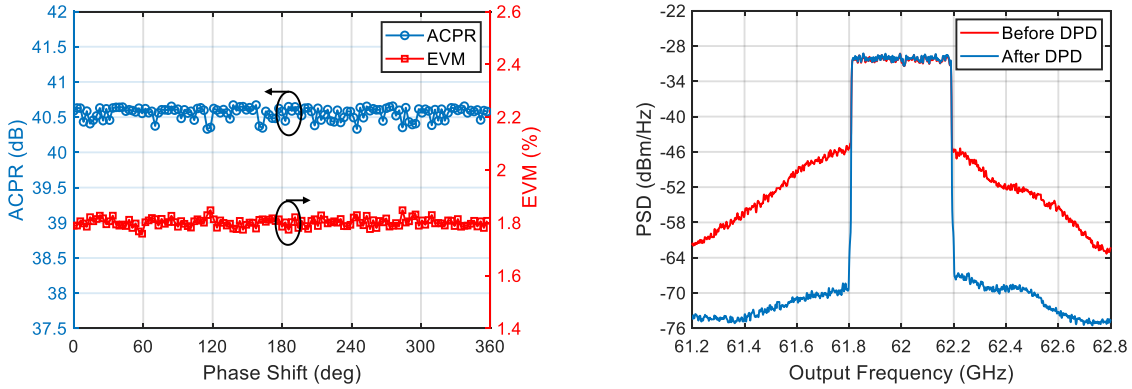
output phase resolution. The measured phase shifts are expressed as the angle of the polar plot while the CG and efficiency are represented by its magnitude shown in Figures 4.23b and 4.23c, respectively. We can see that the measured data shows a perfect match with the ideal phases. Thus, the designed PS enables the proposed frequency doubler-based RF beamforming front-end to have flexibility in choosing the optimal states based on the bit resolution imposed by the system requirement.

The fabricated frequency doubler-based RF beamforming front-end is tested under modulated signal stimuli where a 400 MHz OFDM signal with 256-QAM sub-carriers is used. An arbitrary waveform generator (Keysight M8190A) is used to generate the test signal which is up-converted to 31 GHz. Then, the signal is amplified using an external amplifier and routed through the PNA-X (N5242B) to the front-end input. The output of the front-end is then fed to the PNA-X port 2 to serve in the training of the DPD model. The linearization of the front-end is performed using the low-complexity DPD function



(a) (b) CG. (c) $\eta_{D,t}$.

Figure 4.23: (a) Measured absolute CG and efficiency error versus the phase error. (b)-(c) Measured RF performance of the front-end module across the measured phase shifts for 6-bit front-end's phase resolution at 62 GHz.



(a) (b)

Figure 4.24: (a) Measured ACPR and EVM versus the measured phase shift with DPD applied only on the optimal code words. (b) Power spectrum density before and after DPD for phase state zero (training state).

reported in [22] with a total of 51 coefficients. Instead of trying to linearize all the phase states, only the selected optimal code words are used for the PS control. Figure 4.24a shows the ACPR and EVM after DPD and across different phase settings; while Figure 4.24b shows the measured PSD before and after DPD at phase state zero (training state). These results highlight that the DPD performance, in terms of ACPR and EVM, is not affected by the variation in PS gain versus phase settings when a maximum of ±0.35 dB gain

variation is selected. Using DPD, the EVM and ACPR are maintained below 1.8% and 40.6 dB, respectively, across the whole phase shift range with less than 0.09% and 0.4 dB variation in their respective values. These results are achieved at an average $\eta_{D,t}$ of 3.6% and an average output power of -1.8 dBm.

4.7 Conclusion

This chapter started with investigating the design considerations of the PS in the context of frequency multiplier-based front-end. It then studied the different RTPS reflective load topologies to identify the optimum one that meets the pre-defined design constraints. Accordingly, a proof-of-concept prototype of RTPS is fabricated and validated experimentally. The measurement results showed the validity of the proposed DA-RTPS topology in attaining high gain and phase accuracy which is an important criterion in the design of a frequency multiplier-based front-end.

Subsequently, this chapter presented a compact high-efficiency mm-wave frequency doubler-based RF beamforming front-end module consisting of an 8-bit PS, driver amplifier, and frequency doubler. Due to the multiplying nature of the frequency doubler, the PS was specifically designed to allow for 180° phase tuning range and high gain and phase accuracy. The measurements showed the proposed frequency doubler-based front-end prototype achieved the full 360° phase tuning at the output with a gain and RMS phase accuracy of ±0.35 dB and 0.57°, respectively. The prototype showed also an average CG of 5.7 dB and a front-end efficiency of 16%. By applying DPD, the designed front-end generated 256-QAM OFDM vector modulated signals with an EVM of 1.8% and an average front-end efficiency of 3.6%. The promising performance of the presented V-based frequency doubler-based front-end lays the foundations for the development of front-ends targeting a 120 GHz band by cascading additional frequency doubling stage.

Chapter 5

D-Band Frequency Doubler With Enhanced RF Performance

5.1 Introduction

In this chapter, we are moving one step further in frequency by designing frequency doublers tailored for sub-THz frequency bands, specifically within the D-band range (110-170 GHz). This escalation in the operating frequency introduces distinct challenges to the design process. For instance, it is difficult to create an ideal short circuit impedance at these frequencies due to the inherent losses. Consequently, this chapter advances the analysis established in Chapter 3, proposing a novel design approach for push-push frequency doublers. It exploits more realistic design choices for the harmonic impedance, aiming to enhance RF performance metrics encompassing output power, power efficiency, and CG. Furthermore, this approach is employed to design frequency doublers targeting 120 GHz. The fabricated frequency doublers are then validated experimentally under CW and modulated signal stimuli. Figure 5.1 highlights the focus of this chapter.

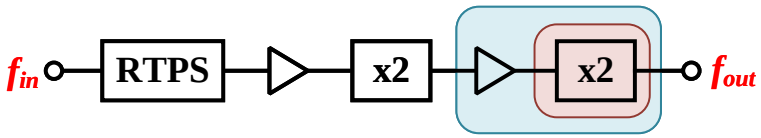


Figure 5.1: Proposed frequency multiplier-based RF beamforming front-end module, highlighting the focus of this chapter.

5.2 Proposed Design Approach

5.2.1 Problem Definition

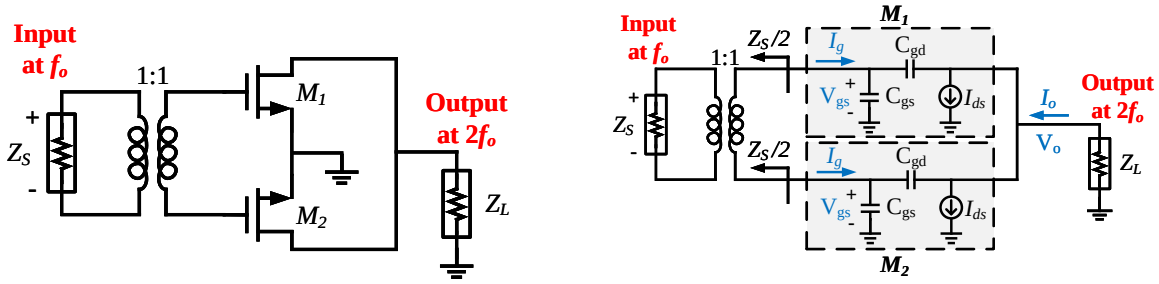
In push-push frequency doublers, the 2^{nd} harmonic output current flows back to the input due to Miller capacitance, C_{gd}, creating an in-phase 2^{nd} harmonic voltage swing at both gates of the push-push pair. These in-phase voltage swings re-shape the input voltage waveform, $v_{gs}(t)$. The re-shaping of $v_{gs}(t)$ cascades into an impact on the 2^{nd} harmonic output current, leading to a degradation in the frequency doubler's RF performance. Hence, the strategic choice of the 2^{nd} harmonic source impedance, $Z_{S,2}$, becomes pivotal, as it introduces a degree of freedom to refine the shape of $v_{gs}(t)$—an endeavor pivotal for advancing RF performance in terms of output power, power efficiency, and CG.

As mentioned in Section 2.4.1, literature has often endorsed the short-circuiting of $Z_{S,2}$ for frequencies below 100 GHz. This practice was predicated on the assumption that such a choice would nullify the influence of the 2^{nd} harmonic feedback current on the re-shaping of $v_{gs}(t)$. Though this choice led to improvements in output power, power efficiency, and CG in comparison to leaving $Z_{S,2}$ not designed for, it was not built on any theoretical derivations. Nevertheless, our analysis in Section 3.2.2 has proven that short-circuiting $Z_{S,2}$ is one of the solutions that improves the AM-PM characteristics of the push-push frequency doubler. However, as we move to sub-THz frequency bands (above 100 GHz), the practical realization of a short-circuited $Z_{S,2}$ becomes arduous due to the extremely high losses inherent to these frequency bands. Hence, most of the existing literature tends to not design for it.

Therefore, we will propose a design approach aiming to eliminate the reliance on the $Z_{S,2}$ short. In the following formulation, our target is to exploit the optimum choice of $Z_{S,2}$ that will help in shaping $v_{gs}(t)$ waveform, taking into account the effect of the feedback current due to Miller capacitance, in a way that improves the 2^{nd} harmonic output current and ultimately enhances the RF performance in terms of output power, power efficiency, and CG.

5.2.2 Proposed Theory

In the following analysis, we will employ the push-push topology for the frequency doubler. Our approach is to investigate how the re-shaping of the input voltage waveform due to the 2^{nd} harmonic feedback current impacts the RF performance. To achieve this, we will formulate the 2^{nd} harmonic output current, $I_o(2\omega_o)$. Subsequently, we will explore



(a) (b)

Figure 5.2: (a) Schematic and (b) simplified small-signal model of the push-push core where C_{gs}, C_{gd}, and C_{ds} designate the transistor parasitic capacitances with C_{ds} absorbed in the load impedance.

the optimal choice of $Z_{S,2}$ (or the 2^{nd} harmonic source admittance, $Y_{S,2}$) that maximizes $I_o(2\omega_o)$. The following steps outline the theoretical formulation we will follow:

1. Define $I_o(2\omega_o)$ as function of $V_{gs}(\omega_o)$ and $V_{gs}(2\omega_o)$.
2. Determine $V_{gs}(2\omega_o)$ in terms of $Y_{S,2}$.
3. Substitute by $V_{gs}(2\omega_o)$, given in Step 2, back in $I_o(2\omega_o)$.
4. Identify the optimum choice of $Y_{S,2}$ that maximizes $I_o(2\omega_o)$.

Note, $V_{gs}(\omega_o)$ and $V_{gs}(2\omega_o)$ designate the fundamental and the 2^{nd} harmonic phasors of the gate voltage.

Step 1

Figure 5.2 depicts the schematic and small-signal model of the push-push core. The drain current of each transistor, $i_{ds}(t)$, can be expressed as a function of the input gate voltage, $v_{gs}(t)$, as follows,

$$i_{ds}(t) = g_{m,1}v_{gs}(t) + g_{m,2}v_{gs}^2(t) + ..., \tag{5.1}$$

where $g_{m,n}$ designate the transistor transconductance at the n^{th} harmonic. Notably, the push-push core is biased in a Class-C bias with a conduction angle of 126°, which maximizes the 2^{nd} harmonic output current. Hence, $g_{m,2}$ has the primary impact on $i_{ds}(t)$. Additionally, as mentioned earlier, the feedback current will create a 2^{nd} harmonic input

voltage swing. This 2^{nd} harmonic voltage swing will get amplified through the transistor $g_{m,1}$ affecting $i_{ds}(t)$. Consequently, we will consider the effect of $g_{m,1}$ in our analysis. Higher-order harmonics of g_m are significantly lower than $g_{m,1}$ and $g_{m,2}$ so that they will have negligible impact on $i_{ds}(t)$.

Assuming that $v_{gs}(t)$ has only components at the fundamental and the 2^{nd} harmonic given by $V_{gs}(\omega_o)$ and $V_{gs}(2\omega_o)$, respectively, the 2^{nd} harmonic drain current, $I_{ds}(2\omega_o)$, can be written in the phasor form as,

$$I_{ds}(2\omega_o) = g_{m,1}V_{gs}(2\omega_o) + g_{m,2}V_{gs}^2(\omega_o). \tag{5.2}$$

Using (5.2), the 2^{nd} harmonic output current of the push-push core can be expressed in the phasor form as,

$$I_o(2\omega_o) = 2I_{ds}(2\omega_o) = 2g_{m,1}V_{gs}(2\omega_o) + 2g_{m,2}V_{gs}^2(\omega_o). \tag{5.3}$$

Note, (5.3) shows that $g_{m,1}$ amplifies the 2^{nd} harmonic component of the input gate voltage which in turn affects the output current of the push-push core. According to (5.3), it is defined by the ratio of the output current and the input gate voltage at the 2^{nd} harmonic and can be expressed as,

$$g_{m,1} = \left.\frac{I_{ds}(2\omega_o)}{V_{gs}(2\omega_o)}\right|_{V_{gs}(\omega_o)=0}. \tag{5.4}$$

While the transistor $g_{m,2}$ can be found using (5.3) by,

$$g_{m,2} = \left.\frac{I_{ds}(2\omega_o)}{V_{gs}^2(\omega_o)}\right|_{V_{gs}(2\omega_o)=0}. \tag{5.5}$$

Moreover, using (5.3), the 2^{nd} harmonic output voltage phasor of the push-push core, $V_o(2\omega_o)$, can be written as,

$$V_o(2\omega_o) = -Z_{L,2}I_o(2\omega_o) = -2g_{m,1}Z_{L,2}V_{gs}(2\omega_o) - 2g_{m,2}Z_{L,2}V_{gs}^2(\omega_o). \tag{5.6}$$

where $Z_{L,2}$ denotes the 2^{nd} harmonic load impedance seen by the push-push core.

Step 2

To proceed, we need to derive a closed form for $V_{gs}(2\omega_o)$ to fully define $I_o(2\omega_o)$ in (5.3). We will start by expressing the input gate current, $i_g(t)$, as a function of the transistor parasitic capacitances, C_{gd} and C_{gs}. Based on Figure 5.2b, $i_g(t)$ can be expressed as,

$$i_g(t) = C_{gd}\frac{d\big(v_{gs}(t) - v_o(t)\big)}{dt} + C_{gs}\frac{d\big(v_{gs}(t)\big)}{dt}. \tag{5.7}$$

Hence, (5.7) can be re-written in the phasor form at the 2^{nd} harmonic as follows,

$$I_g(2\omega_o) = j2\omega_o C_{gd}\big[V_{gs}(2\omega_o) - V_o(2\omega_o)\big] + j2\omega_o C_{gs} V_{gs}(2\omega_o). \tag{5.8}$$

By substituting (5.6) in (5.8) and re-arranging the terms, $I_g(2\omega_o)$ can be given by,

$$I_g(2\omega_o) = V_{gs}(2\omega_o)\Big[j2\omega_o C_g + j2\omega_o C_{gd} 2g_{m,1} Z_{L,2}\Big] + V_{gs}^2(\omega_o)\Big[j2\omega_o C_{gd} 2g_{m,2} Z_{L,2}\Big] \tag{5.9}$$

where $C_g = C_{gd} + C_{gs}$.

Moreover, $I_g(2\omega_o)$ can be written in terms of the 2^{nd} harmonic source admittance, $Y_{S,2}$, using the following equation,

$$I_g(2\omega_o) = -2Y_{S,2} V_{gs}(2\omega_o). \tag{5.10}$$

By equating (5.9) and (5.10) and solving for $V_{gs}(2\omega_o)$, a closed form for the gate voltage phasor at the 2^{nd} harmonis can be defined by,

$$V_{gs}(2\omega_o) = \frac{-V_{gs}^2(\omega_o)\big[j2\omega_o C_{gd} 2g_{m,2} Z_L(2\omega_o)\big]}{2Y_s(2\omega_o) + j2\omega_o C_g + j2\omega_o C_{gd} 2g_{m,1} Z_L(2\omega_o)}. \tag{5.11}$$

Step 3

By substituting $V_{gs}(2\omega_o)$ back into (5.3), the push-push core's output current at the 2^{nd} harmonic can be fully defined by,

$$\begin{aligned} I_o(2\omega_o) &= 2g_{m,2} V_{gs}^2(\omega_o) + 2g_{m,1} \frac{-V_{gs}^2(\omega_o)\big[j2\omega_o C_{gd} 2g_{m,2} Z_{L,2}\big]}{2Y_{S,2} + j2\omega_o C_g + j2\omega_o C_{gd} 2g_{m,1} Z_{L,2}} \\ &= 2g_{m,2} V_{gs}^2(\omega_o)\left[1 + \frac{X}{Y}\right] \end{aligned} \tag{5.12}$$

where

$$X = -j2\omega_o C_{gd} 2g_{m,1} Z_{L,2} \tag{5.13}$$

$$Y = 2Y_{S,2} + j2\omega_o C_g + j2\omega_o C_{gd} 2g_{m,1} Z_{L,2}. \tag{5.14}$$

Equation (5.12) shows that $I_o(2\omega_o)$ comprises two components. The first component arises from the extraction of the 2^{nd} harmonic component of the transistor $g_{m,2}$ (i.e., due to the Class-C bias of the frequency doubler with a conduction angle of 126°). The second component stems from the effect of the feedback current, which flows back to the input through Miller capacitance and then gets amplified at the output by the transistor $g_{m,1}$.

Furthermore, the second component is a function of $Y_{S,2}$, providing a degree of freedom to optimize it so as to maximize $I_o(2\omega_o)$ and consequently improve the output power, power efficiency, and CG of the push-push core.

Step 4

In this step, our target is to exploit the optimum choice of $Y_{S,2}$ that maximizes the 2^{nd} harmonic output current of the push-push core. Based on (5.12), one solution is to short circuit the 2^{nd} harmonic source impedance (i.e., $Y_{S,2} = \infty$) which makes the second current component in (5.12) equals to zero. This solution eliminates the effect of the feedback current on the distortion of the input gate voltage and consequently improves $I_o(2\omega_o)$. However, the practical realization of a short circuit impedance at sub-THz frequency bands is significantly challenging due to the substantial losses at these frequency bands. Hence, we are investigating an alternate solution for $Y_{S,2}$ that is practically realizable.

To maximize $I_o(2\omega_o)$ in (5.12), two conditions need to be satisfied: (i) choose $Y_{S,2}$ such that the second component in (5.12), given by X/Y, is maximized, (ii) ensure that the two current components are in-phase to guarantee their constructive addition. We will explore these two conditions in the following.

For the first condition, to maximize X/Y, we need to minimize the denominator Y. Let the real and imaginary parts of $Y_{S,2}$, $Z_{L,2}$, and $g_{m,1}$ be defined as follows,

$$\begin{aligned} Y_{S,2} &= G_{S,2} + jB_{S,2} \\ Z_{L,2} &= R_{L,2} + jX_{L,2} \\ g_{m,1} &= g_{m,1r} + jg_{m,1i}, \end{aligned} \tag{5.15}$$

using (5.14), the real and imaginary parts of Y can be separated and equated to zero. Hence, one can solve for the optimum solution of $G_{S,2}$ and $B_{S,2}$ which can be found by,

$$G_{S,2} = 2\omega_o C_{gd}\big(g_{m,1r}X_{L,2} + g_{m,1i}R_{L,2}\big) \tag{5.16}$$

$$B_{S,2} = -\omega_o C_g - 2\omega_o C_{gd}\big(g_{m,1r}R_{L,2} - g_{m,1i}X_{L,2}\big). \tag{5.17}$$

Thus, (5.16) and (5.17) define the optimum choice of the real and imaginary parts of $Y_{S,2}$ that minimizes the denominator Y and in turn maximizes the second component of $I_o(2\omega_o)$.

For the second condition, to ensure that the two components of $I_o(2\omega_o)$ add constructively, the following condition needs to be satisfied:

$$\big|0 - \angle X\big| < 90^\circ \tag{5.18}$$

assuming that $X >> Y$. This can be explained by the fact that $I_o(2\omega_o)$ in (5.12) has two phasors. The first one has a phase of zero (i.e., $\angle 1 = 0$) while the second one has a phase of $\angle X$. The degree of phase alignment between these two phasors directly determines the amount of current improvement. For instance, if $\angle X = 0$ (i.e., completely aligns with the first phasor), this will result in the maximum achievable improvement in $I_o(2\omega_o)$.

Using (5.13), $\angle X$ can be found by

$$\angle X = \angle\big(-j2\omega_o C_{gd} 2g_{m,1} Z_{L,2}\big) = -90^\circ + \angle g_{m,1} + \angle Z_{L,2} \tag{5.19}$$

By substituting (5.19) in (5.18), the condition in (5.18) can be re-written as,

$$\big|90^\circ - \angle g_{m,1} - \angle Z_{L,2}\big| < 90^\circ \tag{5.20}$$

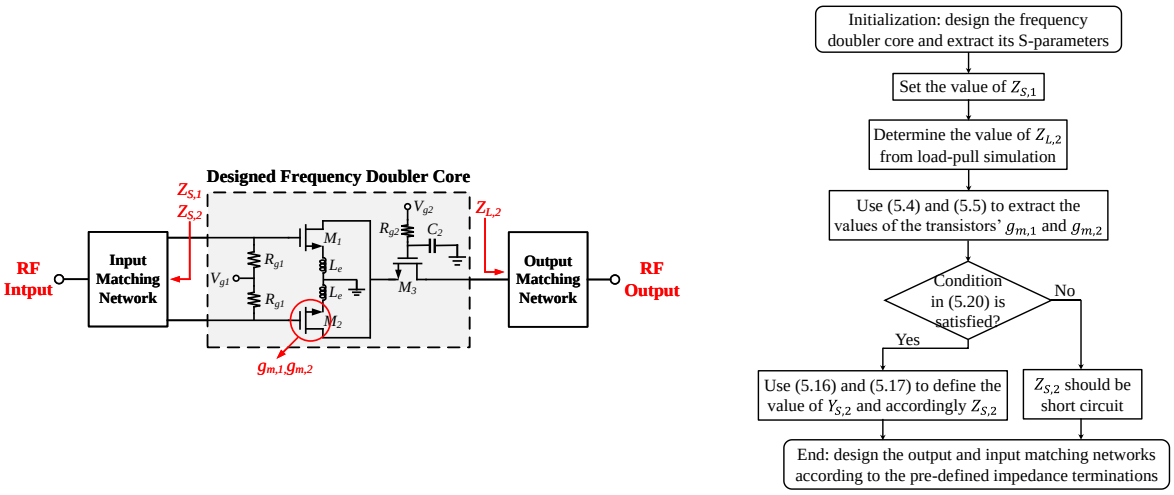
The above condition guarantees that the two components of $I_o(2\omega_o)$ are in-phase, allowing for their constructive addition and consequently improving the total output current of the push-push core. Note, $Z_{L,2}$ is determined based on load-pull simulation for maximizing the power efficiency; hence, its phase is pre-defined. If the condition in (5.20) is not satisfied, one can choose to minimize the second component of $I_o(2\omega_o)$ by designing $Y_{S,2}$ to be an open circuit.

In conclusion, the proposed approach involves determining the optimum choice of the 2^{nd} harmonic source impedance, taking into account the effect of the 2^{nd} harmonic feedback current, to maximize $I_o(2\omega_o)$. Subsequently, the condition in (5.20) is defined to guarantee the constructive addition of the two components of the output current. Accordingly, one can optimize the push-push topology for a maximum 2^{nd} harmonic output current, which enhances the performance of the frequency doubler in terms of output power, power efficiency, and CG. Simulation results that validate the proposed approach will be further discussed in Section 5.3.2.

5.3 Implementation of 120-GHz Frequency Doubler

The previous section presented a novel design approach that determines the optimum choice of the 2^{nd} harmonic source impedance. In this section, we will proceed with designing a frequency doubler based on the proposed approach. As a proof-of-concept demonstration, the frequency doubler is implemented in GlobalFoundries' 45-nm SOI-CMOS process targeting an output frequency of 120 GHz.

Figure 5.3 shows the schematic and procedure used to implement the proposed approach on the frequency doubler design. According to Figure 5.3, initially, the frequency doubler



(a) (b)

Figure 5.3: Implementation of the proposed design approach: (a) schematic of the designed frequency doubler core, and (b) design procedure.

core must be properly designed. This is described in Section 5.3.1. Then, the choice of the harmonic impedance terminations based on the proposed design approach is illustrated in Section 5.3.2. Finally, Section 5.3.3 includes the full implementation of the matching networks along with the post-layout simulation results of the designed frequency doubler.

5.3.1 Frequency Doubler Core

Figure 5.3a depicts the schematic of the frequency doubler core which utilizes a stacked push-push configuration. As discussed earlier in Chapter 3, the common drain connection in the push-push configuration constructively combines the 2^{nd} harmonic current at the output. Also, the use of the stacked transistor, M_3, maximizes the voltage swing and consequently improves the output power. The sizes of M_1 and M_2 are chosen equal to 60 μm each and the size of M_3 is set to 120 μm. Additionally, M_1 and M_2 are biased in a Class-C mode with $V_{g1} = -0.2V$. The gate bias, V_{g2}, and the capacitor, C_2, are determined to ensure equal voltage division among the stacked transistors. Furthermore, a small degeneration source inductor, L_e, is employed to increase the real part of the input impedance, thereby reducing the input matching network complexity and losses.

As recommended by the foundry, the nominal supply voltage of the NMOS transistor, $V_{dd,n}$, in the 45-nm SOI-CMOS process is 1 V. Nevertheless, a slightly over-driven $V_{dd,n}$ has

been reported in the literature [108, 109] to enhance the RF performance of the transistor with no reliability issue. As we are operating at an output frequency of 120 GHz, the transistor operates closer to its f_{max} and suffers from reduced RF performance compared to operating at a lower frequency. Hence, in this design, we opt for choosing the supply voltage of each transistor to be 1.1 V to achieve higher output power and power efficiency. Accordingly, the supply voltage of the stacked push-push core, V_{dd}, is selected by 2.2 V.

5.3.2 Choice of Second Harmonic Source Impedance

Building upon the frequency doubler core design detailed in Section 5.3.1, the proposed design approach outlined in Figure 5.3b will be implemented to determine the required harmonic impedance terminations. Initially, the layout of the frequency doubler core is simulated using Keysight Momentum (EM) simulator to extract its S-parameters. Then, the obtained S-parameter file is imported into Keysight ADS to proceed with the design procedure. While presenting a conjugate match at the fundamental input impedance of the frequency doubler core, an extensive load-pull simulation is carried out to determine the 2^{nd} harmonic load impedance, $Z_{L,2}$, that maximizes the power efficiency. Based on the load-pull simulation results, the value of $Z_{L,2}$ is found by

$$Z_{L,2} = 6 - j10 = 11.6\angle -59^{\circ}. \tag{5.21}$$

Next, the transistor transconductance $g_{m,1}$ needs to be defined. As discussed earlier, $g_{m,1}$ plays a pivotal role in amplifying the 2^{nd} harmonic input common-mode signal, that originates from the feedback current leaking from the output through the Miller capacitance. To properly extract $g_{m,1}$, a common-mode input signal is applied to the frequency doubler core at the 2^{nd} harmonic frequency (i.e., at 120 GHz). Hence, the value of $g_{m,1}$ is calculated using (5.4) and is found by

$$g_{m,1} = (-5.6 + j1.5) * 10^{-3} = 5.8m\angle 165^{\circ}. \tag{5.22}$$

Subsequently, in accordance with the design procedure depicted in Figure 5.3b, the extracted values of $Z_{L,2}$ and $g_{m,1}$ are employed to verify the validity of the condition delineated in (5.20). Using (5.21) and (5.22), the condition in (5.20) is calculated by,

$$\left|90^{\circ} - \angle g_{m,1} - \angle Z_{L,2}\right| = \left|90^{\circ} - 165^{\circ} - (-59^{\circ})\right| = 16^{\circ} < 90^{\circ} \tag{5.23}$$

Equation (5.23) shows that the condition in (5.20) is satisfied. Hence, the two components of the output current, given in (5.12), will combine constructively.

Upon satisfiying the above condition, the 2^{nd} harmonic source admittance, $Y_{S,2}$, is chosen to maximize the second component of $I_o(2\omega_o)$ as discussed in Section 5.2.2. Equations (5.16) and (5.17) are employed to evaluate the real and imaginary parts of $Y_{S,2}$. Accordingly, $Y_{S,2}$ is determined by $0.93m - j17m$ and $Z_{S,2}$ is given by $3.2 + j59$. It is important to note that the real part of $Z_{S,2}$ (i.e., 3.2) is relatively small and might be difficult to realize practically due to the inherent high losses at high frequencies. As such, efforts will be made to minimize the real part while designing the imaginary part of $Z_{S,2}$ to closely align with the calculated value.

5.3.3 Matching Networks Design

Based on the design procedure outlined in Figure 5.3b, after defining the required harmonic impedance terminations of the frequency doubler core, we will proceed with the implementation of the matching networks. Figure 5.4 shows the complete schematic of the designed stacked push-push frequency doubler.

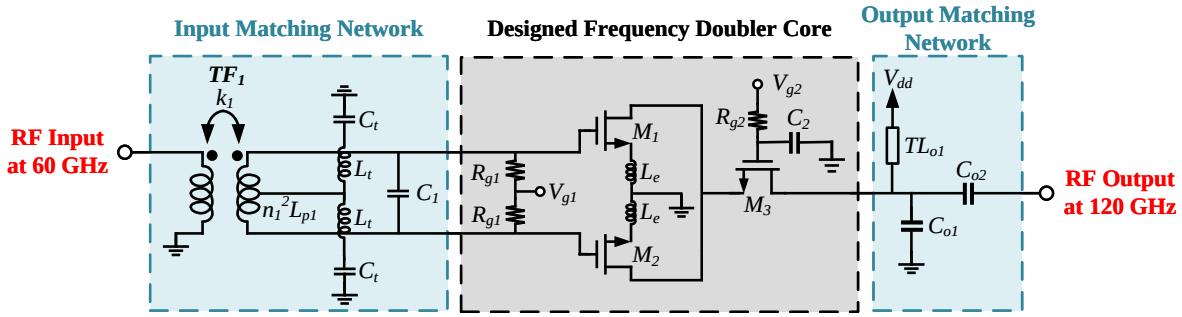
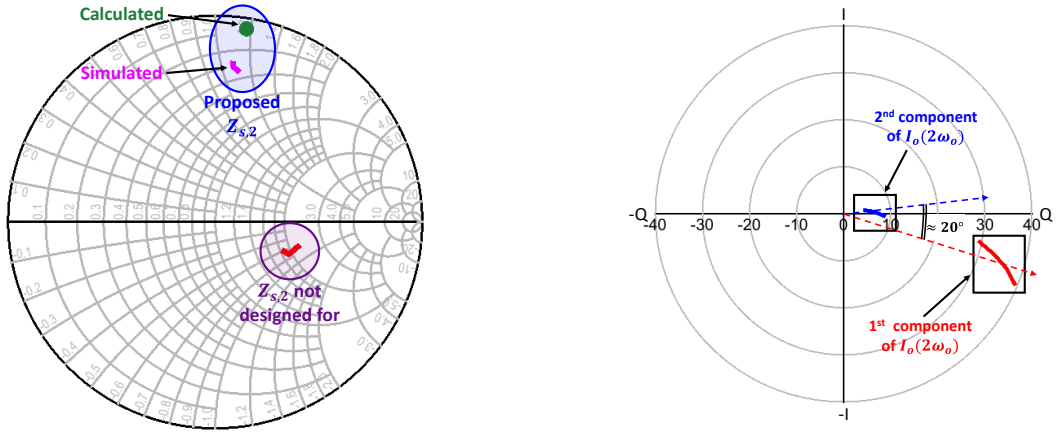


Figure 5.4: Complete schematic of the designed frequency doubler.

As we are operating at frequencies above 100 GHz, the length of the TL is relatively short, occupying less area. Hence, in this design, a TL-based output matching network is implemented. As shown in Figure 5.4, it is comprised of a CPW TL (TL_{o1}) and capacitors (C_{o1} and C_{o2}), together they achieve an impedance transformation from $Z_{L,2}$ given in (5.21) to a 50-Ω output termination. At such high operating frequency, the frequency doubler design is significantly sensitive to the components' parasitics. Hence, after multiple iterations of re-tuning of the output matching network, the characteristic impedance and electrical length of the CPW TL are found to be 58 Ω and 40°, respectively. While C_{o1} and C_{o2} are set to 34 fF and 180 fF, respectively.

Moving on to the input matching network, a step-by-step design is followed to validate the design choice of $Y_{S,2}$ specified in Section 5.3.2. Initially, at the fundamental



(a) (b)

Figure 5.5: (a) The proposed 2^{nd} harmonic source impedance, $Z_{S,2}$, compared to its value when left not designed for. (b) Graphical representation of the two components of the frequency doubler's output current at the 2^{nd} harmonic.

frequency f_o, the input matching network is designed to match the frequency doubler's input impedance, $Z_{in,1}$, to a 50-Ω input termination. Note, $Z_{in,1}$ is selected such that a conjugate match is maintained to maximize the input power transfer. Hence, to achieve such impedance transformation at f_o, a single-to-differential transformer (TF_1) followed by a capacitor (C_1) connected in parallel to TF_1 secondary coil is utilized as shown in Figure 5.4. The value of C_1 is deduced by 35 fF and the primary inductance (L_{P1}), coupling factor (k_1), and turn ratio (n_1) of TF_1 are determined to be 333.6 pH, 0.58, and 0.7, respectively. It is important to note that the designed input matching network that achieves the required matching at the fundamental input frequency presents an impedance at the 2^{nd} harmonic which needs to be considered.

Next, the optimum $Z_{S,2}$ calculated in Section 5.3.2 is utilized to investigate the effectiveness of the theory outlined in Section 5.2.2. We will start with an ideal implementation of the 2^{nd} harmonic source termination which is done by controlling the center-tap of TF_1 secondary coil using ideal L and C components. Figure 5.5a depicts the calculated and simulated values of the optimum $Z_{S,2}$. Note, the simulated value experiences a slightly higher real part compared to the calculated one due to the loss of TF_1 at the 2^{nd} harmonic. Figure 5.5b shows graphically the two components of the frequency doubler's output current, defined in (5.12), extracted from simulation. Figure 5.5b confirms that the second component that originated from the 2^{nd} harmonic feedback current adds in-phase with the

Table 5.1: Numerical values of the frequency doubler output current components (in mA).

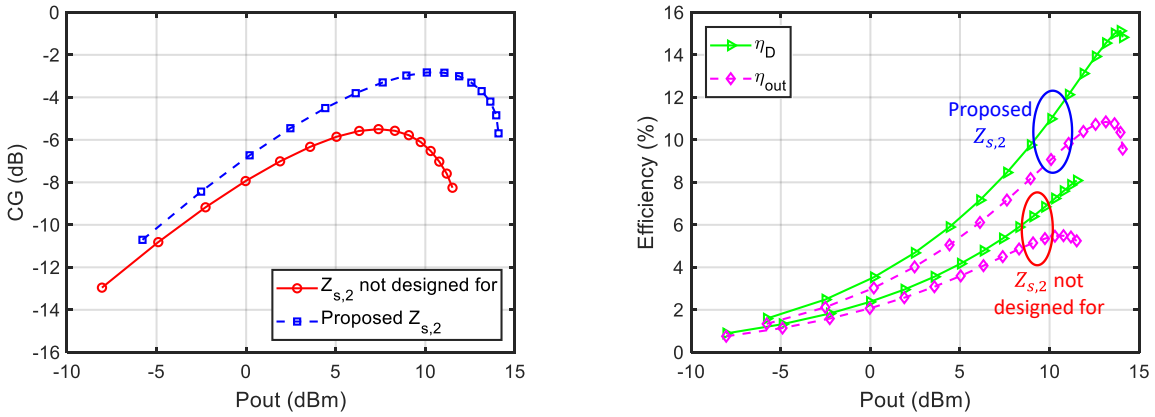
P_{in}	$2g_{m,2}V_{gs}^2(\omega_o)$	$(X/Y)*2g_{m,2}V_{gs}^2(\omega_o)$	$I_o(2\omega_o)$
11	$25.8\angle-8.3$	$3.7\angle13.1$	$29.2\angle-5.7$
12	$29.5\angle-11.7$	$4.6\angle9.2$	$33.9\angle-8.9$
13	$33.1\angle-15.1$	$5.8\angle5.3$	$38.6\angle-12.1$
14	$36.4\angle-18.5$	$7.2\angle1.5$	$43.2\angle-15.3$
15	$39.2\angle-22.3$	$8.6\angle-2.9$	$47.4\angle-18.8$

first component of $I_o(2\omega_o)$ which is due to the deep Class-C bias of the frequency doubler. Also, the angle between them is around 20° which is close to the value calculated in (5.23). Table 5.1 presents their numerical values along with the frequency doubler's total output current. It shows that the added second component of the current improves the total output current by around 14%-21% compared to having only the original first component of the frequency doubler's current (i.e., $2g_{m,2}V_{gs}^2(\omega_o)$).

Figure 5.6 shows the simulated RF performance of the frequency doubler using the proposed $Z_{S,2}$ in comparison with leaving $Z_{S,2}$ not designed for. Note, TF_1 presents an impedance at the 2^{nd} harmonic with its value depicted in Figure 5.5a and given by $89-j28$. This reflects the $Z_{S,2}$ value when not specifically designing for it. According to Figure 5.6, the proposed $Z_{S,2}$ termination improves the CG, η_D, and η_{out} of the frequency doubler by 2.7 dB, 7%, and 5.8%, respectively, compared to leaving $Z_{S,2}$ not designed for. Note, η_D is the drain efficiency while η_{out} is DC-RF efficiency given by $P_{out}/(P_{in}+P_{dc})$.

Subsequently, the targeted 2^{nd} harmonic source impedance termination is implemented using a similar technique used for the frequency doubler design in Chapter 3 where L_t and C_t are connected in a balanced structure to the center-tap of TF_1 secondary coil, as shown in Figure 5.4. The values of L_t and C_t are found by 26.8 pH and 13 fF, respectively. Then, the complete frequency doubler design, depicted in Figure 5.4, is EM-simulated. Figure 5.7 shows the post-layout simulation of the proposed frequency doubler. It highlights an achieved peak CG of -3.6 dB, a peak η_D of 12.7%, and a peak η_{out} of 8.9%. Also, a saturated output power of 13.2 dBm is obtained. Through EM simulation, the 2^{nd} harmonic impedance seen at the frequency doubler input is found by $42+j78$ where the real part is significantly high due to the inherent high losses at 120 GHz.

As mentioned earlier, an ideal $Z_{S,2}$ short is another solution that cancels the effect of the 2^{nd} harmonic feedback current on the distortion of the input signal and consequently improves the output current. However, the practical realization of an ideal $Z_{S,2}$ short (i.e., $0+j0$) is significantly difficult at an operating frequency of 120 GHz due to the extremely



(a) (b)

Figure 5.6: Simulated comparison of frequency doubler's CG and efficiency using the proposed $Z_{S,2}$ and with leaving $Z_{S,2}$ not designed for.

high losses. Our proposed design suffered from a high real part of $Z_{S,2}$ (i.e., $R_{S,2} = 42$) due to such high losses. Assuming that one can achieve a loss of 42 Ω at 120 GHz, we wanted to compare our designed $Z_{S,2}$ with a scenario where we have a non-ideal $Z_{S,2}$ short having similar loss (i.e., $42 + j0$). Figure 5.8a depicts graphically the designed $Z_{S,2}$ and $Z_{S,2}$ of such simulated scenario. Figures 5.8b and 5.8c show the simulated peak CG and η_D for these two solutions of $Z_{S,2}$. They highlight that our proposed solution achieves improved output power, CG, and η_D compared to a $Z_{S,2}$ short that can practically realized at the targeted operating frequency. Hence, the introduction of the $Z_{S,2}$ imaginary part in our proposed solution plays a crucial role in shaping the waveform so as to maintain the RF performance and also eliminates the need for a non-practical $Z_{S,2}$ short solution.

5.4 Pre-Driver Amplifier Design

The previous section proposed a frequency doubler design targeting an output frequency of 120 GHz. However, the design has a low CG. Hence, a pre-driver amplifier is utilized in cascade with the proposed frequency doubler to improve the overall CG and lower the input power-level requirement. Since the amplifier is located before the frequency doubler, it will operate at a lower center frequency of 60 GHz, allowing for high-gain actives and low-loss passives.

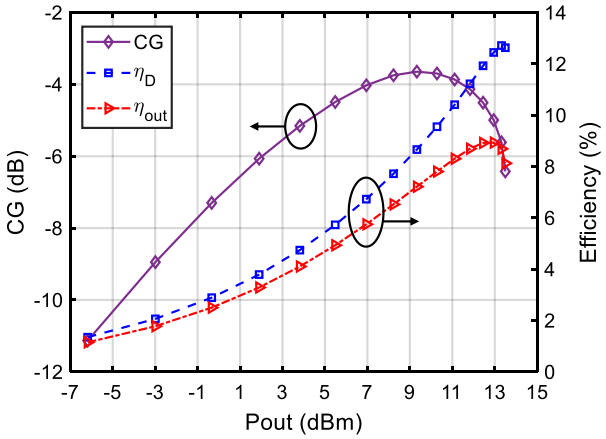
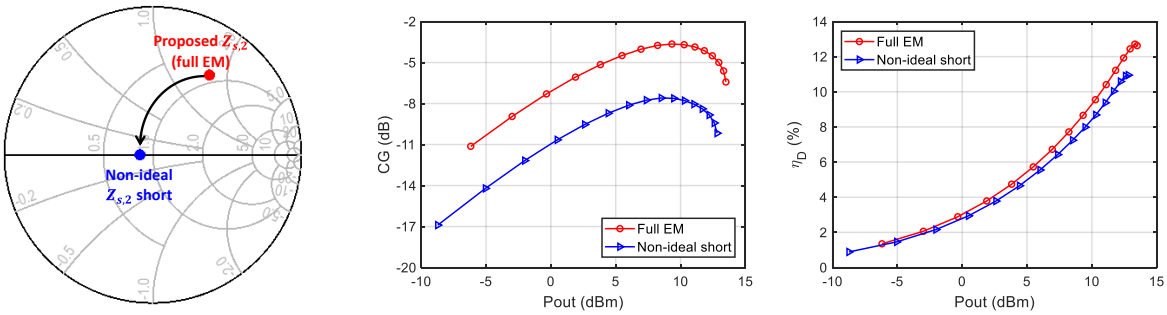


Figure 5.7: Post-layout simulation results of the proposed frequency doubler at 120 GHz output frequency.

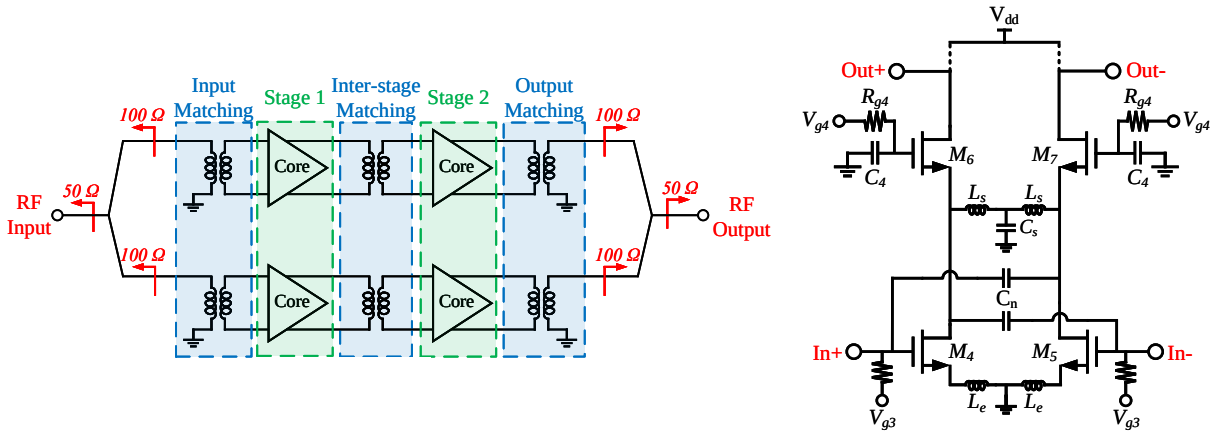
5.4.1 Block Diagram

The required input power of the designed frequency doubler is 17 dBm at 60 GHz. To realize such high output power, the pre-driver amplifier depicted in Figure 5.9a is utilized. It is implemented using a two-way structure with each way consisting of a two-stage amplifier design. The use of the two-way structure boosts the output power by 3 dBm compared to a single-way one. The two-stage design enhances the total gain of the pre-driver amplifier. Moreover, a simple current combiner/splitter is used at the output/input of the amplifier.



(a) $Z_{S,2}$ value. (b) Conversion gain. (c) Drain efficiency.

Figure 5.8: Simulated comparison between the proposed $Z_{S,2}$ and a non-ideal $Z_{S,2}$ short.



(a) (b)

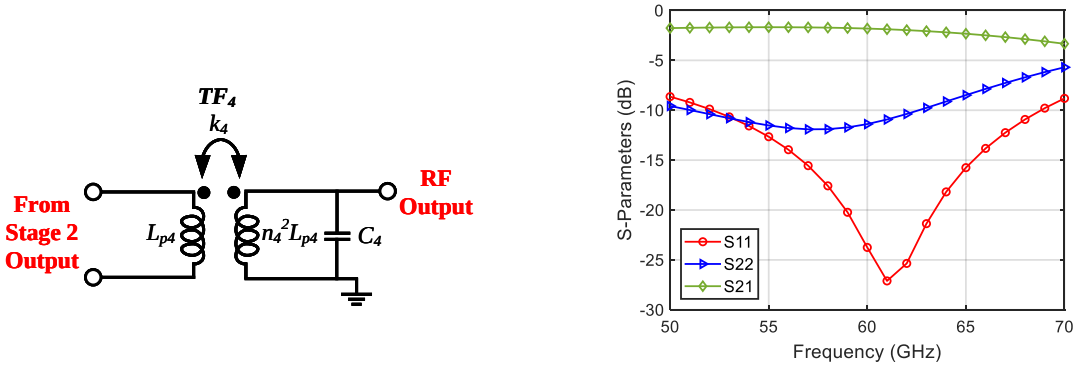
Figure 5.9: (a) Block diagram of the pre-driver amplifier design. (b) Schematic of the amplifier stages' core.

5.4.2 Implementation

As shown in Figure 5.9b, the amplifier core active circuit is realized using a stacked topology to enhance the output power. The number of transistors per stack and the transistors' width are set to two and 180 μm, respectively. An inter-stack matching comprised of L_s and C_s is added to ensure proper voltage division between the two stacked transistors. Moreover, a neutralization capacitor, C_n, is utilized to compensate for the transistor C_{gd}. A degeneration inductor, L_{e1}, is utilized to increase the real part of the input impedance which reduces the pressure on the input matching network design.

Since the required output power from each stage of the amplifier is different, the two stages are biased in a different class of operation. The first stage is designed to provide enough gain to lower the input power-level requirements. Hence, it is biased in a Class-A with a gate voltage, V_{g1}^{s1}, set to 0.42 V. The second stage of the amplifier is required to deliver adequate output power to feed the frequency doubler input. Accordingly, a Class-AB bias is used with a gate voltage, V_{g1}^{s2}, of 0.3 V. The supply voltages of stage 1 and stage 2 are selected to be 2.2 V and 2.4 V, respectively.

Based on load-pull simulation, the optimal load impedance of the amplifier stage 2, Z_L^{s2}, in each way is found by $18 + j28$. The output matching network is then designed to match Z_L^{s2} to a 100-Ω termination. Figure 5.10a shows the circuit model of the designed output matching network where a differential-to-single transformer (TF_4) is utilized with



(a) Circuit model.

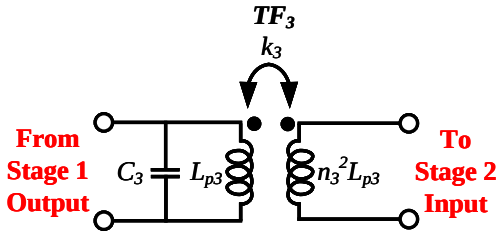
(b) Simulated S-parameters.

Figure 5.10: Designed output matching network.

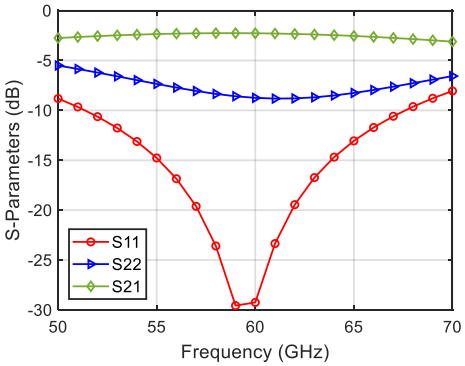
a capacitor connected in parallel to TF_4 secondary coil. The transformer is implemented using a stacked topology where the primary coil is overlaid on the secondary coil. To achieve the targeted impedance transformation, the value of the parallel capacitor is set to 45 fF, while the primary inductance (L_{p4}), coupling factor (k_4), and turn ratio (n_4) of TF_4 are found by 715 pH, 0.85, and 1.06, respectively. Figure 5.10b shows the simulated S-paratmeters of the output network layout structure, revealing an IL of -1.8 dB with good input and output return loss around the targeted 60-GHz band. After designing the output matching network, the outputs of each way of the amplifier are directly connected to combine the output currents and present a 50-Ω output termination.

Next, an inter-stage matching network is utilized to match the two stages of the amplifier. While presenting a conjugate match at the input of stage 2, inter-stage load-pull simulation was performed to determine the optimum load impedance of the amplifier stage 1 that maximizes the output power. Accordingly, as depicted in Figure 5.11a, a differential-to-differential transformer (TF_3) and a capacitor connected in parallel to TF_3 primary coil are utilized to implement the inter-stage matching network. The extracted parameters of TF_3 primary inductance (L_{p3}), coupling factor (k_3), and turn ratio (n_3) are deduced by 194 pH, 0.64, and 0.87, respectively. While C_3 is found by 25 fF. The designed inter-stage network structure achieves an IL of -2.2 dB at an operating frequency of 60 GHz as shown in Figure 5.11b.

Finally, by leveraging a conjugate match at the fundamental input impedance of the amplifier stage 1, an input matching network is designed to match such impedance to a 100-Ω termination at the input of each way of the amplifier. As depicted in Figure 5.12a, it is implemented using a single-to-differential (TF_2) and two capacitors connected in parallel

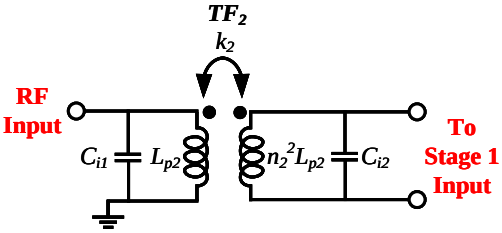


(a) Circuit model.

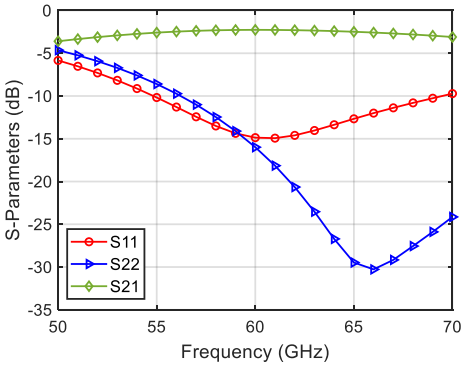


(b) Simulated S-parameters.

Figure 5.11: Designed interstage matching network.



(a) Circuit model.



(b) Simulated S-parameters.

Figure 5.12: Designed input matching network.

to TF_2 primary and secondary coils. Figure 5.12b shows the S-paratmeters of the EM-simulated input matching network, achieving an IL of -2.3 dB at a 60-GHz operating frequency with a return loss below -10 dB from 55 GHz to 69 GHz. Subsequently, the inputs of the two-way amplifier are connected together so that the amplifier is ultimately matched to a 50-Ω input termination. Figure 5.13 summarizes the complete schematic of the designed pre-driver amplifier. Note, the amplifier active core is depicted in Figure 5.9b.

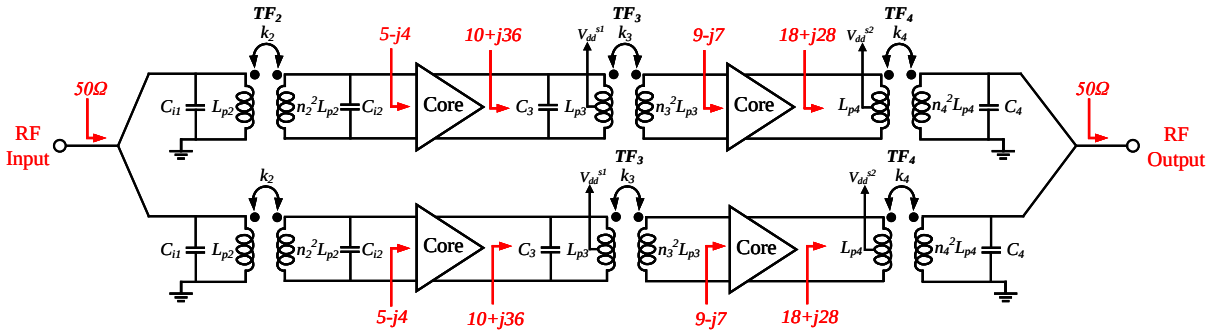


Figure 5.13: Complete schematic of the 60-GHz pre-driver amplifier.

5.4.3 Co-Simulation with The Proposed Frequency Doubler

Since the pre-driver amplifier is designed to present a 50-Ω output termination, it is directly connected to the proposed frequency doubler input which is also matched to a 50 Ω. Initially, to assess the performance of the amplifier, its different blocks (including stage 1 core, stage 2 core, input matching, etc.) are EM-simulated and then their S-Parameter files are connected to the frequency doubler using Keysight ADS. This allows us to investigate the gain and power levels at different nodes in the amplifier-doubler design to make sure that the expected levels are achieved at each node.

Accordingly, Figure 5.14 shows the EM-simulated gain of the amplifier's stage 1 and stage 2 cores along with the EM-simulated total gain of the amplifier across the output power of the amplifier-doubler design at an input frequency of 60 GHz. Note, the total gain includes the losses of the designed matching networks. As depicted in Figure 5.14, the amplifier stage 1 presents a flat gain of 12.8 dB across the output power. On the other hand, stage 2 has a small-signal gain of 10.3 dB and suffers from a gain compression of 1.7 dB at P_{sat} of the amplifier-doubler design. However, at the frequency doubler's peak CG, a gain compression of only 0.7 dB is achieved. Thus, the amplifier stage 2 gain compression has minimal effect on the peak CG and P_{sat} of the frequency doubler. It is

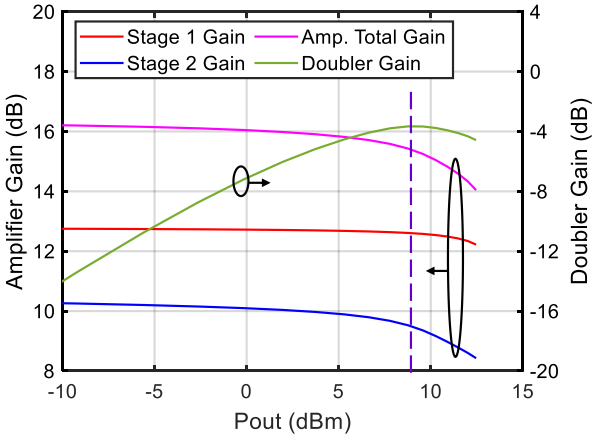


Figure 5.14: Gain at different levels of the amplifier-doubler design.

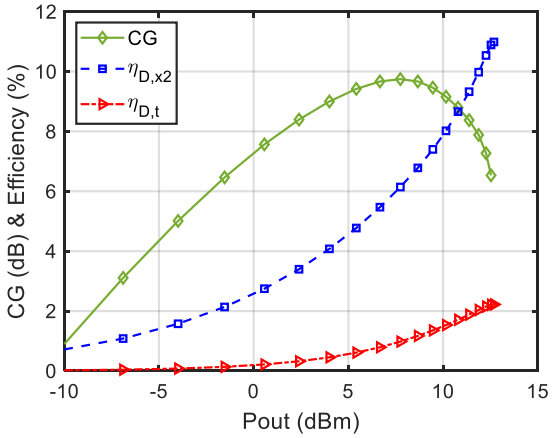


Figure 5.15: Post-layout simulation results of the amplifier-doubler design at an output frequency of 120 GHz.

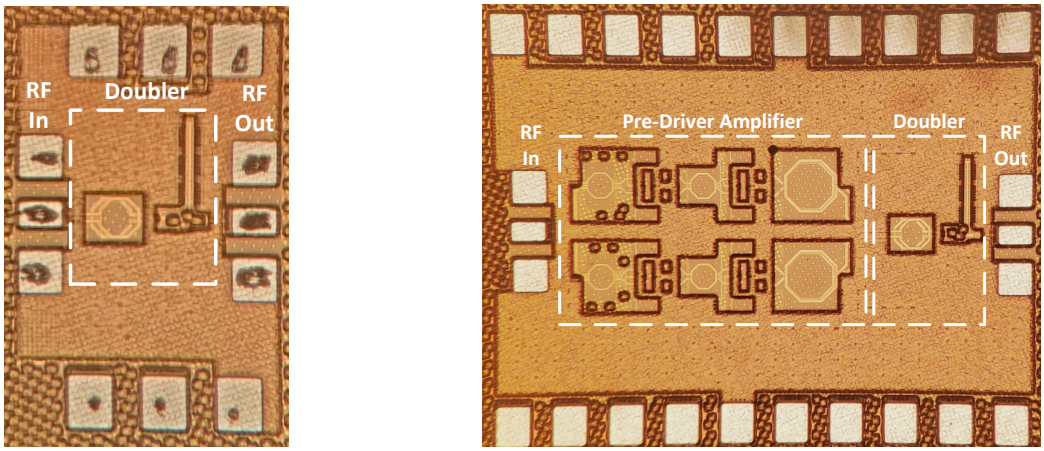
important to note that the use of a bigger amplifier core that maintains a completely linear gain response is avoided as it will consume more DC power which would degrade the total drain efficiency of the amplifier-doubler design. Moreover, the pre-driver amplifier is able to achieve a small-signal gain of 16 dB.

Next, the full layout structure of the amplifier-doubler design is EM-simulated using Keysight Momentum (EM) simulator. Figure 5.15 shows the post-layout simulation of the cascaded design. As we can see from Figure 5.15, a peak total CG of 9.7 dB, doubler

drain efficiency, $\eta_{D,x2}$, of 11%, and total drain efficiency, $\eta_{D,t}$, of 2.2% are achieved with a saturated output power of 13 dBm. Note, the two-stage 2-way pre-driver amplifier experiences high power consumption since it is designed to deliver a relatively high output power required by the frequency doubler input. This significantly affected $\eta_{D,t}$.

5.5 120-GHz Frequency Doubler Measurements

The proposed frequency doublers are fabricated using GlobalFoundries' 45-nm SOI-CMOS process. Figure 5.16 shows the chip micrograph of the two fabricated frequency doubler prototypes. Prototype I, depicted in Figure 5.16a, is the stand-alone frequency doubler occupying a core area of 0.25×0.21 mm^2. Prototype II is the amplifier-doubler design which occupies a core area of 0.98×0.4 mm^2 as shown in Figure 5.16b. The chips are measured via on-wafer probing. In this section, we will present the measurement results of the two frequency doubler prototypes when tested under CW and modulated signal stimuli.



(a) Stand-alone doubler. (b) Amplifier-doubler design.

Figure 5.16: Chip micrograph of the fabricated 120-GHz frequency doubler prototypes.

5.5.1 Measurement Setup

Figure 5.17 shows the block diagram of the measurement setup used for CW measurements. A signal source (Hittite Microwave HMC-T2270) and an external driver amplifier (Qunistar QPW-50752530) were used to bring the input signal to the desired input power

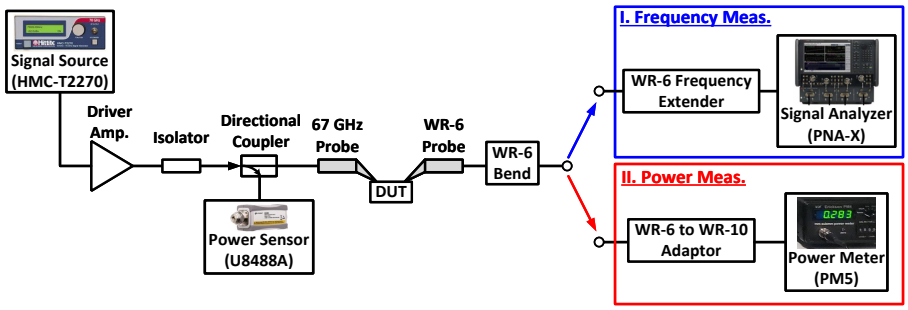


Figure 5.17: Block diagram of the CW measurement setup.

levels. A directional coupler was then used to sample the DUT's input and a power meter (Keysight U2067XA) was utilized at the coupler's coupled port to measure the DUT's input power level. The coupler's output port was fed through a coaxial RF probe (I67 GHz from FormFactor) to the DUT's input. A waveguide RF probe (I170 GHz from FormFactor) was then employed to access the DUT's output. Subsequently, for frequency measurement (i.e., S11), a D-band VNA frequency extender (OML V06VNA2-T/R) followed by a spectrum analyzer (Keysight PNA-X) was used to capture the output signal. While, for power measurement (i.e., output power, power efficiency, and CG), a power meter (Erickson N1913PM5B) augmented with a WR-6 to WR-10 adaptor was employed to measure the DUT's output power level. The losses of the associated components, including waveguides and RF probes at the input and output, have been de-embedded to the probe tips. Figure 5.18 presents a picture of the CW measurement setup.

Figure 5.19 depicts the block diagram of the measurement setup used for modulated signal measurements. An AWG (Keysight M8190A) was utilized to generate an OFDM signal centered at 2.5 GHz. To generate a 60-GHz signal at the DUT input, a two-step up-conversion was utilized. For the first up-conversion step, a cascade of a hybrid 90° and an IQ mixer (Marki MLIQ0416L) was used to up-convert the 2.5-GHz signal generated by the AWG to a center frequency of 11.5 GHz. The output signal is then amplified and filtered by a driver amplifier (Mini-Circuits ZX60-123LN-S+) and band-pass filters (FLP1250). Subsequently, the second up-conversion step was performed, where the signal was up-converted to a center frequency of 60 GHz using a WR-15 balanced mixer (Sage SFB-15-N1-M) and amplified by a driver amplifier (Qunistar QGW-50661720-P2) before being fed to the DUT. The LO signal of the second up-conversion mixer was generated using a cascade of an LO source (Keysight MXG-N5183B) and a frequency multiplier (Quinstar QMM-63251404W2) followed by a variable attenuator (Qunistar QAL-V00000).

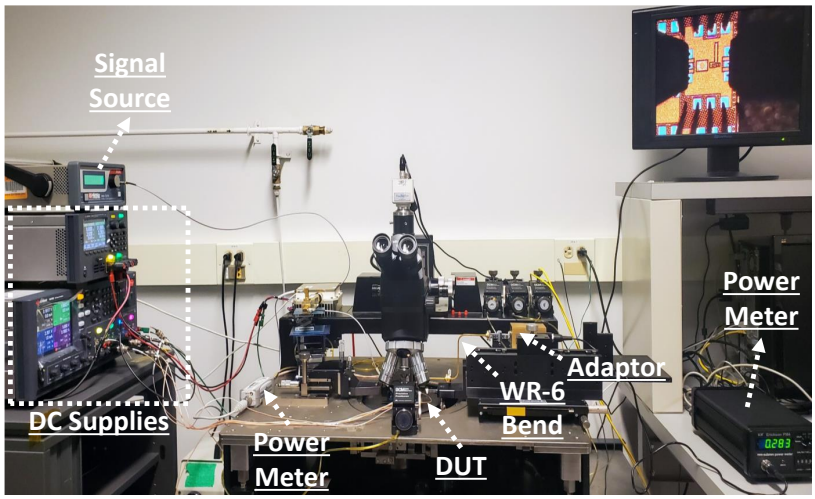


Figure 5.18: Picture of the CW measurement setup.

The DUT was mounted on a probe station where a coaxial GSG RF probe (I67 GHz from FormFactor) and a waveguide GSG RF probe (I170 GHz from FormFactor) were employed to access the DUT's input and output ports, respectively. The DUT output was connected to a waveguide D-band variable attenuator (Eravant STA-30-06-M1), and the RF signal was down-converted using a WR-06 down-converter (Eravant STC-N15-06-S1) and sampled using a 10-bit, 20 GS/s, 8 GHz analog bandwidth oscilloscope (Keysight MSOS804A). For the transmitter calibration, a directional coupler was used to sample the DUT's input where the 60 GHz RF signal was down-converted using a WR-15 balanced mixer (Sage SFB-15-N1-M) and sampled by the oscilloscope (Keysight MSOS804A). An LO source (Hittite Microwave HMC-T2270) was utilized to drive the down-conversion mixer used in the transmitter calibration path. LO sources (two Keysight MXG-N5183B and one Agilent E8267C) were employed to drive the up-conversion and down-conversion mixers in the setup. Figure 5.20 presents a picture of the measurement setup.

5.5.2 Prototype I Measurement Results

The small-signal S-parameters of the proposed frequency doubler are measured using a linear vector network analyzer (Keysight N5247A). Figure 5.21 shows the measured and simulated input reflection coefficient, highlighting achieved matching of better than -9 dB from 58 GHz to 68 GHz. It should be noted that there is a frequency shift observed in the measurement compared to the simulation due to the inaccuracies in the transistor model

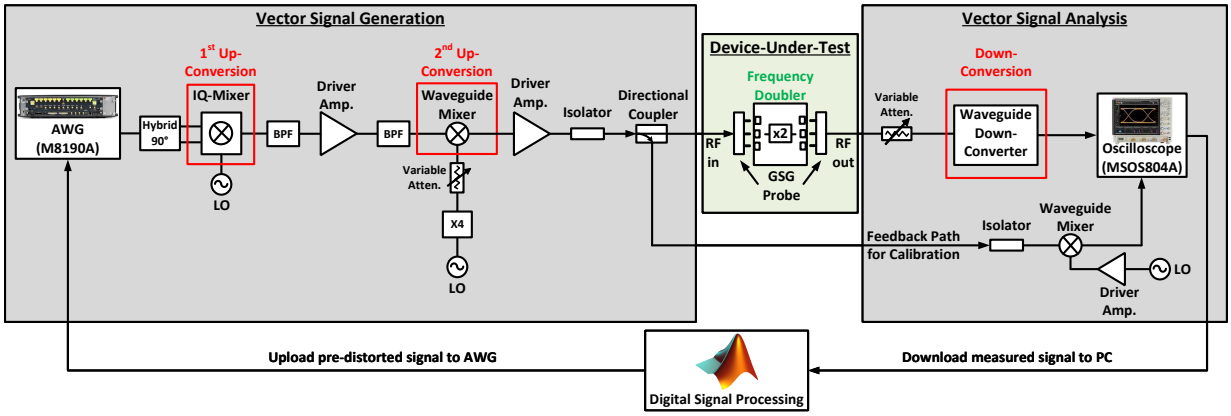


Figure 5.19: Block diagram of the modulated signal measurement setup.

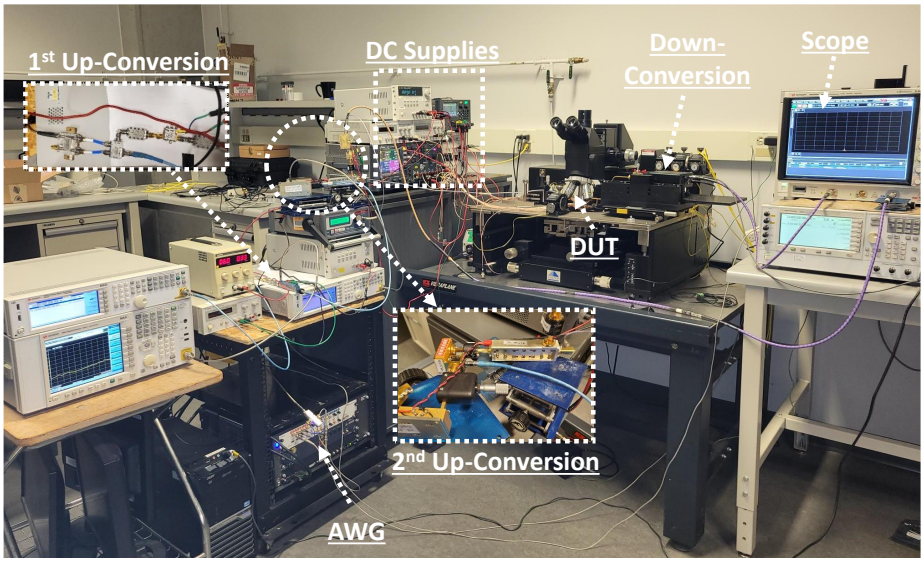


Figure 5.20: Picture of the modulated signal measurement setup.

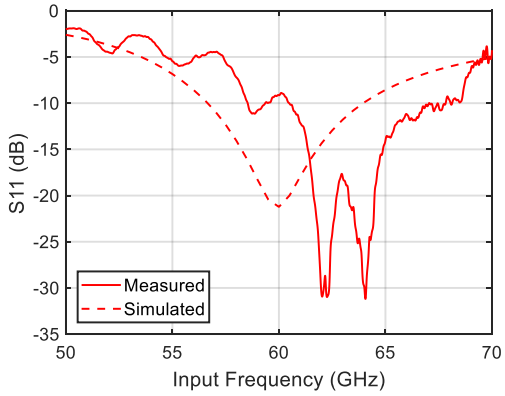
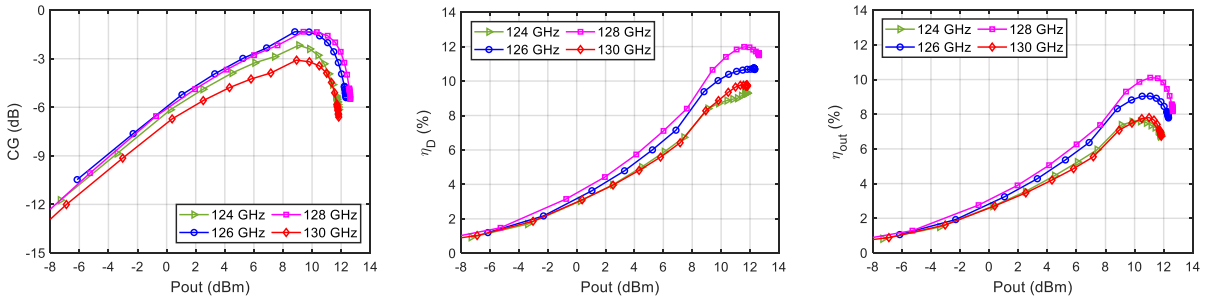


Figure 5.21: Measured and simulated input reflection coefficient of the proposed frequency doubler.



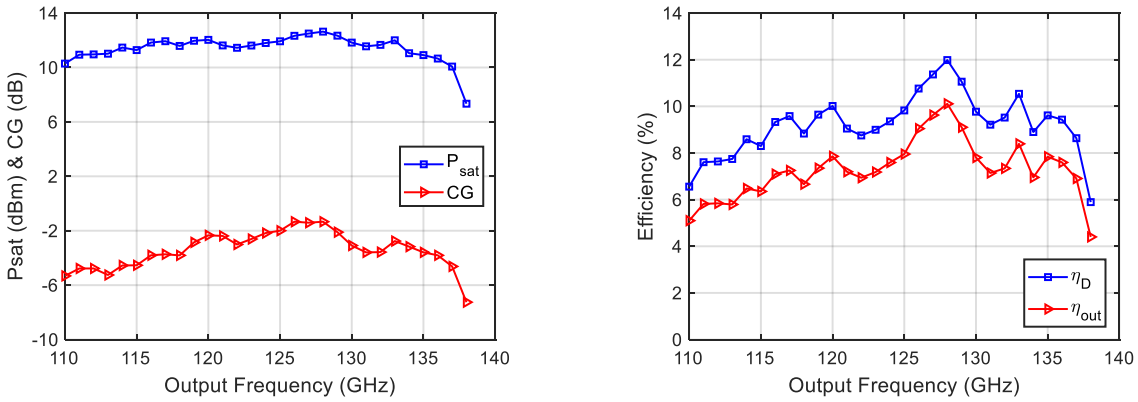
(a) (b) (c)

Figure 5.22: Measured RF performance of the proposed frequency doubler versus output power for different frequencies: (a) CG, (b) drain efficiency, and (c) DC-to-RF efficiency.

when biased in deep Class-C mode.

For the large-signal measurements, Figure 5.22 displays the measured RF performance of the proposed frequency doubler versus output power for different frequencies. It reveals an achieved peak CG, η_D, and η_{out} of -1.3 dB, 12%, and 10%, respectively, with a saturated output power of 12.6 dBm at an output frequency of 128 GHz. Furthermore, at 6-dB output power back-off, the proposed design can maintain a high peak CG of -2.8 dB and peak η_D of 7.1%, which is very advantageous, particularly in the context of generating vector modulated signals having high PAPR.

Figure 5.23 shows the RF performance of the proposed frequency doubler across the out-



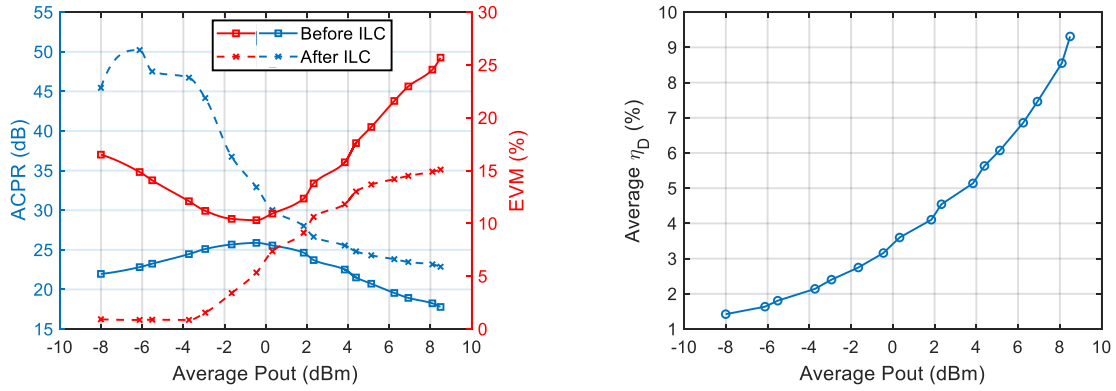
(a) (b)

Figure 5.23: Measured RF performance of the proposed frequency doubler versus the output frequency: (a) saturated output power and CG, and (b) drain efficiency.

put frequency range. As shown in Figure 5.23a, the fabricated frequency doubler exhibits a relatively high P_{sat} of 12.6 dBm, along with a 1-dB P_{sat} bandwidth, BW_{1dB}, ranging from 118 GHz to 132 GHz. Across this bandwidth, the proposed design maintains a relatively high RF performance, achieving a CG, η_D, and η_{out} above -2.5 dB, 9%, and 6.7%, respectively, as depicted in Figures 5.23a and 5.23b. These results demonstrate the effectiveness of the proposed design approach in enhancing the output power, CG, and power efficiency of the frequency doubler. Note that there is a ripply behavior in the RF performance across frequency which can be attributed to calibration issues and/or inaccuracy of the power meter.

The linearizability of the proposed frequency doubler was evaluated using OFDM test signals with their subcarriers modulated using 256-QAM and a subcarrier spacing of 120 kHz. These signals were characterized by a PAPR of 9 dB. The modulation bandwidth of the test signals used are 800 MHz and 1200 MHz. To compensate for signal generator nonidealities and ensure error-free signals at the DUT, a linear source correction was performed using a multi-tone signal with a frequency spacing of 1 MHz and a modulation bandwidth of 3 GHz.

The linearization performance of the stand-alone frequency doubler design was validated using an iterative learning control (ILC) method. Compared to DPD, the ILC linearizer does not suffer from modeling and estimation inaccuracies. Instead, it relies on an iterative approach to find the optimum linearization solution based on the measured error signal at the DUT output. ILC is commonly used to provide a benchmark linearization performance



(a) (b)

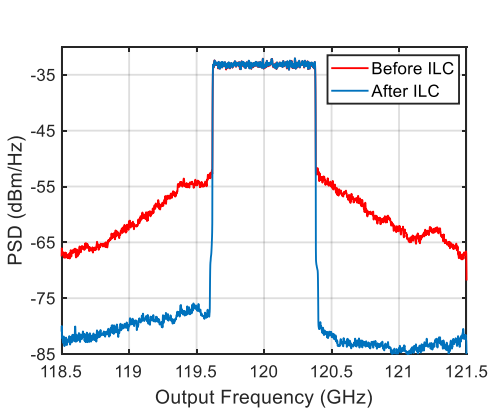
Figure 5.24: Measured (a) ACPR and EVM, and (b) average doubler drain efficiency of prototype I versus the average output power with and without ILC linearization technique using 256-QAM OFDM signal with 800 MHz modulation bandwidth at a carrier frequency of 120 GHz.

for devices.

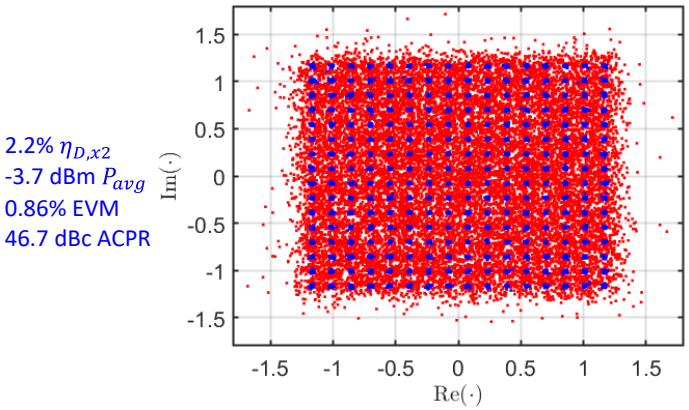
The modulated signal performance of the fabricated design is evaluated at an output frequency of 120 GHz. Figure 5.24 depicts the modulated signal performance versus the average output power when driven by the 800 MHz OFDM signal without and with ILC linearization technique. According to Figure 5.24a, the ACPR and EVM are improved from 24.5 dBc and 12% to 46.7 dBc and 0.86%, respectively, using ILC. Based on Figure 5.24b, these results are achieved at an average η_D of 2.2%. It is important to note that the performance above an average output power of -3 dBm gets worse rapidly since the required input power of the stand-alone frequency doubler is high and consequently the external amplifiers used in the measurement setup are pushed to their nonlinear region. This limits the linearizability at high input power levels.

Figure 5.25 depicts the PSD, constellation plot, gain distortion, and phase distortion at the frequency doubler output, with the average power set to -3.7 dBm and average η_D value of 2.2%. Figure 5.25b shows a clean constellation. Also, Figures 5.25c and 5.25d demonstrate flat gain and phase response after applying ILC linearizer.

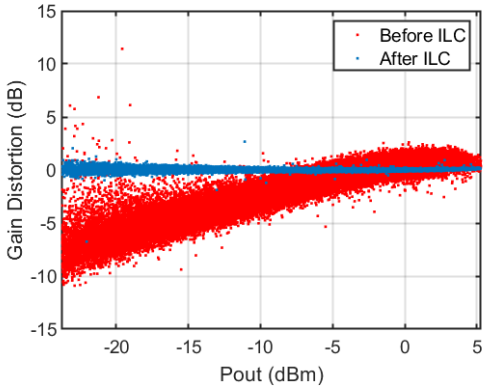
Figures 5.26 and 5.27 show the modulated signal performance of the stand-alone frequency doubler design at a $2f_o$ of 120 GHz when driven by the 1200 MHz OFDM signal with and without ILC linearizer. From Figure 5.26, it can be observed that when ILC is applied, the proposed frequency doubler achieves an output of up to -0.1 dBm average



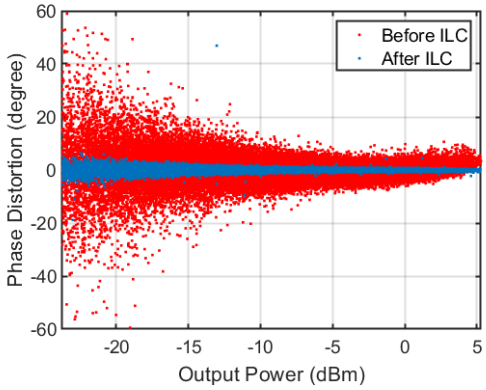
(a) Power spectrum density.



(b) Constellation (before/after ILC).

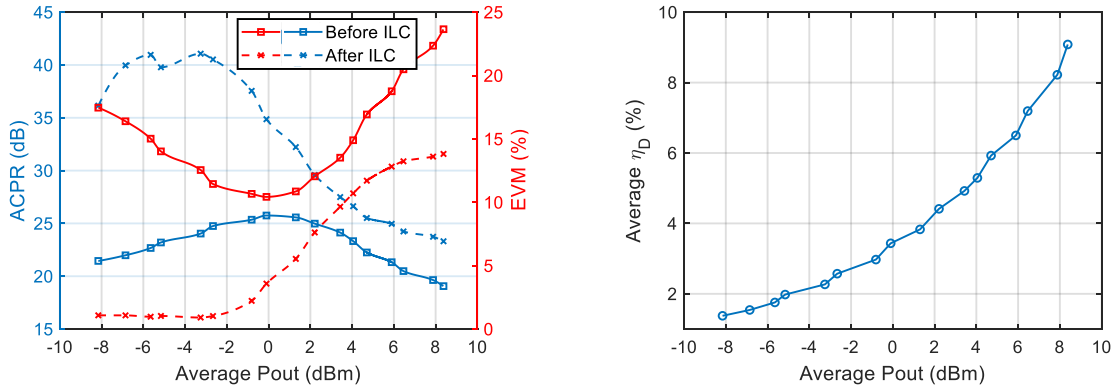


(c) Gain distortion.



(d) Phase distortion.

Figure 5.25: Measured modulated signal performance at the stand-alone frequency doubler output using 256-QAM OFDM signal with 800 MHz modulation bandwidth at a carrier frequency of 120 GHz with and without ILC linearization technique.



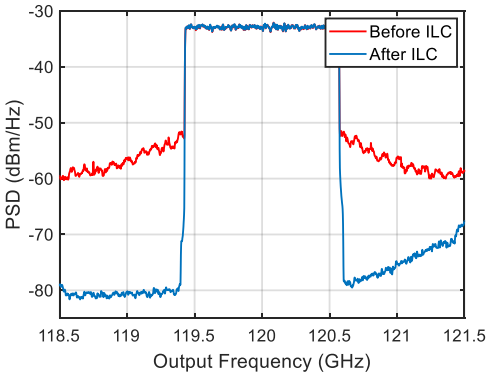
(a) (b)

Figure 5.26: Measured (a) ACPR and EVM, and (b) average doubler drain efficiency of prototype I versus the average output power with and without ILC linearization technique using 256-QAM OFDM signal with 1200 MHz modulation bandwidth at a carrier frequency of 120 GHz.

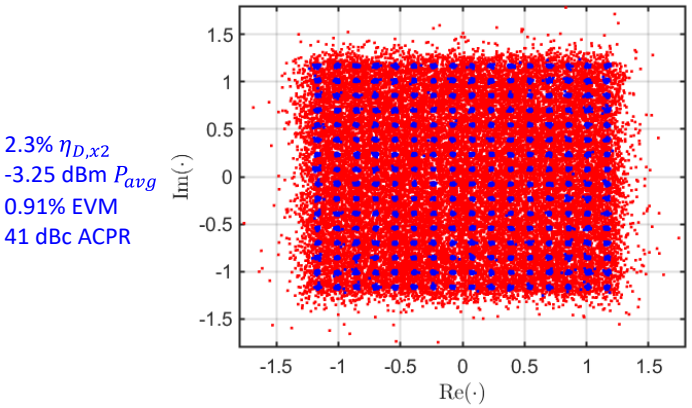
output power, with an average η_D of 3.4%. These results satisfy the 3GPP requirement for 256-QAM OFDM signals, with ACPR and EVM maintained below 31.8 dBc and 3.5%, respectively. Figure 5.27 depicts the PSD, constellation plot, gain distortion, and phase distortion at the frequency doubler output, with the average power set to -3.25 dBm and average η_D of 2.3%. From Figure 5.27a, the ACPR and EVM improved from 24 dBc and 12.5% before ILC to 41 dBc and 0.91% after ILC, respectively. Moreover, Figure 5.27b, 5.27c, and 5.27d demonstrate a clean EVM constellation plot and flat gain and phase response after applying ILC to the proposed frequency doubler design. These results confirm the capacity of the proposed frequency doubler to generate vector modulated signals with high signal fidelity.

5.5.3 Prototype II Measurement Results

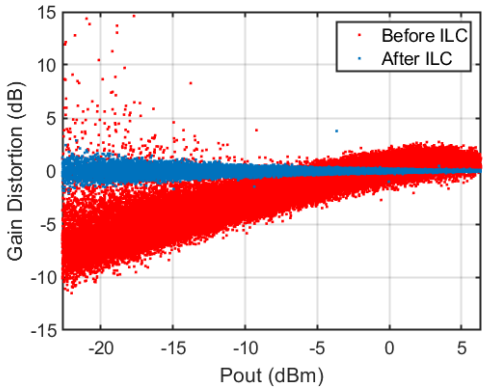
The measurement setup described in Figure 5.17 is used to perform the large-signal measurements on the amplifier-doubler design. Figure 5.28 depicts the measured CG and drain efficiency versus output power for various frequencies. At an output frequency of 128 GHz, a doubler drain efficiency, $\eta_{D,x2}$, of 14%, a total drain efficiency, $\eta_{D,t}$, of 2.8%, and a total peak CG of 13.4 dB are measured with a P_{sat} of 13.1 dBm. After de-embedding the amplifier gain using simulation results, the frequency doubler achieves a peak CG of



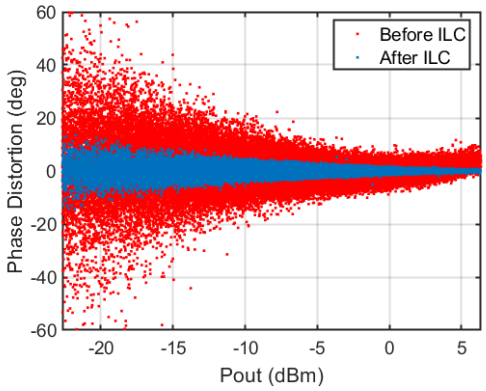
(a) Power spectrum density.



(b) Constellation (before/after ILC).

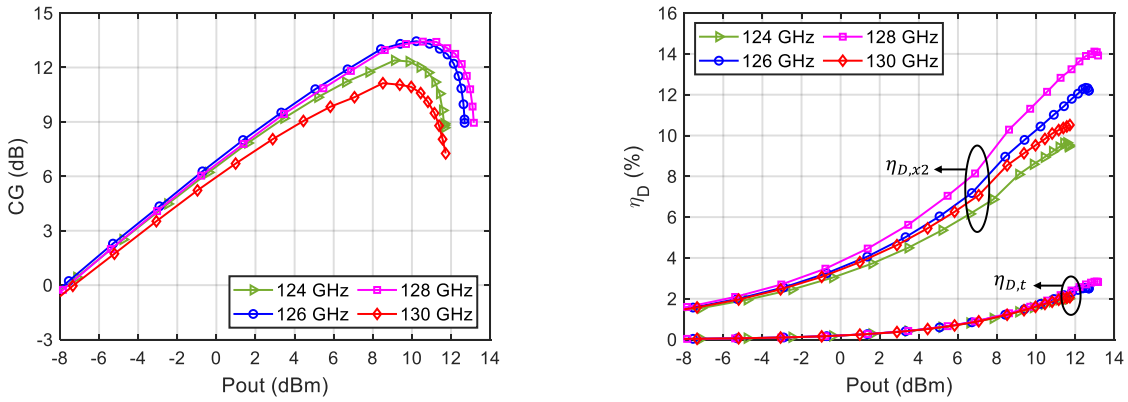


(c) Gain distortion.



(d) Phase distortion.

Figure 5.27: Measured modulated signal performance at the stand-alone frequency doubler output using 256-QAM OFDM signal with 1200 MHz modulation bandwidth at a carrier frequency of 120 GHz with and without ILC linearization technique.



(a) (b)

Figure 5.28: Measured RF performance of the amplifier-doubler design versus output power for different frequencies: (a) CG, and (b) drain efficiency.

-2.1 dB.

Figure 5.29a shows the P_{sat} and CG of the amplifier-doubler design versus the output frequency. It highlights a 1-dB P_{sat} bandwidth of 12 dB (from 118 GHz to 130 GHz) with a reduction in the CG by only 2.3 dB across this bandwidth. Moreover, Figure 5.29b presents the measured efficiency versus the output frequency. We can see that $\eta_{D,\text{x2}}$ and $\eta_{D,t}$ are maintained above 8.5% and 2%, respectively, across the frequency range of 114-130 GHz.

Table 5.2 shows a performance comparison of the proposed frequency doublers with state-of-the-art F-band (90-140 GHz) and D-band (110-170 GHz) frequency doublers. It also compares the frequency doubler performance to PAs at similar frequency ranges. Note that the reported frequency, namely Freq., is the 3-dB P_{sat} bandwidth. The proposed designs achieve the highest output power compared to other works in the literature with competitive power efficiency and CG.

The linearizability of the proposed frequency doubler was evaluated using OFDM test signals with their subcarriers modulated using 256-QAM and a subcarrier spacing of 120 kHz. These signals were characterized by a PAPR of 9 dB. To compensate for signal generator nonidealities and ensure error-free signals at the DUT, a linear source correction was performed using a multi-tone signal with a frequency spacing of 1 MHz and a modulation bandwidth of 3 GHz.

The linearization performance of the amplifier-doubler design was validated using two linearization methods: the DPD model, with a total of 63 coefficients based on [22], and

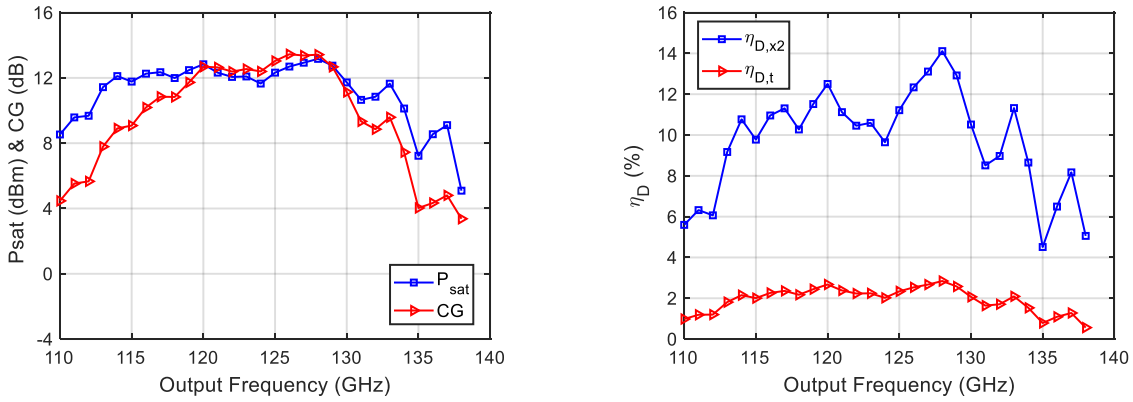


Figure 5.29: Measured RF performance of the amplifier-doubler design versus the output frequency: (a) saturated output power and CG, and (b) drain efficiency.

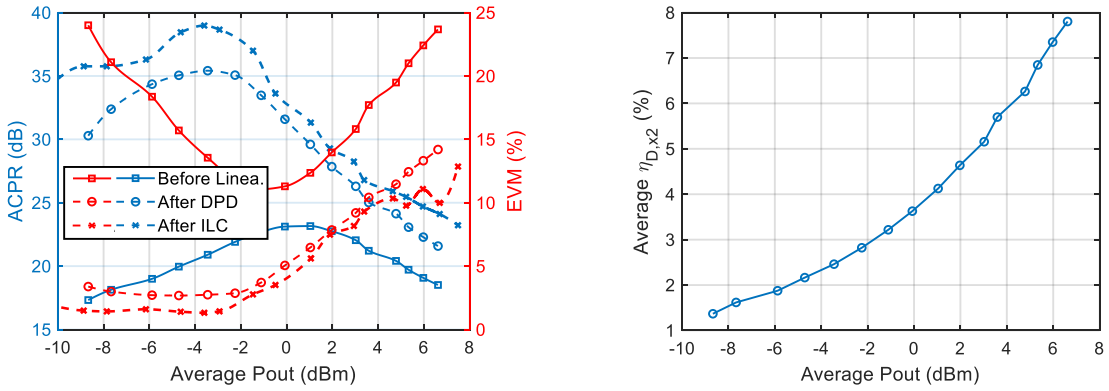
Table 5.2: CW Performance Comparison of F-Band and D-Band Frequency Doublers

Ref.	Technology	Topology	Freq. (GHz)	P_{sat} (dBm)	CG[a] (dB)	η_D[a] (%)	Area (mm^2)
This work	45-nm SOI	x2	110-137	12.6	-1.3	12	0.3
This work	45-nm SOI	Amp.+x2	112-134	13.1	13.4	2.8	1.14
IMS'14 [62]	45-nm SOI	x2	135-160	3.5	-3	9	0.44
EuMIC'22 [66]	22-nm FDSOI	x2	125-145	4.1	-5.5	11.8	0.33
EuMIC'15 [70]	28-nm CMOS	x2	105-130	4	-2.2	18	0.17
JSSC'23 [68]	55-nm CMOS	x2	112-125	7.8	-0.46	6.8	0.21
RFIT'17 [50]	65-nm CMOS	x2+Amp.	100-118	5	17.2	3	0.83
MWCL'14 [63]	130-nm CMOS	Amp.+x2	134	4.2	-3.1	0.33	–
SSC-L'21 [65]	55-nm SiGe	Amp.+x2	116-143	8.1	13.1	6.6	–
MTT'21 [72]	90-nm SiGe	x2+Amp.	118-146	8.85	1.8	8.8	0.9
MTT'21 [72]	90-nm SiGe	x2	128-140	9.4	-0.87	12.1	0.57
RFIC'16 [64]	130-nm SiGe	x2+Amp.	138-170	5.6	4.9	10.9	0.48

[a] Peak value [b] Core area

the ILC method. The ILC is used to provide a benchmark linearization performance for the fabricated design.

The modulated signal performance of the fabricated design is evaluated at two frequency points, 120 GHz and 128 GHz. Figure 5.30 depicts the modulated signal performance versus the average output power at a $2f_o$ of 128 GHz when driven by the 800 MHz OFDM signal: i) without linearization (linea.), ii) after DPD applied, and iii) after ILC applied. According to Figure 5.30a, when no linearization technique is applied and for an average output power of around -2.5 dBm, the proposed design can achieve an ACPR of 22 dBc and an EVM of 12%. By applying linearization techniques, the performance is improved to an EVM of 2.8% (resp. 1.5%) and an ACPR of 35 dBc (resp. 38.7 dBc) using DPD (resp. ILC). Based on Figure 5.30b, these results are achieved at an average $\eta_{D,\text{x2}}$ of 2.8%.

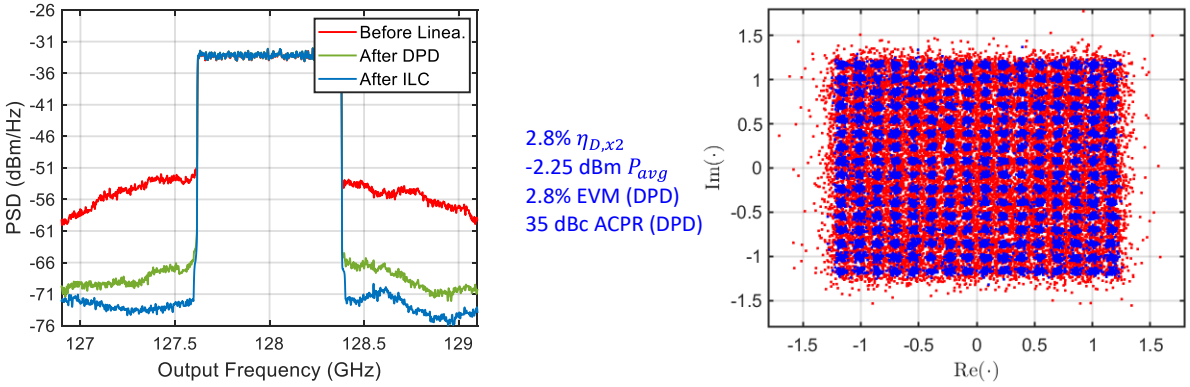


(a) (b)

Figure 5.30: Measured (a) ACPR and EVM, and (b) average doubler drain efficiency versus the average output power without linearization, with ILC and with DPD using 256-QAM OFDM signal with 800 MHz modulation bandwidth at a carrier frequency of 128 GHz.

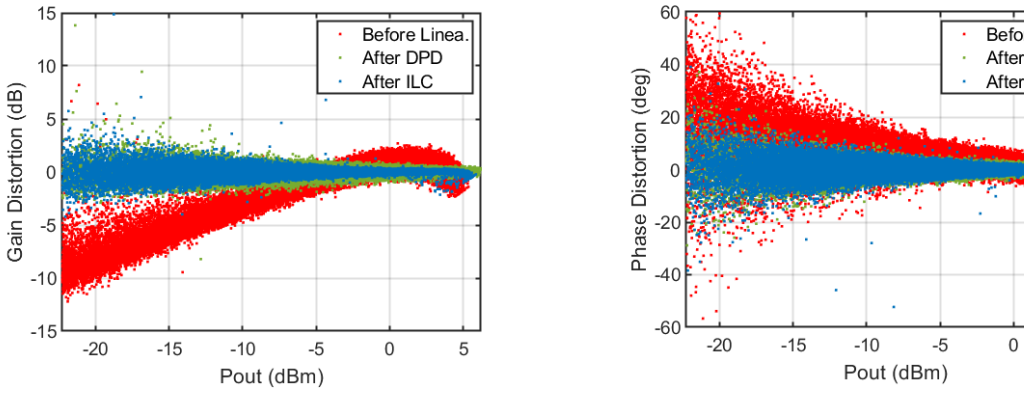
Figure 5.31 depicts the PSD, constellation plot, gain distortion, and phase distortion at the frequency doubler output, with the average power set to -2.5 dBm and average $\eta_{D,\text{x2}}$ value of 2.8%. Figure 5.31b shows a clean constellation. Also, Figures 5.31c and 5.31d demonstrate flat gain and phase response after applying DPD with a slightly better performance after applying the ILC linearizer. These results confirm the capacity of the proposed frequency doubler to generate vector modulated signals with high signal fidelity.

Figures 5.32 and 5.33 present the modulated signal performance of the amplifier-doubler design at a $2f_o$ of 120 GHz when driven by the 800 MHz OFDM signal: i) without linearization, ii) after DPD applied, and iii) after ILC applied. According to Figure 5.32a, a high



(a) Power spectrum density.

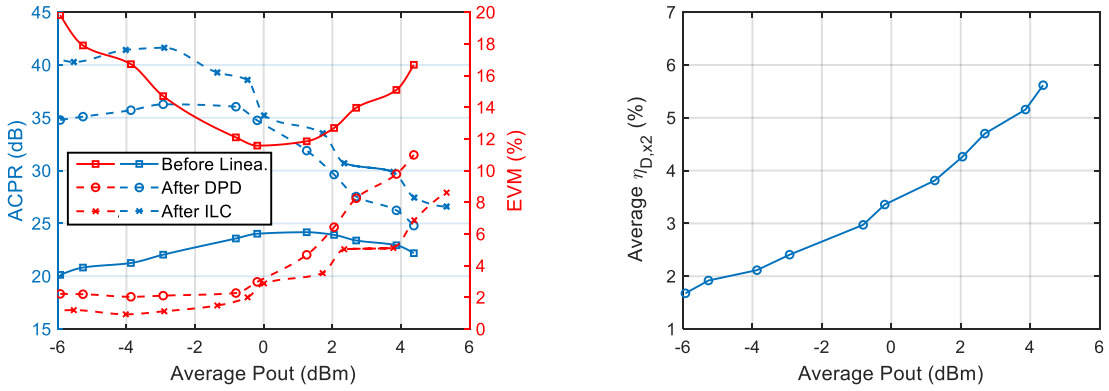
(b) Constellation (before/after DPD).



(c) Gain distortion.

(d) Phase distortion.

Figure 5.31: Measured modulated signal performance at the frequency doubler output using 256-QAM OFDM signal with 800 MHz modulation bandwidth at a carrier frequency of 128 GHz: i) before linearization, ii) after DPD applied, and after ILC applied.



(a) (b)

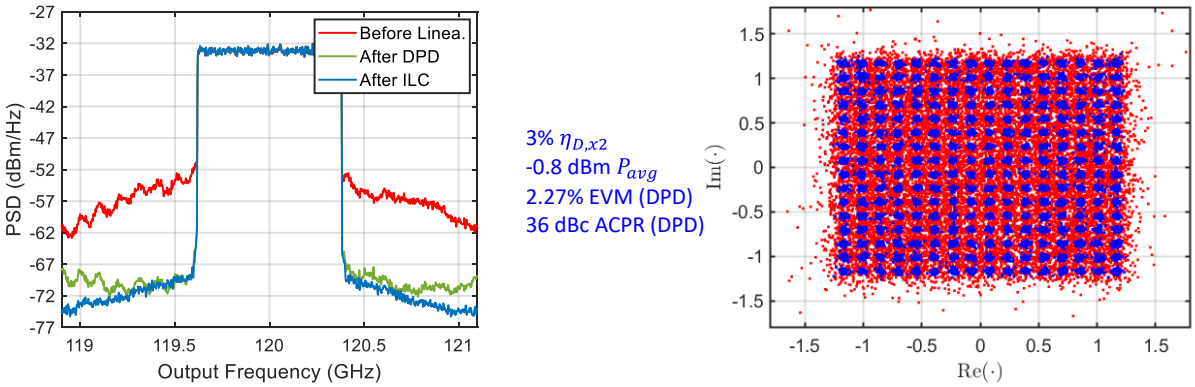
Figure 5.32: Measured (a) ACPR and EVM, and (b) average doubler drain efficiency versus the average output power without linearization, with ILC and with DPD using 256-QAM OFDM signal with 800 MHz modulation bandwidth at a carrier frequency of 120 GHz.

ACPR of 41.6 dBc and a low EVM of 1.12% can be achieved after applying ILC staring from an ACPR of 22 dBc and an EVM of 14% before linearization is applied. This result is achieved at an average $\eta_{D,x2}$ of 2.4% based on Figure 5.32b. Moreover, the gain and phase distortion before and after applying linearization techniques are shown in Figures. 5.33c and 5.33c showing almost flat response.

Table 5.3 summarizes the modulated signal performance of the two D-band frequency doubler prototypes. It shows the ability of the fabricated designs to generate vector modulated signals with low EVM and reasonable output power. Hence, this D-band frequency doubler can be effectively used in the targeted RF beamforming front-end structure for high-frequency vector modulated signal generation.

5.6 Conclusion

This chapter proposed a novel design approach for designing frequency doublers targeting frequencies above 100 GHz. The proposed approach exploited a more realistic solution for the choice of the 2^{nd} harmonic source impedance that can be practically realized at these high frequencies. Accordingly, two frequency doubler prototypes targeting a 120-GHz frequency range are fabricated and evaluated experimentally. These prototypes includes a stand-alone frequency doubler and a cascade of a driver amplifier and a frequency doubler.



(a) Power spectrum density.

(b) Constellation (before/after DPD).

(c) Gain distortion.

(d) Phase distortion.

Figure 5.33: Measured modulated signal performance at the frequency doubler output using 256-QAM OFDM signal with 800 MHz modulation bandwidth at a carrier frequency of 120 GHz: i) before linearization, ii) after DPD applied, and after ILC applied.

Table 5.3: Performance Summary of Frequency Doubler Under Modulated Signal Stimuli

Proto-type	freq. (GHz)	Techn-ique	Mod. Scheme	Mod. BW	ACPR (dBc)	EVM (%)	$P_{avg}{}^{a}$ (dBm)	$\eta_{D,x2}{}^{a}$ (%)
I	120	ILC	256-QAM	800 MHz	46.7	0.86	-3.7	2.2
I	120	ILC	256-QAM	1200 MHz	41	0.91	-3.25	2.3
II	120	ILC	256-QAM	800 MHz	41.6	1.12	-2.9	2.4
II	120	DPD	256-QAM	800 MHz	36.2	2.1	-2.9	2.4
II	120	DPD	256-QAM	800 MHz	36	2.3	-0.8	3
II	128	ILC	256-QAM	800 MHz	38.7	1.5	-2.5	2.8
II	128	DPD	256-QAM	800 MHz	35	2.8	-2.5	2.8

[a] @ the reported EVM

Their measurement results showed the effectiveness of the proposed design approach to improve the output power, power efficiency, and CG by achieving state-of-the-art performance. The amplifier-doubler prototype can be added at the output of the 60-GHz RF beamforming front-end, presented in Chapter 4, to design a complete RF beamforming structure targeting an output frequency of 120 GHz.

Chapter 6

Conclusion

The abundance of untapped spectrum bands at mm-wave and sub-THz frequency bands has spurred the expansion of wireless systems to these bands in order to address the escalating capacity and data throughput requirements imposed by the emerging 6G mobile communication. However, the generation of highly-efficient vector modulated signals at these frequency bands confronts significant challenges. Amongst various front-end architectures, the frequency multiplier-based front-end exhibits notable potential for high-frequency signal generation. The main aim of this thesis is to develop frequency doublers capable of generating vector modulated signals with adequate output power levels, power efficiency, and linearity. The ultimate goal is to seamlessly integrate these frequency doublers into an RF beamforming structure to boost the front-end's output power.

As a first step, a new design methodology for designing high-efficiency push-push frequency doublers with improved AM-PM characteristics was proposed. The methodology commenced by defining the current and voltage waveforms at the output of the transistor to identify the set of harmonic load impedance terminations that can maintain consistent output power and power efficiency over the designated bandwidth. Subsequently, it delved into formulating the AM-PM characteristics, taking into account the transistor parasitic input capacitance, to investigate the optimum choice of the harmonic source impedance termination that minimizes the AM-PM nonlinearity. The proposed methodology was applied to designing frequency doublers around an output frequency of 60 GHz. The fabricated designs were validated using measurement results, showing promising output power, power efficiency, and CG. Also, by applying the DPD linearization technique, the frequency doubler designs showed the ability to generate OFDM vector modulated signals with acceptable EVM and average efficiency.

Next, the design considerations of the phase shifters in the context of frequency multiplier-based front-end were investigated. A comprehensive study of the different RTPS topologies was presented to determine the optimum topology that meets the pre-defined design constraints. It then guided the design of RTPS at an operating frequency of 30 GHz. This paved the way for a proof-of-concept demonstration of the RF beamforming front-end, encompassing a phase shifter, driver amplifier, and V-band frequency doubler. The demonstrator was able to achieve a full 360° phase tuning range at a 7-bit front-end phase resolution with high gain and phase accuracy. It effectively generated a vector modulated signal with a flat EVM and ACPR across the full 360°.

Lastly, targeting the D-band frequency range prompted the introduction of a novel design approach for frequency doublers. This approach explored a practical solution for the harmonic source impedance termination that can be realized at such high frequency range. Based on the proposed approach, two frequency doubler prototypes are developed. The first prototype was a stand-alone frequency doubler while the second one used a pre-driver amplifier in cascade with the frequency doubler to augment the overall gain. These prototypes were validated experimentally and achieved promising output power and power efficiency at an output frequency of around 120 GHz. Also, levering the DPD linearization technique, the fabricated prototypes were able to generate OFDM vector modulated signals with acceptable EVM and ACPR at this elevated frequency.

6.1 Summary of Contributions

The goal of this thesis is to develop a frequency doubler-based RF beamforming front-end module that can generate vector modulated signals. This goal was achieved through the following key contributions:

1. A new design methodology for designing push-push frequency doublers was presented. The methodology proposed the optimum selection of the harmonic load and source impedance terminations that can maintain acceptable RF performance across the designated bandwidth and minimize the AM-PM nonlinearity. Based on this methodology, V-band frequency doublers were fabricated and validated experimentally.

2. An extensive study on the different RTPS topologies was conducted to determine the optimum one that would fit in a frequency doubler-based front-end while meeting its design constraints. Accordingly, a frequency doubler-based RF beamforming front-end module was developed.

3. A new design approach was presented to guide the design of frequency doublers at the D-band frequency range. This approach proposed a practically-realizable harmonic source impedance termination at such elevated frequency range. Then, it was applied to designing frequency doublers around an output frequency of 120 GHz.

6.2 Future Work

In this thesis, we introduced novel design methodologies to improve the RF performance of frequency doublers targeting V-band and D-band frequency ranges along with an initial prototype of a V-band frequency doubler-based RF beamforming front-end module. This work can be extended into several research lines.

The focus of the thesis was centered on the circuit-level design of frequency doublers and phase shifters to achieve an acceptable performance that would establish the foundation for developing RF beamforming front-end modules capable of generating vector modulated signals. An extension can be added by designing an RF beamforming line-up operating at an output frequency of 120 GHz, comprising a phase shifter, amplifiers, and a cascade of two frequency doublers (i.e., frequency quadrupler). This extension could further evolve into an n-way frequency multiplier-based RF beamforming structure, enabling full integration into a large-scale antenna-array system. Another feature that could be added involves implementing a D-band output combiner at the output of the n-way structure to combine the signals from the different paths. This would enable the creation of a high-power high-frequency vector modulated signal source.

Furthermore, this research could lay the foundation for the development of front-end modules targeting the G-band frequency range (e.g., 240 GHz) by simply cascading additional frequency doubler stages. Hence, it would be an interesting topic to explore the design of an extra frequency doubler operating at an output frequency of around 240 GHz and integrating it with this work to achieve a high order of multiplication.

6.3 List of Publications

Journal Papers

1. M. Eladwy, A. Ben Ayed, A. M. Darwish, and S. Boumaiza, "V-Band continuous-mode frequency doubler with enhanced efficiency and AM-PM Characteristic for vector modulated signal generation," submitted to IEEE Journal of Solid-State Circuits, Sept. 2023.

Conference Papers

1. M. Eladwy, A. Ben Ayed, A. M. Darwish, and S. Boumaiza, "A V-Band 16% efficiency frequency doubler-based RF beamforming front-end module for vector modulated signal transmission," in 2023 53rd European Microwave Conference, Sept. 2023.

2. M. Eladwy, A. Ben Ayed, and S. Boumaiza, "VNA-based characterization of frequency multipliers phase-distortions under continuous-wave and modulated signal excitation," in 2023 101th ARFTG Microwave Measurement Conference, Jun. 2023.

3. M. Eladwy, J. Xia, A. Ben Ayed, and S. Boumaiza, "A 60 GHz CMOS-SOI stacked push-push frequency doubler with 12 dBm output power and 20% efficiency," 2021 IEEE MTT-S International Microwave Symposium, Jun. 2021.

4. J. Xia, M. Farouk, and S. Boumaiza, "Digitally-assisted 27-33 GHz reflection-type phase shifter with enhanced accuracy and low IL-variation," 2019 IEEE Radio Frequency Integrated Circuits Symposium, Jun. 2019.

References

[1] Samsung, "6G spectrum expanding the frontier," *White paper*, May 2022.

[2] H. Wang, T.-Y. Huang, N. S. Mannem, J. Lee, E. Garay, D. Munzer, E. Liu, Y. Liu, B. Lin, M. Eleraky, H. Jalili, J. Park, S. Li, F. Wang, A. S. Ahmed, C. Snyder, S. Lee, H. T. Nguyen, and M. E. D. Smith. (2021) Power amplifiers performance survey 2000-present. [Online]. Available: https://gems.ece.gatech.edu/PA_survey.html

[3] M. H. Eissa, A. Malignaggi, R. Wang, M. Elkhouly, K. Schmalz, A. C. Ulusoy, and D. Kissinger, "Wideband 240-GHz transmitter and receiver in BiCMOS technology with 25-Gbit/s data rate," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2532–2542, Jun. 2018.

[4] K. Katayama, K. Takano, S. Amakawa, S. Hara, A. Kasamatsu, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 300GHz 40nm CMOS transmitter with 32-QAM 17.5Gb/s/ch capability over 6 channels," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, USA, Feb. 2016, pp. 342–343.

[5] S. Kang, S. V. Thyagarajan, and A. M. Niknejad, "A 240 GHz fully integrated wideband QPSK transmitter in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2256–2267, Sept. 2015.

[6] C. J. Lee, S. H. Kim, H. S. Son, D. M. Kang, J. H. Kim, C. W. Byeon, and C. S. Park, "A 120 GHz I/Q transmitter front-end in a 40 nm CMOS for wireless chip to chip communication," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Philadelphia, PA, USA, Aug. 2018, pp. 192–195.

[7] P. Rodríguez-Vázquez, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 65 Gbps QPSK one meter wireless link operating at a 225–255 GHz tunable carrier in a SiGe HBT technology," in *2018 IEEE Radio and Wireless Symposium (RWS)*, Anaheim, CA, USA, Jan. 2018, pp. 146–149.

[8] N. Sarmah, P. R. Vazquez, J. Grzyb, W. Foerster, B. Heinemann, and U. R. Pfeiffer, "A wideband fully integrated SiGe chipset for high data rate communication at 240 GHz," in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, London, UK, Oct. 2016, pp. 181–184.

[9] Q. Zhong, Z. Chen, N. Sharma, S. Kshattry, W. Choi, and K. O. Kenneth, "300-GHz CMOS QPSK transmitter for 30-Gbps dielectric waveguide communication," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, San Diego, CA, USA, Apr. 2018, pp. 1–4.

[10] K. K. Tokgoz, S. Maki, J. Pang, N. Nagashima, I. Abdo, S. Kawai, T. Fujimura, Y. Kawano, T. Suzuki, T. Iwai, K. Okada, and A. Matsuzawa, "A 120Gb/s 16QAM CMOS millimeter-wave wireless transceiver," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2018, pp. 168–170.

[11] P. Rodríguez-Vázquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "A 16-QAM 100-Gb/s 1-M wireless link with an EVM of 17% at 230 GHz in an SiGe technology," *IEEE Microwave and Wireless Components Letters*, vol. 29, no. 4, pp. 297–299, Mar. 2019.

[12] S. Carpenter, D. Nopchinda, M. Abbasi, Z. S. He, M. Bao, T. Eriksson, and H. Zirath, "A D-band 48-Gbit/s 64-QAM/QPSK direct-conversion I/Q transceiver chipset," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 4, pp. 1285–1296, Mar. 2016.

[13] K. Takano, S. Amakawa, K. Katayama, S. Hara, R. Dong, A. Kasamatsu, I. Hosako, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 105Gb/s 300GHz CMOS transmitter," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, USA, Feb. 2017, pp. 308–309.

[14] J. Park, H. Ryu, K.-W. Ha, J.-G. Kim, and D. Baek, "76–81-GHz CMOS transmitter with a phase-locked-loop-based multichirp modulator for automotive radar," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1399–1408, Mar. 2015.

[15] J.-H. Song, C. Cui, S.-K. Kim, B.-S. Kim, and S. Nam, "A low-phase-noise 77-GHz FMCW radar transmitter with a 12.8-GHz PLL and a $\times 6$ frequency multiplier," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 7, pp. 540–542, Jun. 2016.

[16] K. Wu, B. Fahs, and M. Hella, "A 220 GHz OOK outphasing transmitter in 130-nm BiCMOS technology," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, San Diego, USA, Oct. 2018, pp. 227–230.

[17] A. Darwish, J. Qiu, E. Viveiros, H. A. Hung, and J. Hesler, "Efficient linear transmission of complex waveforms at 216 GHz using nonlinear multiplier chains," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, San Francisco, USA, May 2016, pp. 1–3.

[18] A. Standaert and P. Reynaert, "A 390-GHz outphasing transmitter in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 10, pp. 2703–2713, Oct. 2020.

[19] Y. Liu, G. Liu, and P. M. Asbeck, "High-order modulation transmission through frequency quadrupler using digital predistortion," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 6, pp. 1896–1910, Jun. 2016.

[20] T. Cao, Y.-J. Liu, J. Jiang, Q. Zhang, C. Lin, D. Yang, G. Zhang, C. Yang, and J. Zhou, "Frequency multiplier-based millimeter-wave vector signal transmitter using digital predistortion with constrained feedback bandwidth," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 5, pp. 1819–1829, May 2020.

[21] A. Chung, A. M. Darwish, E. Viveiros, H. A. Hung, P. Mitran, and S. Boumaiza, "Analysis and compensation of nonidealities in frequency multiplier-based high-frequency vector signal generators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 6, pp. 2270–2283, Jun. 2019.

[22] I. Jaffri, A. B. Ayed, A. M. Darwish, P. Mitran, and S. Boumaiza, "Novel baseband equivalent model for digital predistortion of wideband frequency-multiplier-based millimeter wave sources," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 9, pp. 3942–3957, Sept. 2020.

[23] S. Muralidharan, K. Wu, and M. Hella, "A 165–230GHz SiGe amplifier-doubler chain with 5dBm peak output power," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, USA, May 2016, pp. 302–305.

[24] H.-C. Lin and G. M. Rebeiz, "A SiGe multiplier array with output power of 5–8 dBm at 200–230 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2050–2058, 2016.

[25] J.-D. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *2012 Symposium on VLSI Circuits (VLSIC)*, Honolulu, HI, USA, June 2012, pp. 48–49.

[26] F. Golcuk, O. D. Gurbuz, and G. M. Rebeiz, "A 0.39–0.44 THz 2x4 amplifier-quadrupler array with peak EIRP of 3–4 dBm," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4483–4491, Nov. 2013.

[27] S. Mondal and J. Paramesh, "Power-efficient design techniques for mm-wave hybrid/digital FDD/full-duplex MIMO transceivers," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 8, pp. 2011–2026, May 2020.

[28] J. Pang, Z. Li, X. Luo, J. Alvin, R. Saengchan, A. A. Fadila, K. Yanagisawa, Y. Zhang, Z. Chen, Z. Huang, X. Gu, R. Wu, Y. Wang, D. You, B. Liu, Z. Sun, Y. Zhang, H. Huang, N. Oshima, K. Motoi, S. Hori, K. Kunihiro, T. Kaneko, A. Shirane, and K. Okada, "A CMOS dual-polarized phased-array beamformer utilizing cross-polarization leakage cancellation for 5G MIMO systems," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 4, pp. 1310–1326, Jan. 2021.

[29] M. Elkhouly, J. Ha, M. J. Holyoak, D. Hendry, M. Sayginer, R. Enright, I. Kimionis, Y. Baeyens, and S. Shahramian, "Fully integrated 2D scalable TX/RX chipset for D-band phased-array-on-glass modules," in *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, vol. 65, San Francisco, CA, USA, Feb. 2022, pp. 76–78.

[30] K. K. W. Low, S. Zihir, T. Kanar, and G. M. Rebeiz, "A 27–31-GHz 1024-element Ka-band SATCOM phased-array transmitter with 49.5-dBW peak EIRP, 1-dB AR, and ±70° beam scanning," *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 3, pp. 1757–1768, Mar. 2022.

[31] M. Boers, B. Afshar, I. Vassiliou, S. Sarkar, S. T. Nicolson, E. Adabi, B. G. Perumana, T. Chalvatzis, S. Kavvadias, P. Sen, W. L. Chan, A. H.-T. Yu, A. Parsa, M. Nariman, S. Yoon, A. G. Besoli, C. A. Kyriazidou, G. Zochios, J. A. Castaneda, T. Sowlati, M. Rofougaran, and A. Rofougaran, "A 16TX/16RX 60 GHz 802.11ad chipset with single coaxial interface and polarization diversity," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3031–3045, Dec. 2014.

[32] J. D. Dunworth *et al.*, "A 28GHz bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment," in *2018 IEEE*

International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, Feb. 2018, pp. 70–72.

[33] B. Rupakula, S. Zihir, and G. M. Rebeiz, "Low complexity 54–63-GHz transmit/receive 64- and 128-element 2-D-scanning phased-arrays on multilayer organic substrates with 64-QAM 30-Gbps data rates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 12, pp. 5268–5281, Dec. 2019.

[34] W. Shin, B.-H. Ku, O. Inac, Y.-C. Ou, and G. M. Rebeiz, "A 108–114 GHz 4 $\times$4 wafer-scale phased array transmitter with high-efficiency on-chip antennas," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2041–2055, Sept. 2013.

[35] D. del Rio *et al.*, "A D-band 16-element phased-array transceiver in 55-nm BiCMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 2, pp. 854–869, Feb. 2023.

[36] T. Hagiwara, N. Yamaki, K. Sekine, H. Sakai, K. Sahara, K. Takano, S. Hara, S. Lee, R. Dong, S. Tanoi, S. Kubo, S. Miura, A. Kasamatsu, T. Yoshida, S. Amakawa, K. Sakakibara, Y. Umeda, and M. Fujishima, "A 258-GHz CMOS transmitter with phase-shifting architecture for phased-array systems," in *2021 IEEE MTT-S International Microwave Symposium (IMS)*, Atlanta, GA, USA, Jun. 2021, pp. 705–708.

[37] S. Li, Z. Zhang, and G. M. Rebeiz, "An eight-element 136–147 GHz wafer-scale phased-array transmitter with 32 dBm peak EIRP and >16 Gbps 16QAM and 64QAM operation," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 6, pp. 1635–1648, Jun. 2022.

[38] Y. Yang, O. D. Gurbuz, and G. M. Rebeiz, "An eight-element 370–410-GHz phased-array transmitter in 45-nm CMOS SOI with peak EIRP of 8–8.5 dBm," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4241–4249, Dec. 2016.

[39] X.-D. Deng, Y. Li, J. Li, C. Liu, W. Wu, and Y.-Z. Xiong, "A 320-GHz 1×4 fully integrated phased array transmitter using 0.13-μm SiGe BiCMOS technology," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 6, pp. 930–940, Nov. 2015.

[40] I. Jaffri, A. B. Ayed, A. M. Darwish, and S. Boumaiza, "High-frequency vector-modulated signal generation using frequency-multiplier-based RF beamforming architecture," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, USA, Jun. 2020, pp. 551–554.

[41] A. Ben Ayed, I. Jaffri, M. ElAdwy, A. M. Darwish, P. Mitran, and S. Boumaiza, "Analysis and linearization of frequency-multiplier-based RF beamforming transmitters over a wide steering range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 8, pp. 3987–4001, Aug. 2022.

[42] T.-Y. Yang and H.-K. Chiou, "A 25–75 GHz miniature double balanced frequency doubler in 0.18-μm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 4, pp. 275–277, Mar. 2008.

[43] C. Mao, C. S. Nallani, S. Sankaran, E. Seok, and K. K. O, "125-GHz diode frequency doubler in 0.13-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1531–1538, May 2009.

[44] J. Deng, Y. Yang, Z. Zhu, and X. Luo, "A 140–220-GHz balanced doubler with 8.7%–12.7% efficiency," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 6, pp. 515–517, Apr. 2018.

[45] A. Y.-K. Chen, Y. Baeyens, Y.-K. Chen, and J. Lin, "A 36–80 GHz high gain millimeter-wave double-balanced active frequency doubler in SiGe BiCMOS," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 9, pp. 572–574, Sept. 2009.

[46] Y. Zhu, H. Ghaleb, V. Rieß, N. Joram, and F. Ellinger, "A 60 GHz frequency doubler with 3.4-dBm output power and 4.4% DC-to-RF-efficiency in 130-nm SiGe BiCMOS," in *2021 16th European Microwave Integrated Circuits Conference (EuMIC)*, London, United Kingdom, Apr. 2022, pp. 100–103.

[47] B. Sutbas and G. Kahmen, "A 7.2-mW V-band frequency doubler with 14% total efficiency in 130-nm SiGe BiCMOS," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 579–582, Jun. 2022.

[48] F. Ellinger and H. Jackel, "Ultracompact SOI CMOS frequency doubler for low power applications at 26.5-28.5 GHz," *IEEE Microwave and Wireless Components Letters*, vol. 14, no. 2, pp. 53–55, Feb. 2004.

[49] L. Wang, Y.-Z. Xiong, B. Zhang, S.-M. Hu, and T.-G. Lim, "Millimeter-wave frequency doubler with transistor grounded-shielding structure in 0.13-μm SiGe BiCMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1304–1310, May 2011.

[50] I. Abdo, K. K. Tokgoz, T. Fujimura, K. Okada, and A. Matsuzawa, "A 100–123GHz CMOS frequency doubler with 5.5dBm output power and high fundamental rejection," in *2017 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Seoul, Korea (South), Aug. 2017, pp. 138–140.

[51] Y. Ye, B. Yu, A. Tang, B. Drouin, and Q. J. Gu, "A high efficiency E-band CMOS frequency doubler with a compensated transformer-based balun for matching enhancement," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 1, pp. 40–42, Dec. 2016.

[52] G. Liu, J. Jayamon, J. Buckwalter, and P. Asbeck, "Frequency doublers with 10.2/5.2 dBm peak power at 100/202 GHz in 45nm SOI CMOS," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Phoenix, USA, May 2015, pp. 271–274.

[53] Z. Chen, Y. Yu, Y. Wu, H. Liu, C. Zhao, and K. Kang, "A 19.5% efficiency 51–73-GHz high-output power frequency doubler in 65-nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 29, no. 12, pp. 818–821, Nov. 2019.

[54] C. So and S. Hong, "A V-band differential push–push frequency doubler with a current-reuse gm-boosted buffer," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 3, pp. 299–302, Mar. 2023.

[55] H. Fu, H. Wang, and K. Ma, "A high conversion gain frequency doubler using transformer-based second harmonic feedback technique in 28-nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 9, pp. 1071–1074, Apr. 2022.

[56] J. Oh, J. Jang, C.-Y. Kim, and S. Hong, "A W-band high-efficiency CMOS differential current-reused frequency doubler," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 5, pp. 307–309, Mar. 2015.

[57] W. Lee and A. Valdes-Garcia, "W-band SiGe frequency doubler with optimum harmonic termination for 14% efficiency," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 3, pp. 272–275, Jan. 2021.

[58] X. Wu, Z. Kang, Y. Wang, and L. Wu, "A 53–78 GHz complementary push–push frequency doubler with implicit dual resonance for output power combining," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1–12, Dec. 2022.

[59] J. Jang, H. Lim, and T. W. Kim, "A CMOS complementary common gate capacitive cross-coupled frequency doubler," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 9, pp. 3694–3698, May 2022.

[60] S. Li, T. Chi, T.-Y. Huang, M.-Y. Huang, D. Jung, and H. Wang, "A buffer-less wideband frequency doubler in 45-nm CMOS-SOI with transistor multiport waveform shaping achieving 25% drain efficiency and 46–89 GHz instantaneous bandwidth," *IEEE Solid-State Circuits Letters*, vol. 2, no. 4, pp. 25–28, Apr. 2019.

[61] F. Giannini and G. Leuzzi, *Nonlinear Microwave Circuit Design.* John Wiley & Sons Ltd, 2004.

[62] H.-C. Lin and G. M. Rebeiz, "A 135–160 GHz balanced frequency doubler in 45 nm CMOS with 3.5 dBm peak power," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, Tampa, FL, USA, Jun. 2014, pp. 1–4.

[63] J. Sharma, T. Dinc, and H. Krishnaswamy, "A 134 GHz +4 dBm frequency doubler at $f_{\max}$ in 130 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 11, pp. 784–786, Nov. 2014.

[64] C. Coen, S. Zeinolabedinzadeh, M. Kaynak, B. Tillack, and J. D. Cressler, "A highly-efficient 138–170 GHz SiGe HBT frequency doubler for power-constrained applications," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, USA, May 2016, pp. 23–26.

[65] M. M. Pirbazari and A. Mazzanti, "High gain 130-GHz frequency doubler with colpitts output buffer delivering pout up to 8 dBm with 6% PAE in 55-nm SiGe BiCMOS," *IEEE Solid-State Circuits Letters*, vol. 4, pp. 36–39, Jan. 2021.

[66] M. Möck, I. K. Aksoyak, and A. C. Ulusoy, "A high-efficiency D-band frequency doubler in 22-nm FDSOI CMOS," in *2022 17th European Microwave Integrated Circuits Conference (EuMIC)*, Milan, Italy, Sept. 2022, pp. 272–275.

[67] P.-H. Tsai, Y.-H. Lin, J.-L. Kuo, Z.-M. Tsai, and H. Wang, "Broadband balanced frequency doublers with fundamental rejection enhancement using a novel compensated marchand balun," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 5, pp. 1913–1923, May 2013.

[68] Z. Yang, K. Ma, F. Meng, and B. Liu, "A 120-GHz class-F frequency doubler with 7.8-dBm Pout in 55-nm bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 8, pp. 2173–2188, Aug. 2023.

[69] H. Fu, K. Li, and K. Ma, "A 208–233-GHz frequency doubler with 1.1% power-added efficiency in 28-nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 11, pp. 1311–1314, Nov. 2022.

[70] N. Oz and E. Cohen, "A compact 105–130 GHz push-push doubler, with 4dBm Psat and 18% efficiency in 28nm CMOS," in *2015 10th European Microwave Integrated Circuits Conference (EuMIC)*, Paris, France, Sept. 2015, pp. 101–104.

[71] K. Wu, S. Muralidharan, and M. M. Hella, "A wideband SiGe BiCMOS frequency doubler with 6.5-dBm peak output power for millimeter-wave signal sources," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 1, pp. 187–200, Jan. 2018.

[72] S. G. Rao, M. Frounchi, and J. D. Cressler, "Triaxial balun with inherent harmonic reflection for millimeter-wave frequency doublers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 6, pp. 2822–2831, Sept. 2021.

[73] M. Ko, M. Hussein Eissa, J. Borngräber, A. Cağri Ulusoy, and D. Kissinger, "110–135 GHz SiGe BiCMOS frequency quadrupler based on a single gilbert cell," in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Madrid, Spain, Sept. 2018, pp. 101–104.

[74] M. Kucharski, M. H. Eissa, A. Malignaggi, D. Wang, H. J. Ng, and D. Kissinger, "D-band frequency quadruplers in BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2465–2478, Sept. 2018.

[75] E. Öjefors, B. Heinemann, and U. R. Pfeiffer, "Active 220- and 325-GHz frequency multiplier chains in an SiGe HBT technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1311–1318, May 2011.

[76] Z. Li, J. Chen, D. Tang, R. Zhou, and W. Hong, "A 205–273-GHz frequency multiplier chain ($\times$ 6) with 9-dBm output power and 1.92% DC-to-RF efficiency in 0.13- μ m SiGe BiCMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 7, pp. 2909–2919, Jul. 2023.

[77] N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "235–275 GHz (x16) frequency multiplier chains with up to 0 dBm peak output power and low DC power consumption," in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, Tampa, FL, USA, Jun. 2014, pp. 181–184.

[78] T. Chi, J. Papapolymerou, and H. Wang, "A +2.3dBm 124–158GHz class-C frequency quadrupler with folded-transformer based multi-phase driving," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Phoenix, AZ, USA, May 2015, pp. 263–266.

[79] B.-H. Ku, H. Chung, and G. M. Rebeiz, "A milliwatt-level 70–110 GHz frequency quadrupler with >30 dBc harmonic rejection," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 5, pp. 1697–1705, May 2020.

[80] J. Yu, J. Chen, Z. Li, D. Hou, Z. Chen, and W. Hong, "A 212–260 GHz broadband frequency multiplier chain (×4) in 130-nm BiCMOS technology," in *2021 IEEE MTT-S International Microwave Symposium (IMS)*, Atlanta, GA, USA, Jun. 2021, pp. 454–457.

[81] J. Xia and S. Boumaiza, "Digitally assisted 28 GHz active phase shifter with 0.1 dB/0.5° RMS magnitude/phase errors and enhanced linearity," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 914–918, Jun. 2019.

[82] Y. Xiong, X. Zeng, and J. Li, "A frequency-reconfigurable CMOS active phase shifter for 5G mm-wave applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 10, pp. 1824–1828, Oct. 2020.

[83] J. Park, G. Jeong, and S. Hong, "A Ka-band variable-gain phase shifter with multiple vector generators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 6, pp. 1798–1802, Jun. 2021.

[84] G.-S. Shin, J.-S. Kim, H.-M. Oh, S. Choi, C. W. Byeon, J. H. Son, J. H. Lee, and C.-Y. Kim, "Low insertion loss, compact 4-bit phase shifter in 65 nm CMOS for 5G applications," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 1, pp. 37–39, Jan. 2016.

[85] M. Elkholy, S. Shakib, J. Dunworth, V. Aparin, and K. Entesari, "Low-loss highly linear integrated passive phase shifters for 5G front ends on bulk CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 10, pp. 4563–4575, Oct. 2018.

[86] J.-H. Tsai, Y.-L. Tung, and Y.-H. Lin, "A 27–42-GHz low phase error 5-bit passive phase shifter in 65-nm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 9, pp. 900–903, Sept. 2020.

[87] W. H. Woods, A. Valdes-Garcia, H. Ding, and J. Rascoe, "CMOS millimeter wave phase shifter based on tunable transmission lines," in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, San Jose, CA, USA, Sept. 2013, pp. 1–4.

[88] Y. Tousi and A. Valdes-Garcia, "A Ka-band digitally-controlled phase shifter with sub-degree phase precision," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, USA, May 2016, pp. 356–359.

[89] M. Tabesh, A. Arbabian, and A. Niknejad, "60GHz low-loss compact phase shifters using a transformer-based hybrid in 65nm CMOS," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA, USA, Sept. 2011, pp. 1–4.

[90] H. Krishnaswamy, A. Valdes-Garcia, and J.-W. Lai, "A silicon-based, all-passive, 60 GHz, 4-element, phased-array beamformer featuring a differential, reflection-type phase shifter," in *2010 IEEE International Symposium on Phased Array Systems and Technology*, Waltham, MA, USA, Oct. 2010, pp. 225–232.

[91] F. Meng, K. Ma, K. S. Yeo, S. Xu, C. C. Boon, and W. M. Lim, "Miniaturized 3-bit phase shifter for 60 GHz phased-array in 65 nm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 1, pp. 50–52, Jan. 2014.

[92] W.-T. Li, M.-H. Wu, J.-H. Cheng, and T.-W. Huang, "A 57-to-64 GHz ultra-compact 0.027 mm^2 reflection type phase shifter with low insertion loss," in *2014 11th European Radar Conference*, Rome, Italy, Oct. 2014, pp. 431–434.

[93] R. Garg and A. S. Natarajan, "A 28-GHz low-power phased-array receiver front-end with 360° RTPS phase shift range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4703–4714, Nov. 2017.

[94] T.-W. Li and H. Wang, "A millimeter-wave fully integrated passive reflection-type phase shifter with transformer-based multi-resonance loads for 360° phase shifting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 4, pp. 1406–1419, Apr. 2018.

[95] P. Gu and D. Zhao, "Geometric analysis and systematic design of a reflective-type phase shifter with full 360° phase shift range and minimal loss variation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 10, pp. 4156–4166, Oct. 2019.

[96] Y. Liu, G. Liu, and P. M. Asbeck, "High-order modulation transmission through frequency quadrupler using digital predistortion," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 6, pp. 1896–1910, Jun. 2016.

[97] S. Maas, *Nonlinear Microwave and RF Circuits, Second Edition.* Artech, 2003.

[98] N. Messaoudi, A. B. Ayed, J.-P. Teyssier, and S. Boumaiza, "VNA-based testbed for accurate linearizability testing of power amplifiers under modulated signals," in *2022 99th ARFTG Microwave Measurement Conference (ARFTG)*, Denver, USA, Jun. 2022, pp. 1–4.

[99] Y. Tousi and A. Valdes-Garcia, "A Ka-band digitally-controlled phase shifter with sub-degree phase precision," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, USA, May 2016, pp. 356–359.

[100] J. S. Park and H. Wang, "A transformer-based poly-phase network for ultra-broadband quadrature signal generation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 12, pp. 4444–4457, Dec. 2015.

[101] J. Kim, Y. Lim, H. Yoon, Y. Lee, H. Park, Y. Cho, T. Seong, and J. Choi, "An ultra-low-jitter, mmW-band frequency synthesizer based on digital subsampling PLL using optimally spaced voltage comparators," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3466–3477, Dec. 2019.

[102] C. Clark, A. Moulthrop, M. Muha, and C. Silva, "Transmission response measurements of frequency-translating devices using a vector network analyzer," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 12, pp. 2724–2737, Dec. 1996.

[103] M. E. Knox, "A novel technique for characterizing the absolute group delay and delay linearity of frequency translation devices," in *53rd ARFTG Microw. Meas. Conf. (ARFTG)*, vol. 35, Anaheim, CA, USA, Jun. 1999, pp. 1–7.

[104] M. L. Truong, "Increased accuracy of absolute group delay measurements," *Microw. J,*, vol. 42, no. 9, p. 150, Sep. 2000.

[105] W. Liancheng, "The research on mixer vector characteristic measurement based on de-embedding," in *IEEE Int. Conf. Microw. and Millimeter Wave Tech. (ICMMT)*, vol. 1, Beijing, China, Jun. 2016, pp. 195–197.

[106] J. P. Dunsmore, *Handbook of Microwave Component Measurements with advanced VNA techniques.* John Wiley & amp; Sons, Inc, 2020.

[107] Y. Guo and S. Li, "Frequency converting device measurement," in *Chi. J. Sci.*, vol. 31, Aug. 2010, pp. 294–294.

[108] O. Inac, M. Uzunkol, and G. M. Rebeiz, "45-nm CMOS SOI technology characterization for millimeter-wave applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 6, pp. 1301–1311, Jun. 2014.

[109] H.-T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and design of stacked-FET millimeter-wave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1543–1556, Apr. 2013.

[110] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A low-cost scalable 32-element 28-GHz phased array transceiver for 5G communication links based on a 2 x 2 beamformer flip-chip unit cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, Jan. 2018.

[111] W. Lee, J.-O. Plouchart, C. Ozdag, Y. Aydogan, M. Yeck, A. Cabuk, A. Kepkep, S. K. Reynolds, E. Apaydin, and A. Valdes-Garcia, "Fully integrated 94-GHz dual-polarized TX and RX phased array chipset in SiGe BiCMOS operating up to 105 °C," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2512–2531, Sept. 2018.

[112] F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90-100-GHz 4 x 4 SiGe BiCMOS polarimetric transmit/receive phased array with simultaneous receive-beams capabilities," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 3099–3114, Aug. 2013.

[113] S. Yuan and H. Schumacher, "Compact V band frequency doubler with true balanced differential output," in *2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Bordeaux, France, Sept. 2013, pp. 191–194.