A High-Resolution Direct-Conversion CMOS X-Ray Imager with Code-Division-Multiplexed Readout

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

This thesis presents the design and characterization of a high-spatial-resolution direct-conversion X-ray imager built using complementary metal-oxide-semiconductor (CMOS) technology integrated with an amorphous-selenium photoconductor. Our imager targets applications such as dark field X-ray microscopy and aims to improve the performance of existing imagers by reducing pixel size, and increasing conversion efficiency and frame rate.

We achieve high spatial resolution by reducing the pixel size of the imager. We present the design of a 2.252 μm $\times$ 2.363 μm two-transistor passive-pixel-sensor (PPS) array using analog code-division-multiplexed (CDM) readout. The PPS allows us to reduce the number of components in the pixel and reduce its size. The major drawback of using the PPS is low signal-to-noise ratio (SNR) due to the large column capacitance. To overcome the low SNR, we implement analog CDM readout which enables a longer effective integration time. Our design also contains a column-parallel dual integrator and switched-capacitor difference amplifier (SCDA) to implement the CDM readout. We also show how the pixel size, frame rate, and readout resolution design specifications are met.

We implement our imager in a 180-nm CMOS process and also discuss the design of external hardware to operate the imager. Our preliminary experimental results focus on the characterization of the imager readout circuit. Specifically, we present the measured response of the integrator and SCDA and compare these to simulation results. We also suggest improvements for future iterations of the imager.

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Dedication

This is dedicated to my grandparents Ebrahim Ahmed Lakhani, Zaherali Karim Kurji, Dolatkhanu Ebrahim Lakhani, and Khatija Zaherali Kurji.

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Chapter 1

Introduction

X-ray imaging has developed alongside optical imaging and is widely used in the medical, veterinary, non destructive test, and scientific imaging fields. In medical imaging, X-rays are commonly used for projection radiography and computed tomography (CT). The images formed using these techniques result from variations in X-ray intensity due to the X-ray attenuation properties of different materials in the human body. Projection radiography captures a two-dimensional map of the varying X-ray intensities. CT captures multiple images taken at different angles to construct a three-dimensional image of the body [11].

X-ray imaging is also used for non-biological materials characterization, and conventional techniques pose some limitations on the material study [12]. The use of nanotechnology in commercial applications and research is continuously rising as nanomaterials offer unique properties that bulk materials do not. Studying the material structure can provide fundamental information about imperfections and mechanisms involved in the material's formation. As an example, recent advances in structural microscopy techniques have led to the creation of dark field X-ray microscopy (DFXM) that provides a full-field, non-destructive image of embedded grain structures with resolutions on the order of 100 nm [13]. This resolution is achieved by placing X-ray optics in the diffracted beam which provides a spatial mapping of the diffracting grain [13]. The challenge using this technique

is to overcome the low efficiency of X-ray optics, which involves using longer integration times. However, this results in lower resolution due to the mechanical instabilities present in instruments, thus diminishing the advantages of the DFXM technique [13]. To address this low-signal issue, either a higher photon flux at the sample is required, or a higher-efficiency, high-resolution detector is required. The first is problematic since applying a condenser lens to increase flux will reduce the sample field of view, indicating that efficiency improvements in high-resolution detectors are sorely needed [12][13]. Other techniques that can benefit from this include Bragg coherent diffraction imaging, ptychography, and near-field-diffraction microscopy.

This thesis focuses on the design and characterization of the world's highest -spatial-resolution direct conversion X-ray imager. The imager is built by integrating micron-scale complementary metal-oxide-semiconductor (CMOS) technology with an amorphous selenium X-ray photoconductor. Our imager is specifically targeted towards applications such as DFXM by providing a high resolution, high efficiency solution for X-ray photon energies > 20 keV.

1.1 X-Ray Physics and Imaging

X-rays are a type of electromagnetic radiation discovered in 1895 by Wilhelm Konard Rontgen [1] having wavelengths ranging from 0.01 nm to 10 nm [5]. X-rays are typically classified as "hard" or"soft", depending on the photon energy level. Hard X-rays typically correspond to photons with energies above 2 keV, whereas soft X-rays have energies below 2 keV [14].

1.1.1 X-Ray Generation

X-rays can be generated using an X-ray tube, as illustrated in Figure 1.1, or by using synchrotron radiation, as illustrated in Figure 1.2. An X-ray tube operates as follows. A tungsten filament is heated using an electric current, and thermionic emission occurs

when the filament reaches a specific temperature. The emitted electron is then accelerated towards a target made from tungsten or molybdenum using an electric field created by applying a potential difference across the cathode and anode [5]. The electrons strike the target and emit an X-ray photon.

Most photons emitted are due to Bremsstrahlung radiation, the process by which photon emission results from an electron being slowed or deflected when travelling near atomic nuclei. These photons have lower energy than the travelling electron responsible for producing it [4]. Photons of the same energy are emitted because electrons collide with an atom's nucleus. Photons can also be emitted because of characteristic radiation. This occurs when the travelling electron transfers a portion of its kinetic energy to a bound electron creating a vacancy. A photon is then emitted when a higher state electron fills this vacancy [4].

These three methods of photon emission create an X-ray spectrum shaped using a filter typically made of aluminum and placed between the X-ray tube and the object being imaged. This filter removes lower-energy photons and characteristic radiation that would otherwise be absorbed by the object being imaged [4].

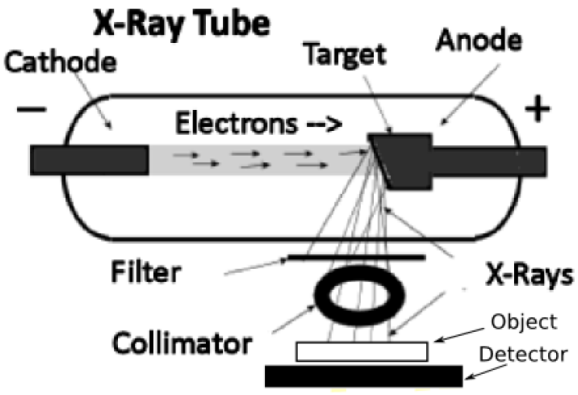


Figure 1.1: Illustration of an X-ray tube to generate X-ray photons (taken from [1]).

X-rays generated using synchrotron radiation are emitted by electrons travelling at high speeds in a circular path controlled by magnetic fields. The process begins by using

an electron gun, where a heated element produces free electrons which travel in a steady stream through a hole using an electric field [15]. The stream of electrons passes through a linear accelerator such that it travels close to the speed of light. The electrons are then fed into a booster ring, where magnetic fields force the stream of electrons along a circular path. The stream is then fed into a storage ring kept under vacuum to prevent molecules from deflecting the beam [15]. Finally, bending magnets deflect the electron beam, and synchrotron radiation is emitted. Machines can also be used to filter and intensify synchrotron radiation. X-rays generated using synchrotron radiation have a larger brilliance (a measure of the beam's brightness in a given area) than the conventional X-ray tube described above [15].

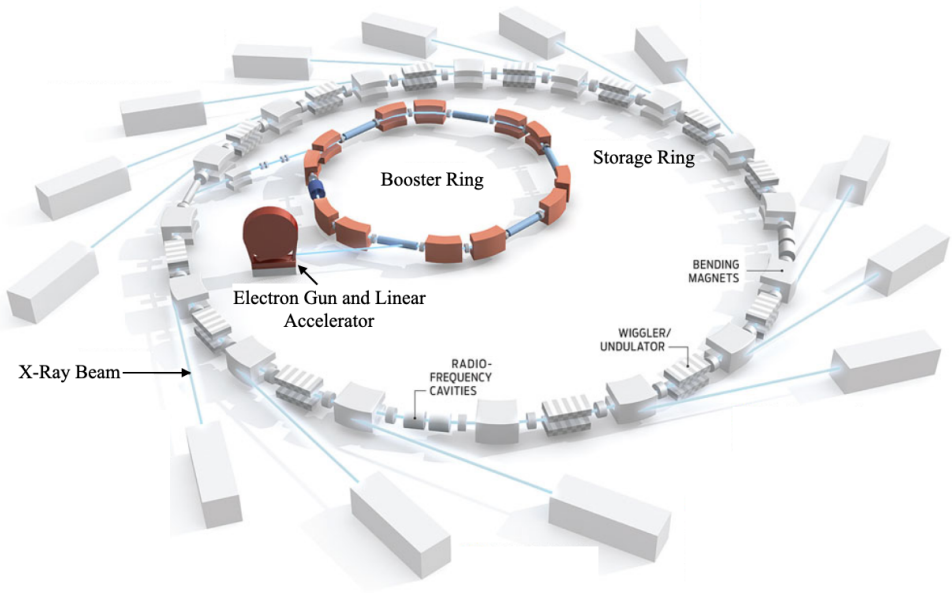


Figure 1.2: Illustration of a synchrotron (adapted from [2]).

1.1.2 X-Ray Imagers

Figure 1.3 illustrates the general structure of a CMOS digital imager. It contains a pixel array, vertical access circuitry (row-select circuits), horizontal access circuitry (column

multiplexers), a readout circuit, and an ADC. Typical CMOS imagers use silicon as a photodiode to absorb visible light. X-ray imagers are hybrid imagers which overlay a material directly on top of the pixel array so that X-ray photons can be absorbed and collected.

X-ray imagers can be categorized based on how X-rays are converted into electron-hole pairs (EHPs). The two categories are indirect conversion and direct conversion, as illustrated in Figure 1.4. To absorb X-ray photons, imagers require either a scintillator material and photodiode for indirect conversion, or a direct-conversion material with a specific thickness [16].

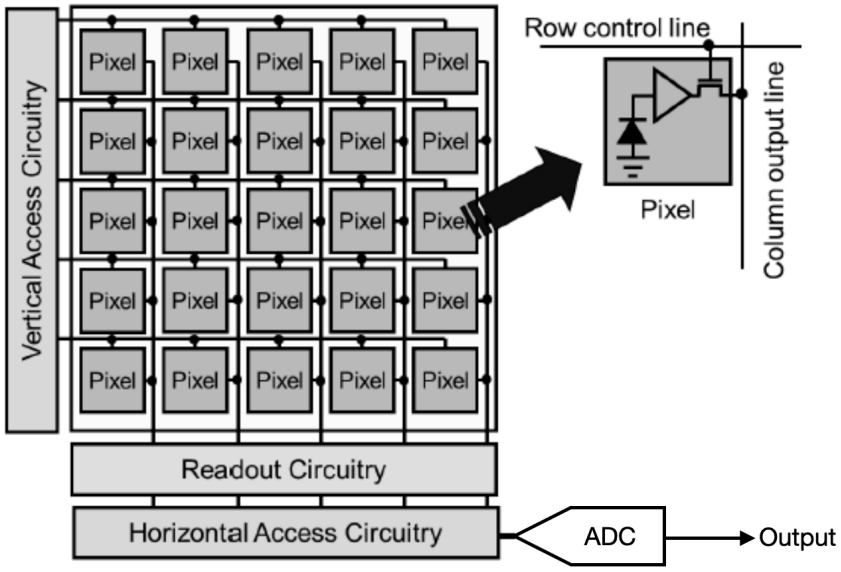


Figure 1.3: General structure of a digital imager (adapted from [3]).

Indirect Conversion

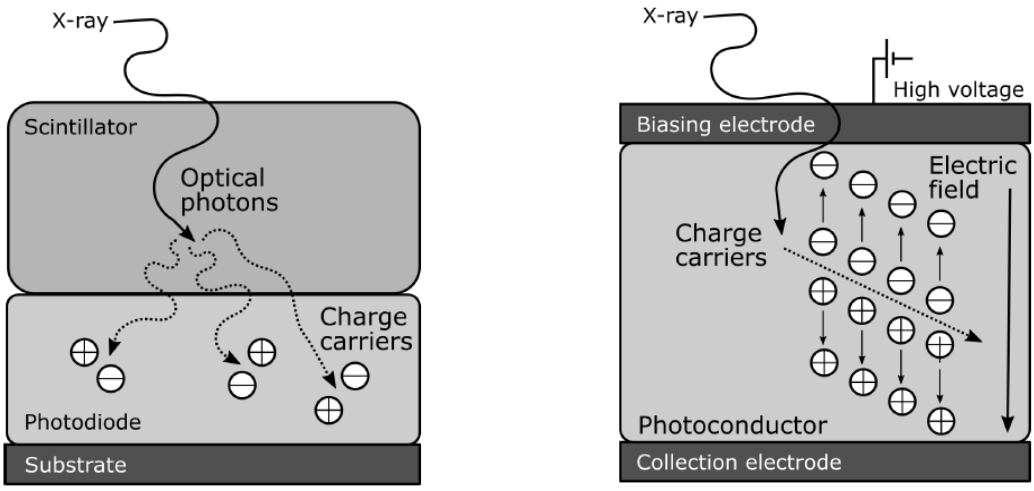
Indirect-conversion imagers use scintillators, such as CsI, to convert X-ray photons into optical photons, which are then collected by a photodiode. Scintillators typically have high X-ray absorption efficiency, but suffer from a loss of spatial resolution due to optical scat-

tering. The only method to achieve higher resolution is to thin the scintillator. Thinning the scintillator enables a reduction in optical scattering, but reduces the material's X-ray absorption efficiency [4]. An indirect-conversion imager typically yields a pixel pitch of 50 μm or larger [17]. State of the art indirect conversion scientific CMOS X-ray imagers can achieve micron scale spatial resolutions but at very low (e.g. 0.01 %) X-ray quantum efficiencies.

Direct Conversion

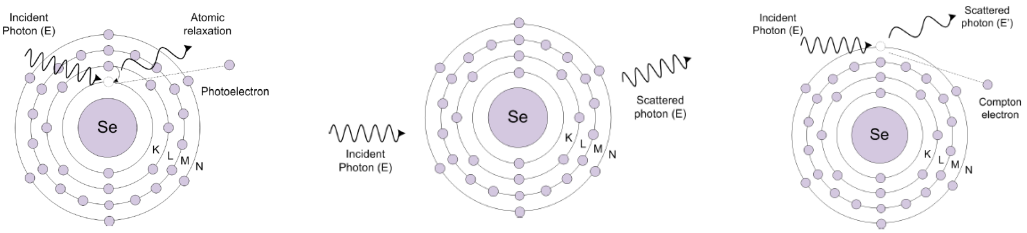
Direct-conversion imagers use photoconductive materials such as amorphous selenium (a-Se), CdZnTe, HgI_2, PbI_2, and PbO, which directly convert X-rays into EHPs. Applying a bias voltage across the photoconductive material helps facilitate the collection of the generated charge carriers at the collection electrode while preserving spatial resolution since the charge is guided by the electric field to stay within the pixel. In order to reduce dark current, a blocking layer can be placed between the collecting electrode and the photoconductive material [4]. The resolution of direct-conversion imagers depends on the spread of EHPs in the photoconductive material generated by an incident photon [5].

X-ray photons incident on the photoconductive material will interact through either the photoelectric effect, Rayleigh scattering, or Compton scattering, as illustrated in Figure 1.5 [5]. The photoelectric effect is the primary method in which EHPs are generated within the photoconductive material. This occurs when an inner shell electron absorbs the energy of an incident X-ray photon and is ejected. An outer shell electron can then fill the vacancy of the ejected inner shell electron, releasing a characteristic photon which can interact with the photoconductive material in a similar manner. Rayleigh scattering occurs when the incident photon is scattered by the atom and does not lose its energy. Compton scattering occurs when the incident X-ray photon ejects an outer shell electron and is subsequently scattered with less energy [5].



(a) (b)

Figure 1.4: (a) Illustration of an indirect-conversion X-ray imager using a scintillator and a photodiode. (b) Illustration of a direct-conversion X-ray imager using a photoconductor with an applied bias (taken from [4]).



(a) (b) (c)

Figure 1.5: (a) X-ray photon interaction via the photoelectric effect. (b) X-ray photon undergoing Rayleigh scattering upon interaction with photoconductive material. (c) X-ray photon undergoing Compton scattering upon interaction with photoconductive material (taken from [5]).

Amorphous Selenium

A-Se is a direct-conversion material widely used in X-ray imaging and exhibits an intrinsically high spatial resolution [18]. It is relatively inexpensive and can be uniformly deposited over large areas with thicknesses up to 1 mm. Another beneficial property of

a-Se is that it exhibits low dark current (< 10 pA/mm^2) compared to other commonly used photoconductors. That is, the thermal generation of charge carriers is low [18]. It is important to consider the dark current due to charge injection from the bias electrodes. In a-Se, the dark current is dominated by hole injection [19].

Given that the charge conversion of a-Se is lower than that of other commonly-used photoconductors due to its high ionization energy (45-50 eV), an applied field of 10 V/µm or higher is typically used to achieve better charge-conversion efficiency [18]. Mitigating the injection of charge carriers is important as the increase in dark current will reduce the imager's dynamic range. As such, a blocking layer like polyimide (PI) is used at the positively biased electrode to reduce hole injection in a-Se. Additionally, using PI as the blocking layer helps with a-Se stability by inhibiting crystallization [18].

Resolution of a-Se

The main objective of our work is to improve the spatial resolution of direct-conversion X-ray imager. This is difficult to achieve using a scintillator. One of the main disadvantages of scintillators is that the optical photons generated spread into adjacent pixels. Thinning the scintillator reduces this effect, but negatively impacts the material's X-ray absorption. Using a-Se helps enable a high-resolution X-ray image sensor. The deposition of a-Se on top of the custom CMOS chip allows for a fill factor close to 100%. Pairing this with a-Se's high quantum efficiency at specific photon energies, the majority of photons incident on the image sensor are collected and converted into EHPs. As such, high-quality images can be obtained using smaller X-ray doses. Figure 1.6 shows the theoretical MTF for a-Se at two different thicknesses and two different X-ray incident angles. This shows the theoretical inherent resolution of the a-Se layer.

The following mechanisms can negatively impact the resolution of a-Se [6]:

1. Image blurring can occur due to charge clouds created where the X-ray photon is converted into an EHP. The charge cloud can increase in size because of diffusion or repulsion from like charges.

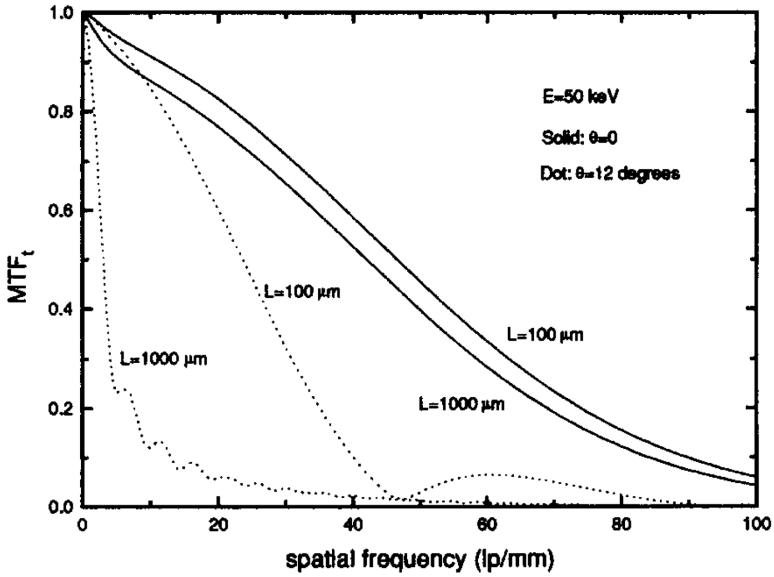


Figure 1.6: A-Se theoretical MTF to show inherent spatial resolution at different thicknesses and X-ray incident angles of 0° and 12° (taken from [6]).

2. Characteristic photons released when an inner shell vacancy is filled can be re-absorbed away from the location where the X-ray photon was absorbed.

3. Scattered photons emitted due to Compton scattering can be re-absorbed away from the location where the X-ray photon was absorbed.

4. A lateral electric field can be produced in the a-Se due to non-uniform charge distribution on the surface, causing EHPs to move laterally.

1.2 Pixel Architectures

Two basic pixel architectures are employed in CMOS digital imagers: the passive pixel sensor (PPS) and the active pixel sensor (APS). Choosing one architecture over the other depends on the imager design specifications. Indirect-conversion imagers make use of the CMOS photodiode pixel array as the light being collected from the circuit is in the visible

range. Direct-conversion imagers replace the silicon photdiode with a sensor material that can absorb X-ray photons. The X-ray sensor material is connected to the CMOS pixel array.

1.2.1 Passive Pixel Sensor

The PPS shown in Figure 1.7 contains a photodiode, PD, with its device capacitance C_{PD}, and a single NMOS transistor switch, M_{SEL}. The sensor is first exposed to light for a specific duration (integration time). During this phase of operation, a low voltage is applied to the gate of M_{SEL} such that it operates in the cutoff region (switch is "off"). The photodiode converts the incident photons into EHPs, and the charge is stored on C_{PD}. After the integration period, a voltage is applied to the gate of M_{SEL} such that it operates in the triode region (switch is "on"). The accumulated charge is then transferred to the feedback capacitor, C_F, using the on-chip column integrator, and the voltage at the output of the integrator is read. The details of charge transfer and readout are discussed in Section 1.3.

The main advantages of the PPS is its simplicity and small size. Given that it only uses a single transistor, the PPS allows the designer to keep the pixel small, which could improve spatial resolution. Second, this architecture allows for a high fill factor (the ratio of photosensitive area of the pixel to the total area of the pixel), resulting in better sensitivity to incident light [1]. Lastly, the PPS has lower pixel-to-pixel fixed-pattern noise (the spatial variation in signal level). This is because the PPS relies on a single transistor and does not have any amplification within the pixel. As such, this architecture is less susceptible to device mismatches from pixel to pixel [7]. However, the major drawback of the PPS is low signal-to-noise ratio (SNR) due to the large column capacitance, C_C, in Figure 1.7 [3].

1.2.2 Active Pixel Sensor

To overcome the SNR issues in the PPS, a CMOS APS implements signal amplification in the pixel but this is only achieved by utilizing more transistors per pixel that takes away

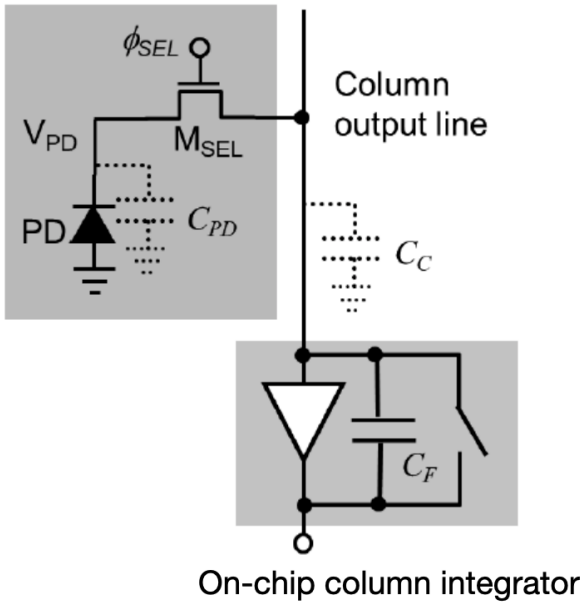


Figure 1.7: PPS using a single transistor and on chip column integrator to read out photodiode charge (adapted from [3]).

from the smallest achievable pixel size. The charge collected is converted to a voltage at the gate of a source-follower instead of directly transferring the charge collected to the column amplifier, as in a PPS. The APS most commonly uses either three transistors (3T) or four transistors (4T), as illustrated in Figure 1.8 and 1.9, respectively.

The 3T-APS in Figure 1.8 contains a transistor switch for reset, M_{RS}, a source-follower transistor, M_{SF}, and a row-select (RS) switch, M_{SEL}. M_{RS} is first turned on to reset the photodiode to V_{dd}. M_{RS} is then switched off, and the integration phase begins, whereby charge carriers that are generated by incident photons accumulate on C_{PD}. This causes the voltage across the photodiode to decrease as a reverse current flows through the diode. After integration, M_{SEL} is switched on, and the voltage across the photodiode (voltage at the gate of M_{SF}) is read out from the column line.

Although the 3T-APS helps to overcome issues affecting the PPS, it suffers from thermal reset noise at the integration node [3]. Furthermore, there is a trade-off between full-well

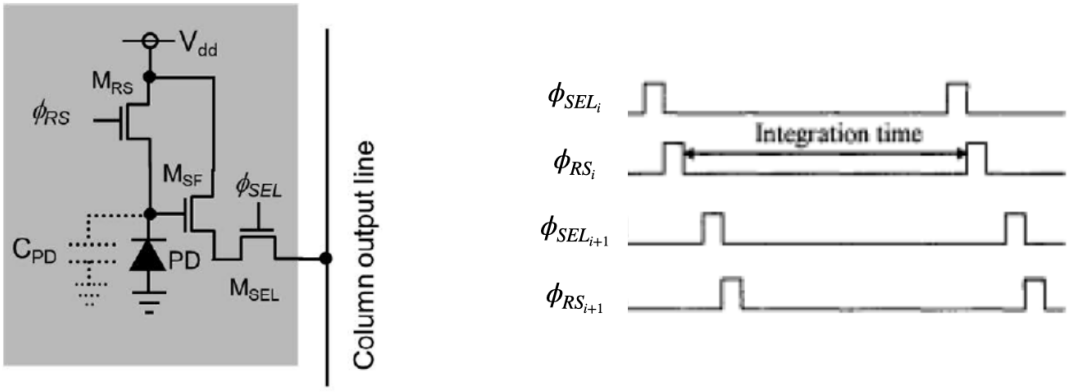


Figure 1.8: 3T APS and its timing diagram (adapted from [3] and [1]).

capacity (maximum amount of charge accumulated in the photodiode) and conversion gain (change in voltage when a single electron or hole is accumulated in the photodiode) in the 3T-APS. This is because the full-well capacity is proportional to the photodiode capacitance, whereas the conversion gain is inversely proportional to this capacitance [3].

The 4T-APS addresses the disadvantages observed with the 3T-APS. A fourth transistor switch, the transfer gate M_{TG}, is added between the photodiode and the gate of M_{SF}. The operation of the 4T-APS is similar to that of the 3T-APS. Before the transfer gate is turned on to transfer the charge from the photodiode to the FD capacitor, this capacitor is reset by switching on M_{RS}, and this reset value is read out. This initial read is the noise and offset from the gate of M_{SF}. The charge is then transferred from the photodiode to the FD capacitor and read out. The final output is the difference of the two readouts from the pixel. As such, the 4T-APS can significantly reduce the amount of low-frequency noise in the pixel compared to the 3T-APS. The 4T-APS also has a trade-off between conversion gain and well capacity as a result of the FD capacitor [3]. The APS structure, in general, has a significantly lower fill factor compared to the PPS because of the additional transistors [3].

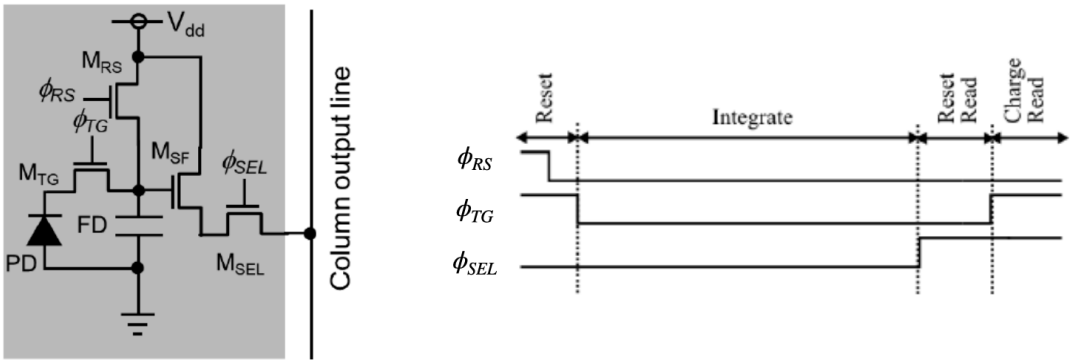


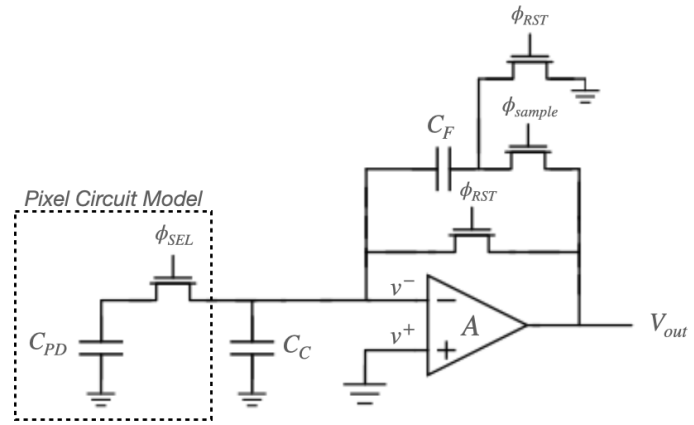
Figure 1.9: 4T APS and its timing diagram (adapted from [3] and [1]).

1.3 Readout Circuits and Methods

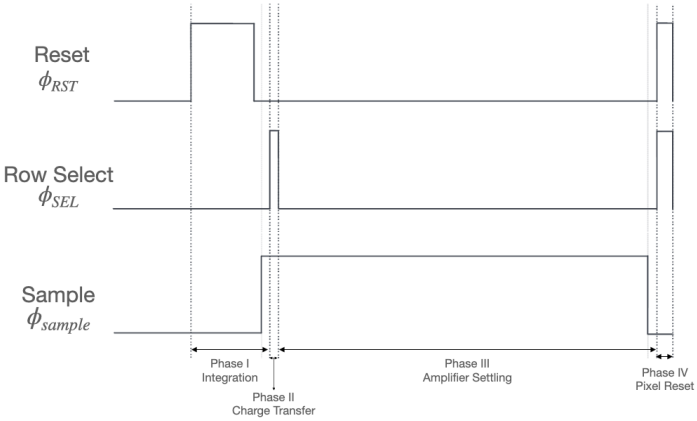
A readout circuit determines the charge accumulated in the pixel. Typically, imagers use time-division multiplexing (TDM) to read out the pixel signal and feed it into an ADC. However, analog code-division multiplexing (CDM) is an alternative readout approach we use in our proposed X-ray imager design.

1.3.1 Integrator

A capacitive-feedback amplifier (integrator) is typically used to convert the charge accumulated on the pixel during the integration time to a voltage that can be digitized by an ADC. A typical integrator is shown in Figure 1.10(a), where the pixel is modelled using C_{PD} and A is the open-loop dc gain of the operational amplifier (opamp). Note that each transistor acts as a switch. The integrator operates in four phases: integration, charge transfer, amplifier settling, and pixel reset [7].



(a)



(b)

Figure 1.10: (a) Pixel and integrator circuit. (b) Timing diagram for integrator operation (adapted from [7]).

In the integration phase, charge accumulates on the pixel capacitor as a result of EHPs being generated due to incident photons. The charge being collected can be modelled as a constant current source, as shown in Figure 1.11. In this phase, the opamp is in unity feedback which resets the charge on C_C and C_F [7].

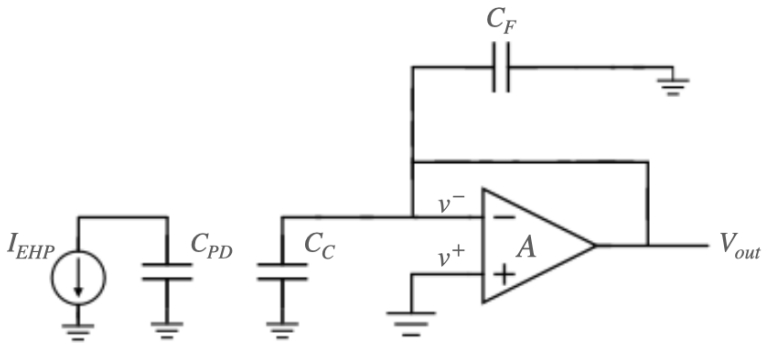


Figure 1.11: Circuit model of the integrator and circuit during the integration phase (adapted from [7]).

In the charge transfer phase shown in Figure 1.12, the charge accumulated, Q_{pixel}, on C_{PD} is shared between C_{PD}, C_C, and C_F. The total charge transferred, Q_{tran}, is given by:

$$Q_{tran} = Q_C + Q_F = Q_{pixel} \times \frac{C_C + C_F}{C_{PD} + C_C + C_F}, \tag{1.1}$$

where Q_C is the charge stored on C_C and Q_F is the charge stored on C_F. Equation (1.1) also shows that to transfer the majority of the accumulated charge, $C_C + C_F >> C_{PD}$ [7]. In this phase, the RS switch, controlled by ϕ_{SEL}, should be closed for a time considerably shorter than the opamp settling time such that the output node is unaffected [7]. The total charge on each capacitor after the charge transfer is given by:

$$Q_{PD} = Q_{pixel} \times \frac{C_{PD}}{C_{PD} + C_C + C_F} \tag{1.2}$$

$$Q_C = Q_{pixel} \times \frac{C_C}{C_{PD} + C_C + C_F} \tag{1.3}$$

$$Q_F = Q_{pixel} \times \frac{C_F}{C_{PD} + C_C + C_F}. \tag{1.4}$$

where Q_{PD} is the charge stored on C_{PD}.

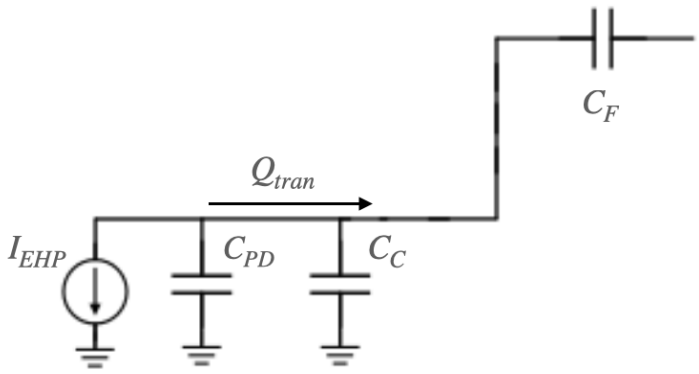


Figure 1.12: Circuit model of the integrator and circuit during the charge transfer phase (adapted from [7]).

In the amplifier settling phase, the pixel is disconnected from the integrator. The opamp virtual ground shifts the charge on C_C to C_F [7]. This configuration is shown in Figure 1.13.

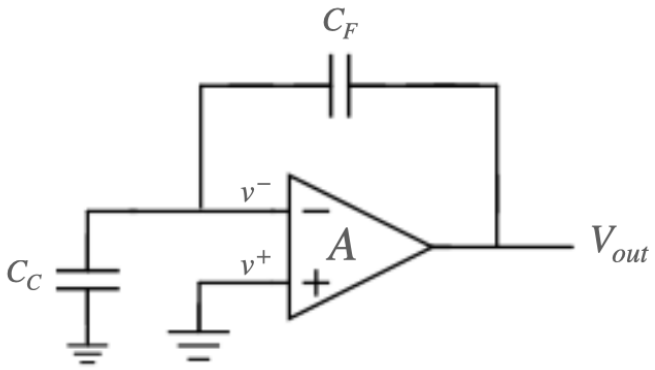


Figure 1.13: Circuit model of the integrator and circuit during the amplifier settling phase (adapted from [7]).

The output voltage can be measured at the end of this phase after the settling time of the opamp. The output voltage, V_{out} ,is given by:

$$V_{out} = v^- + \frac{Q_{tran}}{C_F}, \tag{1.5}$$

where $v^- = \frac{-V_{out}}{A}$. Combining (1.1) and (1.5) gives the following expression for V_{out}:

$$V_{out} = \left(\frac{A}{A+1}\right)\left(\frac{Q_{pixel}}{C_F}\right)\left(\frac{C_F + C_C}{C_{PD} + C_C + C_F}\right). \tag{1.6}$$

Equation (1.6) shows that the charge accumulated on the pixel has a linear relationship with the output voltage of the integrator [7].

In the pixel reset phase shown in Figure 1.14, the opamp is in unity feedback, and the pixel circuit is reconnected to the integrator. The presence of the virtual ground at the opamp's negative input resets the charge on all capacitors. It is important to note that using this readout method the output is free of the opamp's input offset voltage. During the integration phase, the offset voltage is stored on both C_C and C_F. When the charge is transferred from C_C to C_F during the sample phase, C_C holds the offset voltage. The input offset voltage is then cancelled by the offset voltage held on C_F [7].

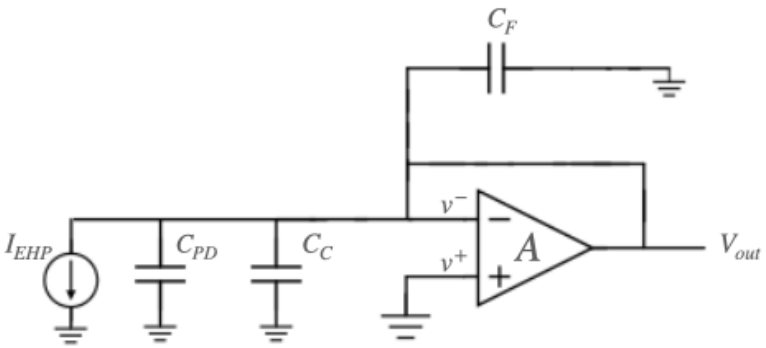


Figure 1.14: Circuit model of the integrator and circuit during the pixel reset phase (adapted from [7]).

1.3.2 Time-Division Multiplexing

Typical TDM readout uses row and column decoders, as shown in Figure 1.15. After the pixel's integration time, a row is selected, and the pixel's charge is transferred to the corresponding column for readout. The columns are then selected individually to convert each pixel charge to a voltage [7]. This process repeats for each row in the imager. The charge-to-voltage conversion occurs using a capacitive-feedback amplifier, and correlated doubling sampling techniques are employed to reduce readout noise [3].

The TDM approach has several drawbacks. As the number of rows and columns increases, the scan time required to read out an entire image also increases. Furthermore, the operation of the device using this readout approach is inefficient [8].

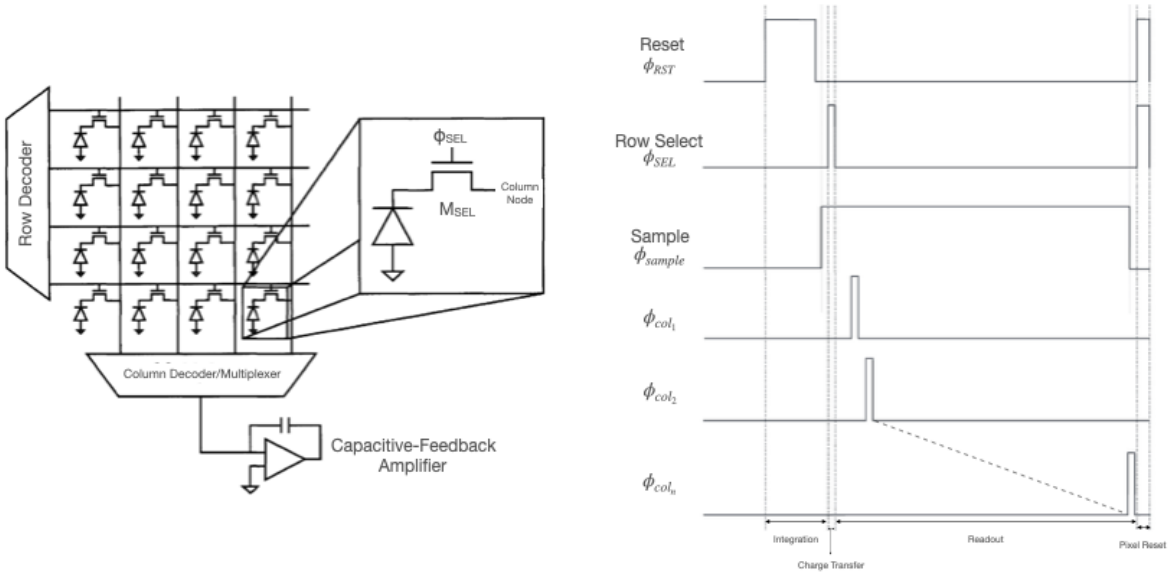


Figure 1.15: Overview of TDM readout approach using an array of PPS (adapted from [7]).

1.3.3 Analog Code-Division Multiplexing

Code-division multiple access (CDMA) is employed in wireless communications whereby multiple transmitted signals use the same channel to relay information. This technique can be applied to the analog domain and used for current-based sensor readouts, such as the PPS. The increase in SNR is the main advantage of using CDM over TDM. This occurs because the CDM approach effectively increases the pixel integration time for a constant frame rate [8]. This is especially important for a PPS array because it is known to have low SNR.

To apply the CDM readout to a PPS array, the pixel circuit requires modification. Instead of a single RS transistor, the pixel contains two RS transistors, M_{RS}^{+} and M_{RS}^{-}, each connected to a separate column line, where each line contains its own integrator, as shown in Figure 1.16.

The charge transfer for each pixel during one readout cycle will be through either the M_{RS}^{+} transistor or the M_{RS}^{-} transistor. The transistor used is governed by an encoding matrix where one column of the encoding matrix is applied to each row in the pixel array to obtain one output frame. The pixel encoding is mathematically shown by [8]:

$$[X(k)]_{1\times n} \times [A_c(k)]_{n\times 1} = y(k), \tag{1.7}$$

where n is the number of columns in the array, $[A_c]$ is an $n \times n$ encoding matrix, $[X(k)]_{1\times n}$ represents a row of pixels, k denotes the sample number, and $y(k)$ is the sum of the charge accumulated for one column [8]. In this mathematical representation of CDM, the sum of the pixel signals is done through (1.7), where the encoding matrix consists of a summing coefficient of 1 or -1. The circuit implementation will sum the photocurrent (charge accumulated) on two separate column lines. Each photocurrent sum will be converted to a voltage using an integrator, and the subtraction is done using a difference amplifier with an output denoted by $y(k)$ [8].

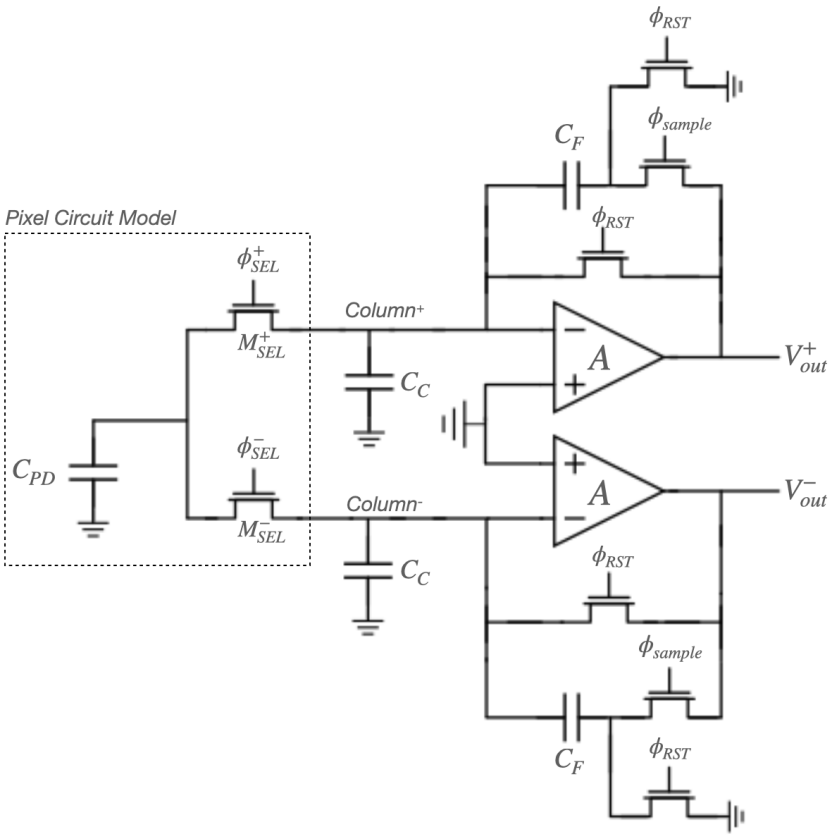


Figure 1.16: Circuit model of modified PPS and integrator for use with CDM readout approach (adapted from [8]).

Each column output is then fed into an ADC and later decoded to form an image once n samples have been taken from each column such that [8]:

$$[Y(k)]_{1\times n} = [y(n) \quad y(n-1) \quad \dots \quad y(1)], \tag{1.8}$$

where $[Y(k)]_{1\times n}$ is the n outputs of one column [8]. To perform the decoding process, the inverse of the encoding matrix is used as follows [8]:

$$[Y(k)]_{1\times n} \times [A_c(k)]^{-1}_{n\times n} = [\hat{X}(k)]_{1\times n}, \tag{1.9}$$

where $[\hat{X}(k)]_{1\times n}$ is the decoded pixel signals for the row corresponding to $[Y(k)]_{1\times n}$ [8]. An example of the decoding process is given in Appendix A.

The main disadvantages to using CDM is the area needed on chip for the readout circuitry and increased pixel size compared to a conventional PPS [8].

Figure 1.17 compares conventional TDM readout to CDM readout. Assume for this comparison that each column in the TDM and CDM approaches have their own readout circuit. We define T_{frame} as the time it takes to read out one frame. Using TDM, the entire column of n-pixels is read out in time T_{frame} as shown in Figure 1.17. Note that each pixel is read out once during this time and each pixel is read out individually. Using CDM each column is read out in the same amount of time it takes to read out an individual pixel using TDM (i.e., each column is read out in a time T_{frame}/n) as shown in Figure 1.17. As such, the rate at which the output of a single column of pixels is read is n-times faster using CDM. However, in order to decode the column output using CDM, n measurements of the column output are required. This effectively increases the integration time by a factor of n and, therefore, provides an increase in SNR by the same factor. Additionally, the time it takes to read out column outputs that can be decoded to construct a frame is T_{frame}. During readout, each column is given the same code that controls the gate of the RS transistors in the pixel. Each time the column is read out, a new code is used. After a frame is read out, the column output voltages are decoded to obtain individual pixel signals.

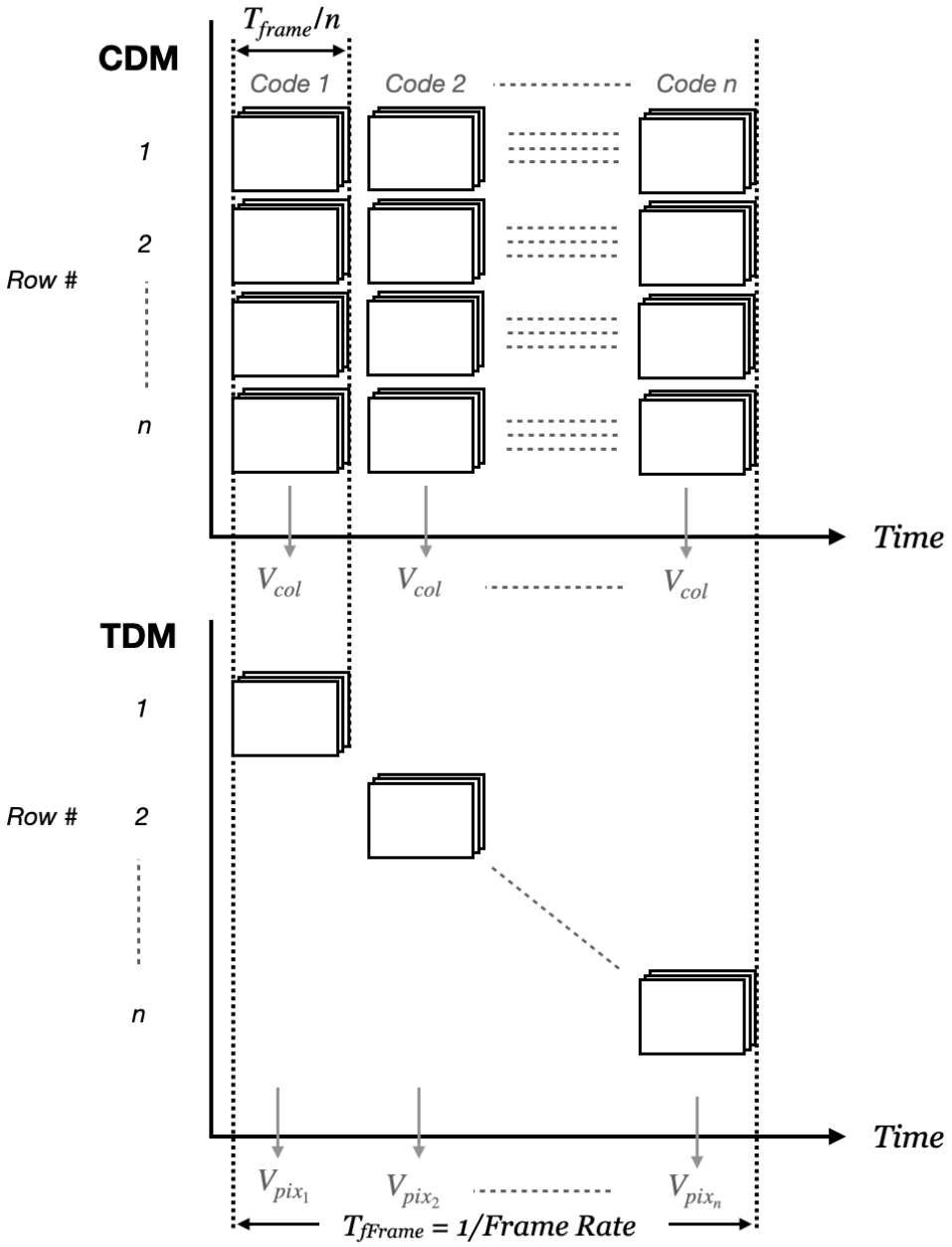


Figure 1.17: Illustration of CDM and TDM imager readout.

1.4 Motivation and Objective

Pixel size can be reduced to increase the spatial resolution of X-ray imagers. However, empirical results have shown that using smaller pixels negatively affects overall sensor performance. It results in a lower pixel dynamic range, higher sensor dark current (therefore worsened sensitivity in low-light applications), higher transistor leakage current (as a result of using smaller transistors), and higher sensitivity to diffraction at the pixel edge for optical imaging and scintillator based X-ray imagers. In X-ray imaging, it is challenging to reduce the sensor's pixel size using scintillators because of the tradeoff between X-ray absorption and spatial resolution. As such, a direct-conversion material can overcome this tradeoff.

Our imager target applications such as DFXM for X-ray photon energies > 20 keV. Current imagers have large pixels and require optics to characterize the material. The conversion efficiency of these detectors is poor, requiring long integration time to generate an image. The use of a-Se not only improves detector efficiency at the target energy range, but also enables a reduction in pixel size due to its inherently high spatial resolution. Our imager will be used in the DFXM application reported in [13], where an image occupies 200×250 pixels of the BrillanSe imager developed by KA Imaging with 8 μm $\times$ 8 μm pixels. This image size dictates the pixel array size of our imager, and renders the need to scale our imager's pixel array redundant.

Additionally, beam time is a valuable resource, and with the integration time required for current detectors, too much time is spent using the synchrotron. Current detectors operate at a 3 Hz frame rate. This work aims to reduce pixel size, and improve the frame rate by a minimum factor of ten, with an 8-bit resolution. Table 1.1 summarizes the key specifications for our imager.

Currently, the pixel size of the direct-conversion X-ray imager with the smallest pixel is 5.6 μm$\times$ 6.25 μm [17]. Our work aims to improve the spatial resolution of the imager developed in [17], where a 4T direct-conversion APS that used a-Se as the X-ray sensor was implemented for radiographic applications and digital phase-contrast imaging.

In this thesis, we implement a direct-conversion PPS with an a-Se X-ray sensor to reduce the pixel size. The main challenge associated with using a PPS is low SNR. This

can be mitigated by using a 2T-PPS array along with CDM readout. This boosts SNR, as it allows for a longer effective integration time. The key imager design specifications are summarized in Table 1.1

Table 1.1: Key X-Ray Imager Design Specifications

Specification	Target
Energy range	> 20 keV
Array size	800×800
Maximum pixel dimension	0.5 μm - 2.5 μm
Frame rate	30 Hz
Readout resolution	8-bit

1.5 Organization

This thesis is organized as follows:

- Chapter 2 discusses the design of the imager. It begins with the design of the pixel circuit, OTA and column readout circuits. This is followed by a circuit noise analysis to estimate the overall noise expected from the chip. The RS control circuit, column output multiplexers, and chip layout are also discussed.
- Chapter 3 presents the design of an external printed-circuit board (PCB) used to digitally control the imager, convert analog outputs to digital signals, and relay the output to a PC. Preliminary testing results of the on-chip readout circuits are also included.
- Chapter 4 concludes the thesis and discusses potential future work.

Chapter 2

Design

This chapter presents the design of our X-ray imager. Figure 2.1 shows the sensor acquisition channel on the CMOS imager, and Figure 2.2 shows the block diagram of the complete system. The system includes a custom CMOS imager fabricated using the TSMC 180-nm CMOS process, a custom PCB, and software used to control a field-programmable gate array (FPGA). The design of the different blocks shown in Figure 2.2 is discussed in this chapter, including the a-Se X-ray sensor.

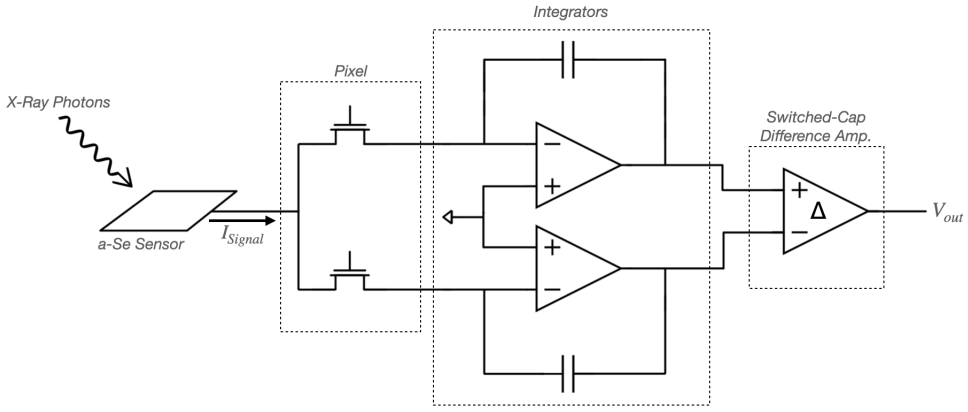


Figure 2.1: Sensor acquisition channel architechture.

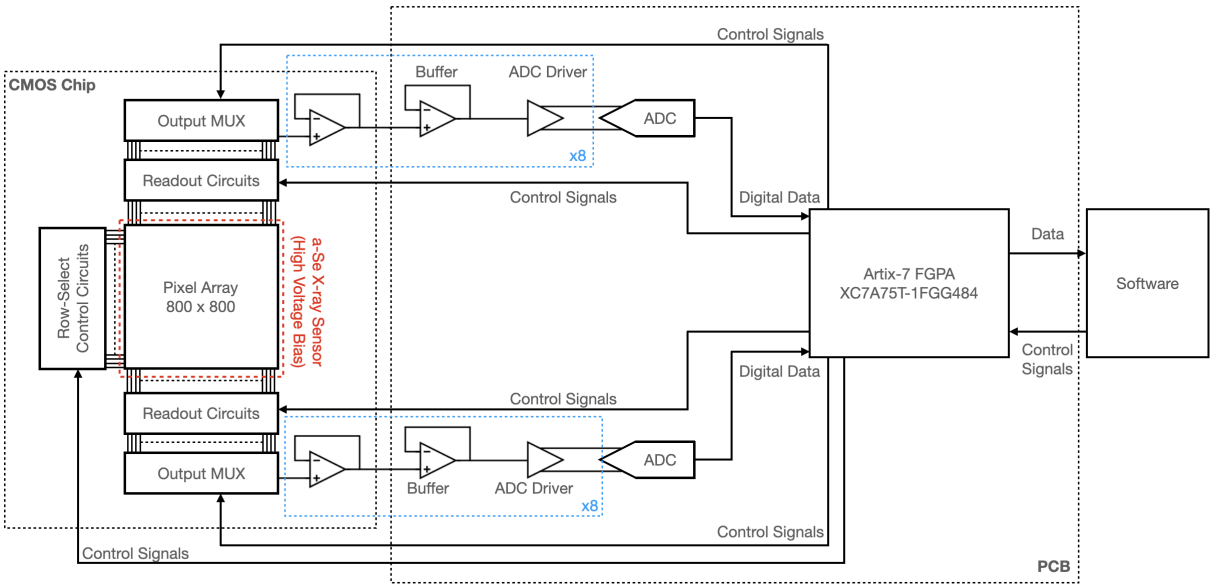


Figure 2.2: Block diagram of the complete X-ray imaging system.

2.1 Amorphous Selenium X-Ray Sensor

We deposit a uniform layer of a-Se directly onto the exposed metal pads of each pixel on the CMOS chip. The deposition of a-Se is performed using thermal evaporation under high vacuum. To prevent crystallization of the a-Se, it is alloyed with arsenic (As). However, this combination impairs hole transport in the alloyed material. As such, the alloy is doped with chlorine (Cl) to improve hole transport. The resulting material (99.8% Se, 0.2% As_2Se_3, and 10 parts-per-million Cl) is referred to as stabilized a-Se and has increased stability and hole transport properties [4].

2.1.1 Quantifying the Input Signal Current

In this section, we discuss the input signal current produced by a-Se illuminated by X-ray photons from a synchrotron. The total number EHPs generated per photon in a-Se is given by [1]:

$$N_{EHP} = \eta(E) \times CG, \tag{2.1}$$

where $\eta(E)$ is the quantum efficiency (QE), E is the photon energy in eV, and CG is the conversion gain in EHP/photon. QE quantifies the percentage of X-ray photons that interact with a-Se to create EHPs, and is given by:

$$\eta(E) = 1 - e^{\alpha\rho d}, \tag{2.2}$$

where α is the mass attenuation coefficient in $\mathrm{m^2kg^{-1}}$, ρ is the material density in $\mathrm{kg \cdot m^{-3}}$, and d is the material thickness. Figure 2.3 shows the varying mass attenuation coefficient with photon energy for a-Se and CsI. EHPs are generated via the mechanisms discussed in Section 1.1.2. From Figure 2.3, an a-Se layer that is 60 μm thick has a quantum efficiency of $\eta(E) = 0.49$. That is, 49% of all incident photons on the a-Se generate EHPs.

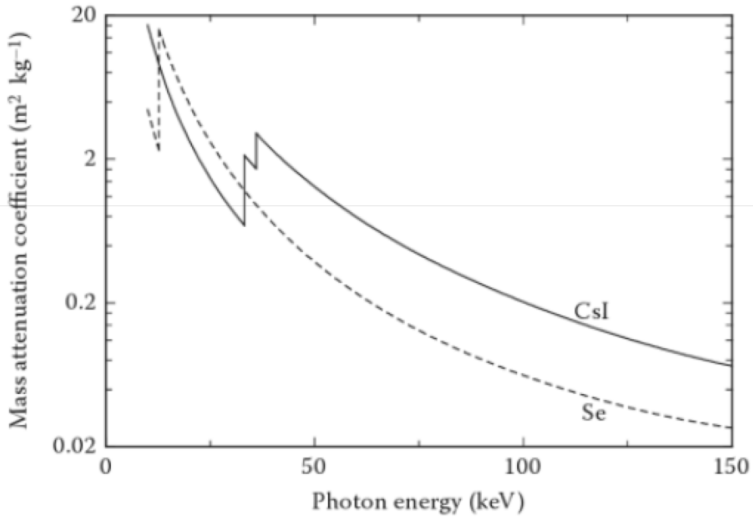


Figure 2.3: Mass attenuation coefficient of a-Se and CsI at different photon energies (taken from [1]).

The conversion gain estimates the number of EHPs generated per photon at a given photon energy [20]:

$$CG = \frac{E}{W_{\pm}} = \frac{E}{W_{\pm}^{0} + \frac{B}{F}} \quad \left[\frac{\text{EHP}}{\text{photon}}\right], \tag{2.3}$$

where $W_{\pm}$ is the EHP creation energy, $W_{\pm}^{0} = 6$ eV, $B = 4.4 \times 10^{2}$ eV$\cdot$ V μm^{-1}, and F is the electric field applied to a-Se in V/μm. Using incident photons of 40 keV and an applied electric field of 5 V/μm, $CG = 425.5 \frac{\text{EHP}}{\text{Photon}}$. This model is not accurate using $F >$ 70 V/μm because a-Se can undergo an avalanche process [18][1].

For our imager design, we use an a-Se layer with $d = 60$-μm with $F = 5$ V/μm. Additionally, our target applications work with $E \approx 40$ keV. Therefore, the total number of EHPs generated per photon is:

$$N_{EHP} = \eta(E) \times CG = 0.49 \times 425.5 \, \frac{\text{EHP}}{\text{photon}} = 208.5 \, \frac{\text{EHP}}{\text{photon}}. \tag{2.4}$$

With a synchrotron flux of $10^{6} \, \frac{\text{photons}}{\text{s}\times\mu\text{m}^2}$, the total signal current in one pixel I_{signal} is calculated as follows:

$$I_{signal} = 10^{6} \, \frac{\text{photons}}{\text{s} \times \mu\text{m}^2} \times 208.5 \, \frac{\text{EHP}}{\text{Photon}} \times 1.6 \times 10^{-19} \text{ C} \times 5.32\mu\text{m}^2 = 0.177 \text{ nA}. \tag{2.5}$$

2.2 Pixel

We implement a 2T-PPS where the pixel transistors are standard 1.8-V NMOS devices with minimum length (180 nm) and minimum width (220 nm). Using a single NMOS transistor as a switch means that the largest voltage that can pass is 1.8V – V_{th}, where V_{th} is the transistor threshold voltage. The on-resistance, R_{on}, is simulated to be 2.2 kΩ and the leakage current is simulated to be 0.6 pA. Figure 2.4 shows the circuit model for one pixel in the 800 $\times$ 800 array.

The 2T-PPS architecture is implemented for the following reasons:

1. Since the PPS architecture requires only two transistors, the pixel can be made small,

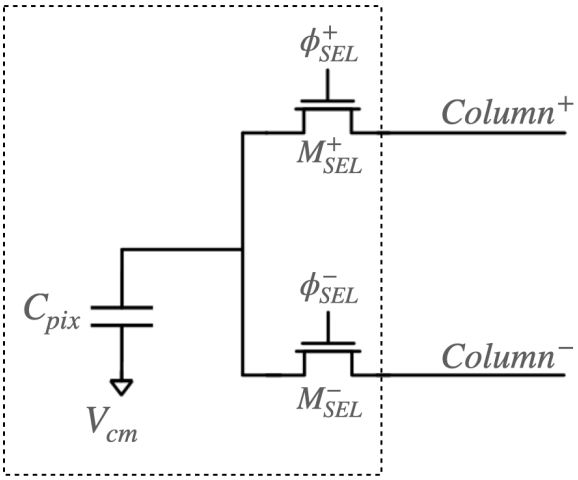


Figure 2.4: 2T-PPS circuit model.

allowing for high spatial resolution. This architecture also allows the imager to meet the pixel dimension specification outlined in Table 1.1. The pixel would not meet this specification if a 3T or 4T pixel architecture were implemented.

2. The main drawback of the PPS architecture is a low SNR. The CDM readout technique is shown to boost the SNR. Given that the conventional 1T-PPS is incompatible with the CDM readout approach, we implement a 2T-PPS.

The capacitor, C_{pix}, in Figure 2.4, is a combination of the transistors' parasitic capacitance at the pixel input node (C_{db} and C_{gd}), the capacitance due to the a-Se layer (C_{aSe}), and the additional capacitance formed between metal layers 3 and 4, C_{M3-M4}, and metal layers 4 and 5, C_{M4-M5}. C_{pix} is therefore given by:

$$C_{pix} = 2C_{db} + 2C_{gd} + C_{aSe} + C_{M3-M4} + C_{M4-M5}. \tag{2.6}$$

We target the highest possible value of C_{pix} to allow for longer integration time and therefore higher achievable SNR. As such, the metal in layers 3 and 5 are added to cover the area of the pixel while maintaining the layout design rules to form additional capacitance.

Note that special high density metal-insulator-metal (MIM) capacitors are not used in the pixel because the minimum size required for fabrication (4 μm $\times$ 4 μm) is larger than the pixel size. The layout for four pixels is shown in Figure 2.5, where the white outline highlights one pixel. This 2×2 grid of pixels is translated vertically and horizontally to form the array. To minimize the pixel layout, vertically adjacent pixels share a source terminal for the $Column^+$ output lines, and the body terminal is shared between the eight transistors directly in the middle of the 2×2 pixel array. Table 2.1 summarizes the device and component information for the pixel. The final pixel size is 2.252 μm $\times$ 2.363 μm.

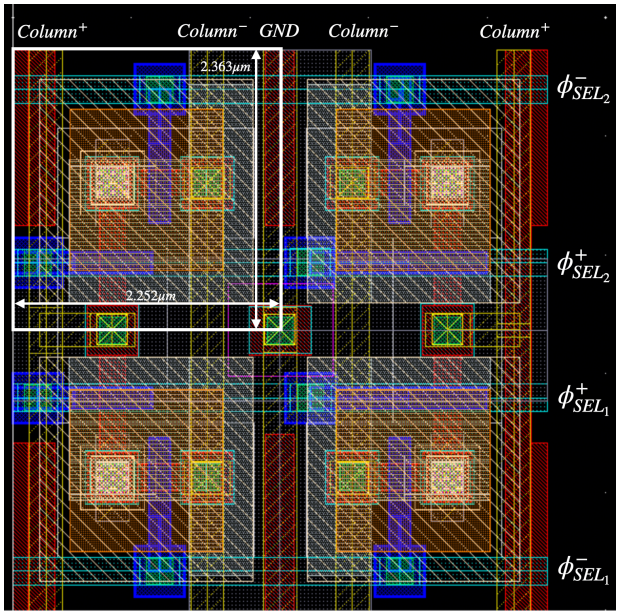


Figure 2.5: Layout of 2×2 array of the implemented 2T-PPS.

Table 2.1: Pixel Components and Sizes

Component	Type	Specification
M^+_{SEL}	NMOS	W/L = 220 nm/180 nm
M^-_{SEL}	NMOS	W/L = 220 nm/180 nm
C_{pix}	Capacitance	1 fF
Pixel	Size	2.252 μm $\times$ 2.363 μm

2.2.1 Noise

Two sources of noise are considered in the pixel: shot noise from photon capture in the a-Se layer and thermal noise from the RS transistors.

Shot Noise

Shot noise arises due to uncertainty in the number of EHPs generated in the X-ray sensor material when a photon is captured. Given the quantized nature of electrons, there is uncertainty in the flow of electrons [21]. For simplicity, we consider the 1T-PPS in the noise analysis.

The shot noise can be represented as a current source in the PPS, as shown in Figure 2.6. The RS transistor in this analysis is open and is modelled using a resistor R_{off}.

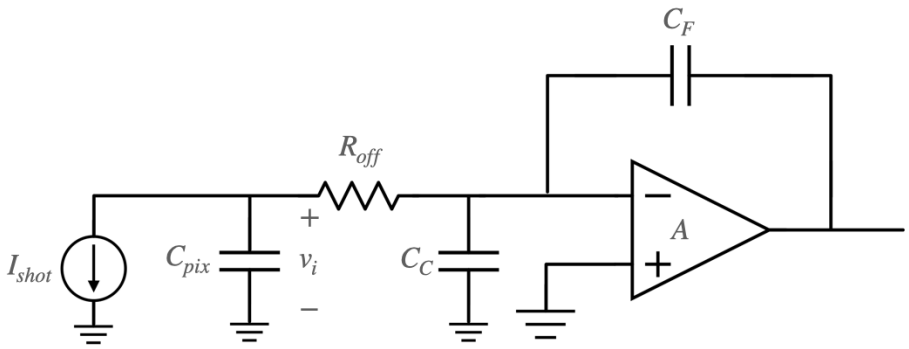


Figure 2.6: Circuit model to analyze shot noise in 2T-PPS.

Using nodal analysis at the pixel node and assuming the resistance of R_{off} is very large, the input voltage, v_i, is given by:

$$v_i = \frac{-I_{shot}}{sC_{pix}}, \tag{2.7}$$

where $\bar{I}^2_{shot}(f) = 2qI_{signal}$. The input-referred voltage noise power spectral density (PSD), $\bar{v}^2_{i_{shot}}(f)$, is given by:

$$\bar{v}^2_{i_{shot}}(f) = \frac{2qI_{signal}}{(2\pi f C_{pix})^2}, \tag{2.8}$$

where q is the elementary charge and f is the frequency in Hz. Integrating over frequency starting from the $1/t_{int}$, the input-referred average noise power, $\bar{v}^2_{i_{shot}}$, due to variations of the input signal is shown in (2.9), and the equivalent number of electrons is shown in (2.10).

$$\bar{v}^2_{i_{shot}} = \int_{\frac{1}{2\pi n t_{int}}}^{\infty} \frac{2qI_{signal}}{(2\pi f C_{pix})^2}\, df = \frac{qnt_{int}I_{signal}}{\pi C^2_{pix}}, \tag{2.9}$$

$$N^{shot}_{\bar{e}_{RMS}} = \frac{\sqrt{nt_{int}I_{signal}}}{\sqrt{\pi q}}. \tag{2.10}$$

The input-referred RMS shot noise is 339 e^-.

Thermal Noise of the Row-Select Transistor

The thermal noise of the RS transistor is modelled using resistor R_{on} for simplicity. This is because the transistor operates in the triode region where the current-voltage characteristic shows linear behaviour. The noise PSD of a resistor, $\bar{V_{n_R}}^2(f)$, is given by:

$$\bar{V_{n_R}}^2(f) = 4kTR, \tag{2.11}$$

where k is Boltzmann's constant and T is the absolute temperature in Kelvin. We analyze the circuit in Figure 2.7 to find the input-referred average noise power due to the thermal noise of the closed RS switch $\bar{v}^2_{i_{RS}}$. For simplicity, we consider only the 1T-PPS in the noise analysis. The noise calculated for the RS transistor and integrator is then multiplied by two to account for the additional noise from the second RS transistor and second integrator. Miller's theorem is applied to C_F, where C_F is replaced by two capacitors: one at the input and another at the output, C_{output}. C_{output} in Figure 2.7 is the sum of the Miller capacitance of C_F and the input capacitance of the switched-capacitor difference amplifier (SCDA).

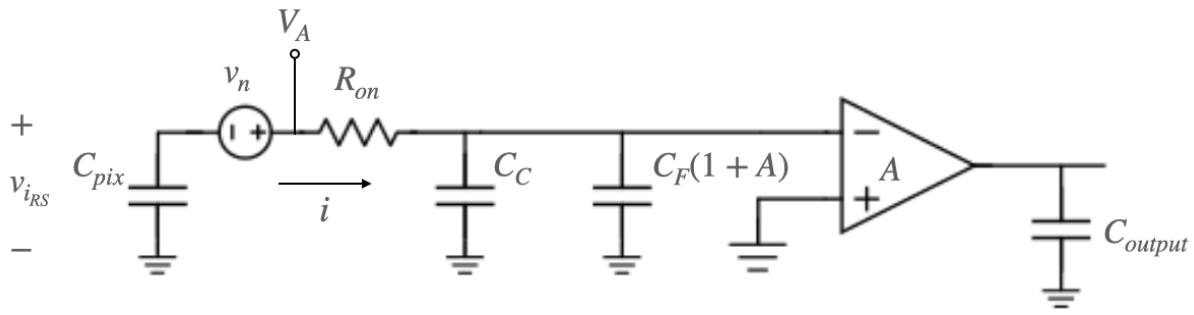


Figure 2.7: Circuit model to analyze thermal noise of the row-select transistors in the 2T-PPS.

The voltage V_A in Figure 2.7 is given by:

$$V_A = v_{i_{RS}} + v_n = i\left(\frac{sR_{on}(C_C + C_F(1+A)) + 1}{s(C_C + C_F(1+A))}\right), \tag{2.12}$$

where A is the open-loop dc gain of the amplifier. Isolating for $v_{i_{RS}}$ in (2.12), gives the noise PSD for the RS switch:

$$\bar{v}^2_{i_{RS}}(f) = \frac{\bar{v}^2_n(f)}{\left(1 + \frac{C_{pix}}{C_C + C_F(1+A)}\right)^2 \left(1 + \frac{(2\pi f)^2 C^2_{pix} R^2_{on}}{(1 + \frac{C_{pix}}{C_C + C_F(1+A)})^2}\right)}. \tag{2.13}$$

The average noise power due to thermal noise for the RS switches in each pixel in the column is given by:

$$\begin{aligned} \bar{v}^2_{i_{RS}} &= 2n \times \int_0^\infty \frac{\bar{v}^2_n(f)}{\left(1 + \frac{C_{pix}}{C_C + C_F(1+A)}\right)^2 \left(1 + \frac{(2\pi f)^2 C^2_{pix} R^2_{on}}{(1 + \frac{C_{pix}}{C_C + C_F(1+A)})^2}\right)} df \\ &= 2n \times \left(\frac{C_F(1+A) + C_C}{C_{pix}}\right)\left(\frac{kT}{C_F(1+A) + C_{pix} + C_C}\right). \end{aligned} \tag{2.14}$$

The equivalent average noise in terms of RMS electrons is given by:

$$N_{e^-_{RMS}}^{RS} = \frac{\sqrt{2n \times \left(\frac{kTC_{pix}(C_F(1+A)+C_C)}{C_F(1+A)+C_{pix}+C_C}\right)}}{q}, \tag{2.15}$$

which evaluates to 509 e^-. The total RMS pixel noise is dominated by the RS thermal noise and is 611 e^-.

2.3 CMOS Chip Floor Plan

The floor plan of the custom CMOS chip is shown in Figure 2.8. The integrator and switched-capacitor circuit layout for each column is constrained to the width of two columns of the pixel array (4.5 μm). These two readout components and the output multiplexer are constrained to a length of approximately 755 μm. With these area constraints, the size of the MIM capacitors used for the readout components are constrained. As such, the size of the MIM capacitors and transistors are minimized where possible. The layout of the readout column and the strategies used to maximize space are discussed in Section 2.14.

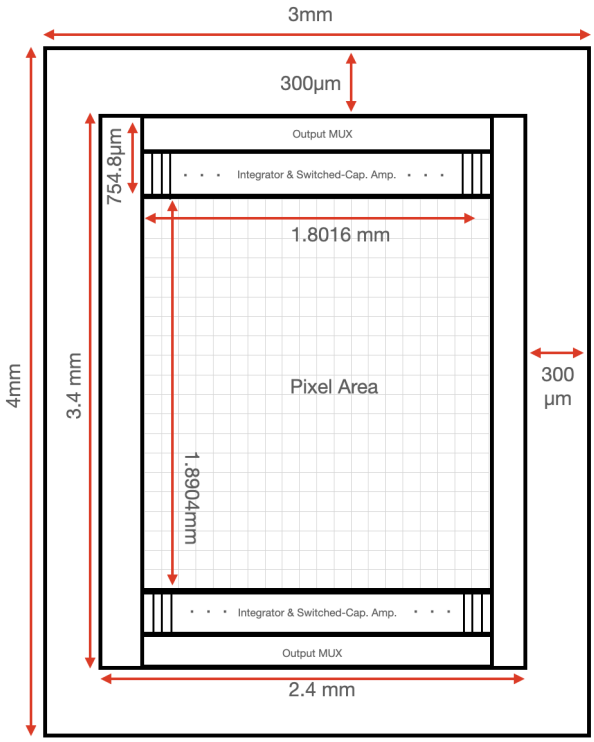


Figure 2.8: Floor-plan and dimensions of our custom CMOS imager.

2.4 Integrator

Our integrator circuit is shown in Figure 2.9. The integrator's feedback capacitor, C_F, is chosen to be 20 fF. This is because the SNR increases as the feedback capacitor decreases, and 20 fF is the minimum-sized MIM capacitor in the TSMC 180-nm CMOS process. This also satisfies the criteria that $C_C + C_F \gg C_{pix}$ so that close to 100% for the charge is transferred to C_C and C_F from C_{pix}.

The value of C_C in Figure 2.9 combines parasitic capacitances from the pixel RS switches, the integrator reset switch, and the metal column line. It is given by:

$$\begin{aligned} C_C &= n \times C_{SEL-Parasitic} + C_{RST-Parasitic} + C_{Metal} \\ &= n \times (C_{gs} + C_{sb}) + (C_{gd} + C_{db}) + C_{Metal}, \end{aligned} \tag{2.16}$$

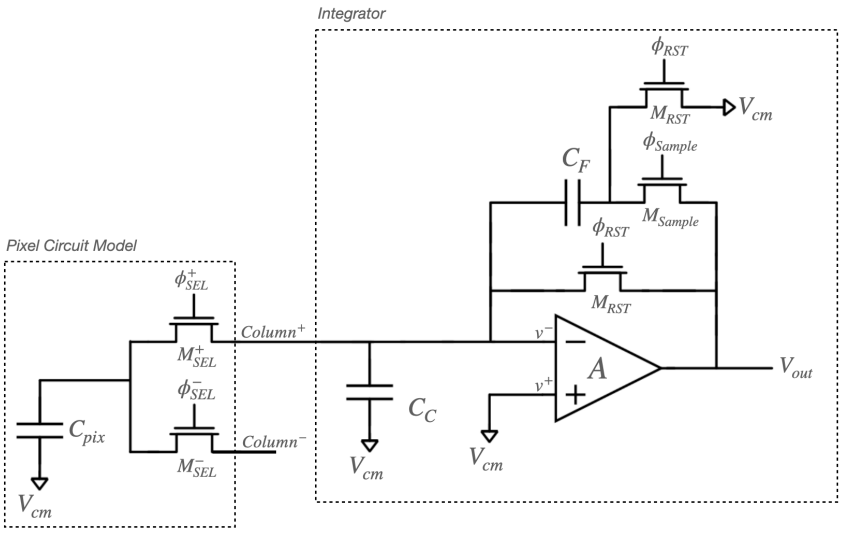


Figure 2.9: Circuit model of the integrator used to convert charge accumulated in the pixel to an output voltage.

where the estimated value is 0.74 pF. The reset transistor, M_{RST}, and sample transistor, M_{Sample}, used for the integrator are chosen to be minimum length and width because of the area constraints. Table 2.2 summarizes the device and component information for the integrator.

Table 2.2: Integrator Components and Sizes

Component	Type	Specification
M_{RST}	NMOS	W/L = 220 nm/180 nm
M_{Sample}	NMOS	W/L = 220 nm/180 nm

2.4.1 Noise

We consider two sources of thermal noise for the integrator: thermal noise from the reset switches and thermal noise from the opamp, which is discussed in Section 2.8.1.

Reset Thermal Noise

The reset thermal noise, which is represented in Figure 2.10. Like the RS transistor, M_{RST} is modelled using a resistor for simplicity. Equation (2.17) shows the noise current PSD, $\bar{I}_n^2(f)$, of a resistor:

$$\bar{I}_n^2(f) = \frac{4kT}{R}. \tag{2.17}$$

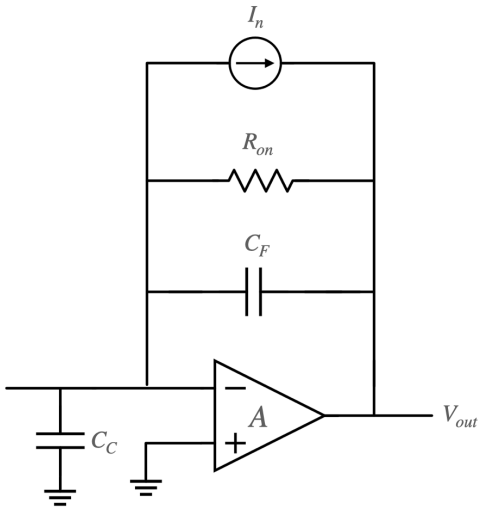


Figure 2.10: Circuit model to analyze reset thermal noise of the integrator.

The noise PSD at the output, $\bar{v}_{o_{RST}}^2(f)$, is given by:

$$\bar{v}_{o_{RST}}^2(f) = \bar{I}_n^2(f) \times Z_f^2 = \frac{4kT}{R_{on}}\left(\frac{R_{on}^2}{1 + C_F^2 R_{on}^2 (2\pi f)^2}\right), \tag{2.18}$$

where Z_f is the equivalent parallel impedance of the resistor, R_{on}, and C_F. The output-referred average noise power, $\bar{v}_{o_{RST}}^2$, is calculated by:

$$\bar{v}_{o_{RST}}^2 = 2 \times \int_0^\infty \frac{4kT}{R_{on}}\left(\frac{R_{on}^2}{1 + C_F^2 R_{on}^2 (2\pi f)^2}\right) df = 2 \times \frac{kT}{C_F}. \tag{2.19}$$

A factor of 2 is introduced to account for both integrators used in the readout circuit. To compare this result to the previously discussed noise source, the input-referred average noise power, $\bar{v}^2_{i_{RST}}$, is found to be:

$$\bar{v}^2_{i_{RST}} = \frac{\bar{v_o}^2}{|A_{v_0}|^2} = 2 \times \frac{kTC_F[(A+1)(C_{pix}+C_C+C_F)]^2}{[AC_{pix}(C_C+C_F)]^2}. \tag{2.20}$$

The equivalent RMS noise, $N^{RST}_{e^-_{RMS}}$, is given by:

$$N^{RST}_{e^-_{RMS}} = \sqrt{2kTC_F}\left(\frac{(A+1)(C_{pix}+C_C+C_F)}{qA(C_C+C_F)}\right), \tag{2.21}$$

and is calculated to be 80.6 e^-.

2.5 Switched-Capacitor Difference Amplifier

A resistor-based difference amplifier is shown in Figure 2.11.

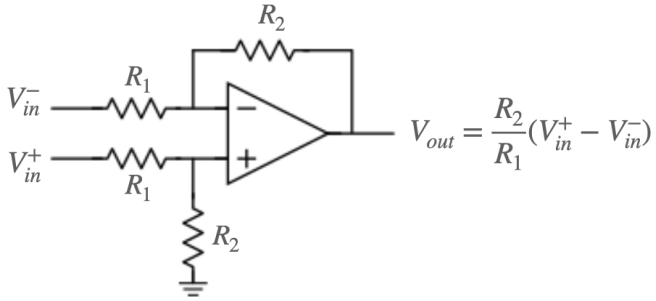


Figure 2.11: Common resistor-based difference amplifier.

Given the area restriction for the readout circuits, the difference amplifier in Figure 2.11 cannot be used due to the high area usage of the resistors. Instead, we implement the SCDA in Figure 2.12 which has an output voltage during its amplify phase given by:

$$V_{out} = \frac{C_1}{C_2}(V^+_{in} - V^-_{in}). \tag{2.22}$$

This SCDA operates in two phases: reset and amplify. During the reset phase, control signal ϕ_2 is high, and the voltage across the capacitors is cleared. During the amplify phase, control signal ϕ_1 is high, and the input voltage charges C_1, and this charging current flows across C_2 simultaneously [9]. As such, the change in charge across each capacitor is equal and the output voltage is given by (2.22) [9]. The output voltage of the amplify phase is coupled to the inverting input using C_3. As such, during the reset phase, the output voltage shifts only by the offset voltage of the amplifier. The transistors controlled by ϕ_3 are used to reset the amplifier on chip power up.

This circuit provides multiple advantages. First, this capacitive-reset gain circuit is insensitive to the opamp's input offset voltage. In addition, the effect of the opamp's $1/f$ noise is reduced [9]. Furthermore, using a switched-capacitor circuit connected to the positive input of the opamp will cancel clock feedthrough of the switches (coupling of the clock signals and analog signals) [9].

We choose the overall gain of the SCDA to be 2 V/V. Therefore, the ratio of capacitors $C_1/C_2 = 2$. The size of the capacitors are chosen based on the area constraints of the column readout circuit. Similarly, all transistors used are minimum length and width. Transmission gate (TG) switches are used instead of single NMOS or PMOS switches as simulation results showed improved linear behaviour. Device and component information is summarized in Table 2.3.

Table 2.3: Switched-Capacitor Difference Amplifier Components and Sizes

Component	Type	Specification
M_1, M_3, M_5, M_{6-11}, M_{13}, M_{15-18}	NMOS	W/L = 220 nm/180 nm
M_2, M_4, M_{12},M_{14}	PMOS	W/L = 220 nm/180 nm
C_1, C_3	MIM Capacitor	50 fF
C_2	MIM Capacitor	25 fF

The closed-loop bandwidth of the SCDA in the amplify phase is given by:

$$f_{-3dB_{CL}} = (1 + A_0\beta)f_{-3dB} = 1.78 \text{ MHz}. \tag{2.23}$$

where $A_0 = 1900$ V/V, $\beta = \frac{C_2}{C_1+C_2}$, and f_{-3dB} is the open-loop bandwidth of the OTA.

2.6 Noise Tolerance

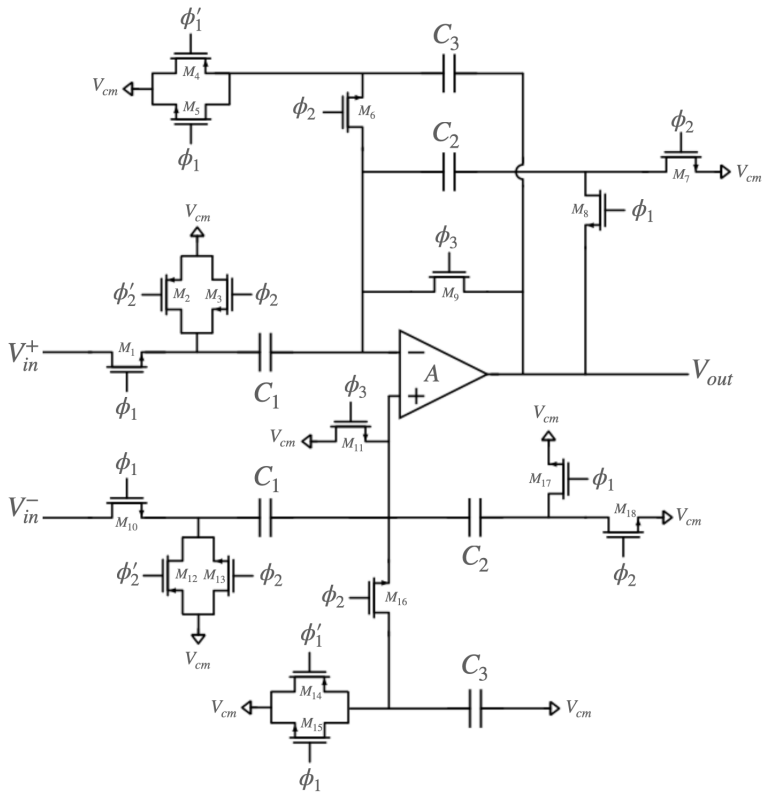
Before discussing the noise related to the opamps used for the integrators and SCDA, we first discuss the minimum tolerable noise the opamps can have in our system. We aim for an 8-bit dynamic range. That is, the minimum detectable signal is 256× smaller than the signal defined in (2.5), and is defined when SNR = 0 dB. Therefore the smallest signal current from one pixel, I_{signal}^{min}, is:

$$I_{signal}^{min} = \frac{I_{signal}}{256} = 0.69 \text{ pA}. \tag{2.24}$$

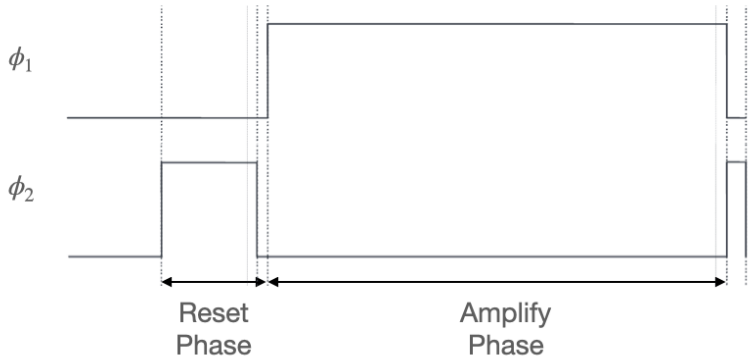
Assuming an entire column is illuminated at this signal with $t_{int} = 0.4067$ μs and the SNR is 0 dB, the total input-referred RMS noise for our signal chain is $N_{e^-_{RMS}}^{max} = 1403$ e^-. Note that the selection of this integration time is discussed later in this section and further in Sections 2.9.2 and 2.12. Accounting for the previously discussed noise sources along the signal chain, the input-referred RMS noise tolerance for the integrator and SCDA is given by:

$$N_{e^-_{RMS_{max}}}^{opamp} = \sqrt{N_{e^-_{RMS}}^{max^2} - N_{e^-_{RMS}}^{shot^2} - N_{e^-_{RMS}}^{RS^2} - N_{e^-_{RMS}}^{RST^2}}, \tag{2.25}$$

where $N_{e^-_{RMS_{max}}}^{opamp}$ is calculated to be 845 e^-.



(a)



(b)

Figure 2.12: (a) Implemented switched-capacitor difference amplifier (adapted from [9]). (b) Timing diagram for SCDA.

2.7 Operational Transconductance Amplifier

An operational transconductance amplifier (OTA) is required for the integrator and SCDA. The OTA is a two-stage amplifier: the first stage is a PMOS differential pair that provides a single-ended output, and the second stage is a common-source amplifier. Figure 2.13 shows the transistor-level schematic of the OTA.

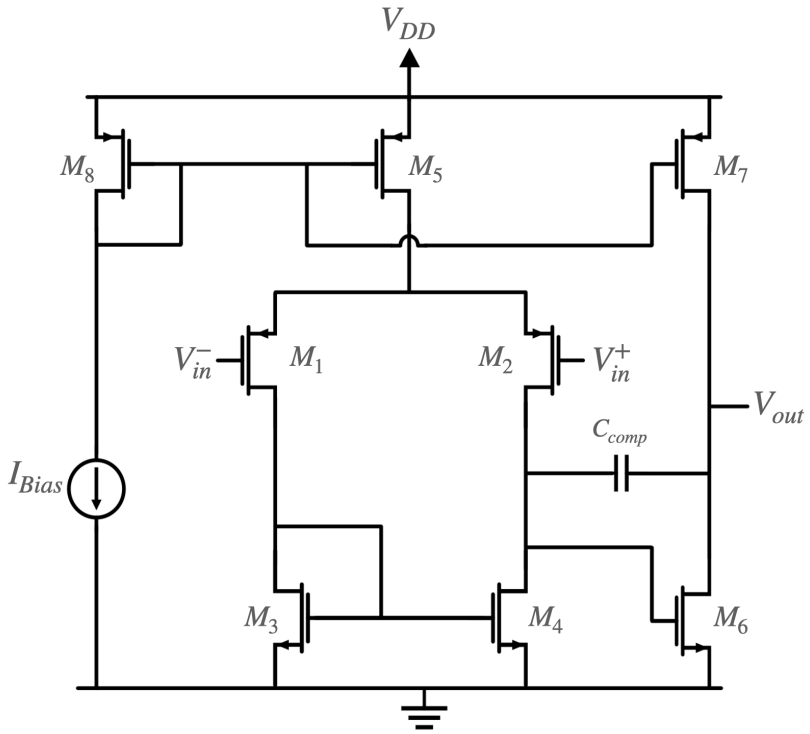


Figure 2.13: Transistor level schematic of the implemented OTA.

The dc gain of the OTA is given by:

$$\begin{aligned} A_{v_0} &= G_{m1}R_{out1} \times G_{m2}R_{out2} \\ &= g_{m1}(r_{o2}||r_{o4}) \times g_{m6}(r_{o6}||r_{o7}), \end{aligned} \tag{2.26}$$

where G_m is the short-circuit transconductance of a given stage, R_{out} is the stage output resistance, and r_o is the output resistance of a given transistor. The small-signal equivalent

circuit shown in Figure 2.14 provides insight into key parameters of the OTA, such as the transfer function, poles, and gain bandwidth product (GBW), which are discussed later in this chapter.

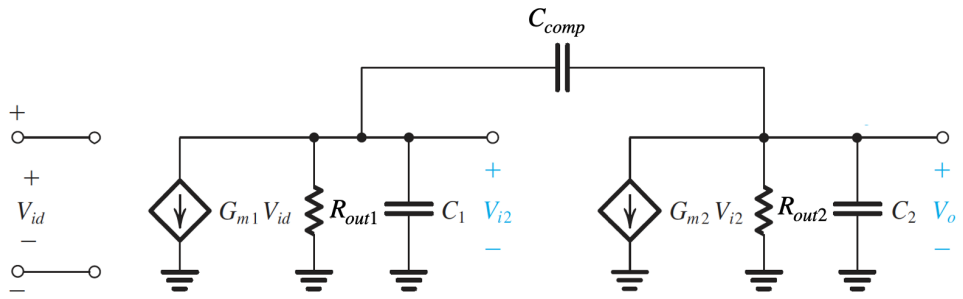


Figure 2.14: Small signal model of the two stage OTA implemented. Adapted from [10]

The transfer function, $\frac{V_o}{V_i}$, of the OTA is given by:

$$\frac{V_o}{V_i} = \frac{A_{v_0}(1 - sC_{comp}/g_{m6})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}, \tag{2.27}$$

where C_{comp} is the compensation capacitors, ω_{p1} is the dominant low-frequency pole, and ω_{p2} is the high-frequency pole. These are given by:

$$\begin{aligned} \omega_{p1} = \omega_{3dB} &= \frac{1}{R_{out1}[C_1 + C_{comp}(1 + g_{m6}R_{out2})] + R_{out2}(C_1 + C_2)} \\ &\approx \frac{1}{g_{m6}R_{out1}R_{out2}C_{comp}}, \end{aligned} \tag{2.28}$$

$$\omega_{p2} \approx \frac{g_{m6}}{C_1C_2 + C_{comp}(C_1 + C_2)}. \tag{2.29}$$

The GBW is given by:

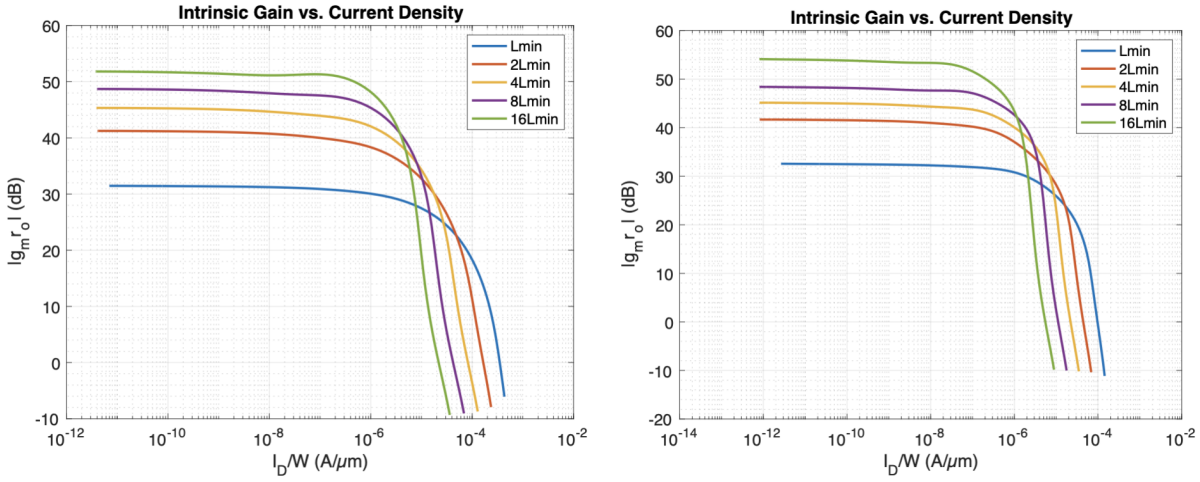
$$GBW = A_v \times f_{3dB} = G_{m1}R_{out1} \times G_{m2}R_{out2} \times \frac{1}{2\pi g_{m6}R_{out1}R_{out2}C_{comp}} = \frac{g_{m1}}{2\pi C_{comp}}. \tag{2.30}$$

2.7.1 DC Gain Design

Based on the specifications previously discussed, the OTA is designed for a resolution of 8 bits. The resolution is important in calculating the closed-loop steady-state error and thus the minimum acceptable dc gain of the OTA. The relative gain error of the OTA should therefore exceed 8 bits in our system. The minimum dc gain is given by:

$$A_{v_{0_{min}}} > \frac{1}{\beta\epsilon}, \tag{2.31}$$

where β and is the feedback factor, and ϵ is the steady-state settling error. Therefore, $A_{v_{0_{min}}} = 256$ V/V for $\beta = 1$ and $\epsilon = \frac{1}{2^8}$. Given that we design the OTA for both the integrator and SCDA, β is chosen to reflect the worst-case mode of operation, which is the reset phase where both circuits are in unity feedback. We multiply the minimum gain by five ($A_{v_{0_{min}}} = 1280$ V/V) to ensure a high open loop gain for better functionality. To achieve this, we aim for a first-stage gain of 85 V/V, and a second-stage gain of 15 V/V. Using the intrinsic gain of NMOS and PMOS transistors shown in Figure 2.15, the transistor sizes are found at a given current density I_D/W for different channel lengths. The intrinsic gain of a transistor is given by $g_m r_o$.



(a) (b)

Figure 2.15: (a) Simulated NMOS intrinsic gain with a width of 1 μm (b) Simulated PMOS intrinsic gain with a width of 1 μm. ($L_{min} = 0.18$ μm)

The intrinsic gain of the first stage A_{v_01} in terms of the intrinsic gain of a transistor can be estimated by:

$$A_{v_01} = \frac{1}{2} g_m r_o. \tag{2.32}$$

By solving for the intrinsic gain, the transistor sizes for the differential pair M_1 and M_2 are found at a bias current of 0.1 μA. Given the number of OTAs used in this design, it is important to minimize the total power consumption of the chip. As such, the bias current is chosen to minimize power and the bias transistors M_5 and M_8 are sized accordingly. A similar approach is used for the second stage amplifier involving M_6 and M_7. The size of M_6 is found by solving for the intrinsic gain of the second stage (using (2.32)) at a bias current of 1 μA. The bias current was chosen to minimize power. Transistor sizes are adjusted in simulation to achieve the minimum gain according to:

$$A_{v_01} = \frac{1}{2} \sqrt{2\mu C_{ox} L \frac{1}{I_D/W}} \left(\frac{1}{\lambda'} \right), \tag{2.33}$$

where λ' is related to the MOSFET channel-length modulation parameter.

Figure 2.16 shows the voltage transfer characteristic (VTC) of the OTA with a common-mode voltage of 0.4 V applied. The VTC shows a systematic input offset voltage of -0.42 mV. The slope of the linear region is A_{v_0}, which is around 1900 V/V and therefore exceeds the minimum gain specification. $A_{v_{01}} = 87$ V/V, $A_{v_{02}} = 22$ V/V, and the OTA power consumption is 2.16 μW. Table 2.4 lists the OTA components and their sizes.

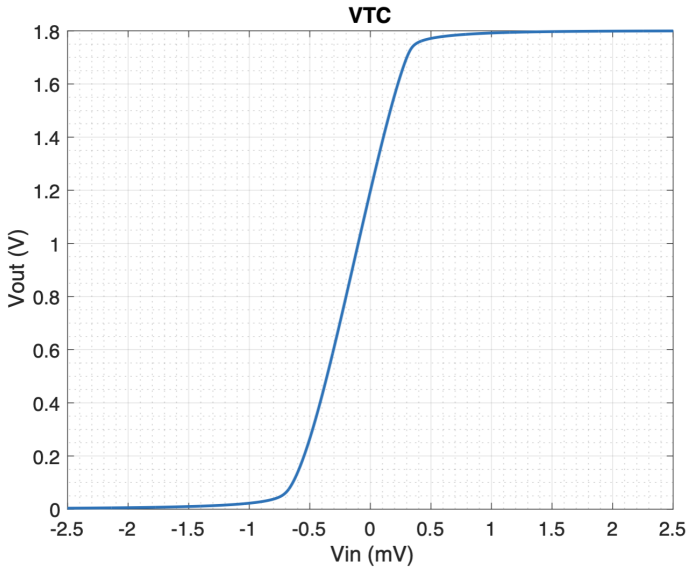


Figure 2.16: Simulated voltage transfer characteristic of the implemented OTA.

Table 2.4: OTA Component and Transistor Sizes

Component	Type	Specification
M_1, M_2	PMOS	W/L = 1 μm/0.9 μm
M_3, M_4	NMOS	W/L = 1 μm/0.7 μm
M_5	PMOS	W/L = 2 μm/0.72 μm
M_6	NMOS	W/L = 1 μm/0.18 μm
M_7	PMOS	W/L = 2 μm/0.18 μm
M_8	PMOS	W/L = 1 μm/0.72 μm
C_{comp}	MIM Capacitor	50 fF
I_{Bias}	Current	0.1 μA
OTA	Power	2.16 μW

2.7.2 Frequency Response and Stability

The GBW of the OTA is important in determining the settling time of the OTA. The settling time, t_s, is defined as the time required for the output voltage to reach its dc steady-state value within the specified error bound. Based on the timing discussion in Section 2.12, and to ensure the imager can operate at frame rates at least two to three times faster than the specification, t_s should be less than 1.5 μs. Therefore, the OTA time constant, τ, is given by:

$$\tau = \frac{t_s}{n_s} = 0.125\mu\text{s}, \tag{2.34}$$

where n_s is the number of time constants required for the OTA to settle to within the desired error. In our design, we use $n_s = 12$ is used such that the output settles to within 99.999% of its ideal value. The target GBW is then calculated by:

$$GBW_{target} = \frac{1}{2\pi\beta\tau} = 3.82 \text{ MHz}, \tag{2.35}$$

where $\beta = \frac{1}{3}$ to account for the worst-case settling of the SCDA. Figure 2.17 shows the frequency response of the OTA. The OTA has a -3-dB bandwidth $f_{3dB} = 2.8$ kHz and a

unity-gain frequency $f_t = 5.3$ MHz. The GBW is then given by:

$$GBW = 10^{\frac{65.75\text{ dB}}{20}} \times 2.8\text{ kHz} = 5.43\text{ MHz} \approx f_t. \tag{2.36}$$

The settling time is then given by:

$$t_s = 12\tau = \frac{12}{2\pi\beta GBW} = 1.1\ \mu\text{s}. \tag{2.37}$$

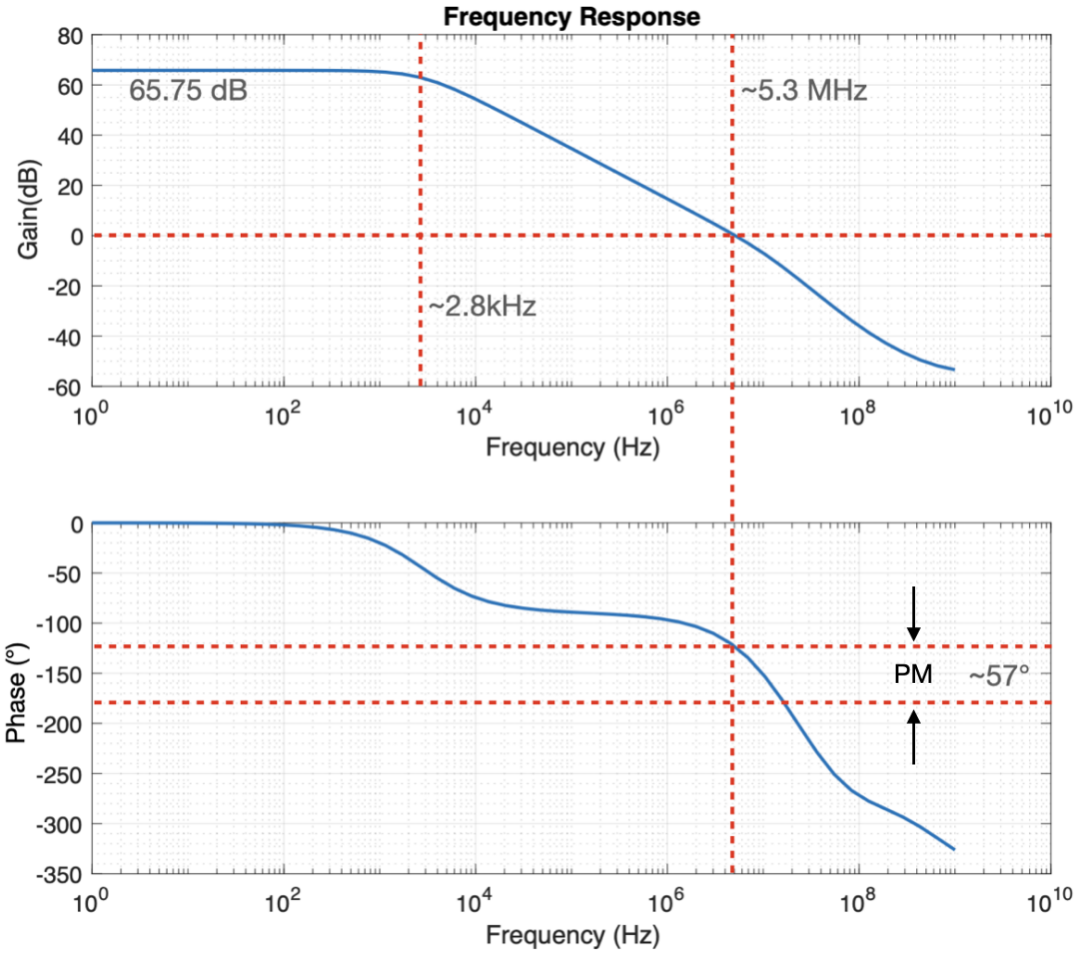


Figure 2.17: Simulated frequency response of the OTA.

The OTA's phase margin (PM) is 57° with $\beta = 1$, as shown in Figure 2.17. We achieve this using a compensation capacitor $C_{comp} = 50$ fF.

2.7.3 Noise

The first stage dominates the overall output noise of the OTA. The first stage with voltage noise sources for each transistor is illustrated in Figure 2.18.

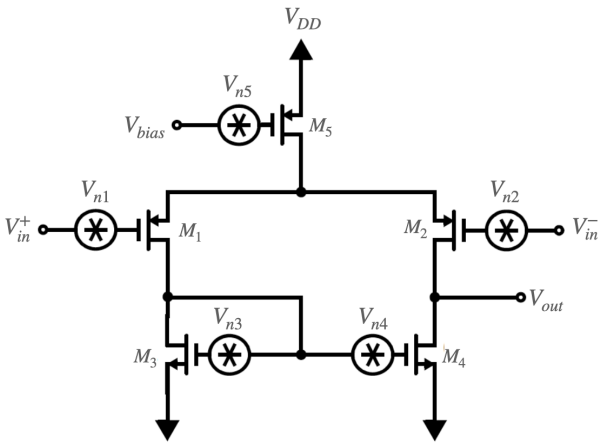


Figure 2.18: First input stage of the OTA with voltage noise sources for each transistor (adapted from [9]).

The output noise of the OTA is found by analyzing how the noise from each transistor propagates to the output. The gain of M_5 is relatively small compared to the gain from all other transistors so we do not include it in the noise analysis. Since transistors M_1 and M_2, and, M_3 and M_4, are matched, the gains from V_{n1} and V_{n2} to the output are the same and given by:

$$\left| \frac{V_{no}}{V_{n1,2}} \right| = g_{m1} R_{o1}. \tag{2.38}$$

The current flowing through the voltage source V_{n3} is zero as one side is connected to the gate of M_3. If we assume that all other sources are zero, the M_3 drain current is unchanged

by V_{n3} and hence the gate voltage of M_3 is also unaffected [9]. Therefore, $V_{n3} = v_{gs4}$ and the gain from V_{n3} and V_{n4} to the output are the same:

$$\left| \frac{V_{no}}{V_{n3,4}} \right| = g_{m3} R_{o1}. \tag{2.39}$$

The output referred noise PSD, $\bar{V}_{no}^2(f)$, is then given by:

$$\bar{V}_{no}^2(f) = 2(g_{m1}R_o)^2 \bar{V}_{n1}^2(f) + 2(g_{m3}R_o)^2 \bar{V}_{n3}^2(f). \tag{2.40}$$

The input-referred noise PSD, $\bar{V}_{input}^2(f)$, can then be calculated by dividing the output-referred noise by the dc gain of the OTA:

$$\bar{V}_{input}^2(f) = \frac{\bar{V}_{no}^2}{(g_{m1}R_o)^2} = 2\bar{V}_{n1}^2(f) + 2\bar{V}_{n3}^2(f)\left(\frac{g_{m1}}{g_{m3}}\right)^2, \tag{2.41}$$

where $\bar{V}_{ni_{th}}^2(f) = \frac{8kT}{3g_{mi}}$ for thermal noise and $\bar{V}_{ni_{fl}}^2(f) = \frac{K_i}{W_i L_i C_{ox} f}$ for flicker noise. The input referred thermal noise power is given by:

$$\bar{V}_{input_{th}}^2 = \frac{16kT}{3g_{m1}} + \frac{16kTg_{m3}}{3g_{m1}^2}. \tag{2.42}$$

The thermal noise is inversely proportional to g_m of the differential pair. To minimize thermal noise, the $g_{m1,2}$ should be maximized. This means that the input pair should operate in weak inversion for a constant drain current. The transconductance is given by:

$$g_{mi} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right) I_{Di}}, \tag{2.43}$$

where μ_p is the mobility of holes, C_{ox} is the gate oxide capacitance density of the transistor, and I_D is the drain current of the transistor. The input referred flicker noise power is given by:

$$\begin{aligned}\bar{V}^2_{input_f} &= \int_{f_1}^{f_2} \frac{2}{C_{ox}}\left[\frac{K_1}{W_1 L_1} + \left(\frac{\mu_n}{\mu_p}\right)\left(\frac{K_3 L_1}{W_1 L_3^2}\right)\right] \mathrm{d}f \\ &= \frac{2}{C_{ox}}\left[\frac{K_1}{W_1 L_1} + \left(\frac{\mu_n}{\mu_p}\right)\left(\frac{K_3 L_1}{W_1 L_3^2}\right)\right] ln\left(\frac{f_2}{f_1}\right).\end{aligned} \tag{2.44}$$

where $\mu_n C_{ox} = 0.197$ mA/V^2, $\mu_p C_{ox} = 35.6$ μA/V^2, and $C_{ox} = 8.67$ fF/μm^2 is the gate oxide capacitance density. Note that $K_1 = 5 \cdot 10^{-25}$ V^{2}F and $K_3 = 10 \cdot 10^{-25}$ V^{2}F are flicker noise constants that are technology dependent. The total noise from 1 Hz to 5.43 MHz is 0.65 mV$_{\text{rms}}$. Figure 2.19 shows the simulated input-referred noise PSD of the OTA. Note that the spike in the noise PSD at high frequencies is due to the OTA input capacitance. The total simulated integrated noise of the OTA from 1 Hz to 5.43 MHz is 0.78 mV$_{\text{rms}}$. The difference between the estimated and simulated noise can be attributed to estimates of device parameters and additional noise due to the second stage.

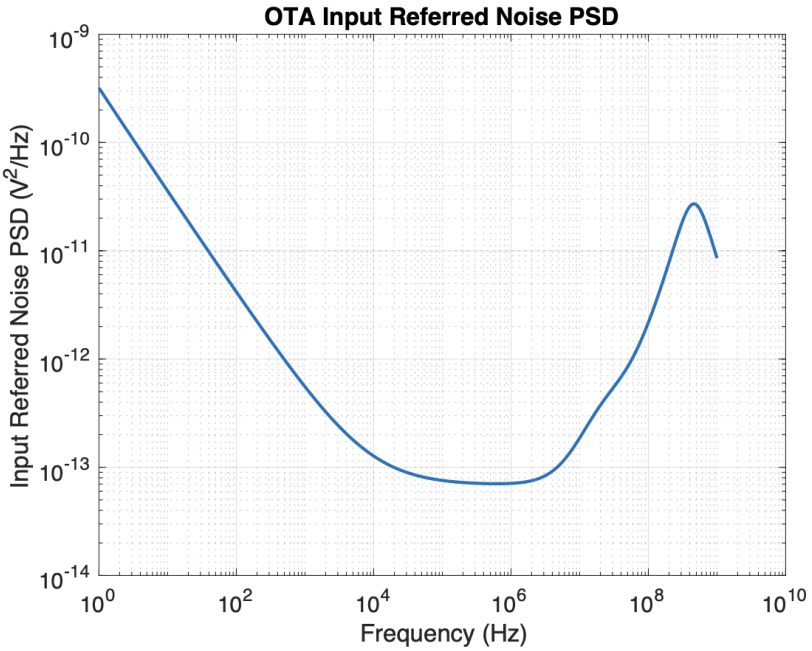


Figure 2.19: Simulated input-referred noise PSD of the OTA.

2.7.4 Slew Rate

Slew rate is defined as the maximum rate at which the OTA output can change when a large differential signal is applied to the input [9]. In terms of transistor operation, all the tail current in M_5 is steered towards M_1 or M_2. If a large positive input signal is applied, the tail current is steered through M_1 and the current mirror load M_3 and M_4. This results in M_2 being in the cut-off region and a current equal to the tail current coming out of C_{comp}. When a large negative voltage is applied, transistor M_1 is off; hence, M_3 and M_4 are off. This results in the tail current going through M_2 and into C_{comp} [9]. The slew rate required from the OTA assuming maximum input signal on all pixels and half the pixels in a column are directed to both integrators in the readout circuit is given by:

$$SR_{target} = \frac{I_{signal} N_{pixels}}{C_F} \approx 3.5 \text{ V}/\mu\text{s}. \tag{2.45}$$

The positive and negative slew rates are then estimated by:

$$SR = \frac{I_{D5}}{C_{comp}} \approx 4 \text{ V}/\mu\text{s}. \tag{2.46}$$

Through simulation, the positive slew rate is $SR^+ = 2.9$ V/μs and the negative slew rate is $SR^- = 3.5$ V/μs. Note that the simulated SR^+ does not meet the targeted slew rate for the maximum I_{signal}. The maximum tolerable input signal that can be tolerated is estimated to be 0.15 nA per pixel.

Table 2.5 summarizes the OTA target specifications and simulated response.

Table 2.5: OTA Target Specifications and Simulated Response

OTA Parameter	Target	Simulated
DC gain (A_{v_0})	>1280 V/V	1900 V/V
Gain bandwidth product (GBW)	>3.82 MHz	5.43 MHz
Settling time (t_s)	<1.5 μs	1.1 μs
Phase Margin (PM)	>45°	57°
Positive slew rate (SR^+)	≥3.5 V/μs	2.9 V/μs
Negative slew rate (SR^-)	≥3.5 V/μs	3.5 V/μs

2.8 Amplifier Noise

2.8.1 Integrator Thermal Noise

We now consider the thermal noise of the integrator OTA. The OTA in the amplifier settling phase, is shown in Figure 2.20.

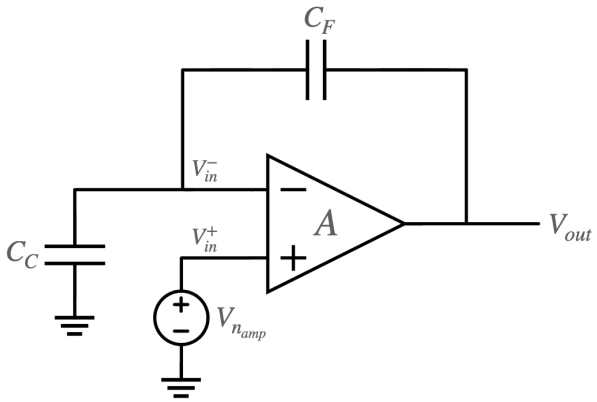


Figure 2.20: Circuit model to analyze amplifier thermal noise of the integrator.

The noise PSD of the amplifier is derived and explained in Section 2.7.3 and is given by:

$$\bar{V}^2_{n_{amp}}(f) = \frac{16kT}{3g_{m1}} + \frac{16kTg_{m3}}{3g^2_{m1}}, \tag{2.47}$$

The amplifier is under negative feedback, and its transfer function is given by [22]:

$$H(s) = \frac{V_{out}(s)}{V_{in}^{+}(s)} = \frac{G_0}{1 + s\tau}, \tag{2.48}$$

where G_0 is the dc gain of the amplifier in feedback and τ is the settling time constant. G_0 is given by [22]:

$$G_0 = \frac{1}{\beta + 1/A} \approx \frac{1}{\beta} = 1 + \frac{C_C}{C_F}, \tag{2.49}$$

where β is the feedback factor, and A is the dc gain of the opamp, which is assumed to be much larger than $1/\beta$. The settling time constant, τ, is given by [22]:

$$\tau = \frac{C_{comp}}{\beta g_{m1}}, \tag{2.50}$$

The output referred average noise power is then given by:

$$\begin{aligned} \bar{v}_{o_{int}}^2 &= 2 \times \int_0^\infty \bar{V}_{n_{amp}}^2 |H(s)|^2 df = 2 \times \frac{\bar{V}_{n_{amp}}^2 G_0^2}{4\tau} \\ &= 2 \times \left(\frac{16kT}{3g_{m1}} + \frac{16kTg_{m3}}{3g_{m1}^2} \right) \left(\frac{g_{m1}}{\beta C_{comp}} \right) \\ &= 2 \times \left(\frac{4kT}{3\beta C_{comp}} \right) \left(1 + \frac{g_{m3}}{g_{m1}} \right). \end{aligned} \tag{2.51}$$

Note that the factor of 2 in (2.51) is introduced to account for both integrators used in the readout circuit. The input-referred average noise power is given by:

$$\bar{v}_{i_{int}}^2 = 2 \times \left(\frac{4kT}{3\beta C_{comp}} \right) \left(1 + \frac{g_{m3}}{g_{m1}} \right) \left(\frac{(A+1)(C_{pix} + C_F + C_C)C_F}{A(C_F + C_C)C_{pix}} \right)^2. \tag{2.52}$$

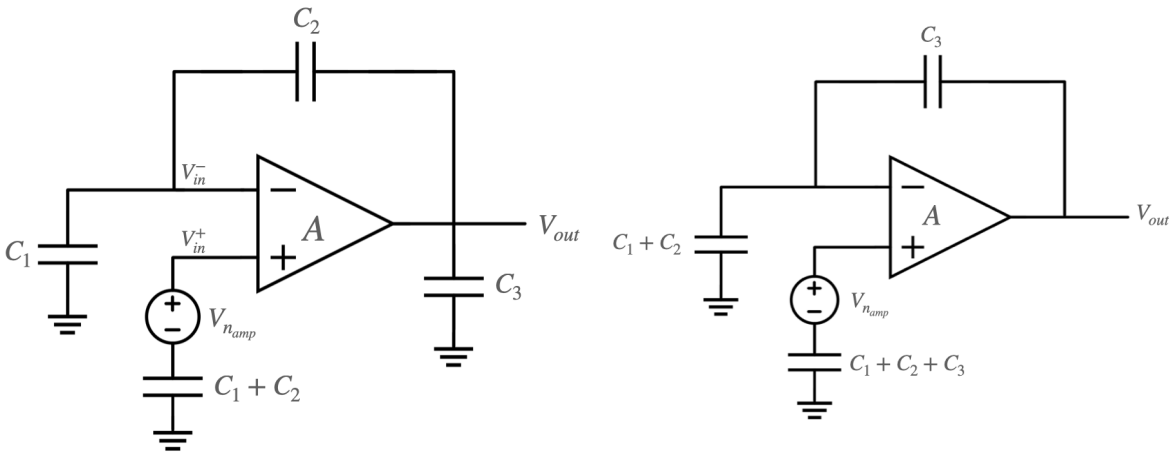
The equivalent RMS noise, $N_{e^-_{RMS}}^{int}$, is given by:

$$N_{e^-_{RMS}}^{int} = \left(\frac{(A+1)(C_{pix}+C_F+C_C)C_F}{qA(C_F+C_C)}\right) \times\sqrt{2\times\left(\frac{4kT}{3\beta C_{comp}}\right)\left(1+\frac{g_{m3}}{g_{m1}}\right)}. \tag{2.53}$$

and is calculated to be 518 e^-.

2.8.2 Switched-Capacitor Difference Amplifier Noise

The noise of the SCDA in the amplify and reset phases is now considered. In this analysis, it we assume that the on-resistance of each switch is zero. We also assume the noise in each phasde is dominated by the thermal noise of the opamp and that each phase is a continuous-time circuit. Figure 2.21(a) shows the amplify phase with the opamp input noise and Figure 2.21(b) shows the reset phase.



(a) (b)

Figure 2.21: (a) Circuit model to analyze amplifier thermal noise of the switched-capacitor difference amplifier in the amplify phase. (b) Circuit model to analyze amplifier thermal noise of the switched-capacitor difference amplifier in the reset phase.

A similar noise analysis provided for the opamp thermal noise in Section 2.8.1 is con-

ducted for the amplify phase of the SCDA. Using (2.47), (2.48), (2.49), and (2.50), the output referred average noise power is given by:

$$\begin{aligned}\bar{v}^2_{o_{amplify}} &= \int_0^\infty \bar{V}^2_{n_{amp}}|H(s)|^2 df = \frac{\bar{V}^2_{n_{amp}} G_0^2}{4\tau} \\ &= \left(\frac{4kT}{3\beta_{amplify} C_{comp}}\right)\left(1+\frac{g_{m3}}{g_{m1}}\right),\end{aligned} \tag{2.54}$$

where $\beta_{amplify} = \frac{C_2}{C_2+C1}$. To input refer the noise power of the amplify phase, the output-referred power is first divided by the magnitude squared of the gain of the amplify phase. This new expression is then divided by the magnitude squared of the gain of the integrator. The input-referred noise power of the amplify phase is then given by:

$$\begin{aligned}\bar{v}^2_{i_{amplify}} &= \left(\frac{4kT}{3\beta_{amplify} C_{comp}}\right)\left(1+\frac{g_{m3}}{g_{m1}}\right)\left(\frac{C_2}{C_1}\right)^2 \\ &\times \left(\frac{(A+1)(C_{pix}+C_F+C_C)C_F}{A(C_F+C_C)C_{pix}}\right)^2.\end{aligned} \tag{2.55}$$

The same noise analysis is conducted for the reset phase of the SCDA. The output referred average noise power is given by:

$$\begin{aligned}\bar{v}^2_{o_{RST}} &= \int_0^\infty \bar{V}^2_{n_{amp}}|H(s)|^2 df = \frac{\bar{V}^2_{n_{amp}} G_0^2}{4\tau} \\ &= \left(\frac{4kT}{3\beta_{RST} C_{comp}}\right)\left(1+\frac{g_{m3}}{g_{m1}}\right),\end{aligned} \tag{2.56}$$

where $\beta_{RST} = \frac{C_3}{C_1+C_2+C_3}$. The input-referred noise power of the reset phase is then given by:

$$\begin{aligned}\bar{v}^2_{i_{RST}} &= \left(\frac{4kT}{3\beta_{RST} C_{comp}}\right)\left(1+\frac{g_{m3}}{g_{m1}}\right)\left(\beta_{RST}\right)^2 \\ &\times \left(\frac{(A+1)(C_{pix}+C_F+C_C)C_F}{A(C_F+C_C)C_{pix}}\right)^2.\end{aligned} \tag{2.57}$$

The equivalent input-referred RMS noise, $N_{e^-_{RMS}}^{SCDA}$, is given by:

$$N_{e^-_{RMS}}^{SCDA} = \left(\frac{(A+1)(C_{pix}+C_F+C_C)C_F}{qA(C_F+C_C)}\right) \times\sqrt{\left[\left(\frac{C_2}{C_1}\right)^2\left(\frac{4kT}{3\beta_{amplify}C_{comp}}\right)\left(1+\frac{g_{m3}}{g_{m1}}\right)+\beta_{RST}^2\left(\frac{4kT}{3\beta_{RST}C_{comp}}\right)\left(1+\frac{g_{m3}}{g_{m1}}\right)\right]} \tag{2.58}$$

and is calculated to be 107 e^-.

The total input-referred RMS noise for the integrator and the SCDA is 529 e^-, and is dominated by the integrator. The reported RMS noise is less than the specified opamp noise tolerance of 845 e^- discussed in Section 2.6.

2.9 Signal-to-Noise Ratio

SNR is calculated as follows:

$$\text{SNR} = 10\log_{10}\left(\frac{\text{Signal Power at Input}}{\text{Noise Power at Input}}\right) \quad \text{[dB]}. \tag{2.59}$$

The input signal voltage power is given by:

$$v_{sig}^2 = \left(\frac{nt_{int}}{C_{pix}} \times I_{sig}\right)^2, \tag{2.60}$$

where the factor of n accounts for the increase in effective integration time. Using the noise estimates summarized in Table 2.6, the input signal for one pixel is given by (2.5), and accounting for the increase in effective integration time, the theoretical SNR when an entire column of pixels is illuminated is 82 dB for $t_{int} = 0.4067$ μs. The theoretical SNR when a single pixel is illuminated is 23.9 dB for the same t_{int}. The dominant noise source is the pixel shot noise and the integrator OTA noise. Note that the selection of this integration time is discussed later in this section and further in Sections 2.9.2 and 2.12.

Figure 2.22 shows how the SNR varies with varying illuminated pixels under these input conditions.

Table 2.6: RMS Noise Summary

Noise Source	RMS Noise (e^-)
Pixel Shot Noise	509
RS Thermal Noise	339
Integrator Reset Noise	80.6
Integrator OTA Noise	518
SCDA Noise	107
Total RMS Noise	812

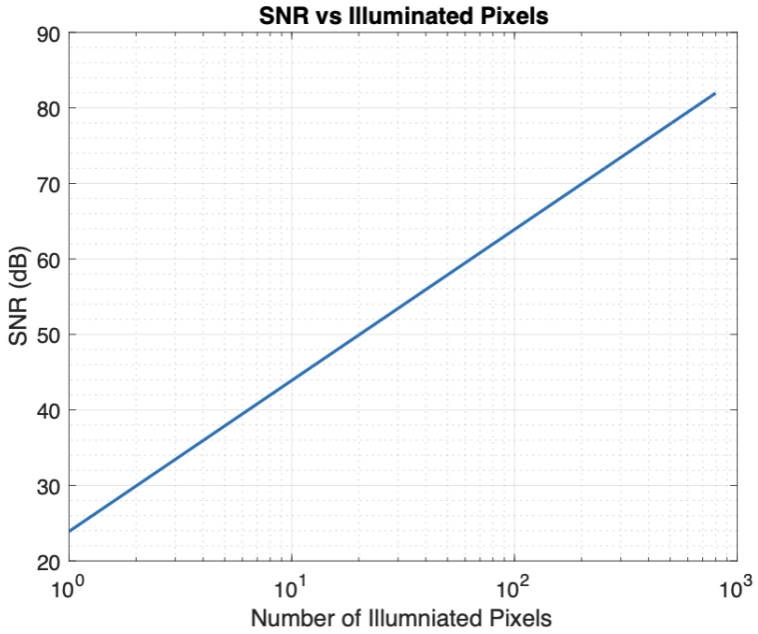


Figure 2.22: Theoretical SNR with varying amounts of illuminated pixels operating under the following input conditions: $I_{signal} = 0.177$ nA per pixel and $t_{int} = 0.4067$ μs.

2.9.1 Limit of Detection

The limit of detection (LOD) is defined as the signal level corresponding to an SNR of 0 dB. It is important to note that t_{int} can vary depending on how the user programs the clocks on the FPGA. In this analysis, the LOD is considered for $t_{int} = 0.4067$ μs while one pixel is illuminated. Figure 2.23 shows how the SNR varies with different input signal levels at a constant $t_{int} = 0.4067$ μs. As shown in Figure 2.23, the LOD of the imager corresponds to a signal of 10.3 pA_{rms} across the column while operating at the fastest frame rate.

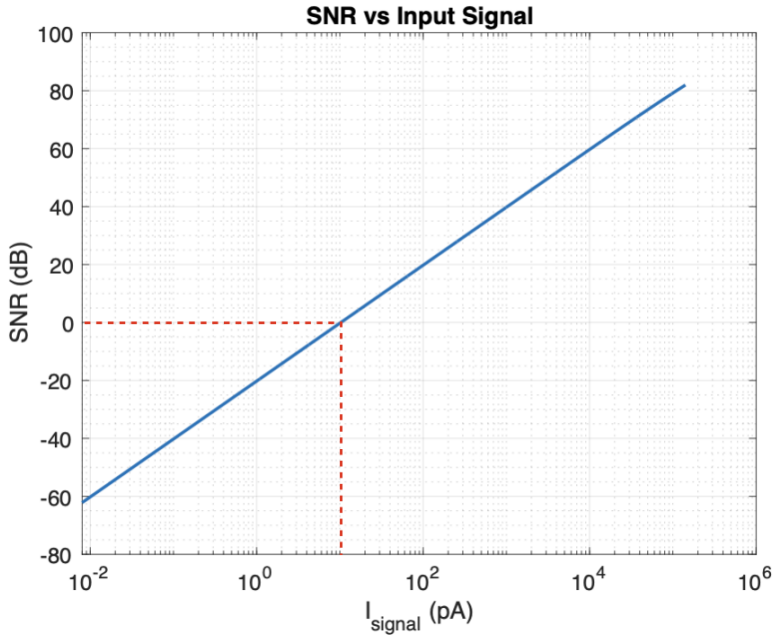


Figure 2.23: Theoretical SNR with varying input signal using $t_{int} = 0.4067$ μs.

2.9.2 Tradeoff between SNR and Frame Rate

To understand the tradeoff between SNR and frame rate, consider how t_{int} is chosen based on the signal level in (2.5). As the charge accumulated on each pixel is summed on the

column line, the maximum voltage of each pixel is such that the summed signals from each pixel on either integrator's C_F is 1.8 V. Figure 2.24 shows the maximum allowable t_{int} that can be used for a given number of pixels on either readout line. Assuming the signals from half the pixels in the column are summed on each line, then $t_{int} = 0.4067$ μs at a signal level of 0.177 nA. This t_{int} limit increases as the signal being used decreases and is the minimum t_{int} estimated for this device as the signal current is calculated based on a synchrotron source.

Figure 2.25 shows that for a constant signal level, the SNR increases as t_{int} increases and as t_{int} increases, the frame rate decreases. A smaller frame rate and longer t_{int} should be used to operate the imager to achieve a higher SNR. At lower signal levels, the time it takes for the column to saturate is longer; therefore, the t_{int} required to reach the same maximum SNR is longer.

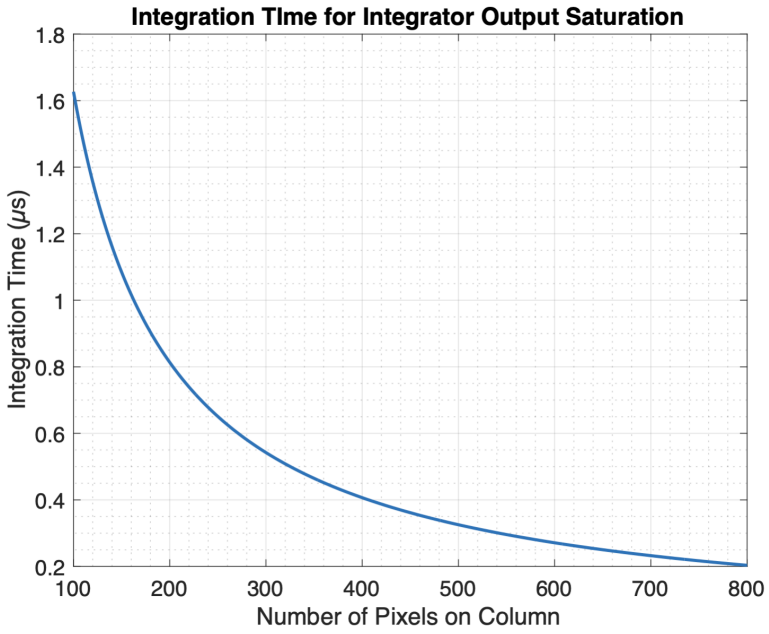


Figure 2.24: Maximum allowable integration time that can be used for a given number of pixels on either readout line before the integrator output saturates.

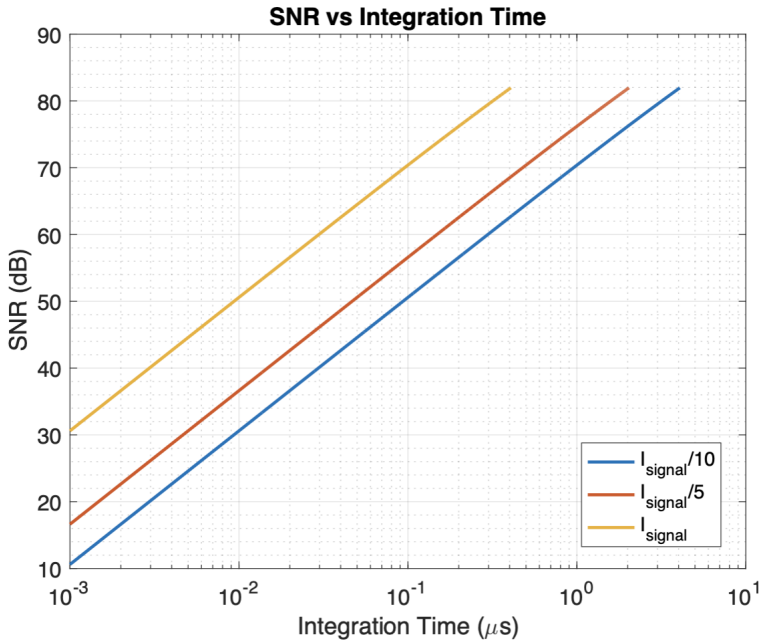


Figure 2.25: SNR variation with integration time at different signal levels ($I_{signal} = 0.177$ nA).

2.9.3 CDM and TDM SNR Comparison

We compare the calculated SNR for CDM and TDM to quantify the SNR improvement for our imager. After adjusting for the circuit differences between TDM and CDM readout, we found that CDM provides a 23 dB improvement in SNR while operating the imager at the same frame rate as shown in Figure 2.26. Given that a single pixel is read out using TDM, we compare the SNR for CDM where a single pixel is illuminated in the column. The improvement in SNR is due to the increase in effective integration time, and averaging of the readout circuit noise.

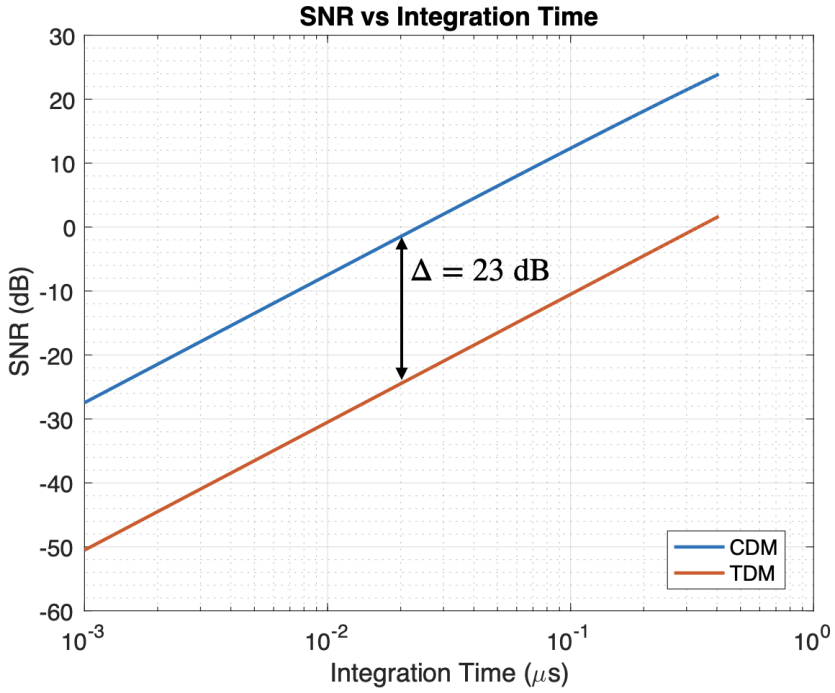


Figure 2.26: Comparison of SNR using CDM and TDM readout.

2.10 Row-Select Control Circuit

The RS control circuit ensures that each RS switch is either open or closed according to the encoding matrix. Figure 2.27 illustrates the implemented circuit. It consists of a scan chain loaded with one column of the encoding matrix during the reset and integration phases. The outputs of each flip-flop in the scan chain are the inputs to the combinational logic that sets the voltage of the gate of each RS switch. The combinational logic includes two three-input AND gates; one to control the gate of M^{+}_{SEL} and the other to control the gate of M^{-}_{SEL}. The AND gate outputs required a buffer to drive the load of the RS line. The implemented buffer is a set of series inverters designed to drive the load of the RS line at a clock speed of 800 MHz. That means the minimum time required to load the scan chain is 1 μs. The transistor-level circuit of the AND gate and buffer is shown in Figure 2.28. The RS line is drawn using the Metal 1 layer. The capacitance per unit length of

this layer is 0.248 fF/μm and the sheet resistance is 0.0078 Ω/sq. Therefore, the lumped capacitance and resistance of the RS line is approximately 0.45 pF and 61 Ω, respectively.

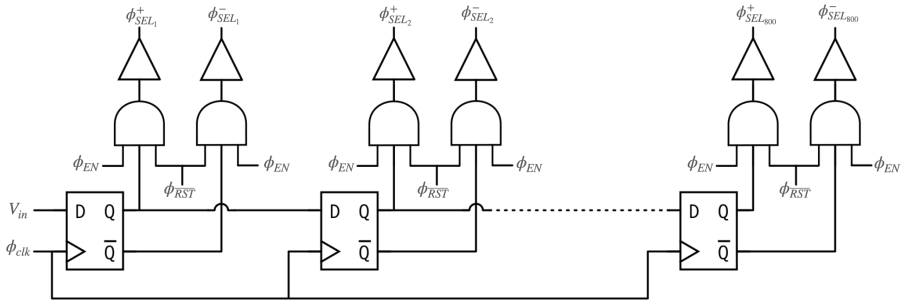


Figure 2.27: Row-select scan chain and combinational logic used to set the gate voltage of the row-select switches.

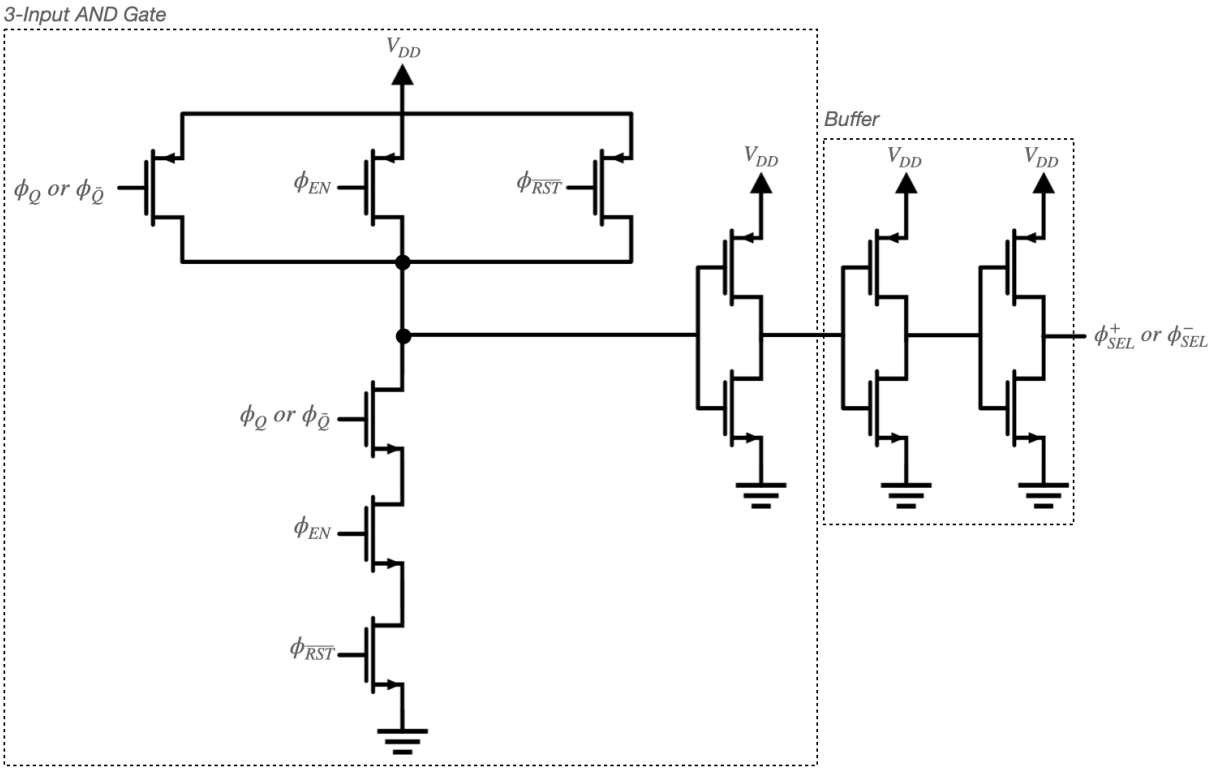


Figure 2.28: Transistor-level circuit of the AND gate and buffer.

2.11 Output Multiplexing

Our imager has sixteen analog output pins. This means the outputs from fifty columns are multiplexed to each output pin. We use a PMOS source follower to buffer the column-line signal. A TG switch, with gates controlled by a 58-bit scan chain, is used to control which output is read out. The output of the TG feeds an NMOS source follower designed to drive the off-chip capacitive load. The fifty column outputs are multiplexed after the output of the SCDA has settled in its amplify phase. The multiplexer is designed to switch between output columns every 80 ns. Therefore, the minimum total time it takes to read fifty column outputs is 4 μs. Note that a 58-bit scan chain is used instead of a 50-bit scan chain to provide design flexibility. Figure 2.29 illustrates the scan chain used to control the TG gate voltages and Figure 2.30 illustrates the circuit used to multiplex each column output.

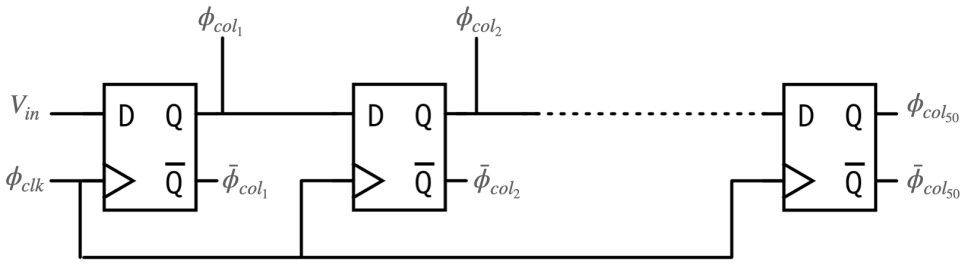


Figure 2.29: Scan chain used to control TG switches to multiplex column outputs.

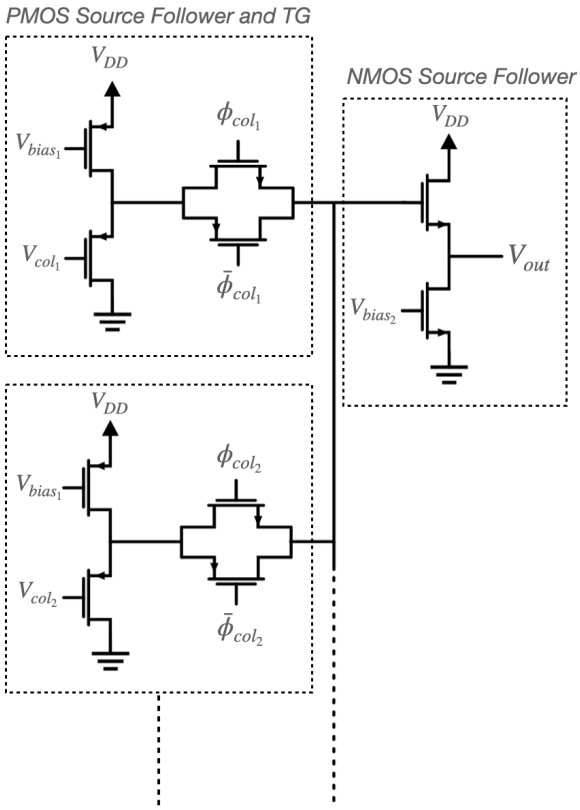


Figure 2.30: Output multiplexer circuit.

2.12 Frame Rate

The minimum target frame rate for our imager is 30 Hz. Therefore, each frame should be captured in 33.3 ms. To construct a single frame using CDM readout, each column is read out n times. To achieve this minimum target frame rate, the time required to read out a single column is 41.6 μs. Figure 2.31 shows the timing diagram for the main components of the imager, where imager operation is divided into four phases.

Phase I is the integration phase of the integrator and part of the reset phase of the SCDA. Based on the discussion in Section 2.9.2, the maximum $t_{int} = 0.4067$ μs while using a synchrotron as the X-ray source. During this phase, charge is stored in the pixel, and

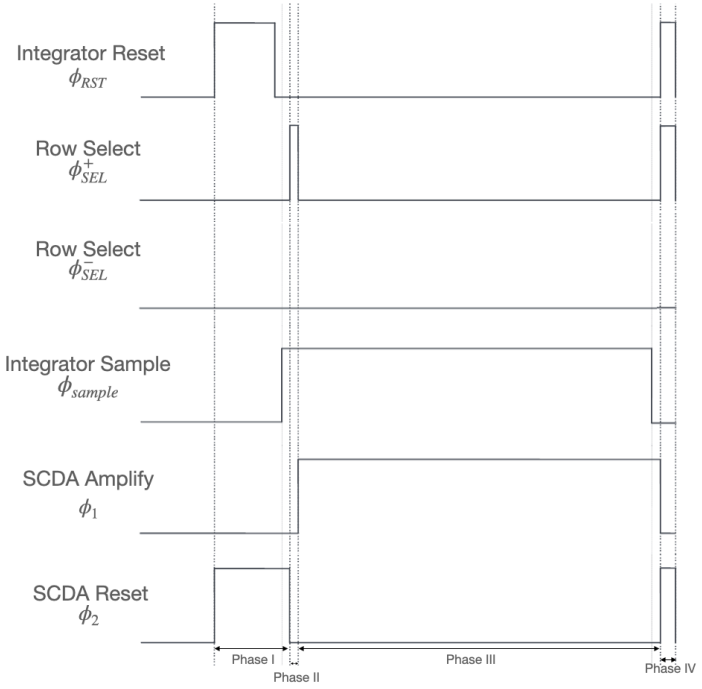
the SCDA is held in reset.

Phase II is the charge transfer phase of the integrator and the non-overlap period for the clocks of the SCDA. The duration of this phase should be much smaller than the time it takes for the OTA to settle. Using this information, as well as simulation and external hardware limitations, the duration of this phase is 0.1 μs.

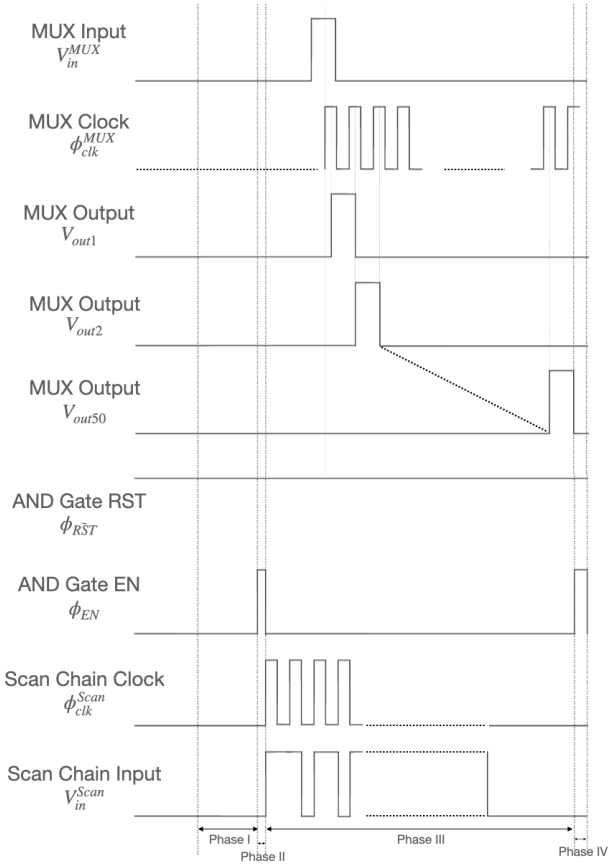
Phase III is the amplifier settling phase of the integrator and the amplify phase of the SCDA. The minimum duration of this phase is given by the addition of the OTA settling time and the time required to multiplex through the outputs of fifty columns. The minimum length of this phase is 5.1 μs. During this phase, the RS scan chain is loaded with the required signal for the gates of the RS switches for Phase IV and the required signals for the gates of the RS switches for the subsequent Phase II. Note that only one RS transistor needs to be high to reset the pixel. As such, the same signals can be used for the Phase IV and the subsequent Phase II. As discussed in Section 2.10, the scan chain was designed to operate at a clock speed of 800 MHz. At this clock speed, the minimum time required to load the scan chain is 1 μs. The external hardware limits the clock speed to 200 MHz. At this clock speed, the minimum time required to load the scan chain is 4 μs. As such, the scan chain can be loaded without adding any additional time to this phase.

Phase IV is the pixel reset phase of the integrator and the SCDA. The minimum time required for this phase is dictated by the settling time of the OTA (1.1 μs). This ensures that the pixel, integrators, and SCDA are fully reset before beginning integration.

Therefore, the fastest time to complete the readout of all column outputs once is 6.7067 μs. The time required to read out a single frame is 5.37 ms, which is a frame rate of approximately 186 Hz. This frame rate estimates are based on using a synchrotron signal source with a photon flux of 10^6 $\frac{\text{photons}}{\text{s}\times\mu\text{m}^2}$. If the flux is lower, then the maximum allowable t_{int} increases, and the frame rate decreases.



(a)



(b)

Figure 2.31: (a) Timing diagram of pixel and readout column control signals. (b) Timing diagram for output multiplexer and row-select scan chain.

2.13 On-Chip Test Structures

We designed on-chip test structures for a column of pixels and the readout circuit to characterize the performance of these components separately from the pixel array.

2.13.1 Test Column

The test column structure is illustrated in Figure 2.32. The pixels are connected to 25 fF MIM capacitors and an off-chip input V_{pix_1} or V_{pix_2} in an alternating pattern. The readout circuit in this test structure contains the two integrators and SCDA. The column output can either be read as an analog signal or a digital signal after having been processed by an ADC.

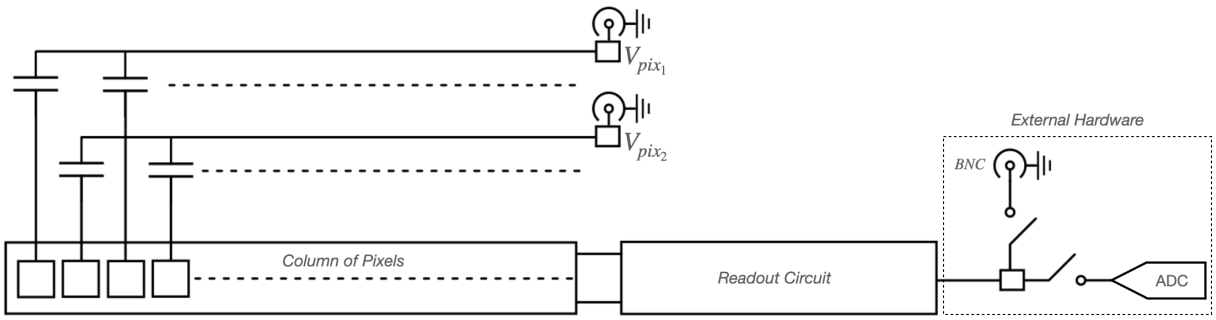


Figure 2.32: Readout circuit test structure.

2.13.2 Readout Circuits

The readout circuit test structure is designed to test the integrator and SCDA separately and together. Figure 2.33 illustrates this test structure. Each integrator has an off-chip input V_{int_1} and V_{int_2}. The output to the integrator can be fed as an input to the SCDA or be read out using the external hardware by closing switches S_{test_1} and S_{test_2}. The output can either be read as an analog signal or a digital signal after having been processed by an ADC. The SCDA can be tested in a similar manner. Off-chip inputs can be used using

the $V_{i/o}$ pin by closing S_{test_2}. The output of the SCDA can either be read as an analog or digital signal after having been processed by an ADC. The integrator and SCDA can be tested simultaneously by using off-chip inputs V_{int_1} and V_{int_2} and closing S_{test_2}.

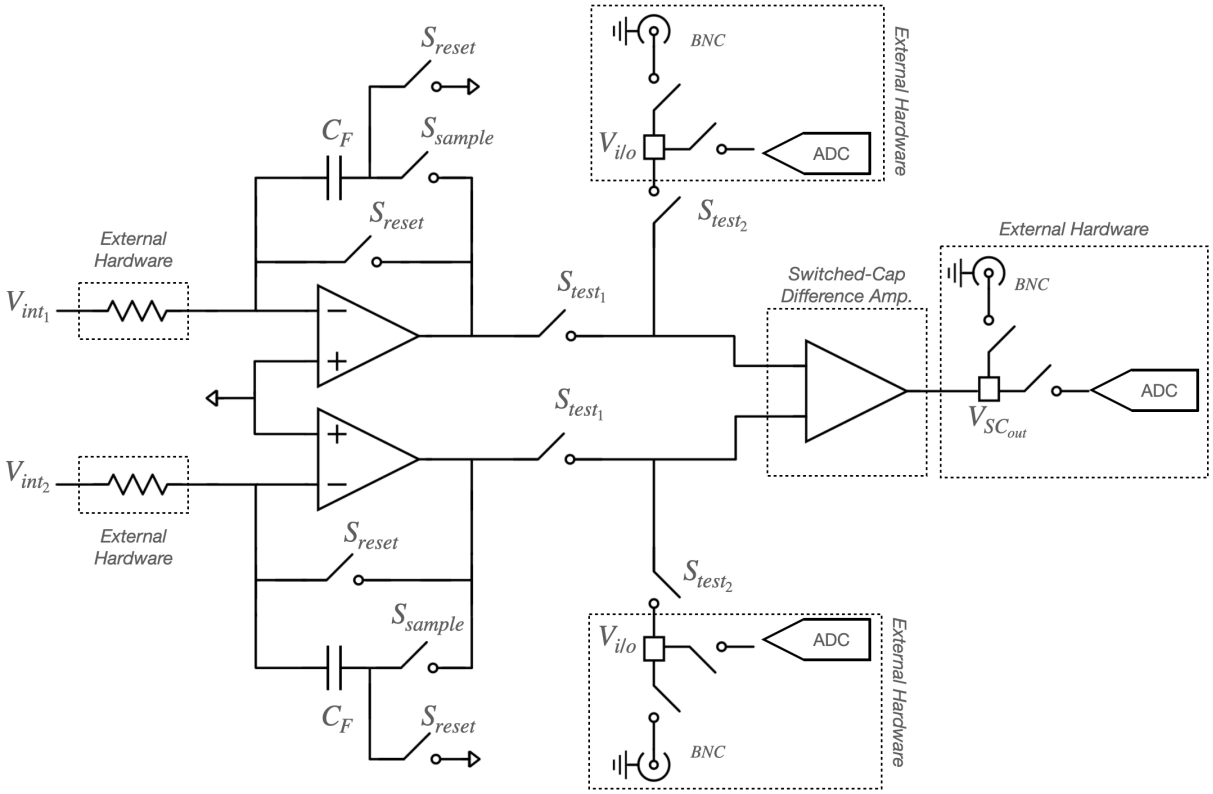


Figure 2.33: Readout circuit test structure.

2.14 CMOS Chip Layout

As discussed in Section 2.3, each readout column is constrained to the width of two columns in the pixel array (4.5 μm). The integrator, SCDA, and output multiplexer is constrained to a length of 755 μm as shown in Figure 2.8. The final chip layout is shown in Figure 2.34. We now discuss the final layout for the readout column and how the OTA bias current is distributed.

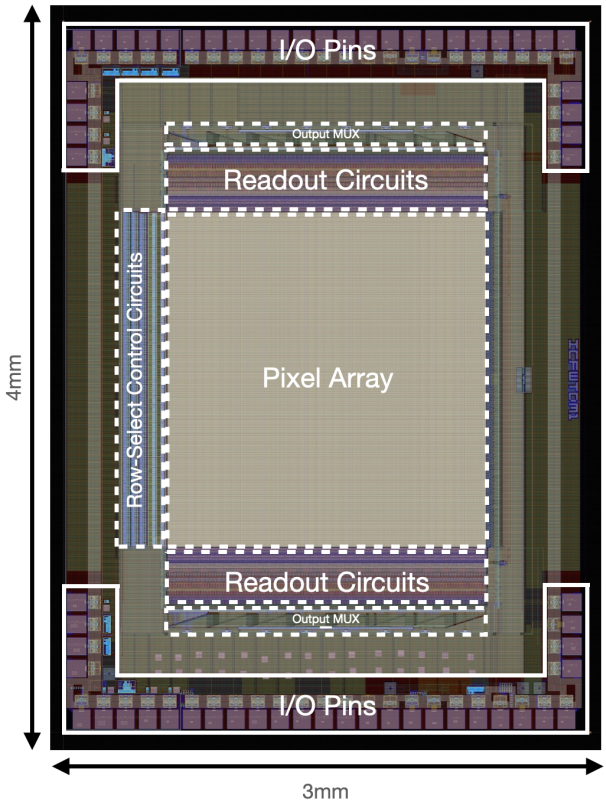


Figure 2.34: Top layout view of the custom CMOS chip with marked regions.

2.14.1 Column Circuit

To maximize the space for the readout column, we use two adjacent readout columns as our building block. This allows us to use any extra space in the adjacent column if necessary.

OTA Layout

Figure 2.35 shows the layout of two OTAs used in adjacent readout columns. The OTAs in Figure 2.35 have the same layout. The OTA on the right is mirrored about the x-axis in order to avoid design-rule violations for the spacing of MIM capacitors and to stay within the area constraints. To maximize space, the gates of M_5, M_7, and M_8 are connected

in the ploysilicon routing layer with a single connection point to a metal layer. Similarly, connections to the power nets all have a single connection point to the Metal 3 lines (shown in green) that run horizontally across the width of all readout columns for all aligned OTAs. The Metal 3 I_{bias} line is discussed in Section 2.15.

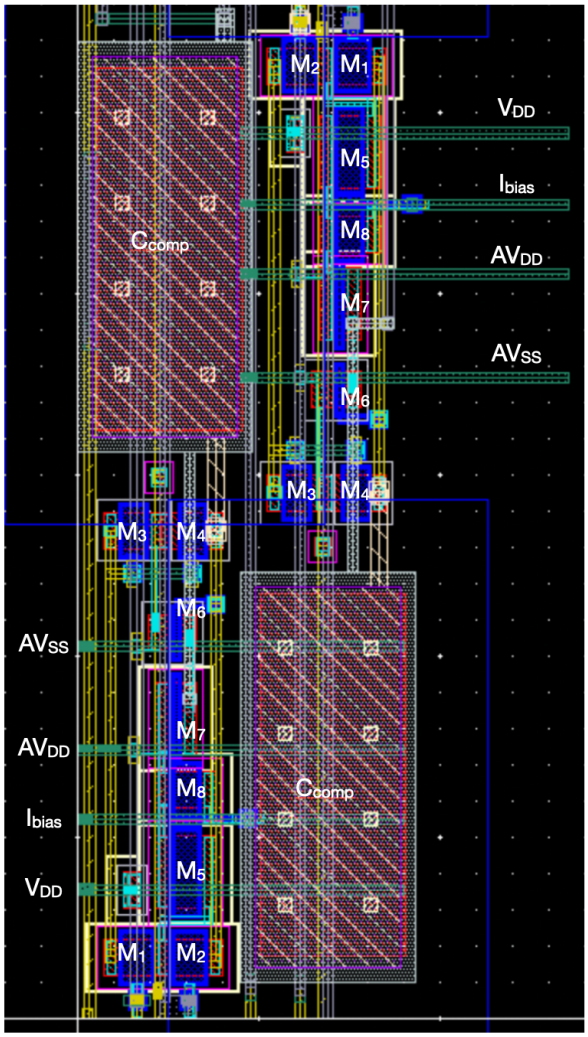


Figure 2.35: Layout of two OTAs used in adjacent readout columns.

Integrator Layout

Figure 2.36 shows the layout of two integrators in adjacent readout columns. The same techniques used in the OTA layout are used in the integrator layout to maximize space in the column. Similar to the OTA layout, the layout for the sample switches and C_F are mirrored about the x-axis in order to avoid design rule violations for the spacing of MIM capacitors and to stay within the area constraints. The sample and reset clock lines have a single connection point in each column to the Metal 3 lines (shown in green) that run horizontally across the width of all readout columns for all aligned sample and reset switches.

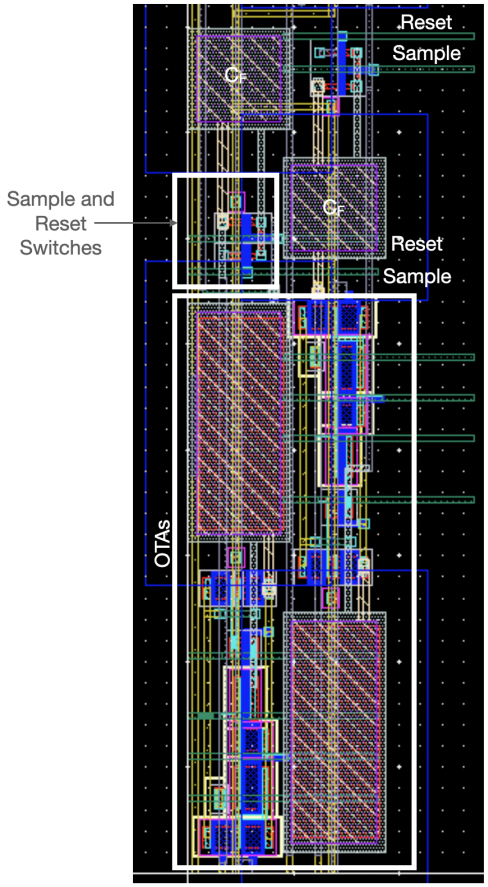


Figure 2.36: Layout of two integrators used in adjacent readout columns.

SCDA Layout

The same techniques discussed for the OTA and integrator layout are used for the SCDA where the layout of the SCDA in an adjacent column is mirrored. The clock lines, ϕ_1, ϕ_2, and ϕ_3, run horizontally across the width of all readout columns for all aligned blocks of switches. A picture of the layout is not included as the length of the circuit layout prevents a detailed view of the layout components.

Figure 2.37 shows the readout columns on one side of the pixel array. The total length of the readout columns excluding the output multiplexer is 347 μm. The metal lines along the side of the readout columns connect all the clock lines and power nets that run horizontally across the readout columns.

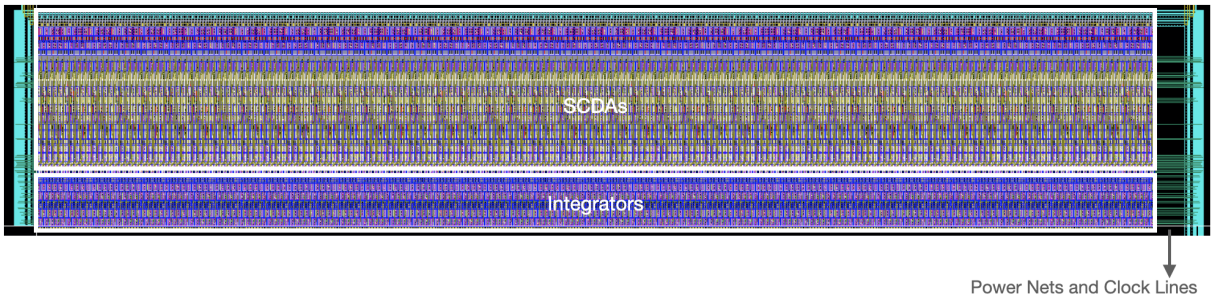


Figure 2.37: Layout of an array of readout columns on one side of the pixel array.

2.15 OTA Bias Current

The bias current is set using an off-chip resistor and on-chip current mirror as shown in Figure 2.38. There are two arrays of readout columns, one on each side of the pixel array, whose biases are set separately off-chip using the circuit in Figure 2.38. Each OTA requires a 0.1 μA bias current. There is a total of 402 readout columns (on each side of the pixel array), including the test structure and columns, and each readout column contains three OTAs. To properly bias the OTAs in one array of readout columns, the variable resistor, R,

is set such that $I_{off-chip} = 120.6\ \mu$A. The length and width of the two NMOS transistors, $M_{1,mirror}$ and $M_{2,mirror}$, are 0.72 μm and 1 μm, respectively.

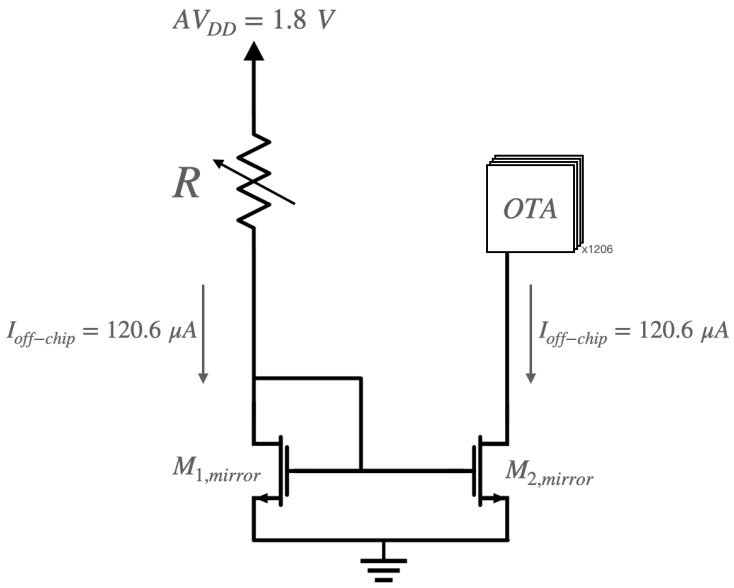


Figure 2.38: Circuit used to set the OTA bias current.

2.16 Imager Static Power Consumption

In Section 2.7.1 we reported the static power consumption of the OTA to be 2.16 μW. To calculate the total static power consumption of the chip, we consider the total number of OTAs used in all readout columns. There are 804 readout columns including the test structures. Each column uses three OTAs which gives a total of 2412 OTAs used on-chip. Therefore the total static power consumption is 5.21 mW.

Chapter 3

Experimental Results

In this chapter, we present the design of the external hardware used for characterizing the electronic performance of our imager. We also demonstrate and discuss the measured response of the integrator and SCDA.

3.1 Fabricated CMOS Chip

Figure 3.1 shows a photo of our fabricated CMOS imager. The chip has a 125-μm I/O pad pitch and is packaged in an 84-pin ceramic pin-grid array (PGA) for electronic testing. The details of the chip pinout can be found in Appendix B. For X-ray testing, a 60-μm-thick layer of a-Se must be deposited on the surface of the chip. A shadow mask is used during deposition to cover areas of the chip that do not require a-Se.

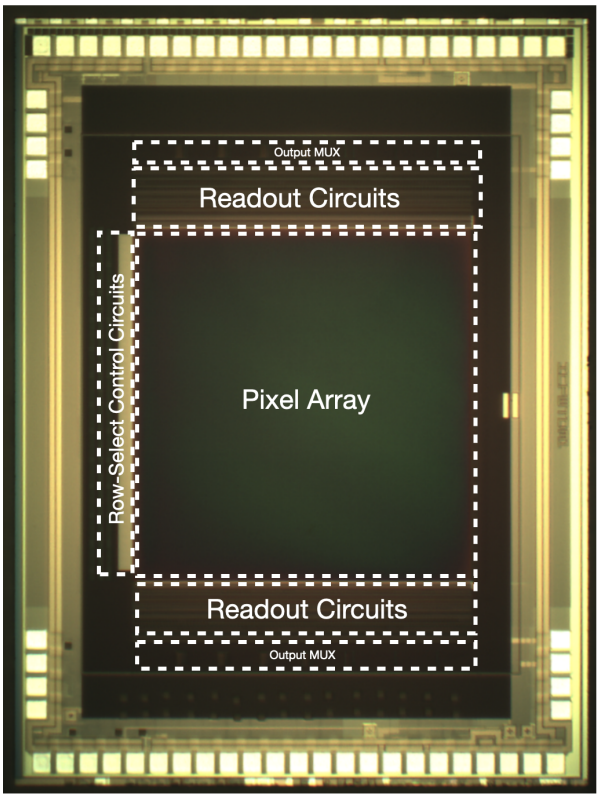


Figure 3.1: Fabricated custom CMOS imager.The chip measure 3 mm × 4 mm.

3.2 External Hardware

We designed a custom four-layer PCB to digitize analog outputs from the imager, digitally control the imager, facilitate data transfer to a PC, and provide a method to use the on-chip test structures, as shown in the block diagram in Figure 2.2. Figure 3.2 shows an annotated picture of the PCB and the component blocks.

Our imager is mounted on the PCB using a PGA IC socket. We choose this socket because it allows us to easily swap out chips without soldering them to the PCB. The imager analog outputs are first fed into a buffer (TI-BUF602). This drives the differential out ADC driver (TI-THS4541), which converts the single-ended analog output to a differential signal used as an input to the ADC. It was also designed specifically to interface with the

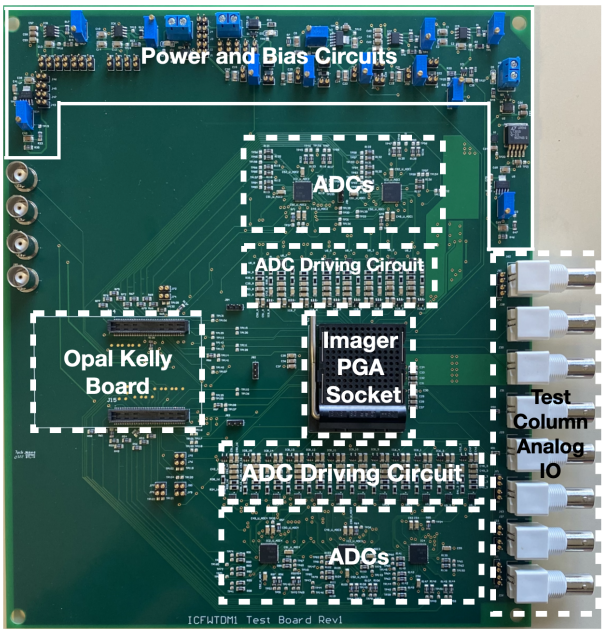


Figure 3.2: PCB Layout and annotated component blocks.

ADC that is implemented. The thermal input-noise PSD reported for the buffer and fully differential amplifier is 4.8 nV/$\sqrt{\text{Hz}}$ and 2.2 nV/$\sqrt{\text{Hz}}$, respectively. The total integrated noise is 16 μV_{RMS} over a bandwidth of 5.43 MHz. This corresponds to an input-referred noise of 0.0025 e^-, which has a negligible effect of the SNR presented in Chapter 2.

3.2.1 ADC

We aim to take at least two samples of the ADC output every frame. Since the on-chip output multiplexer can multiplex the output columns at 12.5 MHz, the minimum ADC sampling frequency is 25 MHz. The TI-ADC342x family of ADCs meets this requirement, so we implement the 12-bit ADC3422. Although we designed the OTA for 8-bit resolution per the specifications discussed, the availability of parts at the time of PCB assembly affected our ADC choice. The quantization noise power of the ADC, $\bar{V}_Q$, is given by:

$$\bar{V_Q} = \frac{V_{LSB}}{\sqrt{12}}, \tag{3.1}$$

where V_{LSB} is the LSB voltage of the ADC. With a 1.8 V reference voltage and 12-bit nominal resolution, $\bar{V_Q} = 0.127$ $\mathrm{mV_{RMS}}$. This corresponds to an input-referred noise of 0.0198 $\mathrm{e^-}$, which has a negligible effect of the SNR presented in Chapter 2. The ADC outputs are differential 1.8 V LVDS signals.

3.2.2 FPGA

An Opal Kelly XEM7310 board with a Xilinx Artix-7 FPGA is used to digitally control the imager and components on the PCB, and transmit data to a PC. The Opal Kelly board is connected to the PCB using basic blade and beam board-to-board connectors.

3.2.3 PCB Noise

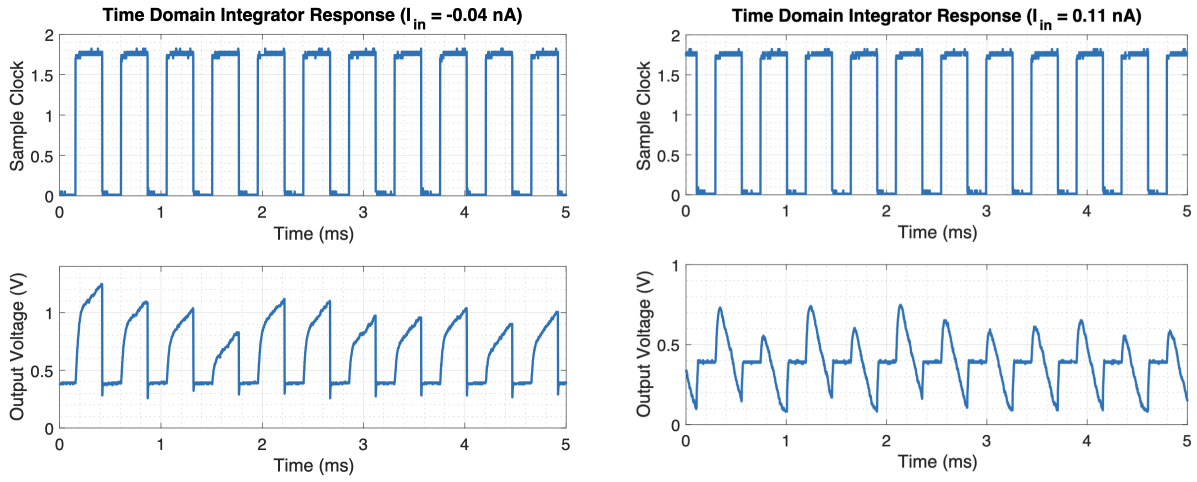
Table 3.1 summarizes the on-board noise measured before and after we made modifications for chip testing. We found that the TI-BUF602 components, TI-THS4541 amplifiers, and ADCs were the major contributor to noise on the power, ground, and common-mode voltage nets. As such, we removed these parts from the PCB. We added additional decoupling capacitors on the PCB to reduce the noise so that the measured noise on the power, ground, and common-mode nets were close to the combined noise of the oscilloscope and power supplies (PS).

Table 3.1: RMS noise measured on the PCB.

Net	Before Modification ($\mathrm{mV_{RMS}}$)	After Modification ($\mathrm{mV_{RMS}}$)
$\mathrm{AV_{DD}}$	9.23	1.16
$\mathrm{AV_{SS}}$	7.09	1.16
$\mathrm{V_{CM}}$	6.74	1.12
Oscilloscope & PS	1.12	1.12

3.3 Integrator

We measure the integrator performance using the test structure shown in Figure 2.33. While testing the integrator, we hold the SCDA in the test structure in reset. The integrator is isolated from the SCDA as the input switches M_1 and M_{10} are open. Input voltages are applied through a BNC on the PCB at V_{int_1} or V_{int_2} and we measure the output by closing the S_{test_1} and S_{test_2} switches. The input current flowing into or being pulled from the integrator can be calculated based on the input voltage applied at V_{int_i}. Figure 3.3 shows the time domain output of the integrator at two different input currents.



(a) (b)

Figure 3.3: (a) Time-domain output of the integrator with an input current of -0.04 nA. (b) Time domain output of the integrator with an input current of 0.11 nA.

The time-domain output voltage shows an initial spike when transitioning from the reset to the sample phase that varies from cycle to cycle in amplitude and duration. After this voltage spike, the integrator behaves as expected, which can be seen through the linear change in voltage. The initial spike in output voltage causes the measured output (voltage at the end of the sample phase) to vary. The variation in output voltage is measured to range up to 172 mV_{rms}. As a result, we take an average of over 200 cycles for each applied input current.

The measured behaviour of the integrator can be attributed to parasitic capacitance, C_{par}, of the PGA packaging and PGA socket at the input of the integrator. We estimate that $C_{par} \approx 2.84$ pF and is much larger than C_F. When the sample switch closes, the integrator is now being operated as a capacitive gain amplifier with a gain of 143 V/V as shown in Figure 3.4.

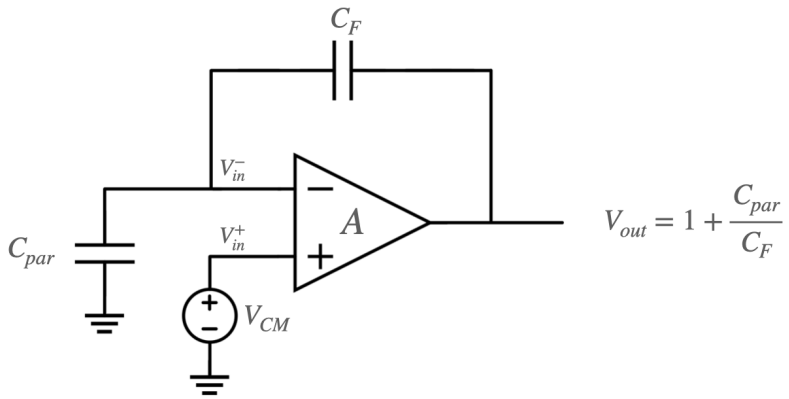
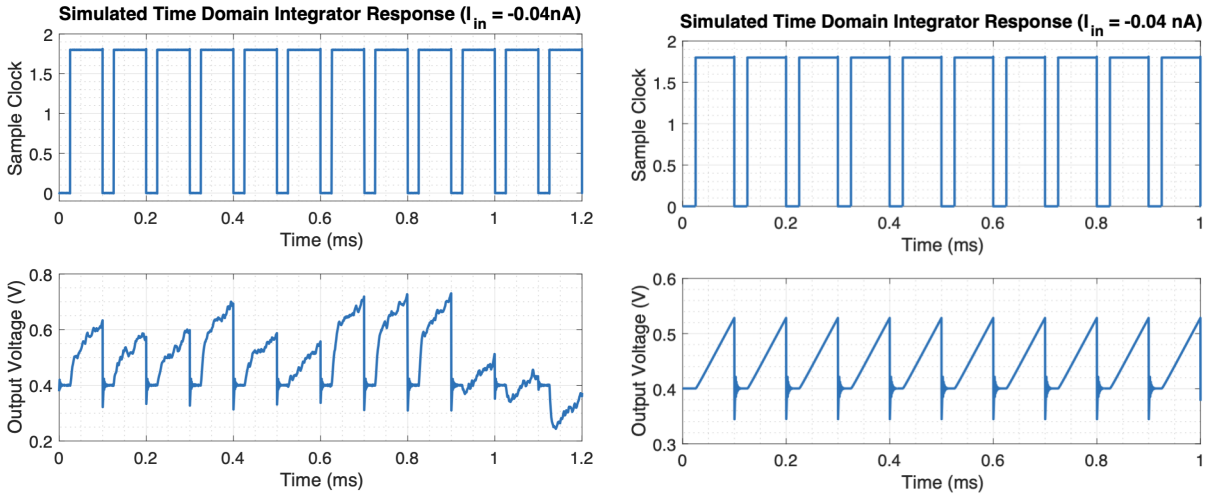


Figure 3.4: Capacitive gain amplifier model of the integrator when $\phi_S ample$ closes.

Any variation on the positive terminal of the OTA (i.e. variation on V_{CM}), will get amplified by 143 V/V. We reported the variation on V_{CM} to be 1.12 mV_{RMS} in Section 3.2.3. This equates to a variation in output of 160 mV. This is verified through simulation as shown through the time domain-integrator output whereby a resistor that generates a noise of 1.12 mV_{rms} over a bandwidth of 5.43 MHz is added to the power and common-mode nets as shown in Figure 3.5(a). The simulated output voltage is calculated to vary by 162 mV_{rms}. Figure 3.5(b) shows the simulated integrator time-domain output without accounting for transient noise of the added resistor. The time domain behaviour shown in Figure 3.5(b) shows the expected output of the integrator. There are no voltage spikes at the beginning of the sample phase, and the output ramps linearly with time during the sample phase.



(a) (b)

Figure 3.5: (a) Simulated time-domain output of the integrator with an input current of -0.04 nA with tranient noise. (b) Simulated time-domain output of the integrator with an input current of -0.04 nA without transient noise.

Figure 3.6 shows the integrator's simulated and measured transfer characteristic (TC). Note that the jump in output voltage for the simulated TC with C_{par} is caused by the variation in voltage spikes at the beginning of the sample phase.

The linear region of the TC can be used to calculate the value of C_F. The simulated C_F, without considering the parasitic capacitance, is 20.2 fF. The simulated C_F considering the parasitic capacitance is 51 fF, and the measured C_F is 45.8 fF. The difference in calculated C_F of the two simulation cases is a result of the size of C_{par} at the input node of the integrator and the variation on V_{CM}. These simulations show the impact of the parasitic capacitance on the measured TC.

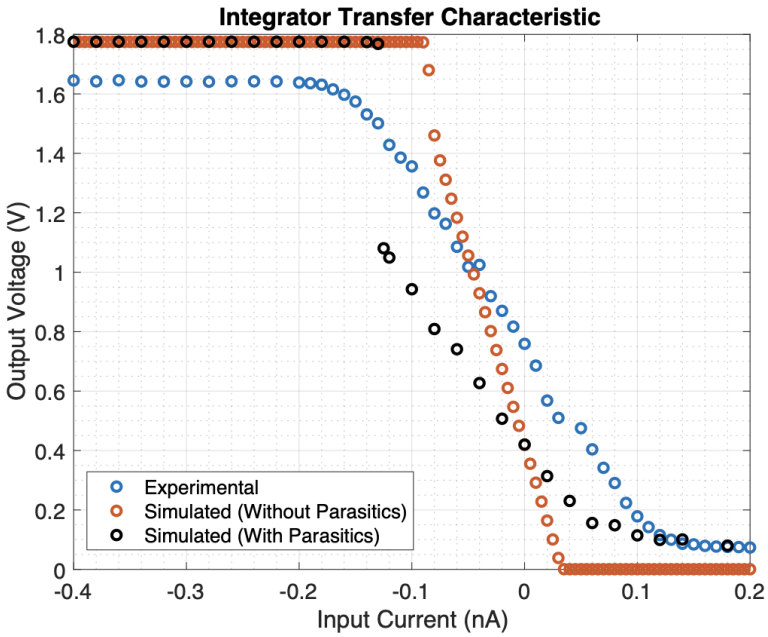


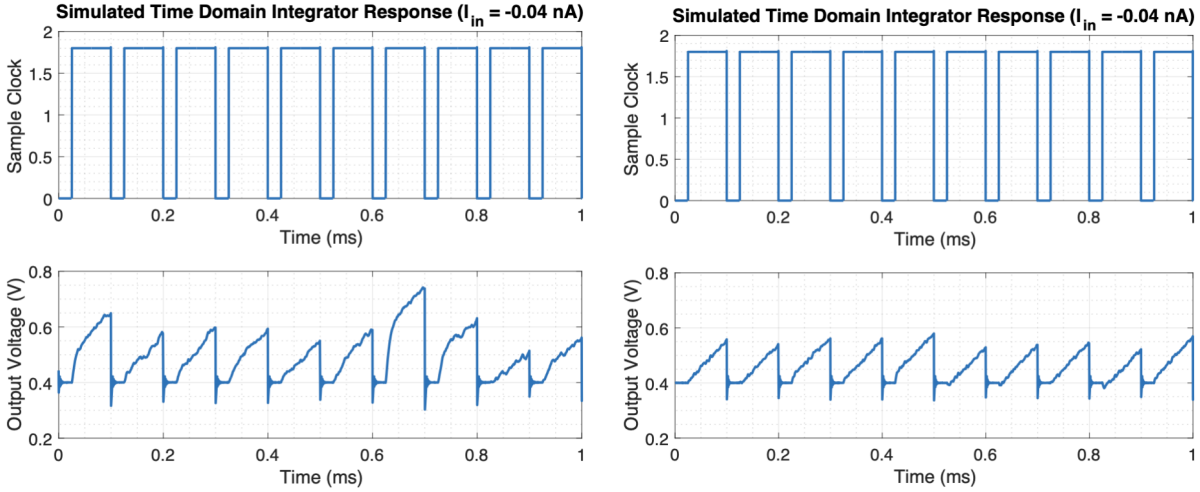
Figure 3.6: Integrator transfer characteristic.

The simulated time domain response of the integrator without the variation of V_{CM} for the estimated C_{par} and the estimated C_C is shown in Figure 3.7(a) and Figure 3.7(b), respectively. The variation in output voltage is due to the thermal noise of the OTA and the large capacitance at the input node of the integrator as previously explained. The variation in output voltage for the test structure using C_{par} is given by:

$$\Delta V = (V_{Noise}^{OTA}) \times \left(1 + \frac{C_{par}}{C_F}\right) = 111.5 \text{ mV} \tag{3.2}$$

The estimated variation in output voltage for the readout columns of the imager is given by:

$$\Delta V = (V_{Noise}^{OTA}) \times \left(1 + \frac{C_C}{C_F}\right) = 29.6 \text{ mV} \tag{3.3}$$



(a) (b)

Figure 3.7: (a) Simulated time-domain output of the integrator with an input current of -0.04 nA, C_{par} at the input node, and without V_{CM} variation. (b) Simulated time-domain output of the integrator with an input current of -0.04 nA, C_C at the input node, and without V_{CM} variation.

The simulated variation in output voltage using C_{par} and C_C at the input node of the integrator is 97.4 $\mathrm{mV_{RMS}}$ and 18.4 $\mathrm{mV_{RMS}}$, respectively. This means that for the imager readout columns we expect a minimum of 18.4 $\mathrm{mV_{RMS}}$ variation in the integrator output as a result of the OTA noise and large C_C. This variation is 5.3× smaller than the minimum variation shown using the test structure. This indicates that the readout columns would suffer from noise and may cause inaccuracy in the imager output.

3.3.1 Noise PSD

We measured the noise PSD of the integrator OTA while holding it in its reset phase and isolated from the SCDA. The output voltage is collected over a long period, and a Fourier transform is used to estimate the PSD. Figure 3.8 shows the PSD of the integrator. The total integrated noise is 1.1 $\mathrm{mV_{rms}}$ over a bandwidth of 6.45 kHz. Note that the spike at approximately 1 kHz can be attributed to interference from the Opal Kelly or other

equipment used in the measurement setup.

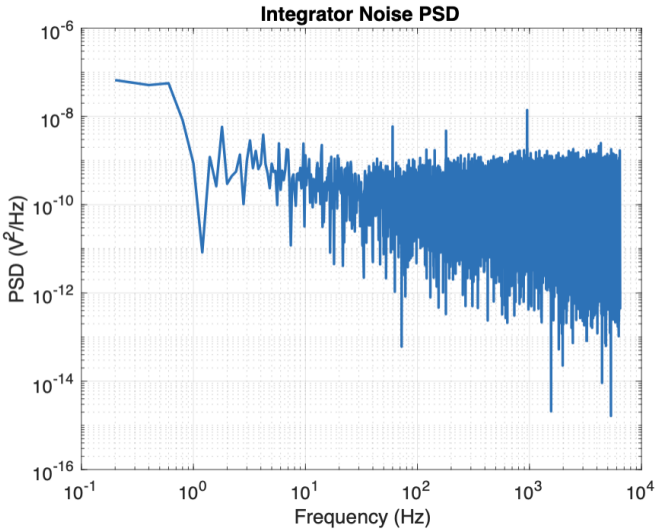


Figure 3.8: Integrator noise PSD.

3.4 Switched-Capacitor Difference Amplifier

We measure the SCDA performance using the test structure shown in Figure 2.33. While testing the SCDA, we hold the integrator in the test structure in reset and isolate it from the SCDA by keeping the S_{test_1} switches open. Input voltages are applied through a BNC on the PCB and by closing the S_{test_2} switches. The differential input voltage is swept by keeping the negative input of the SCDA at the common mode voltage, V_{CM}, and changing the positive input of the SCDA in 100 mV increments. Figure 3.9 shows the simulated and measured VTC of the SCDA.

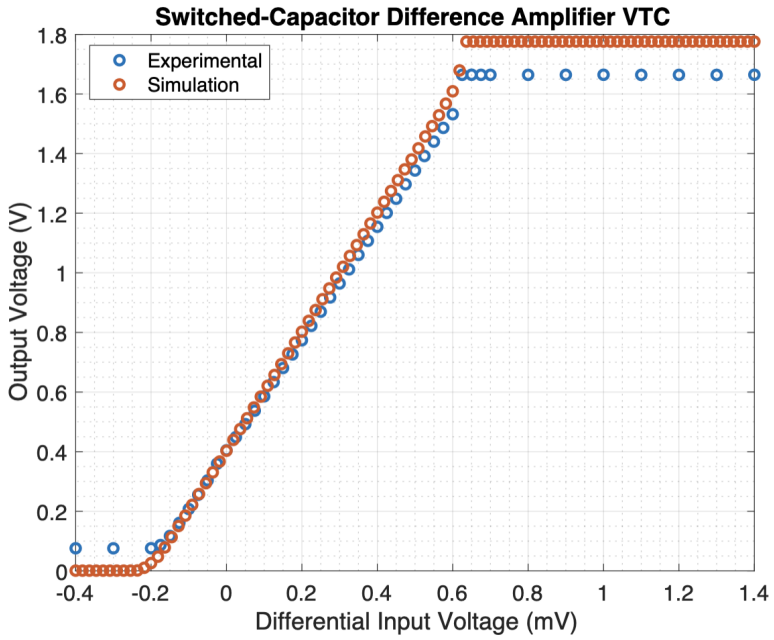


Figure 3.9: Switch-capacitor difference amplifier voltage transfer characteristic.

The voltage gain of the SCDA is measured from the slope of the VTC. As discussed in Section 2.5, the gain of the SCDA is 2 V/V. The simulated gain calculated using the VTC is 1.998 V/V with an input offset voltage of 3.12 mV. The measured gain calculated using the VTC is 1.918 V/V with an input offset voltage of 4.63 mV. This gain corresponds to a relative error of 4%, which can be attributed to a mismatch in capacitor size. Due to area constraints of the column readout circuit, we did not implement any special matching techniques for C_1 and C_2 during the chip layout. Figure 3.10 shows the time domain output of the SCDA at a differential input voltage of 100 mV and the ϕ_1 clock, which is at 1.8 V (logical 1) during the amplify phase.

We average the SCDA output over 1000 cycles for each input voltage. There is a variation in the output voltage from cycle to cycle during the amplify phase. This results from the noise on the PCB, power supplies, and oscilloscope. To confirm the observed cycle-to-cycle variation, we perform an SCDA simulation whereby a resistor that generates a noise of 1.12 $\mathrm{mV_{rms}}$ over a bandwidth of 5.43 MHz is added to the power and common-

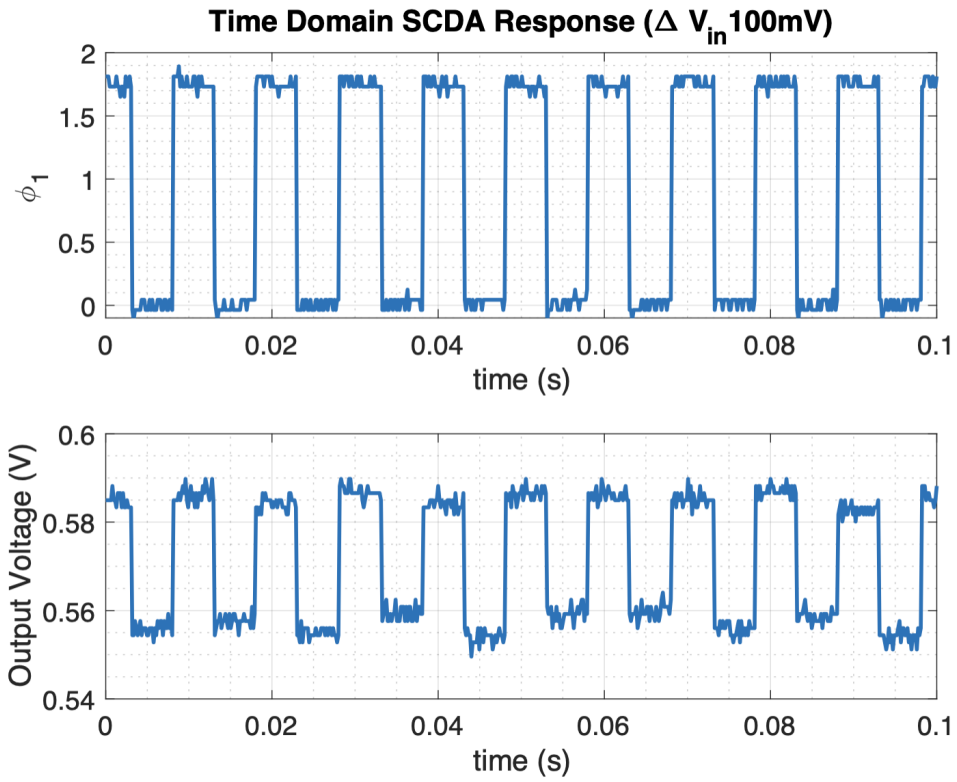
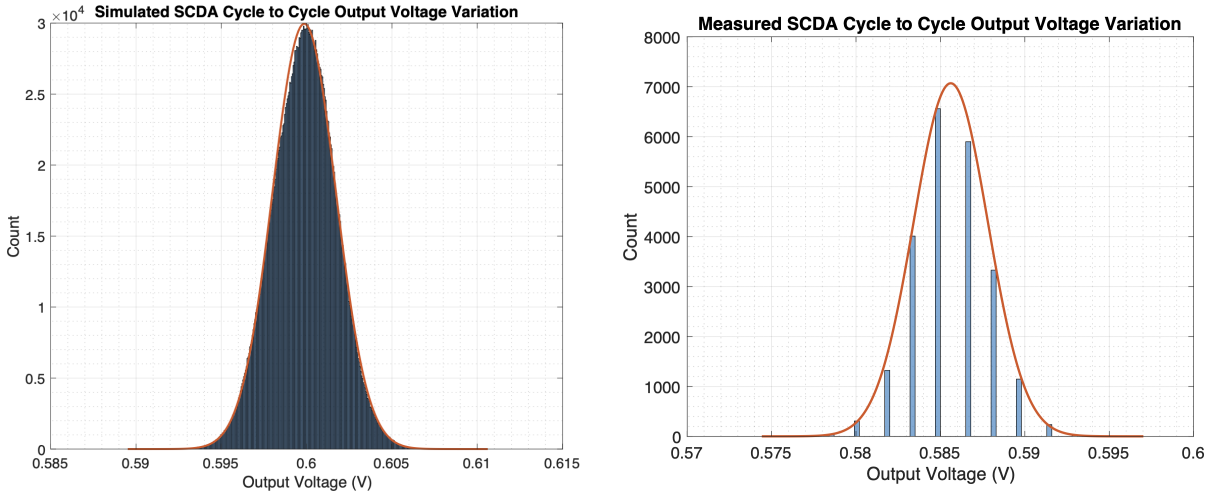


Figure 3.10: Switch-capacitor difference amplifier time domain output.

mode nets. Figure 3.11 shows a histogram of the simulated and measured SCDA outputs with a differential input of 100 mV. It can be seen that the output voltage follows a Gaussian distribution. The simulated RMS noise of the output voltage is 1.85 mV_{rms}. The measured RMS noise of the output voltage is 2.2 mV_{rms}. Therefore, the simulated input-referred SCDA noise is 0.93 mV_{rms} and the measured input-referred SCDA noise is 1.15 mV_{rms}.



(a) (b)

Figure 3.11: (a) Histogram of the simulated SCDA output voltage with 1.12 mV_{rms} noise added to power and common-mode nets. The resulting noise in output voltage is 1.85 mV_{rms}. (b) Histogram of the measured SCDA output voltage. The resulting noise is 2.2 mV_{rms}.

3.4.1 Frequency Response

We also tested the frequency response magnitude of the SCDA. We apply a 100 mV sine wave to the positive input of the SCDA while holding the negative input of the SCDA at V_{CM}. We also clock the SCDA at a sampling frequency of 20 kHz. The frequency of the input sine wave is therefore limited to 10 kHz. The expected output of the SCDA is a 200 mV sine wave over this frequency range. The closed loop bandwidth is given by (2.23). Theoretically, the output of the SCDA is a 200 mV sine wave up to $f_{-3dB_{CL}}$. However the external hardware limits the sampling frequency we are able to use to operate the SCDA. Figure 3.12 shows the theoretical, simulated and measured output from the SCDA averaged over at least 5 sine wave periods. The differences in the measured and simulated response can be attributed to the noise in the measurement setup.

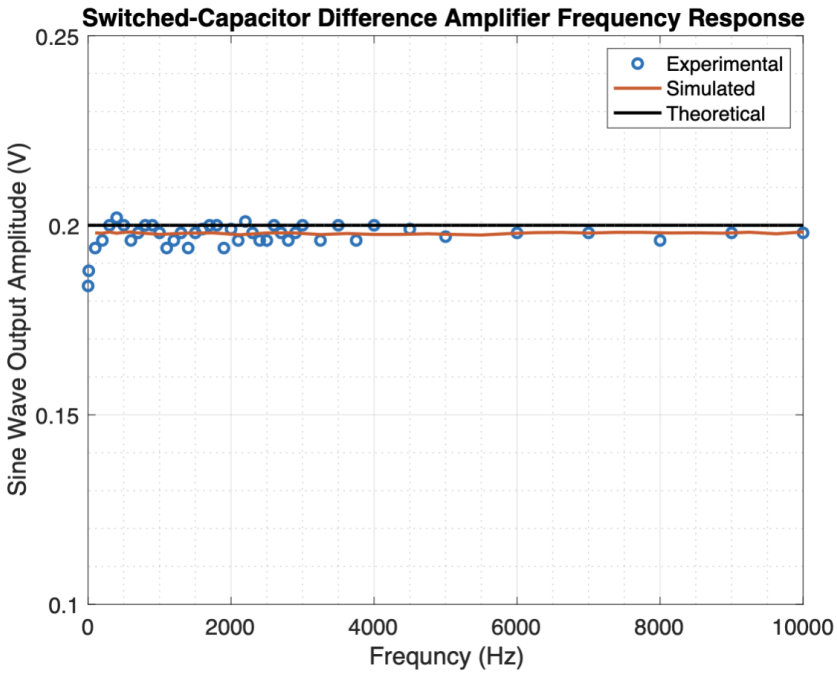


Figure 3.12: Switch-capacitor difference amplifier frequency response magnitude.

3.4.2 Noise PSD

We measured the noise PSD of the SCDA OTA while holding it in its reset phase and isolated from the integrator. Figure 3.13 shows the measured PSD of the SCDA. The total integrated noise is 1.23 mV_{rms}. Note that the spike at approximately 1 kHz can be attributed to interference from the Opal Kelly or other equipment used in the measurement setup.

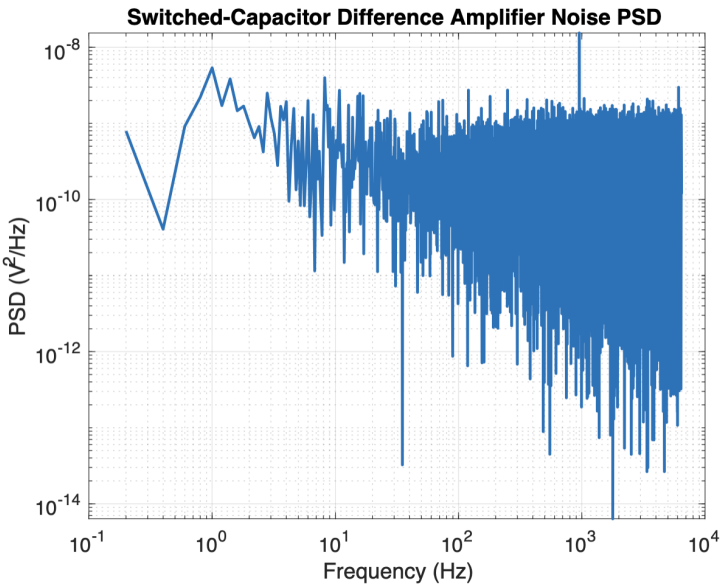


Figure 3.13: Switch-capacitor difference amplifier noise PSD.

3.5 Results Summary

Table 3.2 summarizes the simulated and measured parameters of the integrator and SCDA. The integrator shows a large variation in output voltage due to the large parasitic capacitance at the input node and the noise on the V_{CM} net. This effect should be less significant in the imager readout columns. The measured gain of the SCDA is 1.918 V/V which is within 4% of the desired gain. Note that the pixel test column evaluation and X-ray imaging will be done at a later date.

Table 3.2: Summary of simulated and measured integrator and SCDA parameters.

Parameter	Simulated	Measured
Integrator Capacitor (C_F)	20.2 fF (51 fF[1])	45.8 fF
Input-Referred Integrator OTA Noise	0.78 mV_{rms}	1.1 mV_{rms}
Integrator Output Swing	1.77 V	1.57 V
SCDA Gain	1.998 V/V	1.918 V/V
SCDA Input-Offset Voltage	3.12 mV	4.63 mV
SCDA Bandwidth	1.78 MHz	10 kHz [2]
Input-Referred SCDA OTA Noise	0.78 mV_{rms}	1.23 mV_{rms}
Input-Referred SCDA Noise	0.93 mV_{rms}	1.15 mV_{rms}
SCDA Output Swing	1.77 V	1.57 V

[1]Simulation including the parasitic capacitance.

[2]Measurements for the bandwidth of the SCDA are limited by the external hardware and measurement setup.

Chapter 4

Conclusion

X-ray imaging is widely used for materials characterization. The rise in the use of nanomaterials means a high-spatial-resolution characterization technique is required to consistently develop these materials. This project aimed to design a high-spatial-resolution X-ray imager for applications such as DFXM. The imager would take advantage of a-Se's detection efficiency, inherent spatial resolution, and low dark current and improve existing CMOS imagers by reducing pixel size, and increasing frame rate.

To achieve high spatial resolution, we aimed to reduce the size of the smallest pixel previously implemented in direct-conversion X-ray imagers. Therefore, we built a 2.252μm $\times$ 2.363 μm 2T-PPS. To overcome the low SNR of the PPS, we implement CDM readout, which helps reduce noise by allowing for a longer effective integration time.

We designed the OTA for the integrator and SCDA to have dc gain of 1900 V/V, and GBW of 5.43 MHz. The OTA exhibits a settling time of 1.1 μs, which allows for a maximum imager frame rate of 186 Hz, a six-fold improvement on the design specification of 30 Hz.

The total input-referred RMS noise of the signal chain was calculated to be 812 e^-, dominated by the pixel shot noise and integrator OTA noise. The total RMS noise is less than the noise tolerance of 1043 e^- for an 8-bit dynamic range. The theoretical SNR of the imager was found to be 82 dB when an entire column of pixels is illuminated under the

signal from a synchrotron, and 23.9 dB when a single pixel is illuminated. Use of CDM readout shows a 23 dB improvement in SNR compared to TDM readout.

The integrator showed linear behaviour when the outputs were averaged over 200 cycles. It did not behave as expected and showed a positive spike in voltage at the beginning of the integrator's sample phase that varies from cycle to cycle. The behaviour can be attributed to the large parasitic capacitance of the PGA packaging and PGA socket at the input of the integrator along with the noise of the external hardware and measurement setup. It was shown that the minimum variation will be 5.3× smaller when used in the readout column because the column capacitance is less than the parasitic capacitance at the input node.

The gain of the SCDA was measured to be 1.918 V/V, with an input offset voltage of 4.63 mV. The measured gain is within 4% of the simulated SCDA gain. During operation, cycle-to-cycle variation is observed in the output voltage during the amplify phase due to external hardware and measurement setup noise. The Gaussian behaviour from the different output voltages measured confirms that the cycle-to-cycle variation results from noise.

4.1 Future Work

There are several avenues to pursue this work further. The primary focus of any future work is to test the entire signal acquisition channel using the test column discussed in Section 2.13.1. Once the signal chain is tested and the output is verified, a-Se can be deposited for X-ray imaging. This will allow us to verify the SNR model presented in Section 2, and quantify the spatial resolution of the imager.

Our design can be improved by adding buffers to the output of the test structures. The integrator and SCDA were designed to drive the load of the SCDA output multiplexer, respectively. As such, the high input capacitance of the oscilloscope probes means that a longer settling time is required during measurement, and the circuits could not be tested at the rate for which they were designed to operate.

The next iteration of this design should also include on-chip ADCs. This could reduce the PCB size, reduce cost to procure parts to assemble the PCB, reduce the noise measured on the PCB, and reduce any interference on the chip's output signal.

Lastly, the next iteration of this design should include on-chip current sources to test the integrator in the test structure described in Section 2.13.2. This will help reduce the effect of the parasitic capacitance at the input node of the integrator and reduce the variation in output voltage measured.

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APPENDICES

Appendix A

Illustration of CDM Decoding

This section illustrates the decoding of the CDM readout technique using MATLAB. This example is based on the work presented by *Ouh et al.*, where a 16×8 2T-PPS is used. To replicate this imager, the image shown in Figure A.1 is represented as a 16x8 grid.

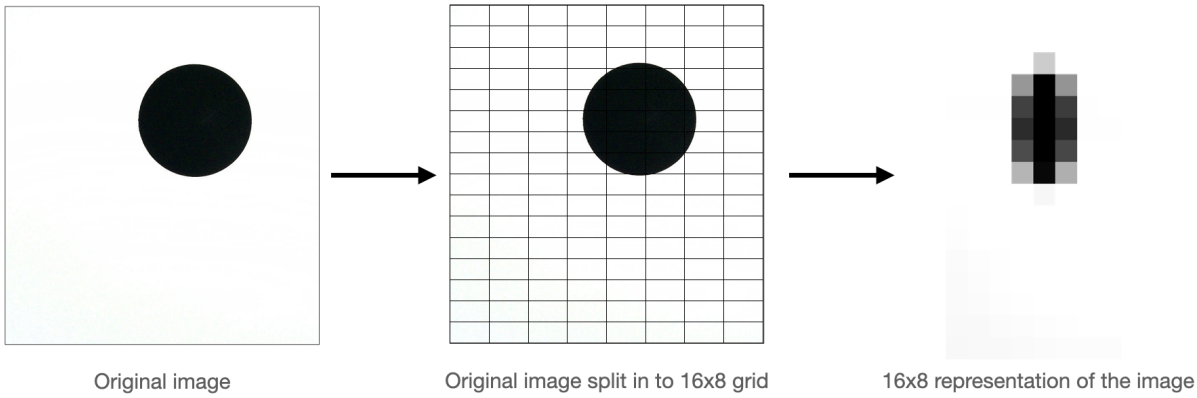


Figure A.1: Original image used to simulate the CDM readout technique and the representation of the image as "captured" bu an image with a 16×8 pixel array.

To simulate an imager, random noise is added to each "pixel" in the 16×8 grid representation of the simulated image capture. As previously explained, each column needs to be read out n times to capture a single frame after decoding. In this example, $n = 16$ and

sixteen "images" are created with random noise added to each pixel to simulate capturing each column of the image 16 times.

The first step in the process is to sum the signal of each column according to the encoding matrix and (1.7). Each image is encoded using one column of the encoding matrix. That is, each column in each image is encoded using the same column of the encoding matrix. This encoding process yields sixteen 1x8 arrays, where each element in the array represents the sum of the photocurrent of each column according to (1.8). This encoding process can be visually represented by Figure A.2, which shows the simulated image, encoding matrix, and the result of the encoding process.

At this point in the simulation, all the summed photocurrents have been collected that are required to decode the image according to (1.9). The summed photocurrents for one column are now multiplied by the inverse of the encoding matrix to yield the signal for each pixel in the column. Hence, the decoded image is formed. This is visually represented in Figure A.3.

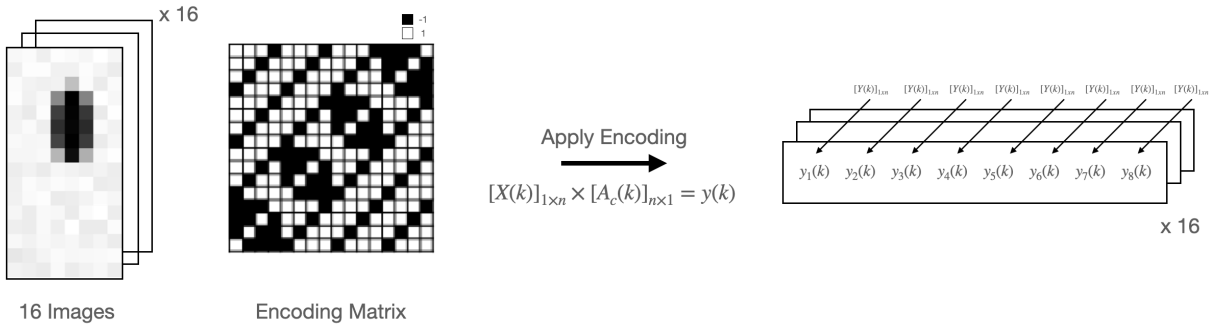


Figure A.2: Illustration of the CDM encoding process using the 16x8 generated images. Encoding matrix taken from [8].

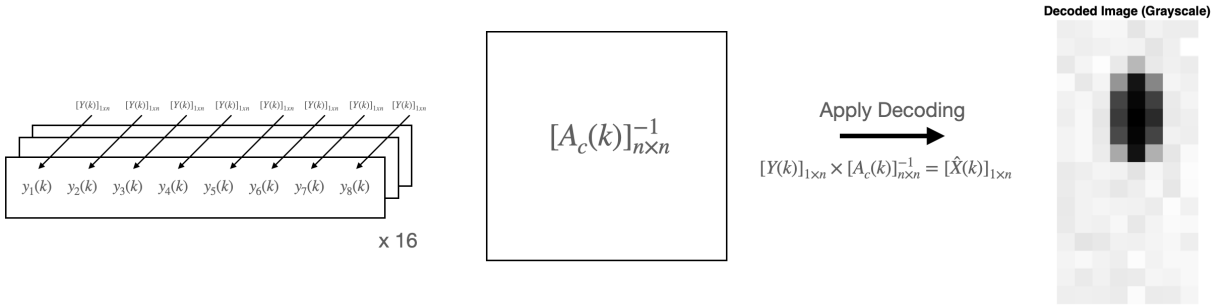


Figure A.3: Illustration of the CDM decoding process using the 16x8 generated images.

The following MATLAB code is implemented for this example:

```
% Encoding Matrix
numColsEncoding = 16;
Ac = [1 1 1 -1 1 1 1 -1 1 1 1 -1 -1 -1 -1 1; ...
      1 1 -1 1 1 1 -1 1 1 1 -1 1 -1 -1 1 -1; ...
      1 -1 1 1 1 -1 1 1 1 -1 1 1 -1 1 -1 -1; ...
      -1 1 1 1 -1 1 1 1 -1 1 1 1 1 -1 -1 -1; ...
      1 1 1 -1 1 1 1 -1 -1 -1 -1 1 1 1 1 -1; ...
      1 1 -1 1 1 1 -1 1 -1 -1 1 -1 1 1 -1 1; ...
      1 -1 1 1 1 -1 1 1 -1 1 -1 -1 1 -1 1 1; ...
      -1 1 1 1 -1 1 1 1 1 -1 -1 -1 -1 1 1 1; ...
      1 1 1 -1 -1 -1 -1 1 1 1 1 -1 1 1 1 -1; ...
      1 1 -1 1 -1 -1 1 -1 1 1 -1 1 1 1 -1 1; ...
      1 -1 1 1 -1 1 -1 -1 1 -1 1 1 1 -1 1 1; ...
      -1 1 1 1 1 -1 -1 -1 -1 1 1 1 -1 1 1 1; ...
      -1 -1 -1 1 1 1 1 -1 1 1 1 -1 1 1 1 -1; ...
      -1 -1 1 -1 1 1 -1 1 1 1 -1 1 1 1 -1 1; ...
      -1 1 -1 -1 1 -1 1 1 1 -1 1 1 1 -1 1 1; ...
      1 -1 -1 -1 -1 1 1 1 -1 1 1 1 -1 1 1 1; ...
];
```

```
% Import test image
I = imread('testIMG.jpg'); % Black dot
I = I(:,:,1);
I = I(1:800, 1:800); % Resize so its divisble by 8 and 16

% Create images based on number of columns in the encoding matrix
sensorReadings = zeros(16, 8, numColsEncoding);

% Resize image to 16x8 pixels
% Take the picture and divide it into 16 rows and 8 columns
% (An average of the pixels within that grid spot is taken
% for the 16x8 represenation)
for z=1:numColsEncoding
    rowCount = 1;
    for i=1:16
        colCount = 1;
        for j=1:8
            % Added "noise" (randi) to model the 16 different images taken
            sensorReadings(i, j, z) = sum(sum(I(rowCount:rowCount+49,...
            colCount:colCount+99))) / 5000 + randi([-10 10], 1);
            colCount = colCount + 100;
        end
        rowCount = rowCount + 50;
    end
end

% Apply [X(k)]*[Ac(k)] = y(k)
% Encoding
y_k = zeros(1, 8, numColsEncoding);
```

```
count = 1;

for i=1:numColsEncoding
    x_k  = sensorReadings(:, :, i)';
    A_k = Ac(:,i);
    y_k(1, :, i) = x_k * A_k;
    count = count + 1;
end

% Apply [Y(k)]*[A(k)]^-1 = [Xhat(k)]
% Decoding
finalIMG = zeros(16, 8);
for i=1:8
    Y_k = squeeze(y_k(1,i,:))';
    col = Y_k/Ac;
    finalIMG(:,i) = col';
end

% Show sample picture taken by imager
figure(1)
newmap1 = mat2gray(mean(sensorReadings,3));
imshow(newmap1, 'InitialMagnification','fit')
title('16x8 represenation of Image (Grayscale)')
set(gca, 'FontSize', 14);

figure(2)
newmap2 = mat2gray(finalIMG);
imshow(newmap2, 'InitialMagnification','fit')
title('Decoded Image (Grayscale)')
set(gca, 'FontSize', 14);
```

Appendix B

CMOS Chip Pinout

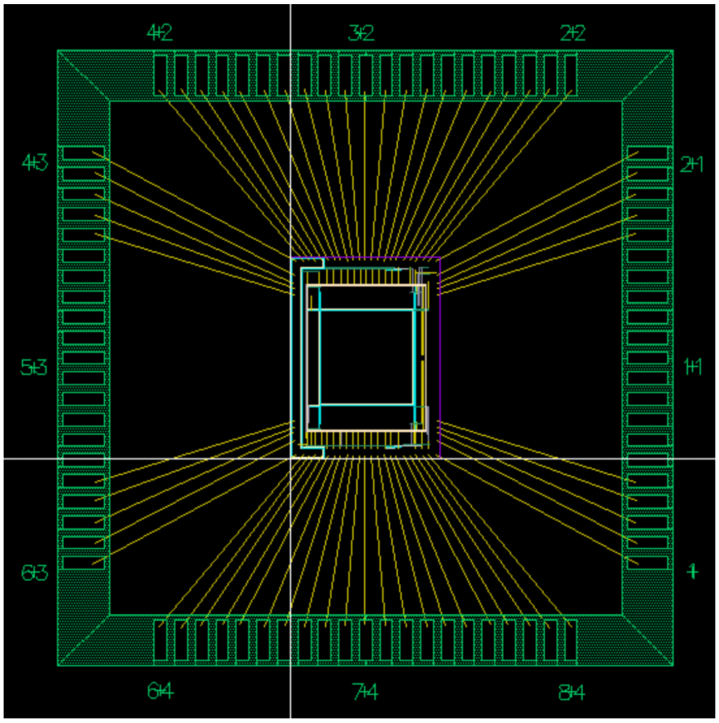


Figure B.1: CMOS chip bonding diagram (Product Number: SSM P/N CPG08421).

Table B.1: Chip pinout details.

Pin Number	Name	Direction	Notes
1	V_Test_Out	Analog Out	Test column output
2	V_Test1	Analog In	Pixel input for test column
3	V_Test2	Analog In	Pixel input for test column
4	VSS1	Analog In	Ground for NMOS body terminals (0 V)
5	Bias2	Analog In	Bias current for output MUX (35 μA)
17	Bias1	Analog In	Bias current for output MUX (1.5 μA)
18	Vint2	Analog In	Input for integrator in test structure
19	Vint1	Analog In	Input for integrator in test structure
20	Test_Gate_In2	Digital In	S_{test_2} gate voltage
21	VDD1	Analog In	VDD for PMOS body terminals (1.8 V)
22	Test_Gate_In2	Digital In	S_{test_2} gate voltage
23	CTIO2	Analog I/O	I/O for integrator and SCDA test structure
24	CTIO1	Analog I/O	I/O for integrator and SCDA test structure
25	ibias_1	Analog In	Bias current for OTAs (120.6 μA)
26	V_Out_Test	Analog Out	Output of SCDA in test structure
27	AVSS2	Analog In	Analog ground
28	AVSS1	Analog In	Analog ground
29	AVDD2	Analog In	Analog VDD (1.8 V)
30	AVDD1	Analog In	Analog VDD (1.8 V)
31	muxout8	Analog Out	Analog MUX output (column readout)
32	muxout7	Analog Out	Analog MUX output (column readout)
33	muxout6	Analog Out	Analog MUX output (column readout)
34	muxout5	Analog Out	Analog MUX output (column readout)
35	muxout4	Analog Out	Analog MUX output (column readout)
36	muxout3	Analog Out	Analog MUX output (column readout)
37	muxout2	Analog Out	Analog MUX output (column readout)
38	muxout1	Analog Out	Analog MUX output (column readout)
39	phi3	Digital In	SCDA ϕ_3 clock
40	phi2a	Digital In	SCDA ϕ_2 clock

Pin Number	Name	Direction	Notes
41	phi1a	Digital In	SCDA ϕ_1 clock
42	sample	Digital In	Integrator ϕ_{Sample} clock
43	DVSS1	Digital In	Digital ground (0 V)
44	DVDD1	Digital In	Digital VDD (1.8 V)
45	scanrowclk	Digital In	Row circuit scan chain clock
46	scanrowrstn	Digital In	Row circuit scan chain reset signal
47	scanrowout	Digital Out	Row circuit scan chain output
59	scanrowin	Digital In	Row circuit scan chain input
60	andgaterst	Digital In	Row circuit AND gate reset signal
61	andgateen	Digital In	Row circuit AND gate enable signal
62	DVDD2	Digital In	Digital VDD (1.8 V)
63	DVSS2	Digital In	Digital ground (0 V)
64	scancolin	Digital In	Output MUX input
65	scancolout	Digital Out	Output MUX output
66	scancolrstn	Digital In	Output MUX scan chain reset signal
67	scancolclk	Digital In	Output MUX scan chain signal
68	muxout9	Analog Out	Analog MUX output (column readout)
69	muxout10	Analog Out	Analog MUX output (column readout)
70	muxout11	Analog Out	Analog MUX output (column readout)
71	muxout12	Analog Out	Analog MUX output (column readout)
72	muxout13	Analog Out	Analog MUX output (column readout)
73	muxout14	Analog Out	Analog MUX output (column readout)
74	muxout15	Analog Out	Analog MUX output (column readout)
75	muxout16	Analog Out	Analog MUX output (column readout)
76	AVDD3	Analog In	Analog VDD (1.8 V)
77	AVDD4	Analog In	Analog VDD (1.8 V)
78	AVSS3	Analog In	Analog ground
79	AVSS4	Analog In	Analog ground
80	Vcm	Analog In	Common-mode voltage (0.4 V Nominal)
81	intrst	Digital In	Integrator ϕ_{RST} clock
82	VDD2	Analog In	VDD for PMOS body terminals (1.8 V)
83	VSS2	Analog In	Ground for NMOS body terminals (0 V)
84	ibias_2	Analog In	Bias current for OTAs (120.6 μA)