

Low-Power CMOS-like Flexible Circuits With Unipolar TFTs

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The increasing demand for [Thin Film Transistor \(TFT\)](#) electronics is driven by their cost-effectiveness and suitability for high-volume production, making them ideal for applications in flexible electronics, wearable devices, on-body sensors, and [Internet-of-things \(IoT\)](#) devices. TFT technologies, including organic, [transition metal oxide \(TMO\)](#), and [amorphous silicon \(a-Si:H\)](#) TFTs, have demonstrated significant potential for large-area, low-cost fabrication. Their integration into flexible electronics has enabled innovations such as bendable displays, electronic skin, and smart patches. However, unlike [Complementary Metal-Oxide-Semiconductor \(CMOS\)](#) technology, [TFTs](#) lack complementary transistors. Therefore, most complex circuits on flexible substrates remain reliant on rigid [CMOS integrated circuits \(IC\)](#)s, connected via soft ribbon cables. This dependency introduces challenges in signal interfacing, cost, and reliability, which constrain the scalability and complexity of flexible electronics. In display technology, [TFTs](#) are predominantly used for pixel circuits, while off-panel [CMOS ICs](#) handle control and driver circuits. Particularly, for high resolution displays, the need for numerous bonding pads to interface with off-panel [ICs](#) creates bottlenecks due to mechanical pitch constraints, and limited scalability, and exacerbates power dissipation caused by high-capacitance bonding pads. Addressing these challenges requires integrating control logic and driver circuits directly onto the [TFT](#) backplane to minimize reliance on off-panel [CMOS](#) circuits.

Unipolar [TFT](#) logic circuits face challenges such as limited output swing and significant direct path current, further complicating their use in low-power applications. To overcome these limitations, various fabrication techniques have been explored to create complementary transistors, but their higher production costs and complexities have limited practical adoption. While several circuit designs have been proposed to achieve full output swing using unipolar [TFTs](#), the persistent issue of substantial direct path current remains a critical obstacle. Moreover, most existing studies fail to consider the impact of bending on device power consumption and performance. This thesis presents a methodology for designing low-power, full-swing [TFT](#) digital circuits, including logic gates, decoders, [D Flip-Flops \(DFF\)](#), and [Static Random Access Memory \(SRAM\)](#) memory cells. The proposed circuits are fabricated on both glass and flexible [polyethylene naphthalate \(PEN\)](#) substrates, with an in-depth analysis of substrate bending effects on device performance. This study paves the way for enhancing existing [TFT](#) models by incorporating bending effects. The designs achieve significant advancements, including over 46.2% power reduction compared to state-of-the-art 3-to-8 address decoder design. These contributions lay the groundwork for low-power “system-on-flex” applications, providing a path toward scalable, efficient, and integrated flexible electronics.

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Dedication

To my dad.

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List of Abbreviations

a-Si:H amorphous silicon [iv](#), [8–12](#), [22](#), [35](#), [37](#), [43](#), [46](#), [51–53](#), [55](#), [63](#), [66](#), [69](#)

AI Artificial intelligence [22](#)

ALU Arithmetic Logic Unit [72](#), [73](#)

CMOS Complementary Metal-Oxide-Semiconductor [iv](#), [1](#), [4](#), [5](#), [11–13](#), [16](#), [18](#), [23](#), [24](#), [26](#), [38](#), [40](#), [41](#), [52](#), [54–57](#), [62](#), [70](#)

CNT carbon nanotube [10](#)

DFF D Flip-Flops [iv](#), [6](#), [7](#), [18](#), [19](#), [54–57](#), [61–63](#), [65–67](#), [70–72](#)

DOS density-of-states [10](#)

FOM Figure of merit [40](#)

IC integrated circuits [iv](#), [1–4](#), [8](#), [9](#), [23](#), [53](#), [54](#)

IGZO indium–gallium–zinc-oxide [8](#), [20–22](#), [57](#)

IoT Internet-of-things [iv](#), [1](#), [8](#), [22](#), [54](#)

LCD liquid crystal display [1](#), [2](#)

LTPS low-temperature polycrystalline silicon [8](#), [9](#), [11](#), [13](#), [16](#), [24](#)

ML Machine Learning [22](#)

NFC near-field communication [x](#), [2](#), [3](#), [16](#)

OLED organic light-emitting diode 1

OTFT organic thin-film transistors 8, 9, 20–22, 57

PDP power-delay-product 40, 62, 70

PECVD Plasma-enhanced chemical vapor deposition 12, 37, 47

PEN polyethylene naphthalate iv, 35, 36, 43, 45–47, 53

RAM Random Access Memory 16

RFID Radio-Frequency IDentification 16

RIE reactive ion etching 12

RISC-V Reduced Instruction Set Computer V 22

RSNM read static noise margins 63

SRAM Static Random Access Memory iv, 6, 7, 19, 20, 54–60, 63–65, 67, 69–71, 73

SWNT single-walled carbon nanotubes 10

TFT Thin Film Transistor iv, x, 1–17, 19–32, 34–38, 40, 43–47, 52–59, 61–63, 66, 67, 69–73

TMO transition metal oxide iv

V_t threshold voltage 46

WSNM write static noise margins 63

Chapter 1

Introduction

1.1 Why are Thin Film Transistors important?

One of the most intriguing aspects of **TFT** technology is its compatibility with cost-efficient, high-volume production techniques. These manufacturing methods facilitate the fabrication of large-area electronics at a fraction of the cost associated with traditional silicon **IC** fabrication. In consumer electronics and **IoT** devices, where affordability is crucial, **TFTs** offer a viable alternative to **CMOS** technology, which becomes economically impractical for large-area applications. Unlike **CMOS**, **TFTs** can maintain uniform performance across extensive surfaces, making them ideal for scalable production [1, 2, 3].

Additionally, **TFTs** are not limited by the rigid, high-cost infrastructure associated with silicon fabrication. Their versatility supports the development of innovative devices that combine functionality with novel form factors, ranging from flexible health monitors to foldable displays [4, 5, 6, 7]. As the demand for adaptable and affordable electronics continues to grow, **TFT** based circuits provide a sustainable and practical pathway for addressing the technological and economic challenges of next-generation applications [8, 9, 10, 11].

1.2 Thin Film Transistors Applications

TFTs play a critical role in flat-panel displays, including **liquid crystal display (LCD)**s, **organic light-emitting diode (OLED)** displays, and emerging flexible and foldable display

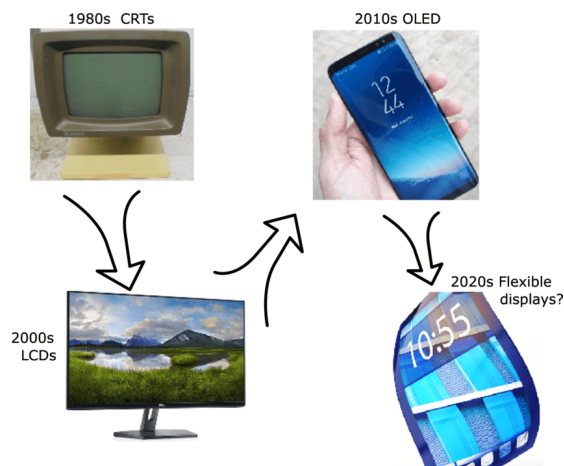


Figure 1.1: Evolution of the display technologies [13].

technologies [12, 13]. The commercialization of TFTs for LCD applications began approximately 30 years ago, marking a significant milestone in display technology. Today, TFTs have become the dominant technology for pixel switches in flat-panel displays, driving advancements in consumer electronics [14, 15]. The demand for higher display resolution, greater brightness, reduced power consumption, and innovative features such as narrow-bezel, curved, foldable, and rollable displays continue to shape the evolution of TFT technology [16].

Figure 1.2 highlights the remarkable benefits of thin-film circuits fabricated on flexible substrates [3]. These circuits can be fabricated over large areas, enabling the creation of ultra-thin, lightweight, and highly flexible electronic devices. Unlike rigid counterparts, flexible thin-film circuits maintain their functionality even when folded, rolled, or crumpled, making them ideal for applications that demand resilience and adaptability. For instance, a flexible TFT based microprocessor (as shown in Figure 1.2(c)) or a thin-film NFC tag (as shown in Figure 1.2(d)) can be seamlessly embedded into objects without affecting their form or functionality [3, 17, 18].

One of the most exciting aspects of TFT technology is its compatibility with ultrathin, stretchable substrates. These substrates can be engineered to be porous, enabling the fabrication of breathable electronic devices that are comfortable for direct skin contact [19]. This feature is particularly advantageous for developing wearable electronics, where comfort, flexibility, and lightweight are critical. For example, thin-film ICs can be designed as electronic tattoos that conform to the skin, offering imperceptible yet robust functionality [20, 21].

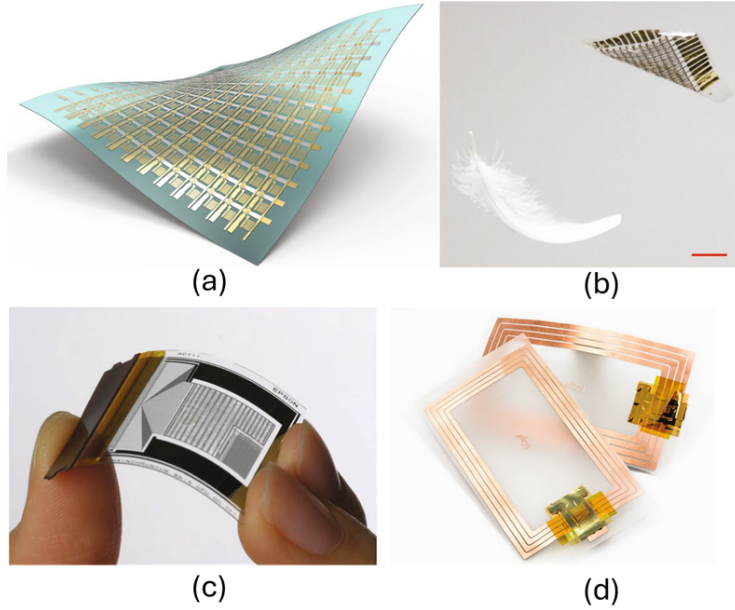


Figure 1.2: Examples of flexible electronics and their applications. (a) active-matrix sensor, (b) Ultrathin plastic electronic foils which, (c) flexible TFT based microprocessor, and (d) NFC tag [3].

These ultrathin, conformable ICs have the potential to revolutionize wearable electronics, enabling innovative and seamless integration into everyday devices [3]. By adhering to the skin like a temporary tattoo, such devices can monitor vital body parameters, including heart rate, temperature, hydration levels, and other health indicators. Data collected by these devices can be transmitted wirelessly to a patient’s smartphone or a medical database, enabling real-time health monitoring and remote diagnostics. This capability could revolutionize personalized healthcare by providing continuous, non-invasive monitoring solutions for patients with chronic conditions or those in critical care.

Additionally, these flexible and stretchable ICs open new possibilities in consumer and industrial applications. Thin-film NFC tags could facilitate seamless connectivity in smart packaging, inventory tracking, and secure transactions [22, 23, 24]. Flexible TFT based microprocessors could power lightweight, portable electronic systems, enhancing the functionality of devices like smart cards, wearable fitness trackers, and next-generation IoT devices [18, 25].

Furthermore, the mechanical durability of thin-film circuits ensures reliable performance even under stress. Whether subjected to folding, bending, or stretching, these

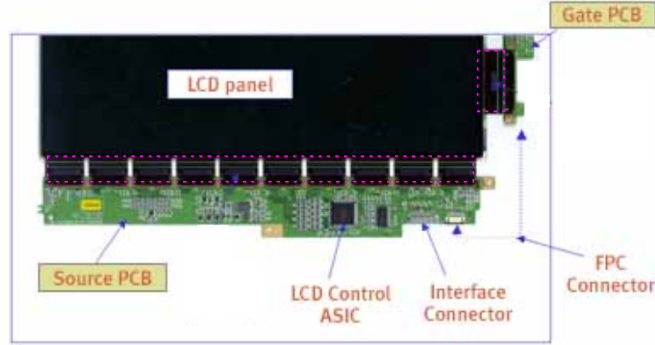


Figure 1.3: The PCB components and the panel of an LCD display [13].

circuits maintain their operational integrity, making them suitable for use in dynamic environments. This characteristic is especially valuable in wearable devices, which must endure continuous movement and environmental exposure.

1.3 Need for low-power Thin-Film Transistor Circuits

The display pixels are primarily controlled by TFT based circuits, while most control and driver circuits are implemented using off-panel CMOS ICs, as shown in Figure 1.3. These CMOS ICs are connected to the TFT display panel via soft ribbon cables (highlighted within dashed pink lines in Figure 1.3) [13]. However, as the demand for higher-resolution displays continues to grow, the number of bonding pads required to interface with external ICs also increases significantly. For example, a 4K display requires 3,840 bonding pads for the columns and 2,160 for the rows, resulting in over 6000 connections.

This poses a significant challenge for achieving higher display resolutions due to the mechanical limitations associated with bonding pad density. Furthermore, the large number of bonding pads introduces high capacitance, which results in increased power dissipation. These factors collectively create bottlenecks in the scalability and energy efficiency of high-resolution displays [13, 26]. Addressing these challenges requires innovative solutions, such as integrating control and driver circuits directly onto the TFT backplane, thereby reducing the reliance on external ICs and minimizing the associated constraints [26, 27].

The growing interest in flexible and wearable electronics has created a demand for circuits that are not only mechanically flexible but also energy efficient. Flexible substrates, such as plastics or thin metal films, often have low thermal tolerance, making high-power

logic circuits impractical. Low-power TFT logic circuits are essential for such applications, enabling the creation of lightweight, durable, and conformable devices like electronic skin, smart patches, and foldable displays [20, 26].

1.4 Motivation

Unlike CMOS technology, which inherently supports complementary transistors for circuit design, TFTs are typically limited to unipolar devices. This constraint arises because fabricating high-performance complementary TFTs is more challenging due to material limitations, higher temperature processes, and higher fabrication costs. Consequently, conventional TFT circuits, which rely solely on unipolar transistors, exhibit several drawbacks, including limited output swing and high power consumption [26].

Limited output swing, which refers to the inability of the circuit to achieve the full voltage range between the supply voltage V_{DD} and ground (V_{SS}), is primarily due to the unipolar nature of the TFT. This limitation is particularly problematic in digital circuits, where reliable signal propagation across multiple stages is essential for overall functionality. Additionally, the reliance on n-type-only devices often leads to significant direct-path currents, further exacerbating the issue of high power consumption.

To address these challenges, researchers have explored the development of complementary TFTs to enable CMOS-like logic [28]. However, significant obstacles remain. A key limitation is the inherently low mobility and short lifetime of holes compared to electrons, which compromises the performance and reliability of p-type TFTs [29]. Additionally, fabricating high-quality p-type TFTs often requires complex and costly processes that are less compatible with the low-cost, low-temperature, and flexible substrate processing advantages of TFT technology [28, 30]. Consequently, complementary TFTs have yet to demonstrate clear benefits or achieve widespread adoption.

Various researchers have attempted to address the challenges associated with unipolar TFT circuits. In [31], an enhanced 2T inverter design was introduced, incorporating a dual-gate architecture. In this approach, the back gate functions similarly to body biasing in silicon CMOS, enabling independent control of each TFT's threshold voltage. However, while this method improves certain aspects of circuit performance, it fails to fully resolve the issue of achieving a complete output swing.

To address this limitation, the researchers in [32] proposed a pseudo-CMOS logic circuit that utilizes an additional voltage source to ensure full output swing. Although this approach successfully achieves the desired voltage levels at the output, it does not mitigate

the issue of direct path current. Consequently, this method still suffers from high power consumption, limiting its applicability in low-power designs.

Moreover, current solutions fail to account for the behavior of flexible TFT circuits under varying bending conditions. Existing simulation models do not incorporate the mechanical strain effects caused by bending, which can significantly impact electrical performance, including threshold voltage shifts, mobility degradation, and variations in circuit reliability [33, 34, 35, 36]. Without accurately modeling these bending-induced changes, the design and optimization of flexible TFT circuits remain incomplete, limiting their practical implementation in real-world applications.

Given these limitations, there is a critical need to design efficient unipolar low-power TFT circuits that overcome inherent shortcomings. Additionally, a thorough investigation of mechanical bending effects on circuit performance is essential for improving the accuracy of existing simulation models. This study aims to develop unipolar low-power TFT circuits that mitigate their inherent drawbacks and provide insight into the effects of substrate bending. These advancements are crucial for addressing the evolving requirements of next-generation technologies, including high-resolution displays, flexible electronics, wearable devices, and IoT systems. A deeper understanding of bending effects will not only refine simulation models but also pave the way for more resilient and scalable flexible electronic systems.

1.5 Thesis organization

The necessity for low-power unipolar TFT based circuits has been thoroughly discussed. In this thesis, we present a novel approach to address these challenges by introducing half-latch-based logic circuits. These circuits achieve full output swing and significantly reduce direct path current, offering a clear advantage over state-of-the-art designs. Additionally, we propose DFF and SRAM memory cells using unipolar TFTs, which exhibit substantially lower static power consumption compared to traditional designs. Furthermore, we present a comprehensive study on the impact of mechanical bending, offering deeper insights into its effects on circuit performance. These advancements aim to enable and unlock the full potential of TFT technology, paving the way for its widespread adoption in modern electronics.

This thesis is organized as follows: Chapter 2 presents a comprehensive overview of various TFT technologies, along with an in-depth analysis of state-of-the-art solutions developed to address the challenges associated with TFT circuits. Chapter 3 introduces

the proposed half-latch-based TFT circuits and demonstrates the implementation of a 3-to-8 decoder using the proposed and the state-of-the-art logic gate on both glass and flexible substrates. The impact of bending on the proposed designs is also thoroughly investigated. In Chapter 4, we introduce a DFF using the unipolar half-latch logic gate. The proposed design and conventional DFF design were fabricated on glass and flexible substrates. Compared to conventional DFF, the proposed DFF design reduces the total power consumption by 79.8%. Furthermore, in Chapter 5, we use half-latch based design to implement an SRAM cell. The analysis reveals that the static power consumption of the proposed SRAM cell is reduced by a remarkable 56x compared to the conventional SRAM design. Finally, Chapter 5 concludes the work, summarizing key findings and outlining potential directions for future research.

Chapter 2

Background

2.1 Introduction

TFT based circuits have the potential to play a key role in modern electronics, providing flexible, affordable, and scalable solutions for industries like consumer electronics, health-care, and **IoT**. These circuits address limitations inherent in traditional silicon-based **ICs**, particularly in applications where flexibility, large-area integration, and affordability are paramount.

This chapter will provide the necessary information to help understand the thesis. It begins by discussing various **TFT** technologies, focusing on their fabrication processes and the fundamental operation of **a-Si:H TFTs**. Additionally, the chapter delves into state-of-the-art designs, examining both single-stage and multistage logic circuits implemented using unipolar **TFTs**. This comprehensive overview provides the context needed to understand the advancements presented in the thesis.

2.2 Overview of TFT Technologies

At present, the predominant **TFT** technologies employed in consumer electronics include **a-Si:H**, **low-temperature polycrystalline silicon (LTPS)**, amorphous metal-oxide semiconductors (primarily **indium–gallium–zinc-oxide (IGZO)**), and **organic thin-film transistors (OTFT)**s.

Table 2.1: Comparison of different properties of the TFT technologies [3].

Parameters	a-Si:H	LTPS	Oxide	Organic
μ (cm ² /V·s)	0.5–1	50–100	10–40	0.1–10
Process complexity	Low	High	Low	Low
Manufacturing cost	Low	High	Low	Low
Light stability	Poor	Good	Fair	Poor
Intrinsic properties on mechanical stress	Poor	Poor	Good	Fair-to-good
Transistor	n-type	p-type, n-type	n-type	p-type (n-type possible)
TFT-to-TFT uniformity	Good	Low	Good	Low
Large-area uniformity	Good	Low	Good	Low

a-Si:H TFTs stand out as a promising n-type-only technology for flexible ICs. They can be fabricated at relatively low process temperatures, staying within the thermal budget required for flexible substrates without causing deformation [37, 13]. In contrast, LTPS transistors necessitate higher processing temperatures and involve a more intricate fabrication process. However, this complexity enables LTPS technology to produce complementary p-type and n-type TFTs with significantly higher mobility (50–100 cm²/V·s), compared to a-Si:H TFTs (mobility 0.5–1 cm²/V·s) [38]. Despite these advantages, the crystallization process in LTPS introduces grain boundaries in the silicon layer, leading to variability in electrical performance across large areas.

Metal-oxide TFT is another promising n-type-only technology for flexible ICs, as it can be manufactured at process temperatures compatible with flexible substrates while offering a charge carrier mobility of around 10 cm²/V·s or higher, compared to 0.5–1 cm²/V·s for a-Si:H [3]. However, it is more susceptible to environmental degradation than a-Si:H TFTs, particularly from moisture and oxygen, which can lead to performance variations.

OTFTs, which are primarily p-type, have gained significant attention as an emerging option for flexible ICs, with the potential to complement n-type metal-oxide TFTs [39, 40]. However, one major challenge with OTFTs is their sensitivity to environmental factors such as oxygen, moisture, and UV light, which can degrade performance over time. Despite these limitations, OTFTs are extensively studied due to their compatibility with solution-based fabrication methods and mechanical flexibility. Considerable research has also focused on developing n-type OTFTs. However, organic materials generally exhibit lower electron mobility than hole mobility due to intrinsic trap states and energetic disorder [41]. These traps capture electrons, hindering efficient conduction. As a result, while n-type OTFTs are

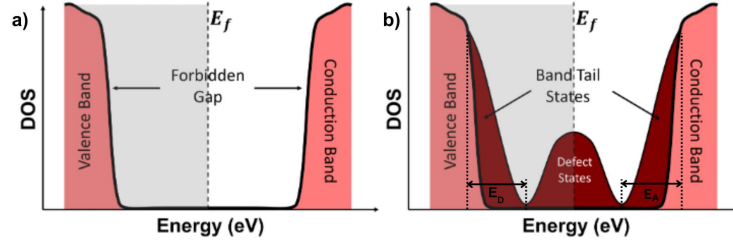


Figure 2.1: DOS diagram for a) crystalline silicon and b) intrinsic a-Si:H [47].

theoretically possible, practical challenges have limited their performance and widespread adoption compared to their p-type counterparts [42].

A comparative analysis of these TFT technologies, including their material properties, mobility, process temperatures, and suitability for flexible substrates, is presented in Table 2.1 [3].

Another promising area of research is the development of carbon nanotube (CNT) TFTs [43, 44]. These transistors are fabricated on flexible substrates using purified, surfactant based CNT suspensions with a high proportion of semiconducting CNTs. Typically, they feature a network of single-walled carbon nanotubes (SWNT)s that serve as the active layer of the transistor. A distinct advantage of CNT TFTs is their ability to operate efficiently at low voltages, setting them apart from other TFT materials. However, achieving high-performance CNT TFTs depends on the availability of highly purified semiconducting CNTs ($\geq 99\%$), which presents significant challenges and involves substantial production costs [45].

This thesis employs a-Si:H TFT technology for fabrication, owing to the mature fabrication process, its compatibility with low-temperature processing, and its ability to be seamlessly fabricated on flexible substrates without causing deformation. Nevertheless, the proposed designs in this thesis can also be implemented using other unipolar TFT technologies, with similar improvements anticipated in design matrices.

2.3 A-Si:H Device Physics and Operation

As shown in Figure 2.1, in crystalline silicon, a well-defined bandgap is evident, characterized by abrupt discontinuities in the valence and conduction bands. In contrast, amorphous silicon exhibits a continuous density-of-states (DOS) across the energy spectrum due to its lack of long-range atomic order. This amorphous nature gives rise to defect states

within the middle of the forbidden energy gap, which are primarily attributed to dangling and strained Si-Si bonds introduced during fabrication processes [46, 47]. These defect states result in localized energy levels, causing a tail broadening that extends into both the valence and conduction bands. The parameters ED and EA denote the valence and conduction tail-band widths, respectively [48].

While the amorphous structure of a-Si:H offers advantages such as uniformity over large areas, particularly when compared to LTPS, it also introduces significant challenges. The presence of dangling bonds lowers carrier mobility and makes the material’s threshold voltage (VT) highly sensitive to induced stress [6, 13, 46, 49].

Furthermore, the intrinsic n-type nature of a-Si:H limits its ability to support complementary transistor types, complicating the implementation of CMOS-like logic circuits [13, 46]. In a-Si:H, dangling bonds and disorder-induced defects introduce deep trap states within the bandgap. While n-type conduction is viable due to shallow donor levels that facilitate electron transport, hole transport is significantly impeded. The deep acceptor levels make it difficult to generate mobile holes, and even when holes are present, they are quickly trapped by defect states near the valence band. As a result, hole mobility is extremely low ($\sim 10^{-6}$ cm²/V·s), in stark contrast to electron mobility ($\sim 0.5\text{--}1$ cm²/V·s), further limiting the practicality of p-type a-Si:H transistors [29].

Despite these limitations, a-Si:H remains an attractive material for TFT applications due to its compatibility with low-temperature fabrication processes and its ability to maintain uniform performance across large substrates.

2.4 Fabrication of a-Si:H TFTs

Fabrication techniques can be employed to reduce the defect density at the semiconductor/dielectric interface of a-Si:H TFTs. Figure 2.2 shows various device architectures employed.

The names “top-gate” and “bottom-gate” refer to the location of the gate electrode in relation to the dielectric. Top-gate TFTs are formed by having the gate electrode on top of the dielectric, whereas bottom-gate TFTs have the gate electrode sandwiched between the dielectric and the substrate. Likewise, the terms “coplanar” and “staggered” refer to the location of the source and drain electrodes and the dielectric, relative to the channel. For coplanar structures, the source and drain electrodes and the dielectric are located on the same side of the channel, whereas for staggered, the dielectric and semiconducting layer is sandwiched in between the source and drain electrodes [13, 46, 50].

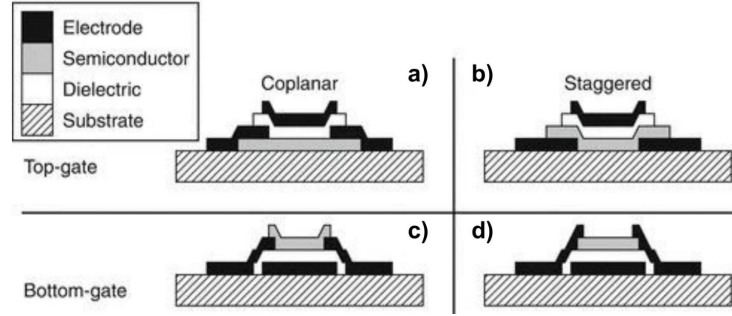


Figure 2.2: TFT device architectures for (a) top-gate coplanar, (b) top-gate staggered, (c) bottom-gate coplanar and (d) bottom-gate staggered a-Si:H TFTs [52].

In terms of performance, the bottom-gate staggered architecture is the best for a-Si:H TFTs. In coplanar structures, the semiconductor and dielectric would have to be deposited separately. Doing so increases the defect density at the semiconductor/dielectric interface. For staggered structures, however, the semiconductor and dielectric can be deposited subsequently, without having to open the vacuum chamber, reducing the defect density. This helps improve the carrier mobility. Additionally, the staggered structure gives a lower contact resistance than the coplanar structure, which contributes to a higher carrier mobility [13, 51, 52].

Typically, the fabrication for bottom-gate staggered a-Si:H TFTs uses a 4-5 mask process. After the gate metal is deposited and patterned, the dielectric (a-SiN_x:H), intrinsic a-Si:H, and the n⁺ a-Si:H doped layer is deposited in a Plasma-enhanced chemical vapor deposition (PECVD) process in the same vacuum [13, 46, 52]. This can be done in a quick, sequential process, thanks to its staggered structure. The PECVD process is normally done at temperatures of around 300°C, which is significantly lower than CMOS technology. Following that, the source and drain electrodes are deposited. These electrodes are patterned and etched, commonly using reactive ion etching (RIE) to do so. This RIE etch continues until the n⁺ a-Si:H layer is etched enough to the point where the intrinsic a-Si:H channel is exposed. There is a slight degree of over-etching into the intrinsic a-Si:H as there is no etching selectivity between the n⁺ a-Si:H and intrinsic a-Si:H. Post-etch annealing is commonly employed to minimize the defect density on the back surface.

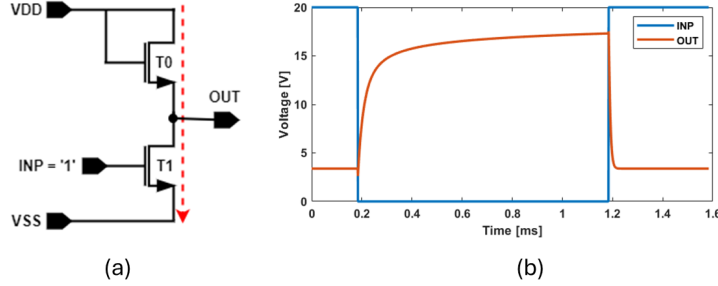


Figure 2.3: (a) Conventional unipolar TFT based inverter design, and (b) its waveform. The red dotted line shows a direct path current from V_{DD} to V_{SS} .

2.5 State-of-the-art approaches to TFT based Logic Gate Design

Logic gates serve as the fundamental building blocks of complex digital circuits and require careful optimization tailored to the specific process technology. CMOS technology is widely regarded as the most efficient configuration, benefiting from the complementary operation of p-type and n-type transistors. While complementary logic can be implemented in LTPS, achieving the same in a-si:H, organic and metal-oxide TFTs is challenging due to the lack of suitable complementary counterparts [3]. However, implementing LTPS TFTs on flexible substrates presents a challenge due to the relatively high processing temperatures required. Therefore, unipolar logic gates are the primary choice for implementing flexible integrated circuits in TFT technologies that lack complementary counterparts. The main disadvantages of unipolar logic gates over complementary logic gates are reduced output swing and increased power consumption due to direct path current.

Figure 2.3(a) shows a conventional 2T inverter, composed of a diode connected load T_0 and a drive transistor T_1 . When the input signal is ‘logic 0’, T_0 charges the load capacitor to a higher voltage. However, it can only reach a maximum output voltage (V_H) of ‘ $V_{DD} - V_{T0}$ ’, where V_{T0} represents the threshold voltage of the TFT. Conversely, when the input signal is ‘logic 1’, both TFTs are active, causing a voltage division at the output. As a result, the minimum output voltage (V_L) does not drop to zero, thereby limiting the output swing ΔV_{out} ($V_H - V_L$), as shown in Figure 2.3(b). Additionally, when the input is ‘logic 1’, both TFTs are on simultaneously, creating a direct current path between V_{DD} and V_{SS} , which leads to high static power consumption.

Researchers in [31] used the dual gate architecture of the device to improve the conventional 2T inverter. In this design, the back gate functions similarly to Si CMOS’s body

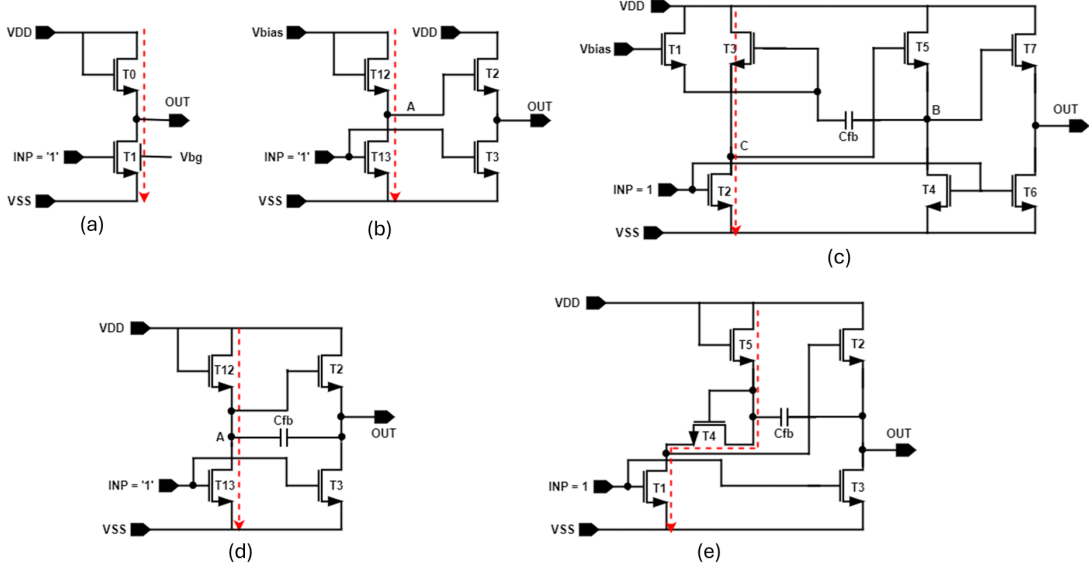


Figure 2.4: Inverter designs using (a) Backgate [31], (b) Pseudo-CMOS logic with additional V_{bias} [32], (c) 7T [53], (d) 4T [55], and (e) 5T [26]. The red dotted line shows a direct path current from V_{DD} to V_{SS}.

bias and is used to individually control the threshold voltage of each TFT. The inverter scheme is shown in Figure 2.4(a). The benefit of this design is it does not require any additional area penalty. Although leakage is controlled to a certain extent by body biasing TFTs, the limited output swing still remains an issue in this design. Furthermore, the feasibility of introducing distinct threshold voltages often hinges on the specific technology in use; examples include channel doping, semiconductor thickness, and gate-dielectric thickness. Therefore, introducing a back-gate for body biasing may affect the yield, depending upon technology. Moreover, the leakage current, although controlled, is not completely eliminated.

To achieve full output swing, researchers in [32] demonstrated a pseudo-CMOS logic circuit on a glass substrate, as illustrated in Figure 2.4(b). This circuit operates in two stages. In the first stage, the devices use an additional power supply voltage (V_{bias}). When the input (INP) is ‘logic 0’, the pull-down TFTs (T13 and T3) are turned OFF, allowing the output of the first stage (A) to reach “V_{bias}−V_T”. Typically, V_{bias} is set higher than V_{DD} (e.g., V_{bias} ≥ V_{DD} + V_T) to ensure that the output (OUT) reaches V_{DD}. When INP switches to ‘logic 1’, both T13 and T3 turn on simultaneously, and the output of the first stage is determined by the ON-resistance ratio of T12 and T13. This ratio is usually

designed to be lower than the V_T of T2, resulting in the deactivation of T2 and allowing OUT to drop to V_{SS} . This design achieves full output swing; however, it does not resolve the problem of high static power consumption.

Hwang *et al.* have proposed a 7-TFT inverter to tackle the challenges [53]. The schematic of the inverter is shown in Figure 2.4(c). In this design, when input is ‘logic 1’, T2, T4, and T6 are turned on, discharging node B and therefore turning off T7. Thus, the output fully discharges to V_{SS} . On the other hand, when the input is ‘logic 0’, T2, T4 and T6 are turned off. Subsequently, the gate of T5 is raised due to the drain current supplied by T3. Then, the gate voltage of both T3 and T5 rises to V_{DD} from the feedback loop. In this design, an external voltage V_{bias} is used to aid in storing charge on C_{fb} which maintains the overdrive voltage of T3. The V_{bias} signal is essential in the operation of the inverter because it aids the output signal to reach full swing. In this design, when input is high, both T2 and T3 are ‘on’, resulting in direct path current and high static power consumption.

Chen *et al.* attempted to tackle the issue of output swing by introducing a 4-TFT (4T) inverter design on a glass substrate using back-gate TFTs [54]. This design was further optimized by Tiwari *et al.* by using a single gate TFT structure, as shown in Figure 2.4(d) [55]. In this 4T inverter design, when the input is high, both T13 and T3 are fully activated, leading to the discharge of node A and the output. Since T12 operates as a diode-connected load, it remains in saturation mode, allowing for minimal leakage current while ensuring T13 has a large channel width ratio, resulting in very low on-resistance. This configuration maintains the voltage at node A at a sufficiently low level to keep T2 from turning on, effectively lowering the output voltage to V_{SS} . During this phase, the voltage at node A is $\sim 1/2 V_{DD}$. When the input signal transitions to low, node A and output node start to rise. Due to the feedback capacitor, node A is boosted and T2 is overdriven, achieving a full V_{DD} at the output. It should be noted that when input is high, both T12 and T13 are ‘on’, resulting in direct path current and high static power consumption.

Papadopoulos *et al.* introduced a bootstrapped 7-TFT (7T) inverter on a glass substrate to achieve full output voltage swing [56]. Li *et al.* demonstrated a similar bootstrapped 5-TFT (5T) inverter on a flexible substrate, shown in Figure 2.4(e), to achieve full output swing with a comparatively smaller area overhead than the 7T inverter [26]. To reduce the direct path current when the input is high, Li *et al.* introduced an additional diode-configured TFT T4. Although these circuits resolve the issue of full output swing in unipolar TFT logic gates, the problem of high direct path current remains a concern.

2.6 Multistage logic circuits using unipolar TFTs

Several multistage logic circuits have been proposed by researchers that demonstrate the application of unipolar TFTs on flexible and glass substrates.

Radio-Frequency IDentification (RFID) tags have received substantial attention in the realm of thin-film electronics due to their potential to serve as cost-effective IoT nodes or be employed for tagging everyday objects. In a study by researchers [57], pseudo-CMOS logic gates were utilized to create a flexible metal-oxide NFC chip compliant with ISO14443-A standards. It was observed that the pseudo-CMOS gate delays were adequate for dividing the 13.56 MHz carrier frequency, although the corresponding power figures suggest limiting the use of these gates when designing the full chip. The architecture of this chip is segmented into seven stages. Power consumption has been progressively reduced across these stages by opting for slower and lower-power pseudo-CMOS gates and by increasing gate length. A balanced distribution between V_{DD} and V_{bias} has been maintained. This symmetry ensures the accurate generation of V_{DD} and V_{bias} by the rectifier circuit, as both power nodes bear a similar load.

Another intriguing and intricate digital circuit is a microprocessor. The first flexible thin-film microprocessor was introduced in 2005 [18]. It consists of approximately 32,000 transistors, utilizing flexible complementary LTPS transistors, which are released from the carrier by employing the ‘surface-free technology by laser ablation/annealing’ process flow. The first unipolar organic microprocessor fabricated directly on flexible substrates exhibited a clock frequency of 40 Hz to execute 8-bit operations [58]. This design, implemented using a back-gated TFT, demonstrated ultra-low power consumption, requiring just 100 μW at a supply voltage of 10 V and a back-gate voltage of 50 V. Researchers in [59] published results about a flexible 8-bit microprocessor and reported the fastest operating frequency of 71.4 KHz till now. The design consumed 134.9 mW of power, operating at a 3 V supply voltage with an additional 6 V V_{bias} voltage. Psuedo-CMOS logic gates, described in the previous section, were used in [58, 59] to design these microprocessors.

Recently, a 32-bit Arm microprocessor, named PlasticARM, was developed using metal-oxide TFT technology on a flexible substrate [60]. This microprocessor incorporates a 32-bit Arm Cortex-M CPU and a Nested Vector Interrupt Controller (NVIC). It is linked to its memory via the interconnect fabric (AHB-LITE). An external bus interface is provided for General-Purpose Input-Output (GPIO) to enable off-chip communication with the test framework. The CPU’s microarchitecture employs a two-stage pipeline, and to conserve space, latch-based Random Access Memory (RAM) is used as registers in PlasticARM. The logic gates used n-type unipolar TFTs with resistive load (similar to the logic gate

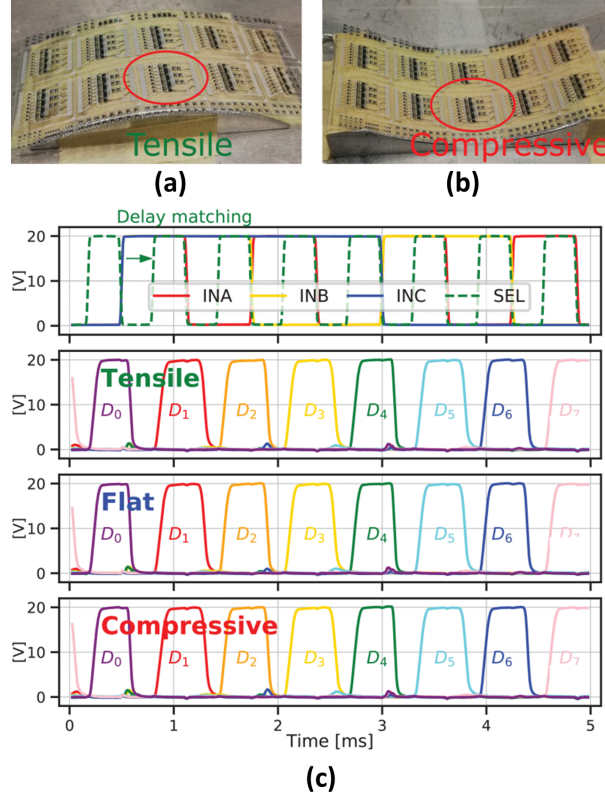


Figure 2.5: Flexible circuit samples taped onto two aluminum sample holders to mimic (a) tensile and (b) compressive strain conditions, (c) the input and output of all eight bits of the decoder under tensile, flat, and compressive strain conditions [26].

shown in Figure 2.3(a), but instead of diode T0, a resistor was used). The overall chip was composed of 39,157 TFT devices and 17,183 resistors, achieving a maximum operating frequency of 29 kHz while consuming 21 *mW* of power.

Another major application of TFTs is in flexible display panels. TFTs are already being used as pixel circuits, but their application can also be expanded to periphery control and driver circuits in displays. Researchers in [26] demonstrated a 3-to-8 decoder, shown in Figure 2.5, to drive pixels using bootstrapped 5T inverter logic gates (shown in Figure 2.4(e)) on a flexible substrate.

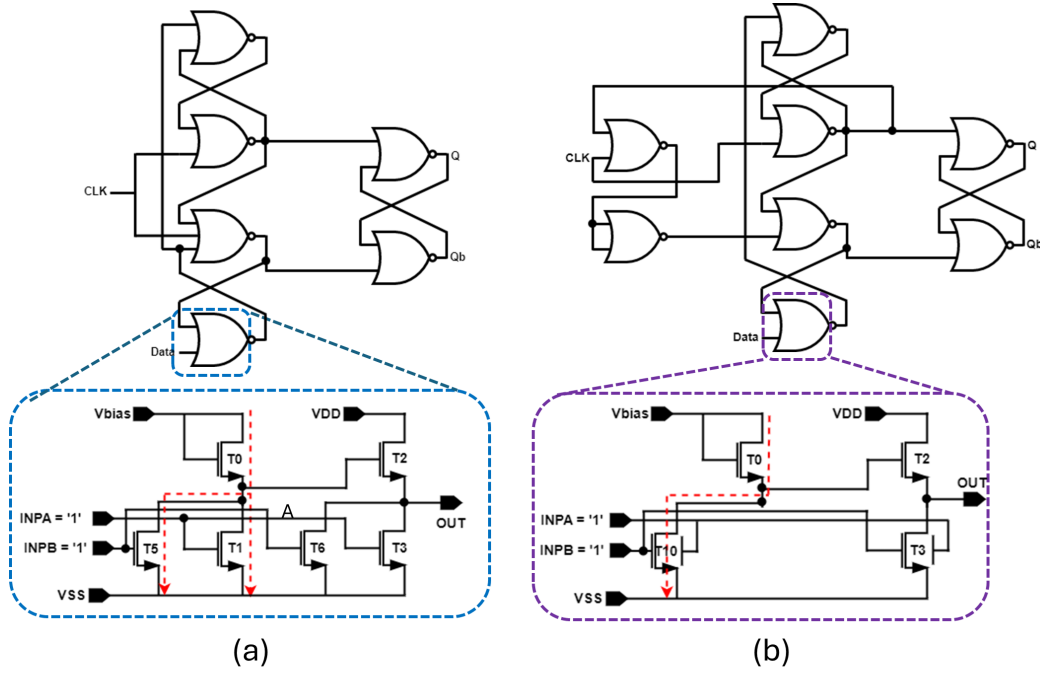


Figure 2.6: DFF designs using (a) Pseudo-CMOS NOR logic gate [61], and (b) Pseudo-CMOS NOR logic with top and bottom gate [62]. The red dotted line shows a direct path current from V_{DD} to V_{SS} .

2.7 State-of-the-art DFFs and SRAMs

Y. Xu *et al.* demonstrated a **DFF** using NOR gates based on pseudo-CMOS logic [61]. The schematic of the **DFF** is shown in Figure 2.6(a). The working of pseudo-CMOS NOR gates is similar to pseudo-CMOS inverter logic (shown in Figure 2.4(b)) discussed earlier. The drawback of this design is that it requires additional bias voltage and excessive direct path current.

The researchers in [62] demonstrated a **DFF** using pseudo-CMOS logic gates and used top and bottom gate structures to incorporate two terminals with a reduced area, shown in Figure 2.6(b). While this method achieves full output swing and reduces the area footprint in the **DFF**, the power consumption due to direct path current is not addressed. Furthermore, adding a bottom gate for a second terminal may affect the complexity and yield of the fabrication process.

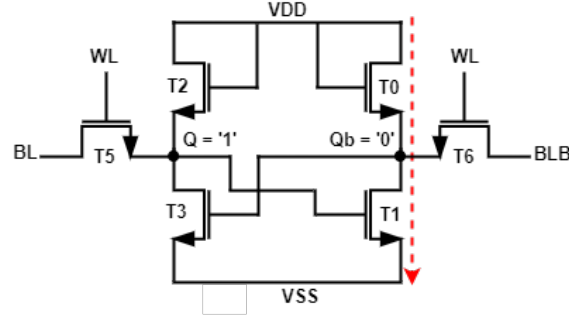


Figure 2.8: Unipolar TFT based conventional SRAM. The red dotted line shows a direct path current from V_{DD} to V_{SS} .

2.8. On the other hand, when the data at node Q and Qb are '0' and '1', respectively, there is a direct path current formed between V_{DD} and V_{SS} through transistors T2 and T3.

The researchers in [65] demonstrated a 6T SRAM cell based on IGZO TFTs, shown in Figure 2.9(a), fabricated on a flexible substrate. They further demonstrated that the circuit remains stable under a tensile mechanical strain of 0.52%, induced by bending to a 5 mm radius. In this design, the cSET and cRESET signals are maintained high in default state, activating TFTs T10 and T11. If the data stored at node Qb is '0', a direct path current flows through T0, T9, and T11. In contrast, if the data stored at node Q is '0', the direct path current flows through T7, T8, and T10. Roose *et. al.* demonstrated 128b SRAM memory using IGZO TFTs with back-gate in pull-down and passgate TFTs, as shown in Figure 2.9(b) [66]. The use of back-gate improves noise margin as well as reduces direct path current.

The researchers in [67] demonstrated a 6T SRAM cell utilizing single-gated p-type OTFTs, as shown in Figure 2.9(c). The study in [68] introduced a 5T SRAM cell, depicted in Figure 2.9(d), using back-gated organic TFTs. This design operates similarly to a standard 6T SRAM but features a single-ended bitline instead of a differential one, reducing the SRAM cell area by 20% and halving the number of required bitlines. They also introduced an extra voltage supply, V_b , to control direct path current and improve noise margins. Although these designs reduce direct path currents in unipolar TFT based SRAM cells by incorporating back-gated TFTs or additional voltage sources, the issue remains persistent. Furthermore, generating an additional voltage source increases overall power consumption. Therefore, developing an SRAM architecture that effectively addresses these challenges is crucial to fully unlocking the potential of TFT technology.

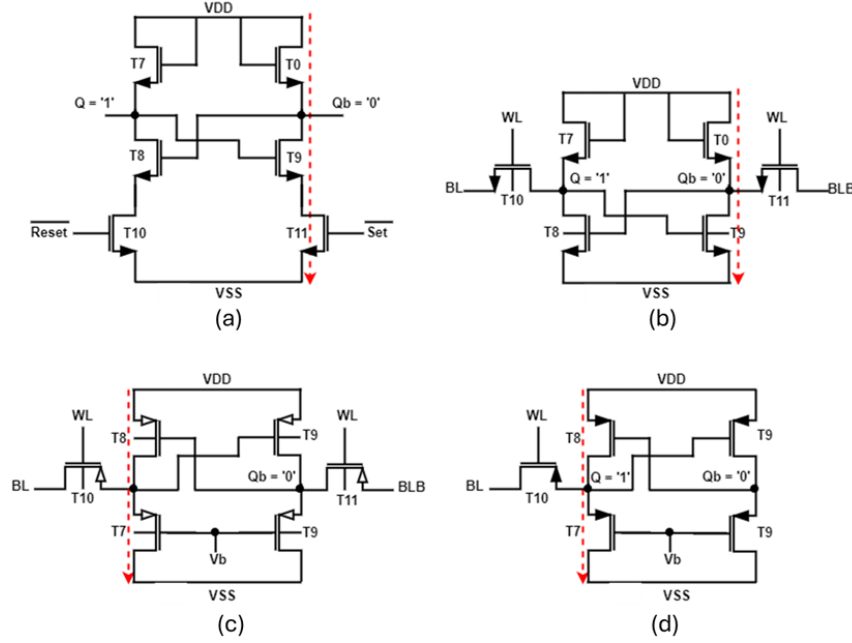


Figure 2.9: SRAM using (a) IGZO TFT [65], (b) back-gated IGZO TFT [66] (c) organic TFT [67], and (d) back-gated organic TFT with additional Vbias voltage [68]. Dotted line shows direct path current between V_{DD} and V_{SS} when data stored at node Q and Qb are ‘1’ and ‘0’, respectively.

2.8 Previous studies on effect of bending

Münzenrieder *et al.* investigate the effects of mechanical bending and illumination on the performance of IGZO TFTs fabricated on flexible substrates [69]. The study explores how TFTs respond to tensile and compressive strain at bending radii below 10 mm, both in darkness and under 90-lux illumination. The findings offer valuable insights into the impact of strain and light exposure on TFT mobility, threshold voltage, and long-term stability. The results indicate that tensile strain increases carrier mobility and decreases threshold voltage, whereas compressive strain reduces mobility and increases threshold voltage. Additionally, mechanical bending alone causes only minor shifts in electrical characteristics, but when combined with illumination, the effects become significantly more pronounced—particularly under tensile strain.

Kim *et al.* investigate the electrical behavior of flexible complementary inverters composed of p-channel pentacene TFTs (OTFTs) and n-channel IGZO TFTs under mechanical

bending, examining how strain impacts key parameters such as voltage transfer characteristics, field-effect mobility, threshold voltage, and source-drain saturation current [70]. The study reveals that mobility decreases and threshold voltage increases in OTFTs due to increased molecular spacing in pentacene, which reduces charge carrier hopping efficiency. In contrast, IGZO TFTs exhibit increased mobility and decreased threshold voltage under bending, attributed to a reduction in electron effective mass and possible changes in oxygen vacancies. These opposing trends in mobility and threshold voltage directly affect inverter performance, causing a negative shift in switching threshold voltage (V_T) as bending radius decreases. While voltage gain initially increases, it slightly declines at very small bending radii, highlighting the mechanical strain sensitivity of these hybrid inverters.

As shown in Figure 2.5, Li *et al.* investigated the impact of compressive and tensile strain on a 3-to-8 decoder utilizing bootstrap logic based on a-Si:H TFTs [26]. Their findings demonstrated superior output swing and lower power consumption compared to other logic gate implementations, highlighting the efficiency of this approach.

Researchers in [25] introduced Flex-RV, a 32-bit bendable microprocessor built on the open Reduced Instruction Set Computer V (RISC-V) instruction set and fabricated using IGZO TFTs on a flexible polyimide substrate. Designed as an ultralow-cost alternative to traditional silicon-based processors, Flex-RV integrates a programmable Machine Learning (ML) hardware accelerator with custom RISC-V instructions, enabling lightweight Artificial intelligence (AI) applications. Its mechanical stress tests demonstrated exceptional durability, with only a 4.3% performance variation when bent to a 3 mm radius, highlighting its potential for wearables, smart packaging, and next-generation flexible electronics.

2.9 Summary

TFT based circuits have the potential to serve as a cornerstone of modern electronics, providing flexible, cost-effective, and scalable solutions to address the growing needs of industries such as consumer electronics, healthcare, and the IoT. In this chapter, we explored the various types of TFTs, their applications, and their limitations. Additionally, we examined several state-of-the-art designs developed to address these challenges effectively. However, existing designs do not adequately account for direct path current, and research on the effects of bending remains limited.

This thesis proposes digital circuit designs to mitigate the direct path current issue while also conducting an extensive study on the impact of bending. A deeper understanding of these factors will contribute to the advancement of TFT based circuit performance and reliability.

Chapter 3

Flexible Low-Power Logic Circuits with Unipolar Thin-Film Transistors

3.1 Introduction

As discussed in previous chapters, TFTs are widely used in flexible electronics, such as bendable displays, wearable devices, electronic skin, and smart patches. CMOS fabrication on flexible substrates is generally unsuitable due to its high-temperature processing requirements and limited mechanical durability. Therefore, TFT based circuits are built on flexible substrates, while most complex circuitry remains on rigid CMOS ICs [3, 71, 72, 73, 74, 75, 76, 77]. A soft ribbon cable is used to connect off-panel rigid CMOS and flexible TFT circuits. This requires a significant number of signals from CMOS ICs, which limits the circuit complexity that can be implemented on flexible substrates [13]. With an increase in the number of signals originating from off-chip components, the cost and reliability of connecting flexible electronics with soft ribbon cables also become an issue [26]. Thus, it is desirable to implement on-chip TFT logic circuits.

Another key application of TFTs is in displays, where TFTs are primarily used for pixel circuits, while most control and driver circuits are implemented using off-panel CMOS ICs [26, 56, 53, 78, 79]. This limits the scalability of display resolution. As the display resolution increases, the number of bonding pads required to interface with off-panel ICs also increases. However, the pitch, constrained by mechanical limitations, becomes a bottleneck in achieving high-density, large-scale displays. Moreover, power dissipation caused by high-capacitance bonding pads needs to be addressed. Therefore, to further enhance display technology, it is crucial to implement the control logic and drivers directly on the TFT

backplane, rather than relying on CMOS circuits, thus reducing the need for numerous bonding pads [26].

Owing to their fundamental dissimilarity from crystalline silicon CMOS technologies, disordered semiconductor TFTs are primarily unipolar, lacking the advantages of complementary transistor types. Therefore, it has always been difficult to implement complex multi-stage logic circuits due to the limited output swing and high static leakage current. To address these issues, several attempts have been made to enhance fabrication techniques to have complementary transistors. Researchers have proposed solutions involving LTPS using laser annealing techniques to achieve a complementary device type [80, 81, 82, 83]. Additionally, researchers have also explored the incorporation of a secondary gate metal to enhance control over the TFT channel [31, 84]. Nevertheless, the considerable expenses and intricate nature of these approaches have not yielded the desired benefits. Consequently, the integration of various TFT based logic circuits on a single substrate has not been able to compete with CMOS technology in terms of performance.

As discussed in Section 2.5, several researchers have previously attempted to address the issue in unipolar logic gates with innovative circuits [26, 32, 53, 55, 56, 85, 86, 87, 88]. However, most research on TFT logic circuits lacks analysis on flexible substrates, especially under conditions of mechanical stress. T. -H. Huang *et al.* demonstrated a technique to achieve full output swing on a glass substrate, but it requires an additional voltage supply [32]. Recently, a bootstrapped technique based TFT circuit to achieve full output swing and limit static leakage current has been proposed [26]. Through these implementations, leakage current is reduced. However, since the TFT switching speed is substantially lower compared to the CMOS transistor, and the presence of direct path current, the static power is a significant fraction of overall power consumption in TFT circuits.

In this chapter, we propose novel half-latch-based logic gates to minimize direct path current and achieve full output swing in TFT circuits. We also implemented a decoder on both glass and flexible substrates using a low-temperature process as an example of the implementation of complex logic using unipolar TFT circuits. The proposed 3-to-8 decoder design results in a total power saving of 46.5% compared to the state-of-the-art design. Additionally, the impact of bending of flexible substrate was also examined. To the best of our knowledge, there are very limited studies to report the effects of substrate change and the bending of flexible substrates on TFT based digital circuits [26, 69, 70].

The chapter is organized as follows: Section 3.2 discusses background and prior art techniques, while Section 3.3 introduces the proposed design, using the inverter gate as an example. This section also covers the implementation of decoder circuits based on the proposed design. Section 3.4 presents device fabrication, modeling, simulation results, and

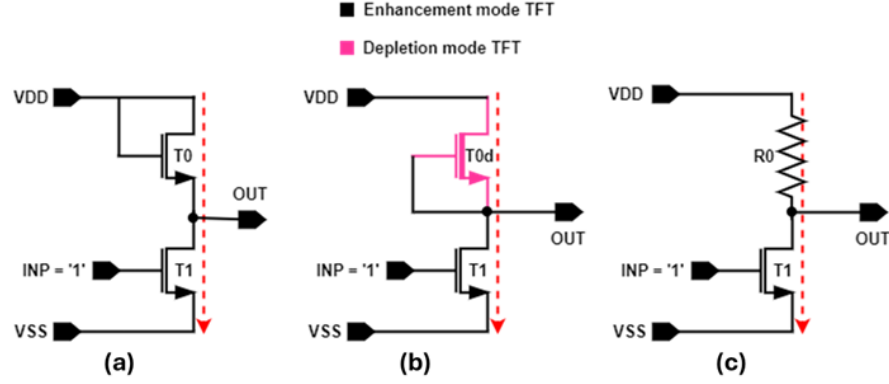


Figure 3.1: Conventional INV with pull-up circuit using (a) enhancement mode TFTs, (b) depletion mode TFT, and (c) resistor. The red dotted line shows a direct path current.

comparative analysis between the proposed design and state-of-the-art techniques. Section 3.5 presents the measurement results. This section also discusses the impact of bending the flexible substrate on TFT performance. Finally, Section 3.6 concludes the chapter.

3.2 Recent Advancements in Unipolar TFT Circuit Design

Figure 3.1(a) shows the conventional 2T inverter, which has significant drawbacks due to its limited output swing, and high static power consumption, as discussed in Section 2.5. Researchers have also explored the use of depletion-mode TFT (instead of conventional enhancement-mode TFT) as a pull-up load, as shown in Figure 3.1(b) [85]. Enhancement mode TFTs are normally OFF devices, meaning no current flows when the gate-source voltage (V_{GS}) is zero; a suitable gate voltage must be applied to induce a conductive channel and turn the device ON. In contrast, depletion mode TFTs are normally ON, with a conductive channel present at $V_{GS} = 0$; applying a gate voltage of the opposite polarity depletes carriers and turns the device OFF. In terms of fabrication, enhancement-mode TFTs are typically designed with undoped or lightly doped channels, requiring precise control of the gate dielectric and semiconductor interface to ensure that the channel forms only under sufficient gate bias. These devices often rely on inducing an inversion or accumulation layer for conduction. In contrast, depletion-mode TFTs are fabricated with a heavily doped or inherently conductive channel, so they conduct at zero gate bias. This may involve higher

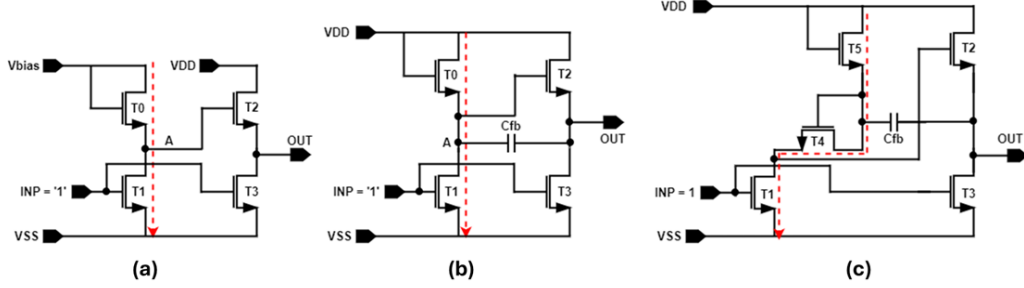


Figure 3.2: (a) 4T pseudo-CMOS INV with additional bias voltage [32], (b) 4T INV [54], and (c) 5T INV [26]. The red dotted line shows a direct path current.

doping levels or different materials/processing steps to ensure that the channel is naturally populated with carriers. As a result, depletion mode devices can require extra steps/masks, which results in higher costs.

In comparison to the resistor-loaded design shown in Figure 3.1(c), where the resistor serves as a fixed passive load, TFT-based load designs shown in Figures 3.1(a) and 3.1(b) offer improved area efficiency. However, all these designs—whether using passive resistors or active TFT loads—suffer from limited output voltage swing and significant direct-path current. In this thesis, the enhancement-mode TFT-based design depicted in Figure 3.1(a) is used as the reference conventional design because of its lower cost.

To achieve full output swing, researchers in [32] demonstrated a pseudo-CMOS logic circuit on a glass substrate, as illustrated in Figure 3.2(a). This design achieves full output swing; however, it does not resolve the problem of high static power consumption. Chen *et al.* attempted to tackle the issue of output swing by introducing a 4-TFT (4T) inverter design on a glass substrate using dual-gate TFTs [54]. This design was further optimized by Tiwari *et al.* by using a single gate TFT structure, as shown in Figure 3.2(b) [55]. Papadopoulos *et al.* introduced a bootstrapped 7-TFT (7T) inverter on a glass substrate to achieve full output voltage swing [56]. Li *et al.* demonstrated a similar bootstrapped 5-TFT (5T) inverter on a flexible substrate, shown in Figure 3.2(c), to achieve full output swing with a comparatively smaller area overhead than the 7T inverter [26]. To reduce the direct path current when the input is high, Li *et al.* introduced an additional diode-configured TFT T4. Although these circuits resolve the issue of full output swing in unipolar TFT logic gates, the problem of high direct path current remains a concern.

To better understand the primary reason behind the high power consumption of TFT circuits, we simulate simple inverter circuits and measure the power consumption across four different time frames (TFs). As illustrated in Figure 3.3, the pulse input response and

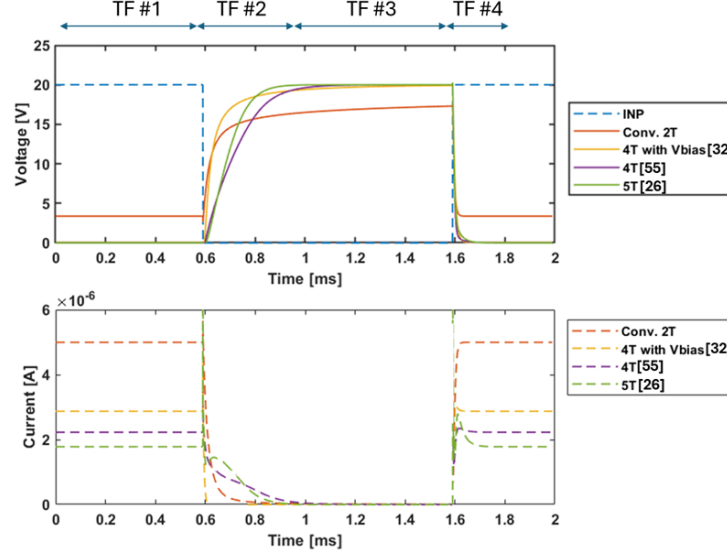


Figure 3.3: Simulated response for a pulse input of conventional 2T inverter, 4T pseudo-CMOS INV with additional bias voltage [32], 4T INV [55], and 5T INV [26]. Power consumption is measured in four different timeframes i.e., TF #1, TF #2, TF #3, and TF #4.

power consumption of the inverters are measured during four distinct timeframes. The first timeframe (TF #1) represents static power consumption when the input is at ‘logic 1’. The second timeframe (TF #2) captures dynamic power as the primary power consumption source when the input transitions to ‘logic 0’. The third timeframe (TF #3) indicates static power consumption when the input is at ‘logic 0’, and the fourth timeframe (TF #4) represents dynamic power as the major power consumption source input switches back to ‘logic 1’. A 10 pF load capacitor is connected to the output terminal of each inverter.

Table 3.1 shows the power consumption of simulated results of conventional and state-of-the-art unipolar **TFT** inverters. The 5T inverter shows superior results in terms of power consumption, consistent with the previous report [26]. Notably, the power consumption in TF #1 is the dominant for all the inverter designs. This is because when the input is ‘logic 1’, there is a direct-path current from V_{DD} to V_{SS} (marked by red dotted lines in Figures 3.1 and 3.2). This leads to high static power consumption as long as the input remains ‘logic 1’ in all the inverters. It is evident that while these methods reduce static power consumption compared to conventional 2T inverters, the direct path current when the input is ‘logic 1’ is an unanswered question. It should be noted that the conventional

Table 3.1: Simulated power consumption of conventional and state-of-the-art inverters across 4 timeframes shown in Figure 3.2.

	Power Consumption (μW)			
Time Frame	TF #1	TF #2	TF #3	TF #4
Major Power Consumption	Static Power	Dynamic Power	Static Power	Dynamic Power
Input State	1	$1 \rightarrow 0$	0	$0 \rightarrow 1$
Conv. 2T	99.88	9.64	0.31	45.60
4T with ext. Vbias [32]	67.55	13.52	0.21	33.82
4T [55]	44.51	14.37	0.17	21.63
5T [26]	35.61	15.90	0.02	21.59

2T inverter consumes less dynamic power compared to other designs. This is because of the limited output swing. It should be noted that the output drives a 10 pF load capacitor, requiring larger sizes for T0 and T1, which results in higher direct path current. In contrast, the load for the 4T inverter and the 4T inverter with an external Vbias driving internal node A is smaller, allowing for reduced sizes of T12 and T13, which leads to lower direct path current. The detailed device sizes are discussed later in section 3.4.

The researchers in [89] introduced a crossover logic to address the issue of direct path current, shown in Figure 3.4. However, the design, implemented on glass substrates, is considerably slow since the transition from ‘logic 0’ to ‘logic 1’ depends primarily on leakage current. This occurs since all the TFTs remain in the off-state during this phase, as shown in Figure 3.4. Furthermore, this method fails to achieve a full output voltage swing, which complicates the design of multi-stage circuits due to inadequate stage-to-stage gain.

Qin et al. demonstrated an alternative method to reduce direct path current using differential logic on a glass substrate, as shown in Figure 3.5 [88]. This design employs differential inputs and cross-coupled pull-down transistors to suppress direct path current while generating complementary outputs. However, it requires twice the number of inputs, leading to increased routing complexity. Additionally, the limited output swing in this design results in low stage-to-stage gain, making it challenging to implement complex circuits.

Unipolar logic gates face the fundamental challenge of high static power consumption.

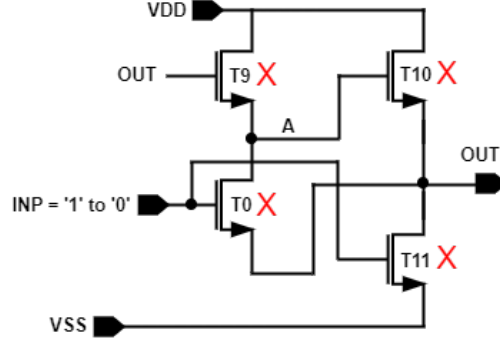


Figure 3.4: Cross-over logic (COL) based inverter design. X mark indicates off state when input transitions from ‘logic 1’ to ‘logic 0’ [89].

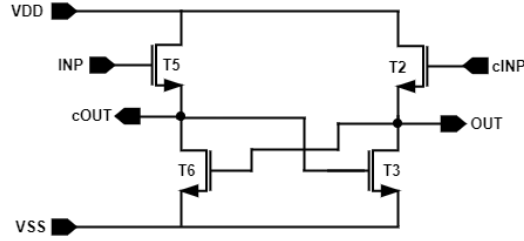


Figure 3.5: Differential logic (DL) based inverter design [88].

Arguably, dynamic logic with pre-charge and evaluation phase would be attractive to implement logic with TFT [90]. However, a closer inspection reveals several challenges with this approach. Firstly, it would require two complementary clocks. Secondly, dynamic logic does not address the output swing problem. Additionally, cascading multistage logic with dynamic logic gates alone is challenging. To ensure proper functionality, domino logic is employed, where an inverter is placed at the output of each dynamic logic gate in every stage to implement multistage logic. However, using these additional high-power-consuming inverters diminishes the advantage of dynamic logic’s low static power consumption. Last but not least, TFT circuits operate at low frequencies (in the kHz range), making charge leakage a significant issue in dynamic logic circuits.

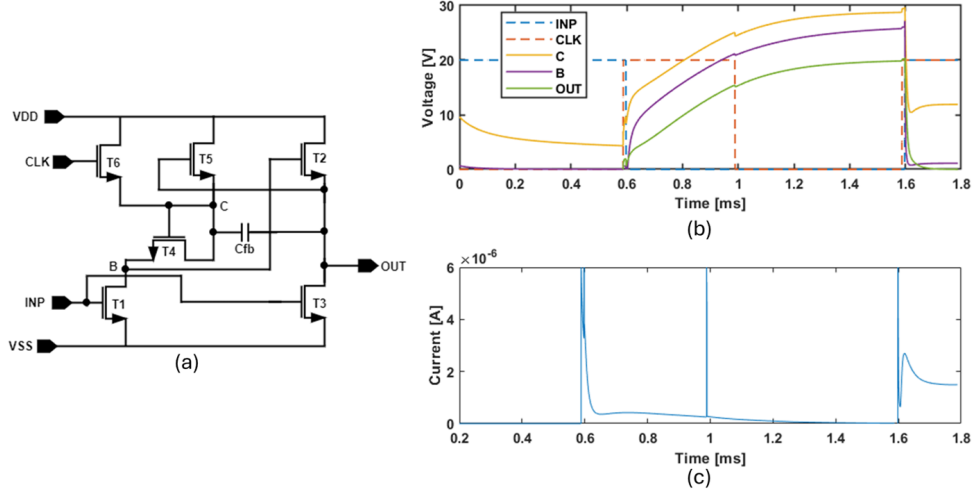


Figure 3.6: (a) Proposed half-latch INV gate design, (b) its input-output waveform, and (c) current waveform.

3.3 Proposed Half-Latch Logic Design

3.3.1 Logic Gates

The schematic of the proposed half-latch 6T inverter is illustrated in Figure 3.6(a). This design is specifically crafted to minimize leakage power in unipolar TFT logic circuits. It employs bootstrap logic to achieve a full output voltage swing. A feedback connection from the output to T5 ensures the direct path current between V_{DD} and V_{SS} is cut off when the input is at 'logic 1'. Additionally, a periodic clock signal (CLK) is introduced to boost the internal node, facilitating smooth output transitions. As discussed in later sections, for multi-stage logic, this periodic signal can be substituted with internally generated signals.

The operation of the proposed 6T inverter proceeds as follows: When the input transitions from 'logic 0' to 'logic 1,' node B and the output are discharged via T1 and T3, respectively. This action deactivates T2, allowing the output to drop to V_{SS} . Once the output reaches V_{SS} , T5 is fully turned off, effectively cutting off the direct current path between V_{DD} and V_{SS} , thereby significantly reducing static leakage current compared to the designs discussed in Section 3.2. When the input transitions from 'logic 1' to 'logic 0,' T1 and T3 are deactivated, and the CLK boosts internal node C. As node C rises, T2 partially turns on, activating T5 and causing node B to rise further. Eventually, the output reaches full V_{DD} due to the bootstrap circuit formed by TFTs T2, T4, T5, and the

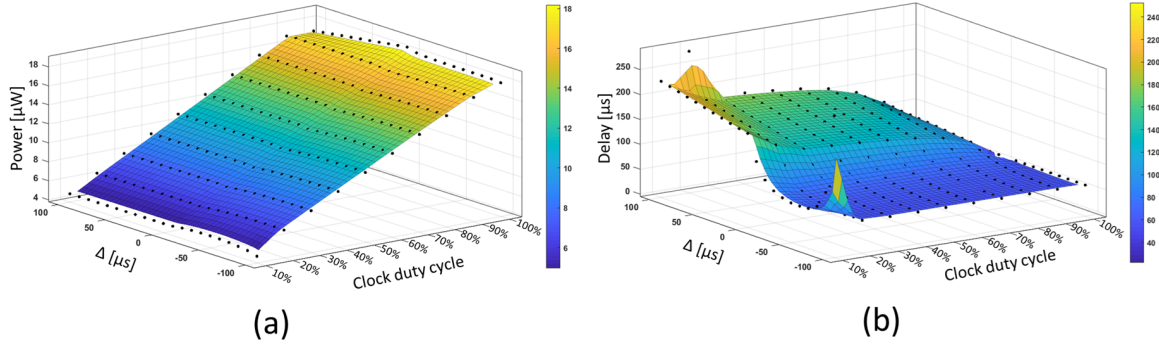


Figure 3.7: Simulation based (a) Power consumption, and (b) Propagation delay as a function of Δ (Clock positive edge – Input positive or negative edge) and clock duty for the proposed inverter design.

feedback capacitor (Cfb).

However, if both the CLK and input are high, a direct path current flows through T6, T4, and T1. Although the CLK is unnecessary during input transitions from ‘logic 0’ to ‘logic 1,’ it is maintained periodically since the input to any logic gate can vary between 0 and 1. The simulated input-output waveform and the behavior of internal nodes are depicted in Figure 3.6(b).

Unlike dynamic logic, the output of the proposed logic gate is actively driven by T2 or T3, making precise clock synchronization less critical. If the clock signal arrives too early, it increases power consumption due to the direct path current flowing through T6, T4, and T1. Conversely, if the clock signal is delayed relative to the input transition, it slows the output transition. However, these timing variations do not disrupt the circuit’s functionality.

Figure 3.7 illustrates the impact of clock synchronization (Δ = Clock positive edge – Input positive or negative edge) and clock duty cycle on the inverter’s power consumption and propagation delay. This characteristic can also be leveraged to mitigate process variations. For example, if fabricated devices exhibit higher threshold voltages (V_T) due to variations, the clock duty cycle can be extended to compensate for the slower speed, ensuring reliable operation.

The schematics for the NAND and NOR gates based on the proposed half-latch logic design are shown in Figure 3.8(a) and Figure 3.8(b), respectively. The output transition from ‘0’ to ‘1’ in these gates operates similarly to the inverter described earlier. However, the output transition from ‘1’ to ‘0’ is governed by the series pull-down TFTs in the NAND

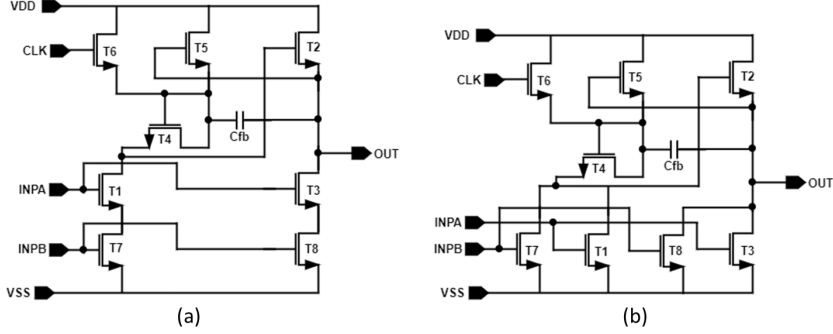


Figure 3.8: Proposed half-latch design based (a) NAND gate, and (b) NOR gate.

gate and the parallel pull-down TFTs in the NOR gate, reflecting their respective logic functions.

To evaluate the impact of limited output swing, we design a test-bench setup consisting of a six-stage inverter delay chain, as illustrated in Figure 3.9(a). As shown in Figure 3.9(b), the conventional unipolar 2T inverter exhibits progressive signal degradation across successive stages due to its restricted output swing. This degradation occurs because the reduced voltage levels are insufficient to fully switch subsequent stages, ultimately compromising signal integrity and circuit reliability.

The state-of-the-art 5T inverter [26] achieves full output swing, thereby preserving signal integrity across stages, as shown in Figure 3.9(c). However, as discussed in the previous section, this design suffers from high direct path current, which remains a significant drawback. Differential logic, shown in Figure 3.5, has been proposed as a solution to mitigate direct path current. However, due to its limited output swing, it suffers from low stage-to-stage gain, leading to signal integrity concerns, as shown in Figure 3.9(d). The proposed design overcomes both the direct path current issue and signal degradation. As shown in Figure 3.9(e), it maintains unity stage-to-stage gain, allowing it to function like true CMOS-logic using unipolar TFTs.

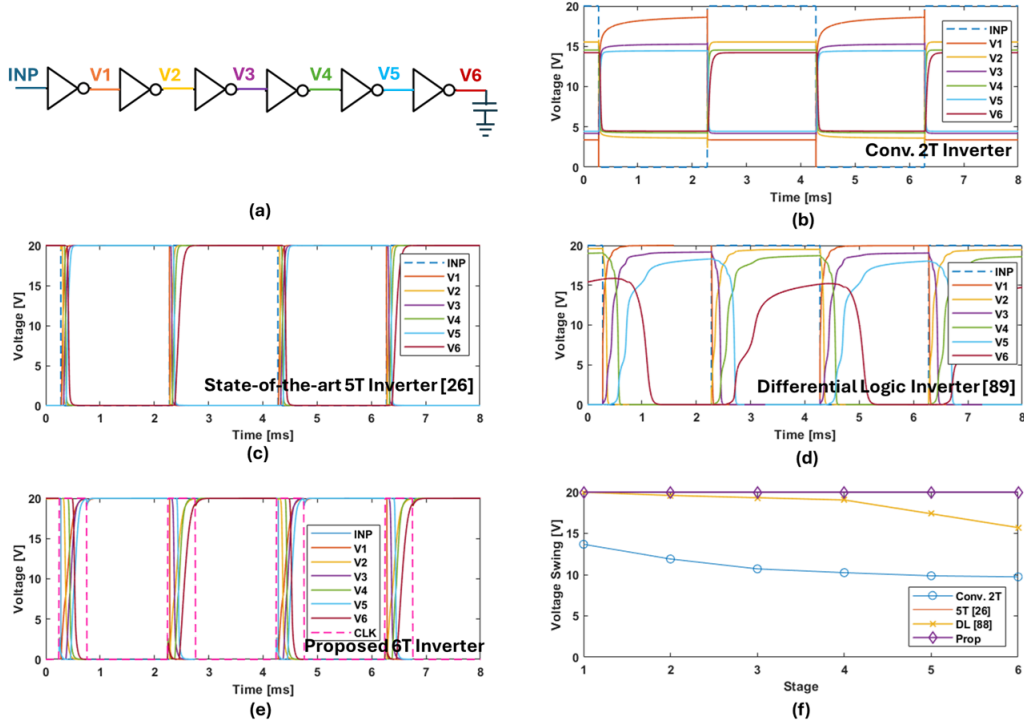


Figure 3.9: (a) Schematic of a six-inverter delay chain. Transient voltage waveform of every stage of the delay chain formed by (b) 2T, (c) 5T [26], (d) DL [89] and (e) Proposed 6T inverters. (f) Comparison of the stage-to-stage voltage swing.

3.3.2 Multi-stage Logic with Local Clock

To demonstrate the implementation of complex multi-stage logic, this work uses decoders as an example. Decoders can function as row-select drivers, significantly reducing the number of bonding pads required to connect the panel substrate to external drivers. For instance, in an $m \times n$ display array, there are typically n row-select pads. However, by incorporating a decoder, the required number of pads can be reduced to $\lceil \log_2 n \rceil + 1$. This advantage becomes increasingly significant as the array resolution grows, given that the physical size of bonding pads does not scale effectively with advancements in technology. For simplicity, the figures in this chapter illustrate the design and operation of a 1-to-2 decoder. Additionally, we have implemented larger configurations, including 2-to-4, 3-to-8, and 4-to-16 decoders, to showcase the scalability of the proposed approach.

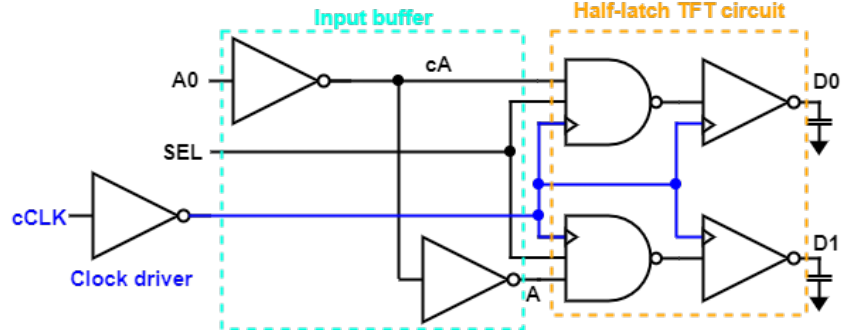


Figure 3.10: Gate level schematic of 1-to-2 decoder using the proposed half-latch circuit. 5T inverter [26] is used for the input buffer and clock driver.

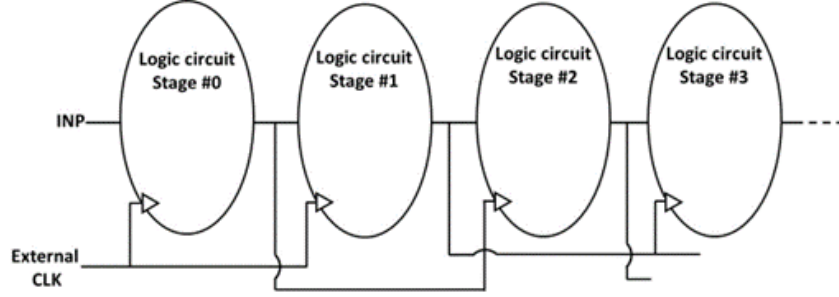


Figure 3.11: Local clocking method to reduce global clock signal load and make the circuit more scalable. The clock in a stage is driven by input to one previous stage.

Figure 3.10 illustrates the implementation of a 1-to-2 decoder, which employs an additional clock signal for each logic gate. This clock signal is generated using a 5T inverter [26]. While the clock signal and its corresponding inverter introduce additional power consumption, the overall power usage is significantly lower due to the minimal static power consumption of the other logic gates in the design.

While the decoder circuit implementation discussed earlier is efficient, we introduce a local clocking method to further enhance power savings. This approach is illustrated in Figure 3.11. In local clocking, the first two stages of the complex logic are driven by an external clock signal, while subsequent stages rely on internal signals for operation. This method reduces the load on the global clock signal, leading to lower dynamic power consumption and improved design scalability.

For example, in the proposed half-latch TFT circuits, the clock signal only needs to

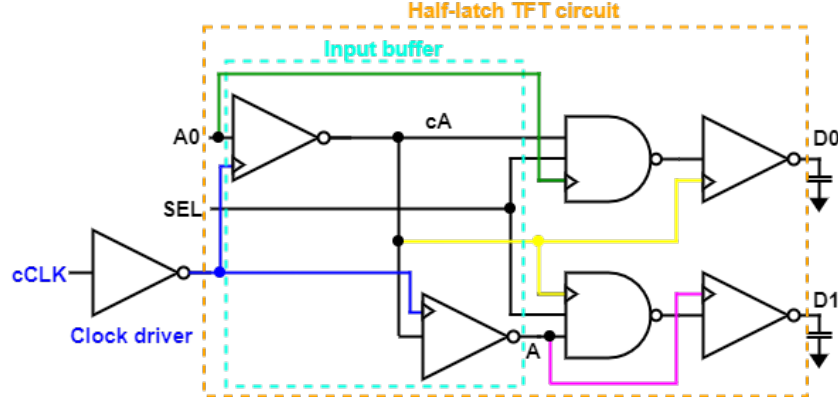


Figure 3.12: Gate level schematic of 1-to-2 decoder using the proposed half-latch circuit with local clocking. A 5T inverter [26] is used for the clock driver. The input buffer is driven by the external clock, while the clock of other half-latch gates is driven by internal nodes.

be at ‘logic 1’ when the gate input transitions from ‘logic 1’ to ‘logic 0.’ When the input to stage 3 changes to ‘logic 0,’ the input to stage 2 is already at ‘logic 1,’ which can be utilized as the clock signal for stage 3. This principle can be extended to derive clock signals for all stages from internal signals. By reducing the reliance on the global clock, the local clocking method decreases the clock’s load, making the design more scalable and power-efficient.

The implementation of a 1-to-2 decoder using local clock based half-latch TFT circuits is shown in Figure 3.12. Please note that the decoder circuit using local clocking, shown in Figure 3.12, is specifically designed for flexible display row drivers, where **A0** (the least significant bit in this case) toggles in every clock cycle.

3.4 Simulation Results

3.4.1 Device model

To analyze and enhance the performance of existing logic gates, a detailed device model for simulation is crucial. Initially, TFTs were fabricated on flexible PEN substrates using a standard five-mask a-Si:H TFT fabrication process, with a minimum feature size of 20 μm . A cross-sectional view is shown in Figure 3.13 [91].

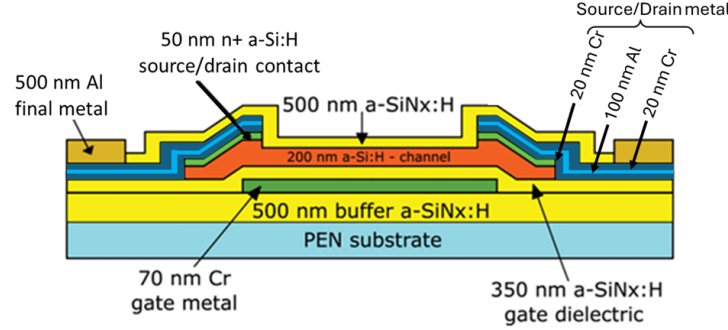


Figure 3.13: Cross-sectional view of fabricated a-Si:H TFT on flexible substrate.

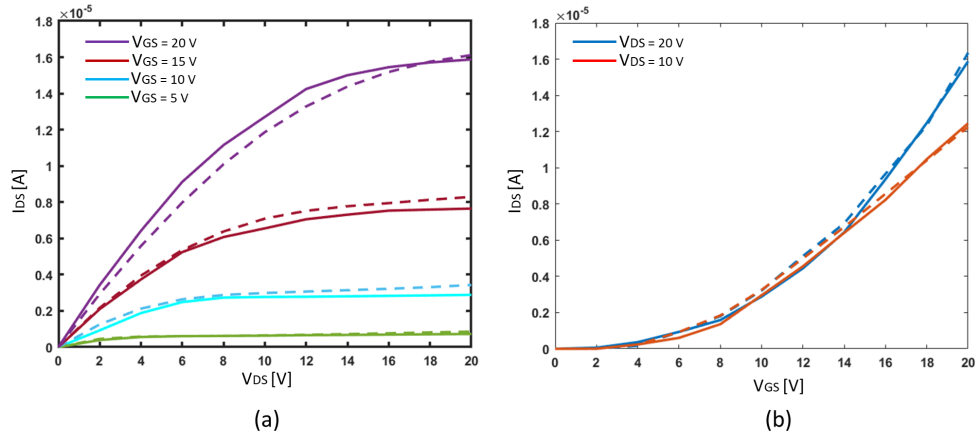


Figure 3.14: (a) I_{DS} vs V_{DS} and (b) I_{DS} vs V_{GS} curves for TFT on a flexible substrate with a channel width of $100 \mu m$ and channel length of $20 \mu m$. The dotted line shows simulation results, while the solid line shows measurement results.

Prior to the TFT process, a 500-nm amorphous silicon nitride (a-SiN:H) buffer layer was deposited on top of 125- μm -thick PEN substrates to: 1) suppress gas out diffusion from the substrate and 2) minimize stress-induced strain deformation of the substrates that improved the adhesion of the TFT layers to the PEN.

The device processing started with a 70-nm Cr deposition at room temperature by DC sputtering on top of the 500-nm a-SiN:H buffer layer on the PEN plastic substrates and the Cr layer was then patterned to form the bottom-gate metal (Mask 1). Next, a tri-layer of 350-nm a-SiN:H gate dielectric, 150-nm a-Si:H channel, and 60-nm n+ a-Si:H source/drain (S/D) ohmic contact layer was consecutively deposited at 170 °C using a

13.56-MHz PECVD.

The low-temperature (170 °C) TFT process was optimized through H₂ dilution of the SiH₄ precursor during deposition of the a-SiN:H gate dielectric and a-Si:H channel layers. H₂-diluted SiH₄ plasma is believed to enhance the effective surface diffusion length of long-lived SiH₃ precursor by increasing H coverage on the growing film surface, thereby creating good material properties at an even low deposition temperature. Using Fourier-transform infrared spectroscopy to compare different deposition conditions, an optimized high-quality N-rich a-SiN:H gate dielectric was obtained using a H₂/SiH₄ ratio of 20 and a H₂/SiH₄ ratio of 5 was employed to deposit a device-grade a-Si:H channel layer.

After patterning the TFT active area using dry etching (Mask 2), a 100-nm Cr/Al/Cr tri-layer for the S/D contact metal was deposited at room temperature by sputtering and subsequently patterned (Mask 3). This structure offers multiple benefits: the bottom Cr layer prevents interaction between Al and the silicon film, the middle Al layer reduces mechanical stress induced by Cr, and the top Cr layer protects the Al during subsequent processing steps such as wet and dry etching. The n+ a-Si:H layer was etched back using dry etching to define the effective channel region, followed by the deposition of a 350-nm passivation a-SiN:H layer. After opening a contact via (Mask 4) in the passivation layer, a 300-nm-thick Al thin film was deposited at room temperature by sputtering and patterned to form the final external metal contacts (Mask 5). The fabricated test wafers were annealed in vacuum at 150 °C for 2 h before the electrical measurements.

After fabrication, two Keithley source meters (models 2400 and 6430) were utilized to measure the I_{DS} vs V_{DS} and I_{DS} vs V_{GS} characteristics. Circuit simulations were performed in the Cadence Virtuoso environment using the model with fitting parameters calibrated to the fabricated TFT device. The modified level-61 a-Si TFT model [33, 34] parameters used for simulation are shown in Table 3.2. Figure 3.14 demonstrates a close match between the measured and simulated I-V curves of the TFT device. The fabrication process on glass substrates is similar, except that the 500 nm a-SiNx buffer layer (shown in Figure 3.13) is omitted.

3.4.2 Simulation Results

The device geometries were determined through simulations and optimization to achieve a balance between power, performance and footprint, as shown in Figure 3.15. Table 3.3 shows the TFT widths used in the comparative study; the channel length for all TFTs was kept at 20 μm *i.e.*, the minimum feature size of the fabricated TFTs. Refer to Figures 3.1(a), 3.2, 3.4, 3.5, 3.6(a), and 3.8 to identify the devices listed in Table 3.3. The V_{DD}

Table 3.2: A-Si:H model parameters based on fabricated TFT devices.

Parameters	Values
Gate dielectric thickness	350 nm
Relative gate dielectric constant (ϵ_r)	6.2
Unit gate dielectric capacitance (C_{dielec})	$0.156 \text{ fF}/\mu\text{m}^2$
Threshold voltage (V_T)	3.1 V
Carrier mobility (μ_n)	$1.05 \text{ cm}^2/\text{V s}$
Source/drain overlap (L_{ovl})	15 μm

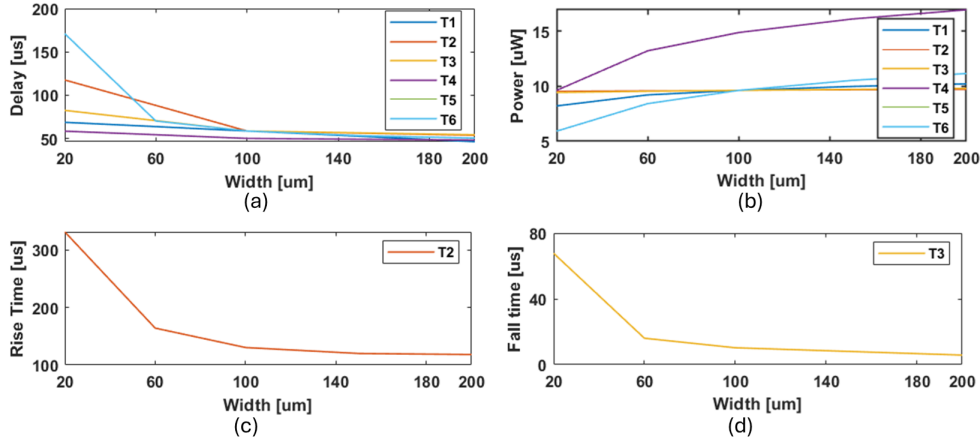


Figure 3.15: Simulation based (a) propagation delay, (b) total power consumption, (c) rise-time, and (d) fall-time of proposed 6T inverter when varying the width of TFTs.

used for simulations was 20 V, while the additional voltage V_{bias} used to simulate the pseudo-CMOS 4T inverter was kept at 23 V. The clock duty cycle was set to 40% for the proposed half-latch based designs.

Table 3.4 provides a simulation-based comparative analysis of various state-of-the-art inverter designs using unipolar TFTs. The table uses a color-coded scheme: red highlights the drawbacks of the designs, while green indicates desirable qualities. The simulation results reveal that the proposed half-latch inverter design achieves significant power savings at the cost of increased propagation delay. Compared to the conventional 2T inverter design, the proposed design reduces static power and total power consumption by 88.8% and 81.1%, respectively. Additionally, when compared to other designs, it delivers power savings of at least 47.3%. The 2T inverter demonstrates the shortest delay due to its single-stage architecture, whereas the other designs employ a two-stage architecture. Notably, the

Table 3.3: TFT channel widths used for comparative analysis.

Transistors	Width (μm)
T4, T12	20
T0, T11	40
T13	50
T1, T2, T3, T5, T6, T7, T8	100
T9, T10	400

Table 3.4: Simulation based comparative analysis of various state-of-the-art inverter designs

	Conv. 2T INV	4T INV with ext. bias [32]	4T INV [55]	COL INV [80]	5T INV [26]	Prop. 6T INV
# TFTs	2	4	4	4	5	6
# Capacitors	0	0	1	0	1	1
Full output swing	No	Yes	Yes	No	Yes	Yes
Clock	No	No	No	No	No	Yes
Add. voltage source	No	Yes	No	No	No	No
Total Power (μW)	51.02	36.07	24.70	18.37	21.51	9.69
Avg. Static power (μW)	49.96	33.77	18.33	10.53	17.80	5.57
Propagation delay (μs)	16.13	19.22	35.45	364.16	44.42	58.90
PDP (nJ)	0.82	0.69	0.87	6.69	0.95	0.57

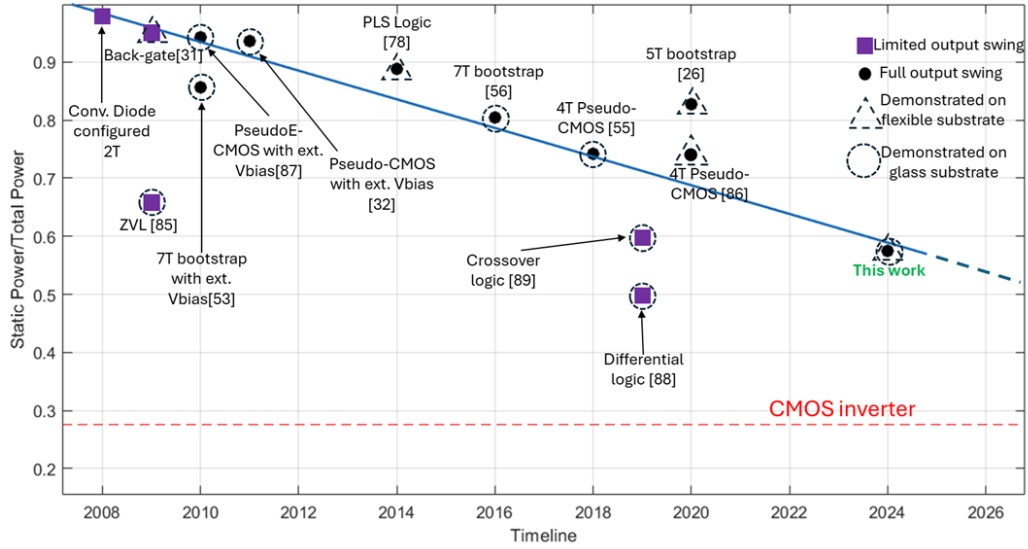


Figure 3.16: Simulation based static-power/total-power ratio trend for unipolar TFT inverter designs. The red dotted line shows the static-power/total-power for the CMOS inverter using TSMC 65nm technology.

crossover logic-based inverter incurs approximately 10 times the propagation delay of other designs because its output transition from ‘logic 0’ to ‘logic 1’ relies on leakage current [89].

It is important to note that the [Figure of merit \(FOM\)](#) used for comparing circuit designs in this work is the [power-delay-product \(PDP\)](#). In TFT circuit design, three key parameters are typically considered for performance evaluation, prioritized as follows: (1) Power consumption, (2) Delay, and (3) Area. Since TFTs are inherently lower in cost compared to CMOS devices, area efficiency is generally a less critical factor. As a result, this study focuses primarily on PDP, which captures the trade-off between power and speed, providing a balanced metric for evaluating the energy efficiency of different circuit designs. Compared to any other designs, the proposed inverter design reduces the PDP by at least 17.4%.

Figure 3.16 shows the simulation based static-power/total-power ratio trend for the unipolar TFT inverters, with a load capacitor of 10 pF and input frequency of 1 KHz. The red dashed line represents this ratio for a CMOS inverter using TSMC 65 nm technology operating at the input frequency of 1 KHz and supply voltage of 1 V. The ratio for TFT inverters is higher, primarily due to direct path current, which significantly contributes to high static power. It can be seen that, in conventional diode configured 2T inverter, more

Table 3.5: Simulation based comparative analysis of decoder circuit using various state-of-the-art TFT Logic gates.

Decoder size	Power consumption (uW)					
	Conv. Decoder Design	Pseudo-CMOS with ext. Vbias [32]	Pseudo-CMOS [55]	Boot-strapped [26]	Prop. Decoder with ext. clock	Prop. Decoder with local-clock
1-to-2	288.31	196.94	131.03	74.76	56.55	42.51
2-to-4	568.53	393.07	263.11	132.81	97.51	81.45
3-to-8	1048.22	720.64	497.96	232.89	149.43	121.90
4-to-16	1910.11	1315.07	934.62	407.78	229.80	200.10

than 95% of the total power is consumed by the direct path current. This is significantly higher compared to conventional CMOS technology, which consumes $\sim 25\%$ static power compared to total power when operated at a frequency of 1 *KHz*.

The graph clearly shows that circuit innovations over the years have progressively reduced leakage current. The proposed design shows significant improvement, indicating progress toward CMOS-like circuits. Although the cross-over inverter design comes close to achieving a low static-power to total-power ratio, it lacks full output swing and propagation delay is significantly higher, which hinders the realization of CMOS-like circuits [89]. Similarly, while differential logic design exhibits a low static-to-total power ratio, its limited output swing makes it challenging to implement multi-stage complex logic, as shown in Figure 3.9(d) [88].

To show the application of the proposed logic gate in multi-stage logic implementations, decoder circuits for display applications were simulated. Table 3.5 presents the power consumption analysis of decoders designed with the proposed logic gates compared to those using other state-of-the-art logic gate designs. Decoders were implemented using the half-latch logic with both a dedicated clock and a local clocking method, as outlined in Section 3.3. The results indicate that decoders designed with the proposed logic gate consume significantly less power than those using alternative designs. For instance, in a 3-to-8 decoder, the proposed designs with a dedicated clock and a local clocking method reduced total power consumption by 35.8% and 47.6%, respectively, compared to the bootstrapped logic gate design by Li *et al.* [26]. This power reduction is primarily attributed to the minimized static power consumption of the half-latch logic gates.

The local clocking approach provides greater power savings than the dedicated clock

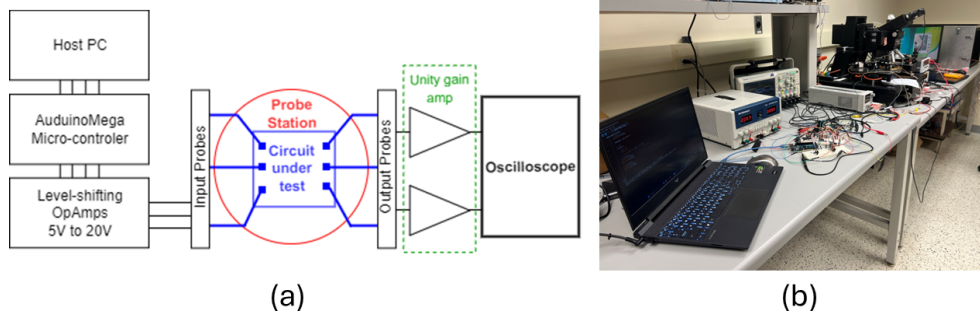


Figure 3.17: (a) Test-bench, and (b) measurement setup.

mechanism because it enhances scalability by reducing the load on the global clock network. This allows buffer stages in the decoder to be replaced with half-latch logic gates, further decreasing the clock load in the local clocking-based design.

To validate the power-saving potential of the proposed logic style, decoders of varying complexities were analyzed. The results revealed that power savings increased with the size of the decoder. This improvement arises because larger circuits involve more logic gates that typically contribute to static power consumption, and the proposed half-latch logic effectively mitigates this component.

3.5 Measurement Results

3.5.1 Testbench setup

To validate the proposed design, we fabricated logic gates and 3-to-8 decoders using both the proposed half-latch design and the state-of-the-art bootstrapped design [26] on glass and flexible substrates. A custom test bench, depicted in Figure 3.17(a), was developed to evaluate these designs. Input signals were generated by an Arduino Mega microcontroller controlled via a host PC and amplified to 20 V using non-inverting operational amplifiers (OpAmps). These amplified signals were directed to the test circuits through a probe station. To ensure accurate measurements, all outputs were fed through unity-gain OpAmps to the oscilloscope. Without the OpAmps, the oscilloscope's resistive load might distort the output signal [13]. Figures 3.18(a)-(c) illustrate the probing setup for circuits on a glass substrate, a flexible substrate under tensile stress, and a flexible substrate under compressive stress, respectively.

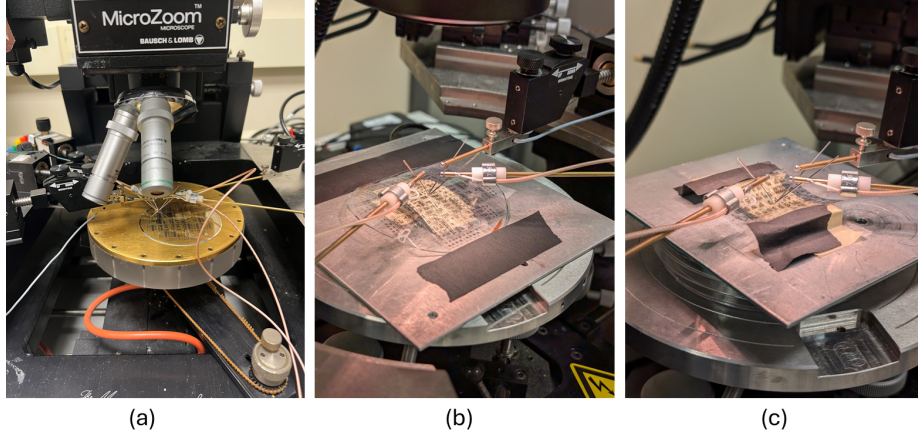


Figure 3.18: Probing of circuit on (a) glass substrate, (b) flexible substrate under tensile strain, and (c) flexible substrate under compressive strain.

3.5.2 Device characterization under tensile and compressive strain

Figure 3.19 shows the I-V characteristics of TFT devices on a glass substrate as well as on a flexible substrate. The results show that TFTs on the glass substrate exhibited higher currents compared to those on the flexible substrate. This is because the rigidity and thermal stability of glass resulted in fewer defects during the deposition of the TFT layers, leading to higher carrier mobility [92]. On the other hand, during deposition on a flexible substrate, slight deformations, thermal expansion, or shrinkage introduce irregularities in the a-Si:H layer. These irregularities can cause atomic misalignment and structural imperfections. These induced defects act as traps or scattering centers that hinder carrier movement, thereby lowering carrier mobility.

The effects of bending and orientation of TFTs on the flexible PEN substrate were also examined. Since the PEN substrate has a $125\ \mu\text{m}$ thickness and the radius of curvature for the sample holders is $4\ \text{cm}$, the resulting strain is $\epsilon = \pm 0.31\%$. On the flexible substrate, under tensile stress, TFTs showed a slight increase in carrier mobility, while under compressive stress, mobility decreased slightly. This behavior can be explained by the defect creation model [16]. When tensile stress is applied, the a-Si:H layer stretches, slightly relieving internal tension in the amorphous silicon network. This relief reduces the structural stress on the weak Si-Si bonds, leading to fewer defect states or trap sites in the material. With fewer defects, charge carriers encounter fewer trap states, making them less likely to be captured or immobilized. This reduction in trapping allows carriers to move more freely, resulting in a slight increase in carrier mobility under tensile stress. In

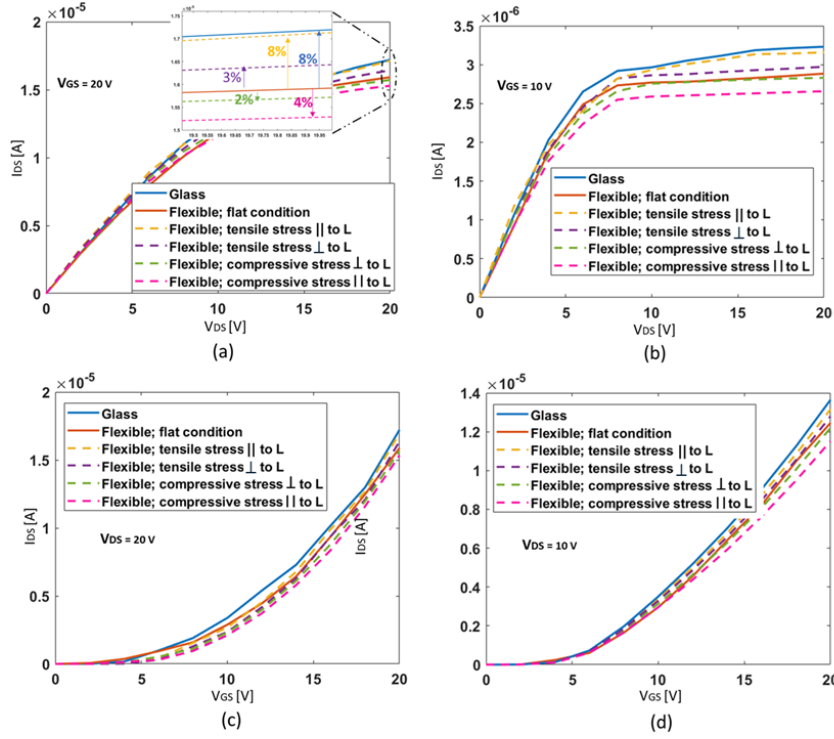


Figure 3.19: Measured I_{DS} versus V_{DS} curve at V_{GS} (a) 20 V, (b) 10 V, and I_{DS} versus V_{GS} curve at V_{DS} (c) 20 V, (d) 10 V for TFT on flexible and glass substrate with a length and width of 20 μm and 100 μm , respectively.

contrast, when compressive stress is applied, the amorphous silicon network is compacted, which puts additional strain on the weak Si-Si bonds. This compression can lead to the breaking or distortion of these bonds, increasing the density of defects within the material. As more weak bonds are disturbed, more dangling bonds and trap sites are created. These defects act as sites where charge carriers can be trapped, reducing their freedom to move and decreasing the overall carrier mobility.

It was also found that when bending occurs in the direction parallel to the current flow (along the TFT length), the impact of bending is most significant ($\sim 8\%$ increase and $\sim 4\%$ decrease in drain current in saturation mode under tensile stress and compressive stress, respectively). In contrast, when bending is perpendicular to the current flow, the mechanical stress has a relatively smaller effect ($\sim 3\%$ increase and $\sim 2\%$ decrease in drain current in saturation mode under tensile stress and compressive stress, respectively) [16]. This is because when bending occurs parallel to the current flow, the stress is directly

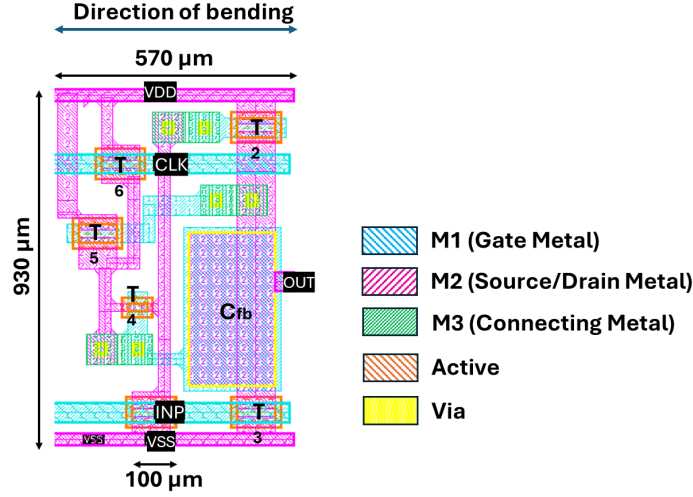


Figure 3.20: Layout of proposed 6T inverter. The TFTs are oriented with their widths parallel to the direction of bending, to minimize the impact of bending.

aligned with the carrier path as they move through the TFT. Therefore, the tensile or compressive forces act directly on the bonds within the channel, altering defect density and carrier mobility along the path of the current. As a result, the impact on carrier mobility is more pronounced. In contrast, when bending is perpendicular to the current flow, the mechanical stress is applied in a direction less critical to the movement of charge carriers through the channel. Although some strain is still present, it doesn't align with the current flow. This results in a relatively smaller effect on carrier mobility, as the primary pathway for charge transport isn't as significantly disturbed by the bending. Therefore, in order to minimize the effect of bending, the layout of circuits is designed such that all TFTs are placed along the direction of bending (i.e., along the TFT width). The layout of the half-latch 6T inverter is shown in Figure 3.20.

Flexible PEN substrates can shrink or deform under thermal or mechanical stress, which may cause misalignment during lithography, film cracking, poor adhesion, and non-uniform layer deposition. To improve TFT fabrication yield under these conditions, a 15 μm overlap was introduced between the source/drain and gate, and a minimum channel length and width of 20 μm was maintained across all designs. Additionally, vias, being critical failure points, were designed with dimensions of 30 $\mu\text{m} \times 30 \mu\text{m}$ and included a 25 μm metal extension beyond the via edge in all directions to enhance contact reliability and alignment tolerance.

As shown in Figure 3.20, in the proposed circuit designs using TFTs on PEN substrates,

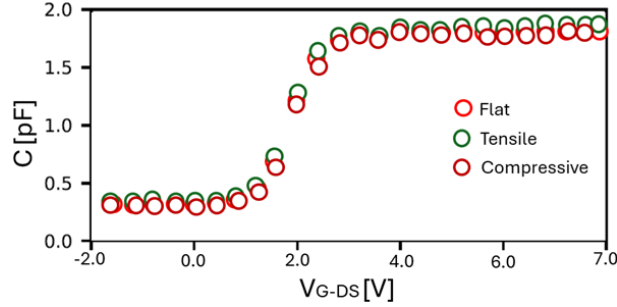


Figure 3.21: Effect of mechanical bending on C–V curve of MOS capacitor with a length and width of 20 μm and 100 μm , respectively [13].

Metal-Insulator-Metal (MIM) capacitors have been chosen for their superior electrical stability, linear voltage-independent behavior, and mechanical robustness—key advantages in flexible electronics. Unlike MOS-type capacitors, which suffer from nonlinear C–V characteristics due to bias-dependent semiconductor behavior, MIM capacitors offer predictable and stable capacitance, making them well-suited for timing-critical and low-power digital circuits. Additionally, MIM capacitors exhibit lower leakage currents and are less prone to degradation from interface traps, bias stress, and environmental factors, enhancing long-term reliability on mechanically flexible PEN substrates [13]. Lim et al. demonstrated that the C–V curve of a MIM a-Si:H capacitor on a flexible PEN substrate remains largely voltage-independent and flat under mechanical strain [93].

The threshold voltage (V_t) of a-Si:H TFTs is also influenced by externally applied mechanical strain. Under tensile strain, the a-Si:H lattice is stretched, which can reduce the density of shallow and deep trap states within the bandgap—particularly near the conduction band edge. This reduction in trap density allows the channel to invert more easily, resulting in a negative shift in threshold voltage [26, 94]. In contrast, compressive strain leads to a positive shift in threshold voltage. Compressive forces tend to increase trap state density, particularly in the deep states, which impedes carrier injection and requires a higher gate voltage to reach the onset of conduction [95, 96].

These effects are supported by the C–V characteristics of MOS capacitors (Figure 3.21 [13]). Tensile strain results in a leftward shift of the C–V curve and a sharper transition due to reduced interface traps, while compressive strain causes a rightward shift and stretch-out, reflecting increased localized states and trap-assisted capacitance. These shifts directly correspond to strain-induced modifications in the a-Si:H.

It should be noted that beyond externally applied strain, intrinsic strain plays a crucial

role in determining the baseline behavior of the device. Intrinsic strain is the built-in stress present in the device even when the substrate is in a nominally flat state. This stress originates from several sources during fabrication, including mismatches in the thermal expansion coefficients (CTEs) of different layers, deposition-induced stress (from PECVD or sputtering), and mechanical warping during cooling from process temperatures. For instance, if a layer deposited at 170 °C on a PEN substrate cools down to room temperature, differences in contraction rates can result in residual compressive or tensile strain in the semiconductor layer. While quantifying intrinsic strain precisely requires mechanical or spectroscopic analysis, its influence can often be inferred from electrical measurements. In this work, the fabricated TFTs exhibit an increase in drain current under applied tensile strain and a decrease under compressive strain. This behavior indicates that in these devices, the intrinsic strain is likely absent in the flat state.

3.5.3 Logic circuits

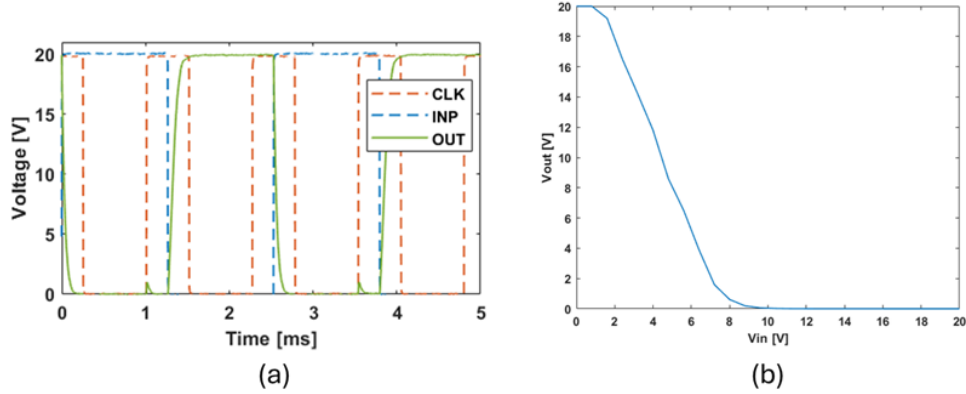


Figure 3.22: Measured (a) Oscilloscope waveform, and (b) transfer curve of the proposed 6T inverter design. The proposed design achieves full output swing.

The oscilloscope waveform of the proposed inverter design, shown in Figure 3.22(a), and the measured transfer curve, shown in Figure 3.22(b), demonstrate that the proposed design achieves a full output swing. Table 3.6 presents the measured power consumption of the proposed and state-of-the-art [26] inverter and 3-to-8 decoder designs on glass and flexible substrate under flat, tensile, and compressive conditions, respectively. At a supply voltage of 20 V, the state-of-the-art 5T inverter [26] and the half-latch inverter show average power consumptions of 25.31 μW and 11.34 μW , respectively. The proposed design

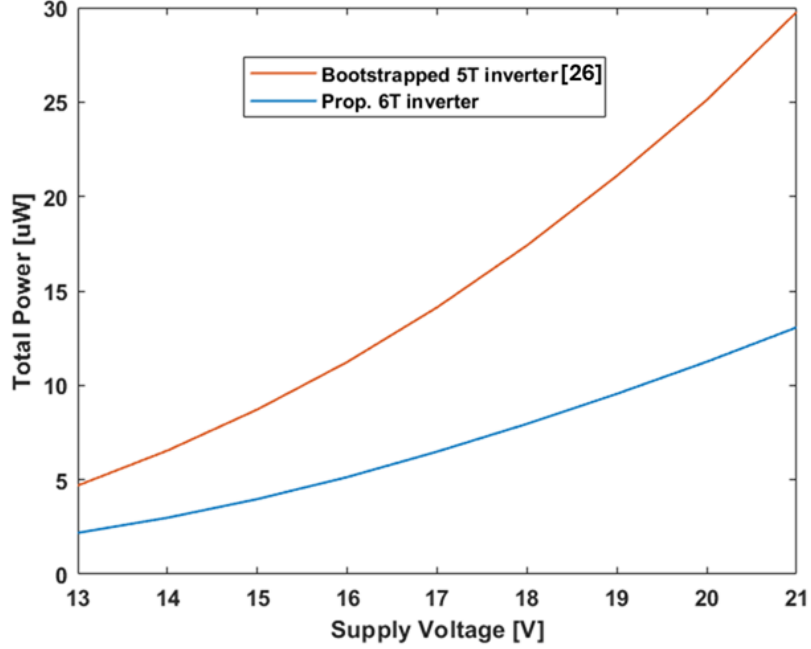


Figure 3.23: Measured Power Consumption V/S Supply voltage of 5T INV [26] and proposed inverter design.

achieves a 55.2% reduction in power consumption compared to the 5T inverter, primarily due to minimized direct path current. Figure 3.23 further compares the measured power consumption of the bootstrapped [26] and proposed inverter designs across varying supply voltages. The measured power is approximately 5% higher than the simulated power, primarily due to output padding and probing effects. Figure 3.24 illustrates the maximum frequency achieved by 3-to-8 decoders with a change in supply voltage, employing both bootstrapped [26] and proposed designs.

Figure 3.25 shows measurement results for the proposed local signaling-based 3-to-8 decoder at 1 kHz input frequency on both a glass substrate and a flexible substrate under flat, tensile, and compressive strain conditions. In all cases, the decoder maintained full-swing output signals and proper functionality. The measured average power consumption for the decoder using the bootstrap design [26] and the proposed local signaling-based half-latch design was 243.21 μW and 130.12 μW , respectively, resulting in a 46.5% average power savings.

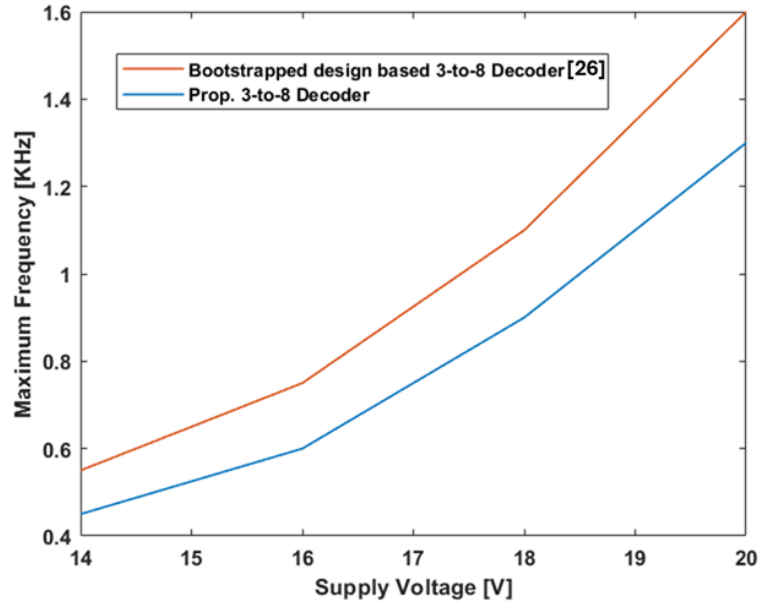


Figure 3.24: Maximum clock frequency V/S Supply voltage of bootstrapped design [26] and proposed design based 3-to-8 decoder.

Table 3.6: Power consumption measurements for the proposed inverter and decoder circuit compared to state-of-the-art designs.

	Power Consumption (μ W)				
Substrate	Glass	Flexible			Average
Condition	-	Flat	Tensile	Compressive	
5T INV [26]	25.55	25.25	25.39	25.06	25.31
Prop. INV	11.62	11.31	11.36	11.06	11.34
3-to-8 Decoder [26]	246.55	242.58	243.10	240.61	243.21
Prop. 3-to-8 Decoder	131.10	129.98	130.50	128.90	130.12

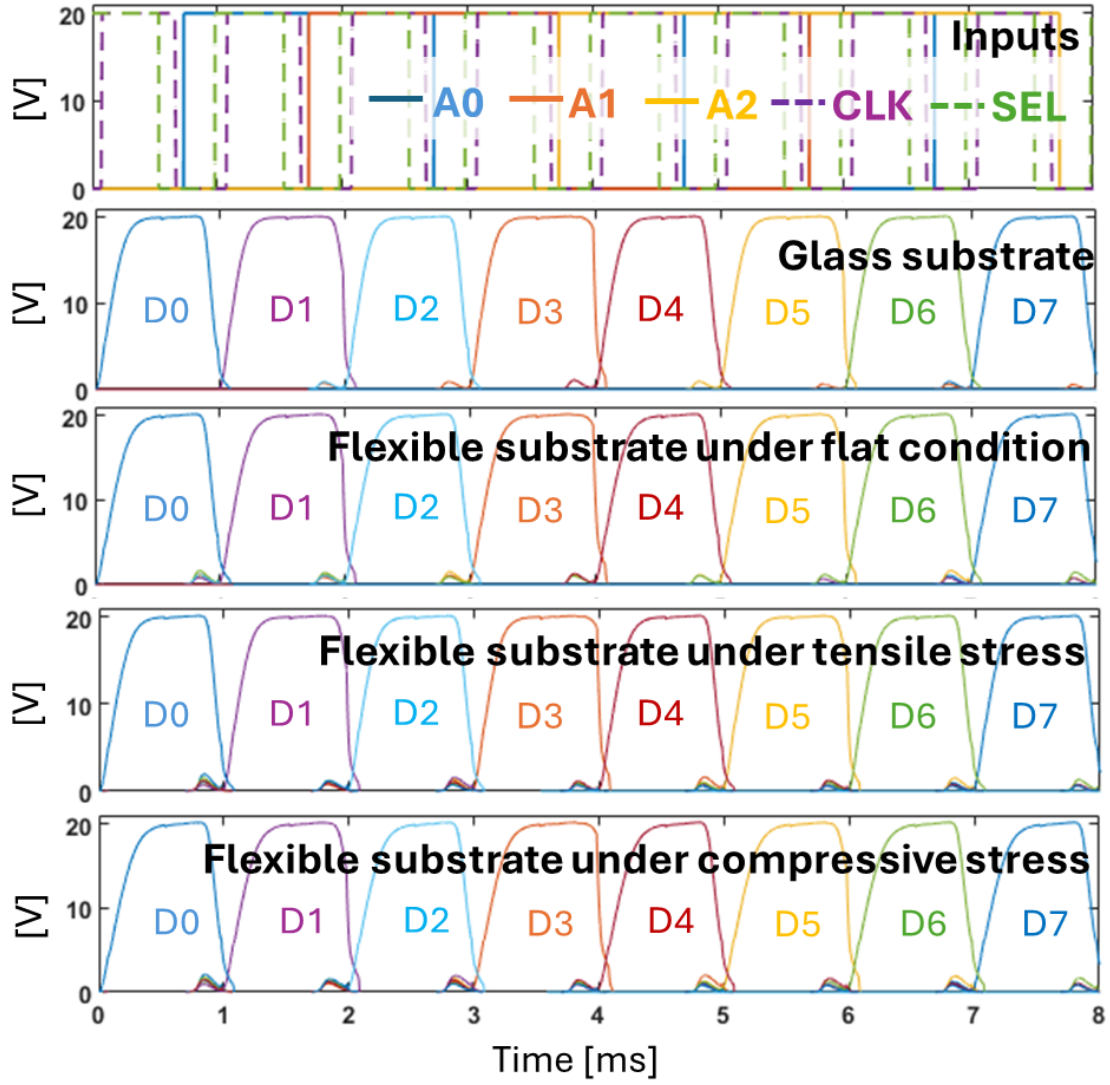


Figure 3.25: Measured input-output waveform of proposed local clocking based 3-to-8 decoder. A0-A2 represent the inputs, while D0-D7 are the corresponding decoded outputs. The design shows robust behavior and achieves full output swing under various conditions.

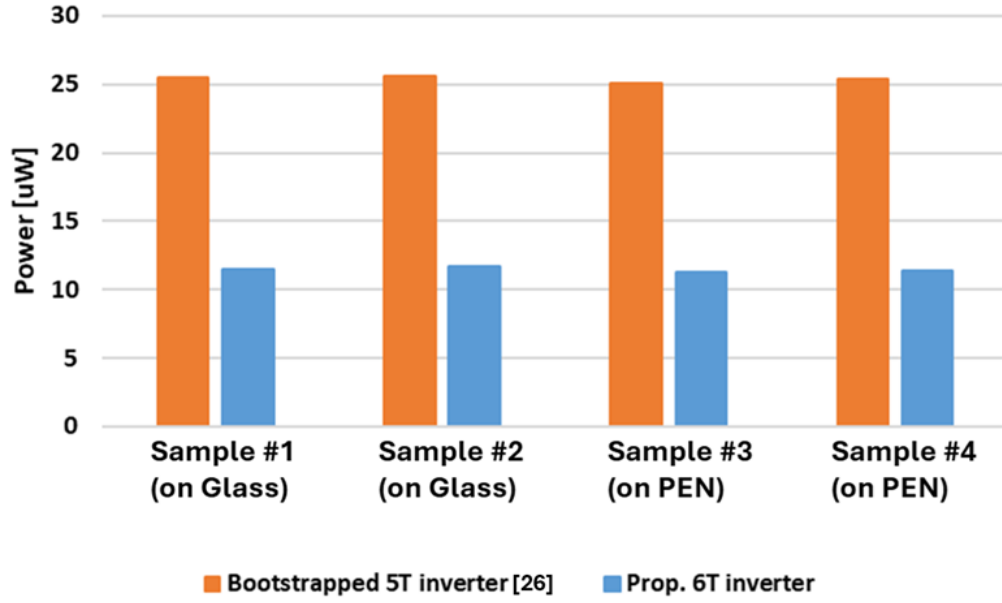


Figure 3.26: Measured variation of inverter power consumption over four samples. The observed variation is less than 4%.

Figure 3.26 shows variability of power consumption of bootstrapped [26] and proposed inverter designs. It was observed error associated with power consumption at different spatial locations is less than 4%. The reason for smaller variation and better yield is use of mature a-Si:H technology with 20 μm design rules.

Table 3.7: Comparison of reported works on Logic Circuits with TFTs.

	[32]	[55]	[85]	[26]	This Work
Technology	a-Si:H	IGZO	IGZO	a-Si:H	a-Si:H
Substrate	Glass	Glass	Glass	PEN	PEN, Glass
Full swing	Yes	Yes	No	Yes	Yes
# TFTs for an INV	7	4	4	5	6
VDD	20 V	10 V	5 V	20 V	20 V
Static Current of an INV	2.0 μ A	-	0.47 μ A	1.4 μ A	0.36 μ A
Total Power of an INV	-	-	-	-	11.34 μ W
Noise Margin of an INV	-	-	1.5 V	-	1.7 V
Propagation delay of an INV	-	-	0.5 μ s	-	63 μ s
Circuit realized	INV	INV, Ring Oscillator	INV, NAND, Ring Oscillator, Adder	INV, NAND, Decoder	INV, NAND, Decoder

Table 3.7 provides a comparison of this work with previous studies across different aspects of logic circuit performance. The inverter presented in this chapter achieves the lowest static leakage current while maintaining a full output swing, exhibiting CMOS-like behavior using a-Si:H technology. It is important to note that although the proposed inverter delay compared to COL inverter design [89] is significantly lower, as shown in Table 3.7, the COL design primarily relies on leakage current for output transition, as discussed in Section 3.2. The relatively slower speed of the proposed design can be attributed to the lower mobility of a-Si:H. However, choice of a-Si:H TFTs was driven by its suitability for

low-cost, low-temperature fabrication on PEN substrates, which are prone to deformation at higher temperatures [30]. Moreover, a-Si:H being more mature process, the yield is high even on flexible substrates. The existing simulation models do not account for variations in carrier mobility. This work provides an in-depth analysis of the effect of bending of the flexible substrate on circuit behavior, in addition, to the change in behavior on a glass substrate. It is important to understand the behavior of circuits under different bending conditions in order to address the deficiencies in existing TFT models. A deeper understanding of flexible circuits under bending conditions is essential for advancing flexible TFT ICs. The proposed half-latch design based circuits show promising results for the use of unipolar TFTs for low-budget low-power flexible circuit applications. In future work, we aim to integrate an LED array to implement TFT driven flexible display circuit.

3.6 Conclusion

This chapter introduced half-latch logic gates designed using unipolar n-type TFT technologies for flexible electronics applications. These gates achieve full output swing while minimizing static power consumption, enabling operation similar to CMOS. The implementation of a decoder was presented as an example of realizing complex logic on both glass and flexible substrates. Additionally, the effects of substrate bending on performance were analyzed. The study demonstrated that as the size of the decoder increased, the power savings with the proposed design became more pronounced. This is attributed to the growing number of static power-consuming gates in larger circuits, which the half-latch design effectively addresses. Measurement results revealed that, compared to state-of-the-art designs, the proposed inverter and 3-to-8 decoder reduced average power consumption by 55.2% and 46.5%, respectively. The proposed design is highly suitable for low-cost, low-power applications in TFT based technologies, including displays and flexible electronics.

Chapter 4

Low-Power DFF and SRAM cell with Unipolar TFTs on Flexible Substrate

4.1 Introduction

With the growing need for displays, IoT devices, augmented reality/virtual reality applications, on-body medical equipment, and flexible electronics, there is increasing interest in TFTs due to their low-cost and large-scale fabrication capabilities [3, 97]. As discussed in previous chapters, unlike single-crystalline CMOS processes, low-thermal-budget TFTs are generally unipolar in nature [98]. Various efforts have been made to address this issue by enhancing fabrication techniques to introduce complementary transistors [99], however, these approaches have not yielded significant advantages. Therefore, the realization of circuits using TFTs has been challenging.

For instance, one of the major applications of TFTs is displays, where in practice, only the pixel array is realized using TFTs, while the control circuits and driver circuits are realized using off-panel CMOS circuits [13, 26]. This, in turn, requires a large number of bonding pads between the CMOS circuits and the TFT pixel array to drive the row line and column line. This method is more challenging for flexible displays due to the rigidity of current CMOS ICs.

As TFT backplanes are becoming larger and more complex, SRAM memory or DFF integrated on the backplane can be exploited for a variety of reasons. The pixel compensation information can be stored on the backplane itself. Additionally, using SRAM or DFF on the TFT backplane can reduce the energy required to transfer frequently accessed data

from CMOS circuits. Furthermore, in display applications with low refresh rates, SRAM based pixels can be exploited for power saving by retaining image data without requiring constant refresh cycles[100, 101]. Beyond displays, TFT based SRAMs can also be used in building smart sensors, edge computing based wearables, and temporary data storage in smart biomedical and implantable devices [3, 9, 10, 11].

However, implementing an SRAM cell with unipolar TFTs presents a challenge due to high static power consumption caused by direct-path current [65, 66]. Similarly, designing a DFF using unipolar TFT technology suffers from limited output swing and excessive direct-path current. While researchers have proposed various solutions to address the issue of limited output swing [61, 62, 63, 64], the problem of high direct-path current remains unresolved.

In this chapter, we present the design of low-power SRAM and DFF circuits using only n-type TFTs. As a proof of concept, we demonstrate a DFF and an SRAM cell on both glass and flexible substrates, utilizing low thermal budget a-Si:H TFTs. We have used a-Si:H TFTs, but the designs can be implemented using other technologies such as transition metal oxides. The proposed SRAM cell achieves $\sim 56\times$ lower static power consumption compared to a standard 6T SRAM cell. The measurement result shows that compared to DFF using conventional logic gates, the average total power consumption is reduced by 79.8%. Additionally, we investigate the impact of substrate bending on circuit robustness, a topic that remains largely unexplored. Furthermore, existing TFT device models do not account for bending-induced variations, underscoring the need for more accurate modeling. This study enhances the understanding of these effects, contributing to the development of improved models and the advancement of flexible electronics design.

This chapter is organized as follows: In the following Section 4.2, we review existing DFF and SRAM cell designs. In Section 4.3, we discuss the proposed low static-power DFF and SRAM cell design. Section 4.4 presents the simulation result of the proposed designs, and its comparative analysis with conventional and state-of-the-art designs. Section 4.5 discusses the measurement results of the proposed design. Finally, we conclude this chapter in Section 4.6.

4.2 Overview of Existing DFF and SRAM Designs

4.2.1 State-of-the-art DFFs

To understand the problem associated with conventional DFFs, we examine the pass-gate design, shown in Figure 4.1(a) composed of 5 inverters. As discussed in Chapters 2 and 3,

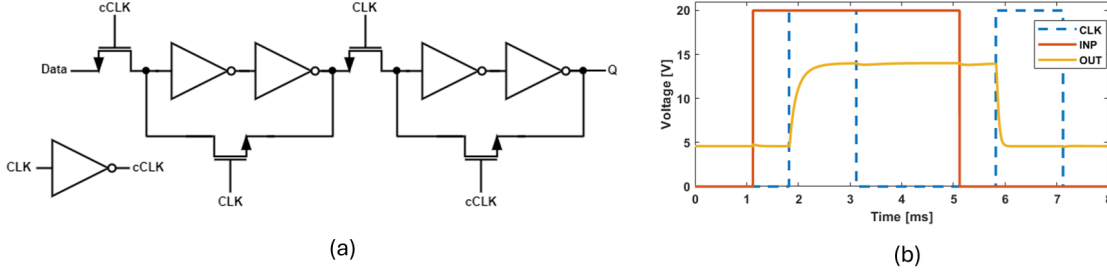


Figure 4.1: (a) Conventional 2T INV based DFF, and (b) its timing diagram. The output swing is limited in this design.

a conventional inverter is composed of a diode-configured pull-up TFT T0 and a pull-down TFT T1, shown in Figure 2.3(a). This design has a major drawback of limited output swing and suffers high direct path current when the input is ‘1’, leading to high power consumption. The limited output swing of the DFF using a conventional inverter can be clearly seen in Figure 4.1(b). It should also be noted that, depending upon the ‘data’ value, the input of the two inverters, one in the master latch and one in the slave latch, will always be ‘1’. This implies that two of the inverters always consume high direct path current, resulting in high power consumption in the conventional DFF design.

As discussed in Section 2.7, several researchers have explored different DFF designs using pseudo-CMOS logic to improve performance. Xu *et al.* implemented a DFF with pseudo-CMOS NOR gates but faced challenges with additional bias voltage and high direct path current [61]. Jo *et al.* addressed area reduction using top and bottom gate structures but did not resolve power consumption issues [62]. Zhan *et al.* introduced an internal feedback-based DFF with bootstrapped NOR gates to minimize direct path current, though some leakage persisted [63]. Tiwari *et al.* proposed a compact DFF using 18 TFTs and a capacitor, achieving full output swing and reduced area but suffering from high power consumption and data stability concerns due to leakage paths [64].

4.2.2 Recent Advances in SRAMs with unipolar TFTs

Similar to DFFs, direct path current is a major issue in unipolar TFT based 6T SRAM cells, resulting in high static power consumption, as discussed in Section 2.7. Since the SRAM cell consists of two back-to-back inverters, one inverter’s input is always ‘1’ regardless of the stored data, leading to continuous direct path current.

Researchers have explored various SRAM designs using IGZO and organic TFTs to

enhance performance. A 6T **SRAM** cell on a flexible substrate demonstrated stability under tensile strain but suffered from direct path current issues depending on stored data [65]. Roose *et al.* implemented a 128b **IGZO TFT SRAM** with back-gated pull-down and passgate **TFTs**, improving noise margins and reducing direct path current [66]. Other designs include a 6T **SRAM** with single-gated p-type **OTFTs** [67] and a 5T **SRAM** using back-gated organic **TFTs**, which reduced area and bitline count while incorporating an extra voltage supply to mitigate direct path current [68]. Despite these efforts, direct path current remains a concern, and additional voltage sources increase overall power consumption.

Due to the persistent direct path current in unipolar **TFT** based **SRAM**, its adoption in **TFT** applications is limited. As a result, a soft ribbon cable is often used to transfer data to and from off-chip **CMOS** based **SRAM**, which not only increases power dissipation but also increases the risk of failure and introduces additional latency. Thus, addressing the direct path current issue in unipolar **TFT** based **SRAM** cells is essential for enhancing power efficiency, reliability, and overall system performance.

4.3 Proposed designs

4.3.1 Low-Power DFF Design

A schematic of the master-slave **DFF**, using the half-latch 6T inverters (discussed in Section 3.3), is illustrated in Figure 4.2(a) where pass transistors facilitate latching of the data in master and slave latches at the appropriate clock edges. The design requires a clock signal, CLK, and a complementary clock signal, cCLK. A 5T inverter, proposed by Qing Li *et al.*, is used to generate cCLK signal [26]. The cCLK signal boosts the internal nodes of the 6T inverters in the master latch, while the CLK signal boosts the internal nodes of the 6T inverters in the slave latch. The simulated waveform is shown in Figure 4.2(b). The 6T inverter design minimizes the direct path between V_{DD} and V_{SS} , leading to a significant reduction in the static power consumption of the proposed **DFF**. This reduction is evident in the current profile shown in Figure 4.2(b), where the proposed **DFF** exhibits considerably lower current consumption compared to other designs. Additionally, Figure 4.2(b) demonstrates that the proposed **DFF** achieves a full output swing.

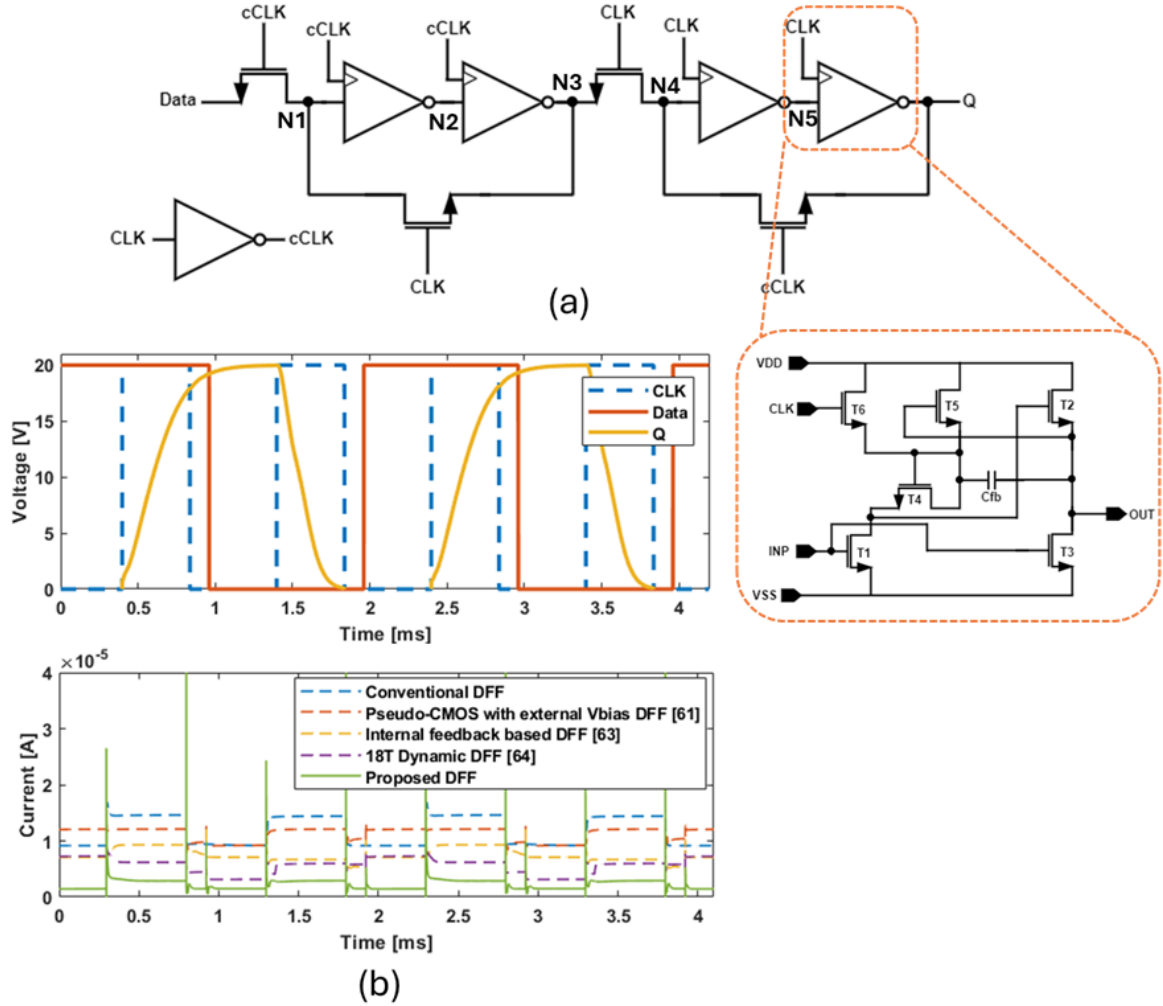


Figure 4.2: (a) Proposed DFF using half-latch 6T inverter gates, and (b) its simulated waveform. The current consumption in the proposed design, shown by solid lines, is reduced compared to other designs, shown by dotted lines, owing to minimized direct path current.

4.3.2 Low-Power SRAM cell

The proposed 10T [SRAM](#) cell is illustrated in Figure 4.3(a). In this design, [TFTs](#) T10 and T11 function as pass gates, while the cross-coupled inverters are formed by [TFTs](#) T12:T15 and T16:T19. The inverter configuration in this [SRAM](#) cell is based on the proposed 6T inverter design but omits the feedback capacitor, diode-configured [TFT](#) and clock-

controlled TFT. These modifications are made because full output swing is not required in the SRAM cell, as it does not directly drive other circuits, eliminating the need for a feedback capacitor and diode configured TFT. Additionally, the clock-controlled TFT is unnecessary for writing new data, since the differential write mechanism inherently provides a temporary boost to the internal node during write operations. The write and read operations are depicted in Figure 4.3(b).

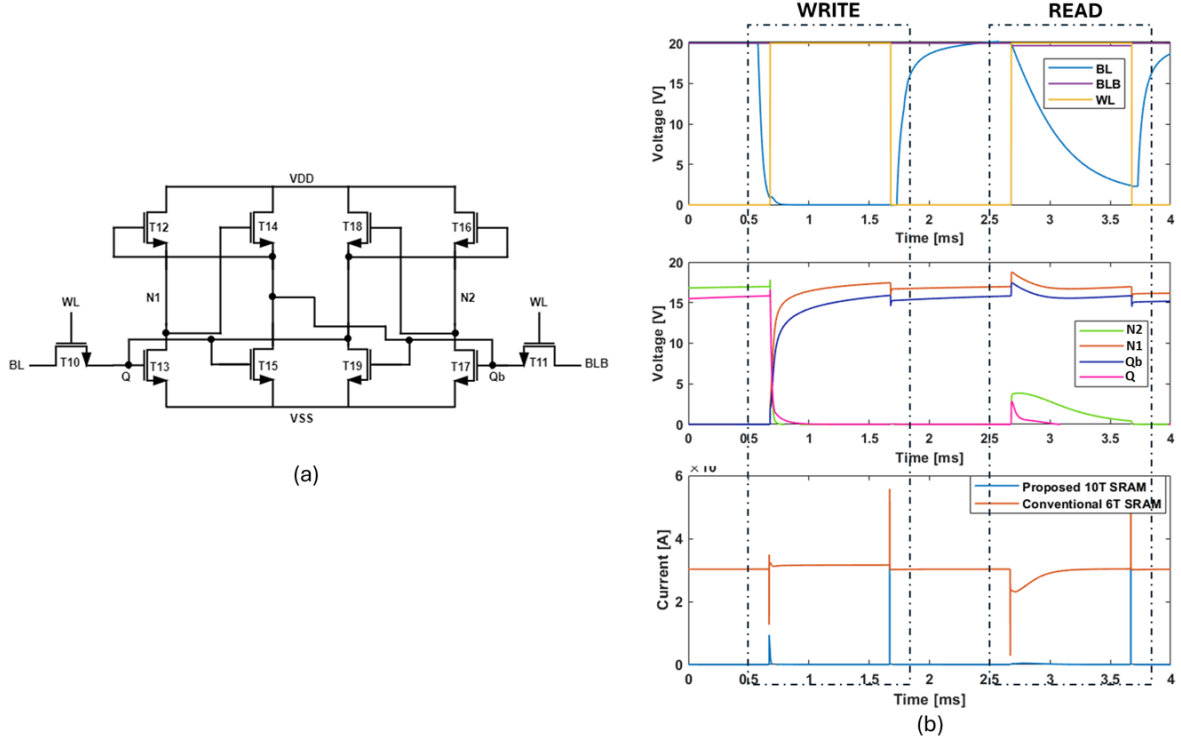


Figure 4.3: (a) Proposed 10T SRAM cell with unipolar TFT, and (b) its timing diagram. The current consumption in the proposed design is reduced compared to conventional 6T SRAM, owing to minimized direct path current.

To write a ‘0’ at node Q, the bitlines BL and BLB are set to V_{SS} and V_{DD} , respectively. The wordline WL is then activated, enabling T10 and T11. With BL at VSS, T13 and T15 turn off, while T11 charges node Qb to $V_{DD} - V_T$, turning on T12. This, in turn, activates T14, ensuring that $V_{DD} - V_T$ is maintained at node Qb. Since node Q stores ‘0’, T16 and T18 remain off, preventing any direct path current. Similarly, when writing a ‘1’ at node Q, BL and BLB are set to V_{DD} and V_{SS} , respectively, and the write operation

follows the same process. In this case, T12 and T14 are fully turned off, ensuring that no direct current path exists in the static state.

For the read operation, the bitlines BL and BLB are precharged to V_{DD} , and the WL is activated, turning on T10 and T11. If data stored at Q is '0', BL is pulled toward V_{SS} ; if data stored at Q is '1', BLB is pulled toward V_{SS} . A sense amplifier then detects the voltage difference between the bit-lines and determines the stored data in the [SRAM](#) cell. As illustrated in the current profile in Figure 4.3(b), the proposed 10T [SRAM](#) design significantly reduces current consumption compared to conventional 6T [SRAM](#), primarily due to the reduction of direct path current.

4.4 Simulation Results

In this section, we analyze the proposed designs and compare them with conventional and state-of-the-art approaches using the simulation model discussed in Section 3.4.1.

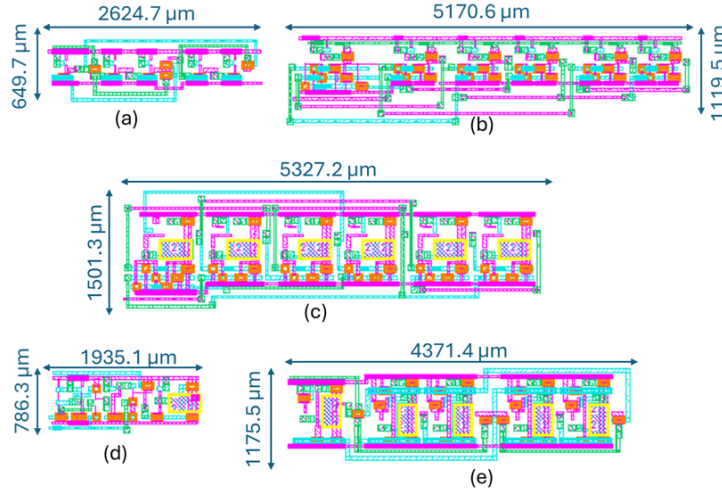


Figure 4.4: Layout of (a) Conventional DFF, (b) Pseudo-CMOS with bias voltage DFF [61], (c) Internal Feedback based DFF [63], (d) 18T dynamic DFF [64], and (e) Proposed DFF.

4.4.1 Simulation-Based Analysis of DFF Power and Performance

Table 4.1 presents a simulation-based comparative analysis of various state-of-the-art and proposed DFF designs using unipolar TFTs. Color code red represents the drawback of the designs, while green represents desirable quality. All DFFs were evaluated at a clock frequency of 1 kHz , with a relaxed setup time and hold time of 500 μs .

Table 4.1: Comparative analysis based on simulation of conv. DFF, Pseudo-CMOS logic with external bias voltage based DFF [61], internal feedback based DFF [63], 18T DFF [64] and prop. DFF.

	Conv. DFF	Pseudo- CMOS with bias vol. DFF [61]	Internal feedback based DFF [63]	18T DFF [64]	Prop. DFF
Full Swing	No	Yes	Yes	Yes	Yes
Additional supply voltage	No	Yes	Yes	No	No
# TFTs	14	38	38	18	33
Area (μm^2)	1.7	5.8	8.0	1.5	5.1
Static/Dynamic Topology	Static	Static	Static	Dynamic	Static
Average Total Power (μW)	226.9	262.9	147.2	111.8	42.1
Average Static Power (μW)	215.7	257.8	138.5	109.3	39.2
Minimum required setup time (μs)	10.3	2.1	2.0	30.1	72.8
Clk-to-Q delay (μs)	91.3	107.5	147.4	150.8	196.7
D-to-Q delay (μs)	101.6	109.6	149.4	180.9	269.5
PDP (nJ)	23.1	28.8	22.0	20.2	11.3
Minimum required hold time (μs)	0	25.1	15.3	113.6	0

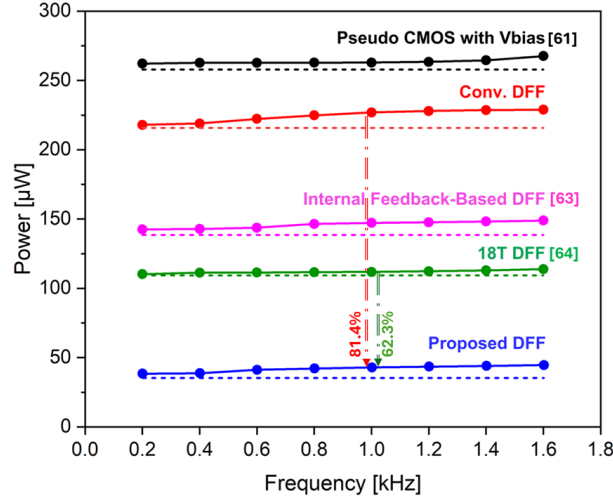


Figure 4.5: Power consumption of DFFs with change in clock frequency. The solid line shows total power consumption, and the dotted line shows static power consumption. The static power is comparable to the total power in all the designs because of the direct path current.

It can be clearly seen that the total power consumed by the proposed DFF is significantly lower than that of the conventional logic gate based DFF and other state-of-the-art DFF designs. Compared to conventional and 18T [64] DFF, the proposed DFF reduces power consumption by 81.4% and 62.3%, respectively. This is because the use of the 6T inverter logic gates eliminates the direct path current between V_{DD} and V_{SS} . However, this result comes at the cost of increased setup time and clock-to-Q delay. Compared to the 18T DFF, the clk-to-Q and D-to-Q delay (Setup time + clk-to-Q delay) increased by 30.4% and 48.9%, respectively. It can be seen that the PDP (Total Power $\times$ D-to-Q delay) is decreased by at least 44% compared to all other designs, for the given technology. It should be noted that conventional 2T based passgate DFF design consumes less power compared to state-of-the-art design in [61] because of the lower number of logic gates in passgate DFF architecture, as well as the higher bias voltage (23 V) used in pseudo-CMOS than the nominal voltage (20 V) in the conventional design. The area of the proposed design is also reduced compared to other static DFF designs proposed in [61, 63]. The layouts of all DFF designs are shown in Figure 4.4.

Figure 4.5 shows the total power consumption of the DFFs w.r.t. change in clock frequency. It can be observed that the power consumption of the TFT based DFF varies little with clock frequency. This is because the average static power is comparable to

the total power consumption for all DFF designs, as shown in Table 4.1. This implies that the dynamic power consumption is small compared to static power for unipolar TFT technology because of direct path current. Notably, the proposed DFF design exhibits the lowest power consumption across all frequencies when compared to other existing designs using the given a-Si:H TFT technology.

4.4.2 SRAM Stability and Power Analysis

To determine stability of SRAMs, static noise margin (SNM) is used as a metric. SNM in SRAM refers to the maximum amount of noise voltage that can be tolerated at a storage node without flipping the stored bit.

There are two main types of SNM commonly used for characterizing SRAM cells: read static noise margins (RSNM) and write static noise margins (WSNM). RSNM quantifies the stability of the cell during a read operation when the bitline is connected to the internal storage node via the access transistor. It is determined by the largest square that can fit within the voltage transfer curve of the SRAM cell during the read cycle. A degraded RSNM can lead to read-disturb failures, where the stored data is unintentionally flipped. In contrast, WSNM measures how easily a new value can be written into the cell; it represents the minimum voltage required to flip the internal node during a write operation. It is determined by the largest square that fits within the voltage transfer curve during the write cycle. Figure 4.6-4.7 illustrates the RSNM and WSNM of the conventional and proposed SRAM cells, respectively.

It is evident that the proposed SRAM cells exhibit improved noise margins compared to conventional designs. In traditional SRAM cells, during a read operation, the pull-down TFT must compete with both the passgate TFT and the always-on pull-up TFT, which limits the cell's ability to maintain its state and degrades the read stability. In contrast, the proposed design disables the pull-up circuit during read access, thereby reducing contention and significantly enhancing the RSNM. Similarly, during write operation, which is performed by passgate TFT discharging node with data 1, the contention is primarily between the passgate and the pull-up TFT. Since the pull-up TFT in conventional cells remains partially on, it resists the write operation, resulting in poor WSNM. By effectively turning off the pull-up path during write access, the proposed design minimizes this contention and improves writability.

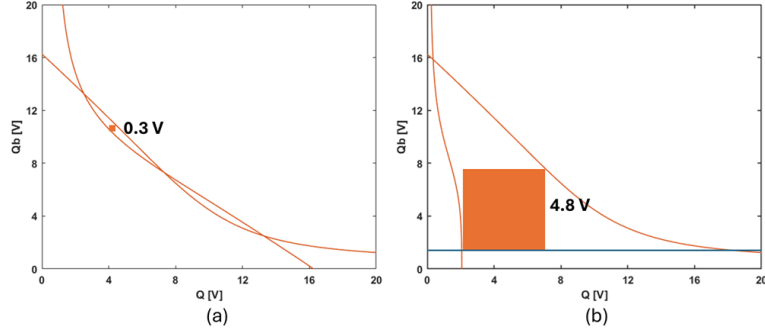


Figure 4.6: (a) Read SNM and (b) Write SNM for a conventional 6T SRAM cell. The largest square that fits in the transfer curve during the operation determines the noise tolerance of the cell.

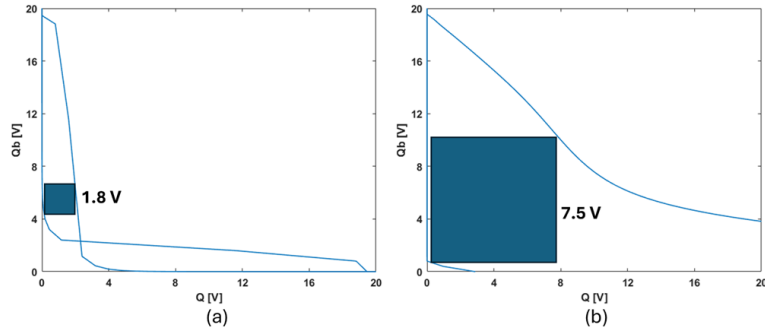


Figure 4.7: (a) Read SNM and (b) Write SNM for a proposed 10T SRAM cell. The largest square that fits in the transfer curve during the operation determines the noise tolerance of the cell.

Simulations show that conventional 6T **SRAM** consumes $3.02 \mu A$, $3.47 \mu A$, and $3.64 \mu A$ currents under static, read, and write conditions, respectively. In contrast, the proposed 10T **SRAM** significantly reduces power consumption, drawing $0.95 nA$, $3.64 nA$, and $3.51 nA$ currents under the same respective conditions. The stark difference can also be understood from the current profile of the proposed inverter design and the conventional 2T inverter design in Figure 3.4(c) and Figure 3.2, respectively, when the input is '1'. This significant reduction is achieved because the proposed designs use feedback from internal nodes Q and Qb to cut off the direct path current, drastically reducing the static current. The read/write power of the 10T **SRAM** cell is also reduced due to feedback from Q and Qb.

4.5 Measurement results

To validate the effectiveness of the design, we also fabricated the proposed and conventional DFFs on glass and flexible substrates. A custom test bench, discussed in Section 3.5.1 was used to assess the behavior of the DFFs and SRAMs.

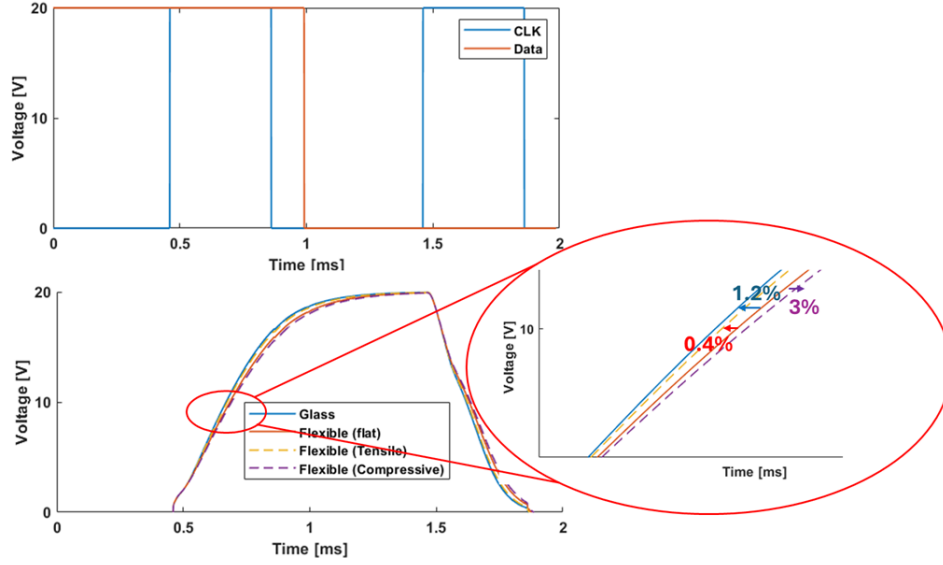


Figure 4.8: Measured input-output waveform of proposed DFF under different conditions. The proposed design shows robust behavior and achieves full output swing under various conditions.

4.5.1 DFF Measurement Results

Figure 4.8 shows the measured oscilloscope waveform of the proposed DFF design on a glass substrate and flexible substrate under flat, tensile, and compressive strain conditions. The results demonstrate that the proposed designs achieve full output swing in all scenarios. These results are tabulated in Table 4.2. The clk-to-Q delay on the glass substrate was observed to be 207.4 μs , while on the flexible substrate, it was observed to be 209.9 μs , 209.1 μs , and 216.5 μs under flat, tensile, and compressive conditions, respectively.

Table 4.2: Power consumption measurements for the conventional DFF and proposed DFF.

	Power Consumption (μ W)				
Substrate	Glass	Flexible			Average
Condition	-	Flat	Tensile	Compressive	
Conv. DFF	233.1	228.1	229.7	227.6	229.6
Prop. DFF	47.1	46.2	46.7	45.6	46.4

The results show that the DFF on the glass substrate exhibited higher power consumption and smaller clk-to-q delay in comparison to the DFF on the flexible substrate. This can be attributed to the rigidity and thermal stability of the glass, which results in fewer defects during the deposition of the TFT layers, leading to higher carrier mobility [92]. In contrast, flexible substrates may experience slight deformations, thermal expansion, or shrinkage during deposition, introducing irregularities in the amorphous silicon (a-Si:H) layer. These irregularities can cause atomic misalignment and structural imperfections, acting as traps or scattering centers that hinder carrier movement, thereby lowering carrier mobility. It was observed that on flexible substrates, tensile strain slightly increases TFT carrier mobility, while compressive strain causes a slight decrease. This aligns with the defect creation model, which suggests that tensile stress stretches the a-Si:H layer, relieving internal tension, and reducing defect states [16]. Fewer defects allow charge carriers to move more freely, enhancing mobility. In contrast, compressive stress compacts the silicon network, increasing defects that trap carriers and reduce mobility.

Figure 4.9 shows the measured and simulated power consumption of the conventional and proposed DFF designs with the change in the supply voltage. At a nominal voltage of 20 V and clock frequency of 1 kHz, the proposed DFF design uses 79.8% less power w.r.t. the conventional DFF. The trend remained the same when the supply voltage was reduced. It was also observed that the proposed design was able to function properly at lower voltage compared to the conventional DFF because of its improved swing at internal nodes. As shown in Figure 4.10, the measured and simulated results are in close agreement, validating the simulation results. The measured power is approximately 2% more than the simulated power, which comes from the measurement setup and the parasitic pad.

Table 4.3 compares all the reported DFFs. We used a-Si:H technology for fabrication, which is widely used in industries such as displays. However, the proposed design can be used for other TFT technologies as well. It can be seen that, although the technology used for the proposed DFF operates at 20 V, the power consumption is significantly less. The design operates at a lower frequency, this is partly also because of the lower carrier mobility of a-Si:H and increased channel length used for fabrication compared to other

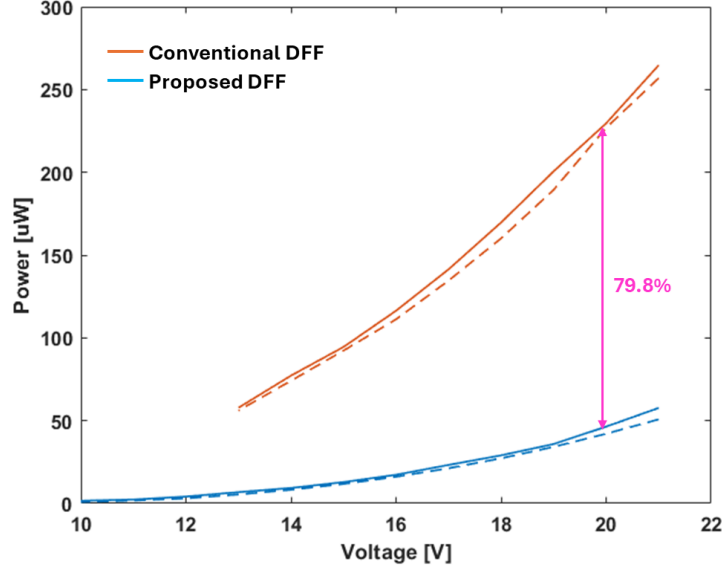


Figure 4.9: Power consumption with change in voltage for conventional and proposed DFFs. The solid line indicates measurement results, while the dotted line indicates simulated results.

reported designs.

The proposed DFF shows promising results for the use of unipolar TFTs for low-power applications. In future work, our aim is to decrease the delay without impacting power consumption. One simple way to achieve this is to modify the passgate DFF and connect the slave input to node N2, instead of N3 in Figure 4.2(a) and use N5 as the output terminal.

4.5.2 SRAM Measurement Results

Figure 4.10 shows the oscilloscope waveform of the proposed 10T SRAM cell, demonstrating a successful write operation. Since this is a single-bit SRAM implementation, the read operation is performed directly from the node Q of the SRAM cell. Table 4.4 presents a comparative analysis of static current measurements for both conventional and proposed SRAM cells on glass and flexible substrates under various bending conditions. The results show that the proposed 10T SRAM cell achieves a $\sim 56\times$ reduction in average static current, primarily due to the elimination of direct path current in its design. However, this comes with an area penalty of 52.4%. The current consumption through the proposed 10T

Table 4.3: Comparison of various reported state-of-the-art DFFs

	[61]	[62]	[63]	[64]	This work
Technology	ITO-stabalized Zno	IGZO	IZO	IGZO	a-Si:H
Full swing	Yes	Yes	Yes	Yes	Yes
VDD	10	6	4.5	4	20
Carrier Mobility ($cm^2/V s$)	17.4	6.34	34	-	1.05
Channel length (μm)	10	5	10	4	20
Total Power (μW)	-	-	57.9	80	46.4
Frequency (kHz)	5	-	202	20	1
Substrate	Glass	Flexible	Glass	Flexible	Glass, Flexible

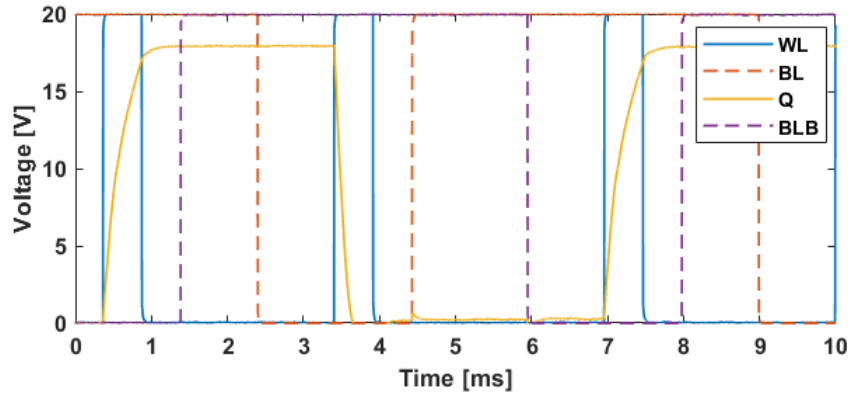


Figure 4.10: Measured oscilloscope waveform of proposed 10T SRAM.

Table 4.4: Measurement based comparative analysis of proposed and conventional SRAM memory cell.

	Static Current (μA)				
	Glass	Flexible			Average
		Flat	Tensile	Compressive	
Conventional 6T SRAM	3.74	3.44	3.66	3.23	3.52
Proposed 10T SRAM	0.07	0.06	0.07	0.05	0.06

Table 4.5: Comparison of reported works on SRAMs.

	[65]	[66]	[67]	[68]	This Work
Technology	IGZO	IGZO	OFET	OFET	a-Si:H
# TFTs/SRAM	6	6	5	5	10
VDD used	5	15	-40	40, -40	20
Static Current per SRAM (μA)	192	3.6	-	3.0	0.06
Memory size realized	1 bit	128 bits	16 bits	144 bits	1 bit

SRAM during read and write operation under the flat condition on a flexible substrate was observed to be $0.12 \mu\text{A}$ and $0.11 \mu\text{A}$, respectively. The discrepancy between measured and simulated current consumption can be attributed to factors such as ambient light exposure, variations in a-Si:H TFT characteristics, and additional power consumption from the probe and measurement setup. These factors predominantly affect the off-state current, which is the primary source of static current in the 10T SRAM cell, rather than the on-state current (direct path current), which dominates the static current consumption in the 6T SRAM cell.

Table 4.5 presents a comparison of various reported SRAM circuit designs utilizing unipolar TFT technology. The results clearly demonstrate that the proposed SRAM cell achieves a significant reduction in static power consumption by eliminating direct path current, outperforming previously reported designs. However, this improvement comes at the cost of increased area due to the higher number of TFTs per memory cell. Nevertheless, unlike in silicon technology, where chip real estate is highly constrained, the lower integration density of flexible large-area electronics mitigates this drawback, making the

larger **SRAM** footprint less of a concern in such applications. In the future, our aim is to integrate a complete memory array with a peripheral control circuit on a flexible substrate.

4.6 Conclusion

TFTs offer a cost-effective approach for fabricating large-area electronic circuits. However, due to their fundamental differences from conventional **CMOS** technology and the limitations of unipolar transistors, designing large-scale gates is challenging, particularly because of limited output swing and high static power consumption. To address these challenges, we introduced a **DFF** design that demonstrated a reduction of at least 44% in **PDP** compared to existing designs for a given technology. Furthermore, a 10T **SRAM** cell was proposed based on the same inverter design concept. The proposed designs were fabricated on both glass and flexible substrates, and the effect of bending was analyzed. Measurement results for the proposed **DFF** design showed a 79.8% reduction in total power consumption compared to the conventional **DFF** design, showcasing the efficiency of the proposed approach. The proposed 10T **SRAM** cell reduces static power consumption by $\sim 56\times$ compared to the conventional approach. These advancements make the proposed design highly suitable for low-cost, low-power applications in **TFT** technologies, such as displays and flexible electronics.

Chapter 5

Conclusion

5.1 Thesis Contribution

In this thesis, we presented circuit designs based on flexible amorphous [TFTs](#) to improve power efficiency and address challenges related to direct path current. Our work introduced a novel half-latch based logic gate architecture, which significantly reduced total power consumption by 55.2% compared to state-of-the-art designs. This approach effectively mitigates direct path current, a factor that had not been previously explored in depth by researchers in this domain. Additionally, we implemented a 3-to-8 decoder as a demonstration of multi-stage logic integration. The proposed decoder design exhibited a 46.5% reduction in power consumption compared to the state-of-the-art bootstrapped design, further highlighting the efficiency of our approach.

Furthermore, we developed a DFF design, using the proposed half-latch logic inverter, that demonstrated a 79.8% reduction in total power consumption compared to conventional [DFF](#) architectures. Additionally, we proposed an [SRAM](#) cell design that reduced static current by $\sim 56\times$ in comparison to the conventional 6T [SRAM](#) cell. These advancements contribute to enhancing the energy efficiency of flexible [TFT](#) based circuits, which is crucial for the development of low-power and sustainable electronic applications.

Beyond circuit design improvements, we also investigated the effects of mechanical bending on these circuits. We observed that the compressive strain decreased the carrier mobility, leading to a decrease in power consumption and speed. On the other hand, tensile strain increased the carrier mobility, leading to an increase in power consumption and speed. Notably, these effects were more pronounced when bending occurred in the

direction parallel to the channel length. To mitigate the impact of bending, TFT layouts should be designed such that the bending direction aligns parallel to the channel length. Additionally, we observed that carrier mobility was slightly higher on glass substrates compared to flexible substrates, primarily due to defect formation caused by thermal expansion and contraction during deposition on flexible substrates. These findings provide valuable insights into the reliability and performance variations of TFT circuits under mechanical strain, enhancing the understanding of flexible electronics and establishing a foundation for future research in this field.

Overall, this thesis contributes valuable knowledge to the field of flexible electronics and offers a promising direction for further advancements in low-power circuit design. By addressing critical power consumption challenges and investigating the effects of bending, this work lays the foundation for future research and development in flexible electronic systems. As flexible electronics continue to evolve, the methodologies and design strategies presented in this thesis will play an important role in shaping the next generation of power-efficient, bendable electronic devices.

5.2 Future Research Direction

The findings of this research highlight the potential of novel design techniques in enhancing the reliability and power efficiency of flexible unipolar TFT circuits. Building on this foundation, our future work will focus on the following key areas:

1. Model Optimization for Bending Effects – To further understand the impact of mechanical strain on flexible TFT circuits, we aim to refine our existing models to incorporate the effects of bending. This includes designing and testing various TFT architectures under different bending radii to quantify variations in electrical characteristics. By systematically analyzing the relationship between bending radius and current fluctuations, we can develop more robust and adaptive circuit designs.

2. Development of Low-Power Dual-Edge and Dynamic DFFs with Scan Chains – To enhance circuit efficiency, we are working on designing low-power dual-edge and dynamic glsdfs, as well as implementing scan chains. These optimizations will improve throughput while maintaining minimal power consumption, making them ideal for energy-efficient flexible electronic applications.

3. Large-Scale Integration and Bit-Serial Arithmetic Logic Unit (ALU) for Flexible Microprocessors – Future research will focus on optimizing the proposed designs for large-scale

integration, with an emphasis on implementing a bit-serial [ALU](#). This will serve as a foundational component for the development of low-power, low-cost flexible microprocessors, further advancing the practical application of [TFT](#) based computing systems.

4. Scalable Memory Design and Periphery Circuits – While our current work has focused on a 1-bit [SRAM](#) memory cell, we plan to extend this research by developing larger memory arrays. This includes the integration of essential peripheral circuits such as decoders and sense amplifiers, enabling the realization of low-power, high-density memory solutions on flexible substrates.

By addressing these areas, we aim to push the boundaries of flexible electronics, paving the way for more efficient, scalable, and commercially viable [TFT](#) based computing and storage solutions.

5.3 Contributions

5.3.1 Journal articles

- S. Ranjan, S. Kapar, C. -H. Lee, W. S. Wong and M. Sachdev, "Flexible Low-Power Digital Circuits With Unipolar Amorphous Silicon Thin-Film Transistors," in IEEE Journal on Flexible Electronics, doi: 10.1109/JFLEX.2025.3525598.
- S. Ranjan, S. Kapar, C. -H. Lee, W. S. Wong and M. Sachdev, "A Low Static-Power D Flip-Flop with Unipolar Thin Film Transistors on a Flexible Substrate," in IEEE Journal of the Electron Device Society, doi: 10.1109/JEDS.2025.3562575.
- S. Ranjan, S. Kapar, C. -H. Lee, W. S. Wong and M. Sachdev, "Realization of Low-Power Digital Circuits with Unipolar TFTs on Flexible Substrate," in IEEE Journal on Flexible Electronics, doi: 10.1109/JFLEX.2025.3564228.
- S. Kapar, S. Ranjan, C. -H. Lee, W. S. Wong and M. Sachdev, "A Flexible Decoder with Charge-Sharing Feature for TFT Backplanes," in Journal of the Society for Information Display (Submitted).

5.3.2 Conference publications

- S. Ranjan, S. Kapar, C. -H. Lee, W. Wong and M. Sachdev, "Low-Power CMOS-like Digital Circuits on Flexible Substrates," 2024 IEEE International Flexible Electron-

ics Technology Conference (IFETC), Bologna, Italy, 2024, pp. 1-4, doi: 10.1109/IFETC61155.2024.10771859.

- S. Ranjan, S. Kapar, C. -H. Lee, W. Wong and M. Sachdev, "Low-Power D Flip-Flop with Amorphous Thin Film Transistors," 2025 IEEE International Flexible Electronics Technology Conference (IFETC), Vancouver, Canada, 2025. (Submitted)
- S. Ranjan, S. Kapar, C. -H. Lee, W. Wong and M. Sachdev, "A Low-Power Bit-Serial ALU with Unipolar TFTs," 2025 IEEE International Flexible Electronics Technology Conference (IFETC), Vancouver, Canada, 2025. (Submitted)

5.3.3 Patents

- M. Sachdev and S. Ranjan, "Low-Power Electronic Components With Unipolar Thin-Film Transistors," K8956946US (Provisional Patent).

References

- [1] E. Fortunato, P. Barquinha, and R. Martins, “Oxide semiconductor thin-film transistors: a review of recent advances,” *Advanced materials*, vol. 24, no. 22, pp. 2945–2986, 2012.
- [2] K. Nomura, “Recent progress of oxide-tft-based inverter technology,” *Journal of Information Display*, vol. 22, no. 4, pp. 211–229, 2021.
- [3] K. Myny, “The development of flexible integrated circuits based on thin-film transistors,” *Nature electronics*, vol. 1, no. 1, pp. 30–39, 2018.
- [4] J. Sheng, H.-J. Jeong, K.-L. Han, T. Hong, and J.-S. Park, “Review of recent advances in flexible oxide semiconductor thin-film transistors,” *Journal of Information Display*, vol. 18, no. 4, pp. 159–172, 2017.
- [5] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos, and G. Tröster, “Metal oxide semiconductor thin-film transistors for flexible electronics,” *Applied Physics Reviews*, vol. 3, no. 2, 2016.
- [6] M. J. Mirshojaeian Hosseini and R. A. Nawrocki, “A review of the progress of thin-film transistors and their technologies for flexible electronics,” *Micromachines*, vol. 12, no. 6, p. 655, 2021.
- [7] G. Cantarella, J. Costa, T. Meister, K. Ishida, C. Carta, F. Ellinger, P. Lugli, N. Münzenrieder, and L. Petti, “Review of recent trends in flexible metal oxide thin-film transistors for analog applications,” *Flexible and Printed Electronics*, vol. 5, no. 3, p. 033001, 2020.
- [8] A. Tixier-Mita, S. Ihida, B.-D. Ségard, G. A. Cathcart, T. Takahashi, H. Fujita, and H. Toshiyoshi, “Review on thin-film transistor technology, its applications, and possible new applications to biological cells,” *Japanese Journal of Applied Physics*, vol. 55, no. 4S, p. 04EA08, 2016.

- [9] Y. Hu, L.-Q. Guo, C. Huo, M. Dai, T. J. Webster, and J. Ding, “Transparent nano thin-film transistors for medical sensors, oled and display applications,” *International Journal of Nanomedicine*, pp. 3597–3603, 2020.
- [10] A. Kumar, A. K. Goyal, and N. Gupta, “thin-film transistors (tfts) for highly sensitive biosensing applications: a review,” *ECS Journal of Solid State Science and Technology*, vol. 9, no. 11, p. 115022, 2020.
- [11] H. Zhang, Y. Lou, Z. Zhang, Y. Li, F. Rokhan, G. Wang, and J. Zhao, “A fully ltps-tft-based bi-directional biomedical interface circuit for large-area healthcare applications,” *IEEE Journal on Flexible Electronics*, 2025.
- [12] D. Barnes, “5.1: Invited paper: Lcd or oled: Who wins?,” in *SID Symposium Digest of Technical Papers*, vol. 44, pp. 26–27, Wiley Online Library, 2013.
- [13] Q. Li, “Backplane circuit design with amorphous silicon thin-film transistors for flexible displays,” 2020.
- [14] J.-H. Lee, J.-H. Kim, and M.-K. Han, “A new a-si: H tft pixel circuit compensating the threshold voltage shift of a-si: H tft and oled for active matrix oled,” *IEEE electron device letters*, vol. 26, no. 12, pp. 897–899, 2005.
- [15] D. Kim, Y. Kim, S. Lee, M. S. Kang, D. H. Kim, and H. Lee, “High resolution a-igzo tft pixel circuit for compensating threshold voltage shifts and oled degradations,” *IEEE journal of the Electron Devices Society*, vol. 5, no. 5, pp. 372–377, 2017.
- [16] Q. Li, C.-H. Lee, M. Asad, W. S. Wong, and M. Sachdev, “A 6-tft charge-transfer self-compensating pixel circuit for flexible displays,” *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 792–800, 2019.
- [17] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwödiauer, I. Graz, S. Bauer-Gogonea, *et al.*, “An ultra-lightweight design for imperceptible plastic electronics,” *Nature*, vol. 499, no. 7459, pp. 458–463, 2013.
- [18] N. Karaki, T. Nanmoto, H. Ebihara, S. Utsunomiya, S. Inoue, and T. Shimoda, “A flexible 8b asynchronous microprocessor based on low-temperature poly-silicon tft technology,” in *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, pp. 272–598, IEEE, 2005.

- [19] L.-Y. Ma, N. Soin, S. N. Aidit, F. A. M. Rezali, and S. F. W. M. Hatta, “Recent advances in flexible solution-processed thin-film transistors for wearable electronics,” *Materials Science in Semiconductor Processing*, vol. 165, p. 107658, 2023.
- [20] A. A. Alekseeva, G. B. Livshits, A. S. Klimovich, S. A. Romanov, V. A. Kondrashov, A. K. Grebenko, D. V. Krasnikov, and A. G. Nasibulin, “Temporary tattoo transfer of sub-percolating single-walled carbon nanotube films for high-yield thin film transistor arrays,” *Available at SSRN 5082496*.
- [21] J. Barsotti, “Free-standing, ultra-thin and ultra-conformable functional polymeric films applied to organic electronic devices,” 2018.
- [22] K. Myny, A. K. Tripathi, J.-L. van der Steen, and B. Cobb, “Flexible thin-film nfc tags,” *IEEE Communications Magazine*, vol. 53, no. 10, pp. 182–189, 2015.
- [23] K. Myny and S. Steudel, “16.6 flexible thin-film nfc transponder chip exhibiting data rates compatible to iso nfc standards using self-aligned metal-oxide tfts,” in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 298–299, IEEE, 2016.
- [24] P. Z. Wiczorek, K. Starecki, K. Gołofit, M. Radtke, and M. Pilarz, “A thin elastic nfc forum type 1 compatible rfid tag,” *IEEE Journal of Solid-State Circuits*, vol. 59, no. 3, pp. 935–946, 2023.
- [25] E. Ozer, J. Kufel, S. Prakash, A. Raisiardi, O. Kindgren, R. Wong, N. Ng, D. Jausseran, F. Alkhalil, D. Kong, *et al.*, “Bendable non-silicon risc-v microprocessor,” *Nature*, vol. 634, no. 8033, pp. 341–346, 2024.
- [26] Q. Li, C.-H. Lee, M. Asad, W. S. Wong, and M. Sachdev, “Energy-efficient full-swing logic circuits with unipolar tfts on flexible substrates,” *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1949–1958, 2020.
- [27] W.-S. Shin, H.-A. Ahn, J.-S. Na, S.-K. Hong, O.-K. Kwon, J.-H. Lee, J.-G. Um, J. Jang, S.-H. Kim, and J.-S. Lee, “A driving method of pixel circuit using a-igzo tft for suppression of threshold voltage shift in amled displays,” *IEEE Electron Device Letters*, vol. 38, no. 6, pp. 760–762, 2017.
- [28] G. Woo, H. Yoo, and T. Kim, “Hybrid thin-film materials combinations for complementary integration circuit implementation,” *Membranes*, vol. 11, no. 12, p. 931, 2021.

- [29] D. R. Allee, L. T. Clark, B. D. Vogt, R. Shringarpure, S. M. Venugopal, S. G. Uppili, K. Kaftanoglu, H. Shivalingaiah, Z. P. Li, J. R. Fernando, *et al.*, “Circuit-level impact of a-si: H thin-film-transistor degradation effects,” *IEEE Transactions on Electron Devices*, vol. 56, no. 6, pp. 1166–1176, 2009.
- [30] G. W. Shim, W. Hong, J.-H. Cha, J. H. Park, K. J. Lee, and S.-Y. Choi, “Tft channel materials for display applications: From amorphous silicon to transition metal dichalcogenides,” *Advanced Materials*, vol. 32, no. 35, p. 1907166, 2020.
- [31] M.-J. Spijkman, K. Myny, E. C. Smits, P. Heremans, P. W. Blom, and D. M. De Leeuw, “Dual-gate thin-film transistors, integrated circuits and sensors,” *Advanced Materials*, vol. 23, no. 29, pp. 3231–3242, 2011.
- [32] T.-C. Huang, K. Fukuda, C.-M. Lo, Y.-H. Yeh, T. Sekitani, T. Someya, and K.-T. Cheng, “Pseudo-cmos: A design style for low-cost and robust flexible electronics,” *IEEE Transactions on Electron Devices*, vol. 58, no. 1, pp. 141–150, 2010.
- [33] J. Zhao, P. Yu, S. Qiu, Q. Zhao, L. Feng, S. Ogier, W. Tang, J. Fan, W. Liu, Y. Liu, *et al.*, “Universal compact model for thin-film transistors and circuit simulation for low-cost flexible large area electronics,” *IEEE Transactions on Electron Devices*, vol. 64, no. 5, pp. 2030–2037, 2017.
- [34] M. Yang, “Amorphous silicon thin film transistor models and pixel circuits for amoled displays,” 2014.
- [35] X. Cheng, S. Lee, G. Yao, and A. Nathan, “Tft compact modeling,” *Journal of Display Technology*, vol. 12, no. 9, pp. 898–906, 2016.
- [36] N. Lu, W. Jiang, Q. Wu, D. Geng, L. Li, and M. Liu, “A review for compact model of thin-film transistors (tfts),” *Micromachines*, vol. 9, no. 11, p. 599, 2018.
- [37] R. A. Street, “Thin-film transistors,” *Advanced Materials*, vol. 21, no. 20, pp. 2007–2022, 2009.
- [38] G. Fortunato, A. Pecora, and L. Maiolo, “Polysilicon thin-film transistors on polymer substrates,” *Materials Science in Semiconductor Processing*, vol. 15, no. 6, pp. 627–641, 2012.
- [39] B. Kumar, B. K. Kaushik, and Y. S. Negi, “Organic thin film transistors: structures, models, materials, fabrication, and applications: a review,” *Polymer Reviews*, vol. 54, no. 1, pp. 33–111, 2014.

- [40] B. Kumar, B. K. Kaushik, and Y. S. Negi, “Perspectives and challenges for organic thin film transistors: Materials, devices, processes and applications,” *Journal of Materials Science: Materials in Electronics*, vol. 25, pp. 1–30, 2014.
- [41] M. Kuik, G.-J. A. Wetzelaer, H. T. Nicolai, N. I. Craciun, D. M. De Leeuw, and P. W. Blom, “25th anniversary article: charge transport and recombination in polymer light-emitting diodes,” *Advanced Materials*, vol. 26, no. 4, pp. 512–531, 2014.
- [42] J. T. Quinn, J. Zhu, X. Li, J. Wang, and Y. Li, “Recent progress in the development of n-type organic semiconductors for organic field effect transistors,” *Journal of Materials Chemistry C*, vol. 5, no. 34, pp. 8654–8681, 2017.
- [43] D.-M. Sun, C. Liu, W.-C. Ren, and H.-M. Cheng, “A review of carbon nanotube-and graphene-based flexible thin-film transistors,” *Small*, vol. 9, no. 8, pp. 1188–1205, 2013.
- [44] B. Chandra, H. Park, A. Maarouf, G. J. Martyna, and G. S. Tulevski, “Carbon nanotube thin film transistors on flexible substrates,” *Applied Physics Letters*, vol. 99, no. 7, 2011.
- [45] D. Lee, M.-L. Seol, D.-I. Moon, P. Bennett, N. Yoder, J. Humes, J. Bokor, Y.-K. Choi, and S.-J. Choi, “High-performance thin-film transistors produced from highly separated solution-processed carbon nanotubes,” *Applied Physics Letters*, vol. 104, no. 14, 2014.
- [46] S. Kapar, “Low power tft logic implementation on display backplane, using unipolar tfts,” 2024.
- [47] L. S. Valor, *Electronic Transport Properties of Hydrogenated Amorphous Silicon-Germanium Thin Films*. PhD thesis, university of minnesota, 2022.
- [48] T. Belaroussi, D. Rached, W. Rahal, and F. Hamdache, “Sensitivity of a hit c-si solar cell to structural distortions of the hydrogenated amorphous silicon constituting the front face of the device,” 2020.
- [49] D. Geng, K. Wang, L. Li, K. Myny, A. Nathan, J. Jang, Y. Kuo, and M. Liu, “Thin-film transistors for large-area electronics,” *Nature Electronics*, vol. 6, no. 12, pp. 963–972, 2023.
- [50] F. F. Vidor, T. Meyers, and U. Hilleringmann, “Flexible electronics: integration processes for organic and inorganic semiconductor-based thin-film transistors,” *Electronics*, vol. 4, no. 3, pp. 480–506, 2015.

- [51] T. P. Brody, “The thin film transistor—a late flowering bloom,” *IEEE Transactions on Electron Devices*, vol. 31, no. 11, pp. 1614–1628, 1984.
- [52] A. J. Flewitt, “Hydrogenated amorphous silicon thin-film transistors (a-si: H tfts),” *Handbook of Visual Display Technology*, pp. 887–909, 2016.
- [53] T.-H. Hwang, I.-S. Yang, O.-K. Kwon, M.-K. Ryu, C.-W. Byun, C.-S. Hwang, and S.-H. K. Park, “Inverters using only n-type indium gallium zinc oxide thin film transistors for flat panel display applications,” *Japanese Journal of Applied Physics*, vol. 50, no. 3S, p. 03CB06, 2011.
- [54] Y. Chen, D. Geng, T. Lin, M. Mativenga, and J. Jang, “Full-swing clock generating circuits on plastic using a-igzo dual-gate tfts with pseudo-cmos and bootstrapping,” *IEEE Electron Device Letters*, vol. 37, no. 7, pp. 882–885, 2016.
- [55] B. Tiwari, J. Martins, S. Kalla, S. Kaushik, A. Santa, P. G. Bahubalindrani, V. G. Tavares, and P. Barquinha, “A high speed programmable ring oscillator using ingazno thin-film transistors,” in *2018 International Flexible Electronics Technology Conference (IFETC)*, pp. 1–6, IEEE, 2018.
- [56] N. P. Papadopoulos, C.-H. Lee, A. Tari, W. S. Wong, and M. Sachdev, “Low-power bootstrapped rail-to-rail logic gates for thin-film applications,” *Journal of Display Technology*, vol. 12, no. 12, pp. 1539–1546, 2016.
- [57] K. Myny, Y.-C. Lai, N. Papadopoulos, F. De Roose, M. Ameys, M. Willegems, S. Smout, S. Steudel, W. Dehaene, and J. Genoe, “15.2 a flexible iso14443-a compliant 7.5 mw 128b metal-oxide nfc barcode tag with direct clock division circuit from 13.56 mhz carrier,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 258–259, IEEE, 2017.
- [58] K. Myny, E. Van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, “An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 284–291, 2011.
- [59] H. Çeliker, A. Sou, B. Cobb, W. Dehaene, and K. Myny, “Flex6502: a flexible 8b microprocessor in 0.8 μm metal-oxide thin-film transistor technology implemented with a complete digital design flow running complex assembly code,” in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65, pp. 272–274, IEEE, 2022.

- [60] J. Biggs, J. Myers, J. Kufel, E. Ozer, S. Craske, A. Sou, C. Ramsdale, K. Williamson, R. Price, and S. White, “A natively flexible 32-bit arm microprocessor,” *Nature*, vol. 595, no. 7868, pp. 532–536, 2021.
- [61] Y. Xu, S. Deng, Z. Wu, B. Li, Y. Qin, W. Zhong, R. Chen, G. Li, M. Wong, and H. S. Kwok, “The implementation of fundamental digital circuits with ito-stabilized zno tfts for transparent electronics,” *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5395–5399, 2018.
- [62] Y. Jo, J. Kwon, J.-L. van der Steen, A. J. Kronemeijer, and S. Jung, “Programmable a-ingazno gate array with laser-induced forward transfer,” *Flexible and Printed Electronics*, vol. 6, no. 1, p. 015014, 2021.
- [63] F. Zhan, J.-D. Wu, L. Zhou, J.-H. Zou, H. Tao, M. Xu, L. Wang, M. Huang, Y.-R. Liu, W.-J. Wu, *et al.*, “A low-power d flip flop integrated by metal oxide thin film transistors employing internal feedback control,” *Semiconductor Science and Technology*, vol. 33, no. 11, p. 115004, 2018.
- [64] B. Tiwari and P. G. Bahubalindrani, “A compact low-voltage d-type flip flop using oxide tfts and its application in sequential circuits,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 1184–1188, 2022.
- [65] N. Münzenrieder, C. Zysset, T. Kinkeldei, K. Cherenack, and G. Tröster, “A flexible ingazno based 1-bit sram under mechanical strain,” in *2011 Semiconductor Conference Dresden*, pp. 1–4, IEEE, 2011.
- [66] F. De Roose, K. Myny, M. Ameys, J.-L. P. van der Steen, J. Maas, J. de Riet, J. Genoe, and W. Dehaene, “A thin-film, a-igzo, 128b sram and lprom matrix with integrated periphery on flexible foil,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 3095–3103, 2017.
- [67] J. Avila-Niño, E. Patchett, D. Taylor, H. Assender, S. Yeates, Z. Ding, and J. Morrison, “Stable organic static random access memory from a roll-to-roll compatible vacuum evaporation process,” *Organic Electronics*, vol. 31, pp. 77–81, 2016.
- [68] M. Takamiya, T. Sekitani, Y. Kato, H. Kawaguchi, T. Someya, and T. Sakurai, “An organic fet sram with back gate to increase static noise margin and its application to braille sheet display,” *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 93–100, 2006.

- [69] N. Munzenrieder, K. H. Cherenack, and G. Troster, “The effects of mechanical bending and illumination on the performance of flexible igzo tfts,” *IEEE Transactions on Electron Devices*, vol. 58, no. 7, pp. 2041–2048, 2011.
- [70] D. Kim, B. Hwang, J. Park, H. Jeon, B. Bae, H. Lee, and N.-E. Lee, “Mechanical bending of flexible complementary inverters based on organic and oxide thin film transistors,” *Organic electronics*, vol. 13, no. 11, pp. 2401–2405, 2012.
- [71] R. Martins, D. Gaspar, M. J. Mendes, L. Pereira, J. Martins, P. Bahubalindrani, P. Barquinha, and E. Fortunato, “Papertronics: Multigate paper transistor for multifunction applications,” *Applied Materials Today*, vol. 12, pp. 402–414, 2018.
- [72] A. F. Paterson and T. D. Anthopoulos, “Enabling thin-film transistor technologies and the device metrics that matter,” *Nature communications*, vol. 9, no. 1, p. 5264, 2018.
- [73] Y. Liu, H. Zhou, R. Cheng, W. Yu, Y. Huang, and X. Duan, “Highly flexible electronics from scalable vertical thin film transistors,” *Nano letters*, vol. 14, no. 3, pp. 1413–1418, 2014.
- [74] M. Magliulo, M. Y. Mulla, M. Singh, E. Macchia, A. Tiwari, L. Torsi, and K. Manoli, “Printable and flexible electronics: From tfts to bioelectronic devices,” *Journal of Materials Chemistry C*, vol. 3, no. 48, pp. 12347–12363, 2015.
- [75] H. Çeliker, W. Dehaene, and K. Myny, “Multi-project wafers for flexible thin-film electronics by independent foundries,” *Nature*, vol. 629, no. 8011, pp. 335–340, 2024.
- [76] J. R. Pradhan, S. S. Priyadarsini, S. R. Nibgoor, M. Singh, and S. Dasgupta, “Oxide semiconductor based deep-subthreshold operated read-out electronics for all-printed smart sensor patches,” in *Exploration*, p. 20230167, Wiley Online Library, 2024.
- [77] X. Wang, Y. Hu, X. Hu, Q. Zhang, K. Sun, Y. Xiang, *et al.*, “Electronic skin based on plla/tft/pvdf-trfe array for multi-functional tactile sensing and visualized restoring,” *Chemical Engineering Journal*, vol. 434, p. 134735, 2022.
- [78] D. Raiteri, P. van Lieshout, A. van Roermund, and E. Cantatore, “Positive-feedback level shifter logic for large-area electronics,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 524–535, 2014.
- [79] S. Y. Yoon, Y. H. Jang, B. Kim, M. D. Chun, H. N. Cho, N. W. Cho, C. Y. Sohn, S. H. Jo, C.-D. Kim, and I.-J. Chung, “P-172l: Late-news poster: Highly stable

- integrated gate driver circuit using a-si tft with dual pull-down structure,” in *SID Symposium Digest of Technical Papers*, vol. 36, pp. 348–351, Wiley Online Library, 2005.
- [80] G. Fortunato, L. Maiolo, F. Maita, A. Minotti, S. Mirabella, V. Strano, G. Metta, D. Ricci, and A. Pecora, “Ltps tft technology on flexible substrates for sensor applications,” in *2014 21st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)*, pp. 311–314, IEEE, 2014.
 - [81] D. Y. Jeong, Y. Chang, W. G. Yoon, Y. Do, and J. Jang, “Low-temperature polysilicon oxide thin-film transistors with coplanar structure using six photomask steps demonstrating high inverter gain of 264 v v⁻¹,” *Advanced Engineering Materials*, vol. 22, no. 4, p. 1901497, 2020.
 - [82] S. M. S. Faramarzi, N. Papadopoulos, J. Genoe, and K. Myny, “Flexible tft read-out circuit blocks for large area sensor array system integration measuring photovoltaic modules and batteries,” *IEEE Journal on Flexible Electronics*, 2024.
 - [83] A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, M. Chida, T. Kakehi, Y. Ebiko, Y. Sano, and N. Sasaki, “High performance low temperature polycrystalline silicon thin film transistors on non-alkaline glass produced using diode pumped solid state continuous wave laser lateral crystallization,” *Japanese journal of applied physics*, vol. 43, no. 4R, p. 1269, 2004.
 - [84] S. H. Nam, P. J. Jeon, Y. T. Lee, S. R. A. Raza, and S. Im, “Not and nor logic circuits using passivation dielectric involved dual gate in a-ingazno tfts,” *IEEE electron device letters*, vol. 34, no. 12, pp. 1527–1529, 2013.
 - [85] H. Yin, S. Kim, J. Park, I. Song, S.-W. Kim, J. Hur, S. Park, S. Jeon, and C. J. Kim, “High performance low voltage amorphous oxide tft enhancement/depletion inverter through uni-/bi-layer channel hybrid integration,” in *2009 IEEE International Electron Devices Meeting (IEDM)*, pp. 1–4, IEEE, 2009.
 - [86] B. Tiwari, P. G. Bahubalindrani, A. Santos, A. Santa, C. Figueiredo, M. Pereira, R. Martins, E. Fortunato, and P. Barquinha, “Low-voltage high-speed ring oscillator with a-ingazno tfts,” *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 584–588, 2020.
 - [87] T.-C. Huang, K. Fukuda, C.-M. Lo, Y.-H. Yeh, T. Sekitani, T. Someya, and K.-T. Cheng, “Pseudo-cmos: A novel design style for flexible electronics,” in *2010 Design*,

Automation & Test in Europe Conference & Exhibition (DATE 2010), pp. 154–159, IEEE, 2010.

- [88] Y. Qin, G. Li, Y. Xu, R. Chen, S. Deng, W. Zhong, Z. Wu, B. Li, G. Li, F. S. Yeung, *et al.*, “Low-power design for unipolar ito-stabilized zno tft rfid code generator using differential logic decoder,” *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4768–4773, 2019.
- [89] F. De Roose, J. Genoe, W. Dehaene, and K. Myny, “Crossover logic: A low-power topology for unipolar dual-gate thin-film technologies,” *IEEE Solid-State Circuits Letters*, vol. 2, no. 7, pp. 49–52, 2019.
- [90] J.-S. Kim, J.-H. Jang, Y.-D. Kim, J.-W. Byun, K. Han, J.-S. Park, and B.-D. Choi, “Dynamic logic circuits using a-igzo tfts,” *IEEE Transactions on Electron Devices*, vol. 64, no. 10, pp. 4123–4130, 2017.
- [91] C.-H. Lee, N. P. Papadopoulos, M. Sachdev, and W. S. Wong, “Effect of mechanical strain on hydrogenated amorphous silicon thin-film transistors and compensation circuits on flexible substrates,” *IEEE Transactions on Electron Devices*, vol. 64, no. 5, pp. 2016–2021, 2017.
- [92] K. R. Sarma, “Flexible displays: Tft technology: Substrate options and tft processing strategies,” *Handbook of Visual Display Technology*, vol. 2, pp. 897–929, 2012.
- [93] G. Zhang, H. Wu, C. Chen, T. Wang, J. Yue, and C. Liu, “Transparent and flexible capacitors based on nanolaminate,” *Nanoscale Research Letters*, vol. 10, no. 76, pp. 4768–4773, 2015.
- [94] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” *Nature*, vol. 432, no. 432, p. 488–492, 2004.
- [95] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, J. M. Tour, and G. Cho, “All-printed and roll-to-roll-printable 13.56-mhz-operated 1-bit rf tag on plastic foils,” *IEEE Transactions on Electron Devices*, vol. 57, no. 3, pp. 571–580, 2010.
- [96] R. Bollström, J. Bobacka, P. Dolietis, M. Lindén, R. Österbacka, T. Remonen, P. Salminen, J. Sarfraz, D. Tobjörk, S. Viljanen, C.-J. Wikman, C.-E. Wilén, and M. Toivakka, “Roll to roll printed electronics on paper,” 01 2012.

- [97] J. C. Costa, A. Pouryazdan, J. Panidi, F. Spina, T. D. Anthopoulos, M. O. Liedke, C. Schneider, A. Wagner, and N. Münzenrieder, “Flexible igzo tfts and their suitability for space applications,” *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 1182–1190, 2019.
- [98] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, “Amorphous silicon thin film transistor circuit integration for organic led displays on glass and plastic,” *IEEE Journal of solid-state circuits*, vol. 39, no. 9, pp. 1477–1486, 2004.
- [99] J. S. Chang, A. F. Facchetti, and R. Reuss, “A circuits and systems perspective of organic/printed electronics: Review, challenges, and contemporary and emerging design approaches,” *IEEE Journal on emerging and selected topics in circuits and systems*, vol. 7, no. 1, pp. 7–26, 2017.
- [100] J.-K. Cho and M. Jeong, “A low-voltage-driven high-voltage sram pixel circuit for power reduction in a digital micro-display panel,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 5, pp. 1640–1652, 2020.
- [101] J.-K. Cho and M. Jeong, “A low-power digital pixel driving scheme for single-pulse-pwm-based display using and-embedded pixel circuits,” *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 29, no. 11, pp. 3382–3392, 2018.
- [102] Y. Ma, S. Wagner, N. Verma, and J. C. Sturm, “Design and characterization of high quality-factor inductors for wireless systems compatible with flexible large-area electronics,” *IEEE Journal on Flexible Electronics*, 2024.