

A Study on the Impacts of Wide-Bandgap Devices on Turn-to-Turn Insulation Performance in Hairpin Winding for Electric Vehicle Traction Motors

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Electric Vehicles (EVs) are one of the important levers of transportation electrification. However, charging time and limited mileage per charge remain significant barriers to widespread EV adoption. Continuous advancements in EV technology aim to mitigate these challenges. Three major improvements addressing these issues include increasing the operating voltage level, replacing random-wound motors with hairpin winding, and utilizing wide-bandgap (WBG)-based power converters to drive the motors. These advancements, however, raise concerns regarding motor reliability, particularly in the winding insulation system. Therefore, it is crucial to study and characterize the effects of higher voltage levels and WBG device-based drives on hairpin winding insulation.

Turn-to-turn insulation is the most vulnerable point in motor stators. Power electronic converters employ pulse-width modulation (PWM) techniques to generate AC output waveforms, producing pulses with fast (short) rise times, overshoot, high frequency, and variable duty cycles. These PWM-driven systems subject insulation to greater electrical stress than conventional AC-fed machines. The adoption of WBG device-based drives exacerbates this stress due to their inherently fast switching characteristics and high-frequency components. Increased electrical stress may lead to partial discharge (PD) activity, which accelerates insulation degradation. Consequently, evaluating turn-to-turn insulation under WBG device-based drive operation and PD exposure is critical.

This study develops a high-voltage SiC-MOSFET pulse generator to investigate the impact of WBG device-based drives on turn-to-turn insulation. A comprehensive analysis is conducted by examining the effects of pulse rise time, overshoot, frequency, and duty cycle. Three rise times (40 ns, 500 ns, and 800 ns) are considered to assess the influence of fast-switching transients inherent to WBG devices. Overshoot effects are examined using 10% and 20% overshoot pulses, while frequency effects are evaluated at 5 kHz and 10 kHz. Additionally, the impact of duty cycle is studied at 20% and 50%. Since traction motors operate under elevated thermal conditions, this study also evaluates the effect of increased temperature on insulation degradation to more accurately replicate in-service stress conditions.

To assess turn-to-turn insulation performance, back-to-back test samples replicating hairpin winding structures are developed using actual flat wires employed in EV motors. Two wire types, corona-resistant and non-corona-resistant, are evaluated and compared. Experimental tests are designed based on Design of Experiment (DOE) principles, with samples subjected to 24-hour aging under high-

voltage pulses generated by the SiC-MOSFET pulse generator in the presence of PD activity. Insulation performance is assessed before and after aging by measuring partial discharge inception voltage (PDIV) and conducting dielectric frequency response (DFR) analysis. Wire surface temperature is continuously monitored during the aging process, and PD activity is confirmed through the detection of PD electromagnetic wave emissions using a UHF antenna. Furthermore, optical microscopy, atomic force microscopy (AFM), scanning electron microscopy (SEM) images, and EDX analysis are utilized to examine wire coating integrity before and after aging.

Results indicate that corona-resistant wires exhibit superior performance under PD conditions compared to non-corona-resistant wires. Additionally, frequency is identified as the dominant factor influencing PDIV drop, whereas overshoot has the most significant effect on the increase in dissipation factor after aging. Microscopy, AFM, SEM, and EDX analysis reveal clear evidence of PD-induced wire coating damage. The combined impact of thermal and electrical stress is examined, with findings compared to room-temperature test results.

This research provides critical insights into the reliability of turn-to-turn insulation in hairpin-wound EV motors under WBG device-based drive operation, offering valuable guidance for motor reliability improvement in next-generation EV powertrains.

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Dedication

To my beloved parents, wife, and sister.

Table of Contents

List of Figures.....	xii
List of Tables.....	xvii
Chapter 1 Introduction	1
1.1 Transportation Electrification.....	1
1.2 Motor Windings	2
1.3 Power Electronics Drives	3
1.4 Insulation Concerns	4
1.5 Research Motivation.....	6
1.6 Summary	7
Chapter 2 Literature Review.....	9
2.1 Motor Insulation	9
2.1.1 Random-Wound Winding	9
2.1.2 Hairpin Winding.....	12
2.2 Pulse Generators for Motor Insulation Testing	17
2.3 Research Gap.....	20
2.4 Thesis Objectives	21
Chapter 3 Materials and Methods	22
3.1 Sample Preparation.....	22
3.2 Experimental Test Setup.....	25
3.3 High Temperature Tests	26
3.4 Insulation Performance Measurements	27
3.5 SEM Analysis.....	28

3.6 Test Procedures	28
3.6.1 PD Measurement	29
3.6.2 Temperature Measurement	29
3.6.3 Test Voltage and Duration	31
3.6.4 Tests with Failed Samples	31
3.7 Design of Experiments	32
Chapter 4 SiC-MOSFET High-Voltage Pulse Generator for Motor Insulation Testing	33
4.1 Pulse Generating Module	33
4.2 Generator Modular Topology	34
4.3 Control Signals	39
4.4 Gate Driver Circuit	41
4.5 Design and Implementation Considerations	42
4.6 Protection Circuit	43
4.7 Simulation and Experimental Work	44
4.7.1 Simulation Work	45
4.7.2 Experimental Work	51
4.8 Modified Pulse Power Supply for Long-Term Aging	62
4.9 Summary	63
Chapter 5 Results	64
5.1 Rise Time and Overshoot Effects on Corona-Resistant and Non-Corona-Resistant Wires	64
5.1.1 Test Conditions and Voltage Waveform Parameters	65
5.1.2 Measured PDIV Values of the Samples	66
5.1.3 Measured DF Values of the Samples	69
5.1.4 Measured Capacitance Values of the Samples	71

5.1.5 Measured Temperature Values at the Crotch Area of the Samples	73
5.1.6 Optical Microscope and AFM Images from the Surface of the Wires	74
5.1.7 Summary of the CR and NCR Wires' Performance under Variable Rise Time and Overshoot	77
5.2 Effects of Overshoot, Frequency, and Duty Cycle on Corona-Resistant Wires.....	77
5.2.1 Test Conditions and Voltage Waveform Parameters.....	77
5.2.2 Measured PDIV Values of the Samples	79
5.2.3 Measured DF Values of the Samples	80
5.2.4 Measured Temperature Values at the Crotch Area of the Samples.....	82
5.2.5 Optical Microscope, AFM, and SEM Images from the Surface of the Wires	83
5.3 Effects of Thermal and Electrical Stress on Corona-Resistant Wires	86
5.3.1 High Temperature Test.....	87
5.3.2 Combined Thermal and Electrical Stresses	89
Chapter 6 Discussion.....	92
6.1 Rise Time and Overshoot Effects on Enamel Insulation Performance	92
6.1.1 Rise Time Effect on Enamel Insulation Performance	92
6.1.2 Overshoot Effect on Enamel Insulation Performance	93
6.1.3 Pulse Rise Time and Overshoot Effects' Characterization.....	94
6.2 Overshoot, Frequency, and Duty Cycle Effects on Enamel Insulation Performance.....	98
6.2.1 Frequency Effect on Enamel Insulation Performance	98
6.2.2 Duty Cycle Effect on Enamel Insulation Performance.....	99
6.2.3 Pulse Overshoot, Frequency, and Duty Cycle Effects' Characterization	99
6.3 Temperature Effect on Enamel Insulation Performance	105
6.4 Wire Surface Degradation Analysis	107

6.4.1 Optical Analysis of Wire Surface	107
6.4.2 EDX Analysis of Wire Surface Degradation.....	107
Chapter 7 Conclusion and Suggestions for Future Work.....	110
7.1 Summary	110
7.2 Conclusions	111
7.3 Contributions	112
7.4 Suggestions for Future Work.....	113
References	114
Appendix A	125
EDX Analysis Results	125

List of Figures

Fig. 1.1 Conductors in a stator slot: (a) random-wound winding and (b) hairpin-wound winding [11].	3
Fig. 1.2 System overview representing the DC source, drive, cable, and the motor [3].	4
Fig. 2.1 Schematic representation of the structure of hairpin winding [46].	13
Fig. 2.2 Structure of miniaturized test block used in [46].	14
Fig. 2.3 Test specimen to represent the insulation system in the slot area [50].	14
Fig. 2.4 Back-to-back samples used to study turn-to-turn insulation [17].	15
Fig. 3.1 Block diagram representing the overall research methodology.	22
Fig. 3.2 The proposed sample improvements (a) the aluminum holder and (b) the plexiglass holder.	23
Fig. 3.3 The proposed sample improvements: crotch area filled with (a) silicone and (b) resin in the VPI process.	24
Fig. 3.4 The proposed sample (a) the side view of the holder and (b) the front view of the holder.	25
Fig. 3.5 The experimental setup used for aging the back-to-back samples.	26
Fig. 3.6 DFR measurement setup for the un-grounded specimen test.	28
Fig. 3.7 The controlled experiment setup to calibrate and validate the IR camera settings.	30
Fig. 4.1 Pulse generating module.	34
Fig. 4.2 Proposed modular topology.	35
Fig. 4.3 The first mode of operation.	36
Fig. 4.4 The second mode of operation.	37
Fig. 4.5 The third mode of operation.	38
Fig. 4.6 Sequence of control signals for the fastest rise time.	39
Fig. 4.7 Sequence of control signals for variable rise times.	40
Fig. 4.8 Sequence of control signals for multilevel waveform.	41
Fig. 4.9 The gate driver system schematic.	42
Fig. 4.10 The protection circuit schematic.	44
Fig. 4.11 Simulated voltage waveforms: (a) output 3.2 kV pulses, (b) zoomed view of 3.2 kV pulses, (c) output of each module, and (d) voltage across the capacitors.	46
Fig. 4.12 Simulated voltage waveforms across: (a) charging switch and (b) discharging switch.	47
Fig. 4.13 Simulated voltage waveforms across the diodes: (a) D ₁ , (b) D ₂ , (c) D ₃ , (d) D ₄ , and (e) D ₅ .	48
Fig. 4.14 Simulated multilevel voltage waveforms with: (a) 2-level, (b) 3-level, (c) 4-level, and (d) 5-level.	49

Fig. 4.15 Simulated voltage waveforms: (a) without load, (b) with 0.1 nF and 1 G Ω load, and (c) with 1 nF and 1G Ω load.	50
Fig. 4.16 Experimental setup: (a) the full modular pulse generator that includes: (1) microcontroller, (2) power sources for drive circuits, (3) buffer and optical transmitter board, (4) wave-shaping resistors, (5) drive circuit board, (6) modular HV pulse generator, and (b) the modular topology.	51
Fig. 4.17 Measured voltage waveforms: (a and b) 3.2 kV rectangular pulses, and (c) zoomed view of the rise time (66 ns).	52
Fig. 4.18 Measured voltage waveforms: (a) output of each module and (b) capacitor's voltage.	53
Fig. 4.19 Measured voltage waveforms: (a) across charging switch and (b) across discharging switch.	53
Fig. 4.20 Measured voltage waveforms of diodes: (a) D ₁ , (b) D ₂ , (c) D ₃ , (d) D ₄ , and (e) D ₅	54
Fig. 4.21 Measured voltage waveforms with different rise times: (a) 80 ns, (b) 110 ns, (c) 164 ns, and (d) 208 ns.	55
Fig. 4.22 Measured voltage waveforms with different duty cycles: (a) t ₃ =6% and (b) t ₃ =34%.	56
Fig. 4.23 Measured voltage waveforms with different overshoots: (a) control 1, (b) control 2, (c) control 3, and (d) control 4.	57
Fig. 4.24 Measured voltage waveforms with different frequencies: (a) 1 kHz and (b) 10 kHz.	57
Fig. 4.25 Measured multilevel waveforms: (a) 5-level, (b) 5-level, (c) 4-level, (d) 3-level, and (e) 2-level.	59
Fig. 4.26 Measured 2 kV pulses: (a) without any sample, (b) with one sample, and (c) with two parallel samples.	61
Fig. 4.27 Zoomed view of the measured 2 kV pulses with increasing load: (a) without any sample, (b) with one sample, and (c) with two parallel samples.	62
Fig. 4.28 The modified version of the pulse generator for the aging tests.	63
Fig. 5.1 The flowchart representing the parameters studied on the wires.	64
Fig. 5.2 The applied voltage waveshape of the pulse rising edge measured at the terminal of the test objects.	66
Fig. 5.3 The measured PDIV values of the aged samples at (a) 10% OS and (b) 20% OS.	68
Fig. 5.4 The measured average DF values of the aged samples in a frequency sweep of 1 kHz down to 0.1 Hz at (a) 10% OS and (b) 20% OS.	69

Fig. 5.5 The measured average DF values of the aged samples at 0.1 Hz at (a) 10% OS and (b) 20% OS.....	71
Fig. 5.6 The measured average capacitance values of the aged samples in a frequency sweep of 1 kHz down to 0.1 Hz at (a) 10% OS and (b) 20% OS.....	72
Fig. 5.7 The measured temperature of the samples in the crotch area under energization at (a) 10% OS and (b) 20% OS.....	74
Fig. 5.8 The optical microscope images from the surface of the (a) unaged CR wire and (b) aged CR wire.....	75
Fig. 5.9 The optical microscope images from the surface of the (a) unaged NCR wire and (b) aged NCR wire.....	75
Fig. 5.10 The 3D AFM images of the surface of (a) the unaged CR wire and (b) the aged CR wire. .	76
Fig. 5.11 The 3D AFM images of the surface of (a) the unaged NCR wire and (b) the aged NCR wire.	77
Fig. 5.12 The applied voltage waveshape of the pulse rising edge measured at the terminal of the test objects.....	78
Fig. 5.13 The measured PDIV values of the aged samples at (a) 10% overshoot and (b) 20% overshoot.	80
Fig. 5.14 The measured average DF values of the aged samples in a frequency sweep of 1 kHz down to 0.1 Hz at (a) 10% overshoot and (b) 20% overshoot.	81
Fig. 5.15 The measured average DF values of the aged samples at 0.1 Hz at (a) 10% overshoot and (b) 20% overshoot.....	82
Fig. 5.16 The measured temperature of the endpoint of the samples during the experiments at (a) 10% overshoot and (b) 20% overshoot.....	83
Fig. 5.17 The optical microscope images from the surface of the (a) unaged CR wire and (b) aged CR wire.....	84
Fig. 5.18 The 3D AFM images of the surface of (a) the unaged CR wire and (b) the aged CR wire. .	85
Fig. 5.19 The SEM images of the surface of the unaged CR wires at (a) 300 μm , (b) 10 μm , and (c) 100 nm magnification.....	86
Fig. 5.20 The SEM images of the surface of the electrically aged CR wires at (a) 300 μm and (b) 300 nm magnification.....	86

Fig. 5.21 The measured PDIV (PU) values of the aged samples of the controlled thermal test and the combined thermal and electrical test.	87
Fig. 5.22 The measured average %DF (PU) of the aged samples of the controlled test and the combined temperature and electrical test in a frequency sweep of 1 kHz down to 0.1 Hz.	88
Fig. 5.23 The optical microscope images from the surface of the (a) unaged CR wire and (b) thermally aged CR wire.	88
Fig. 5.24 The SEM images of the surface of the thermally aged CR wires at (a) 3 μm and (b) 300 nm magnification.	88
Fig. 5.25 The optical microscope images from the surface of the (a) unaged CR wire and (b) thermally & electrically aged CR wire.	90
Fig. 5.26 The optical microscope image from the surface of the thermally and electrically aged CR wire.	90
Fig. 5.27 The SEM images of the surface of the combined thermally and electrically aged CR wires at (a) 100 μm (b) 20 μm , and (c) 500 nm magnification.	91
Fig. 6.1 Main effect and interaction of the factors considering (a) % Δ PDIV and (b) % Δ DF as a response.	95
Fig. 6.2 Interaction plots of the % Δ PDIV for (a) CR wires and (b) NCR wires.	96
Fig. 6.3 Interaction plots of the % Δ DF for (a) CR wires and (b) NCR wires.	97
Fig. 6.4 Main effect and interaction of the factors considering (a) % Δ PDIV and (b) % Δ DF as a response.	101
Fig. 6.5 Interaction plots of the % Δ PDIV for the factors (a) A and B, (b) A and C, and (c) B and C.	103
Fig. 6.6 Interaction plots of the % Δ DF for the factors (a) A and B, (b) A and C, and (c) B and C. .	104
Fig. 6.7 The measured PDIV (PU) of the tests in the oven.	106
Fig. 6.8 The measured average DF values of the aged samples in a frequency sweep of 1 kHz down to 0.1 Hz.	106
Fig. 6.9 The intentionally failed sample showing the high-field regions on the wire edge.	107
Fig. 6.10 Chemical structure of poly (amide imide) monomeric unit [93].	109
Fig. 6.11 The comparison plot showing the Carbon and Oxygen percentage content on the CR wire surfaces under different stress conditions.	109
Fig. A.1 The EDX result from the surface of the unaged CR wire.	125

Fig. A.2 The EDX result from the surface of the thermally aged CR wire.	125
Fig. A.3 The EDX result from the surface of the electrically aged CR wire.....	126
Fig. A.4 The EDX result from the surface of the thermally and electrically aged CR wire.....	126

List of Tables

Table 2.1 Summary of the focus of the reviewed studies on twisted pair wire samples.	12
Table 2.2 Summary of the focus of the reviewed studies on flat conductors.	17
Table 2.3 Comparison between the proposed topology and 15 other pulse generation topologies used in the literature.....	19
Table 3.1 Omicron PD measurement system specifications.	27
Table 3.2 The temperature measurement results for the controlled experiment with different emissivity values.....	30
Table 4.1 Simulation parameters of the generator for 3.2 kV pulses.	44
Table 4.2 Experimental parameters of the generator for 3.2 kV pulses.	45
Table 5.1 High and low levels of the voltage waveform factors.	65
Table 5.2 The test conditions and pulse parameters.	66
Table 5.3 High and low levels of the voltage waveform factors.	78
Table 5.4 The test conditions and pulse parameters.	78
Table 6.1 The % Δ PDIV and % Δ DF results at 0.1 HZ.	94
Table 6.2 The % Δ PDIV and % Δ DF Results.	100

Chapter 1

Introduction

1.1 Transportation Electrification

Global warming is a significant concern, and transportation electrification presents a viable solution for mitigating it by reducing fossil fuel consumption and CO₂ emissions. Among the primary areas of electrification that are gaining global adoption is the transition to electric vehicles (EVs) [1]. While EVs are already on the road, challenges such as extended charging times and limited range per charge continue to hinder wider consumer adoption, slowing the shift from internal combustion (IC) engines to EVs.

Continuous improvements in the EV field aim to address these limitations through technological advancements, including increasing the voltage level, utilizing hairpin-wound motors, and integrating wide-bandgap (WBG)-based drives. Currently, EVs typically operate at a voltage level of 400 V. However, factors such as reducing charging time, improving efficiency, and meeting higher power requirements are pushing toward 800 V systems [2]. In an 800 V EV, the current required to achieve the same output power is halved. This reduction in current enables the utilization of smaller conductor cross-sections and results in decreased heat generation [3]. Doubling the voltage in EVs offers numerous benefits but introduces new challenges such as higher electrical stress on the insulation system.

Hairpin-wound motors are increasingly adopted in EVs due to their notable advantages over conventional random-wound motors. These advantages include higher power density, reduced weight and size, and better control over voltage distribution within the windings [4], [5]. The improved mechanical and thermal properties of hairpin windings further make them ideal for high-power applications in EVs.

Another critical development in EV technology is the adoption of WBG device-based power electronics, which are gradually replacing traditional silicon (Si)-based devices. WBG semiconductors, offer significant benefits, including lower on-state resistance (resulting in reduced conduction losses), faster switching times, higher operating temperatures, and the ability to handle higher voltage and current ratings [6]. These advantages translate into improved overall system efficiency, reduced component size, and enhanced power density. However, the higher switching frequency and fast rise

time of WBG device-based drives introduce increased electrical stresses, particularly on motor windings, which necessitates further investigation into their long-term reliability and insulation performance.

1.2 Motor Windings

Based on the voltage level, motors employed in the industry can be categorized into three distinct groups: low voltage (LV), medium voltage (MV), and high voltage (HV) motors. Irrespective of the voltage level employed in a motor, it is essential to ensure that the electrical insulation system is of sufficient quality to ensure the motor's safe operation. The efficacy of the insulation system is influenced by the thermal and electrical stresses imposed due to the voltage level.

Motor insulation systems are generally classified into two main types: Type-I and Type-II insulation. Type-I insulation systems are typically employed in LV motors, such as those used in EVs. The materials that are used in Type-I insulation cannot sustain partial discharge (PD) and should be operated under PD-free conditions [7]. Conversely, MV and HV motors utilize Type-II insulation systems, which are designed to withstand PD activity [8]. Within the scope of this research, the focus will be directed towards examining LV motors equipped with Type-I insulation systems.

Random-wound windings used to be the common stator motor windings used in EVs. Random-wound windings consist of insulated round conductors that form coils in the stator slot. These windings typically exhibit a low fill factor, which refers to the ratio of conductive material to the total slot area. Two approaches can be taken to increase the fill factor: increasing the number of conductors in each slot or increasing the cross-section of the conductors. The fill factor directly affects the power density of the motor, which is a critical factor for EV applications [9], [10].

In recent years, there has been a shift toward the adoption of hairpin windings in the automotive industry. Hairpin windings utilize rectangular flat conductors, which offer several advantages over traditional random-wound windings. These benefits include a higher fill factor, improved machine performance, increased efficiency, enhanced thermal dissipation, and reduced overall winding length and weight [4], [5]. The use of rectangular conductors allows for better slot utilization, resulting in a more compact and efficient motor design. Conductors in the stator slot for both random-wound and hairpin-wound windings are illustrated in Fig. 1.1 [11].

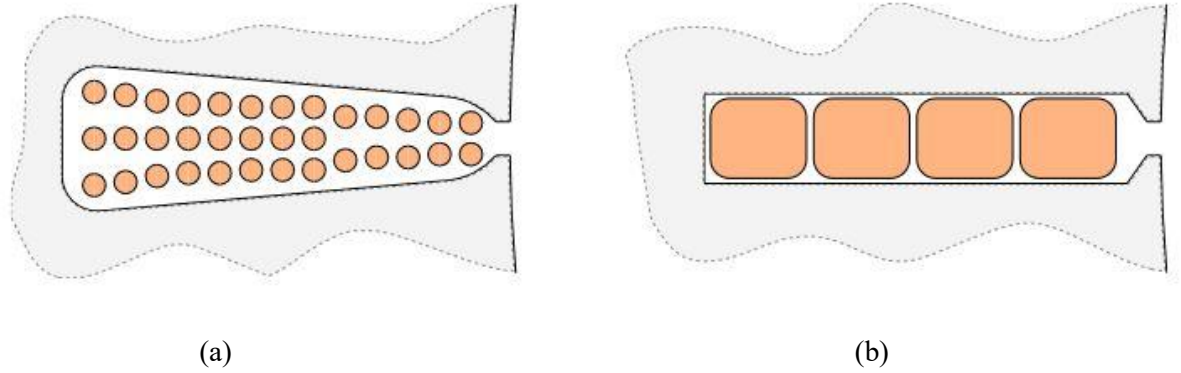


Fig. 1.1 Conductors in a stator slot: (a) random-wound winding and (b) hairpin-wound winding [11].

1.3 Power Electronics Drives

Power electronics converters, employing pulse width modulation (PWM) techniques, are extensively used to drive motors. The overall view of the drive system used in EVs is depicted in Fig. 1.2, which has a DC bus, an inverter, and a motor connected to the inverter by cable [3]. While conventional Si switches have been commonly employed in these drives, the introduction of WBG devices has brought significant advancements. The two main types of WBG devices are silicon carbide (SiC) and gallium nitride (GaN) devices. Compared to Si switches, WBG device-based switches offer valuable advantages, including improved temperature performance, higher voltage and current ratings, higher switching frequencies, and faster switching transitions [6].

Notably, WBG devices possess the capability to handle high voltages and currents, making them well-suited for high-power applications. These switches can operate at a higher switching frequency, enabling the reduction in size, weight, and cost of the converter due to the use of smaller components and filters. Furthermore, in comparison to Si-based devices, WBG devices exhibit superior thermal conductivity, which results in reduced heatsink size requirements [6], [12], [13].

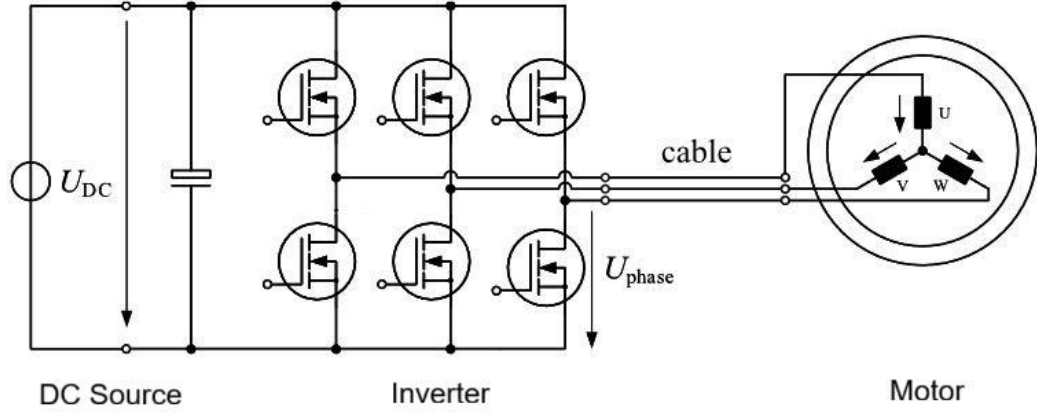


Fig. 1.2 System overview representing the DC source, drive, cable, and the motor [3].

The integration of power converters incorporating WBG switching devices offers significant advantages that are appealing for EV applications. However, the introduction of these devices also poses challenges for the insulation system, primarily due to the rapid voltage transients and higher electrical stresses they introduce [6], [12], [13]. These transients can adversely impact the insulation system's reliability and long-term performance.

To evaluate the impact of WBG device-based drives on motor insulation, it is crucial to replicate the overvoltage and transient conditions observed during inverter-fed motor operation. HV pulses are commonly used in testing to simulate these conditions, as they can effectively reproduce the rapid switching transients [2], [3], [7]. HV pulses have diverse applications [14], [15], one of which is assessing the reliability and safety of motor insulation systems. Given the ongoing trend of integrating WBG switching devices in EVs, there is an urgent need to evaluate and understand the behavior of motor insulation systems under these operating conditions to ensure safe and reliable performance.

1.4 Insulation Concerns

Among the leading causes of motor failures, bearings are widely recognized as the most common issue. However, stator-related failures rank second, with turn-to-turn insulation breakdown being the most prevalent cause of failure within the stator [16], [17], [18]. This thesis focuses on turn-to-turn insulation, particularly in hairpin-wound motors. While numerous studies have investigated the turn-to-turn insulation of random-wound windings, their findings may not be applicable to hairpin windings. This is due to the difference in voltage stress experienced by turn-to-turn insulation in random-wound versus form-wound windings [19].

The insulation system of inverter-fed motors is subjected to distinct characteristics of transients and overvoltage, necessitating pre-operational testing. Many of these characteristics cannot be replicated using the drive circuits employed for motor operation. Hence, it is necessary to utilize specialized pulse drive circuits capable of emulating the stresses that converters impose on motor insulation. HV pulse generators represent the appropriate drive circuits for generating comparable or analogous conditions to test insulation systems. These conditions include various parameters like voltage amplitude, rise time, switching frequency, duty cycle, overshoot, and waveshape. A summary of the effects of each parameter on motor insulation is provided below:

The voltage amplitude of a system is directly linked to the electrical stress experienced by insulation. A higher voltage level results in an elevated electric field. While increasing the insulation thickness is a viable solution for higher voltage levels, it presents challenges such as elevated costs, space constraints, and reduced thermal dissipation efficiency, which can hinder overall motor performance [20], [21].

The impact of rise time on insulation should be noted, as a faster rise time corresponds to increased stress exerted on the insulating material. A fast rise time results in an uneven voltage distribution, leading to an uneven distribution of the electric field in a motor winding. Consequently, certain regions may experience elevated electric field strengths, which can initiate PDs. Compared to conventional Si switching devices, WBG device-based devices have much faster rise times, typically in the nanosecond range, making it crucial to evaluate their impact on motor insulation [2], [22].

High switching frequency increases the overvoltages at motor terminals and stator neutral, due to voltage reflection and common-mode voltage. These overvoltages impose additional stress on the insulation system, reducing its lifespan. The drive's switching frequency also influences PD activity, which affects insulation performance. However, the relationship between PD magnitude and switching frequency remains debated, with conflicting findings reported in the literature [6], [23], [24]. Higher frequencies are expected to accelerate degradation due to greater energy deposition per unit of time, as PD signals occur more frequently, leading to intensified insulation damage [19], [25]. Additionally, higher frequencies exacerbate localized heating from PD activities and repeated charge-discharge cycles, further weakening the insulation [18], [19].

The duty cycle of the applied voltage is another critical parameter. A higher duty cycle reduces the insulation system lifespan, even in the absence of PD activity. However, it is worth noting that certain

studies have presented contrasting findings, suggesting that the duty cycle may not have a significant effect on the insulation lifetime [2].

Overshoot is another important factor that imposes stress on the insulation system. It can be generated by different reasons like stray inductance and capacitance, fast rise time, and cable length [26]. A higher overshoot increases the insulation degradation rate, due to increased electric field stress [22], elevated PD intensity [18], [22] and a rise in temperature [27].

In the context of motor vehicles, the waveshape of the applied voltage also plays a significant role. The utilization of multilevel waveforms has been shown to effectively mitigate overvoltage and reduce stress imposed on the insulation system. By increasing the levels of the output voltage in multilevel waveshapes, the stress on the insulation is diminished, thereby enhancing the overall lifetime of the insulation system. However, multilevel waveform generation comes with trade-offs, including higher costs and increased complexity in the power converter design [2], [28], [29].

Another significant concern pertaining to drive-fed motors is the cable length between the motor and the drive. Wave propagation and the subsequent reflection along the cable can lead to overvoltages at the motor terminals that may reach up to twice the operating voltage. Longer cable lengths worsen the overvoltage problem, particularly for systems with short pulse rise times. One mitigation strategy is the adoption of integrated motors, where the drive circuit is directly mounted on the motor. This integration minimizes cable length, reducing overvoltage risks [30]. However, in EVs, the cable length is not typically a concern, as the drive is located near the motor.

1.5 Research Motivation

Electrification is undergoing significant advancements across various transportation sectors. Three pivotal areas of transformation are motor winding, power converters, and energy storage devices. The shift from random-wound winding to hairpin-type winding, a form-wound configuration, is gaining prominence. Additionally, power converters are transitioning from traditional Si-based switches to WBG device-based switches. These developments are crucial and need a comprehensive investigation for reliability concerns.

Pulse generators are widely used for insulation testing, yet there is limited literature specifically addressing their design for this purpose. Existing pulse generators often rely on simple configurations using switches and DC power supplies, which fail to replicate many transient conditions encountered

in real-world scenarios. Consequently, there is a need for a pulse generator that provides extensive control over various pulse parameters to effectively test motor insulation. A WBG device-based pulse power supply with highly configurable output parameters becomes indispensable for insulation testing purposes.

The use of flat conductors in transportation applications offers numerous advantages, particularly in the context of hairpin technology in EVs. Hairpin windings employ flat conductors with Type-I insulation, yet this area lacks standardized practices and is not well investigated, especially concerning the interaction of hairpin windings with WBG device-based power converters. This gap highlights the necessity of the targeted study in this thesis.

1.6 Summary

Transportation electrification is undergoing rapid advancements and transformations. In the context of EVs, three inevitable changes are occurring, including the shift from random-wound to hairpin winding, the transition to higher operating voltage levels, and the adoption of WBG device-based drives. These changes are driven by numerous advantages, including improved performance, higher efficiency, and increased power density.

These advancements also introduce new challenges, particularly for motor insulation systems, which must be thoroughly investigated under the impact of these technological shifts. Currently, there are no established standards in this field, and limited research has been conducted to provide a comprehensive understanding of the implications of these inevitable changes in EV technology.

To address these gaps, this research proposes and develops a WBG device-based HV pulse generator to study the effects of WBG device-based drives on motor insulation. Additionally, back-to-back wire samples, fabricated using actual wires employed in EV motors, have been developed to examine the turn-to-turn insulation performance of hairpin windings.

The structure of the thesis is as follows:

Chapter 2: Literature Review This chapter briefly describes the existing literature on turn-to-turn insulation studies of LV motors and the HV pulse generators available for testing motor insulation. The limitations and drawbacks of these generators are discussed. Additionally, the research gap, motivation, and objectives driving this thesis are presented.

Chapter 3: Materials and Methods This chapter outlines the materials and methodologies employed in this research. It details the sample preparation process, experimental test setup, insulation performance measurement techniques, test procedures, and the design of experiments.

Chapter 4: SiC-MOSFET High-Voltage Pulse Generator for Motor Insulation Testing This chapter focuses on the development of a WBG device-based pulse generator designed specifically for testing motor insulation. The proposed generator is thoroughly described, including its design, functionality, and technical specifications. Simulation results and experimental validation are also presented.

Chapter 5: Results This chapter presents the results of the performance evaluation of turn-to-turn insulation in hairpin windings under repetitive pulse conditions and PD activity.

Chapter 6: Discussion This chapter discusses the results obtained in the previous chapter, characterizing the effects of pulse parameters such as rise time, overshoot, frequency, and duty cycle on turn-to-turn insulation performance.

Chapter 7: Conclusion and Suggestions for Future Work This chapter summarizes the research findings and highlights the contributions of this work. Recommendations for future research directions are also provided.

Chapter 2

Literature Review

The literature review chapter is structured into four main sections. The first section reviews studies on motor insulation, focusing specifically on turn-to-turn insulation. The second section examines pulse generation methods used to evaluate motor insulation. The next section identifies research gaps and presents the motivation for this thesis. The final section presents the thesis objectives.

2.1 Motor Insulation

2.1.1 Random-Wound Winding

Random-wound windings have been widely used in EVs, with their turn-to-turn insulation typically modeled using twisted-pair wire samples. The insulation system in random-wound windings is classified as Type-I insulation, which is composed of materials that need to be operated under PD-free conditions [7], [31]. Numerous studies have examined the turn-to-turn insulation of random-wound windings (using twisted pairs), focusing primarily on the effects of pulse parameters on PD activities, as well as on thermal aging tests, and endurance tests.

Turn-to-turn insulation endurance of twisted pairs and coils made with flat conductors were tested under an SiC-based inverter in [19]. Among the wires tested, corona-resistant wires demonstrated superior endurance. It was observed that an increase in voltage level, combined with a higher switching frequency, significantly reduced the time to failure of the turn-to-turn samples.

The effects of WBG device-based drives on PD behavior in motors were investigated in [20]. The investigation employed two-level, three-level, and quasi-level PWM waveforms. A twisted-pair model was created, consisting of one enameled wire and one bare wire, to replicate turn-to-turn insulation. The experiments were conducted within a pressure vessel maintained at a pressure of 65 kPa, with PD activities being monitored using a UHF antenna. Two distinct testing setups were employed: in the first one, the drive output was directly connected to the motor sample, while in the second one, a 12-meter cable was used to connect the motor sample to the converter. Results revealed that a higher voltage jump between multilevel waveforms led to increased PD activity, emphasizing the importance of waveshape design in mitigating insulation stress.

The effect of resin on PD activities was explored in [21] for automotive applications. Twisted pairs with different insulation materials and thicknesses were analyzed under AC and pulse voltage while considering the temperature effect. The study revealed that thicker insulation reduces the electric field intensity, thereby increasing the partial discharge inception voltage (PDIV). Conversely, increasing the conductor thickness decreased the PDIV, as demonstrated for rectangular conductors in [32].

PD behavior was further investigated under fast-rise-time pulses in [22]. It was observed that PDs mainly appear at the voltage flanks; however, with faster rise times, PDs could also occur at the maximum voltage. Faster rise times were associated with higher PD magnitudes and more frequent PD events per cycle. Additionally, the study demonstrated a direct correlation between the highest PD amplitude and the overshoot level.

The effect of short-width pulses generated by SiC converter on the PDIV of twisted pairs was studied in [33]. The samples were tested under 2-level and 3-level square waveforms with varying pulse widths. Results showed that 3-level waveforms with shorter pulse widths yielded higher PDIV compared to 2-level waveforms. Also, a lower duty cycle led to a higher PDIV, which can be attributed to the lower average electrical stress.

The PD behavior and repetitive PDIV of twisted pairs energized by pulses generated from an SiC pulse generator were evaluated under varying rise times in [34]. It was found that PDs predominantly occurred during the switching slope of the test voltage. Over the studied rise time range (70 to 900 ns), the rise time had no significant effect on the PDIV, underscoring the complexity of insulation performance under transient conditions.

The PD behavior and lifetime of the turn-to-turn insulation of twisted pairs and back-to-back samples under pulses generated by an SiC converter were compared in [35]. It was found that results from twisted pairs cannot be directly generalized to hairpin windings. The back-to-back samples exhibited lower PD activity and higher PDIV, and the finite element method (FEM) analysis indicated a more uniform electric field distribution for the back-to-back samples.

The effects of different voltage waveforms on the PDIV and PDEV of random-wound turn-to-turn samples were evaluated in [36]. The results concluded that higher temperatures and waveforms with overshoot increase PD activity and decrease PDIV. Furthermore, the temperature effect on the PDIV of twisted-pair wires was studied in [37]. Samples tested at various temperatures and pressures showed that PDIV values decreased with increasing temperature.

Twisted-pair Litz wires were tested under HV pulses to evaluate the PDIV and time-to-failure analysis in [38]. The findings indicated a higher PDIV under 3-level low duty cycle waveforms compared to 2-level waveforms, though no significant improvement in endurance time was observed. A short time-to-breakdown, measured in minutes, was recorded for voltages just above the PDIV threshold.

In [39], the influence of inverter levels and pulse rise times on PD and the life behavior of twisted pairs was analyzed. Using a PWM power supply with varying rise times (60 ns, 1 μ s, and 25 μ s) at a 50 Hz fundamental frequency and a 1 kHz switching frequency, the study showed that increased inverter levels reduced PD magnitude and repetition rates. Additionally, the voltage jump between inverter modulation levels decreased with higher inverter levels, contributing to improved insulation reliability. Faster rise times (e.g., 60 ns) significantly increased PD magnitude and repetition rates, while no substantial differences were observed between 1 μ s and 25 μ s rise time pulses. The study also highlighted the importance of considering the fundamental frequency for multilevel converters, aligning with findings from [40] that emphasized its role in determining insulation performance.

The effects of waveform polarity and switching frequency on PDIV in enameled wires were studied in [41]. Results indicated that PDIV was higher for unipolar waveforms compared to bipolar waveforms, attributed to space charge accumulation within the insulation. Furthermore, unipolar waveforms cause larger PD amplitudes due to the sustained electric field. While the PDIV remained relatively constant with increasing switching frequency, PD magnitudes increased, suggesting accelerated insulation aging. This suggests that a higher switching frequency accelerates the aging process of the insulation, not only due to more cycles per second but also due to the higher magnitude of PD activity.

Results in [41] align with the observations reported in [42], where the life of twisted pair wires was found to be reduced as the supply frequency increased, irrespective of whether the supply was sinusoidal or square waveforms, even in cases where no PD occurrences were observed. However, the effect of frequency was much more pronounced when PD activity was present.

The influence of various PWM parameters on twisted enameled wires was investigated in [43]. The effects of duty cycle, switching frequency, rise time, overshoot, and ringing on PDIV were studied. Lower PDIV was observed with smaller duty cycles, while switching frequency (100 Hz to 1 kHz) and

rise time (70 ns to 250 ns) had no significant impact on PDIV. However, increased overshoot, rather than rise time itself, led to lower PDIV.

Twisted pairs with three different coatings were tested under repetitive bipolar pulses to analyze PD degradation and life endurance in [44]. Boehmite/polyimide coatings exhibited superior performance, with longer life and smaller wear loss compared to neat polyimide coatings.

The summary of the focus of the reviewed studies on twisted pair wire test samples is presented in Table 2.1. The findings emphasize the importance of considering overall waveform characteristics.

Table 2.1 Summary of the focus of the reviewed studies on twisted pair wire samples.

Parameter	PD Behavior	Thermal Test	Endurance Test
Reference	[20], [21], [22], [33], [34], [35], [36], [38], [39], [40], [41], [43]	[21], [36], [37]	[19], [21], [35], [38], [39], [40], [42], [44]

2.1.2 Hairpin Winding

In EVs, random-wound windings are being replaced by hairpin windings due to their various advantages. Hairpin windings provide a more robust solution for transportation applications compared to random-wound windings. They offer improved mechanical strength and thermal performance, making them suitable for demanding transportation operating conditions. Additionally, hairpin windings have a higher fill factor, meaning they utilize the available space more efficiently, resulting in increased power density [45].

Hairpin winding is a form-wound winding (using Type-I insulation) (shown in Fig. 2.1 [46]) that has gained significant importance in the transportation electrification trend. The fabrication of hairpin windings is different from form-wound windings, due to the different motor insulation systems used in these windings. The manufacturing process for hairpin windings is simpler than that of random-wound windings, which reduces cost, complexity, and production time. The higher slot fill factor in hairpin windings leads to greater power density. Additionally, the reduced amount of insulation material in hairpin winding enhances the heat transfer rate, allowing higher currents to flow through the

conductors. Moreover, the compact end-winding design results in lower DC copper losses and smaller motor sizes compared to random-wound motors [5], [11], [47], [48], [49].

Despite their advantages, hairpin windings present two primary challenges: limited conductor configurations per slot and increased AC losses. These issues have been addressed through advancements in winding transposition techniques and optimized winding connection configurations [47].

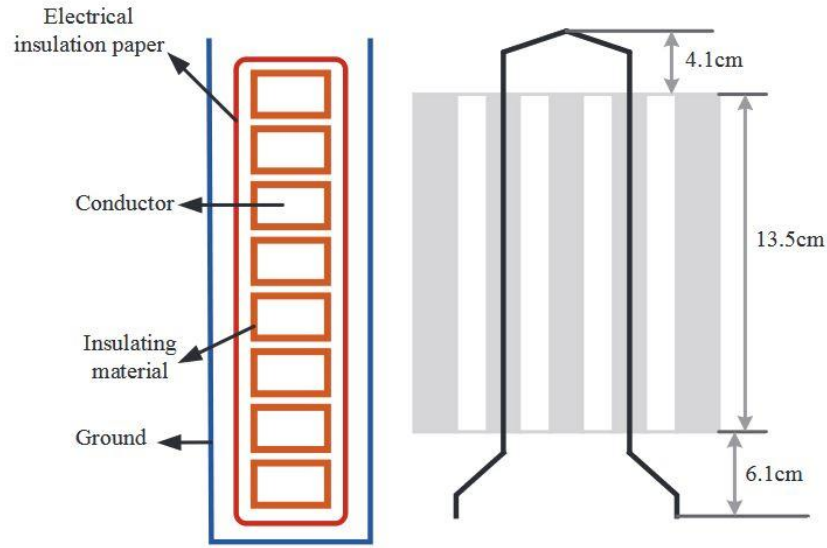


Fig. 2.1 Schematic representation of the structure of hairpin winding [46].

The turn-to-turn insulation in hairpin winding is modeled as parallel conductors or back-to-back samples. Previous studies have explored some aspects of turn-to-turn insulation in hairpin windings. For instance, PD activity under various pulse parameters has been investigated to understand PD behavior under distinct voltage stresses [35], [46], [50]. Additionally, back-to-back samples have been subjected to different temperature conditions, sometimes combined with mechanical vibrations, to examine the effects of thermal and mechanical stress on turn-to-turn insulation [16], [17]. Some research has focused on testing insulation under sustained electrical stress until failure [17], [19], [35], [50], though these approaches have not addressed aging effects under electrical stress accompanied by PD activity.

PD measurement under ac voltage using phase-resolved partial discharge (PRPD) pattern in the slot of hairpin-wound stator was investigated in [46]. This work focused on testing a single stator slot with

multiple conductors (Fig. 2.2). Six different winding configurations were tested, and it was observed that the PDIV varies considerably across different configurations. It was shown that as the winding configuration is more symmetrical, there will be a more uniform voltage distribution among the windings, which will lead to a higher PDIV.

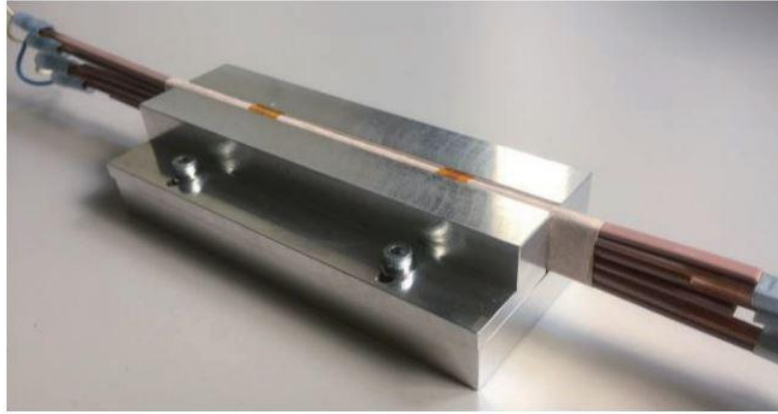


Fig. 2.2 Structure of miniaturized test block used in [46].

The insulation system was examined under repetitive partial discharge inception voltage (RPDIV) on hairpin winding in [50]. The test specimens in the slot area are flat conductors with enamel insulation and slot insulation as shown in Fig. 2.3. To fill the air space between the test samples, they were impregnated with resin by trickle process. PD measurements were carried out, and failure reasons were investigated. It was shown that the specimens in the end winding fail faster than other specimens, so there should be careful attention to the end winding.

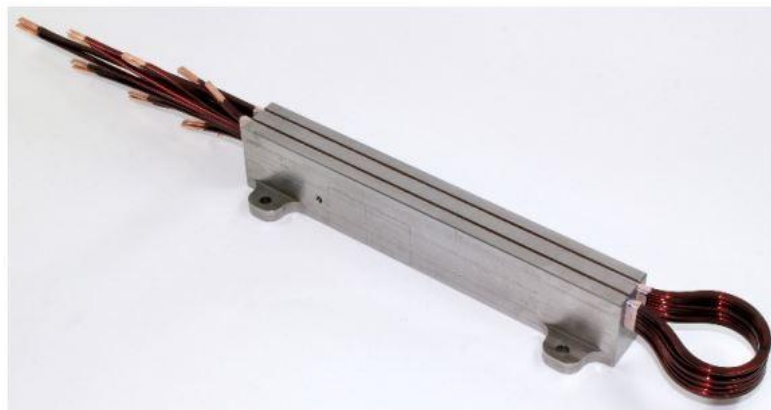


Fig. 2.3 Test specimen to represent the insulation system in the slot area [50].

In [17], hairpin winding insulation analysis was performed, and it was shown that turn-to-turn insulation is the weakest point in the hairpin motor winding, so the focus was on turn-to-turn insulation. Back-to-back bars were used as a model for turn-to-turn insulation as the test samples, which are shown in Fig. 2.4. The focus was to evaluate the thermal and mechanical stress, and these stresses led to insulation breakdown without PD.

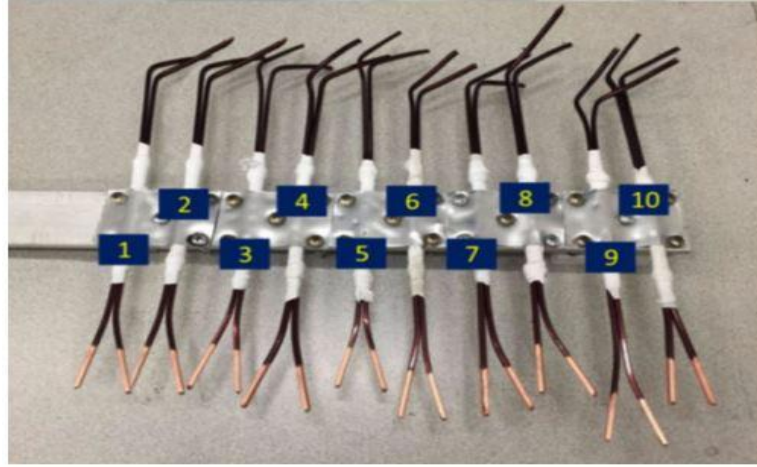


Fig. 2.4 Back-to-back samples used to study turn-to-turn insulation [17].

The thickness and length of winding copper strands have a significant impact on the PDIV and the lifetime of turn insulation in electric machines [32], [51]. Test sample dimensions are not defined by IEC/TS 60034-18-42, so in order to avoid the dependency of sample dimensions on PDIV, a complete coil was tested in [32]. The effects of vacuum pressure impregnation (VPI) on PDIV and the effect of copper strand thickness on VPI and PDIV were examined. The study found that the PDIV of thicker strands decreased after the VPI process, while the PDIV of thinner strands increased. However, before the VPI process, thicker copper strands exhibited higher PDIV compared to thinner strands. Turn insulation thickness was also analyzed before and after the VPI process. Without VPI, thicker turn insulation exhibited a higher PDIV than thinner turn insulation. However, after the VPI process, the PDIV decreased for thicker turn insulation but increased for thinner turn insulation [32]. Different insulation structures and copper strand thicknesses were tested in [51], and PDIV and lifetime tests were conducted. It was found that samples without filler have higher PDIV but larger scattering due to air pockets. Furthermore, longer copper strands resulted in lower PDIV for samples with main insulation.

The effect of thermal aging on polyamide-imide and perfluoroalkoxy-coated magnet wires was studied in [16]. The perfluoroalkoxy-coated magnet wires outperformed the polyamide-imide wires under the thermal aging test, with insulation delamination and degradation observed only in the polyamide-imide-coated wires.

The effect of the pulse voltage duty cycle on PD behavior and insulation endurance on single-contact enameled wires was tested in [52]. Shorter pulse widths led to asymmetric PD patterns, with lower PD magnitudes at falling flanks. Symmetric PD patterns were observed at 50% duty cycle. Insulation endurance decreased significantly with increasing duty cycle. PD magnitudes increase with pulse width, stabilizing for widths longer than 100 μ s.

Voltage stress and voltage distribution in the stator winding are studied in [6], [53], [54]. In [6], three distinct types of overvoltages were examined using a complete winding: phase-to-phase motor terminal overvoltage, phase-to-ground overvoltage, and neutral-to-ground overvoltage. The findings revealed that the neutral overvoltage in the motor can be generated without the presence of any cables. The motor terminal overvoltages will mostly drop on the first coils, however, the motor neutral overvoltage will mostly drop on the last turn, close to the neutral point. Consequently, during the insulation design stage, special attention should be given to the neutral overvoltage of the motor. The overvoltages under investigation were generated using WBG devices, and the study specifically explored the effects of fast switching and high switching frequency on these overvoltages. The motor and the drive were interconnected using cables of varying lengths, specifically 3.9 meters and 70 meters. The findings revealed that faster rise times of the pulse necessitate a reduction in the critical cable length.

A model based on inductive and capacitive coupling mechanisms is presented in [53] for voltage distribution in stator windings. It was shown that the first turn of the first coil experiences the highest voltage stress. Voltage stress calculations for hairpin winding under SiC MOSFET operation were detailed in [54]. The inter-turn voltage stress was calculated using a high-frequency equivalent circuit model. The study revealed that the maximum voltage stress occurs on the first and last turn coils. These findings are critical for identifying the most stressed spots in a motor to prevent failure.

The summary of the focus of the reviewed studies on hairpin-wound windings is presented in Table 2.2.

Table 2.2 Summary of the focus of the reviewed studies on flat conductors.

Parameter	PD Behavior	Thermal Test	Endurance Test
Reference	[32], [35], [46], [50], [51], [52]	[16], [17]	[17], [19], [32], [50], [51], [52]

2.2 Pulse Generators for Motor Insulation Testing

HV pulse generators play a critical role in the evaluation of motor insulation systems. In [55], a square wave HV pulse generator was introduced for motor insulation testing. The generator employs two distinct configurations: a one-channel structure that allows for variable rise time and a multi-channel structure with a fixed rise time. The basic topology of the generator is a first-order RC circuit, where the pulse parameters are controlled by varying the resistance through HV relays. The design incorporates two power sources connected to a push-pull switch, enabling the delivery of continuous positive or negative voltage to the load without a zero-voltage level. However, this continuous voltage characteristic deviates from the stress profiles typically associated with PWM waveforms, potentially limiting its representational accuracy.

In [56], a rectangular HV pulse generator capable of producing both unipolar and bipolar pulses was proposed. The design utilizes push-pull switches as a DC chopping circuit, powered by two HVDC voltage sources. To manage high voltage levels, multiple MOSFETs are connected in series, with a control strategy implemented to address voltage distribution challenges across the devices. To mitigate the prolonged turn-off time inherent to the main switches, additional MOSFETs are integrated to expedite the turn-off process. This design includes several types of switches: some designed to withstand high-voltage stress and others to drive the primary switching components. There are charging resistors in this structure, which result in energy consumption, heat generation, and may adversely affect voltage regulation.

A bipolar HV pulse generator employing a full-bridge topology was presented in [57]. This design integrates multiple IGBTs connected in series within each leg of the bridge. Snubber circuits are incorporated to mitigate issues associated with the series connection of the switches. Additionally, a resistor is connected in parallel with the load to stabilize switch operation. The output of this generator

is a two-level pulse alternating between positive and negative values. There is no control over the rise time, except by using additional components like resistors or capacitors in the circuit.

HV pulses were used to investigate PD activities in twisted pairs in [58], [59], [60], [61]. The HV pulse generator in [58] consists of an HVDC source with a pulse generator as the input voltage source. A capacitor is connected in parallel to the load that controls certain pulse parameters. This generator has several limitations such as the ability to generate only negative surge pulses, single-level output, and a lack of control over pulse parameters. In [59], the pulse generator is similar to [58], but it allows for the generation of positive or negative pulses with 6 to 60 Hz frequency range. In [60], square pulses with an amplitude of 6 kV peak-to-peak were generated using an HV RF source. Semi-square pulses were generated in [61] using IGBTs, with rise times varying from 800 ns to 3.5 μ s and frequencies between 0.1 to 2 kHz. A current limiting resistor was incorporated in series with the output, and a capacitor was connected in parallel to the load to control the pulse slew rate.

Square pulses were utilized to study motor insulation in [62], [63]. In [62] two generators were used to achieve rise times between 200 ns and 400 μ s. The first generator was IGBT-based, generating pulses with 200 ns to 1 μ s rise times, and the second one was a Trek 30/20 high voltage amplifier, generating pulses with rise times greater than 16 μ s. In [63], bipolar 16 kV pk-pk pulses were generated, having either negative or positive values without a zero-volt level, with the fastest rise time recorded at 2 μ s.

Hairpin winding samples were tested using pulses generated by SiC-MOSFETs in [54]. The generator employed a simple bridge structure consisting of a DC voltage source in parallel with a capacitor and two switches. The pulse generation procedure for motor insulation testing is similar in [22], [64], [65], [66]. Multiple switches are used in these works for pulse generation, and various resistors are used to control pulse rise time. Additionally, multiple input voltage sources are used to generate multilevel waveshapes.

A robust IGBT-based modular unipolar HV pulse generator has been developed at the HV engineering laboratory at the University of Waterloo for testing medium and HV motor insulation systems [67]. This topology allows for adjustments to voltage amplitude, frequency, and duty cycle, but control over rise time or overshoot requires external resistors or capacitors. While this generator can produce unipolar square pulses and PWM voltage waveforms, it lacks the capability to generate multilevel waveforms. An IGBT-based unipolar/bipolar square pulse generator was implemented in [68], [69]. This design features two capacitors, two switches, and a manual switch to toggle between

unipolar and bipolar modes. In bipolar mode, the output alternates between positive and negative values without a zero-voltage period.

Table 2.3 Comparison between the proposed topology and 15 other pulse generation topologies used in the literature.

Reference	WBG device-based	Type of Switch	Rise Time	Overshoot	Multilevel Output	Bipolar Output	No. of V_{in}	Modular
[22]	No	Push-Pull	Yes*	Yes*	No	Yes	2	Yes
[54]	Yes	SiC-MOSFET	Yes*	Yes*	No	No	1	No
[55]	No	Push-Pull	Yes*	Yes*	No	Yes	2	No
[56]	No	Push-Pull	Yes*	Yes*	No	Yes	2	No
[57]	No	IGBT	Yes*	Yes*	No	Yes	1	No
[58]	No	Semiconductor Switch	Yes*	Yes*	No	No	1	No
[59]	No	Semiconductor Switch	Yes*	Yes*	No	No	1	No
[60]	No	-	Yes*	Yes*	No	Yes	1	No
[61]	No	IGBT	Yes*	Yes*	No	Yes	2	No
[62]	No	IGBT	Yes*	Yes*	No	Yes	2	No
[63]	No	Push-Pull	Yes*	Yes*	No	Yes	1	No
[64]	No	Push-Pull	Yes*	Yes*	Yes	Yes	Multiple	Yes
[65]	No	Push-Pull	Yes*	Yes*	Yes	Yes	Multiple	Yes
[66]	No	Push-Pull	Yes*	Yes*	Yes	Yes	Multiple	Yes
[67]	No	IGBT	Yes*	Yes*	No	No	1	Yes
Proposed	Yes	SiC-MOSFET	Yes	Yes	Yes	No	1	Yes

* The variable parameter is available only by having extra components (resistor and/or capacitor) connected to the circuit.

The summary of the pulse generation topologies in the literature is presented in Table 2.3. The proposed pulse generator in Chapter 4 is also included in this table to compare with the other pulse generation methods in the literature.

Duty cycle and frequency are not included in the table because the pulse generation methods in the studied articles can adjust these parameters with or without minor changes to their control circuits or topologies. Only [54] utilizes WBG device-based switching devices. Regarding rise time and overshoot control, some of the reviewed literature (Table 2.3) controlled the rise time and overshoot by using additional components (resistors and/or capacitors). Topologies used in [64], [65], [66] can generate multilevel pulses; however, these topologies rely on several input voltage sources to achieve multilevel output pulses.

2.3 Research Gap

The identified research gap from the literature is summarized below:

- There is a lack of a pulse generator based on WBG devices that provides control over the pulse parameters required for insulation testing studies, including voltage level, pulse rise time, overshoot, frequency, duty cycle, and waveshape.
- There is a lack of a proper test sample design for the turn-to-turn insulation of hairpin winding. Twisted pair wires are extensively used to study the turn-to-turn insulation of random-wound windings, but they do not represent the turn-to-turn stress of hairpin winding. A proper sample should be proposed to accurately replicate the turn-to-turn insulation of hairpin winding.
- The turn-to-turn insulation performance of hairpin winding under pulse stress has not been thoroughly studied. Specifically, the turn-to-turn insulation performance under PD activities has not been considered in the literature, although which is what the hairpin winding would be subjected to.
- There is no standard in the motor insulation of EVs using hairpin winding. The IEC 60034-18-41 standard discusses the random-wound windings with Type-I insulation, but it does not cover hairpin winding.

This research addresses these challenges by proposing an HV pulse generator based on WBG switching devices. The proposed pulse power supply offers flexibility in adjusting and investigating various pulse parameters critical to insulation studies. Furthermore, actual EV motor winding

conductors, in the form of enameled flat copper conductors, are utilized to examine the insulation properties of hairpin windings under WBG device-based-driven motor conditions. Using these flat conductors, a back-to-back sample configuration has been developed to evaluate the turn-to-turn insulation of hairpin windings. By integrating the proposed WBG device-based converter with actual EV motor winding conductors, this study aims to bridge the critical gap in understanding the behavior of turn-to-turn insulation in hairpin windings under the operation of WBG device-based drive and PD activities.

2.4 Thesis Objectives

The ongoing improvements to EVs have introduced a range of technological advancements, including the adoption of WBG semiconductor devices, hairpin-wound motors, and higher operating voltage. These innovations, while providing numerous benefits such as improved efficiency and reduced weight, also introduce significant challenges, particularly concerning the electrical insulation systems of motor windings. Based on the studied shortcomings in the literature, and the ongoing improvements in EVs, the goal of this thesis is to bridge the critical gap in understanding the effects of the PWM pulses generated by the WBG device-based drives on the turn-to-turn insulation of hairpin winding used in EVs. The objectives of the thesis are as follows:

1. To develop representative samples of hairpin winding turn-to-turn insulation to evaluate the effects of different WBG device-based drives' pulse parameters on their performance under PD activities.
2. To design and develop a WBG device-based HV pulse generator capable of generating pulses with variable pulse parameters, simulating the behavior of actual EV drives.
3. To analyze, compare, and characterize the impacts of different pulse parameters on turn-to-turn insulation performance. This includes identifying the effects of each parameter and exploring potential interactions between them.
4. To evaluate the effect of elevated temperature on hairpin winding. This includes studying the combined effects of electrical and thermal stress on the turn-to-turn insulation of hairpin winding.

Chapter 3

Materials and Methods

This chapter presents a detailed discussion of the methodology used to conduct this research. The details of sample preparation, experimental test setup, insulation performance measurements, test procedures, and design of experiments are discussed. The overall block diagram of the research methodology is presented in Fig. 3.1.

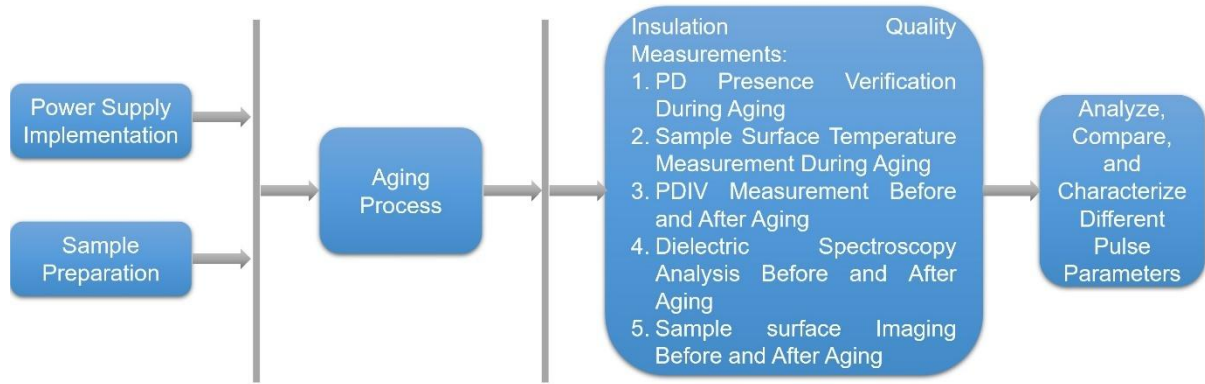


Fig. 3.1 Block diagram representing the overall research methodology.

3.1 Sample Preparation

The focus of this research is the turn-to-turn insulation of hairpin winding. The turn-to-turn insulation of hairpin winding is modeled with back-to-back samples, using flat enameled conductors. Previous studies have used tape to hold the wires together [17], [35], but this method may not provide sufficient stability to keep the wires in the correct position. Additionally, some studies have bent flat wires to investigate turn-to-turn insulation [19]; however, bending can damage the enamel coating, introducing defects that compromise the reliability of the insulation study. In other approaches, the flat wires were placed in a block [46], [50], but this method cannot ensure proper contact in the flat areas of the wires. To address the above-mentioned challenges and accurately model turn-to-turn insulation in hairpin windings, this work proposes an improved back-to-back sample preparation method. The improvements and preparation steps are detailed below.

The wires in back-to-back samples must be held tight in the flat contact area to ensure that no significant gaps exist between them. Initially, an aluminum holder was proposed to hold the wires (as

shown in Fig. 3.2 (a)), with the ends of the wires bent to keep them separated, similar to the design outlined in IEC 60034-18-42 [8] for back-to-back samples. However, the aluminum holder, being conductive, could get an unknown potential when the wires are energized under fast repetitive transients, which could affect the electrical stress during the aging process. Grounding the holder was considered as a solution to prevent it from floating, but this would increase the stress on the wire connected to the HV source, and it might affect the insulation quality measurements.

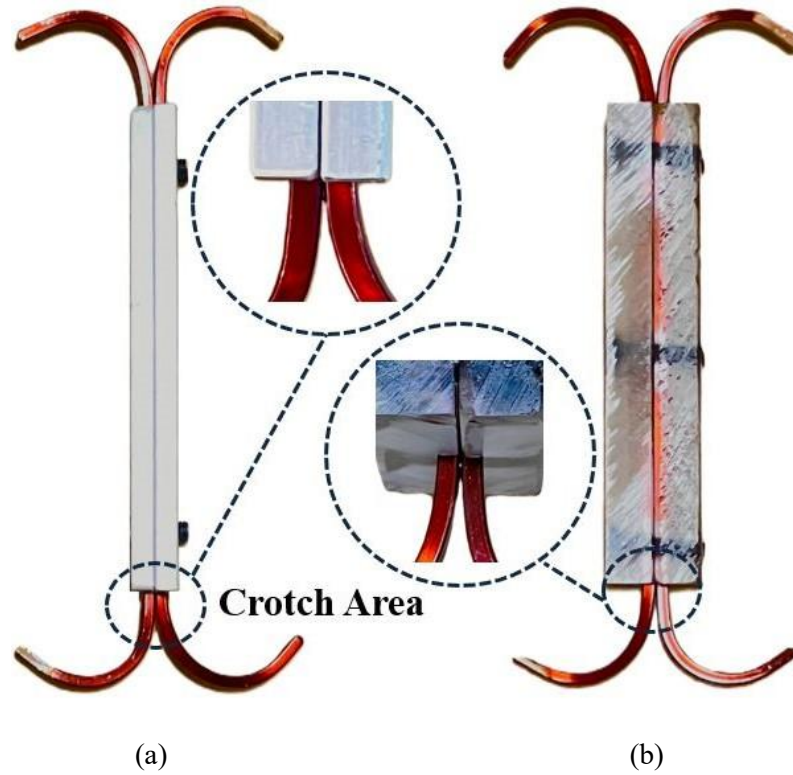


Fig. 3.2 The proposed sample improvements (a) the aluminum holder and (b) the plexiglass holder.

To address this issue, the aluminum holder was replaced with a polycarbonate plexiglass holder (as shown in Fig. 3.2 (b)). This holder is non-conductive and transparent, allowing for visual inspection of the samples during the aging process. Although this change resolved the conductivity issue, the wires were still bent at the ends, leading to corona activities at the crotch area. The presence of corona in this region can degrade the insulation, causing the sample to fail within hours and making it impossible to conduct prolonged aging tests. Multiple attempts were made to fill the crotch area and eliminate the high-field region, using materials such as silicone, resin, and vacuum pressure impregnation (VPI), as

shown in Fig. 3.3 (a) and (b), but none of them provided a consistent solution. Additionally, submerging the entire sample in oil successfully mitigated the crotch area issue, but the oil penetrated between the wires, introducing an additional insulating material that altered the turn-to-turn enamel insulation characteristic of the Type-I insulation system.

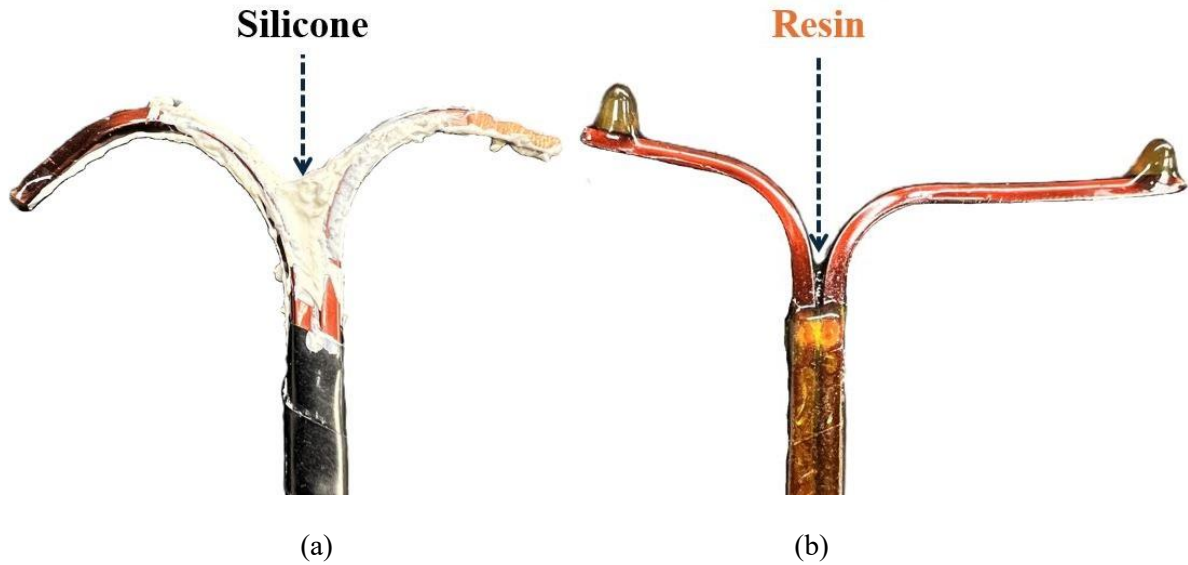


Fig. 3.3 The proposed sample improvements: crotch area filled with (a) silicone and (b) resin in the VPI process.

Finally, the wires were kept straight, without bending the ends, and a thin layer (0.3 mm) of 3M Scotch Self-Fusing Silicone Rubber Electrical Tape 70 was applied only in the crotch area to resolve the corona problem. This approach consistently addressed all the previously mentioned issues, and additional improvements were implemented. After cutting the wires, the enamel coating was removed from one end to allow for the connection of HV and ground connections. All sharp edges were smoothed, and the opposite end of the wire, which was not connected to any terminals, was covered with silicone glue to prevent potential partial discharges. This was confirmed by examining the smoothed areas with a corona camera to ensure there were no discharges. The wire length was set to 15 cm, while the holder length was 10 cm. To ensure precision and consistency, all wire holders were fabricated using a computer numerical control (CNC) machine. Each holder was equipped with six screws, ensuring that the wires were evenly held along the entire 10 cm flat contact area. Using this sample design, turn-to-turn insulation can be effectively studied without encountering issues related to corona in the crotch area or wire bending issues. The proposed sample is illustrated in Fig. 3.4.

Two types of wires are used in this study: corona-resistant (CR) and non-corona-resistant (NCR). Both wire types are the actual wires used in the 400 V hairpin stator winding of EVs. The CR wires have dimensions of 2×2.4 mm, with an enamel coating consisting of three layers of polyamide-imide, where the middle layer is a corona-resistant material. The NCR wires have dimensions of 2×3.5 mm and feature a dual coating of polyester and polyamide-imide, without any corona-resistant material.

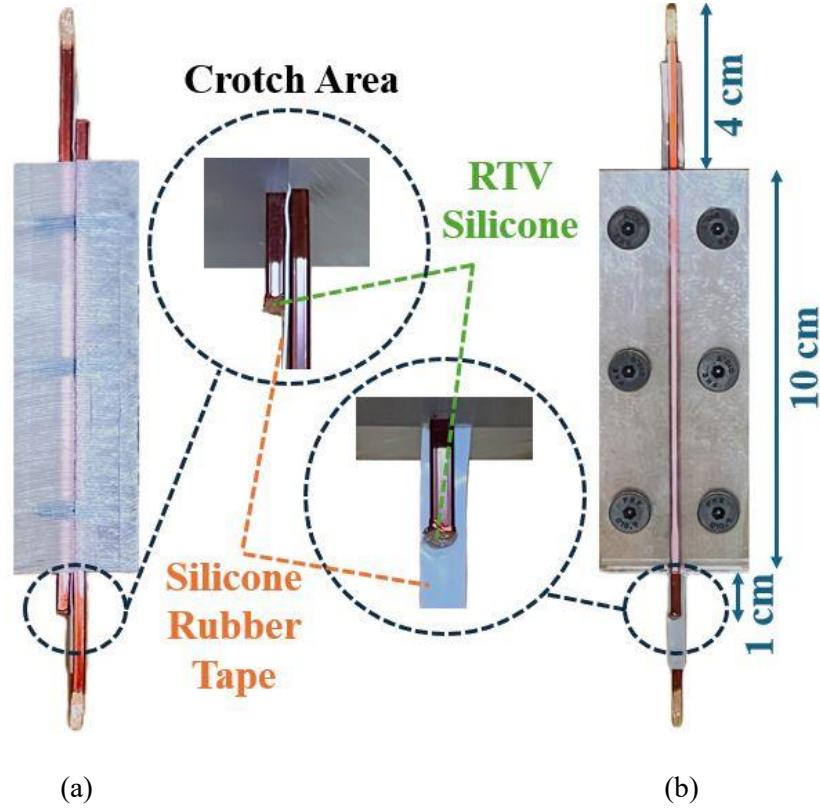


Fig. 3.4 The proposed sample (a) the side view of the holder and (b) the front view of the holder.

3.2 Experimental Test Setup

The experimental test setup is illustrated in Fig. 3.5. An SiC-MOSFET-based HV pulse generator is employed to study the effects of WBG device-based power converters on motor insulation in EVs [70]. This generator is capable of producing HV pulses with adjustable pulse amplitude, frequency, duty cycle, rise time, and overshoot. Additionally, it can generate both unipolar rectangular pulses and multilevel pulses (up to five levels). The details of the power supply are discussed in the next chapter. For the aging tests, a modified version of the generator described in [70] is used, incorporating the MSC400SMA330B4 SiC-MOSFET, which has a blocking voltage of 3.3 kV, a rise time of 8 ns, and a

turn on delay time of 16 ns. Unipolar pulses are selected for the aging tests because unipolar pulses cause higher damage to the insulation than the multilevel waveforms and bipolar pulses [69].

To monitor the surface temperature of the samples during the aging process, a FLIR T650sc infrared (IR) camera is employed. PD signals are captured using an A-INFOMW octave horn antenna (Model: LB-OH-650-15-C-NF), which is connected to a Rohde and Schwarz (R&S) oscilloscope with a 2 GHz bandwidth and a sampling rate of 10 GS/s. Voltage waveforms are periodically recorded throughout the aging period to ensure that the pulse parameters remain stable. A Tektronix P6015A HV probe is used to measure the voltage waveforms, and these measurements are taken using a Tektronix MDO3024 oscilloscope, which has a 200 MHz bandwidth and a sampling rate of 2.5 GS/s.

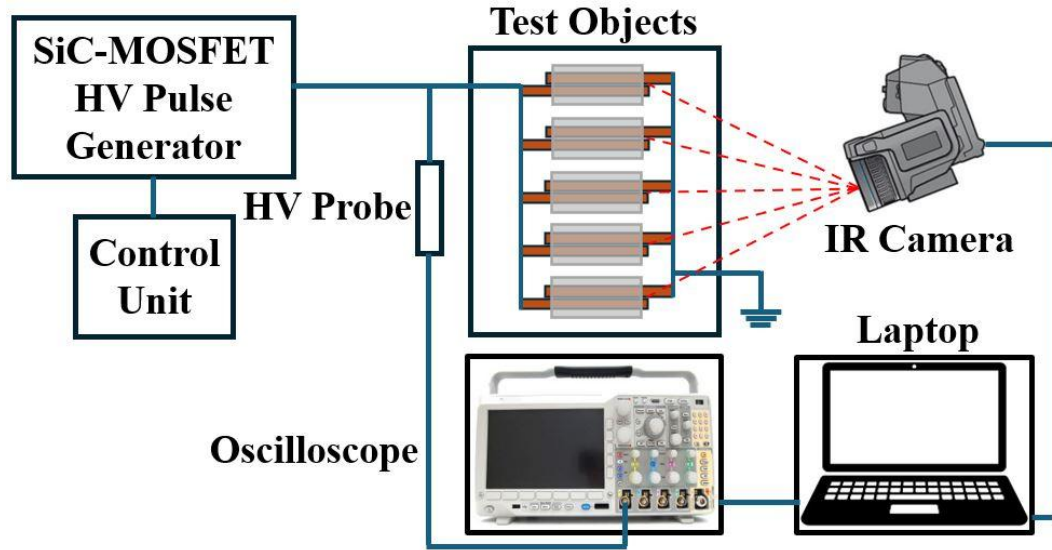


Fig. 3.5 The experimental setup used for aging the back-to-back samples.

3.3 High Temperature Tests

Temperature is a critical factor influencing motor performance, directly affecting efficiency and reliability. In EV applications, where compactness is essential, the impact of thermal stress becomes even more pronounced. EV motors operate at high temperatures, typically ranging from 50 to 130 °C [71], [72], [73], [74], [75], [76], depending on motor size, cooling system efficiency, and operating conditions. The heat generated during operation significantly affects the integrity of the insulation system, particularly under combined thermal and electrical stress.

To assess the impact of simultaneous thermal and electrical stress on insulation degradation under PD activity, aging tests were conducted using an INTBUYING 101-2AB forced-air convection drying oven. This oven provides a temperature range from ambient +10°C to 250°C, with a maximum temperature of 300°C and a fluctuation of $\pm 1^\circ\text{C}$. A hot air circulation system ensures uniform temperature distribution, minimizing temperature gradients among samples. Several tests were conducted at different temperatures, and it was found that at 100 °C, noticeable damage occurred at 2.5 kV pulses. Therefore, 100 °C was selected for the combined thermal and electrical aging tests.

3.4 Insulation Performance Measurements

In this study, PDIV measurements and dielectric frequency response (DFR) analysis are used to evaluate the aging effect on the insulation performance of the samples before and after the aging tests. The Omicron PD measurement setup, MPD 600, equipped with a 1 nF coupling capacitor, is utilized to measure the PDIV values. These measurements are performed using a 60 Hz ac voltage waveform. The specifications of the PD measurement system are summarized in Table 3.1. Additionally, the percentage dissipation factor (%DF) and capacitance (C) are analyzed through DFR analysis using the Megger IDAX-300 instrument. The DFR measurements setup for the un-grounded specimen test (UST) is shown in Fig. 3.6. The DFR analysis is conducted over a frequency range from 1 kHz down to 0.1 Hz at a voltage level of 140 V_{rms}. Optical microscopy, atomic force microscopy (AFM), and scanning electron microscopy (SEM) images were employed to examine the enamel insulation changes on the wires. An Olympus optical microscope was used to capture microscopic images, and the Redux AFM was used to get the AFM images.

Table 3.1 Omicron PD measurement system specifications.

Designation	Model
PD measuring device	MPD 600
PD measuring device power source	MPP 600
Impedance measuring unit	CPL 542
Control unit	MCU 502
Charge calibrator	CAL 542
Coupling capacitor	MCC 210L

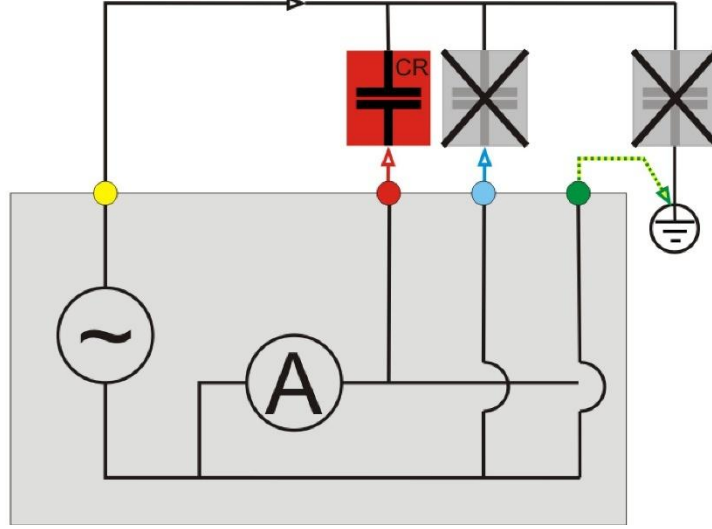


Fig. 3.6 DFR measurement setup for the un-grounded specimen test.

3.5 SEM Analysis

Scanning electron microscopy (SEM) is employed to characterize the morphological changes in the samples. Microstructural observations are obtained using an FESEM ZEISS Sigma 300 machine, which is equipped with an EDX detector to facilitate elemental composition analysis via energy-dispersive X-ray spectroscopy (EDS/EDX). The SEM is operated at an acceleration voltage range of 1 - 10 kV in high-vacuum mode to optimize imaging conditions and resolution.

To mitigate the charging effects inherent to insulating samples, a thin gold coating (10 nm thick) is deposited on the specimen surfaces using a sputtering technique before imaging. This conductive layer improves image quality and prevents surface charge accumulation.

3.6 Test Procedures

To evaluate the impact of WBG device-based power converters on the turn-to-turn insulation of hairpin winding, the prepared samples were subjected to 24 hours of aging under electrical stress at room temperature. In each sample, one wire was connected to the HV source and the other to the ground, simulating the worst-case scenario. For each experiment, five samples were connected in parallel to ensure conclusive results. The PDIV and DFR measurements were taken from all the samples before aging, to make sure all the samples exhibited similar characteristics. This quality assurance process enhances the reliability and validity of the research findings, allowing for meaningful comparisons and analysis between the different samples.

Insulation performance measurements, including PDIV and DFR, were conducted prior to the start of the aging process and repeated 24 hours after de-energizing the samples. This de-energizing period allowed the samples to stabilize and mitigate the residual charge, ensuring accurate measurements [34].

3.6.1 PD Measurement

The samples were aged in the presence of PD activities, which was verified by capturing the electromagnetic emissions from the PD signals using the antenna. The antenna was used solely to confirm the presence of PD activity during aging and not to characterize PD signals with varying pulse parameters. The antenna has a 1-2 GHz bandwidth, with a corresponding gain of 15 dB within a one-meter distance. According to a similar work on back-to-back sample studies under HV pulses [77], it was observed that the PD signals were in the range of 1-1.8 GHz.

The antenna will capture all the signals in the bandwidth range. To ensure that the captured signals by the antenna are specifically related to the PD occurring in the samples and not influenced by other sources, certain considerations and verification steps are necessary. The electromagnetic waves emitted by the power supply and any discharges in the air at the crotch area have a lower frequency compared to PD activities in the region between the two enamel wires. These low-frequency signals were filtered by post-processing filtering using MATLAB software. Furthermore, the directional feature of the horn antenna was also considered to minimize the potential interference from the power supply. The captured signals were transmitted by a flexible RG 142 double-shielded coaxial cable with a 50 Ω impedance for its excellent shielding properties to minimize any external interference.

The use of fast rise-time pulses generated by WBG device-based pulse generators may interfere with the electromagnetic waves emitted by PDs. Therefore, studies considering PD behavior characterization should consider specific approaches to eliminate the fast rise time effect on the captured electromagnetic signals [78].

3.6.2 Temperature Measurement

During the aging tests, the surface temperature of the samples at the wire holder exit area (as circled in Fig. 3.4 as the crotch area) was continuously recorded. The actual temperature of the wires within the holder could not be accurately measured because the wires are held by polycarbonate plexiglass, which does not let the IR camera capture the actual reflected temperature of the wires within the holder. To validate the accuracy of the IR camera measurements and ensure proper calibration (emissivity), a

controlled experiment was conducted, as illustrated in Fig. 3.7. In this experiment, the surface temperature of the same wire was simultaneously measured using both the IR camera and a thermocouple to verify the accuracy of the IR camera readings. Different emissivity values of the IR camera were tested (as per the suggestions of the manual of the camera: 0.85 – 0.95), and the results are presented in Table 3.2. The emissivity of the IR camera is set to 0.95 based on the conducted controlled experiment results, the IR camera manual, and reference [79].

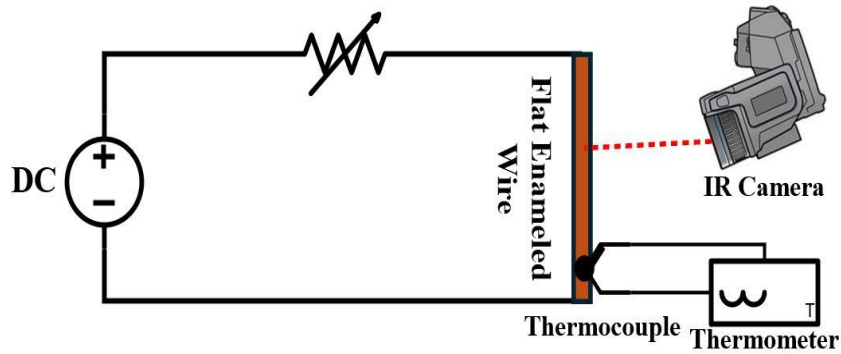


Fig. 3.7 The controlled experiment setup to calibrate and validate the IR camera settings.

Table 3.2 The temperature measurement results for the controlled experiment with different emissivity values.

Parameter	Thermocouple (°C)	IR Camera (°C)
Emissivity		
0.85	23.5	24.7
0.9	23.5	24.1
0.95	23.5	23.5

By using the IR camera, the temperature of the samples can be monitored during various stress conditions, such as the application of different pulse parameters. This enables the exploration of any potential correlation between temperature variations and the different pulse parameters applied to the samples. Analyzing this correlation provides valuable insights into the influence of pulse parameters on the sample's temperature behavior, contributing to a better understanding of the thermal effects in the insulation system.

3.6.3 Test Voltage and Duration

The average PDIV of the samples was measured at about 900 V_{rms} using the MPD 600 PD measurement setup. From the rms voltage value, the peak-to-peak voltage was calculated to be approximately 2.55 kV. Additionally, the PDIV of the samples was measured under pulse voltage by capturing electromagnetic waves using the antenna. These measurements revealed that the PDIV under pulse voltage ranged between 2.3 and 2.4 kV.

Extensive experiments were conducted to determine the appropriate voltage for aging tests, a voltage high enough to induce PD activity for effective aging but not so high as to cause failure of the samples within the aging period. The voltage range considered for these tests was between 2 kV and 3 kV. After various trials, 2.5 kV pulses were identified as the optimal voltage level for aging the samples under PD activity without causing unintended sample failure.

For the aging test duration, experiments were conducted over periods ranging from 1 to 3 days. Two types of wires were investigated in this study: corona-resistant and non-corona-resistant wires. The non-corona-resistant wires exhibited shorter endurance times, often failing after one day of exposure to 2.5 kV pulses at 5 kHz frequency. This endurance was further reduced under conditions of higher electrical stress, such as faster rise time, increased switching frequency, overshoot, or duty cycle. Conversely, the corona-resistant wires demonstrated greater durability, sometimes withstanding more than two days under the same conditions considered for the non-corona-resistant wires. However, even the corona-resistant wires failed within one or two days when subjected to higher electrical stresses.

In this work, various electrical stress conditions with different pulse parameters are tested on the samples, and the results are compared between the corona-resistant and non-corona-resistant wires. A 24-hour test duration was selected for aging experiments, as it provided a balance between inducing significant aging under PD activity and maintaining sample integrity for a comparative analysis of insulation performance on both wire types.

3.6.4 Tests with Failed Samples

In some experiments, samples failed before the completion of the intended 24-hour aging test, triggering automatic termination of the test. In such cases, the experiment was excluded from the dataset, and the same test was repeated under identical conditions until the 24-hour aging test could be successfully completed without sample failure.

3.7 Design of Experiments

The purpose of this work is to characterize the impacts of the different pulse parameters of the WBG device-based drives and to find the main factor affecting the turn-to-turn insulation performance. One of the primary methods used in designing tests to study a system is the one-factor-at-a-time (OFAT) approach. In this method, only one factor will change in each test, and the system's response will be evaluated under one parameter changing while all other parameters are kept constant. While widely used, this approach cannot capture interaction effects between factors, often leading to inaccurate conclusions [80].

Multiple factors are used in this research, and the OFAT approach is not an efficient way to design the experiments. A more effective strategy for experiments involving multiple factors is a statistically designed approach, such as factorial design. This method allows simultaneous, systematic variation of factors to evaluate their main effects and interactions. The 2^k factorial design is particularly notable, where each factor (k) is tested at two levels, typically denoted as “-1” (low) and “+1” (high). In this design, each factor's effect is assessed at varying levels of the other factors, effectively providing replicated responses without requiring additional observations. The main effect of each factor is determined by averaging the response values across different levels of other factors, yielding results applicable to a broader range of conditions [77], [81]. The 2^k factorial design method is used in this thesis to design experiments to systematically evaluate each parameter's effect and analyze the interactions between the factors.

Chapter 4

SiC-MOSFET High-Voltage Pulse Generator for Motor Insulation Testing

To replicate the effects of WBG device-based drives on motor insulation, an HV pulse generator based on WBG devices is necessary. An SiC-MOSFET-based pulse generator is proposed and developed to investigate the effects of WBG device-based converters on motor insulation in EVs [70]. The converter is designed and optimized to meet the required specifications that are needed for replicating various scenarios encountered in EV applications. Both rectangular and multilevel pulses can be generated with the proposed topology. Pulse rise time is an important factor in motor insulation studies, especially by introducing WBG devices, which have very fast rise times (even less than 10 ns). The proposed converter can change pulse rise time by shifting the switches' gate signals and inserting each module in the discharge stage stepwise. The variable pulse rise time is achieved through the control system, not by adding extra components to the circuit, which is advantageous [31], [67]. Controlling overshoot is another important aspect of motor insulation evaluation, and this converter addresses this by sequentially inserting modules into the discharge mode. The pulse duty cycle is variable, allowing for the investigation of different pulse duration effects. The pulse frequency is determined by the switching frequency of the circuit and can be adjusted accordingly. Additionally, the pulse amplitude can be varied to observe the impact of the voltage amplitude on the insulation system. The performance of the converter is validated through MATLAB Simulink simulations and experimental results.

4.1 Pulse Generating Module

The proposed HV pulse generator module is demonstrated in Fig. 4.1. Each module consists of a capacitor, a diode, and two switches. The diode and S_c switch are used to charge the capacitor to the input voltage, V_{in} . On the other hand, the S_d switch is employed in discharge mode to generate pulses at the load.

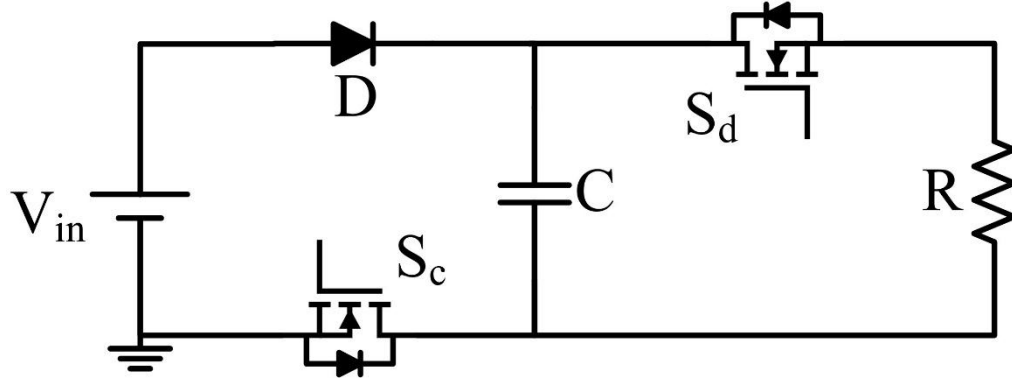


Fig. 4.1 Pulse generating module.

4.2 Generator Modular Topology

The schematic of a 5-stage modular generator is depicted in Fig. 4.2. There are 5 similar modules used to reach the theoretically desired output voltage amplitude $5V_{in}$ and up to 5 voltage levels in the output waveform. In order to ensure safety, the first module is designed without a charge switch, maintaining a continuous ground connection between the load and the input voltage source. The charging and discharging switches, S_c and S_d operate in a complementary manner to prevent any short circuits. Additionally, each module is connected to a wave-shaping resistor (R_i). The modular design can have n modules, and considering the overall component count for an n module configuration with an nV_{in} output voltage amplitude, there are n capacitors, diodes, wave shaping resistors, and $2n-1$ switches. By utilizing n modules, it is possible to achieve up to n levels in the output waveform.

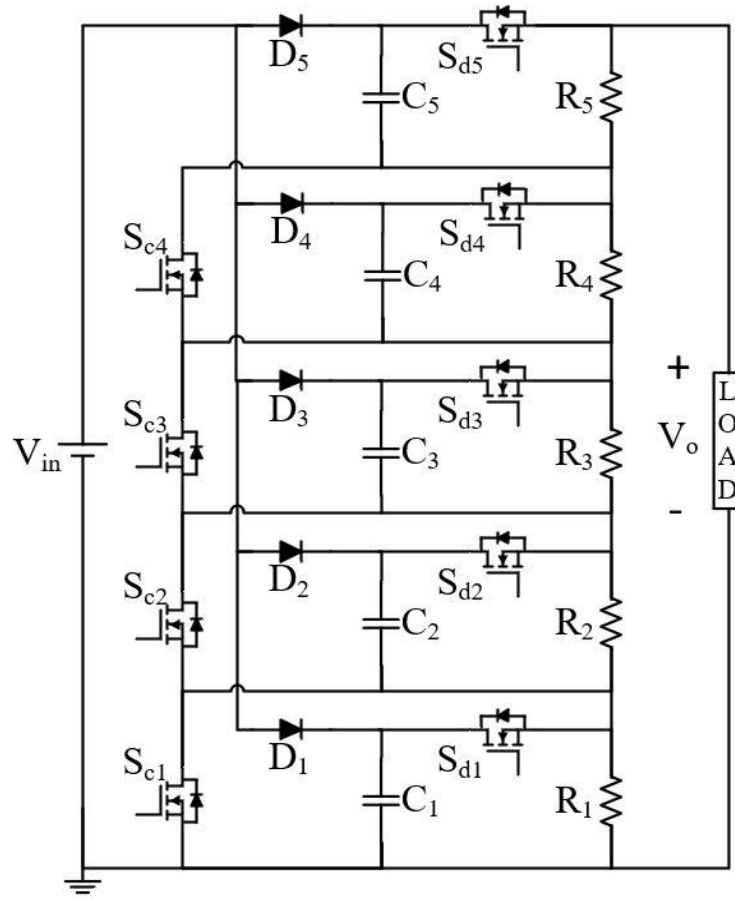


Fig. 4.2 Proposed modular topology.

Basically, there are two main operation modes for the proposed circuit. However, to have a better insight into its practical operation principles, four modes are discussed.

The charging mode, which is the first mode of operation (happening in the time period of t_1) is demonstrated in Fig. 4.3. In this mode, all the capacitors are simultaneously charged in parallel to the voltage V_{in} . In this mode, the diodes (D_1 to D_5) and the charging switches (S_{c1} to S_{c4}) are ON (the discharge switches (S_{d1} to S_{d5}) are OFF). The voltage stress of the discharging switches is the voltage of each module, which is equal to the input voltage. The voltage equations of the capacitors (V_{Ci}), the discharging switches ($V_{S_{di}}$), the charging switches ($V_{S_{ci}}$), the diodes (V_{Di}), the output of each module (V_{Ri}), and the output voltage (V_o) in the first mode are as follows. The on-state voltages of diodes and switches are assumed to be zero in circuit analysis.

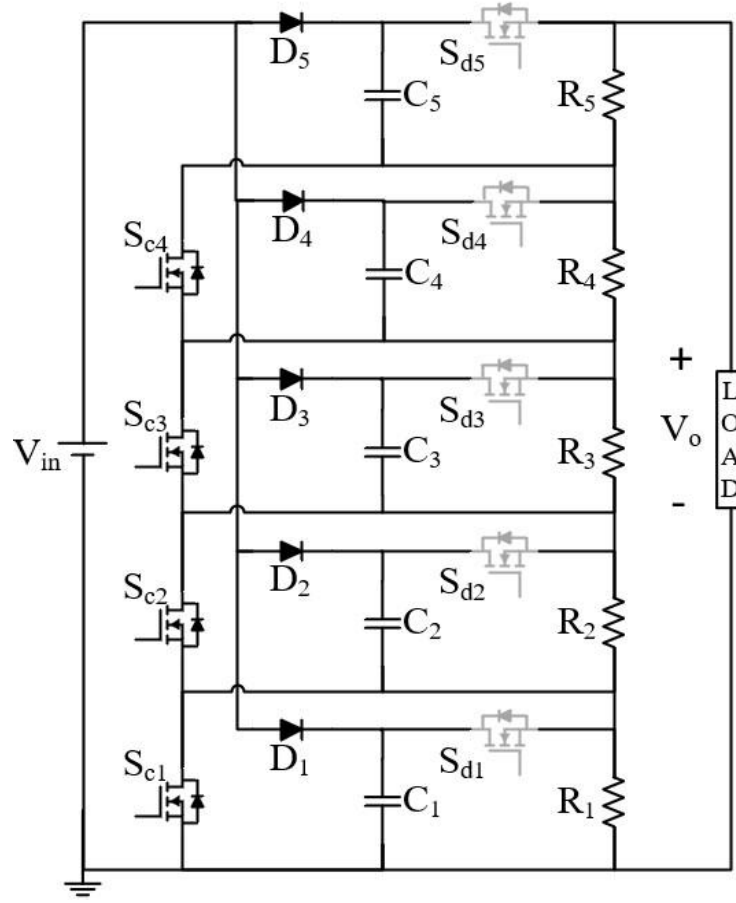


Fig. 4.3 The first mode of operation.

$$V_{c_i} = V_{in} \quad (1a)$$

$$V_{Sd_i} = V_{c_i} \quad (1b)$$

$$V_{Sc_i} = V_{D_i} = V_{R_i} = V_o = 0 \quad (1c)$$

The second operation mode, happening in the time period of t_2 , (shown in Fig. 4.4) is the idle mode of the circuit. A dead time is incorporated between the switching sequences of the charging and discharging switches. It is essential to prevent any simultaneous conduction of the charging and discharging switches, thereby avoiding potential short circuits. All the switching devices are OFF in this mode. The minimum delay time is determined by the characteristics of the gate-driver circuit and the time required for the switches to be fully turned ON and OFF. While the minimum delay time can be calculated based on the gate-driver circuit and switch dynamics, it can be extended beyond that to

maintain the circuit in idle mode, allowing for control of the pulse width. The voltage equations in this mode are as follows:

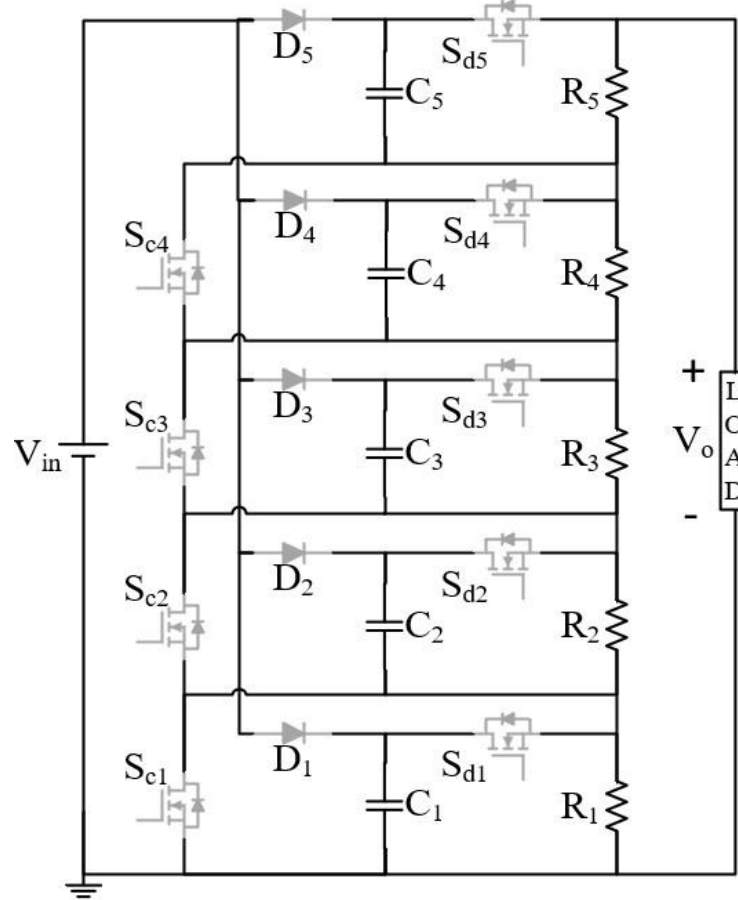


Fig. 4.4 The second mode of operation.

$$V_{Ci} = V_{in} \quad (2a)$$

$$V_{Sdi} = V_{Ci} \quad (2b)$$

$$V_{Sci} = V_{Di} = V_{Ri} = V_o = 0 \quad (2c)$$

The third mode of operation, happening in the time period of t_3 , is the discharge mode, which is presented in Fig. 4.5. In this mode, the discharge switches (S_{d1} to S_{d5}) will turn ON to connect the capacitors in series and generate the output HV pulses (charging switches (S_{c1} to S_{c4}) and the diodes (D_1 to D_5) are OFF). The series balancing issue of capacitors has been addressed by using the wave-

shaping resistors (R_i) as the resistive voltage dividers. The voltage equations in this mode are presented below.

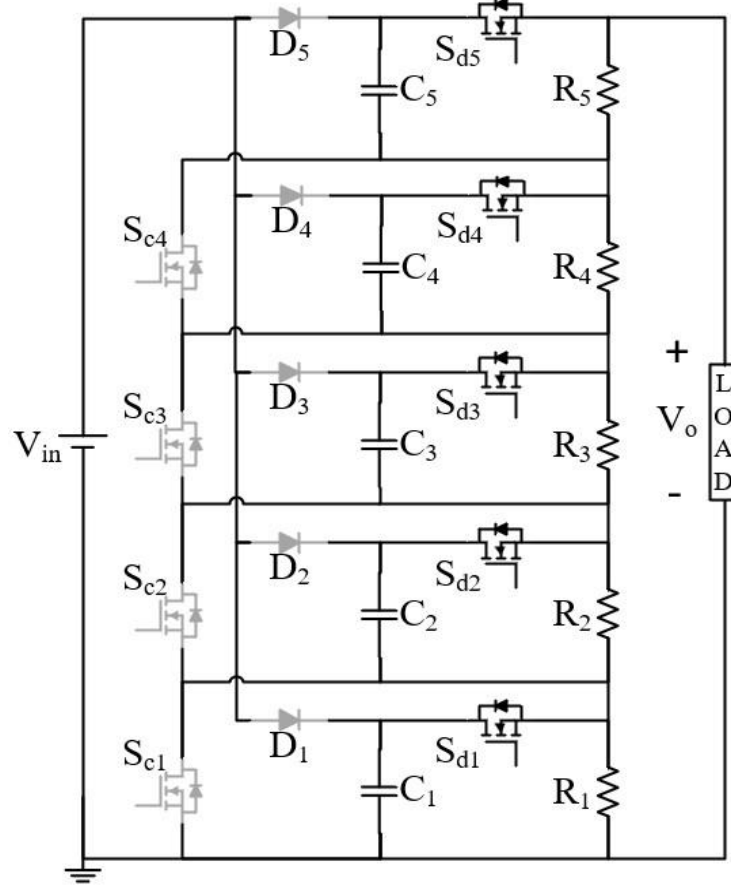


Fig. 4.5 The third mode of operation.

$$V_{c_i} = V_{in} \quad (3a)$$

$$V_{Sd_i} = 0 \quad (3b)$$

$$V_{Sc_i} = V_{c_i} \quad (3c)$$

$$V_{D_i} = -(i - 1)V_{c_i} \quad (3d)$$

$$V_{R_i} = V_{c_i} \quad (3e)$$

$$V_o = nV_{R_i} \quad (3f)$$

The fourth mode, happening in the time period of t_4 , is the same as the second mode shown in Fig. 4.4. The purpose of having this mode of operation and the voltage equations are the same as the second mode.

4.3 Control Signals

The control signals play a crucial role in controlling the dead time, rise time, frequency, duty cycle, overshoot, and wave shape of the pulses. The control signals for generating a rectangular waveform with the fastest rise time of this topology are shown in Fig. 4.6.

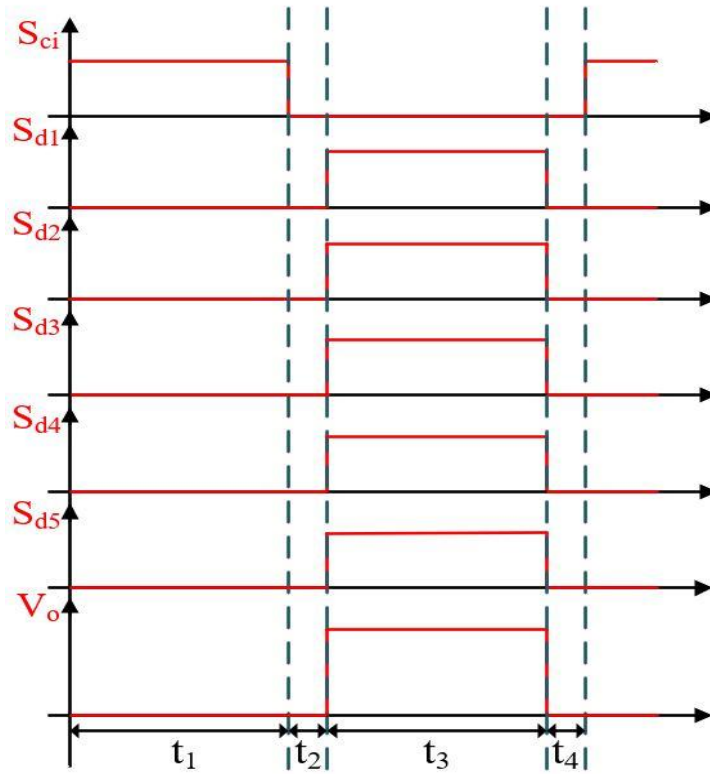


Fig. 4.6 Sequence of control signals for the fastest rise time.

A rectangular waveform with different rise times can be generated by using the control signals demonstrated in Fig. 4.7. while maintaining the necessary dead time to prevent short circuits. To achieve variable rise times, a pre-determined delay is set between the insertion of each capacitor into the discharge path. This delay can be implemented by sequentially adding each capacitor to the discharge path or by selectively including a desired number of modules in the discharge cycle while the remaining modules are added to the discharge sequence after a specific time interval.

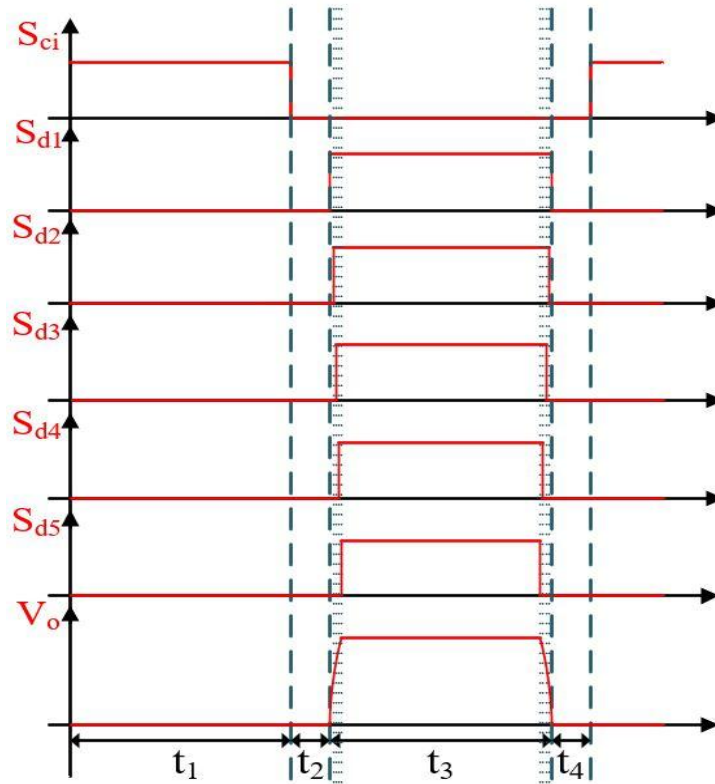


Fig. 4.7 Sequence of control signals for variable rise times.

A multilevel waveform can be generated by having a sufficiently long delay between the discharge signals applied to the discharge switches, as demonstrated in Fig. 4.8. It is not necessary for the delay times to be equal. The desired arrangement of delay times and levels in the output waveform is achievable. By having n modules in the structure, 1 to n voltage levels can be generated at the output.

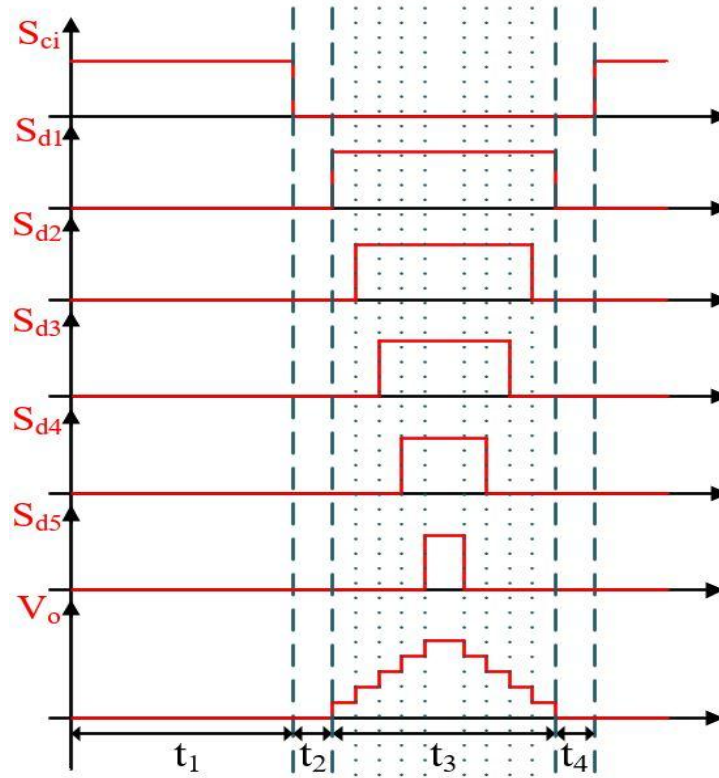


Fig. 4.8 Sequence of control signals for multilevel waveform.

4.4 Gate Driver Circuit

The switches used in this structure need isolated gate-source signals. The gate driver circuit is developed in this work, and the schematic of the gate driver system is shown in Fig. 4.9. The signals generated from the microcontroller are sent to optical isolation ICs through optical transmitters to reduce electromagnetic interference and electrical isolation between the drivers and the microcontroller. The optical isolation ICs' outputs are connected to the gate driver ICs to drive the switches. The gate driver boards are powered by DC sources with isolated grounds provided by isolation transformers. Also, to reduce the effect of common-mode noise, capacitive filters are used in the AC/DC converter. The gate drivers are located very close to the switches to minimize the wire length and stray inductance between the gate driver circuit and the switch.

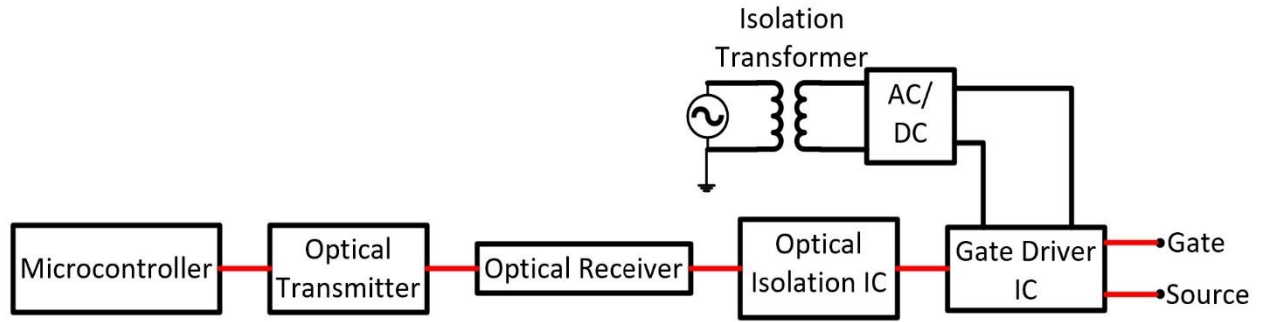


Fig. 4.9 The gate driver system schematic.

4.5 Design and Implementation Considerations

In this study, the target voltage of the power supply is set to a maximum of 3.2 kV, and to achieve this, a configuration with 5 modules has been employed. During motor operation, overvoltages up to two times the DC bus [2] or higher [6] can be generated on motor terminals. Considering the 400 V existing EVs and the 800 V future EVs, 3.2 kV pulses (4 times higher than the 800 V operating voltage) are considered as the maximum target output voltage. Based on the circuit analysis presented in Chapter 4, it has been determined that the maximum voltage across the switches is equal to the voltage of the capacitors, which is the same as the input voltage source. Using the voltage stress equations of the switches (4) and (5) and diode (6), suitable switches and diodes can be selected accordingly.

$$\hat{V}_{Sc_i} = V_{c_i} \quad (4)$$

$$\hat{V}_{Sd_i} = V_{c_i} \quad (5)$$

$$\hat{V}_{Di} = -(i - 1)V_{c_i} \quad (6)$$

The storage capacitors are usually chosen to be at least 10 times the load capacitance [55], [56]. In the case of twisted-pair and back-to-back motor insulation test samples (representing turn-to-turn insulation of random-wound and form-wound windings, respectively), the sample capacitance typically ranges from tens of pF to a few nF. To cover a wide range of motor insulation test sample loads, 10 μ F Metallized Kunststoff (plastic) Polypropylene (MKP) film capacitors with a rated voltage of 1.2 kV have been utilized. 5 k Ω EBG-UXP 600, low inductance resistors have been used as the wave-shaping resistors.

The gate driver signals are generated by the MSP-EXP430FR2355 microcontroller. SN75451BP dual-peripheral driver has been used as the buffer to intensify the signals and power the optical

transmitters. TLP-250 is connected to the optical receivers as the optical isolator ICs, and TD-351IN is used as the gate driver ICs to drive the MOSFETs.

For waveform acquisition, the Tektronix-P6015A HV probe is connected to the Tektronix-MDO3024 oscilloscope, which has a bandwidth of 200 MHz and a sampling rate of 2.5 GS/s.

The SiC-MOSFET, G3R160MT17D, is used in the modular topology with a 1700 V drain-source voltage. The rise time and turn-on delay time are 12 and 22 ns, respectively. The SiC Schottky diodes are GP3D005A170B with a 1700 V breakdown voltage.

4.6 Protection Circuit

Considering the nature of insulation tests, breakdown and short circuits during the tests are inevitable aspects that need to be addressed. Hence, a robust protection system has been incorporated to safeguard against load breakdown and short circuits. The protection schematic, depicted in Fig. 4.10, has been developed and extensively utilized in insulation tests for prolonged durations in the HV Engineering Lab at the University of Waterloo. This protection system is designed to promptly interrupt the input power supply and control circuit power in the event of a short circuit, thereby mitigating any potential hazards for both the operator and the circuit.

The current on the primary side of the transformer is measured using a current transformer (CT), and this signal is monitored by an adjustable current relay. The relay's current threshold can be set by the user. If the current drawn by the converter exceeds the preset limit, the relay activates the contactor to disconnect both the input power and the control circuit. To provide additional protection for both the circuit and the user, a fast-blow fuse is connected in series with the insulation sample. In the event of a failure, the fuse quickly disconnects the load from the generator.

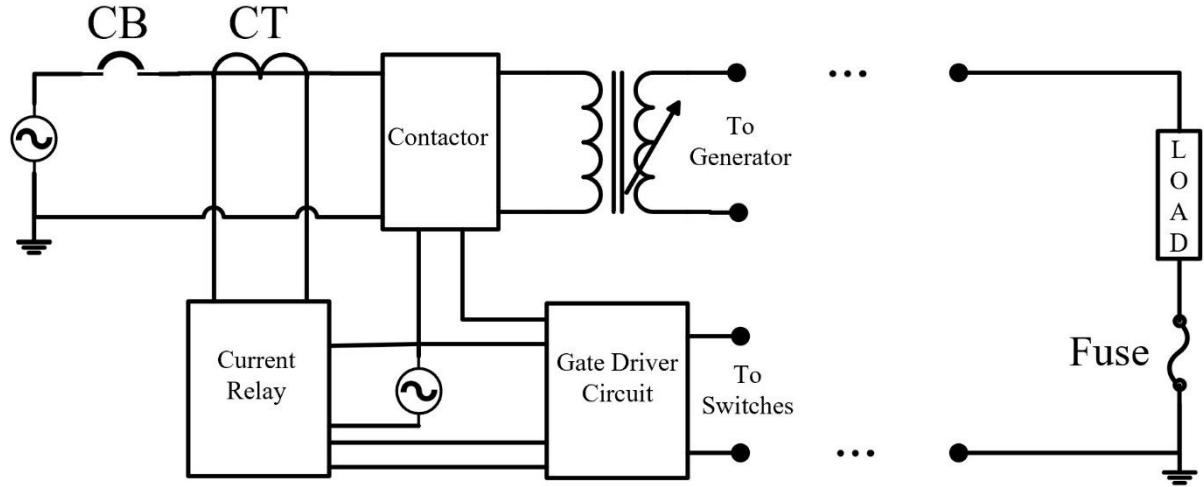


Fig. 4.10 The protection circuit schematic.

4.7 Simulation and Experimental Work

The proposed topology is simulated in MATLAB Simulink with the design considerations from the design section. Also, the proposed circuit is built and tested, and the circuit components' values for the simulation and experimental setup are presented in Table 4.1 and Table 4.2, respectively.

Table 4.1 Simulation parameters of the generator for 3.2 kV pulses.

Parameter	Value
Input DC voltage	$V_{in} = 640 \text{ V}$
Output pulse voltage	$V_o = 3.2 \text{ kV}$
Switching frequency	$f_s = 2 \text{ kHz}$
Pulse duty cycle	$t_3 = 18 \%$
Number of modules	$n = 5$
Wave-shaping resistors	$R_i = 5 \text{ k}\Omega$
C_i capacitors	$C_i = 10 \text{ }\mu\text{F}$

Table 4.2 Experimental parameters of the generator for 3.2 kV pulses.

Parameter	Value
Input DC voltage	$V_{in} = 640 \text{ V}$
Output pulse voltage	$V_o = 3.2 \text{ kV}$
Switching frequency	$f_s = 2 \text{ kHz}$
Pulse duty cycle	$t_3 = 18 \%$
Number of modules	$n = 5$
Wave-shaping resistors	$R_i = 5 \text{ k}\Omega$
C_i capacitors	$C_i = 10 \text{ }\mu\text{F (MKP)}$
SiC MOSFET	G3R160MT17D
SiC Diode	GP3D005A170B

4.7.1 Simulation Work

4.7.1.1 Output and Capacitors' Voltage Waveshape

The simulation results are presented in Fig. 4.11-Fig. 4.14. The rectangular 3.2 kV pulses are shown in Fig. 4.11. The pulse duty cycle is 18%, and the output of each module is 640 V on an open circuit. The capacitors do not completely discharge in the topology, and the voltage across the capacitors has a very low ripple, as shown in Fig. 4.11 (d). Each capacitor is charged to the input voltage source, which is 640 V. Both the charge and discharge switches have the same voltage stress, i.e., the capacitor's voltage, which is the same as the input voltage as shown in Fig. 4.12. According to (6), each module's diode has a different voltage stress. The voltage waveforms of the diodes are shown in Fig. 4.13.

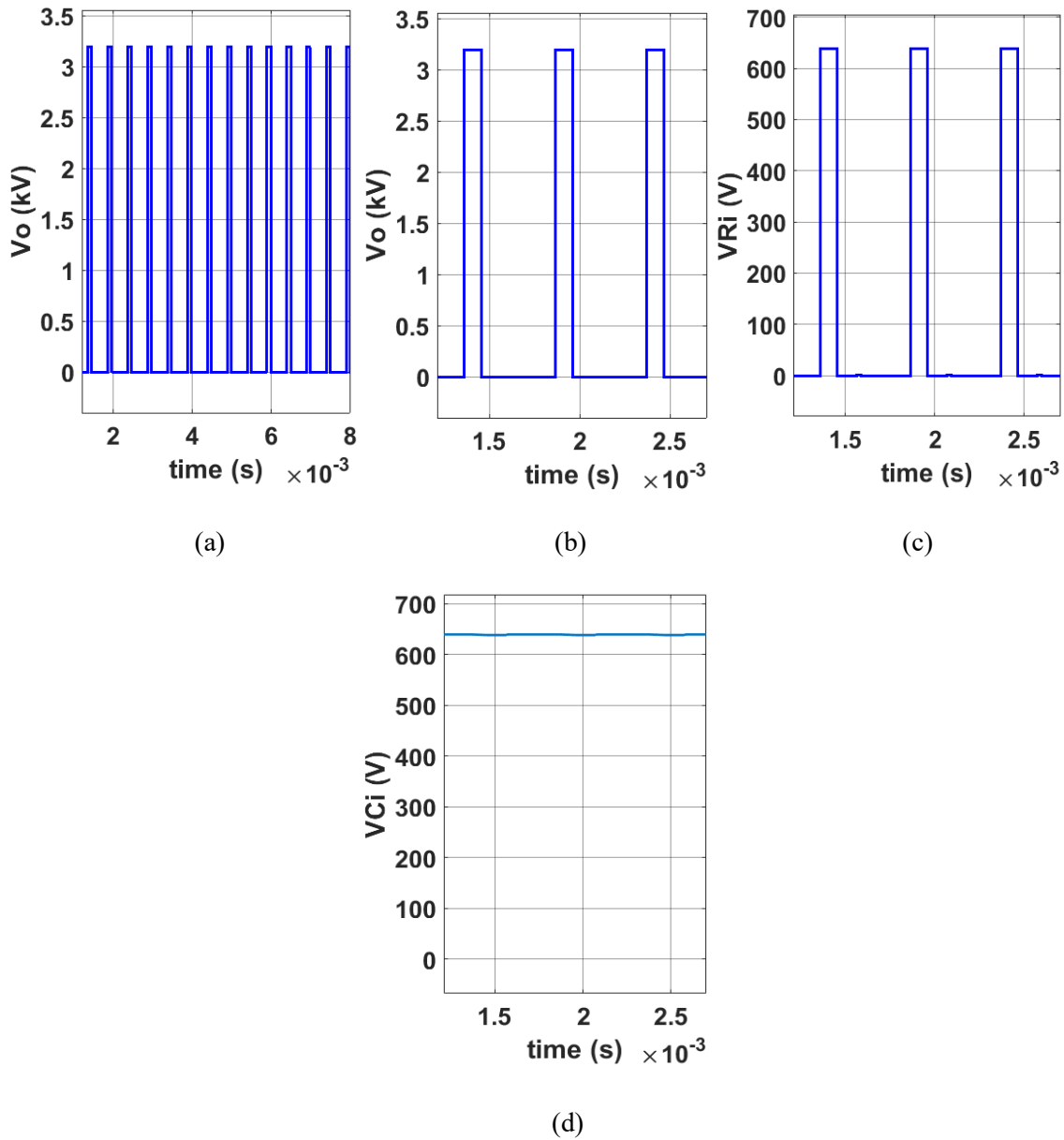


Fig. 4.11 Simulated voltage waveforms: (a) output 3.2 kV pulses, (b) zoomed view of 3.2 kV pulses, (c) output of each module, and (d) voltage across the capacitors.

Each module delivers 640 V to the output. 10 μ F capacitors have been used, and the wave shaping resistors' value is 5 k Ω . Looking at Fig. 4.11 (d), the capacitors' voltage is constant, and the capacitors do not discharge completely during the pulse generation period. This behavior is attributed to the interplay of several factors. The capacitors' large capacity, along with the relatively high resistance of the wave-shaping resistor and load resistance (which acts as a very high impedance, like an open

circuit), prevents significant discharge of the capacitors. As a result, the capacitors do not experience the typical charging and discharging cycles, leading to increased lifetime and reliability. In practice, there should be a little discharge, but due to the point that it is very negligible, it is ignored. Having a constant voltage across the capacitor and avoiding frequent charging and discharging cycles have a positive impact on the lifetime of the capacitors, the switches, and the diodes used in the converter. The extended lifetime of the converter can be attributed to the reduced stress on its components, such as having a constant voltage across the capacitors. This practice prevents switches and diodes from conducting high currents during each cycle, ultimately enhancing their reliability.

4.7.1.2 Switches' Voltage Waveshape

Voltage waveforms of the switches are demonstrated in Fig. 4.12. The voltage stress experienced by the charging switches is 640 V, and this stress is present during the pulse generation period only. On the other hand, the discharge switches also have a voltage stress of 640 V, but their stress is continuous, except during the pulse generation period. In other words, the discharge switches experience 640 V voltage stress throughout the non-pulse generation period.

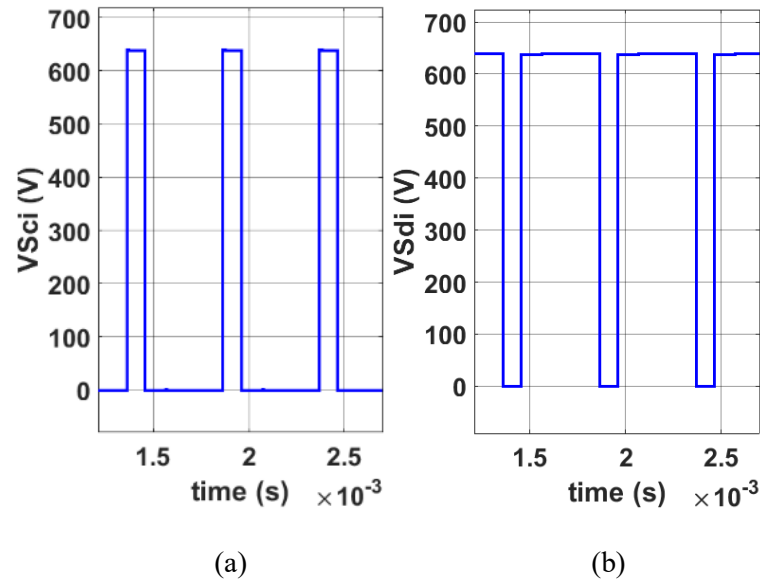


Fig. 4.12 Simulated voltage waveforms across: (a) charging switch and (b) discharging switch.

4.7.1.3 Diodes' Voltage Waveshape

As for the diodes, their voltage stress varies based on their stage number. Similar to the charging switches, diodes also experience voltage stress only during the pulse generation period.

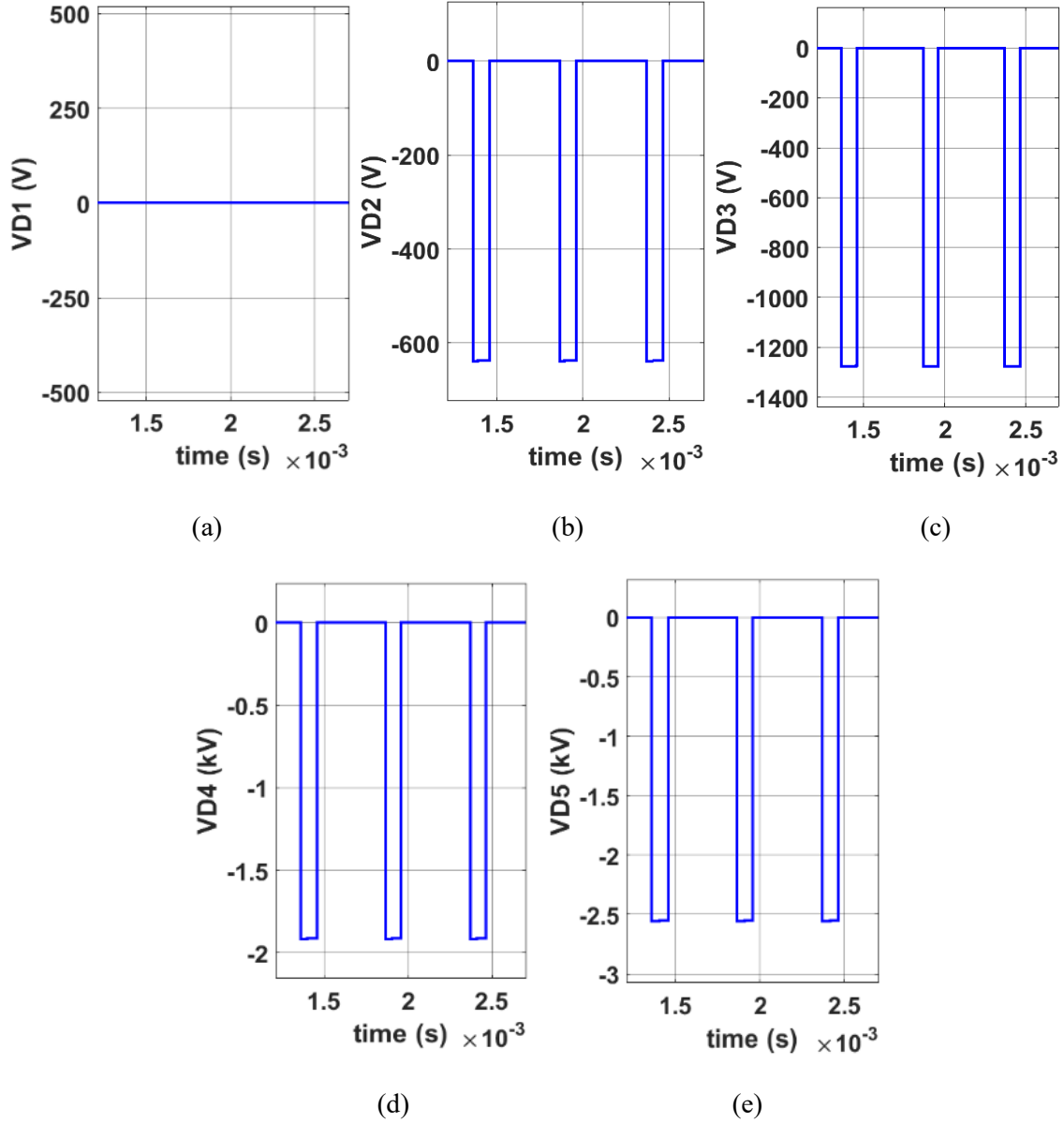


Fig. 4.13 Simulated voltage waveforms across the diodes: (a) D₁, (b) D₂, (c) D₃, (d) D₄, and (e) D₅.

4.7.1.4 Multilevel Output Voltage Waveshape

Multilevel waveforms can be generated up to 5 levels (without counting the 0-level). Different multilevel waveforms are shown in Fig. 4.14. The generation of these multilevel waveforms is achieved through the control signals depicted in Fig. 4.8. The control signals are responsible for coordinating the switching actions of the different modules within the converter. The capability to generate multilevel

waveforms is a valuable feature of the power converter, as it allows for a wider range of output voltage options and facilitates the emulation of various motor drives' operating conditions.

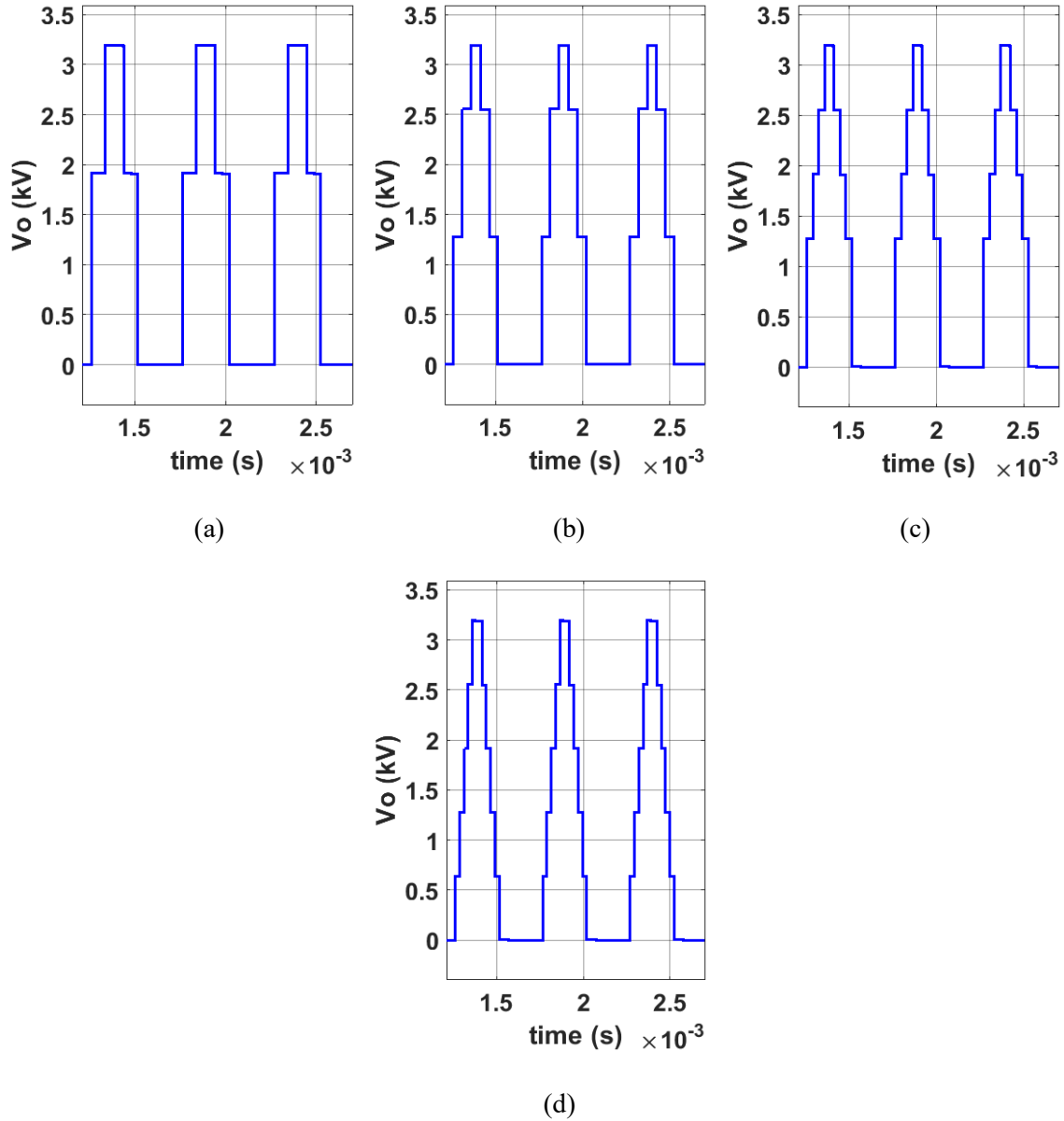


Fig. 4.14 Simulated multilevel voltage waveforms with: (a) 2-level, (b) 3-level, (c) 4-level, and (d) 5-level.

4.7.1.5 Loading Effect on the Generator Output

Simulated voltage waveforms, both with and without load, are illustrated in Fig. 4.15. The insulation samples are modeled by a parallel combination of a capacitor and a resistor. The output waveform

without any samples is demonstrated in Fig. 4.15 (a). The output waveform with a $1\text{ G}\Omega$ resistor in parallel with a 0.1 nF capacitor is depicted in Fig. 4.15 (b), and with a $1\text{ G}\Omega$ resistor in parallel to a 1 nF capacitor is depicted in Fig. 4.15 (c). It is observed that the output voltage level remains unaffected even with a 1 nF capacitive load. However, the fall time of the pulses can be affected by higher capacitance at the output side. These representations serve to visualize the impact of different resistor and capacitor configurations on the generated voltage waveshapes, giving insights into the system's behavior under varying load conditions.

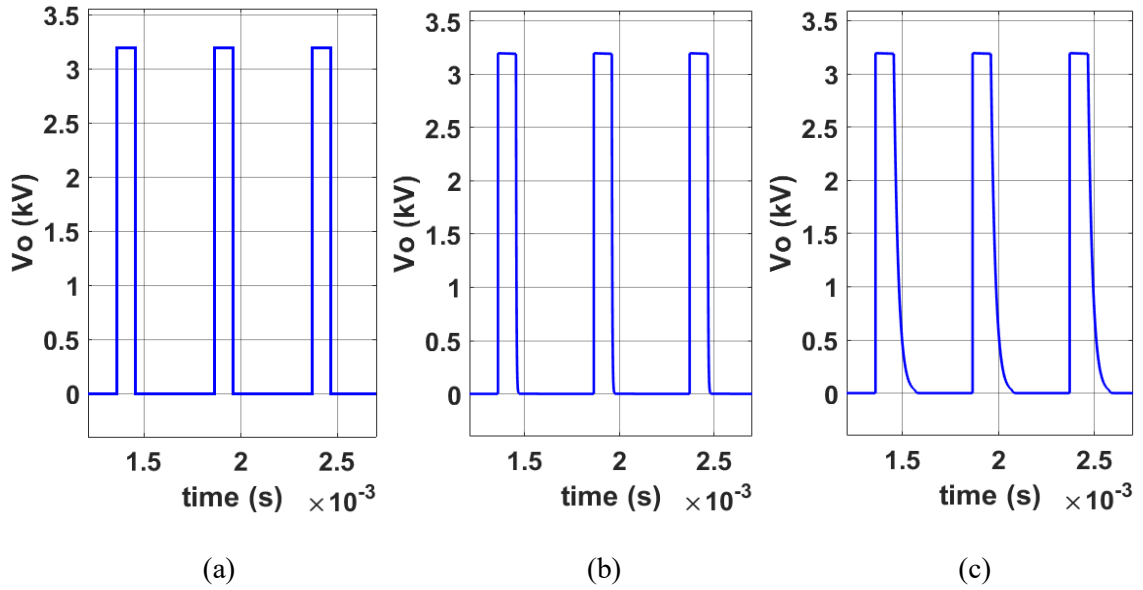


Fig. 4.15 Simulated voltage waveforms: (a) without load, (b) with 0.1 nF and $1\text{ G}\Omega$ load, and (c) with 1 nF and $1\text{ G}\Omega$ load.

4.7.2 Experimental Work

4.7.2.1 Experimental Setup

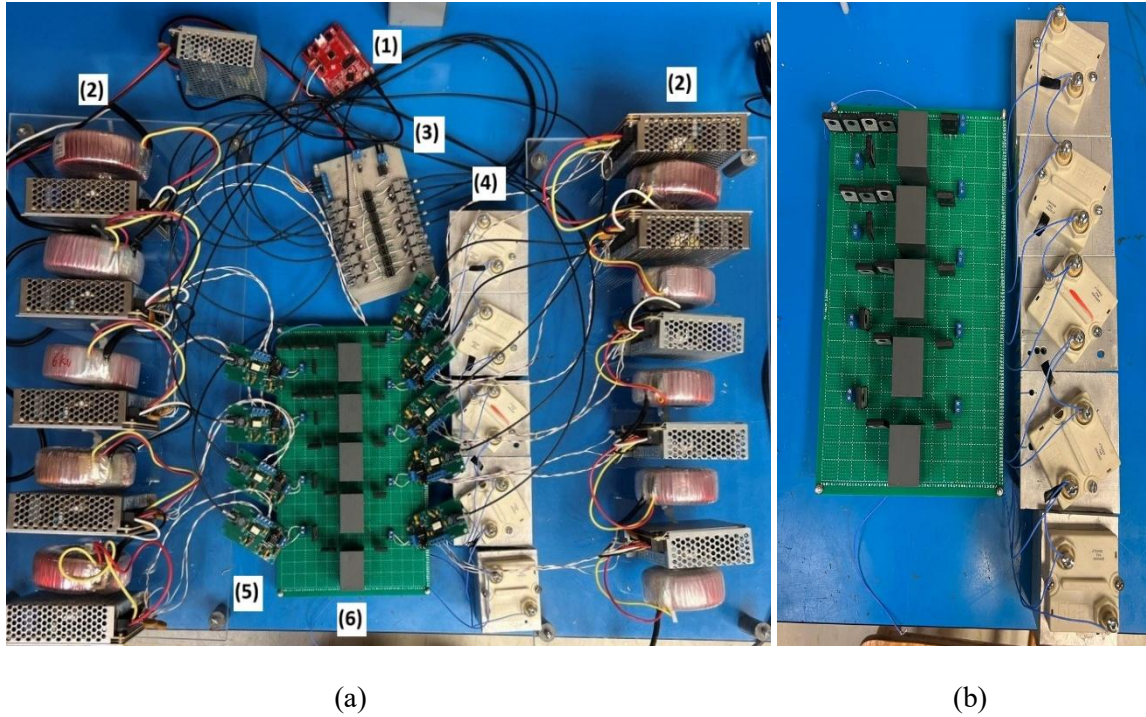


Fig. 4.16 Experimental setup: (a) the full modular pulse generator that includes: (1) microcontroller, (2) power sources for drive circuits, (3) buffer and optical transmitter board, (4) wave-shaping resistors, (5) drive circuit board, (6) modular HV pulse generator, and (b) the modular topology.

The experimental setup is shown in Fig. 4.16, which includes the control circuit, gate driver system, and the modular topology. The modular topology itself, without the control and gate driver circuit, is demonstrated in Fig. 4.16 (b).

4.7.2.2 Output and Capacitors' Voltage Waveshape

The measured experimental voltage waveforms are shown in Fig. 4.17 - Fig. 4.27. The 3.2 kV rectangular pulses with an open circuit output are shown in Fig. 4.17. The zoomed view of the rise time is shown in Fig. 4.17 (c), which is 66 ns. 5 modules are used to generate 3.2 kV pulses with 640 V input voltage. The output waveform of each module is demonstrated in Fig. 4.18 (a), which is the same as the simulated waveform (Fig. 4.11 (c)). The capacitors hold 640 V at each moment, as shown in Fig. 4.18 (b). As seen in Fig. 4.18 (b), the capacitors do not discharge considerably in each operating cycle, as mentioned earlier and depicted in Fig. 4.11 (d). Maintaining a constant voltage across the capacitors

mitigates frequent charge and discharge cycles, thereby extending the capacitors' lifespan. Additionally, it prevents high currents from flowing through the switches and diodes during each cycle. These factors collectively contribute to enhancing the overall lifetime and reliability of the converter.

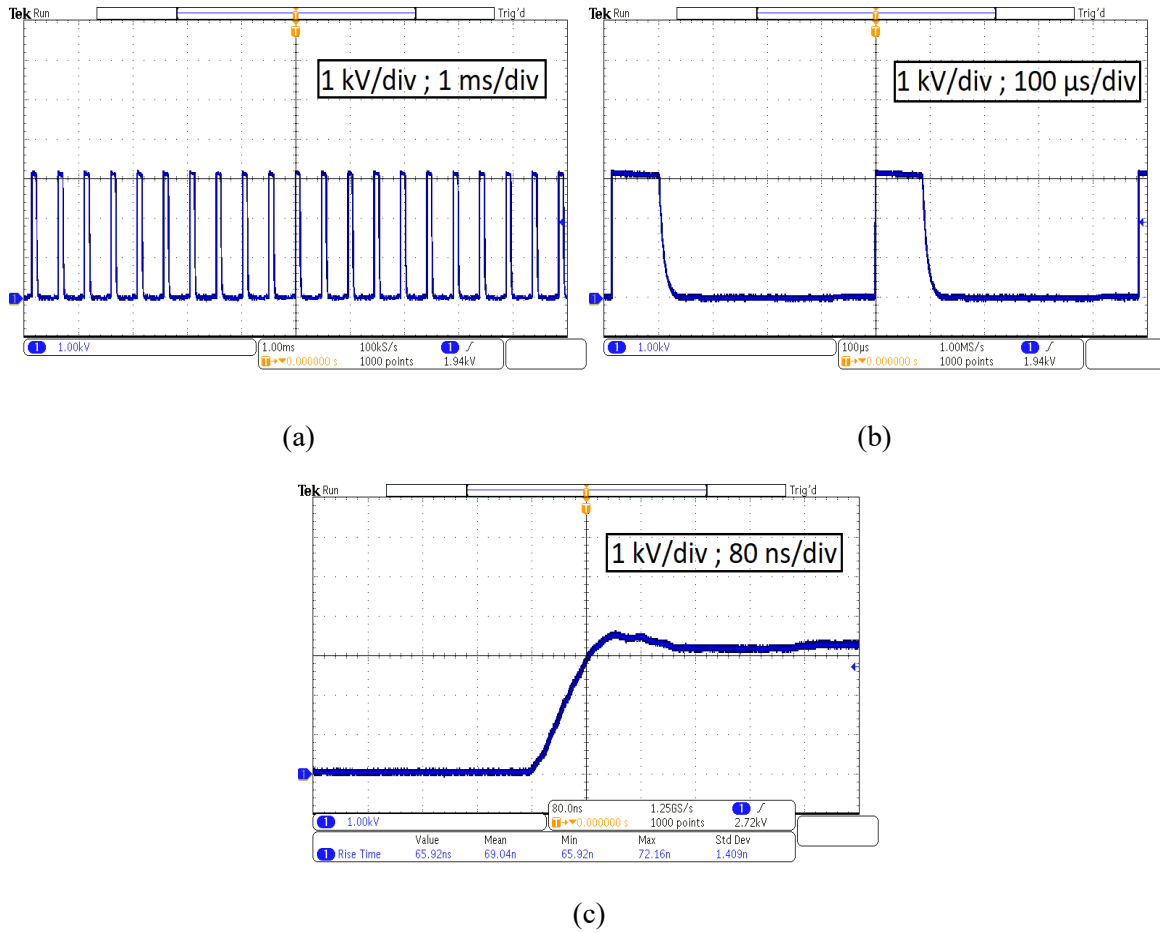


Fig. 4.17 Measured voltage waveforms: (a and b) 3.2 kV rectangular pulses, and (c) zoomed view of the rise time (66 ns).

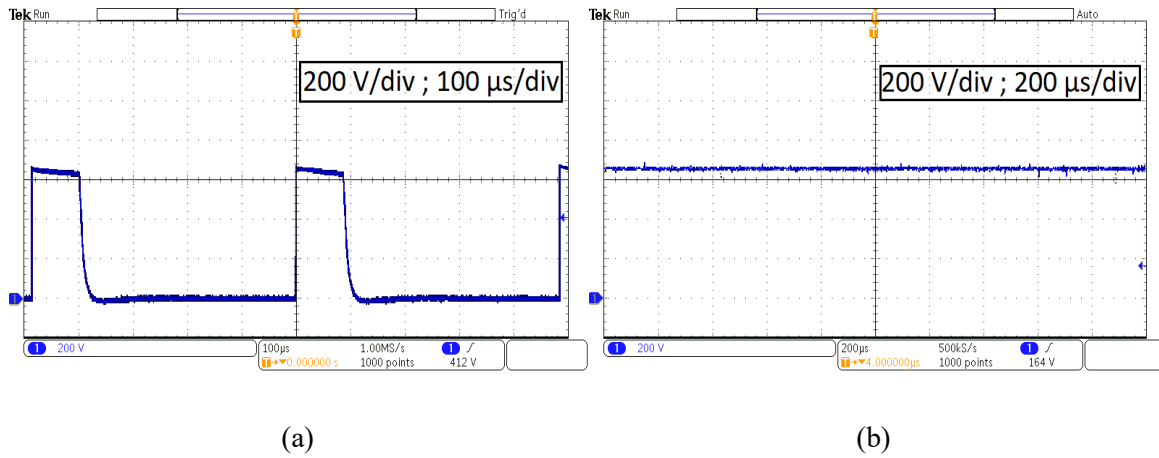


Fig. 4.18 Measured voltage waveforms: (a) output of each module and (b) capacitor's voltage.

4.7.2.3 Switches' Voltage Waveshape

The voltage waveform across the charging switches is shown in Fig. 4.19 (a), and the discharge switches' voltage waveform is depicted in Fig. 4.19 (b). The charging switches experience a voltage stress of 640 V, which is present only during the pulse generation period. On the other hand, the discharge switches endure a continuous voltage stress of 640 V, except during the pulse generation period. These waveforms follow the simulation results in Fig. 4.12.

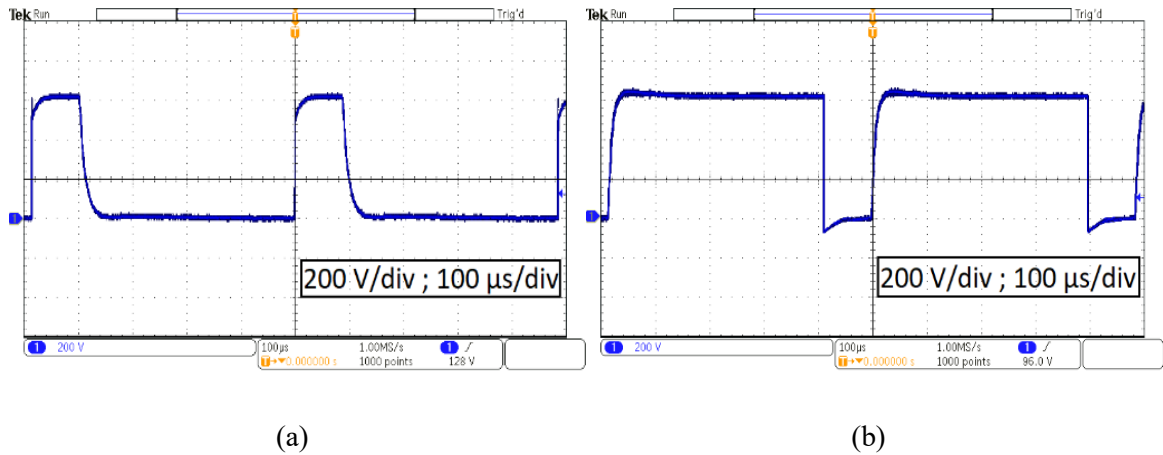


Fig. 4.19 Measured voltage waveforms: (a) across charging switch and (b) across discharging switch.

4.7.2.4 Diodes' Voltage Waveshape

The voltage waveforms across the diodes are shown in Fig. 4.20, following the same waveforms in simulation results, presented in Fig. 4.13. The voltage stress on diodes (6) varies according to their

stage number. Similar to the charging switches, diodes also experience voltage stress only during the pulse generation period.

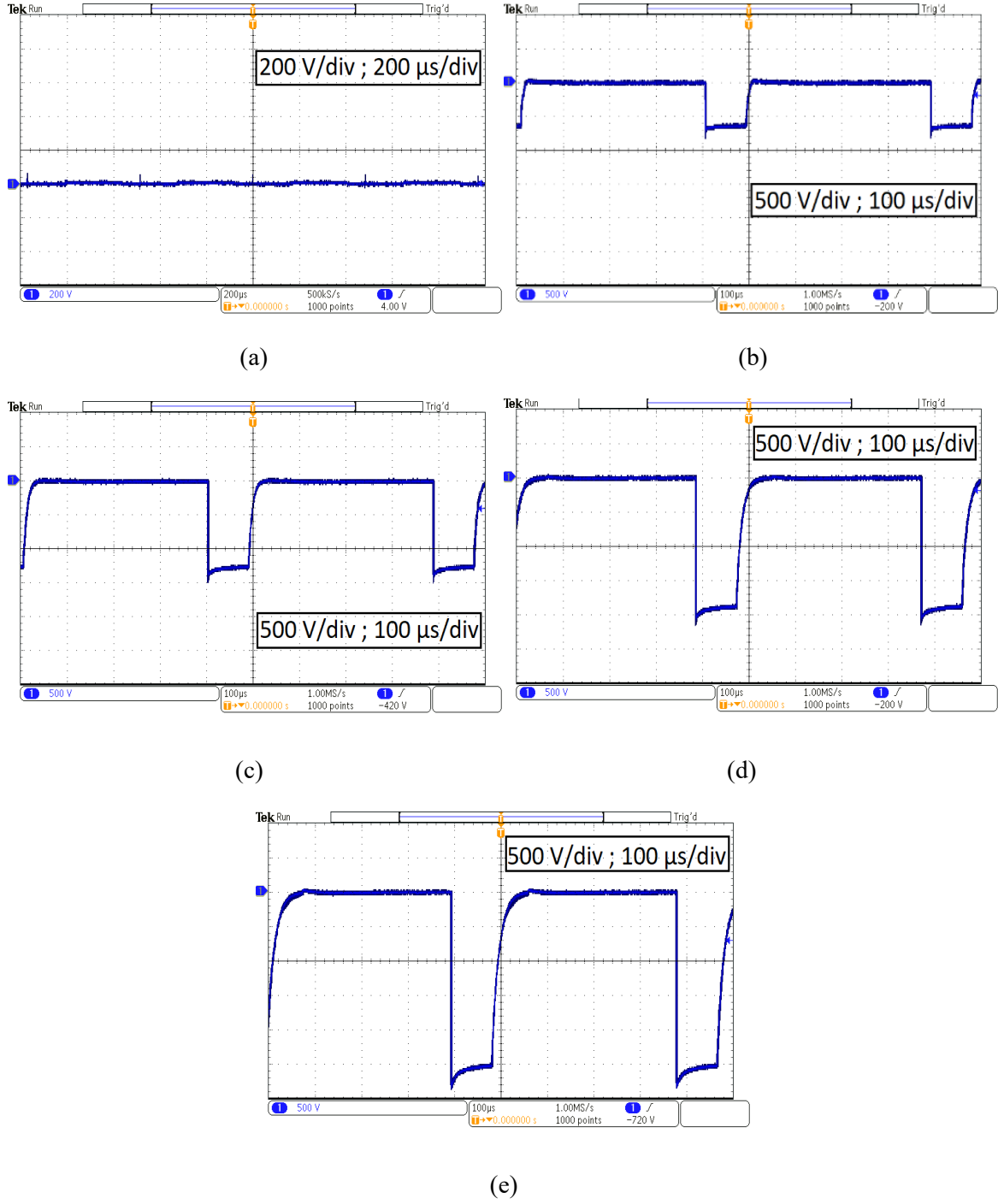


Fig. 4.20 Measured voltage waveforms of diodes: (a) D₁, (b) D₂, (c) D₃, (d) D₄, and (e) D₅.

4.7.2.5 Output Pulses with Different Rise Times

Output pulses with different rise times, duty cycles, overshoots, frequencies, and multilevel waveforms are shown in Fig. 4.21 - Fig. 4.25.

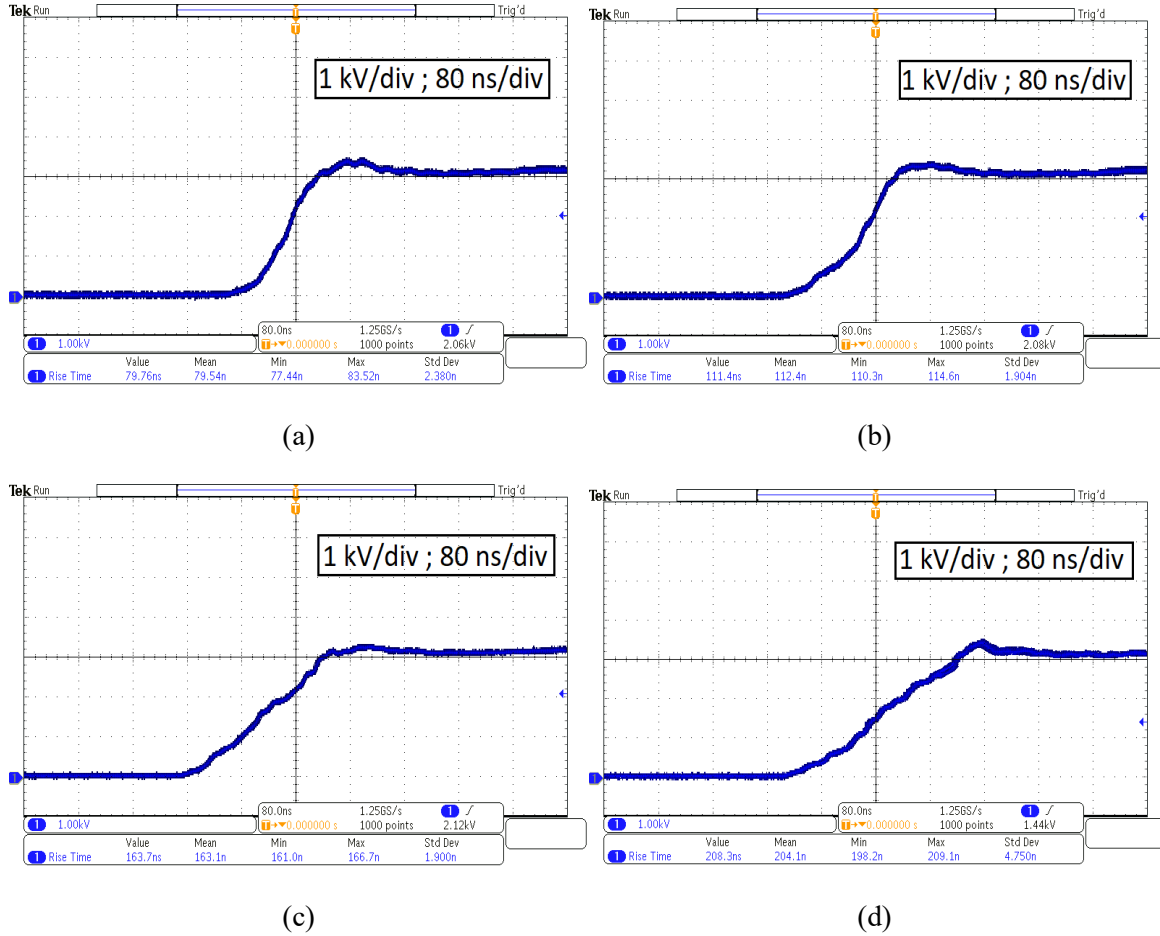


Fig. 4.21 Measured voltage waveforms with different rise times: (a) 80 ns, (b) 110 ns, (c) 164 ns, and (d) 208 ns.

Indeed, the pulse rise time is a critical factor in motor insulation studies, especially when dealing with WBG devices with very fast switching speeds. The proposed WBG device-based converter not only provides a very fast rise time but also offers the advantage of variable pulse rise time. This variable pulse rise time is a significant feature that enables the investigation of the effects of different rise times on PD behavior and insulation performance. 4 different rise times (80, 110, 164, and 208 ns) are shown in Fig. 4.21. The voltage waveshape during the rising edge is smooth, without any noticeable glitches. The variable pulse rise time is achieved by integrating the modules into the discharge cycle with delays, as depicted in Fig. 4.7.

4.7.2.6 Output Pulses with Different Duty Cycles

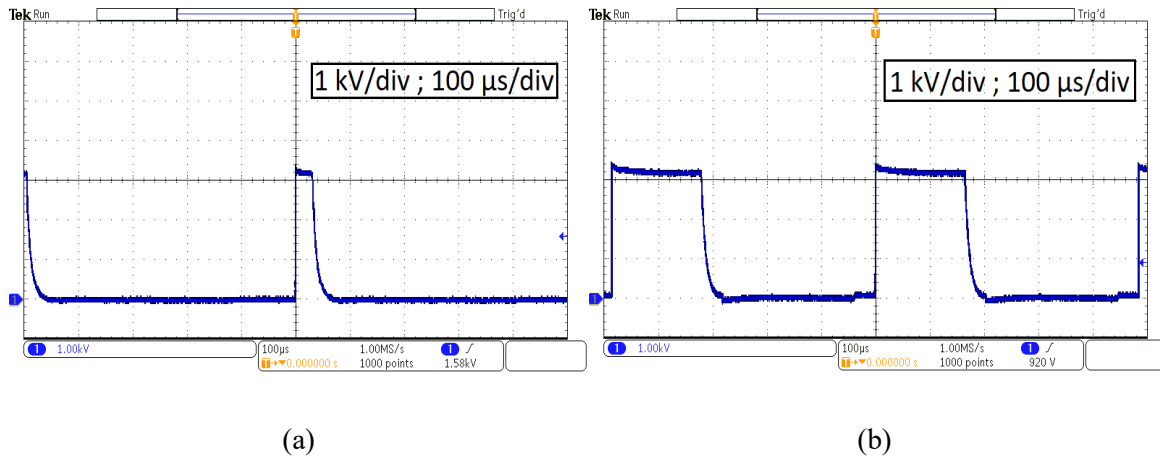


Fig. 4.22 Measured voltage waveforms with different duty cycles: (a) $t_3=6\%$ and (b) $t_3=34\%$.

The duty cycle is variable in this work and is controlled by the discharge switches' conduction time. Pulses with different duty cycles (6% and 34 %) are demonstrated in Fig. 4.22. The pulse duty cycle is determined by the time period t_3 , as demonstrated in Fig. 4.6.

4.7.2.7 Output Pulses with Different Overshoots

Overshoot is a significant concern in motor insulation studies and can have detrimental effects on the quality of insulation systems. Overshoot refers to a sudden transient increase in voltage or current beyond the desired or steady-state value. This phenomenon can subject the insulation materials to higher stress and potentially lead to insulation breakdown or reduced insulation lifetime. Overshoot control is shown in Fig. 4.23 and it is controlled by the control circuit (gate signals) and the structure of the topology (order of inserting the modules). Another approach to address overshoot, involves adding a capacitor in parallel to the load side or gate-source pins of the MOSFETs in the converter. Capacitors act as energy storage elements, smoothing out the transient variations in voltage or current and reducing overshoot.

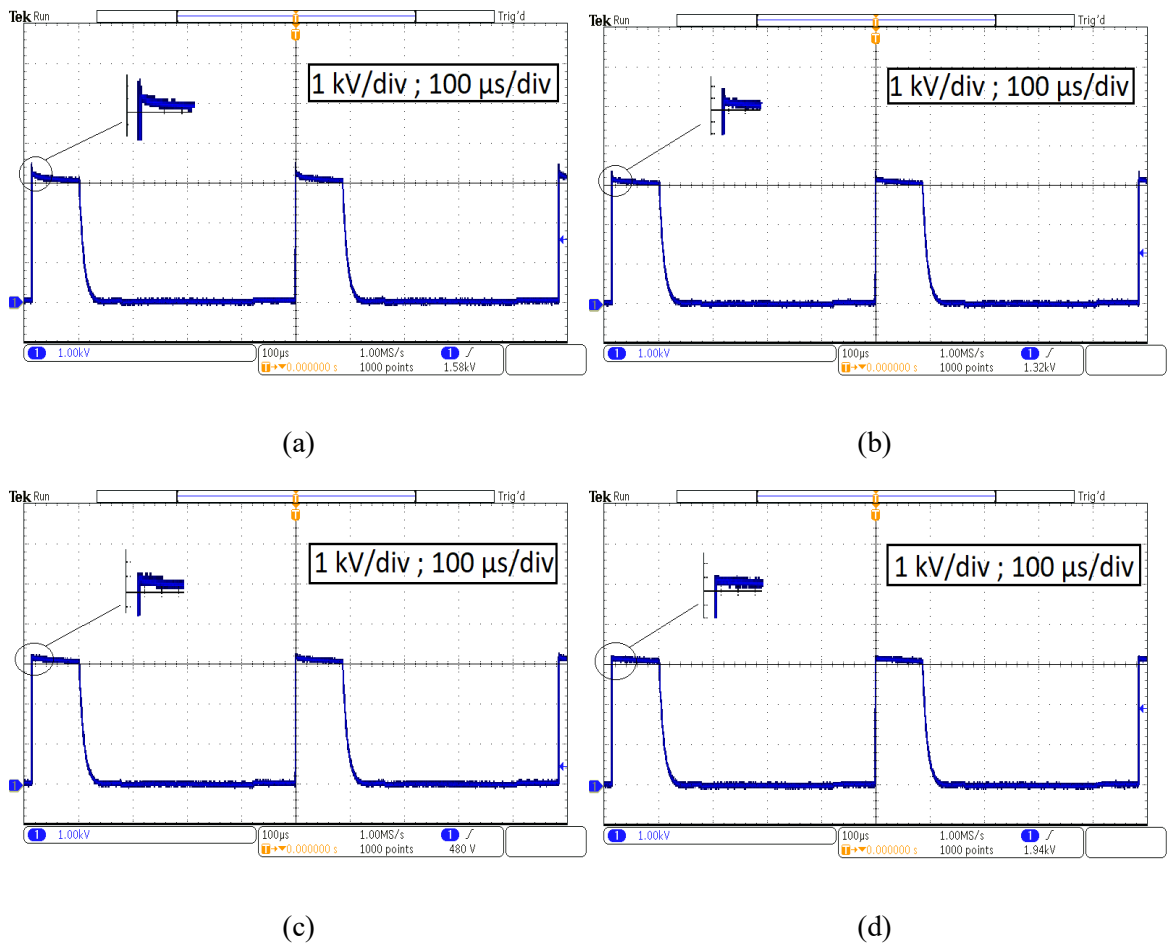


Fig. 4.23 Measured voltage waveforms with different overshoots: (a) control 1, (b) control 2, (c) control 3, and (d) control 4.

4.7.2.8 Output Pulses with Different Frequencies

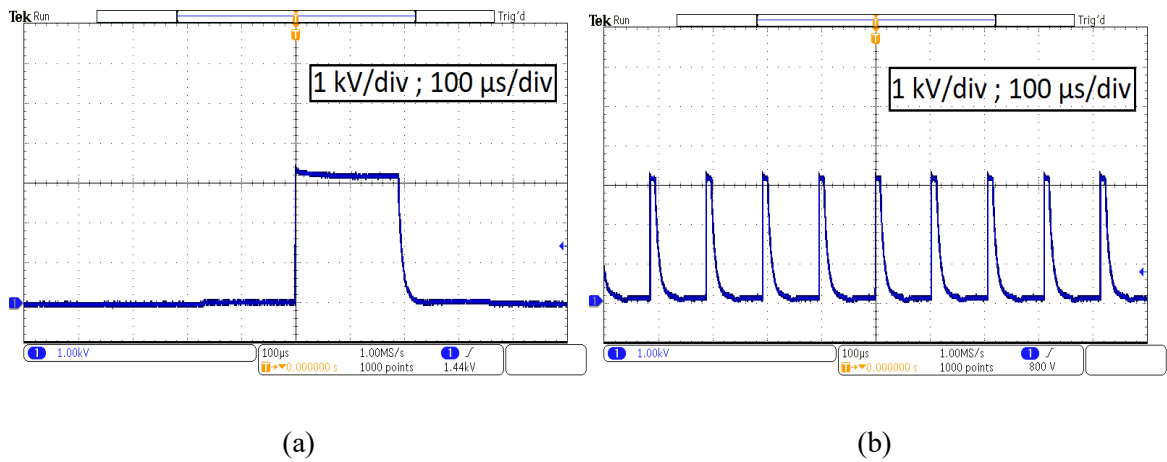


Fig. 4.24 Measured voltage waveforms with different frequencies: (a) 1 kHz and (b) 10 kHz.

It is important to study the effect of frequency on motor insulation, because EV drives operate at different frequencies. The generator is capable of generating pulses with different frequencies by changing the switching frequency. Output pulses with different frequencies (1 and 10 kHz) are shown in Fig. 4.24.

4.7.2.9 Multilevel Output Voltage Waveshape

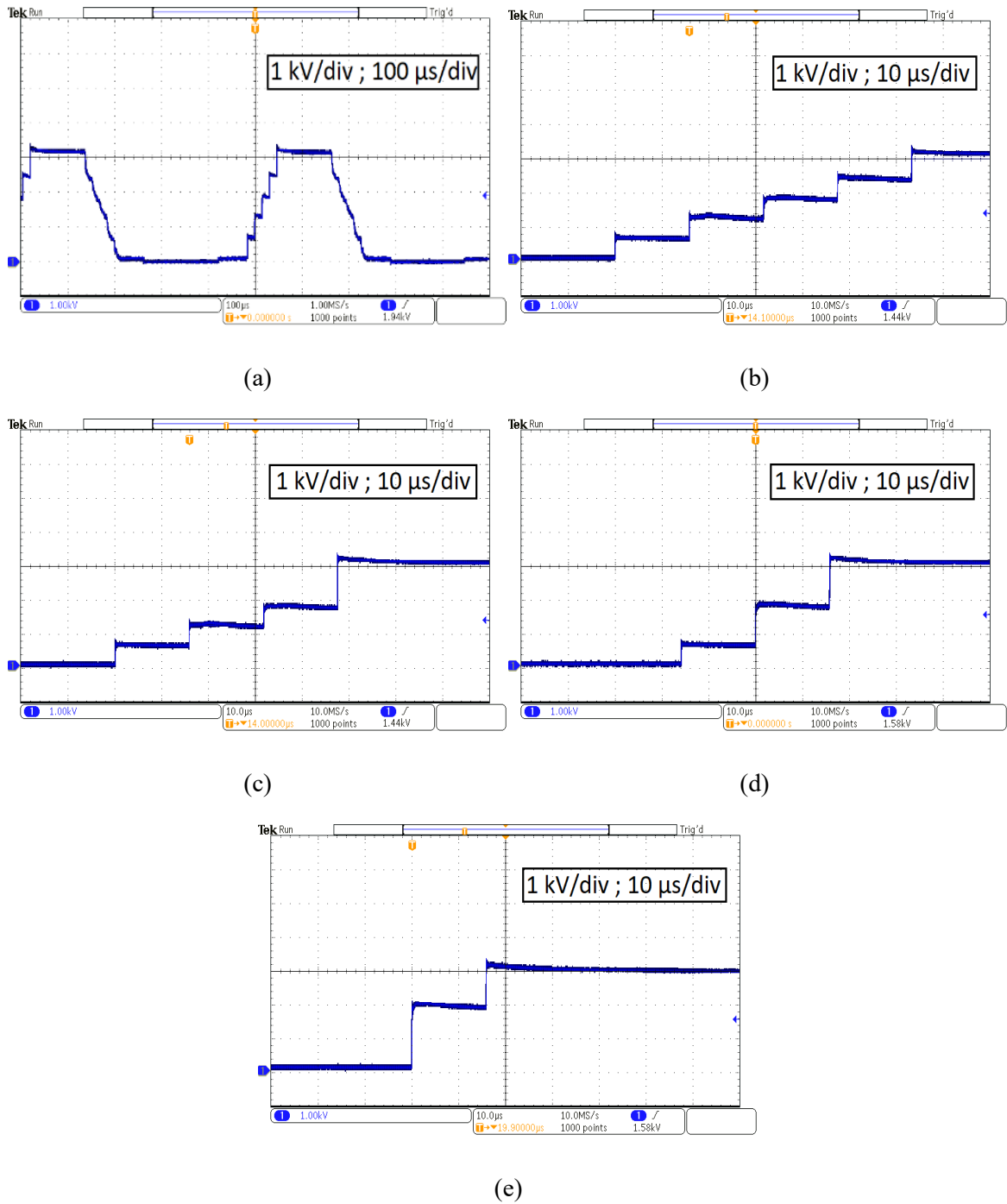
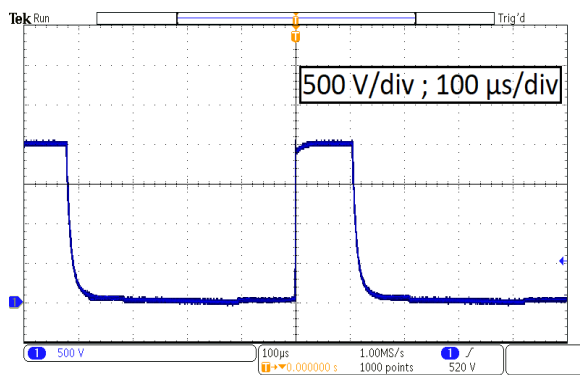


Fig. 4.25 Measured multilevel waveforms: (a) 5-level, (b) 5-level, (c) 4-level, (d) 3-level, and (e) 2-level.

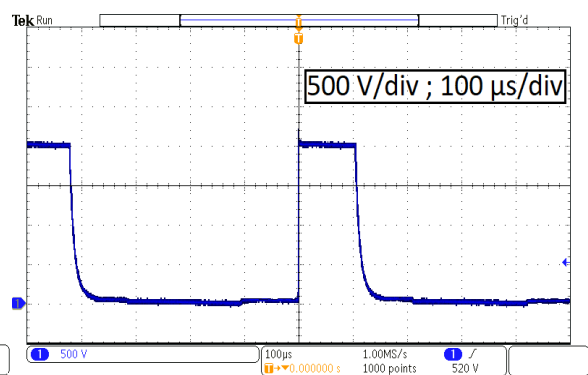
Multilevel waveforms are adopted in EV drives due to their numerous advantages, such as reduced harmonic content, lower switching losses, and improved voltage quality. The multilevel waveforms generated by the converter are presented in Fig. 4.25. 5 modules have been used, so multilevel waveforms up to 5 levels (as demonstrated in Fig. 4.8) can be generated at the output.

4.7.2.10 Loading Effect on the Generator Output

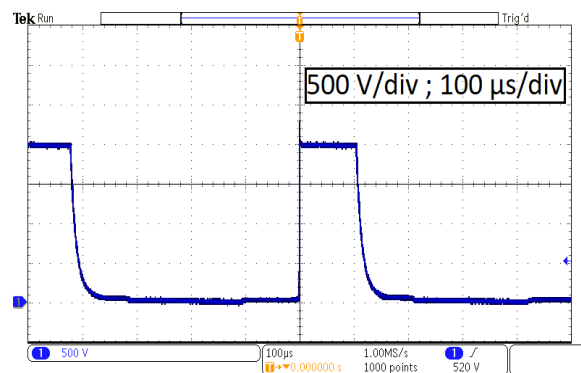
2 kV pulses have been applied to back-to-back test samples to evaluate the generator's performance under loading conditions. Fig. 4.26 (a-c) show the voltage waveforms without any sample (Fig. 4.26 (a)), with one sample (Fig. 4.26 (b)), and with two parallel samples (Fig. 4.26 (c)), connected as loads. Looking at Fig. 4.26, the amplitude of the pulses is not affected by the samples' loading effect. The zoomed view of the pulses is demonstrated in Fig. 4.27 (a-c). Waveform oscillation after the rise time can be seen in Fig. 4.27 (a-c) with no sample, one sample, and two parallel samples, respectively. These oscillation and overshoot differences can be attributed to the samples' capacitance and inductance and the additional wires used to connect the samples to the converter.



(a)

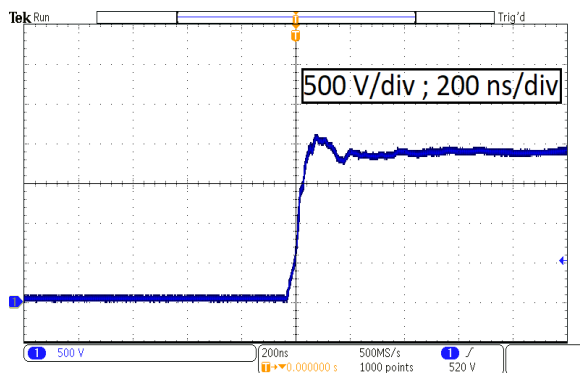


(b)

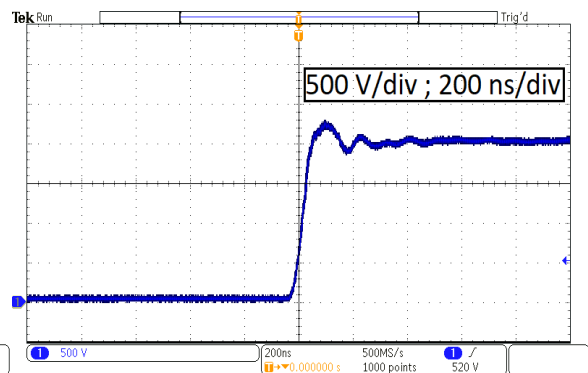


(c)

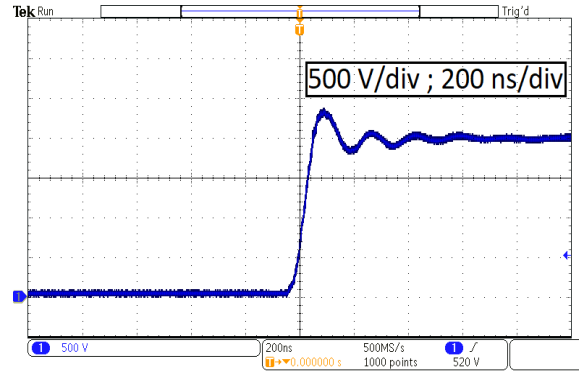
Fig. 4.26 Measured 2 kV pulses: (a) without any sample, (b) with one sample, and (c) with two parallel samples.



(a)



(b)



(c)

Fig. 4.27 Zoomed view of the measured 2 kV pulses with increasing load: (a) without any sample, (b) with one sample, and (c) with two parallel samples.

The simulation and experimental results are in good agreement, and the waveforms closely match the expectations derived from theoretical analysis. The experimental results verified the functionality of the proposed converter in controlling different pulse parameters that are required for motor insulation testing purposes.

4.8 Modified Pulse Power Supply for Long-Term Aging

For the aging tests, a modified version of the proposed modular generator [70] is used, which includes only the first module of the generator explained in this chapter. The modified version uses fewer components and provides higher circuit reliability, pulses with faster rise times, and easier maintenance. The modified version, as shown in Fig. 4.28, incorporates the MSC400SMA330B4 SiC-MOSFET, which has a blocking voltage of 3.3 kV, a rise time of 8 ns, and a turn-on delay time of 16 ns. The modified version uses two parallel 2 μ F, 5 kV capacitors and three parallel 20 k Ω EBG-UXP 600 low inductance resistors as the wave-shaping resistors. The generator has been used for more than 1600 hours for the aging tests.

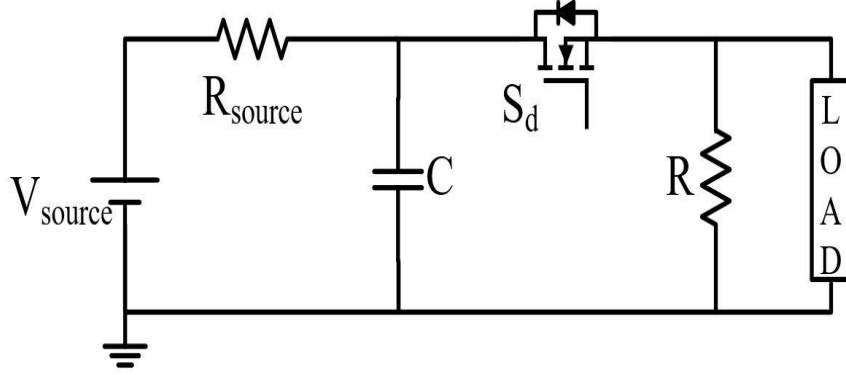


Fig. 4.28 The modified version of the pulse generator for the aging tests.

4.9 Summary

An SiC-MOSFET-based HV pulse generator has been developed and evaluated for investigating the impacts of repetitive fast transients on motor insulation used in EVs. The proposed modular design provides control over the pulse parameters such as amplitude, rise time, frequency, duty cycle, and overshoot. In addition, by varying the sequence of switching in the modules, multilevel voltage waveforms can be generated. Accordingly, the desired pulse parameters can be achieved by the control circuit and the modular circuit architect. The switching sequence of modules defines the simplicity of controlling the above-mentioned pulse parameters.

The functionality of the proposed HV pulse generator has been evaluated through both simulation and experimental studies. The five-module generator presented in this chapter is capable of producing 3.2 kV square pulses or up to five-level voltage waveforms. The generator has been tested to ensure its suitability for long-term aging tests using back-to-back motor insulation samples. The generator is optimized for high-impedance capacitive loads, like insulation systems.

The focus of this thesis is to age the samples under defined conditions that are discussed in the next chapter. For the aging experiments, it is more efficient to use the modified version of the generator to reduce circuit components, increase circuit reliability, reduce pulse rise time, and reduce stray capacitance and inductance in the circuit, which affects the output pulse waveform. If the effect of multilevel waveforms or studying PD signals under different pulse conditions is of interest, it is recommended to use the modular version of the power supply due to its capability to control pulse parameters by the control circuit.

Chapter 5

Results

The effects of integrating hairpin winding and WBG device-based power converters in EVs are investigated in this chapter. The results of the back-to-back samples aging under PD activities are studied under different pulse rise times, overshoots, frequencies, duty cycles, and temperatures. The insulation performance measurements are performed before and after aging to understand the aging effect. PDIV, DFR analysis, temperature measurements, and microscopic, AFM, and SEM images are used to evaluate the insulation performance. The tests are designed based on DOE principles to systematically assess each parameter's effect and find any probable interaction between the factors. The parameters studied in the thesis are presented in Fig. 5.1. The effects of rise time and overshoot are evaluated on both the CR and NCR wires, but the effects of frequency, duty cycle, and temperature are studied only on the CR wires.

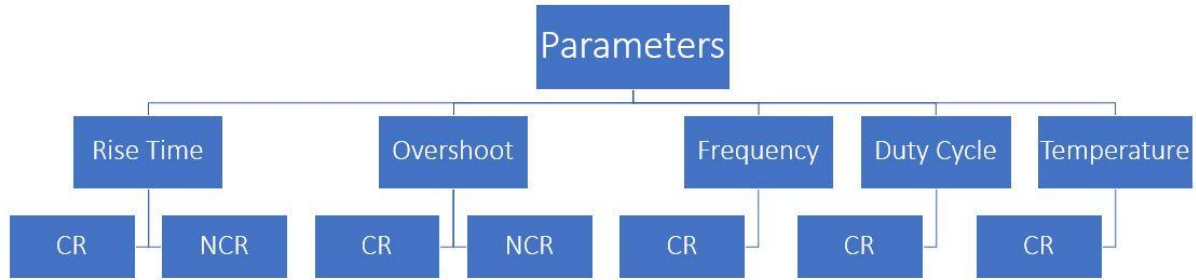


Fig. 5.1 The flowchart representing the parameters studied on the wires.

5.1 Rise Time and Overshoot Effects on Corona-Resistant and Non-Corona-Resistant Wires

The effects of rise time and overshoot of the WBG device-based drives on turn-to-turn insulation in hairpin windings are studied in this section [82]. WBG switching devices have a very fast rise time in the range of tens of nanoseconds, which will cause uneven voltage distribution among the motor windings. Uneven voltage distribution results in local electric field enhancement, which may lead to local discharges in the stator winding. Therefore, it is crucial to evaluate the fast rise time effect associated with the WBG device-based drives on insulation performance. Two types of flat wires, corona-resistant and non-corona-resistant, are tested to evaluate insulation performance. The wires are

aged under PD conditions with varying rise times and overshoots. Key parameters measured include PDIV, %DF, sample surface temperature, and wire surface morphology before and after aging.

5.1.1 Test Conditions and Voltage Waveform Parameters

The experimental settings are designed following the principles of Design of Experiments (DOE), using a full-factorial, two-factor, two-level approach. The two factors considered here are overshoot (OS) and rise time. For each type of wire, four different experiments were initially conducted to cover all combinations of the factor levels, based on Table 5.1. To better observe the trend of changes with respect to rise time, an additional midpoint value of 500 ns was included. As a result, six experiments were conducted for each wire type. The low and high levels of the factors are presented in Table 5.1.

Table 5.1 High and low levels of the voltage waveform factors.

Factor	Identification	Low Level	High Level
OS (%)	A	10	20
Rise Time (ns)	B	40	800

The effects of pulse voltage rise time and overshoot are investigated in this section by examining three different rise times and two overshoot levels while keeping other waveform parameters constant: a pulse voltage of 2.5 kV, a frequency of 5 kHz, and a 50% pulse duty cycle. The 40 ns rise time was selected considering the high dV/dt of WBG switching devices, and the other two rise times were selected based on the circuit connection between the motor and the drive. According to [7], the rise time can vary in the range of $0.05 \mu s$ - $2 \mu s$; hence, 500 and 800 ns were selected. The overshoot values were selected in the range of the moderate stress category mentioned in [7]. A total of 12 tests were conducted, as detailed in Table 5.2, with the rising edge of the pulse voltage waveforms corresponding to each experiment shown in Fig. 5.2. Each test involved 5 samples, and to ensure conclusive results, the average values for each test have been reported. The aging tests are conducted at room temperature ($24^\circ C$) under intentional PD activities, in the region of interest, that is, in the 10cm area, as shown in Fig. 3.4, throughout the aging experiments.

Table 5.2 The test conditions and pulse parameters.

Test NO	OS%	Rise Time (ns)	Wire Type
T1	10	40	CR
T2	10	40	NCR
T3	10	500	CR
T4	10	500	NCR
T5	10	800	CR
T6	10	800	NCR
T7	20	40	CR
T8	20	40	NCR
T9	20	500	CR
T10	20	500	NCR
T11	20	800	CR
T12	20	800	NCR

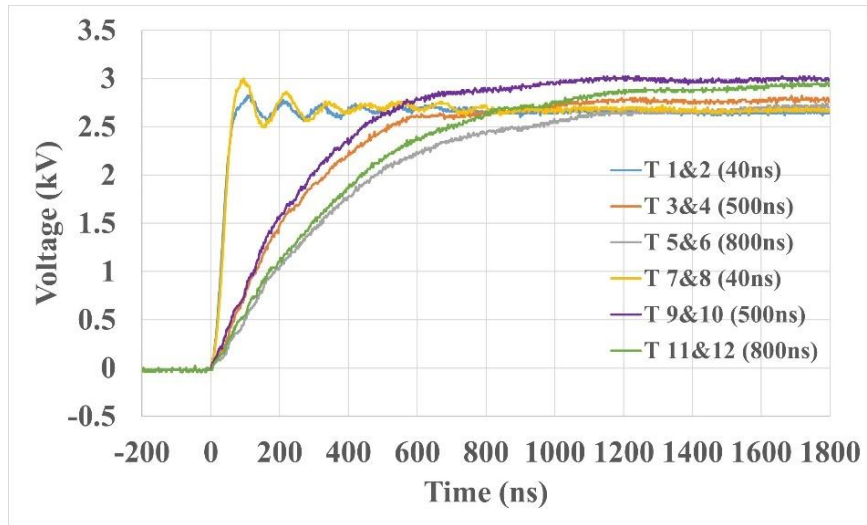


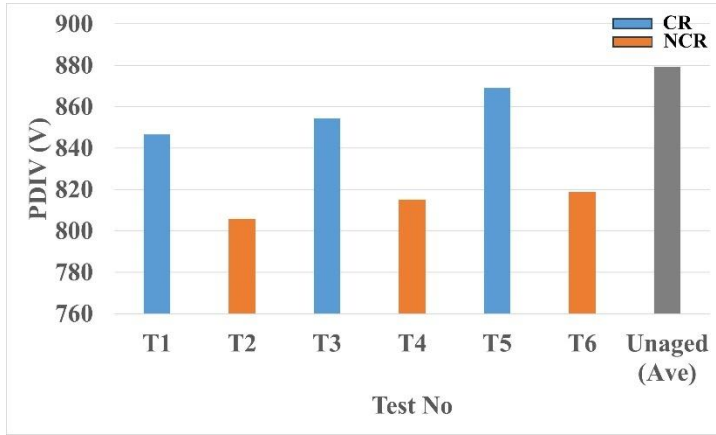
Fig. 5.2 The applied voltage waveshape of the pulse rising edge measured at the terminal of the test objects.

5.1.2 Measured PDIV Values of the Samples

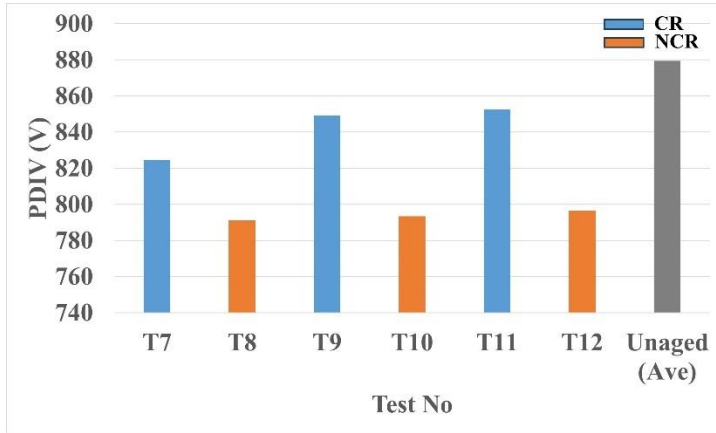
PDIV is a direct measure of insulation robustness. The PDIV of the back-to-back samples has been measured and compared before and after aging to evaluate the insulation performance under PD

activities. The measured PDIV values after aging for both wires, with 10% and 20% OS, are shown in Fig. 5.3 (a) and (b), respectively. For a fair comparison between the results of both wires, the PDIV values of the aged samples have been normalized to the average PDIV value of the samples before aging, which was 880 V.

Examining the PDIV results for the aged samples at 10% OS (Fig. 5.3 (a)) reveals that faster rise times lead to a more significant drop in PDIV across all test conditions. There are several reasons for this observation, such as a higher energy deposition in dielectric material per pulse with a faster rise time compared to a slower rise time. This higher energy deposition accelerates the thermal and mechanical stress on the insulation, leading to faster aging and material breakdown. Furthermore, a faster rise time can increase the intensity and frequency of PD signals, which would degrade the insulation and lead to a lower PDIV. This will also generate localized heating in the insulation that can soften or degrade the polymeric material of the enamel coating, weakening its ability to withstand PD activity and thus contributing to a faster reduction in PDIV. Additionally, there is a clear distinction between the PDIV results of the CR and NCR wires. In all the similar test conditions, the CR wires demonstrated a lower PDIV drop than the NCR wires. CR wires are manufactured using specialized enamel coatings that contain inorganic fillers. These fillers enhance the insulation's resistance to PD-induced erosions, which slows down the breakdown process and minimizes insulation thinning over time. Furthermore, these fillers also help distribute the electric field more evenly across the insulation, reducing stress concentration that can accelerate degradation. Therefore, CR wires are specifically designed to resist PD to some extent and have improved surface insulation coating that reduces the rate of aging and degradation. Looking at Fig. 5.3 (a), the CR wire exhibited the smallest PDIV drop in T5, with 10% OS and an 800 ns rise time, while T2 showed the largest PDIV drop, corresponding to the NCR wire with 10% OS and a 40 ns rise time.



(a)



(b)

Table 5.2 The test conditions and pulse parameters.

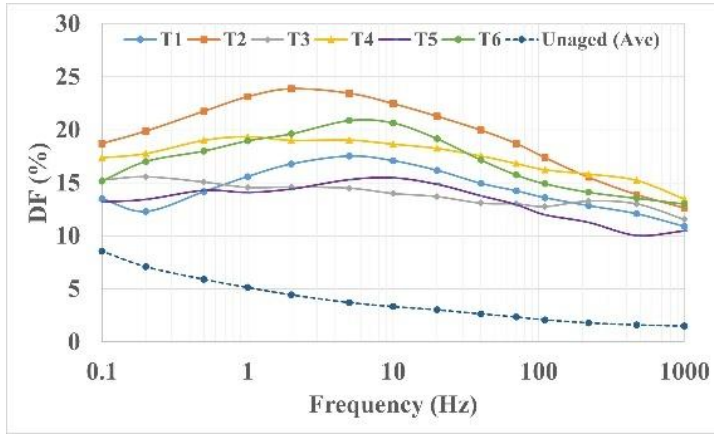
Test NO	OS%	Rise Time (ns)	Wire Type
T1	10	40	CR
T2	10	40	NCR
T3	10	500	CR
T4	10	500	NCR
T5	10	800	CR
T6	10	800	NCR
T7	20	40	CR
T8	20	40	NCR
T9	20	500	CR
T10	20	500	NCR
T11	20	800	CR
T12	20	800	NCR

Fig. 5.3 The measured PDIV values of the aged samples at (a) 10% OS and (b) 20% OS.

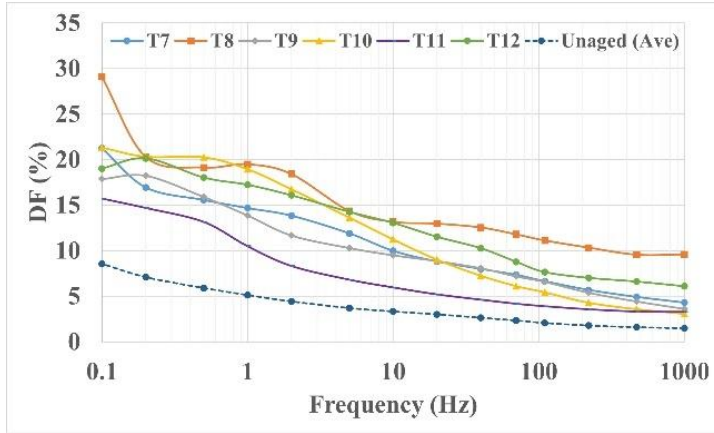
The PDIV results for the aged samples at 20% OS are shown in Fig. 5.3 (b). The trend is consistent with the 10% OS results, where PDIV values decrease more significantly with faster rise times for the same reasons discussed earlier. However, in the case of the NCR wire, the PDIV does not vary significantly with changes in rise time at 20% OS. T11 exhibited the lowest PDIV drop, while T8 had the highest, following the same reasoning observed in T5 and T2. When comparing the 10% OS and 20% OS graphs with the same rise time, the PDIV drop is more severe in all tests with 20% OS compared to those with 10% OS. The higher PDIV drop can be derived from a higher electrical field stress at higher OS, higher PD intensity, and higher temperatures from hotspots, which will result in faster insulation degradation.

5.1.3 Measured DF Values of the Samples

The dissipation factor, also known as $\tan \delta$, is a parameter used to assess insulation health. The DF represents the ratio of resistive current to capacitive current in an insulation system. Healthy insulations exhibit low dielectric losses, meaning most of the applied electrical energy is stored rather than dissipated. DF measurements are considered to observe the aging effect on the samples in this work. The average measured %DF values from the DFR analysis, based on a frequency sweep from 1 kHz down to 0.1 Hz, are presented in Fig. 5.4.



(a)



(b)

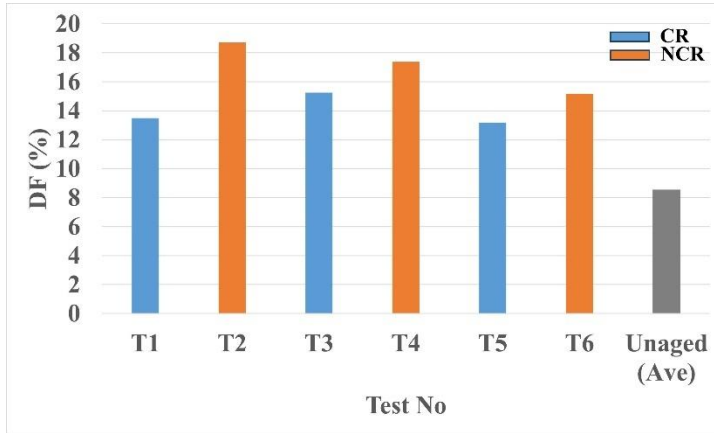
Table 5.2 The test conditions and pulse parameters.

Test NO	OS%	Rise Time (ns)	Wire Type
T1	10	40	CR
T2	10	40	NCR
T3	10	500	CR
T4	10	500	NCR
T5	10	800	CR
T6	10	800	NCR
T7	20	40	CR
T8	20	40	NCR
T9	20	500	CR
T10	20	500	NCR
T11	20	800	CR
T12	20	800	NCR

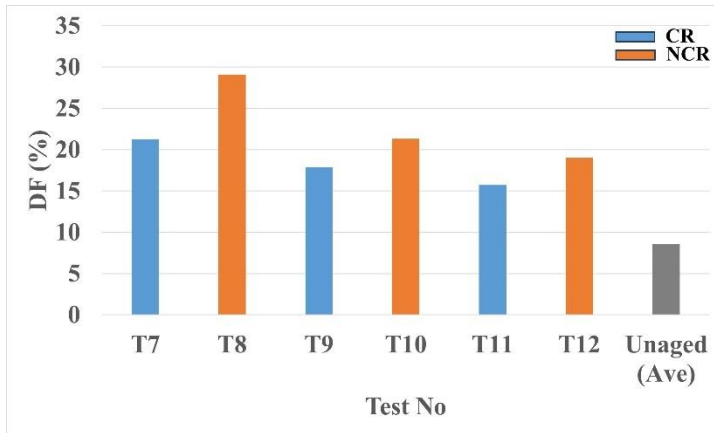
Fig. 5.4 The measured average DF values of the aged samples in a frequency sweep of 1 kHz down to 0.1 Hz at (a) 10% OS and (b) 20% OS.

The measured DF values, normalized to the average DF of the unaged samples, at different frequencies with 10% and 20% OS are shown in Fig. 5.4 (a) and (b), respectively. A consistent increase in DF values across all frequencies is observed when compared to the average DF of the unaged samples in both cases. This can be attributed to the damage caused by the PD activities, which can cause small voids or channels in the insulation material.

The average DF values at 0.1 Hz for 10% and 20% OS are presented in Fig. 5.5 (a) and (b) to assess the aging effect at a reference point. As can be seen from the DF values at the frequency sweep, DF increases at lower frequencies, as multiple polarizations, like interfacial polarization, happen at lower frequencies. 0.1 Hz is chosen to compare the DF results to see the aging effect and the damage in microcavities. For comparison, the DF values of the aged samples are normalized to the average DF value at 0.1 Hz before aging, which was 8.55%. The DF values before and after aging at 10% OS are depicted in Fig. 5.5 (a). The NCR wires exhibit higher DF values than the CR wires across all studied rise times, indicating a higher degradation rate in the NCR wires. Additionally, there is a consistent trend of increasing DF values with faster rise times due to the more intense PD signals and insulation degradation, though this trend is not observed in the CR wires. The highest DF value was recorded in T2, which corresponds to the fastest rise time.



(a)



(b)

Table 5.2 The test conditions and pulse parameters.

Test NO	OS%	Rise Time (ns)	Wire Type
T1	10	40	CR
T2	10	40	NCR
T3	10	500	CR
T4	10	500	NCR
T5	10	800	CR
T6	10	800	NCR
T7	20	40	CR
T8	20	40	NCR
T9	20	500	CR
T10	20	500	NCR
T11	20	800	CR
T12	20	800	NCR

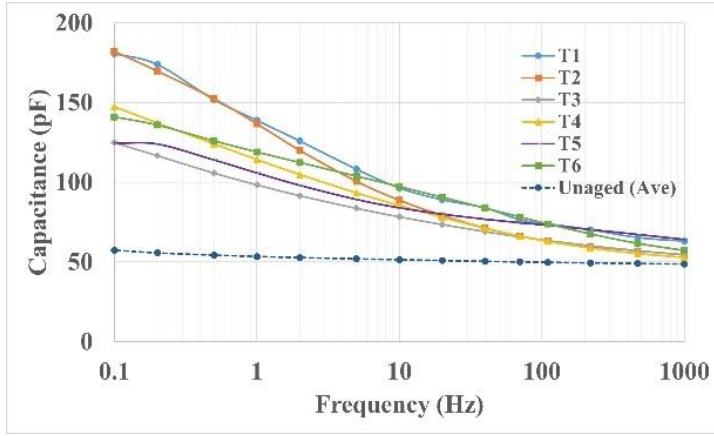
Fig. 5.5 The measured average DF values of the aged samples at 0.1 Hz at (a) 10% OS and (b) 20% OS.

Examining the DF results at 20% OS (Fig. 5.5 (b)), T8, which corresponds to the NCR wire with the fastest rise time, shows the highest DF value. There is a consistent trend of increasing DF values with faster rise times for both types of wires, as previously explained. Additionally, NCR wires exhibit higher DF values than CR wires after the aging process, which is related to the lower degradation rate of CR wires.

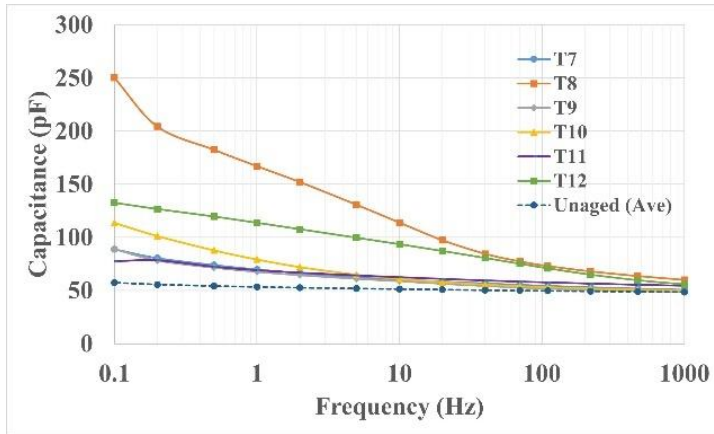
5.1.4 Measured Capacitance Values of the Samples

The normalized average capacitance values measured from the DFR analysis over the frequency range from 1 kHz down to 0.1 Hz, with 10% and 20% OS, are presented in Fig. 5.6 (a) and (b), respectively. These capacitance values have been normalized to the average capacitance of the unaged

samples. Changes in capacitance are evident across all studied frequency ranges, with more pronounced variations in the insulation material observed at lower measurement frequencies, as expected.



(a)



(b)

Table 5.2 The test conditions and pulse parameters.

Test NO	OS%	Rise Time (ns)	Wire Type
T1	10	40	CR
T2	10	40	NCR
T3	10	500	CR
T4	10	500	NCR
T5	10	800	CR
T6	10	800	NCR
T7	20	40	CR
T8	20	40	NCR
T9	20	500	CR
T10	20	500	NCR
T11	20	800	CR
T12	20	800	NCR

Fig. 5.6 The measured average capacitance values of the aged samples in a frequency sweep of 1 kHz down to 0.1 Hz at (a) 10% OS and (b) 20% OS.

With the 20% OS tests, the trend in capacitance changes differs from that observed in the 10% OS tests. The CR wires exhibited almost consistent capacitance across the different tested rise times (T7, T9, and T11), although the capacitance values were higher than those of the unaged samples. However, in the 20% OS tests, the capacitance values varied with different rise times, though not consistently with the rise time changes. The highest capacitance was observed in T8, which corresponds to the NCR

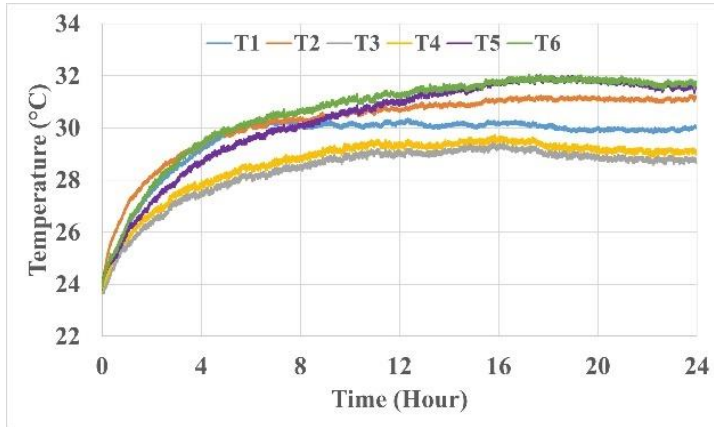
wire test with the 40 ns time at 20% OS. Overall, the capacitance increases along with the DF increase of all samples, indicating the insulation degradation under PD activities.

5.1.5 Measured Temperature Values at the Crotch Area of the Samples

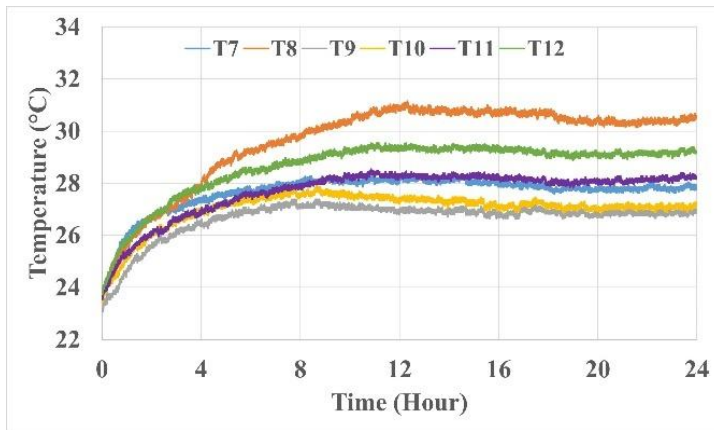
The temperature of the samples in their exit area (as circled in Fig. 3.4 as the crotch area) was continuously measured throughout the experiments, with the average temperature values for each experiment reported here. The tests were conducted at room temperature, and the sample crotch area temperatures at 10% and 20% OS are shown in Fig. 5.7 (a) and (b), respectively. Initially, the temperature of the samples rose quickly before stabilizing for the remainder of the experiment. The temperature rise can be attributed to PD activities, dielectric losses, and the aging time duration. Across all experiments, the NCR wires exhibited higher temperatures than the CR wires due to a higher degradation rate. This observation is in line with the PDIV, DF, and capacitance measurement results for the CR and NCR wires, where the degradation rate was higher for the NCR wires.

For the 10% OS tests (Fig. 5.7 (a)), the measured temperature at the crotch area of the samples with a 500 ns rise time (T3 and T4) and 800 ns rise time (T5 and T6) demonstrated nearly the same values for the CR and NCR wires. However, there was a significant temperature difference in the tests with the 40 ns rise time (T1 and T2).

In the 20% OS tests (Fig. 5.7 (b)), the test samples with a 500 ns rise time exhibited nearly identical temperatures, whereas the other tests showed varying temperatures with different rise times. In all cases, the NCR wires reached higher temperatures than the CR wires.



(a)



(b)

Table 5.2 The test conditions and pulse parameters.

Test NO	OS%	Rise Time (ns)	Wire Type
T1	10	40	CR
T2	10	40	NCR
T3	10	500	CR
T4	10	500	NCR
T5	10	800	CR
T6	10	800	NCR
T7	20	40	CR
T8	20	40	NCR
T9	20	500	CR
T10	20	500	NCR
T11	20	800	CR
T12	20	800	NCR

Fig. 5.7 The measured temperature of the samples in the crotch area under energization at (a) 10% OS and (b) 20% OS.

5.1.6 Optical Microscope and AFM Images from the Surface of the Wires

The performance of the insulation system's surface was further investigated using microscope images and AFM images to assess surface roughness. The microscope and AFM images were taken from the 10 cm contact area surface of the wires, where PD activities were happening. The microscope images, with 1×1.8 mm dimensions, have been shown in Fig. 5.8 and Fig. 5.9 for the CR (from T7) and the NCR (from T8) wires, respectively, revealing visible insulation damage on the surface of both wires after aging.

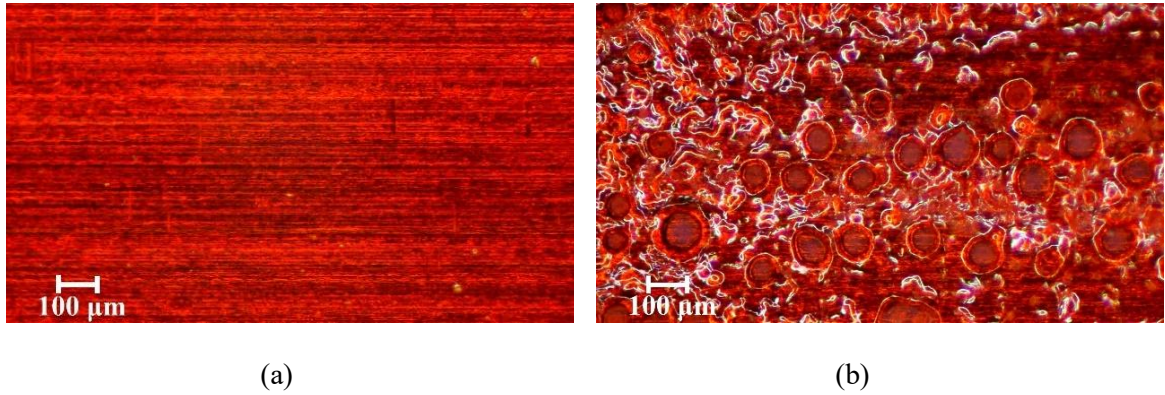


Fig. 5.8 The optical microscope images from the surface of the (a) unaged CR wire and (b) aged CR wire.

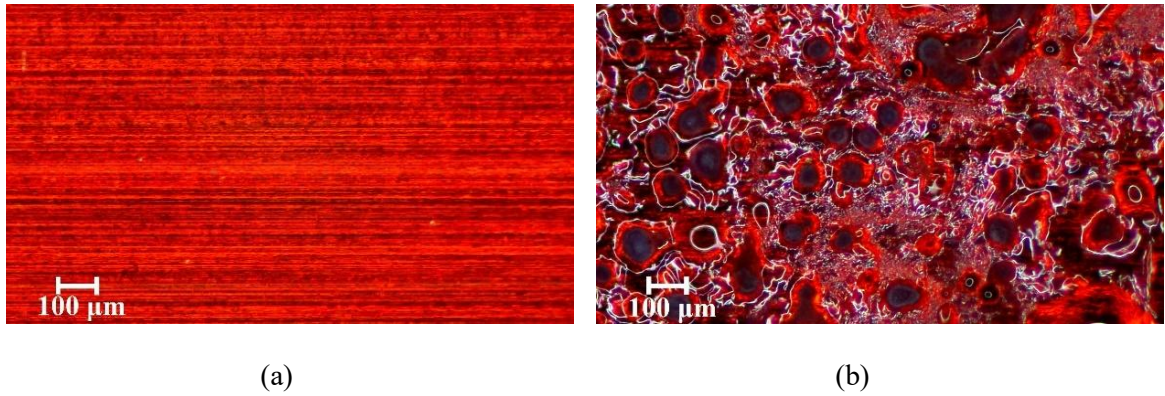
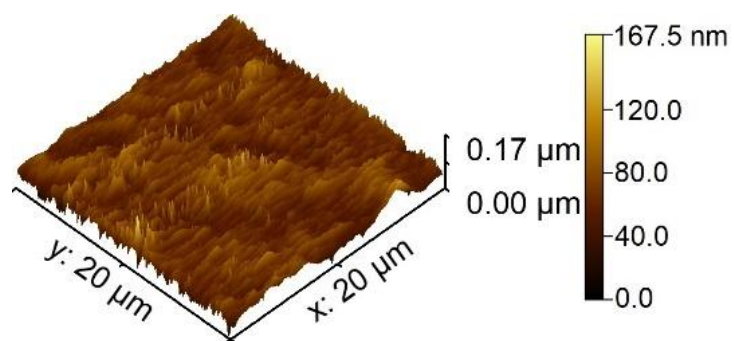


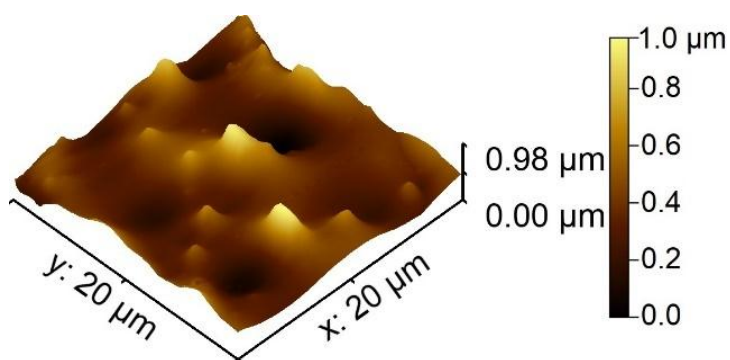
Fig. 5.9 The optical microscope images from the surface of the (a) unaged NCR wire and (b) aged NCR wire.

To quantify the surface differences between unaged and aged wires, surface roughness was measured using AFM topographical images (Fig. 5.10 and Fig. 5.11) with dimensions of $20 \times 20 \mu\text{m}$. Although scanning different locations on the wire could yield varying roughness values, the significant roughness difference caused by PD activities between the unaged and aged wires was evident across the entire surface.

For the CR wire (from T7), the rms roughness of the unaged wire, shown in Fig. 5.10 (a), was 13 nm. After aging, the rms roughness increased to 128 nm, as demonstrated in Fig. 5.10 (b). Similarly, the unaged NCR wire had an rms roughness of 11 nm, as shown in Fig. 5.11 (a). Post-aging, the NCR wire's rms roughness (from T8) escalated to 140 nm. This considerable increase in surface roughness (10 times and more) in the AFM results and the wire's microscope images clearly indicate significant insulation surface degradation due to the PD activities.

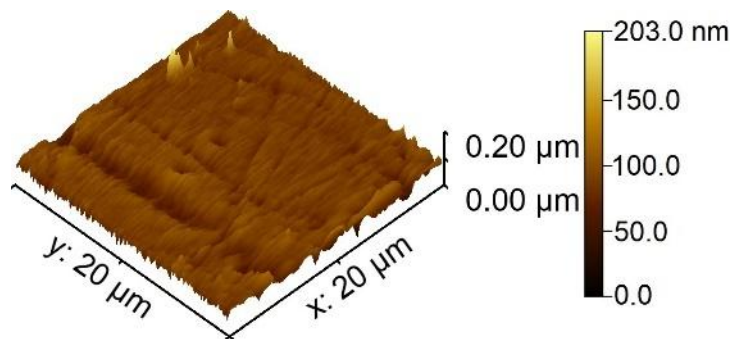


(a)

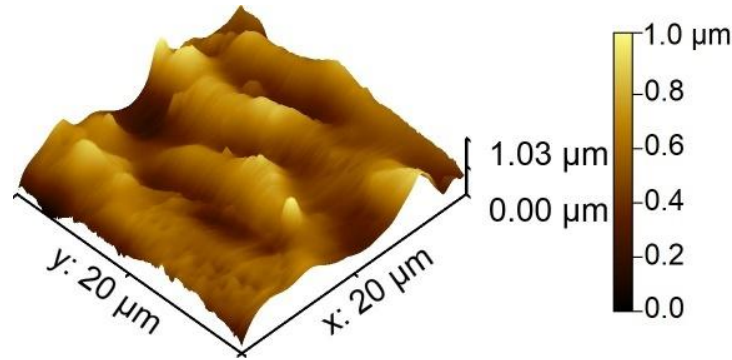


(b)

Fig. 5.10 The 3D AFM images of the surface of (a) the unaged CR wire and (b) the aged CR wire.



(a)



(b)

Fig. 5.11 The 3D AFM images of the surface of (a) the unaged NCR wire and (b) the aged NCR wire.

5.1.7 Summary of the CR and NCR Wires' Performance under Variable Rise Time and Overshoot

The comparative analysis of PDIV and DF measurements, along with the wire surface imaging, demonstrated the superior performance of the CR wires compared to the NCR wires. The NCR wires frequently failed under higher electrical stress, making it difficult to continue the tests. Therefore, the rest of the studies involving higher stress levels were conducted only on the CR wires.

5.2 Effects of Overshoot, Frequency, and Duty Cycle on Corona-Resistant Wires

The back-to-back samples are subjected to a 24-hour aging process under unipolar rectangular pulses with 40 ns rise time and PD activities happening during the test period. Testing is conducted with varying pulse parameters, including overshoot, frequency, and duty cycle [83], [84]. The samples' insulation performance is assessed by measuring PDIV, percentage dissipation factor (%DF), sample temperature, and sample surface imaging before and after aging.

5.2.1 Test Conditions and Voltage Waveform Parameters

This section examines three pulse parameters, overshoot, frequency, and duty cycle, each at two levels. A full factorial DOE is used to structure the tests, resulting in eight experimental configurations for a comprehensive analysis of all parameter effects and interactions. Table 5.3 presents the specific levels used for each factor in the DOE process, while Table 5.4 summarizes the experiments designed based on these configurations. Other pulse parameters were kept constant, with a voltage of 2.5 kV and a rise time of 40 ns. The rising edge of the waveform used in the experiments is illustrated in Fig. 5.12. The aging tests are conducted at room temperature (24 °C) under intentional PD activities.

Table 5.3 High and low levels of the voltage waveform factors.

Factor	Identification	Low Level	High Level
Overshoot (%)	A	10	20
Frequency (kHz)	B	5	10
Duty Cycle (%)	C	20	50

Table 5.4 The test conditions and pulse parameters.

Test NO	Overshoot (%)	Frequency (kHz)	Duty Cycle (%)
T1	10	5	20
T2	10	5	50
T3	10	10	20
T4	10	10	50
T5	20	5	20
T6	20	5	50
T7	20	10	20
T8	20	10	50

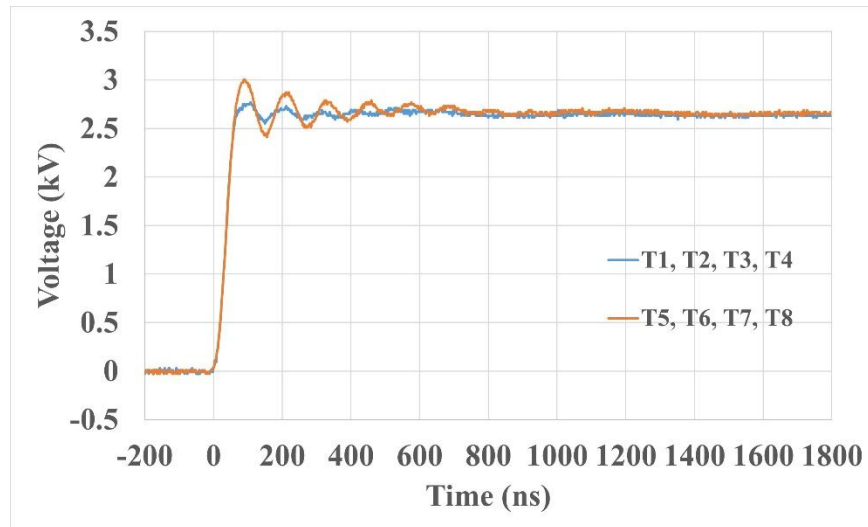
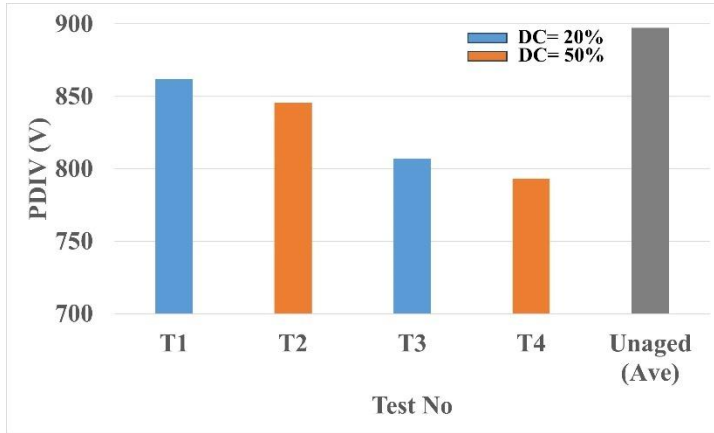


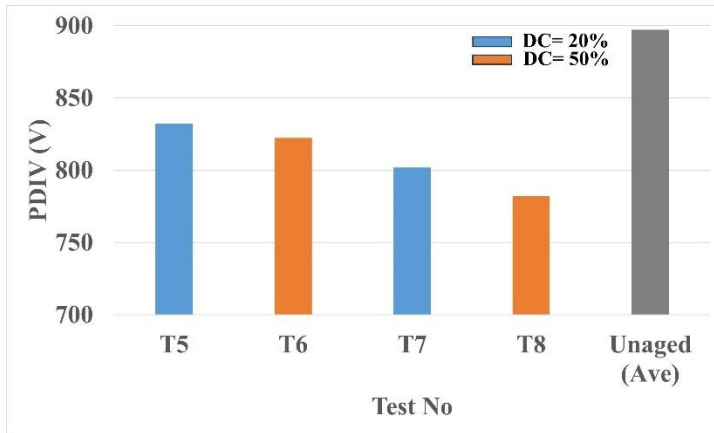
Fig. 5.12 The applied voltage waveshape of the pulse rising edge measured at the terminal of the test objects.

5.2.2 Measured PDIV Values of the Samples

The PDIV values measured at 10% and 20% overshoots are shown in Fig. 5.13 (a) and Fig. 5.13 (b), respectively. The PDIV data from aged samples are normalized to the average PDIV of unaged samples, which was measured at 897 V. Both plots indicate a consistent trend of PDIV drop with increased switching frequency and duty cycle (DC). Higher frequencies are expected to accelerate degradation due to greater energy deposition per unit of time, as PD signals occur more frequently, leading to intensified insulation damage. Additionally, higher frequencies contribute to localized heating from PD activities and repeated charge-discharge cycles, resulting in increased damage to the insulation. The elevated frequency also promotes more rapid growth of electrical trees, which can lead to insulation failure. A longer duty cycle further intensifies PDIV reduction due to increased thermal accumulation, higher average electrical stress, and enhanced PD activity that collectively accelerates cumulative damage.



(a)



(b)

Table 5.4 The test conditions and pulse parameters.

Test NO	Overshoot (%)	Frequency (kHz)	Duty Cycle (%)
T1	10	5	20
T2	10	5	50
T3	10	10	20
T4	10	10	50
T5	20	5	20
T6	20	5	50
T7	20	10	20
T8	20	10	50

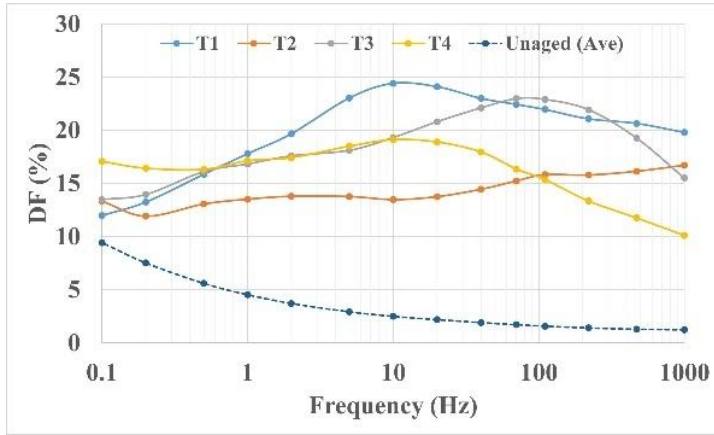
Fig. 5.13 The measured PDIV values of the aged samples at (a) 10% overshoot and (b) 20% overshoot.

Comparing Fig. 5.13 (a) and Fig. 5.13 (b), higher overshoot levels result in a more pronounced PDIV reduction due to increased electric field stress, elevated PD intensity, and a rise in temperature, all of which amplify insulation degradation.

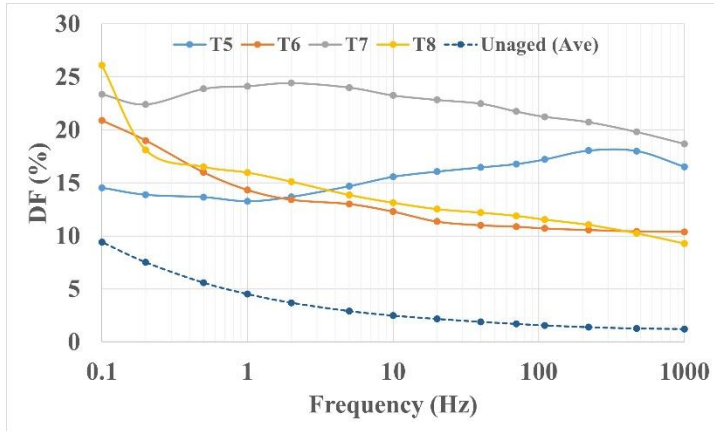
5.2.3 Measured DF Values of the Samples

The %DF measurements, recorded over a frequency range from 1 kHz to 0.1 Hz, are illustrated in Fig. 5.14 (a) and (b), normalized to the average %DF of unaged samples. Across all frequencies, %DF consistently increases, correlating with insulation damage from PD signals. Such degradation produces micro-voids and channels within the insulation, consequently raising the %DF. Damage accumulation is further accelerated by higher frequency and duty cycle, which increases the electrical stress.

The %DF results are compared at 0.1 Hz as a reference point in Fig. 5.15. Higher DF values are observed with higher duty cycle and frequency levels. %DF is consistently higher in the 20% overshoot condition in comparison to the 10% overshoot, as shown in Fig. 5.15 (a) and (b). For consistent comparison, DF data were normalized to the unaged samples' average DF of 9.4%. These %DF trends align with the observed PDIV drops previously discussed.



(a)

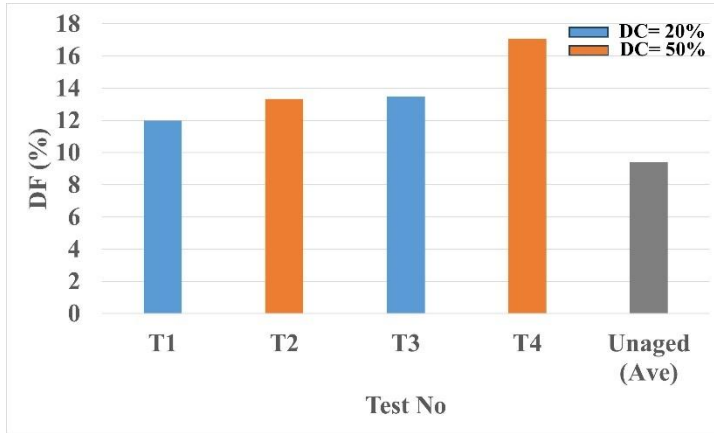


(b)

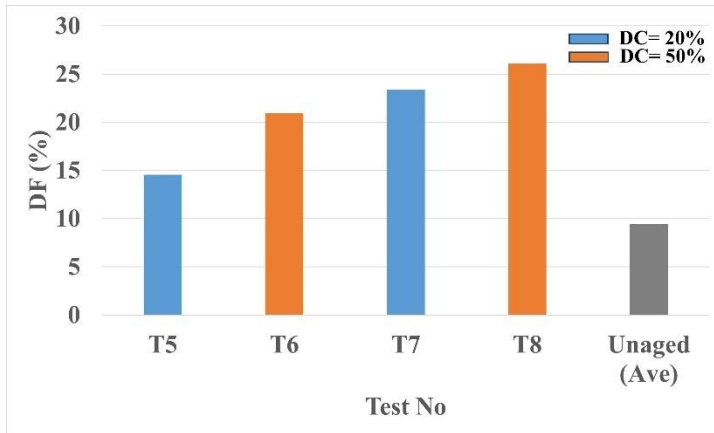
Table 5.4 The test conditions and pulse parameters.

Test NO	Overshoot (%)	Frequency (kHz)	Duty Cycle (%)
T1	10	5	20
T2	10	5	50
T3	10	10	20
T4	10	10	50
T5	20	5	20
T6	20	5	50
T7	20	10	20
T8	20	10	50

Fig. 5.14 The measured average DF values of the aged samples in a frequency sweep of 1 kHz down to 0.1 Hz at (a) 10% overshoot and (b) 20% overshoot.



(a)



(b)

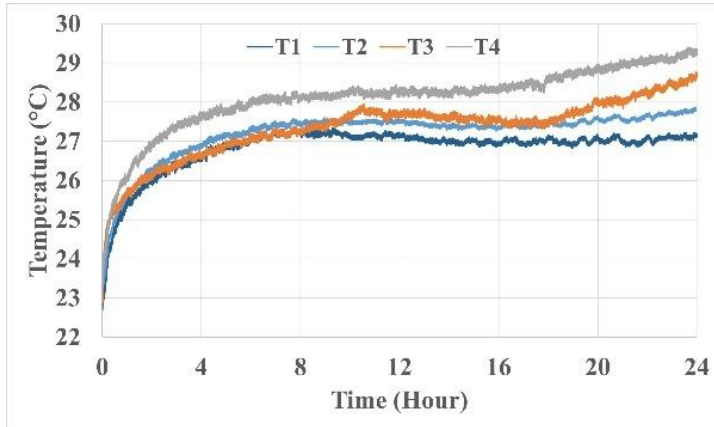
Table 5.4 The test conditions and pulse parameters.

Test NO	Overshoot (%)	Frequency (kHz)	Duty Cycle (%)
T1	10	5	20
T2	10	5	50
T3	10	10	20
T4	10	10	50
T5	20	5	20
T6	20	5	50
T7	20	10	20
T8	20	10	50

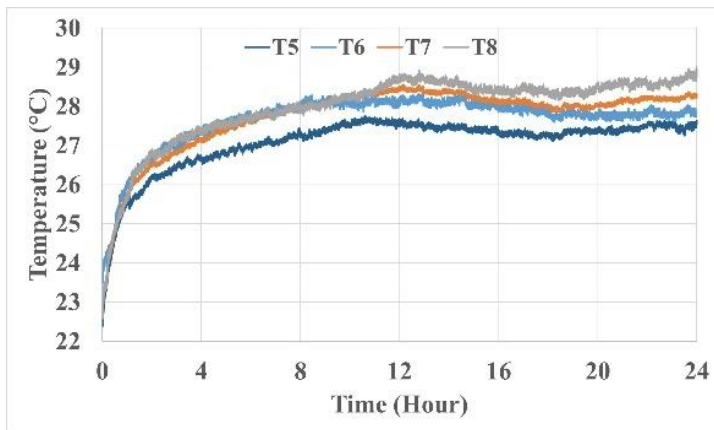
Fig. 5.15 The measured average DF values of the aged samples at 0.1 Hz at (a) 10% overshoot and (b) 20% overshoot.

5.2.4 Measured Temperature Values at the Crotch Area of the Samples

The average temperature at the wire exit area was continuously measured during the tests, with results plotted in Fig. 5.16 (a) and (b) for the 10% and 20% overshoot conditions, respectively. Temperature trends increase consistently with frequency and duty cycle. Higher frequency amplifies PD activity and, thus, temperature. Additionally, increased dielectric losses under higher frequencies contribute to further temperature rise. A longer duty cycle extends the period of electrical stress and allows more time for heat accumulation, which also raises average power loss and dielectric loss, resulting in higher temperatures. These thermal trends align with the observed PDIV reductions and DF increases.



(a)



(b)

Table 5.4 The test conditions and pulse parameters.

Test NO	Overshoot (%)	Frequency (kHz)	Duty Cycle (%)
T1	10	5	20
T2	10	5	50
T3	10	10	20
T4	10	10	50
T5	20	5	20
T6	20	5	50
T7	20	10	20
T8	20	10	50

Fig. 5.16 The measured temperature of the endpoint of the samples during the experiments at (a) 10% overshoot and (b) 20% overshoot.

5.2.5 Optical Microscope, AFM, and SEM Images from the Surface of the Wires

The wire surface degradation was evaluated through the microscope, AFM, and SEM imaging. Fig. 5.17 (a) and (b) show the microscope images at a magnification covering a 1×1.8 mm area. In Fig. 5.17 (b), insulation damage is evident, with the top insulation layer partially peeled away, exposing the middle CR material layer. The white residues are the inorganic substances that form the middle CR layer.

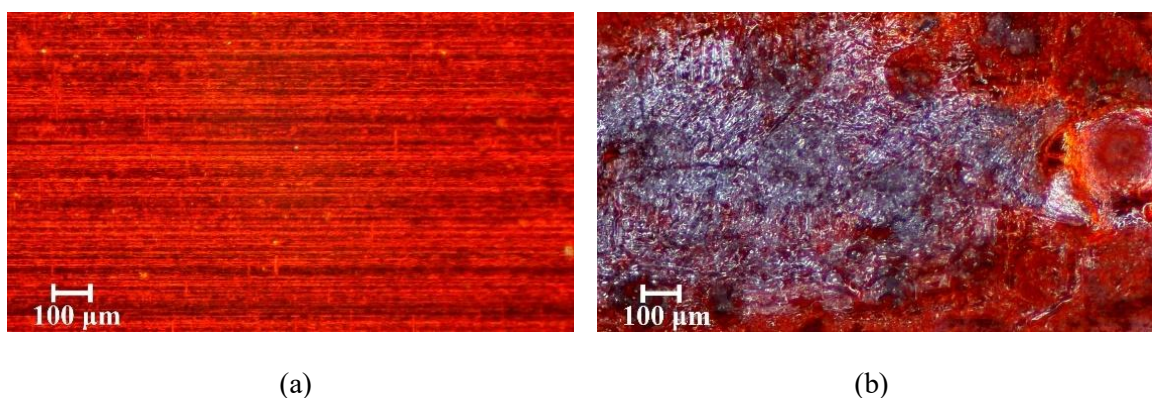
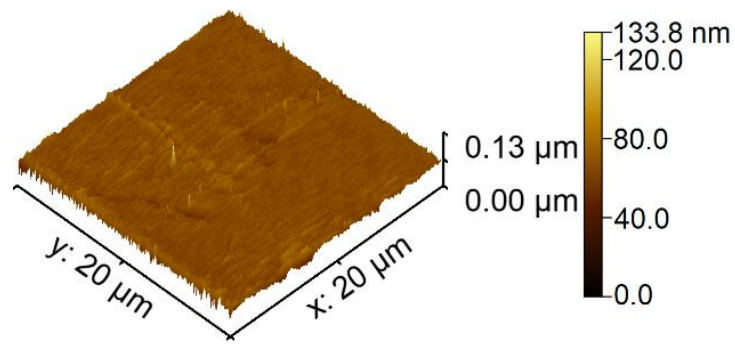


Fig. 5.17 The optical microscope images from the surface of the (a) unaged CR wire and (b) aged CR wire.

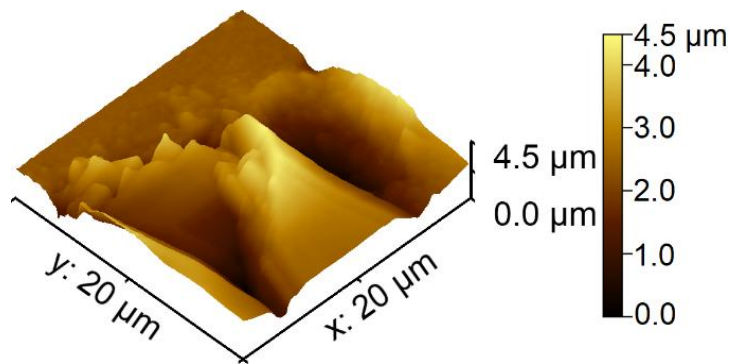
AFM topographical images quantitatively assessed surface roughness, covering a $20 \times 20 \mu\text{m}$ area, as shown in Fig. 5.18 (a) and (b) for unaged and aged samples, respectively. The rms roughness of the unaged wire was 4.9 nm, while the aged sample's roughness increased significantly to 733 nm, highlighting the pronounced difference in surface roughness. It should be noted that scanning different areas of the wires leads to different roughness values, but a considerable roughness difference between the unaged and aged samples was observed in all scans. This marked rise in roughness is indicative of severe insulation degradation attributed to PD activities.

The SEM images of the unaged and aged wires are presented in Fig. 5.19 and Fig. 5.20, respectively. The surface morphology of the unaged wire appears relatively smooth and uniform, while the aged sample exhibits clear signs of surface degradation caused by PD activity. In particular, localized erosion and roughened surface features can be observed, which indicate progressive deterioration of the insulation layer. These morphological changes are consistent with the expected damage mechanisms associated with PD-induced aging.

The SEM observations not only reveal the physical degradation of the insulation surface but also serve as the basis for subsequent EDX analysis in the next chapter, which is employed to investigate possible chemical and compositional changes in the enamel layer after aging.

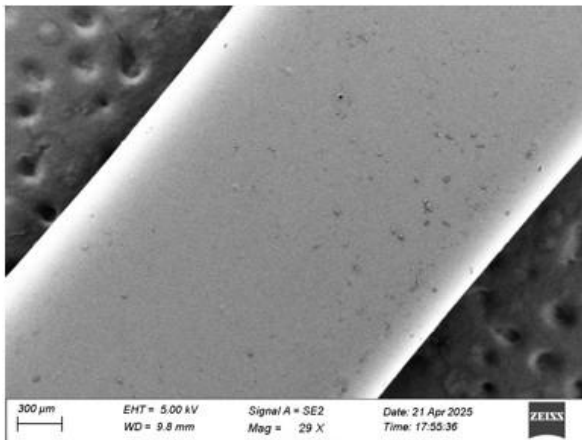


(a)

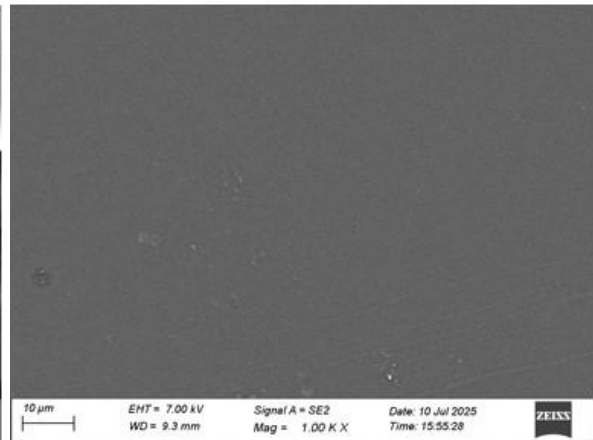


(b)

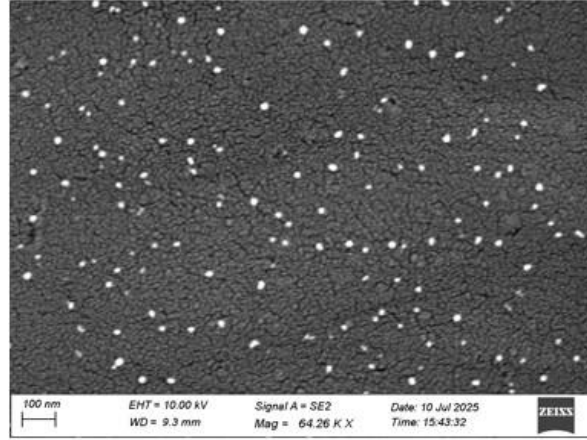
Fig. 5.18 The 3D AFM images of the surface of (a) the unaged CR wire and (b) the aged CR wire.



(a)

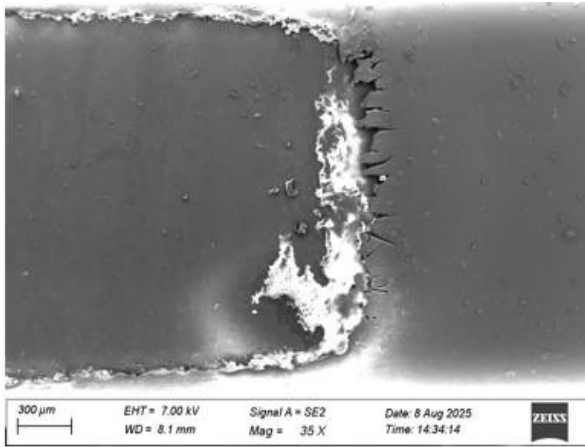


(b)

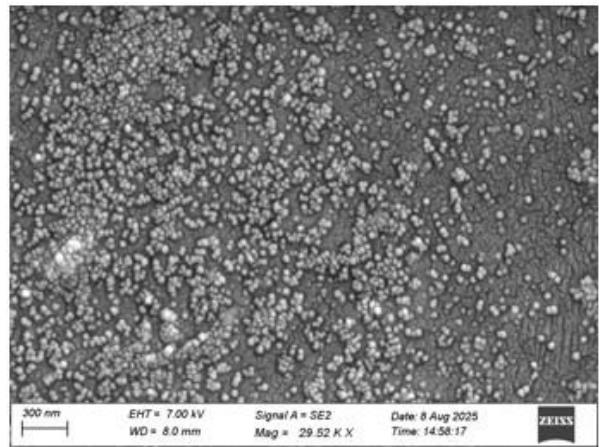


(c)

Fig. 5.19 The SEM images of the surface of the unaged CR wires at (a) 300 μm , (b) 10 μm , and (c) 100 nm magnification.



(a)



(b)

Fig. 5.20 The SEM images of the surface of the electrically aged CR wires at (a) 300 μm and (b) 300 nm magnification.

5.3 Effects of Thermal and Electrical Stress on Corona-Resistant Wires

The impact of the combined effects of thermal and electrical stress is evaluated in this section. Based on typical EV motor operating temperatures and the wire holders' thermal limitation, a test temperature of 100°C was selected for insulation aging experiments. To ensure thermal uniformity, two thermocouples were placed in proximity to the samples inside the oven. These thermocouples did not measure the temperature of the samples; rather, the ambient temperature inside the oven was monitored and controlled.

5.3.1 High Temperature Test

A controlled experiment was performed to confirm that the insulation does not degrade under purely thermal stress at 100°C over a 24-hour period. Five samples were tested, and their %DF and PDIV were measured before and after the thermal aging. The samples were subjected to thermal exposure without electrical stress for 24 hours. As illustrated in Fig. 5.21 and Fig. 5.22, no significant changes were observed in PDIV or %DF, confirming that thermal stress alone at 100°C does not lead to measurable insulation degradation.

To further validate this observation, microscopic imaging was conducted to examine potential surface degradation. As shown in Fig. 5.23, no visible changes were detected on the wire surface. The SEM images of the wire subjected to thermal aging are shown in Fig. 5.24. In comparison with the unaged wire (Fig. 5.19), no significant morphological changes can be observed. Consistent with the results from the optical microscope, the enamel surface appears largely intact. This aligns with the electrical measurement results, reinforcing the conclusion that thermal exposure at 100°C does not contribute to insulation deterioration under the given conditions. The PDIV and DF measurements were performed after a 24-hour resting period at room temperature to eliminate any transient effects.

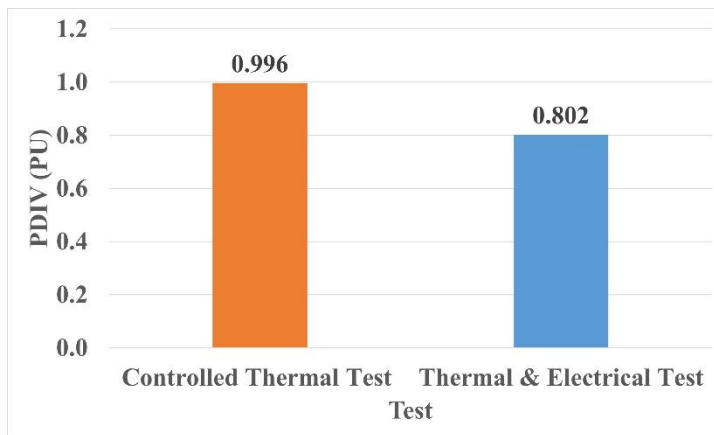


Fig. 5.21 The measured PDIV (PU) values of the aged samples of the controlled thermal test and the combined thermal and electrical test.

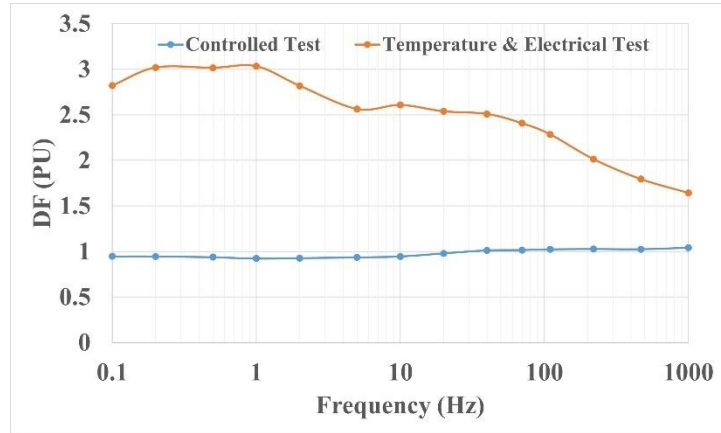


Fig. 5.22 The measured average %DF (PU) of the aged samples of the controlled test and the combined temperature and electrical test in a frequency sweep of 1 kHz down to 0.1 Hz.

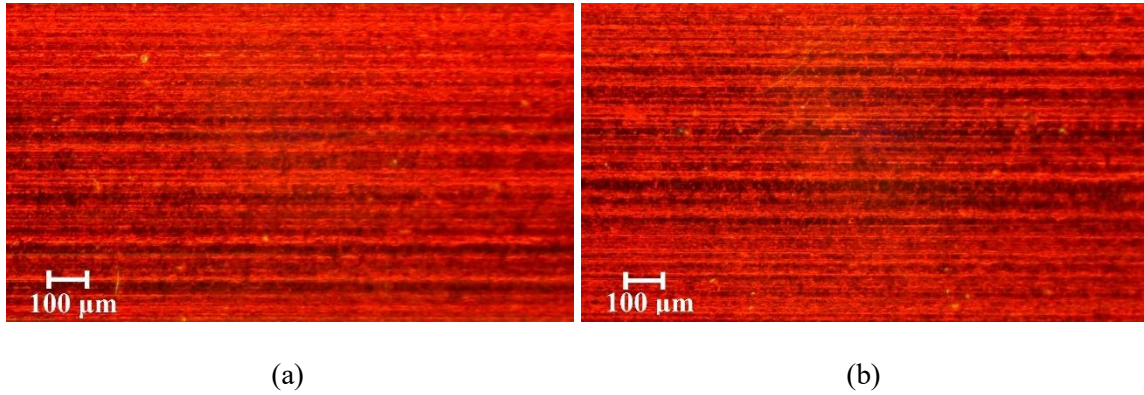


Fig. 5.23 The optical microscope images from the surface of the (a) unaged CR wire and (b) thermally aged CR wire.

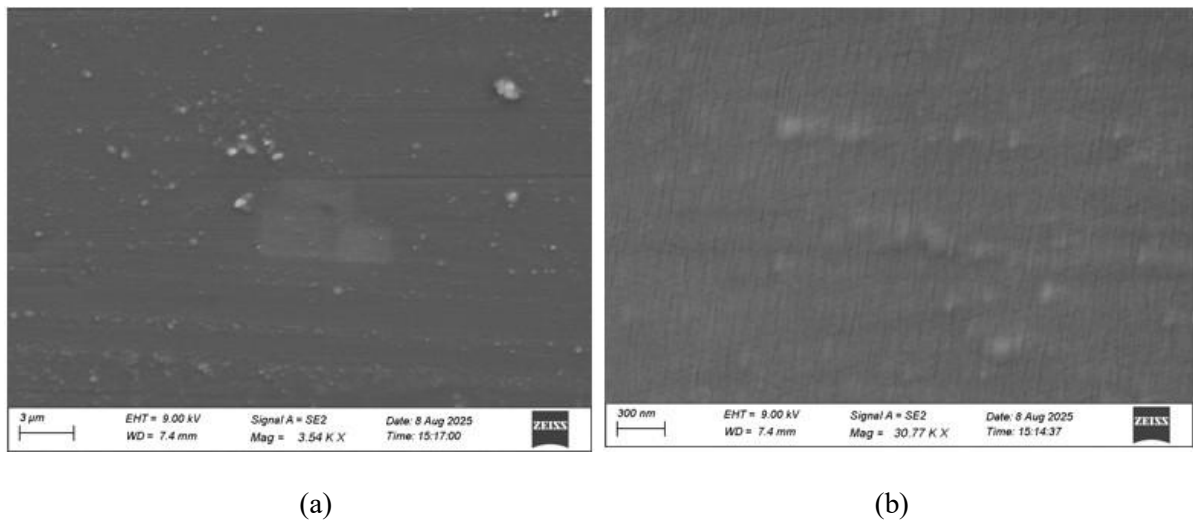


Fig. 5.24 The SEM images of the surface of the thermally aged CR wires at (a) 3 μm and (b) 300 nm magnification.

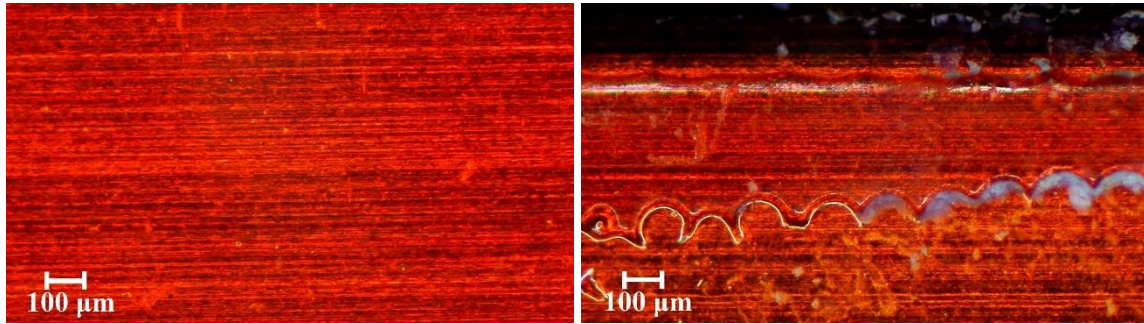
5.3.2 Combined Thermal and Electrical Stresses

To evaluate the impact of simultaneous thermal and electrical stress, aging experiments were conducted using pulse voltage stress characterized by a rise time of 40 ns, a frequency of 5 kHz, a duty cycle of 50%, and an overshoot of 10%. These tests were performed under the combined application of electrical and thermal stresses at 100°C under intentional PD activities for 24 hours.

Fig. 5.21 and Fig. 5.22 show a significant reduction in PDIV (by approximately 20%) and a considerable increase in %DF, indicating severe insulation degradation. Microscopic images further support these findings, as evident in Fig. 5.25 and Fig. 5.26. Fig. 5.25 (b) highlights extensive surface damage, with portions of the first insulation layer being removed, exposing the underlying CR layer. The comparison between unaged and aged wires in Fig. 5.26 provides additional confirmation of insulation deterioration. These results demonstrate that while thermal stress alone does not degrade the insulation at 100°C, the combination of thermal and electrical stress significantly accelerates degradation.

The insulation system of the tested enamel wire is based on a multilayer structure, where each of the three insulation layers consists of multiple sublayers. As shown in Fig. 5.26, some sublayers of the primary insulation layer have been peeled off along the contact areas of the wires. This progressive delamination suggests that the interaction between thermal and electrical stress considerably accelerates insulation degradation, underscoring the necessity for optimized insulation design in high-temperature, high-voltage applications.

The SEM images in Fig. 5.27 clearly reveal intense damage to the wire surface after combined thermal and electrical aging. Compared to the samples exposed to electrical stress alone (Fig. 5.20), the surface degradation appears more pronounced, with deeper erosion marks, extensive cracking, and a rougher morphology. This indicates that the simultaneous action of thermal and electrical stresses accelerates the degradation of the enamel layer, leading to more severe insulation deterioration.



(a)

(b)

Fig. 5.25 The optical microscope images from the surface of the (a) unaged CR wire and (b) thermally & electrically aged CR wire.

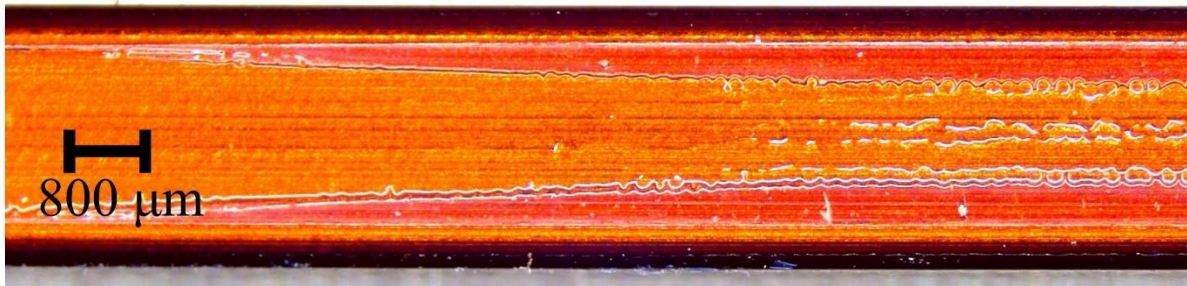
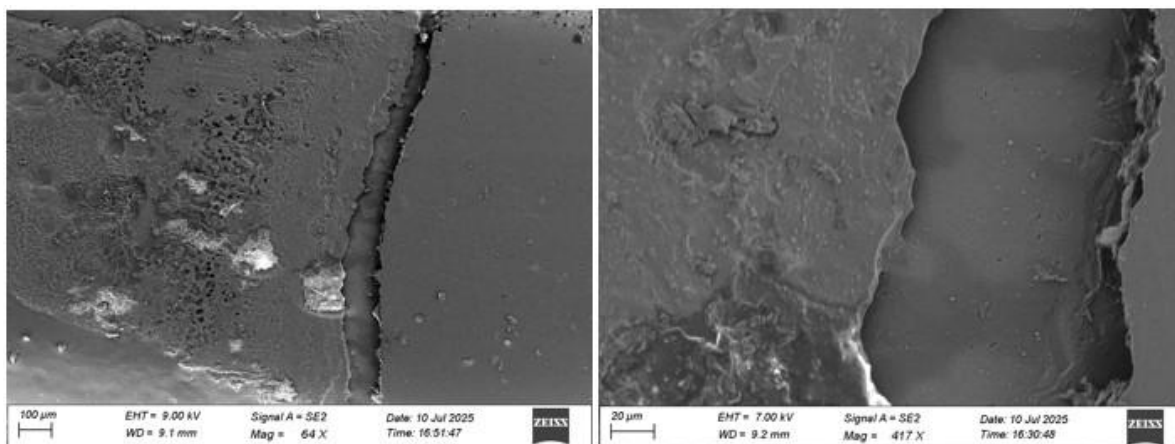
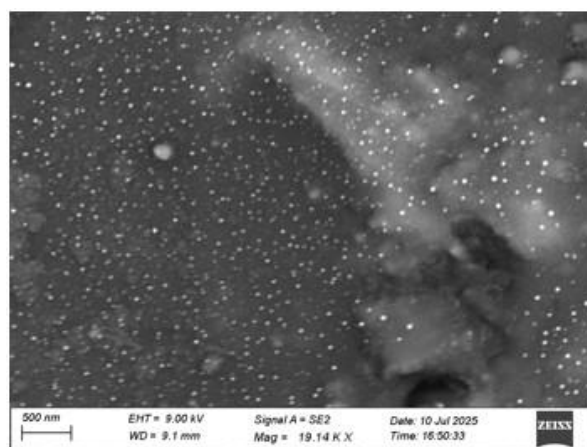


Fig. 5.26 The optical microscope image from the surface of the thermally and electrically aged CR wire.



(a)

(b)



(c)

Fig. 5.27 The SEM images of the surface of the combined thermally and electrically aged CR wires at (a) 100 μm (b) 20 μm , and (c) 500 nm magnification.

Chapter 6

Discussion

This chapter presents the characterization of pulse parameters and examines the effect of each parameter on insulation performance, including discussions on their interactions. Additionally, it addresses the combined effects of thermal and electrical stresses, the electric field distribution along the wire, and the resulting surface damage.

6.1 Rise Time and Overshoot Effects on Enamel Insulation Performance

6.1.1 Rise Time Effect on Enamel Insulation Performance

The experimental results indicate that faster pulse rise times lead to a more pronounced decrease in PDIV and an increase in DF across all test conditions. This phenomenon can be attributed to multiple mechanisms that influence the degradation of the insulation system.

One primary factor contributing to this trend is the increased PD energy deposition per pulse when the rise time is shorter. A steeper voltage transition results in a more rapid charge accumulation within the dielectric material, intensifying the local electric field stress. This abrupt stress application accelerates the initiation of PD activity, as the insulation is exposed to sharper voltage differentials over shorter time intervals. Consequently, the dielectric material experiences higher localized energy dissipation, leading to accelerated thermal and physical degradation [27], [85].

Additionally, the interaction between fast rise-time pulses and the insulation structure enhances the likelihood of charge trapping and localized heating. The intensified electric field associated with rapid transitions can lead to increased space charge accumulation at material interfaces or defects, further distorting the local field distribution and creating weak points in the insulation. Over prolonged exposure, these weak points develop into failure spots, progressively reducing the PDIV as the insulation becomes less capable of withstanding voltage stresses [18], [22], [27], [86].

Thermal effects also play a role in the observed insulation damage. The rapid voltage transitions generate localized heating due to resistive and dielectric losses in the enamel coating. This heating effect is particularly critical in polymeric insulation materials, as elevated temperatures can initiate physicochemical processes, beginning with increased chain mobility, followed by polymer chain

scission, ultimately leading to material degradation. Thus, as the polymer structure weakens, its ability to resist electrical discharges diminishes, further degrading the insulation [27].

Another significant factor is the intensity of the PD pulses associated with faster rise times. Steeper pulses generate stronger transient electric fields, increasing the magnitude of PD occurrences per cycle. This is related to the statistical and formative time lag of PD signals. The statistical time lag is the time from the moment that the field is high enough to initiate PD and the appearance of the initiatory electron. The formative time lag is defined as the time required for the initiatory electron for ionization and discharge development. A faster rise time will lead to the generation of a PD signal at a higher voltage, which results in a larger PD magnitude [25], [62]. This heightened discharge activity accelerates insulation deterioration by promoting surface erosion and void expansion. As PD activity persists, the insulation becomes increasingly susceptible to further degradation, reinforcing the trend of higher damage [18], [22], [27], [86]. This highlights the importance of considering the fast rise time pulses generated by the WBG device-based power converters.

6.1.2 Overshoot Effect on Enamel Insulation Performance

When comparing test conditions with 10% OS and 20% OS in the previous chapter, it is evident that higher overshoot results in more severe insulation degradation. This behavior can be attributed to multiple interrelated factors, including intensified electric field stress, increased PD activity, and elevated thermal stress.

One of the primary reasons for the accelerated PDIV reduction and DF increase at higher overshoot levels is the increased electrical field stress imposed on the insulation. Overshoot represents a transient overvoltage condition that exceeds the nominal peak voltage, subjecting the insulation to extreme electric field conditions. This elevated field stress is particularly harmful at weak points such as microvoids, defects, or dielectric interfaces, where localized field enhancement can trigger early PD activity [22], [85], [87], [88], [89], [90]. Repeated exposure to such extreme stress weakens the insulation structure over time, leading to more significant insulation damage.

In addition to the higher field stress, increased overshoot correlates with intense and frequent PD occurrences. The sharper and more pronounced voltage spikes associated with higher overshoot can promote stronger ionization processes within voids or weak regions of the insulation, increasing the intensity of PD events [18], [22]. Thermal effects also play a role in this degradation process. The voltage spikes induced by overshoot lead to a more severe localized heating within the insulation

material. As the insulation undergoes repeated thermal stress due to the pulse voltages with overshoots, mechanical fatigue can develop, contributing to crack formation and further loss of dielectric strength [27].

6.1.3 Pulse Rise Time and Overshoot Effects' Characterization

PDIV and DF were the primary insulation performance metrics used in this study. The percentage changes in PDIV ($\% \Delta$ PDIV) and $\%DF$ ($\% \Delta$ DF) values at 0.1 Hz before and after the aging tests from the previous chapter are summarized in Table 6.1.

Table 6.1 The $\% \Delta$ PDIV and $\% \Delta$ DF results at 0.1 HZ.

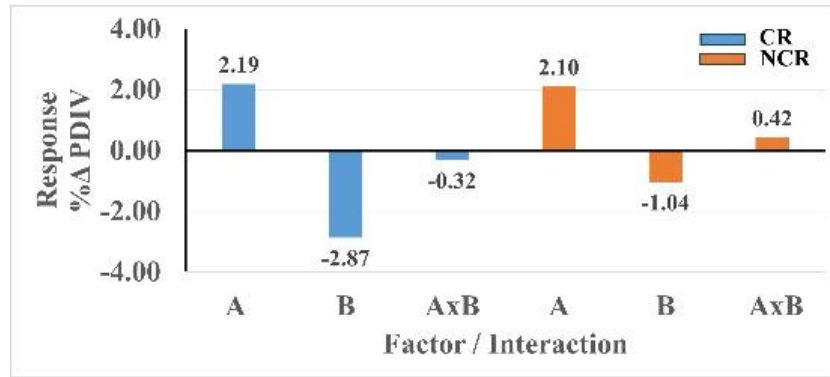
Test No	Parameter	$\% \Delta$ PDIV	$\% \Delta$ DF
T1		3.79	57.76
T2		8.43	118.73
T3		2.92	78.4
T4		7.37	103.04
T5		1.24	54.31
T6		6.97	77.36
T7		6.3	148.72
T8		10.11	240.06
T9		3.49	108.95
T10		9.85	149.12
T11		3.11	83.94
T12		9.49	122.35

The results in Table 6.1 reveal that the average $\% \Delta$ PDIV for the CR wire samples is 3.5%, while it is 8.7% for the NCR wire samples, about 2.5 times higher. The highest $\% \Delta$ PDIV occurred in T8, with a 10.1% drop after aging, and the lowest in T5, with only a 1.2% drop. T8 corresponds to the test with NCR wires, the fastest rise time (40 ns), and 20% OS, while T5 represents the test with CR wires, the slowest rise time (800 ns), and 10% OS.

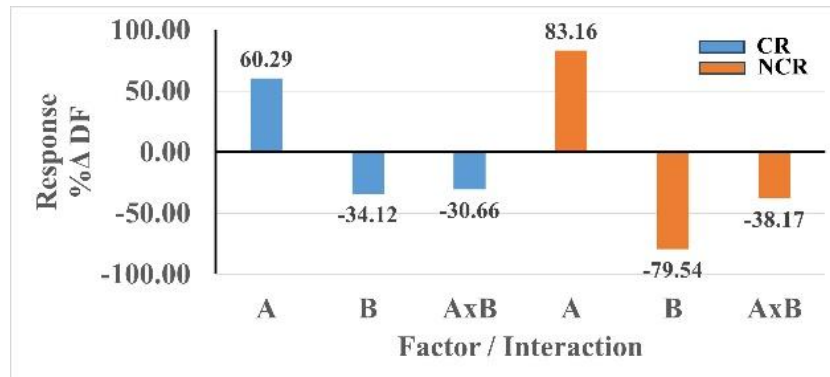
Regarding the $\% \Delta$ DF values at 0.1 Hz, the average $\% \Delta$ DF for the CR wire samples is 88.7%, compared to 135.1% for the NCR wire samples, 1.52 times higher. The highest $\% \Delta$ DF increase was

observed in T8, while the lowest was in T5. These findings suggest that the insulation degradation rate under PD activities is significantly higher for NCR wires compared to CR wires [91], [92].

While the experimental results and trends have been discussed in the previous chapter, it is essential to understand the effect of each factor and the interactions between them. Therefore, to analyze the results and identify the main effects and interactions on PDIV and DF, the low and high levels of the factors are considered. The low and high levels of these factors are presented in Table 5.1, and their effects and interactions are illustrated in Fig. 6.1 (a) and (b).



(a)



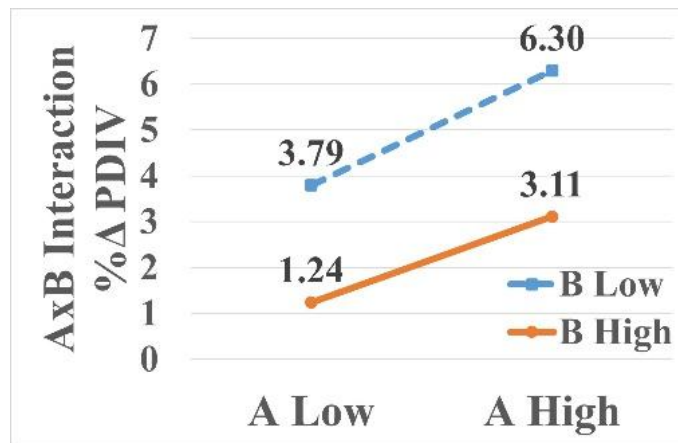
(b)

Fig. 6.1 Main effect and interaction of the factors considering (a) %Δ PDIV and (b) %Δ DF as a response.

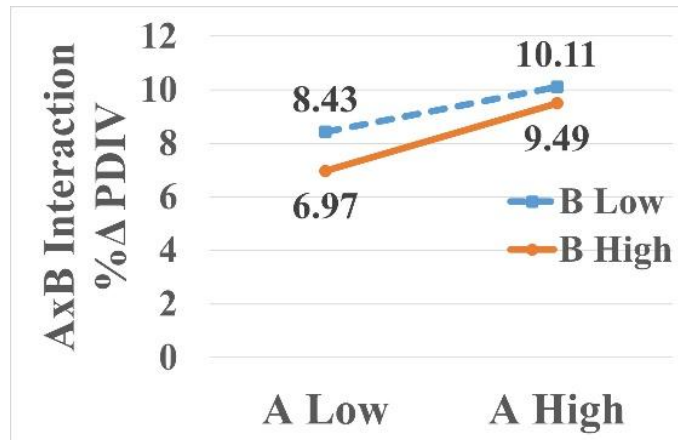
As shown in Fig. 6.1 (a), overshoot directly influences the PDIV drop in the CR wire, while the rise time and the interaction between the factors inversely impact the changes in PDIV values after aging. The negative effect of rise time (factor B) indicates that increasing the rise time reduces the PDIV drop, meaning slower rise times result in less PDIV drop. The same pattern is observed on the right side of

Fig. 6.1 (a) for the NCR wire regarding the effects of OS and rise time. However, unlike the CR wire, there is no negative interaction between the factors for the NCR wire.

The effects of OS, rise time, and their interaction on the DF increase after aging for both the CR and NCR wires are shown in Fig. 6.1 (b). OS directly affects DF, while rise time and the interaction between these factors inversely impact the changes in DF values after aging for both wires. Notably, the effects of each factor and their interaction are more pronounced for the NCR wire compared to the CR wire. Similar to its effect on PDIV, the rise time effect (factor B) is negative for both wires, meaning that increasing the rise time from 40 ns to 800 ns reduces the DF increase after aging.

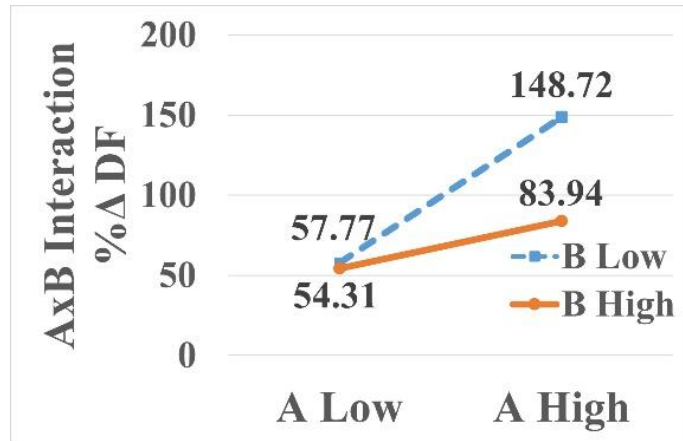


(a)

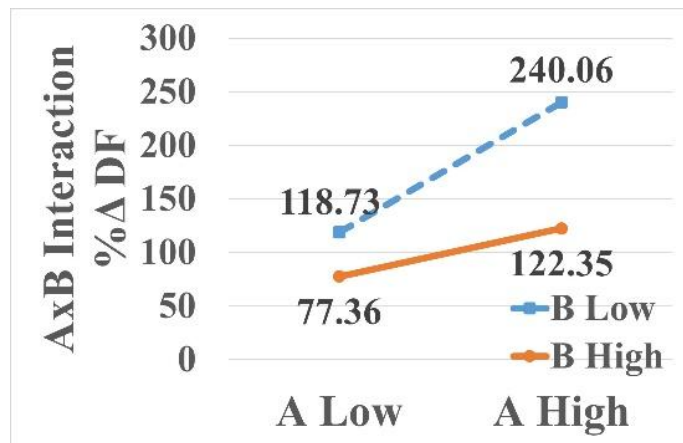


(b)

Fig. 6.2 Interaction plots of the %Δ PDIV for (a) CR wires and (b) NCR wires.



(a)



(b)

Fig. 6.3 Interaction plots of the %Δ DF for (a) CR wires and (b) NCR wires.

To better illustrate the main effects and the interaction between the factors influencing PDIV and DF, Fig. 6.2 and Fig. 6.3 have been provided, respectively. The interaction plot for PDIV in the CR wire is shown in Fig. 6.2 (a), which indicates that there is no significant interaction between the factors. The rise time emerges as the main factor affecting the PDIV drop in the CR wire, slightly higher than the effect of OS, as seen in Fig. 6.2 (a). Moreover, the impact of OS is more severe at the lower level of factor B (faster rise time) compared to the higher level of factor B.

In contrast, Fig. 6.2 (b), representing the NCR wire, shows a slightly higher interaction than Fig. 6.2 (a), although it still remains insignificant. The main effect on PDIV in the NCR wire is attributed to OS, which has a greater impact than the rise time. Similar to the CR wire, the OS effect is more prominent at faster rise times. However, the difference in OS effect between low and high levels of factor B is more substantial in the CR wire (Fig. 6.2 (a)) than in the NCR wire (Fig. 6.2 (b)), though the overall effect is more severe in the NCR wire. Additionally, the rise time shows a greater influence on the higher levels of factor A (higher OS) in both plots.

The interaction plots for DF are depicted in Fig. 6.3 (a) and (b), revealing significant interactions between the factors in both cases. For the CR wire, both OS and rise time have considerable effects on DF changes, with the effect of OS being almost twice as strong as that of rise time. In the case of the NCR wire, OS and rise time also significantly influence DF, although the impact of OS is slightly higher. Furthermore, increasing OS has a more pronounced effect at faster rise times for both wires. Consistent with the PDIV results, the overall impact is considerably more severe on the NCR wires than on the CR wires.

6.2 Overshoot, Frequency, and Duty Cycle Effects on Enamel Insulation Performance

6.2.1 Frequency Effect on Enamel Insulation Performance

The results indicate that higher switching frequencies accelerate insulation degradation, leading to a more pronounced reduction in the PDIV. This degradation is attributed to several interrelated mechanisms, including increased energy deposition per unit time, intensified PD activity, and localized heating effects.

One of the primary reasons for the increased rate of degradation at higher frequencies is the greater energy deposition per unit of time. Since PD events occur more frequently in high-frequency conditions (PD per unit of time), the cumulative energy injected into the insulation system rises significantly [19], [25]. This repeated exposure to PD-induced energy leads to a higher degradation rate.

In addition to energy deposition, higher frequencies intensify insulation degradation by increasing localized heating effects. The continuous occurrence of PD activity and charge-discharge cycles at a higher rate generates additional thermal stress in the insulation system. Over time, the combination of thermal and electrical stresses contribute to accelerated aging, crack formation, and material deterioration [18], [19], [25], [52].

Another contributing factor is the effect of frequency on charge dynamics within the insulation. At higher frequencies, charge carriers generated by PD events do not have sufficient time to dissipate before the next voltage cycle begins. This leads to charge accumulation at defect spots, intensifying local electric field stress and further reducing the PDIV. Additionally, the presence of residual space charges can distort the local electric field distribution, intensifying the development of weak points in the insulation.

6.2.2 Duty Cycle Effect on Enamel Insulation Performance

The higher insulation degradation rates with higher duty cycle settings observed in the results are due to multiple interrelated factors, including increased thermal accumulation, prolonged exposure to high electrical stress, and enhanced PD activity, all of which contribute to cumulative insulation damage over time.

One of the primary factors influencing PDIV reduction at higher duty cycles is the accumulation of space charge. A longer duty cycle means that the HV pulses remain active for a greater proportion of the switching period, reducing the charge relaxation time. As a result, heat generated from both conduction losses and PD activity accumulates within the insulation system, leading to a steady rise in temperature [25], [52]. Over time, these changes weaken the dielectric properties of the insulation, making it more susceptible to electrical breakdown and PDIV reduction.

In addition to thermal effects, a higher duty cycle leads to prolonged exposure to high electric field stress. This increased exposure can cause gradual degradation of dielectric strength due to charge accumulation at weak points, increased space charge effects, and enhanced electric field distortions. The continuous stress reduces the insulation's ability to recover between pulses, leading to faster aging and premature failure.

Furthermore, a longer duty cycle enhances PD activity, which plays a crucial role in insulation deterioration. When the duty cycle is extended, the number of PD events occurring within a given time frame can increase. The cumulative effect of this repetitive PD activity accelerates insulation erosion, promoting surface degradation, electrical treeing, and micro-cracking.

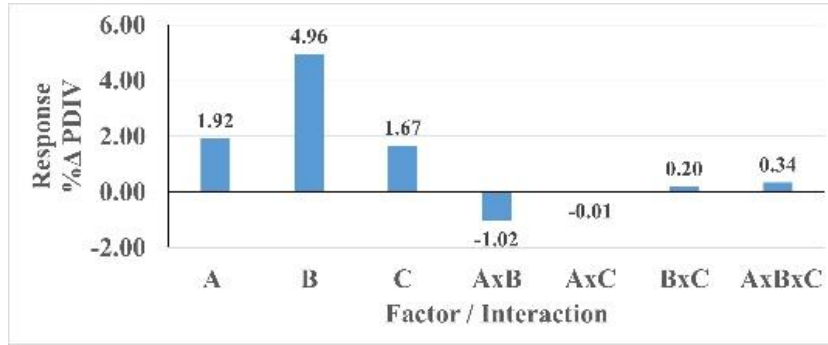
6.2.3 Pulse Overshoot, Frequency, and Duty Cycle Effects' Characterization

To further analyze the effects of overshoot, frequency, and duty cycle, the percentage changes in PDIV ($\% \Delta$ PDIV) and %DF ($\% \Delta$ DF) at 0.1 Hz are summarized in Table 6.2. Using Table 6.2, the

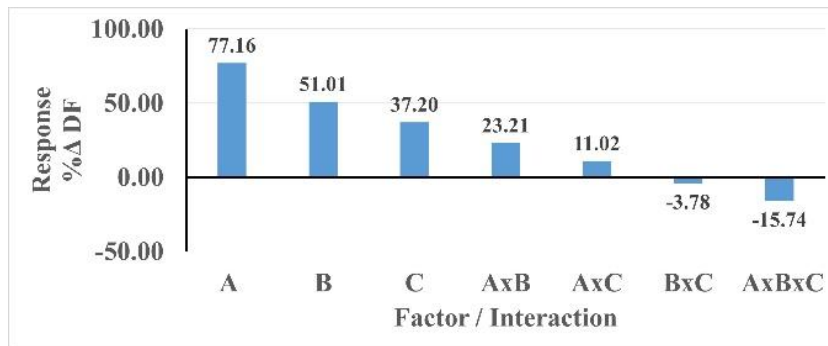
individual effects and interactions among the factors were analyzed and presented in Fig. 6.4 (a) and (b).

Table 6.2 The % Δ PDIV and % Δ DF Results.

Test No	Parameter	% Δ PDIV	% Δ DF
T1		3.91	27.37
T2		5.74	41.59
T3		10.03	43.20
T4		11.57	81.35
T5		7.20	54.56
T6		8.32	122.30
T7		10.60	148.30
T8		12.81	177.01



(a)



(b)

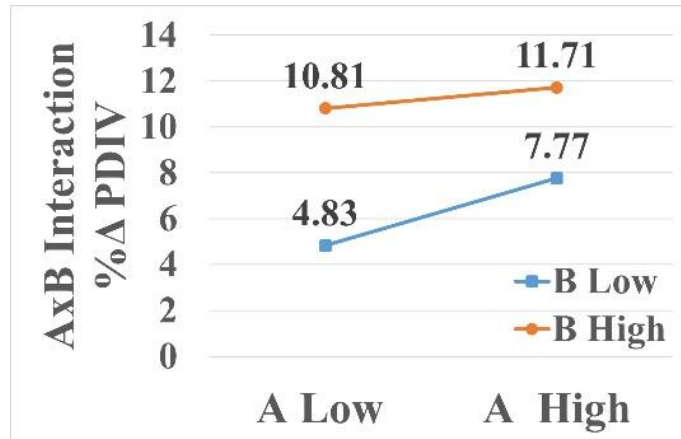
Fig. 6.4 Main effect and interaction of the factors considering (a) %Δ PDIV and (b) %Δ DF as a response.

Overshoot, frequency, and duty cycle all directly influence the PDIV drop, with frequency having the most significant effect, as shown in Fig. 6.4 (a). There is no considerable interaction between the factors other than the interaction between overshoot and frequency, which inversely affects the PDIV drop.

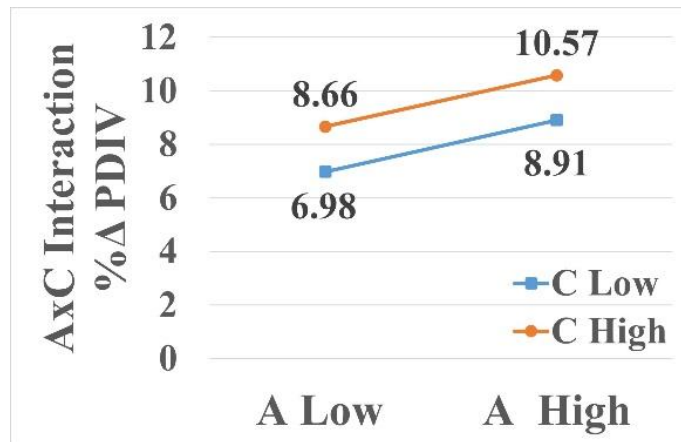
In Fig. 6.4 (b), all factors contribute to an increase in DF, with overshoot having the main effect, which aligns with findings from the effects of rise time and overshoot. Notable positive interactions exist between overshoot-frequency ($A \times B$) and overshoot-duty cycle ($A \times C$), while frequency-duty cycle ($B \times C$) and the combined $A \times B \times C$ interactions are negative, although the $B \times C$ interaction is minimal.

Interaction plots for %Δ PDIV and %Δ DF are provided in Fig. 6.5 and Fig. 6.6, respectively, to further clarify factor effects. Looking at Fig. 6.5, there is no interaction between the factors other than $A \times B$ interaction. The frequency effect on PDIV drop (Fig. 6.5 (a)) is more pronounced than the overshoot effect, as is the frequency effect relative to the duty cycle (Fig. 6.5 (c)). Similarly, overshoot

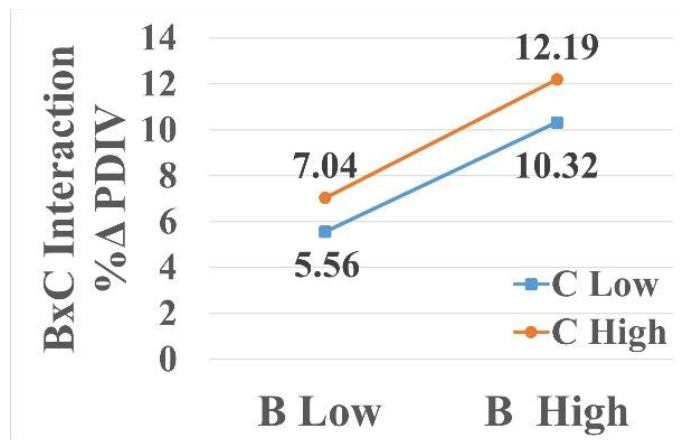
has a greater impact than the duty cycle (Fig. 6.5 (b)). Looking at Fig. 6.5, the effect of each factor is more severe at the higher level of the other factors, e.g., considering Fig. 6.5 (a), frequency has a more severe effect on PDIV drop at a higher overshoot value, and overshoot has a higher impact at the higher level of frequency. This pattern is consistent across all factor pairings.



(a)

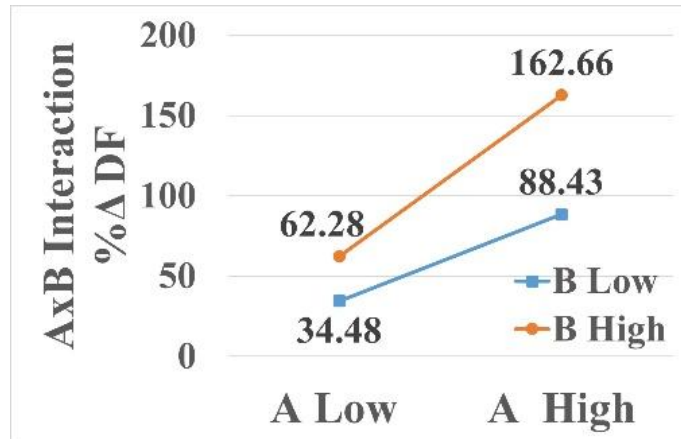


(b)

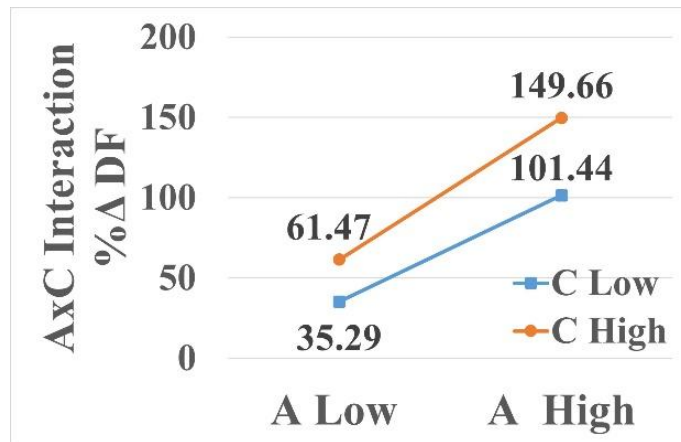


(c)

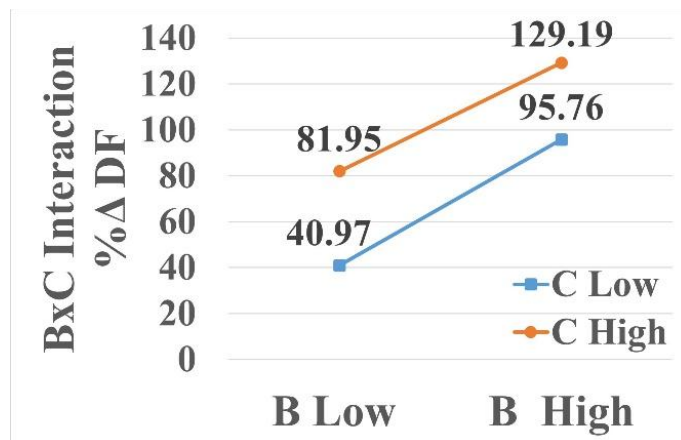
Fig. 6.5 Interaction plots of the %Δ PDIV for the factors (a) A and B, (b) A and C, and (c) B and C.



(a)



(b)



(c)

Fig. 6.6 Interaction plots of the $\% \Delta DF$ for the factors (a) A and B, (b) A and C, and (c) B and C.

For % Δ DF, the highest interaction is again between overshoot and frequency (A $\times$ B), as depicted in Fig. 6.6. Overshoot shows a stronger influence on the DF increase than either frequency (Fig. 6.6 (a)) or duty cycle (Fig. 6.6 (b)), with frequency having a greater effect than duty cycle (Fig. 6.6 (c)). Similar to the PDIV results, each factor's effect on DF is more severe at higher levels of the other factors.

Collectively, the PDIV and DF results demonstrate that higher overshoot, frequency, and duty cycle lead to an accelerated insulation degradation rate. These findings are consistent with previous studies examining the impact of overshoot, frequency, and duty cycle on PD activity and time to failure of turn-to-turn insulation [18], [19], [25], [52].

6.3 Temperature Effect on Enamel Insulation Performance

The impact of temperature on insulation degradation, in conjunction with electrical stress, was examined in Section 5.3. To isolate the effect of temperature, a comparative analysis is conducted between two aging tests performed under identical electrical stress conditions: 10% overshoot, 50% duty cycle, 5 kHz switching frequency, and 40 ns rise time. One test is conducted at room temperature, while the other is carried out at 100°C. The results reveal a significant difference in insulation degradation between the two conditions, as evidenced by the post-aging per-unit values of PDIV drop presented in Fig. 6.7.

To assess the influence of the oven's chamber on the experimental results, a controlled experiment was performed. In this experiment, the same test previously conducted at standard room temperature and ambient conditions was repeated inside the oven, with the oven temperature set to match the room temperature (24°C). Since the oven's closed chamber does not have any source of humidity, this setup allowed the effect of ambient humidity to be eliminated from the result at room temperature. It was confirmed that all the damage to the wires was caused by PD, not the environment, and the absence of humidity variation did not alter the experimental outcome. Therefore, the results obtained from experiments conducted in the oven at 24 °C are similar to those performed under open room conditions. The outcomes of the controlled experiment are presented in Fig. 6.7 and Fig. 6.8.

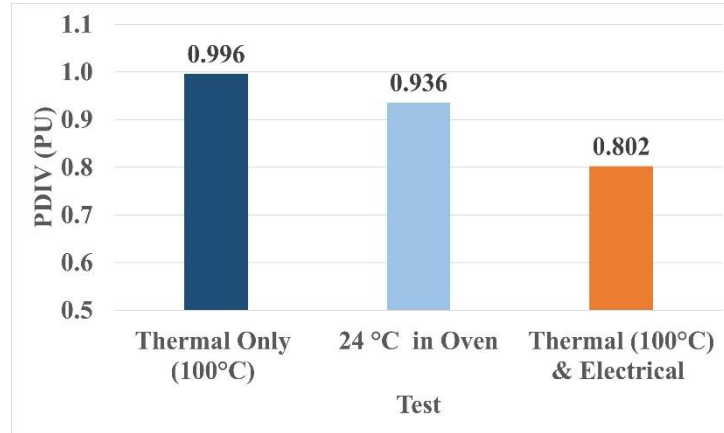


Fig. 6.7 The measured PDIV (PU) of the tests in the oven.

The %DF was also measured before and after aging, normalized to the average values before aging. The results, shown in Fig. 6.8, indicate that %DF increased more for the high-temperature (combined with electrical) test than for the room-temperature test at lower measurement frequencies. This suggests a pronounced deterioration in insulation performance under elevated thermal conditions.

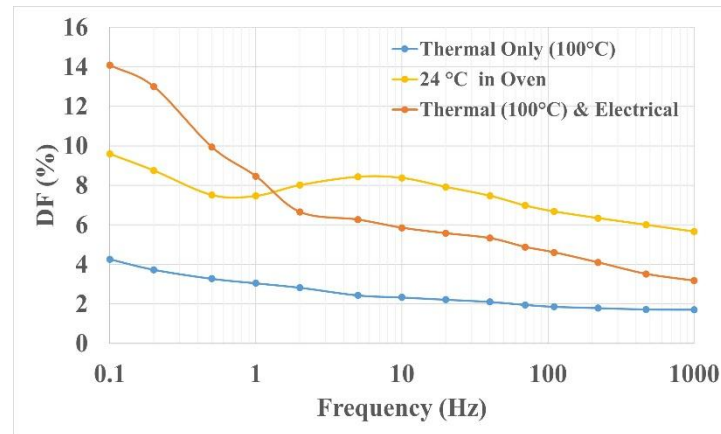


Fig. 6.8 The measured average DF values of the aged samples in a frequency sweep of 1 kHz down to 0.1 Hz.

The combined effects of elevated temperature, electrical stress, and PD activity accelerate insulation degradation and erosion. Higher temperatures increase charge carrier mobility, dielectric loss, and permittivity, all of which facilitate PD initiation and expansion, further intensifying insulation deterioration. The simultaneous application of thermal and electrical stresses creates a compounding effect, where electrical stress alone induces localized defects due to high field intensities, while thermal

stress accelerates defect propagation. This synergy leads to a significantly higher rate of insulation degradation [16], [21], [36], [37].

6.4 Wire Surface Degradation Analysis

6.4.1 Optical Analysis of Wire Surface

The high field region at the wire edge was examined in one of the experiments, where the test was intentionally allowed to continue after the failure. The resulting failure image in Fig. 6.9, shows edge blackening, and this was observed across all tests, but the wire failure test was conducted to show the intensified situation.

The damage observed on the wire surface in Fig. 6.9, is due to the PD activities happening between the wires [44], [89]. PD can erode the surface insulation of the wire, as illustrated in Fig. 5.17 (b), where the first insulation layer of the CR wire has been peeled away. The white residues visible in Fig. 5.17 (b) are remnants of the CR material, which were also reported in [44].

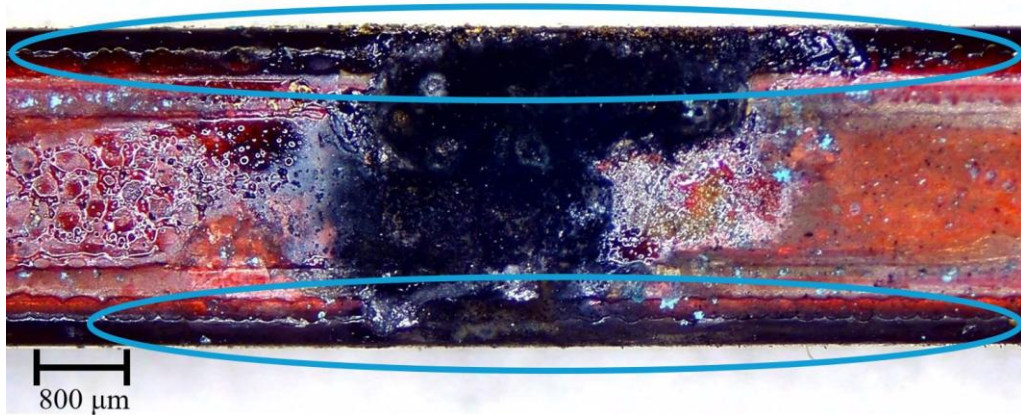


Fig. 6.9 The intentionally failed sample showing the high-field regions on the wire edge.

6.4.2 EDX Analysis of Wire Surface Degradation

Energy Dispersive X-ray Analysis (EDX) was performed to quantitatively evaluate the elemental composition of the enamel surface and to investigate the chemical mechanisms underlying insulation degradation under different stress conditions. The CR wire enamel is based on polyamide-imide (PAI), and its general chemical structure is shown in Fig. 6.10. The relative atomic percentages of carbon and oxygen detected on the wire surface for unaged, thermally aged, electrically aged, and combined thermally and electrically aged samples are presented in Fig. 6.11.

The EDX results clearly indicate that the carbon concentration on the enamel surface decreases with increasing severity of aging, with the most pronounced reduction observed under combined thermal and electrical stress. This reduction in carbon content can be attributed to bond breaking within the polymer backbone, primarily induced by the localized high-energy PDs. Conversely, the oxygen content increases consistently with aging severity, which reflects the strong oxidative nature of the PD degradation process. The EDX analysis data for all stress scenarios are provided in Appendix A.

A strong correlation exists between the EDX data (Fig. 6.11) and the electrical characterization and the surface imaging results. For the unaged and purely thermally aged wires, the carbon and oxygen contents remain nearly unchanged, indicating negligible chemical degradation at 100 °C in the absence of electrical stress. This finding is consistent with the electrical measurements, where no measurable variation was observed in PDIV or %DF before and after thermal aging, as shown in Fig. 5.21 and Fig. 5.22. Morphological observations through optical microscopy (Fig. 5.23) and SEM Imaging (Fig. 5.24) further confirm the absence of visible degradation in thermally aged samples.

In contrast, electrical aging introduces compositional changes, with reduced carbon and increased oxygen content, and these effects are intensified in the combined thermal and electrical condition. This behavior aligns well with the electrical measurements shown in Fig. 6.7 and Fig. 6.8, where PDIV decreases and %DF increases after both electrical and combined aging tests. The degradation is more severe when both stress mechanisms act simultaneously, suggesting a synergistic effect between thermal and electrical stresses that accelerates the insulation degradation. The optical microscope and SEM results are also consistent with this trend; the electrically aged wires (Fig. 5.17 and Fig. 5.20) exhibit moderate surface erosion, whereas the combined thermally and electrically aged wires (Fig. 5.25, Fig. 5.26, and Fig. 5.27) show extensive damage.

In conclusion, EDX, PDIV, %DF, and wire surface imaging results (optical and SEM) collectively provide a coherent picture of the degradation mechanism. All results consistently demonstrate that thermal stress alone at 100 °C produces negligible enamel damage, while electrical stress accelerates material degradation. The most severe insulation deterioration occurs under combined thermal and electrical stresses. These findings highlight the strong interplay between chemical, electrical, and morphological changes in enamel insulation systems subjected to simultaneous stress factors.

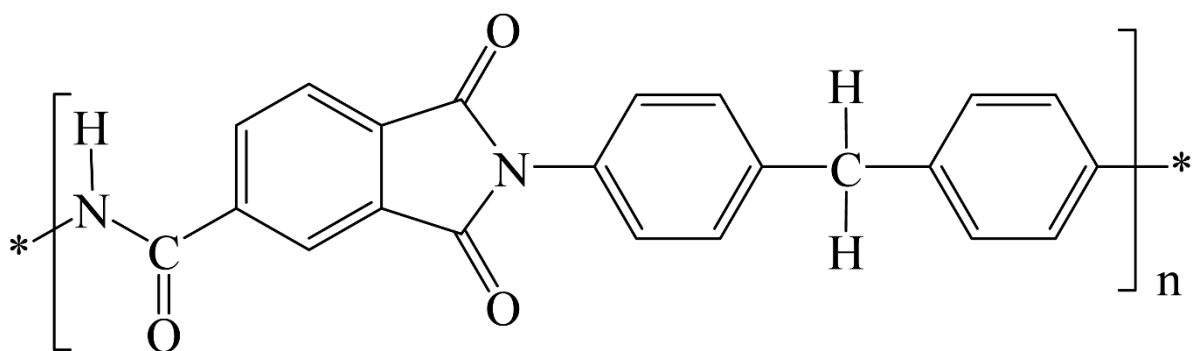


Fig. 6.10 Chemical structure of poly (amide imide) monometric unit [93].

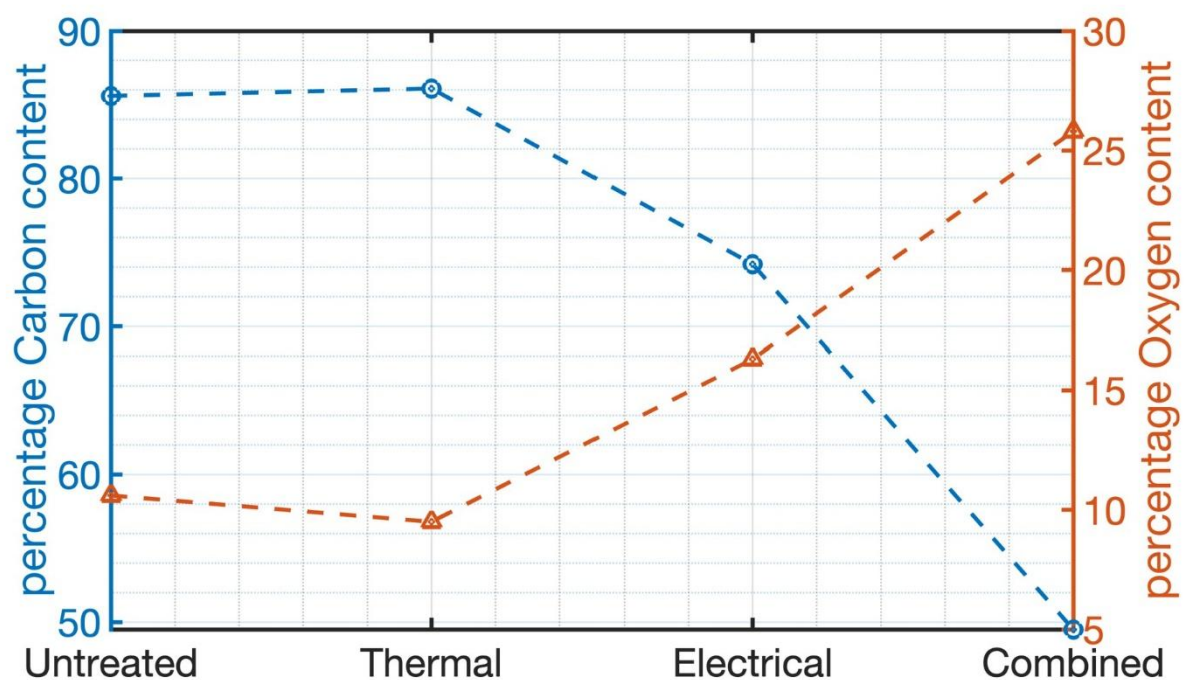


Fig. 6.11 The comparison plot showing the Carbon and Oxygen percentage content on the CR wire surfaces under different stress conditions.

Chapter 7

Conclusion and Suggestions for Future Work

7.1 Summary

The objective of this research was to systematically investigate the impact of the integration of wide-bandgap (WBG) device-based power converters and hairpin winding on the turn-to-turn insulation performance of electric vehicle (EV) hairpin-wound traction motors. Recent advances in WBG devices, such as silicon carbide (SiC) MOSFETs, enable high-frequency and fast-switching operation of power converters, which improves power density and efficiency but also subjects motor windings to high dv/dt stress and partial discharge (PD) activity. At the same time, the adoption of hairpin winding in EV traction motors has led to a different motor winding type, rather than random-wound windings. These two improvements, when combined, present new reliability challenges that remain insufficiently addressed in the literature. This work tries to fill this gap by experimentally evaluating the degradation mechanisms of hairpin winding insulation under the operation of WBG device-based-driven stress conditions and PD activities.

To achieve this goal, a back-to-back wire configuration was developed to emulate the turn-to-turn insulation of hairpin windings. Two types of magnet wires used in EV motors, corona-resistant (CR) and non-corona-resistant (NCR), were tested. An SiC-MOSFET-based high-voltage pulse generator was designed and developed to apply repetitive square-wave pulses with controlled rise time, overshoot, frequency, and duty cycle. These parameters were selected to replicate the fast transient conditions encountered in WBG device-based inverters. In addition, the influence of thermal stress was studied by evaluating the combined effect of elevated temperature and repetitive voltage pulses on insulation degradation. A full-factorial design of experiments (DOE) was employed to capture both the main effects and interaction effects of the studied parameters.

The aging experiments were performed for 24 hours. Insulation performance was quantitatively assessed before and after aging using partial discharge inception voltage (PDIV) measurements and dielectric frequency response (DFR) analysis. Temperature rise during testing was recorded with an infrared thermal camera, particularly at the crotch area of the samples. Surface degradation was investigated using optical microscopy, atomic force microscopy (AFM), and scanning electron

microscopy (SEM), providing morphological evidence of insulation erosion. Complementary to these tests, Energy-Dispersive X-ray Analysis (EDX) was employed to quantify elemental composition changes (carbon depletion and oxygen enrichment), thereby linking chemical degradation results with electrical and morphological findings.

Overall, the results provide a comprehensive understanding of the mechanisms governing turn-to-turn insulation degradation in EV hairpin windings when subjected to WBG device-based converter stress profiles. By integrating electrical, thermal, chemical, and surface imaging analyses, this work establishes direct correlations between PD activity, temperature measurements, polymer breakdown, PDIV, and %DF in insulation performance analysis.

7.2 Conclusions

The following conclusions are drawn from this research:

- Corona-resistant (CR) wires exhibited significantly superior insulation stability compared to non-corona-resistant (NCR) wires, with the average percentage PDIV drop in CR wires being approximately 2.5 times smaller.
- In the investigation of rise time and overshoot effects, rise time was identified as the main factor influencing the PDIV drop in CR wires, whereas overshoot was the dominant factor for PDIV reduction in NCR wires.
- Studying the rise time and overshoot effect, overshoot was the primary factor for the increase in the percentage dissipation factor (%DF) in both CR and NCR wires. However, CR wires exhibited a % Δ DF increase approximately 1.5 times smaller than that of NCR wires, reflecting their improved resistance to PD-induced degradation. Also, NCR wires showed a more pronounced increase in capacitance compared to CR wires.
- Optical microscope and AFM imaging revealed less severe surface degradation and erosion from PD activity on CR wires, further validating their superior resistance under PD.
- Surface temperature measurements at the crotch area consistently showed lower values for CR wires, which correlated with their improved insulation stability and reduced damage compared to NCR wires.
- By evaluating the effects of overshoot, frequency, and duty cycle on CR wires, it was determined that frequency was the dominant factor influencing PDIV reduction, while duty cycle had the least impact.

- The combined action of thermal and electrical stresses was found to drastically accelerate insulation degradation, confirming a strong synergistic effect between the two mechanisms.
- SEM imaging and EDX analysis further substantiated the influence of different stress conditions on the enamel insulation, demonstrating progressive surface cracking, carbon depletion, and oxygen enrichment.

7.3 Contributions

- A back-to-back wire sample configuration was developed to effectively study turn-to-turn insulation degradation in hairpin windings, while mitigating the limitations associated with crotch-area issues. By employing actual EV motor wires in the proposed design, this setup provides a more accurate and representative model of turn-to-turn insulation behavior in hairpin winding applications.
- An advanced WBG device-based power converter was proposed, designed, and developed for insulation testing. The proposed SiC-MOSFET-based high-voltage pulse generator allows control of pulse parameters, including rise time, overshoot, frequency, duty cycle, and waveform shape, addressing a critical gap in both industry and research for insulation testing under WBG device-based stress conditions.
- The effects of different pulse parameters on turn-to-turn insulation performance were systematically studied, compared, and characterized. This provides valuable insights into the role of fast-switching transients and PD activity in accelerating insulation degradation in hairpin windings operated with WBG device-based drives.
- The combined influence of thermal and electrical stresses on turn-to-turn insulation was evaluated, highlighting the synergistic effect of temperature and repetitive pulse stress on the acceleration of aging mechanisms.
- The different degradation rates under various test conditions, with and without thermal stress, were quantified. The results were validated through multi-measurement techniques that combined EDX elemental analysis, electrical measurements (PDIV and DFR), and surface imaging (optical microscopy, AFM, SEM).
- The findings of this research provide new insights into insulation reliability in WBG device-based EV motors. In the absence of established testing standards for hairpin winding insulation under the electrical stress from WBG device-based drives, the findings of this

work may lay the groundwork for the development of future guidelines that complement existing standards, such as IEC 60034-18-41 for low-voltage machines.

7.4 Suggestions for Future Work

The suggestions for future work are listed below:

- Conduct testing on complete stator windings under WBG device-based drive operation to evaluate the insulation performance of a fully wound machine in the presence of PD activity, thereby extending the findings from wire-level testing to machine-level validation.
- Investigate the effect of bipolar voltage pulses on turn-to-turn insulation performance. While this work examined the influence of unipolar pulse parameters (rise time, overshoot, frequency, and duty cycle), the impact of bipolar pulses combined with PD activity remains to be assessed.
- Perform more detailed material-level analyses of the insulation to characterize chemical and structural changes after aging under PD activity. It is recommended to analyze degradation pathways and byproducts to support the development of mitigation strategies and improved insulation materials.
- Test insulation samples under varying environmental conditions, such as different air pressures and humidity levels. This line of work could be further expanded to assess insulation performance in other transportation electrification domains, such as electric aircraft, where operating conditions differ significantly from EV applications.

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Appendix A

EDX Analysis Results

The EDX analysis results obtained from SEM imaging are presented below to investigate the material changes that occurred on the surface of the CR wires under different aging conditions.

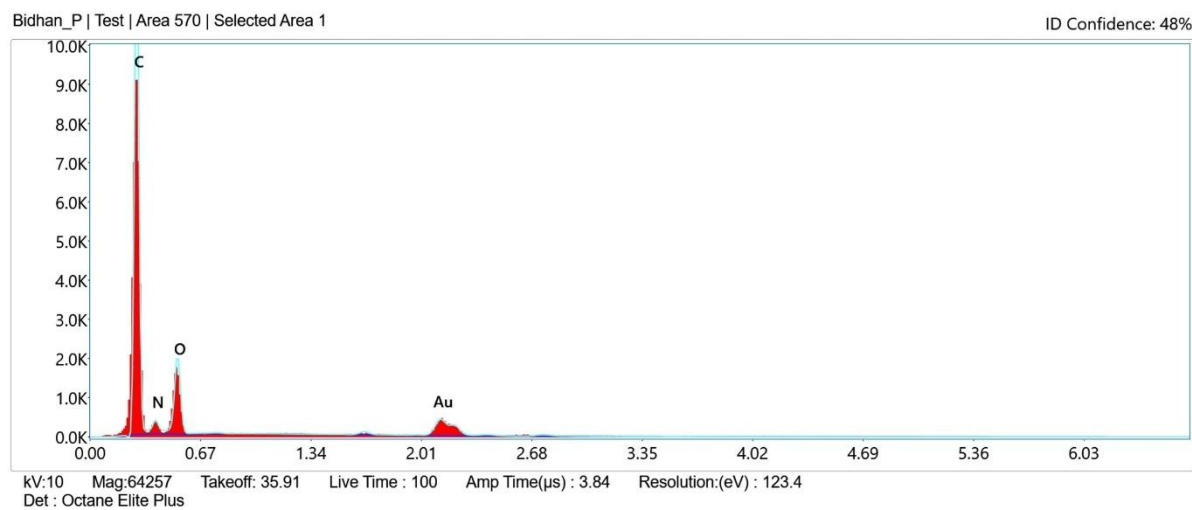


Fig. A.1 The EDX result from the surface of the unaged CR wire.

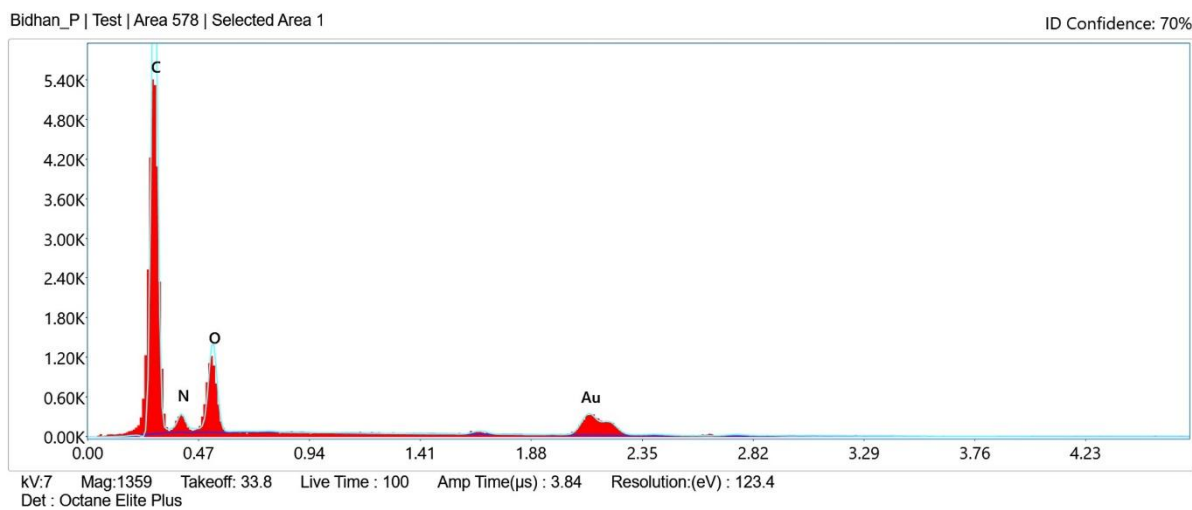


Fig. A.2 The EDX result from the surface of the thermally aged CR wire.

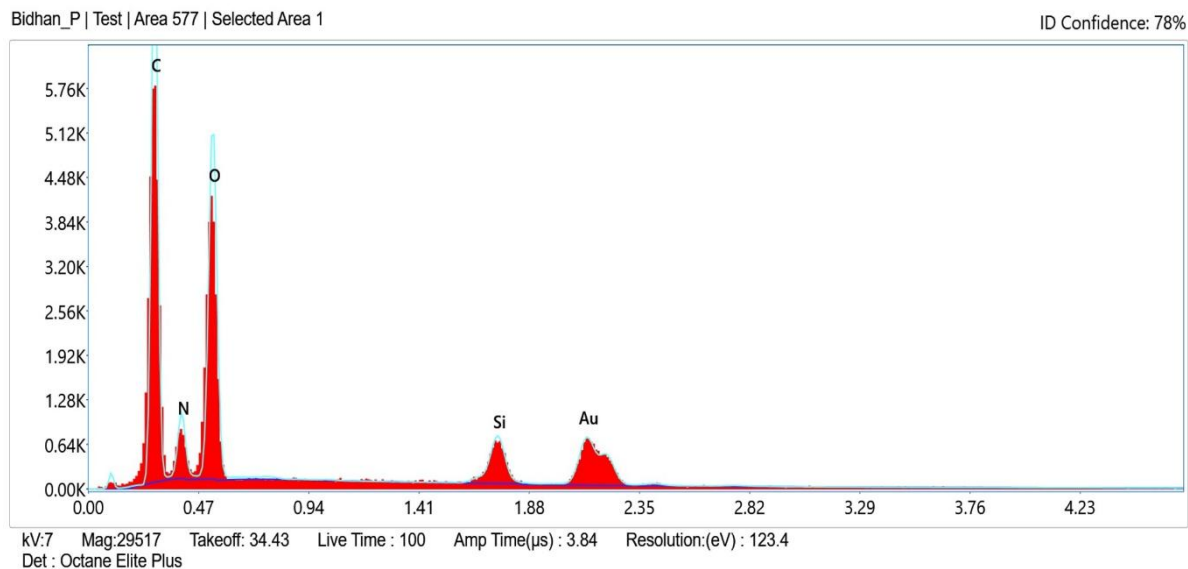


Fig. A.3 The EDX result from the surface of the electrically aged CR wire.

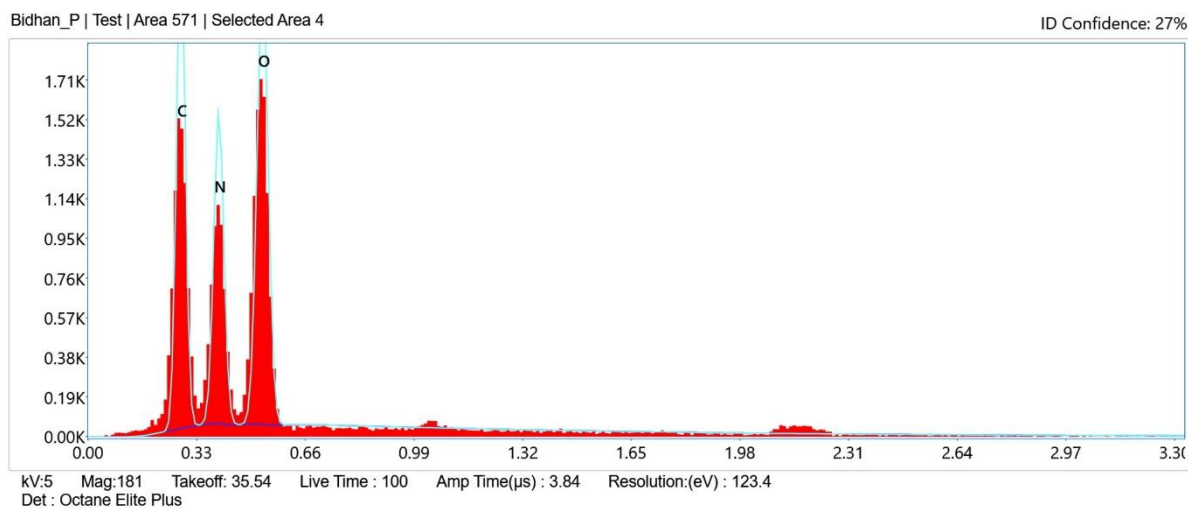


Fig. A.4 The EDX result from the surface of the thermally and electrically aged CR wire.

For the unaged wire (Fig. A.1), the spectrum is dominated by carbon (C), with smaller contributions from oxygen (O) and nitrogen (N), which is consistent with the organic nature of the enamel insulation. A distinct gold (Au) peak is also present, originating from the surface coating used in the SEM imaging process. No additional elements are detected within the scanned area, and the absence of copper (Cu) peaks confirms that the enamel remains intact, fully covering the conductor. The lack of metallic or inorganic signatures further suggests that the surface is free from contamination and that the insulation is chemically in its initial state.

The thermally aged wire (Fig. A.2) exhibits nearly identical elemental characteristics to the unaged sample. The spectrum remains C-rich, with the same O and minor N contributions, confirming the polymeric composition of the enamel. These results indicate that thermal stress at 100 °C does not induce detectable chemical degradation of the insulation surface. This finding is consistent with the earlier microscopic, SEM observations, and electrical insulation measurements, where no significant changes were identified under thermal-only aging.

In contrast, the electrically aged wire (Fig. A.3) shows a pronounced increase in oxygen content compared to the unaged sample, reflecting oxidation of the enamel surface caused by PD activity and the associated generation of ozone. Additionally, silicon (Si) is detected in the spectrum. While the exact origin of Si requires further analysis, its presence might be due to the exposure of the filler.

For the combined thermal and electrical aging (Fig. A.4), a similar but more pronounced trend is observed. The oxygen content increases further, consistent with accelerated oxidative degradation under the higher stress caused by heat and PD. Nitrogen levels are also higher than in both the unaged and electrically aged samples, suggesting additional chemical modifications of the enamel. These combined stresses appear to intensify the chemical breakdown of the insulation surface compared to individual stress factors.