Physics-based Compact Model of GaN/AlGaN Schottky Barrier Diode and SiC MOSFET

by

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Author's Declaration

This thesis consists of material all of which I authored or co-authored: see Statement of Contributions included in the thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Statement of Contributions

Chapter 3 uses the content of the following publication.

Y. Feng, R. Fang, M. Xiao, J. Alant, J. Chong, H. Wang, Y. Zhang, U. Radhakrishna, L. Wei. Physics-based Compact Model for Multi-channel AlGaN/GaN Schottky Barrier Diodes. In *the 35th International Symposium on Power Semiconductor Devices and ICs. ISPSD 2024*. Bremen, June 2024. [1]

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The use of their content in this thesis have been approved by all co-authors.

Abstract

Silicon Carbide (SiC) and Gallium Nitride (GaN) are actively employed in Power Electronics (PE) circuits due to their superior material properties. They both have wide bandgap, high carrier saturation velocity and high thermal conductivity, enabling High Voltage (HV), High Frequency (HF) and High Power (HP) applications. Besides using materials with superior properties, device structure innovations further improve power device performance, such as multi-dimensional structures including super-junction, multi-channel (stacked 2-Dimensional Electron Gas (2DEG)) and FinFETs. Compared with one-dimensional structure, it could enhance trade-off between Breakdown Voltage (BV) and On-state Resistance (R_{ON}).

In order to facilitate circuit design using SiC/GaN transistors with innovative device architectures, there is a growing demand of accurate, scalable, robust and standardized compact models. Using an innovative modular approach, this thesis first proposes a compact model for multi-channel AlGaN/GaN Schottky Barrier Diode (SBD) for kilo-volt applications. The modelling approach, detailed model formation as well as model evaluation against an experimental SBD with five stacked 2DEG channels are explained in detail. Using a similar modular formulation method, the thesis also proposes Waterloo Virtual-source SiC Compact Model (WAVSiC), a comprehensive and user-friendly physics-based compact model for SiC MOSFETs. Accuracy, flexibility and scalability are demonstrated for WAVSiC via benchmarking against measurements of commercial devices. The WAVSiC model is also validated for computational efficiency and robustness, circuit simulator compatibility and ready for Process Design Kit (PDK) integration.

In summary, by using a modular approach, the thesis introduces two innovative physics-based compact models for wide-bandgap power electronic devices with accuracy, scalability, and computational efficiency, enabling efficient circuit simulation and PDK development based on these device technologies.

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Dedication

I dedicate this to my mother Ming Zhou and father Min Feng.

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List of Abbreviations

2DEG 2-Dimensional Electron Gas

BV Breakdown Voltage

DIBL Drain Induced Barrier Lowering

DPT Double Pulse Test

FP Field Plate

GaAs Gallium Arsenide

GaN Gallium Nitride

GFP Gate Field Plate

HEMT High Electron Mobility Transistors

HF High Frequency

HP High Power

HV High Voltage

MVSG MIT Virtual-source GaN HEMT

PDK Process Design Kit

PE Power Electronics

R_{ON} On-state Resistance

RESURF Reduced Surface Field

SBD Schottky Barrier Diode

SiC Silicon Carbide

VS Virtual Source

WAVSiC Waterloo Virtual-source SiC Compact Model

Chapter 1

Introduction

1.1 Power Semiconductor Devices

PE refers to the use of semiconductor devices for controlling and converting electrical power, such as AC-DC, DC-AC, stepping-up/stepping-down voltage/current levels and etc. They are essential in achieving high-efficiency energy conversion, which is beneficial for lowering energy loss, reducing carbon dioxide emission and advancing sustainable technology. This field has been rapidly growing, accelerated by the promising applications of electric vehicles (market size exceeding $2 Billion), smart electric grids, data centers, and renewable energy processing.

Power semiconductor devices are used as solid-state switches in PE systems. They are expected to have low R_{ON}, high BV and low switching losses. Their performance depends both on material properties and device architectures.

Material properties: Since the critical electric field (E_c) approximately scales with the square root of the bandgap, wide bandgap semiconductors such as SiC and GaN, have emerged to complement or even replace traditional silicon-based devices for achieving high BV, high electric field, high-operating temperature, high-switching frequency and low losses [2]. Comparison of the fundamental properties of these materials are shown in Fig. 1.1. SiC and GaN both have a wide energy bandgap, leading to a large breakdown electric field, 10 times larger than that of silicon, which is important for realizing HV operation. In terms of mobility, SiC is in a weaker position compared to silicon, while people can choose devices where transport occurs in the bulk to improve channel mobility [3]. GaN, on the other hand, is at a great advantage in terms of electron mobility due to the high density

of 2DEG at GaN/AlGaN interface. In terms of thermal conductivity and melting point, both GaN and SiC have a clear advantage, with SiC being exceptionally well-positioned, enabling the device to operate at high temperatures.

	Si CMOS	4H SiC CMOS	GaN HEMT
Critical Electric Field [MV/cm]	0.3	3	3.5
Energy Bandgap [eV]	1.12	3.23	3.4
Electron Mobility [$cm^2/(Vs)$]	500	35	1500
Electron Saturation Velocity [$10^7 cm/s$]	1	1.8	3.4
Thermal Conductivity [W/(K cm)]	1.3	3.7	1.5
Melting Point [K]	1412	3103	2500

Figure 1.1: Comparison of fundamental properties of semiconductors used for power electronics, data from [4]

Innovative device architectures: Besides the use of wide band-gap materials to improve power device performance, innovative device architecture such as multidimensional structure has also been proposed to enhance power device performance, with the comparison between one-dimensional and multi-dimensional power devices shown in Fig. 1.2 [5]. Power transistors usually comprise a gated channel for current modulation (R_{ch}) and a long drift region (R_{dr}) to block high voltage. Including a Ohmic contact (R_C), the theoretical relationship between R_{ON} and BV is the following:

$$R_{ON} = R_C + R_{ch} + \frac{4BV^2}{\epsilon \mu E_C^3} \tag{1.1}$$

where ϵ, μ are material permittivity and majority carrier mobility in the drift region respectively. R_{dr} is proportional to BV^{α}, where α is from 2.18 to 2.5 [6] [7]. R_{ch} of vertical GaN and SiC MOSFET is constrained by the low channel mobility, which can be up to 10 times lower than that in Si, attributed to interface states and carrier trapping [8] [9]. At low bias voltage, R_{ON} of 1D WBG devices is dominated by the gated channel R_{ch}. With bias voltage up to at least kilovolt, R_{dr} dominates and device performance is improved taking advantage of wide bandgap material properties. There are two constrains in one-dimensional power devices. (i) $R_{dr} \sim BV$ trade off in the high voltage region. (ii) R_{ch} due to low channel mobility in the low voltage region.

These 1D limit discussed above ($R_{dr} \sim BV$ trade-off and constrained R_{ch}) can be broken by adopting multidimensional device architectures. For example, superjunction incorporates charge balance in the direction perpendicular to the current conduction path. It modifies the electric field in the drift region and achieves breakthrough of R_{dr} and BV

trade-off compared to 1D devices, allowing for linear dependence [10]. Another example is stacking multiple two dimensional electron gas (2DEG) channels perpendicular to the current conduction plane, which effectively reduces R_{ON} through increasing n_{2D}. Last example is to employ FinFET or tri-gate devices. It can (i) achieve better gate control for realizing lower R_{ON} by scaling channel-length, and E-mode operation. (ii) increasing n_{2D} to reduce R_{ch} that dominates R_{ON} for voltage up to kilovolt. Other benefits include reduced current collapse and better thermal management [11].

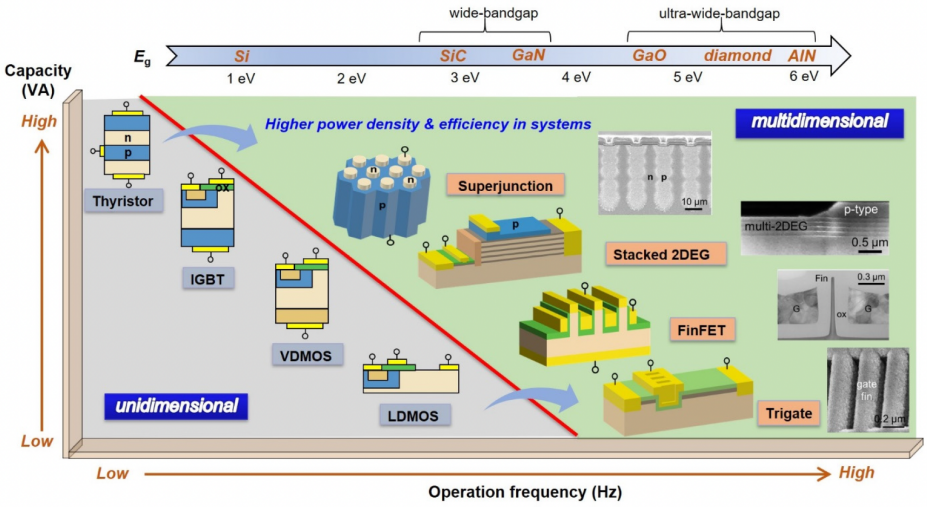


Figure 1.2: Trade-off between power capacity and frequency in one-dimensional and multidimensional power devices, figure from [5]

1.2 Compact Model

After the device being fabricated using SiC/GaN with innovative architecture, it will be characterized with I-V, C-V curves, then compact model could be developed to reflect the current and charge as mathematical functions in terms of device terminal voltages and temperature. It has to be (i) accurate - the simulation result should match the measurement data, (ii) complete - the compact model could capture all the critical physical effects, (iii) computationally efficient and robust - achieve fast circuit simulation without convergence problems, (iv) standardized - compatible with multiple commercial design simulators, such as Spectre®, ADS®, HSPICE®, with consistent results, and (v) scalable

- if some structural/technology parameters change (e.g. channel length under the gate), the model could still predict the correct behaviour without the need to change all of its parameters. Scalability enables the compact model to predict how a device behaves with different structural/technology parameters, which can be used by device/circuit designers for scaling projection and optimization. Overall, the compact model connects the gap between device design/characterization and circuit simulation/fabrication.

Device compact models can be classified into four categories depending on their modeling methods, ranging from the simplest behavioural models to more complex physics-based models. i) Behavioural models: It uses mathematical fitting methods without direct physical meanings. It is simple and easy to fit, but it has low accuracy when the device is operated under different operating conditions such as temperature or biasing. New fitting is required every time device structure or dimension is varied. ii) physics-based models: equations are based on semiconductor physics, with some simplifications. It achieves a good balance between accuracy, flexibility and scalability. Most parameters have clear physical meanings, which is user-friendly and require minimum change under different device variations. iii) numerical models: Numerical simulation tools such as SILVACO, Sentaurus TCAD are available for power devices simulation. The simulation results are accurate, but are computation-demanding and require detailed material properties and device geometry [12]. iv) empirical model using artificial neural networks (ANNs). Parameters do not have inituitive physical meanings. It also requires large training data but yield very good fitiing for non-ideal physical effects such as heating and trapping [13] [14].

1.3 Research Objective

With the active employment of GaN and SiC transistors in PE applications and rapidly evolving device structure, there is a growing demand for compact models, which facilitates integrating GaN, SiC devices into circuit simulations. It needs to meet the requirement of accuracy, completeness, scalability, computational efficiency and robustness. Besides that, it also serves as a tool for device/circuit designers to optimize/innovate on device design. The physical parameters of the model could be changed to preview the device behaviors.

This thesis proposes two comprehensive physics-based compact models for multi-channel GaN/AlGaN Schottky Barrier Diodes (SBD) and SiC MOSFET. Both models achieve good flexibility, scalability and ease of use through (1) mapping the device into a netlist with each component closely connected with a specific device region. (2) using modular approach for transistor-like and diode-like regions, where the core functions are inspired from

MIT virtual-source GaN compact model (MVSG), with proven functionalities and computational robustness.

1.4 Thesis Organization

The thesis is organized as follows. Chapter 2 introduces the industry-standard GaN HEMT model (MVSG model) and the modular approach used for compact modeling. Chapter 3 demonstrates the first application using modular approach, which is a multi-channel AlGaN/GaN SBD. Before introducing the second application, Chapter 4 reviews the current SiC MOSFET model. Afterwards, Chapter 5 shows the second example using modular approach for SiC MOSFET. Finally, in chapter 6, summary and conclusions of the thesis are presented, along with a discussion of future work.

Chapter 2

Modular Formulation Method

2.1 Basic Modules in MVSG model

MIT Virtual-source GaN HEMT (MVSG) Compact Model is an industry-standard compact model since 2018. It has been approved and supported by Compact Model Coaltion (CMC) [15], with proven accuracy, scalability and robustness in modeling RF and power GaN High Electron Mobility Transistors (HEMT). The physical structure of GaN HEMT is quite complex. The cross-section of it with Gate Field Plate (GFP) is shown in Figure 2.1 and Figure 2.2 illustrates its cross-section with p-GaN layer. Its physical structure includes versatile Field Plate (FP), non-linear access region and p-GaN gate to achieve E-mode operation. There are also multiple critical physical effects need to be considered such as gate leakage, self-heating, thermal coupling and charge trapping. Therefore, it is essential to organize and represent the underlying physics concepts clearly by diving the device model into several basic modules, with each module accounting for its corresponding physics.

The 5-pin symbol of MVSG is shown in Fig 2.3. There are four electrical terminals (D, G, S, B), with one optional thermal terminal dt to take into account the external power dissipation due to internal (self) device heating or thermal coupling from adjacent component. The external power dissipation can be applied at dt at the netlist level, with the thermal subcircuit shown in Fig. 2.4. Further additions to the thermal network can be easily done to account for different system-level thermal and cooling capabilities by introducing separate thermal R-C network for different regions of the device.

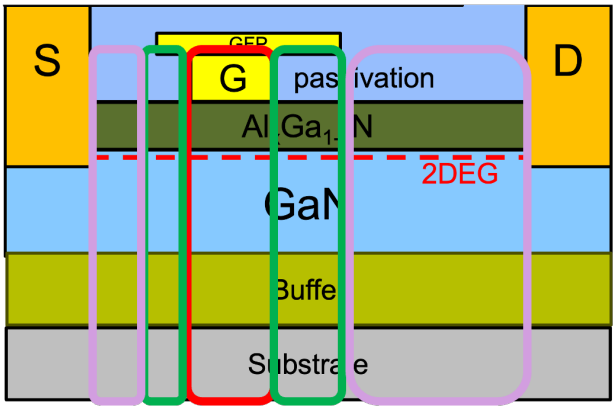


Figure 2.1: Cross-section of GaN HEMT with GFP

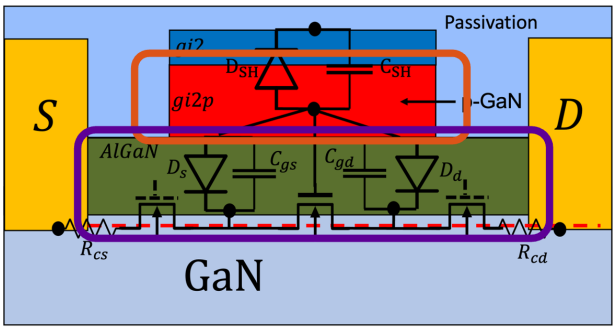


Figure 2.2: Cross-section of GaN HEMT with p-GaN layer

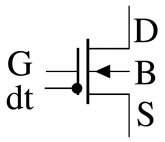


Figure 2.3: 5-pin symbol of MVSG

The equivalent circuit of the MVSG model is shown in Figure 2.5. The model is formulated by mapping the entire structure into several basic components, with each component in the equivalent circuit clearly associated with a specific region of the device, where the shaded color indicates the region in cross-section, shown in Figure 2.1 and Figure 2.2. It includes (i) intrinsic gated region between node *si* and *di* (region under gate electrode), (ii) FP regions at source/drain side (region under GFP). There are four FPs on each side of

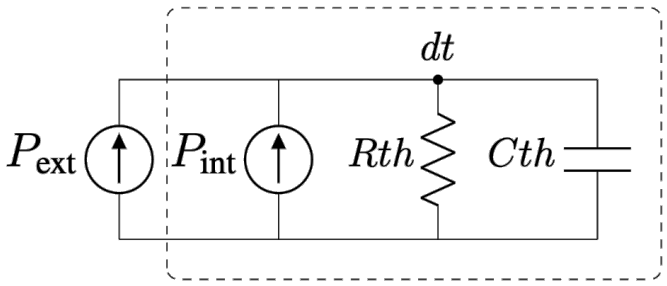


Figure 2.4: Thermal subcircuit in MVSG

the intrinsic gated region, which could be activated/deactivated based on users' needs, also with the flexibility of setting gate potential to either $gi2$ or s. (iii) implicitly-gated access regions (region that do not have an explicit gate), which used to represent the non-linear resistance behavior. All these three regions are represented by transistors, where the key equations used for transistors will be explained in the next subsection.

The Schottky diode D_S, D_D with their corresponding charge components (C_{gs}, C_{gd}) are used to describe gate leakage between p-GaN/AlGaN/UID-GaN [16]. D_{BD} is used to describe the channel breakdown. The Schottky p-GaN module, introduced in [17], is represented by C_{SH}, D_{SH} (depletion-mode), with the option to add R_{SH} accounting for hybrid p-GaN process. It is used to model the E-mode GaN power devices, which shows prominent results in capturing critical effects in power GaN devices. All these diode modules use the same function calls, where the key equations will be explained in the next subsection.

Besides the two basic modules used in MVSG, there are voltage-independent lumped resistors ($R_{g1}, R_{g2}, R_{cs}, R_{cd}$). R_{g1}, R_{g2} are layout-dependent gate resistance and R_{cs}, R_{cd} are contact resistances.

The method to use universal functions for transistor-like (T-Module) and diode-like (D-Module) behaviors models enables the scalability of the compact model. Each component has their own set of parameters and scale with dimensions. It can also adapt to device structure/technology modifications easily. It also allows simplicity and enhances the robustness. Meanwhile, for both T-Module and D-Module, it is able to capture essential physics with a very small number of parameters ($\sim$ 20 parameters per transistor and $\sim$ 13 parameters per diode, most of which have clearly defined physical meanings).

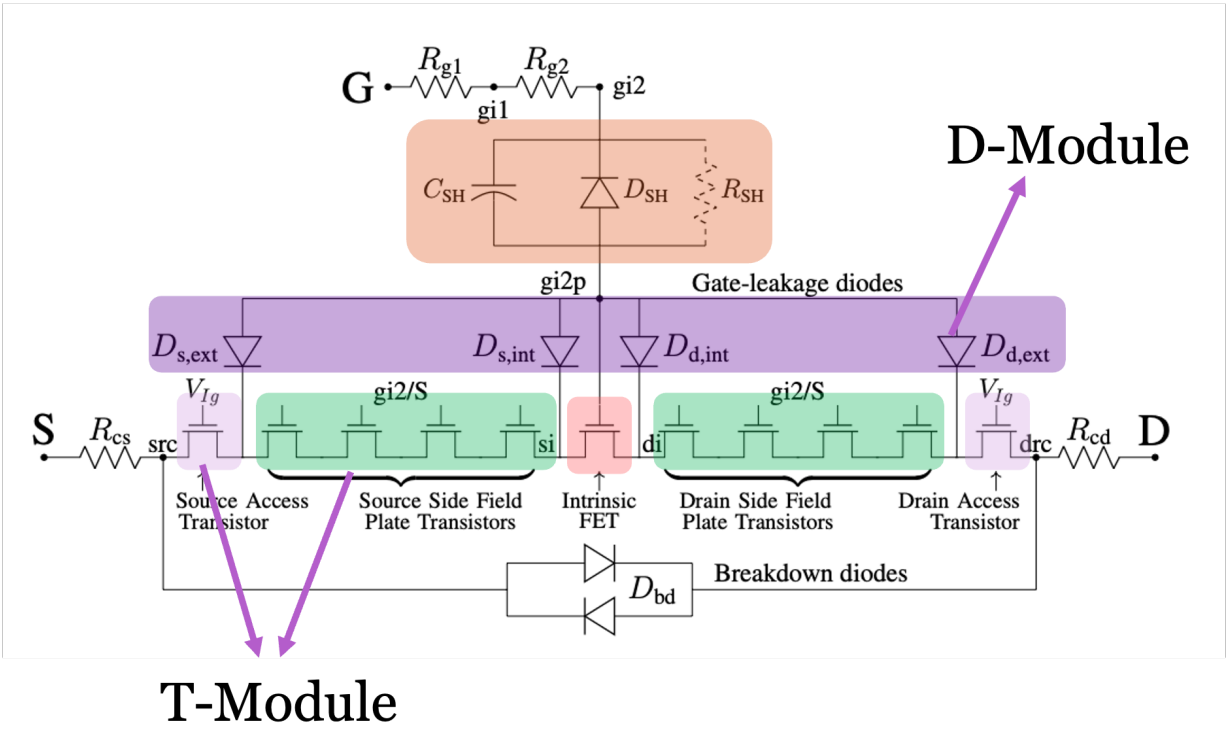


Figure 2.5: MVSG subcircuit with colors indicating that component in cross-section

2.2 Key Equations in T-Module

The Virtual Source (VS) concept was initially proposed at MIT used for highly scaled Si-FETs in a quasi-ballistic mode of transport, which the channel-length is a few mean-free-paths such that scattering is not significant in the channel [18]. The transistor cross-section with its band diagram are shown in Figure 2.6 and Figure 2.7. The virtual source point ($x = x_o$) is where the barrier peaks. The current normalized to width will be the product of local-area charge-density and local carrier velocity. The charge at the virtual source point is easy to model using gradual-channel approximation (GCA). The velocity at VS point is empirically found and is bias independent at saturation region (v_{xo}) or have V_{DS} dependence in non-saturation regime using $v_{xo} \cdot F_{sat}$, where F_{sat} is an empirical saturation function.

It was later extended to account for drift-diffusive transport in GaN HEMTS [19] [20][21]. The current is still the product of charge (Q_{is}, Q_{id}) and velocity (vel) in Eqn. 2.1,

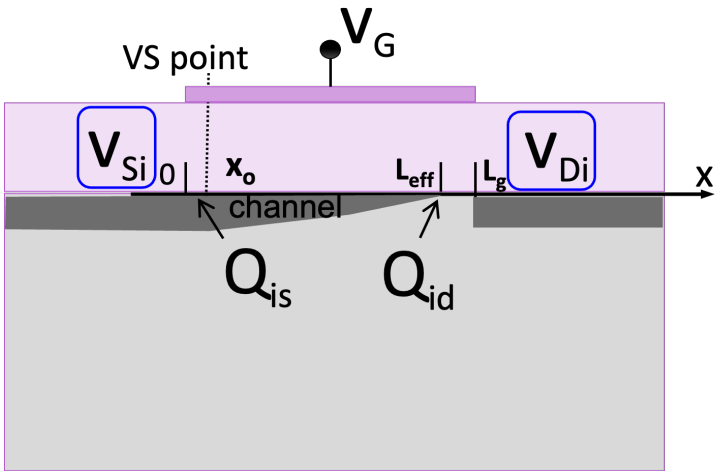


Figure 2.6: Cross section of transistor with Virtual Source (VS) point labelled

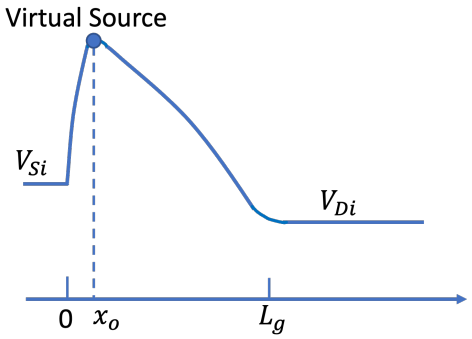


Figure 2.7: Band diagram under the gate with VS Point labelled

where $W \cdot ngf$ is total device width. However, the velocity is no longer bias-independent in the saturation-regime and depend on the local lateral field due to small electron mean-free-path.

$$I_{DS} = Wngf\frac{Q_{is} + Q_{id}}{2}vel \tag{2.1}$$

Q_{is}, Q_{id} are source-end and drain-end charges, which allow smooth transition from sub-threshold to above-threshold regions by using the $ln(1 + exp(x))$ formulations. Equations are given in Equation 2.2, 2.3, where C_{inv} is unit-area gate capacitance representing the

strength of electrostatic coupling from the gate, and n is relevant to sub-threshold slope (SS) by $SS = n\phi_t ln10$.

$$Q_{is} = C_{inv} 2n\phi_t ln(1 + exp(\frac{V_{GD} - V_{SX} - V_T}{2n\phi_t})) \tag{2.2}$$

$$Q_{id} = C_{inv} 2n\phi_t ln(1 + exp(\frac{V_{GS} - V_{DX} - V_T}{2n\phi_t})) \tag{2.3}$$

V_{SX}, V_{DX} (Equation 2.4, 2.5) ensure that the drain/source terminal charges will saturate under velocity-saturation and then remain independent of the applied V_{DS} to the first order through the use of $\frac{x}{(1+x^\beta)^{1/\beta}}$. The max function is to make sure thet the model passes Gummel Symmetry test since the model can automatically assign the lowest potential to be its source terminal.

$$V_{SX} = \frac{-V_{DS}}{(1 + (max(0, \frac{-V_{DS}}{VDSAT})^\beta))^{1/\beta}} \tag{2.4}$$

$$V_{DX} = \frac{V_{DS}}{(1 + (max(0, \frac{-V_{DS}}{VDSAT})^\beta))^{1/\beta}} \tag{2.5}$$

Velocity (vel) equation is given by

$$vel = [2ff\phi_t \frac{\mu}{L} + (1 - ff)v_x]F_{vsat} \tag{2.6}$$

where ff smooths between strong and weak inversion, v_x is the saturation velocity, μ is low-field mobility. F_{vsat} is given in Equation 2.7, F_{vsat} controls carrier transport transitioning from non-velocity-saturation to velocity-saturation regime, and is important to enable the model to scale correctly with channel length L. For small channel-length device, $F_{vsat} = 1$, the current will have velocity-dependent saturation, which is similar to the VS model for Si-FETs. For long channel-length device, current will have mobility dependent saturation. V_{DSAT} is the saturation voltage given by $V_{DSAT} = V_{DSATS}(1-ff)+\phi_t ff$ and $V_{DSATS} = \frac{v_x L}{\mu}$.

$$F_{vsat} = \frac{\frac{Q_{is}-Q_{id}}{C_i nv V_{DSAT}}}{(1 + (\frac{Q_{is}-Q_{id}}{C_{inv} V_{DSAT}})^\beta)^{1/\beta}} \tag{2.7}$$

Terminal charges Q_G, which is divided into Q_s, Q_d, are all calculated using Q_{is}, Q_{id} through linear Ward Dutton partitioning [22], shown in Equation 2.8 2.9 2.10. This guarantees self-consistency between channel current and charges. The terminal capacitance are derived from these channel charges, shown in Equation 2.11, 2.12, 2.13

$$Q_S = \frac{2WL}{(Q_{is}^2 - Q_{id}^2)^2}[-Q_{id}^2\frac{Q_{is}^3 - Q_{id}^3}{3} + \frac{Q_{is}^5 - Q_{id}^5}{5}] \tag{2.8}$$

$$Q_D = \frac{2WL}{(Q_{is}^2 - Q_{id}^2)^2}[-Q_{is}^2\frac{Q_{is}^3 - Q_{id}^3}{3} + \frac{Q_{is}^5 - Q_{id}^5}{5}] \tag{2.9}$$

$$Q_G = \frac{2WL}{(Q_{is}^2 - Q_{id}^2)^2}[\frac{Q_{is}^3 - Q_{id}^3}{3}] \tag{2.10}$$

$$C_{gs} = -\frac{\delta Q_S}{\delta V_G} \tag{2.11}$$

$$C_{gd} = -\frac{\delta Q_D}{\delta V_G} \tag{2.12}$$

$$C_{gg} = C_{gs} + C_{gd} \tag{2.13}$$

2.3 Key Equations in D-Module

Diode current contains three parts (each can be activated/deactivated independently) - forward with high-injection included (I_F), reverse-recombination (I_R) and breakdown (I_{BD}). The I-V curve in all three regions is shown in Figure 2.8.

A diode symbol shown in Fig. 2.9 to explain its equations, with the overall diode current consisting three components following equation 2.14. I_F (Equation 2.15) is computed with the unit-width reverse saturation current i_j, bandgap dependence (V_{jg}), temperature coefficient ($p_{g,param}$), and inverse ideality factor (p_g) to the first order. High-injection effect is also included following [16].

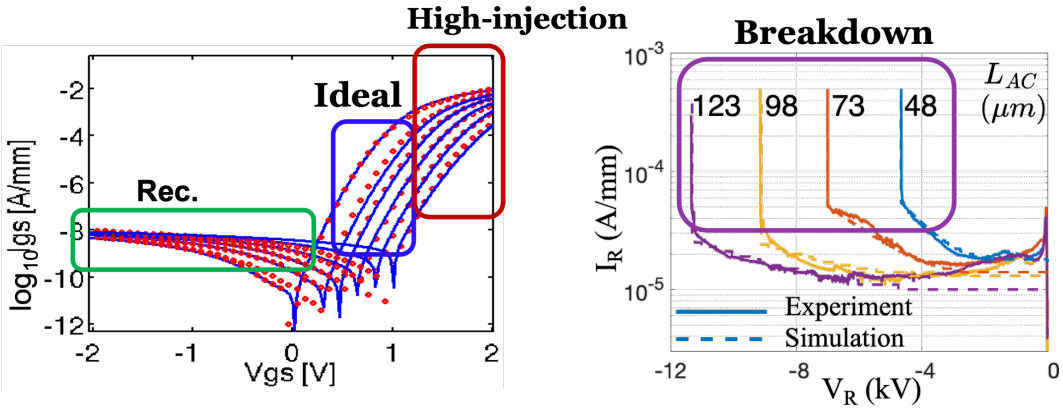


Figure 2.8: Diode I-V curve in forward (with high-injection), reverse and breakdown regions [20] [1]

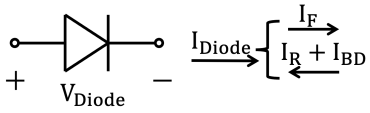


Figure 2.9: Diode symbol to explin current equations

$$I_{Diode} = I_F - I_R - I_{BD} \tag{2.14}$$

$$I_F = Wi_j exp(-\frac{p_{g,param}}{V_{jg}})(exp(\frac{p_g}{V_{Diode}}) - 1) \tag{2.15}$$

The reverse recombination current (Equation 2.16) is calculated using the unit-width reverse leakage current (i_{rec}), inverse recombination ideality factor ($p_{g,rec}$) and saturation effect (through F_{rec}, given in Equation 2.17).

$$I_R = Wi_{rec} exp(\frac{p_{g,rec}F_{rec}}{\phi_t} - 1) \tag{2.16}$$

$$F_{rec} = \frac{-V_{Diode}}{(1 + |\frac{V_{Diode}}{V_{SAT}}|^{\beta})^{1/\beta}} \tag{2.17}$$

The breakdown current (Equation 2.18) is calculated with unit-width reverse saturation current i_{jbd}, inverse ideality factor p_{bd} and breakdown on-set voltage V_{BD}.

$$I_{BD} = Wi_{jbd} exp(-p_{bd} V_{BD} - \frac{p_{g,param} V_{jg}}{\phi_t})(exp(-p_{bd} V_{Diode}) - 1) \tag{2.18}$$

2.4 Summary on Modular Formulation Approach

The key equations in T-Module and D-Module are discussed in this chapter, with proven accuracy, scalability and robustness through device-circuit validation in both RF and HV applications [21].These modules can be extended in other technology or device design to capture transistor-like and diode-like device behaviors, which will greatly facilitate the user-friendly and straightforward development of compact models.

Such modular model formation approach where most of these basic modules have been proven efficient, scalable and computationally robust in the family of MVSG compact models developed for GaN devices (including GaN HEMTs for both radio-frequency and PE applications [21], kilo-volt multi-channel GaN diodes [1] (Chapter 3) and GaN-based transmission-line non-linear resistors [23]).

Two applications using the modular approach will be discussed in detail, which is a multi-channel SBD and SiC MOSFET in Chapter 3 and Chapter 5 respectively.

Chapter 3

Multi-channel AlGaN/GaN SBD Compact Model

This chapter showcases the first application using the modular formulation approach, which is a simple yet comprehensive compact model for multichannel AlGaN/GaN SBD with a p-GaN Reduced Surface Field (RESURF) layer. Model formulation, including equivalent circuit, key equations, and parameter assignment, are explained in details, together with parameter extraction flow.

In terms of model formulation, it makes use of the modular formulation described above (T-Module, D-Module). The model correctly reflects the device physics in forward-bias, reverse-bias and breakdown conditions, capturing critical behaviors associated with multi-channel turn-on and RESURF effects from the p-GaN layer. Good accuracy, scalability, and computation robustness are validated via: IV, CV, breakdown simulations. The physics-based model can also be used as a tool for technology optimization and scaling projections. This is illustrated via simulations on (1) the impact of barrier/channel thickness on device capacitance and (2) the effect of RESURF-length (L_{RESURF}) on the Baliga Figure-of-Merit (FoM) and area-scaling FoM. With minimum adjustment, the proposed model also serves as a first step towards compact modeling of multi-channel AlGaN/GaN transistor.

3.1 Motivation

As a recent development in the rapidly growing GaN-based device family, AlGaN/GaN multi-channel SBD has become a promising candidate for medium-/high- voltage power

electronics, with low R_{ON} from multi-channels and high BV from recent device structure innovations (e.g. p-GaN RESURF) [5] [24]. The structure has been further integrated to achieve multi-kilovolt GaN multi-channel transistors [25]. To facilitate circuit design and simulations using multi-channel AlGaN/GaN devices, there is a growing demand for compact models that are accurate, scalable, flexible, standardized, computationally efficient and with simple parameter extraction method.

3.2 Model Formulation

Figure 3.1 illustrates the 3-D schematic and cross-section of a five-channel AlGaN/GaN SBD, with device fabrication details reported in Xiao *et al.* [24]. From top to bottom of its cross-section, it contains 20nm p^+-GaN, 350nm p-GaN, five AlGaN/GaN heterostructure channels and a buffer layer. The anode metal makes Schottky contact with all two dimensional electron gas (2DEG) channels, and it extends on top of p-GaN with length L_A. The RESURF area (with length L_{RESURF}) prevents electric field crowding, and is critical to achieve a high BV. The thickness of the RESURF layer is carefully optimized to balance net charges from multiple channels. A portion of p-GaN of length L_{PC} is fully etched to prevent potential p-GaN punch-through. Cathode is formed from a self-aligned Ohmic contact process.

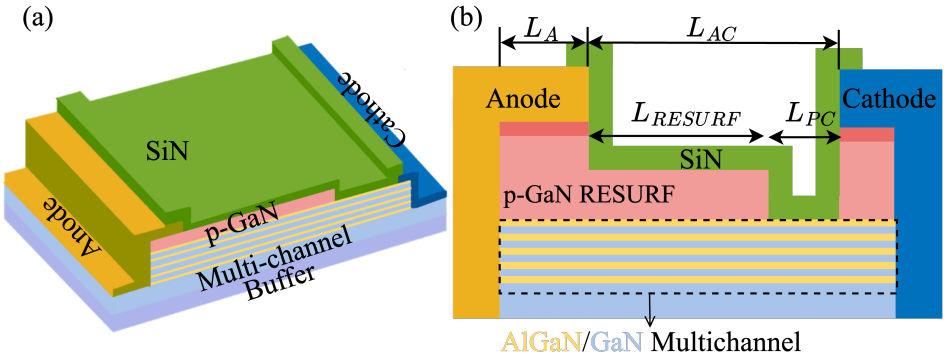


Figure 3.1: **(a)** 3-D schematic of multichannel SBD, with cross-section shown in **(b)**.

While the multi-channel SBD device structure is rather complex, the model introduced in this work achieves good flexibility, scalability and ease of use through (1) mapping the device into a netlist with each component closely connected with a specific device region, (2) all diodes and all transistors are described using single and common function calls with different input parameters. All the transistors use equations in T-Module and all the

diodes use equations in D-Module. Such approach allows simplicity (via simple function calls) and enhances convergence robustness of the compact model. The model is also able to smoothly transition between forward, reverse and breakdown regions, taking advantage of the MVSG model.

Model netlist Figure 3.2 shows equivalent circuit model of this device with multiple channels (CH1-CH5 in this example) connected in parallel along with a breakdown diode (D_{BD}). Each component in the equivalent circuit is clearly associated with a specific region of the device, with the mapping shown in Figure 3.3; hence, the proposed physics-based model is well scalable and can easily adapt to device structure modifications.

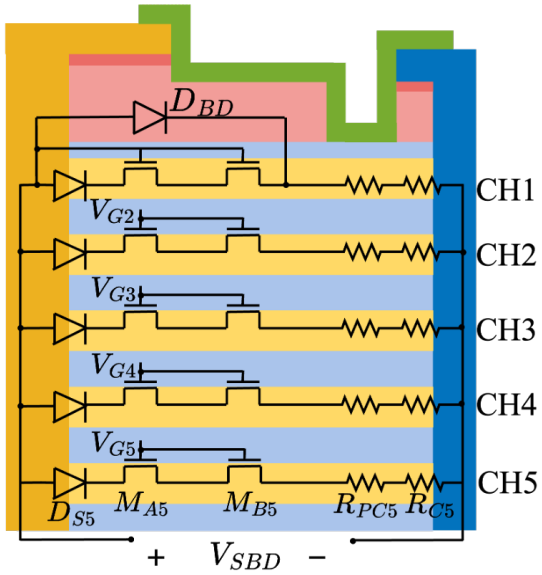


Figure 3.2: Equivalent circuit of multichannel SBD.

Each channel can be modeled as a serial connection of components that include (i) a sidewall diode (D_S) representing the anode-to-channel Schottky contact, (ii) a first transistor (M_A) represents the gated area under the extended anode with length L_A, (iii) a second transistor (M_B), represents the channel under RESURF area with length L_{RESURF}, (iv) a series resistor (R_{PC}) with the length L_{PC} and (v) a contact resistor (R_C) represents the Ohmic contact at the cathode. We use subscription i to refer to the circuit-branch representing the i^{th} channel from the top. A breakdown diode (D_{BD}), which is directly connected to the p-GaN terminal without being de-biased through D_S, is added to describe the leakage and breakdown between channel and p-GaN layer. It is expected that negative V_{SBD} fully depletes all the channels before the complete depletion of p-GaN RESURF. The

p-GaN layer is partially depleted under large negative V_{SBD}, which is reflected in an increased gate resistance of M_{B5} (not shown) as well as a decreased gate capacitance lumped into the gate capacitance of M_{A5} and M_{B5}.

Common function calls All the transistors (M_A, M_B) use T-Module equations, while all the diodes (D_S, D_{BS}) use D-Module equations. It not only ensures the accuracy, scalability, robustness of the compact model through reusing equations from MVSG, it also achieves model simplicity and easy development of PDK. It can easily expand to model non-transistor devices such as transistors, diodes, and non-linear resistors.

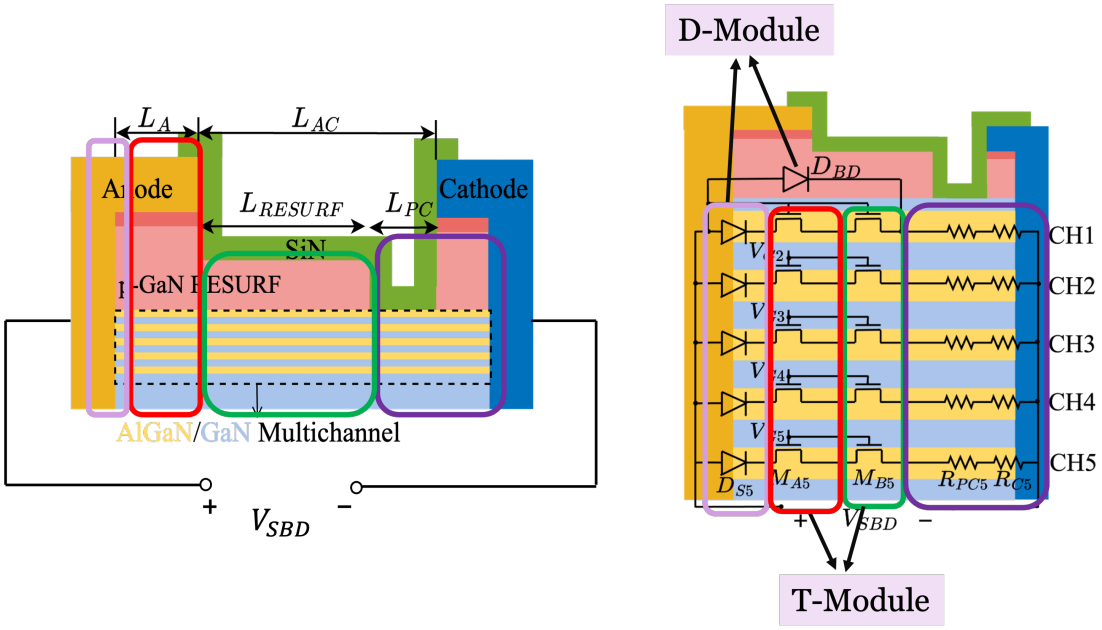


Figure 3.3: Component mapping between SBD cross-section and its equivalent circuit

3.3 Mode of Operation

Unique physical effects in multi-channel SBD, such as individual channel turn-on, and lower channel screening, are reflected through proper assignment of threshold voltage (V_{Th}) and gate voltage (V_G) to each transistor. p-GaN RESURF depletion is lumped into the gate capacitance of the lowest channel (CH5). Without loss of generality, we use the CH5 branch, shown in Figure 3.4, to explain the details of key parameter assignment (e.g. V_{Th} and V_G) to M_A, M_B.

Transistor threshold voltage V_{Th}: V_{Th} naturally corresponds to the voltage when the 2DEG starts to form in each channel. The lower channel has a more negative V_{Th}, due to the increased separation from top-side p-GaN and screening from upper channel(s). In a well-tempered device, p-GaN RESURF depletion is minimum for upper channels, hence is only considered in the lowest channel through a lumped gate capacitance. In this work, M_A and M_B in the same channel are assigned the same V_{Th}, as p-GaN RESURF are still not fully depleted when the 5^{th} channel is turned off. However, the model is formulated so that M_B may be assigned a different V_{Th} than M_A, to reflect cases where pGAN is fully depleted before the channel is turned off.

Transistor gate voltage V_G: V_G will be the effective gate voltage for each transistor. Due to screening effect from the upper channels, the effective gate voltage of the transistors in the lower channels is affected, hence the maximum gate voltage of the transistors in a lower channel is capped at the threshold voltage of the transistor right above it.

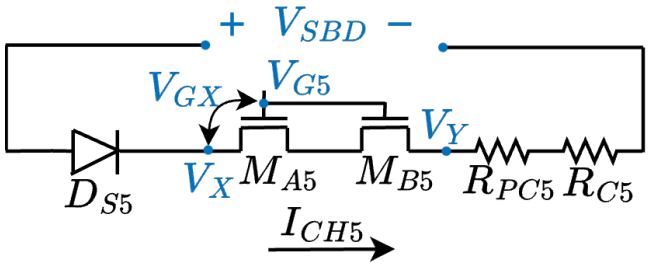


Figure 3.4: Circuit branch corresponding to CH5.

Device operation in forward bias When V_{SBD} is above the turn-on voltage (V_{ON}) of Schottky junction, D_S is in forward bias, and $M_A + M_B$ forms a diode-connected transistor. The two transistors parameters such as mobility and saturation velocity, together with resistivity of R_{PC}, R_C determines the slope in I-V curve (R_{ON}). With increasing L_{RESURF}, both BV and R_{ON} increase.

Device operation in reverse bias When $V_{SBD} < 0$, depletion-mode channels are turned on one-by-one based on the V_{Th} of transistors. Refer to Figure 3.4 for voltage definitions (V_{GX}, V_{G5X}, V_X), and note that V_X becomes source terminal for M_{A5} when $V_{SBD} < 0$ since $V_X < V_Y$. In Figure 3.5 with V_{SBD} from -100V to -20V, $V_{Th3}(= -20V), V_{Th4}(= -44V), V_{Th5}(= -76V)$ separate device operation into three regions.

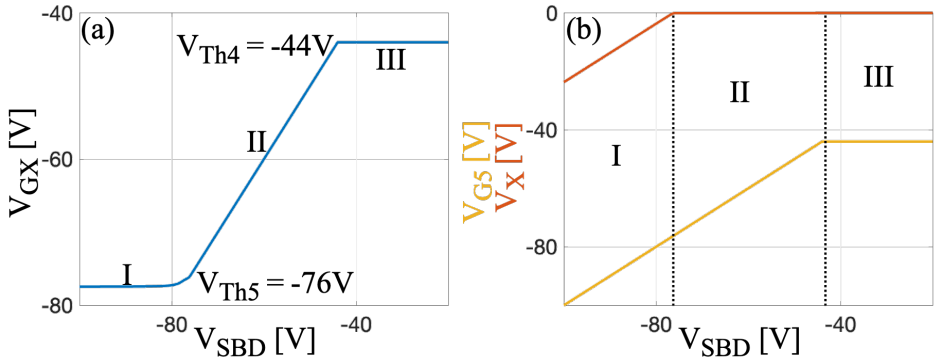


Figure 3.5: Key voltage for CH5 operation when V_{SBD} increases from -100V to -20V

Region I: (Figure 3.6) $(V_{SBD} < V_{Th5})$ with no channel turned on, all mobile charges are depleted, potential in CH5 is modulated by p-GaN, hence V_{G5} is set by p-GaN/anode voltage. M_{A5} is off with V_{GX} pinned at V_{Th5}.

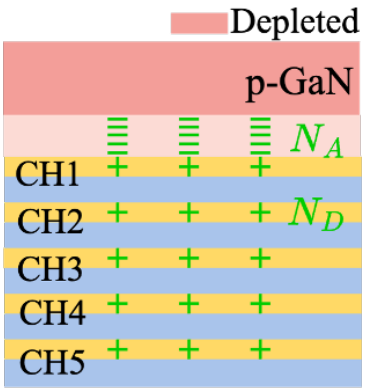


Figure 3.6: Dopants and mobile charges in Region I

Region II: (Figure 3.7) $(V_{Th5} < V_{SBD} < V_{Th4})$ with only CH5 is fully on. 2DEG forms along CH5, with V_{G5} still tied to p-GaN voltage, but V_{GX} also starts to increase with V_{SBD} at the same time.

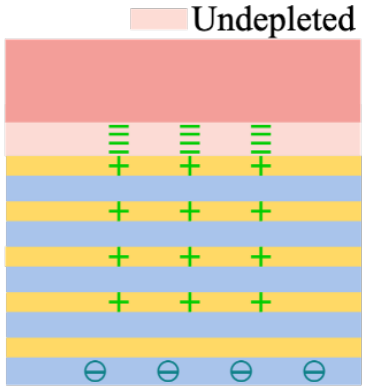


Figure 3.7: Dopants and mobile charges in Region II

In Region III: (Figure 3.8) ($V_{Th4} < V_{SBD} < V_{Th3}$) with both CH5 and CH4 turned on. Carriers start to populate CH4, screening CH5 from electrically coupled to the p-GaN layer. From Region III, V_{G5} is capped at V_{Th4} and no longer increase with V_{SBD}. For a well-tempered device, p-GaN depletion is not significant once CH4 turns on.

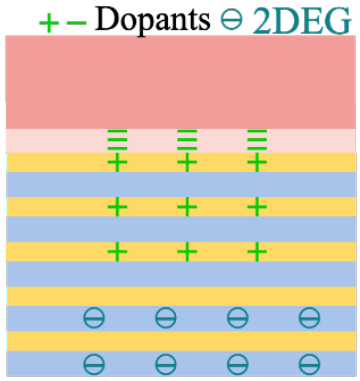


Figure 3.8: Dopants and mobile charges in Region III

The key voltage and channel charges for the three regions when V_{SBD} sweeping from -100V to -20V is also summarized into Figure 3.9.

	Region I	Region II	Region III
V_{SBD}	(-100, -76)	(-76,-44)	(-44, -20)
Channel charges	No channel	CH5 on	CH5, CH4 on
Key voltage	V_{GX5} pinned at V_{Th5}	V_{GX5} increases with V_{SBD}	VG5 capped at V_{Th4}

Figure 3.9: Key voltages and channel charges when sweeping V_{SBD} from -100V to -20V, separated into three regions

3.4 Parameter Extraction Flow

The parameter extraction flow to get calibrated physical compact model against measurement is shown in Figure 3.10, with three steps. Model parameter values can be easily extracted from I-V and C-V data. Afterwards, circuit designers could use it for circuit simulation and fabrication.

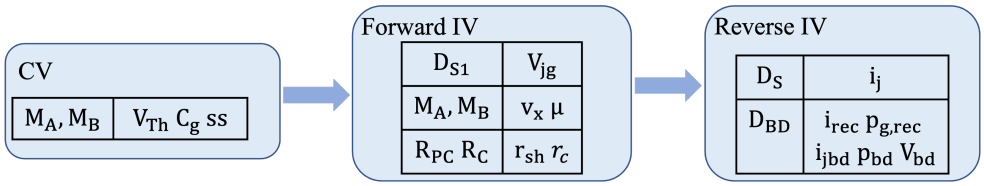


Figure 3.10: Parameter extraction flow for multi-channel AlGaN/GaN SBD.

Step I: C-V: (Figure 3.11) From the CV plot, V_{Th} of transistors in five channels are found at the five transition point (e.g V_{Th1}, V_{Th2}). C_g of transistors are calculated from the change of capacitance at each V_{Th}. SS controls the slope of the C-V curve near each V_{Th} transitioning from OFF to ON.

Step II: (Figure 3.12) From the forward IV plot, V_{jg} of D_{S1} is determined from the turn-on voltage and the I-V slope is determined by v_x, μ from the two transistors M_A, M_B and r_c, r_{sh} from two series resistors R_C, R_{PC}.

Step III (Figure 3.13) From the reverse IV plot, parameters related to D_{BD}, D_S are determined. Current partition at negative V_{SBD} is also shown in Figure 3.13 (b). I_{SBD} is dictated by the reverse saturation current from D_S at small negative V_{SBD}, and by the leakage and breakdown current from D_{BD} at large negative V_{SBD}.

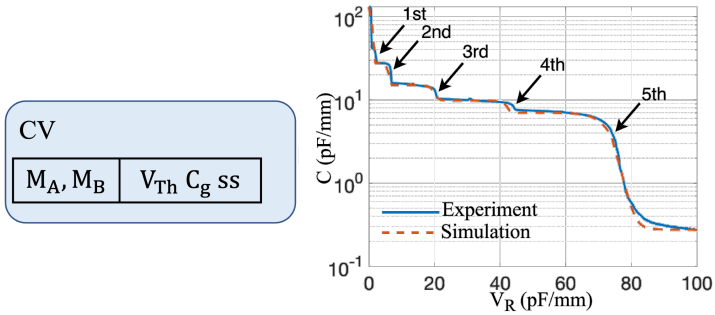


Figure 3.11: Step I in SBD parameter extraction flow

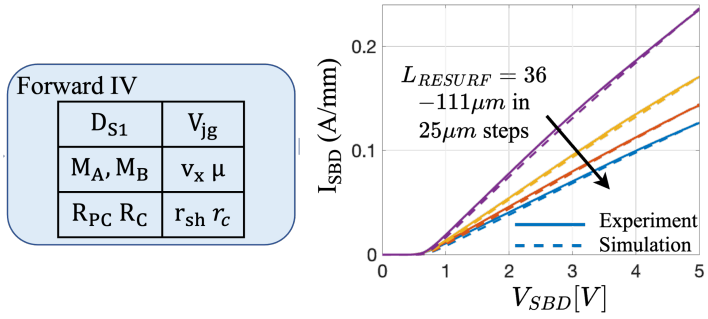


Figure 3.12: Step II in SBD parameter extraction flow

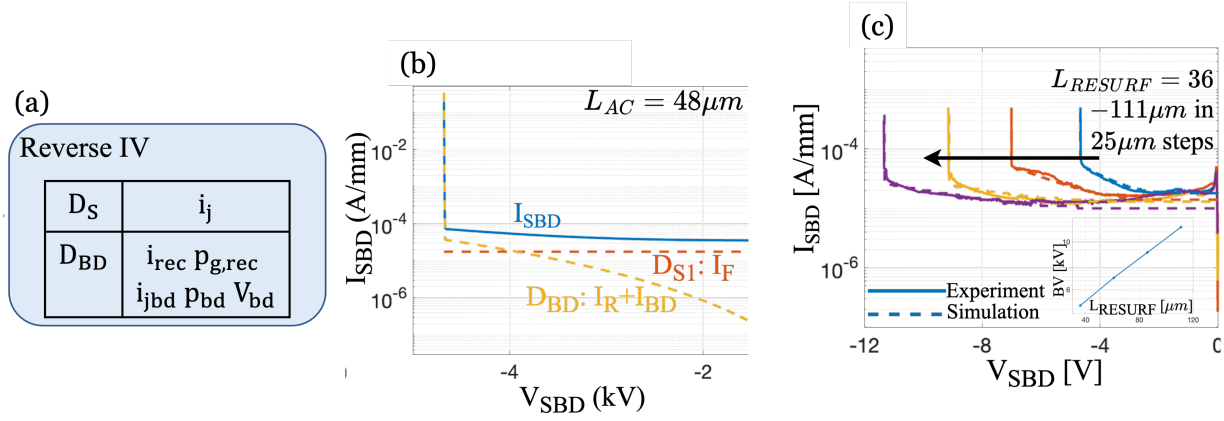


Figure 3.13: Step III in SBD parameter extraction flow

3.5 Results and Significance

Following the extraction flow discussed in the last subsection, Figure 3.14a-c illustrates model benchmarking against experiments, proving the model's accuracy in all three (forward, reverse and breakdown) operational modes, as well as good scalability with L_{RESURF}. Solid lines correspond to experimental data reported in Xiao *et al.* [24], and dashed lines are used to represent model simulation results. Figure 3.15 shows key parameter values used for Figures 3.14.

In Figure 3.14a, the turn-on voltage V_{ON} of 0.7V is from the Schottky-contact (D_S). After $V_{SBD} > V_{ON}$, $M_A + M_B$ behave like diode-connected transistors, and the overall current is modulated by L_{RESURF}. In Figure 3.14b, depletion voltage of each 2DEG channel is marked, matching the value assigned to V_{Th} of each channel. In Figure 3.14c, reverse I-V characteristics showing device breakdown voltage scaling with different L_{RESURF}.

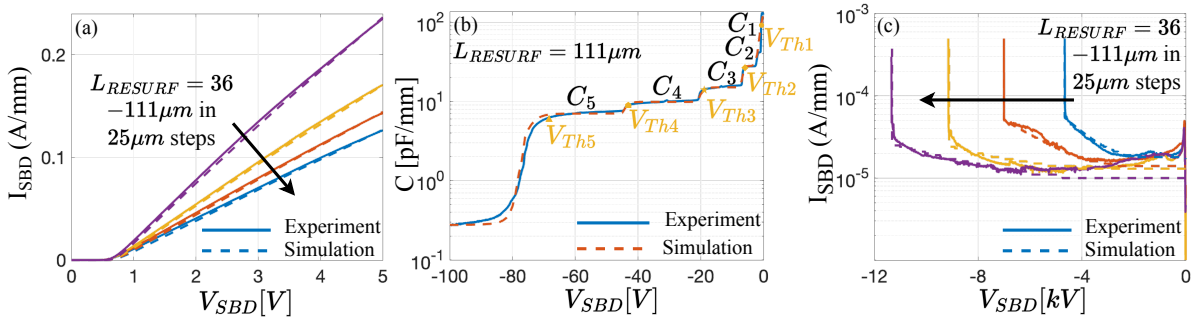


Figure 3.14: **(a)** Forward I-V characteristics with different L_{RESURF}. **(b)** C-V characteristics of the SBD with $L_{RESURF} = 111\mu m$ **(c)** Reverse I-V characteristics showing device breakdown voltage scaling with different L_{RESURF}.

A major advantage of introducing p-GaN RESURF layer is to increase BV, which shows a linear increase with L_{RESURF} (Figure 3.16). As lateral electric field is significantly larger than that in the vertical direction, increasing L_{RESURF} effectively improves BV in a linear fashion [26].

(a)	D_S	D_{BD}
V_{jg} [V]	0.7	0.7
$p_{g,param}$ [1/V]	0.82	0.82
i_j [A/m]	0.01	0
p_g [1/V]	1	0
i_{rec} [A/m]	4e-17	4e-20
$p_{g,rec}$ [1/V]	2.05	1.94
V_{BD} [V]	0	-10k ~ -4.6k
i_{jbd} [A/m]	0	1e-10
p_{bd} [1/V]	0	2.0

(b)	M_A M_B
L_A L_B [μm]	2, 36 ~ 111
V_{Th} [V]	-76 ~ -0.5
C_g [F/m^2]	6e-5 ~ 1.5e-3
SS [V/dec]	0.1
v_x [m/s]	≈ 7.1e4
μ [m^2/(Vs)]	≈ 2.0

(c)	R_{PC}	R_C
L_{PC} [μm]	12	-
r_{sh} [Ω/Sq]	225	-
r_c [Ωm]	-	5e-4

Figure 3.15: Key parameters used to generate Figures 3.14.

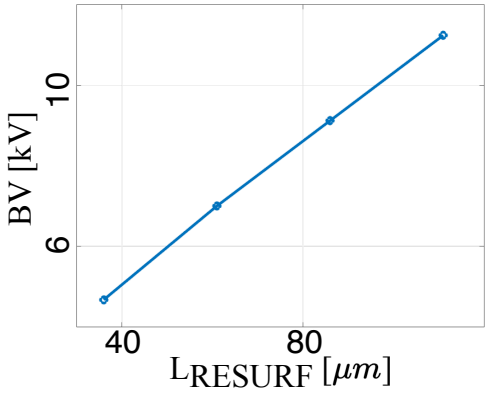


Figure 3.16: Reverse I-V characteristics showing device breakdown voltage scaling with different L_{RESURF}.

Figure 3.17 (solid line) shows TCAD results, demonstrating the effect of varying GaN or AlGaN layer thickness on depletion rate [26]. Solid line is TCAD results and dashed line is model simulation results. The proposed model is able to match well with it using the parameter extraction flow described in Figure 3.10. It further demonstrates the scalability of the proposed SBD model.

Proposed model's scalability with device geometry makes it a convenient tool for device FoM projection (Figure 3.18). $FoM_1 = \frac{BV^2}{R_{on}Q_G}$, showing a longer L_{RESURF} is preferred from

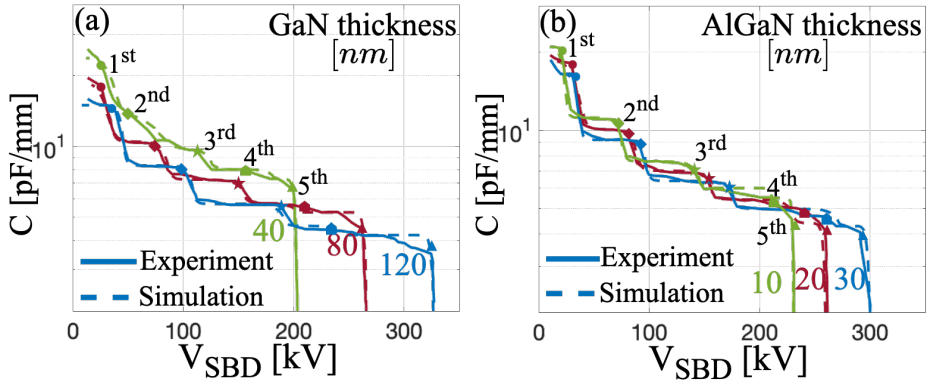


Figure 3.17: C-V plots for devices with different GaN thickness and AlGaN thickness.

device performance perspective. $FoM_2 = \frac{BV^2}{R_{on}Q_G L_{SBD}}$ combining device performance and footprint, showing lower L_{RESURF} is preferred if footprint is taken into consideration.

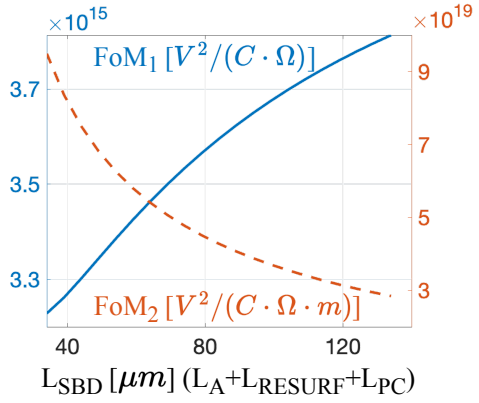


Figure 3.18: FoM projection using the calibrated SBD compact model

The proposed model is also capable to model multi-channel transistor with minimum changes to accommodate the different device structure (e.g. separate source and gate terminals, and ohmic contacts on both source/drain ends). Cross-section of a depletion-model multi-channel AlGaN/GaN transistor with ohmic contacts at both source and drain, with its equivalent circuit model is shown in Figure 3.19 (a). Simulated I_{DS} vs V_{DS} is shown in Figure 3.19 (b). The principle of model formulation and equations remain unchanged. This showcases the potential of adopting the proposed modeling approach for future development of multi-channel AlGaN/GaN transistor compact models.

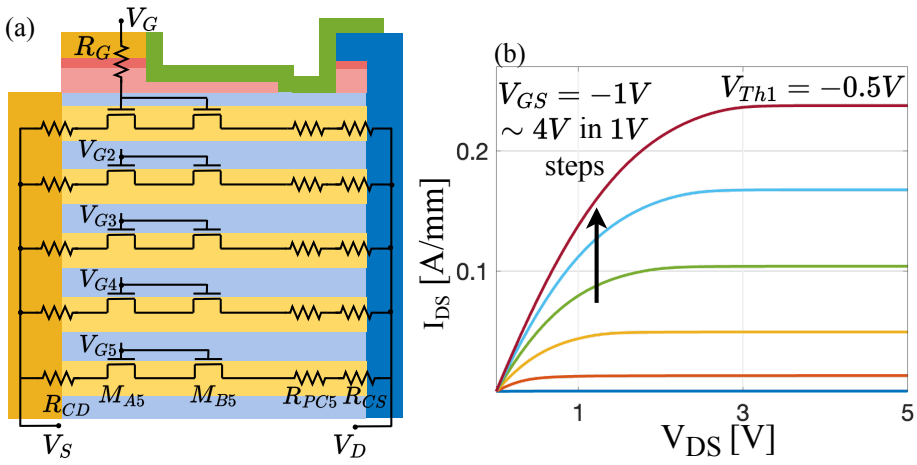


Figure 3.19: **(a)** Cross-section of a depletion-model multi-channel AlGaN/GaN transistor with ohmic contacts at both source and drain **(b)** Simulated I_{DS} vs V_{DS} of a multi-channel depletion mode transistor.

3.6 Summary on Multi-channel SBD Compact Model

In summary, a compact model is proposed for multi-channel AlGaN/GaN SBDs with the flexibility to account for p-GaN RESURF, which is able to accurately captures the device behaviors in forward, reverse and breakdown regions, with benchmarking to measurements. The model is (i) simple - applying modular formulation approach, (ii) scalable - with respect to L_{RESURF} and (iii) flexible - accounting for different GaN and AlGaN thickness. This model also provides insights on technology optimization and scaling projections for designers. It also works to model multichannel AlGaN/GaN transistor with minimum adjustment.

Chapter 4

Literature Review on SiC MOSFET Model

Various compact models for SiC MOSFET have been reported and has been surveyed in [12] [27] [28]. It can be categorized into behavioral/empirical model and physics-based models.

4.1 Behavioural/Empirical Model

Angelov model is a widely used empirical non-linear IV equivalent circuit model that is well-suited for Gallium Arsenide (GaAs), GaN, SiC, and even CMOS technologies [29] [30] [31]. The core in this model is to capture the 'bell-shaped' transconductance (g_m) observed in GaN, GaAs and other material technologies, illustrated in Figure 4.1. The current equation is shown in Equation 4.1.

$$I_{DS} = \beta \cdot (1 + tanh(\varphi))(1 + \lambda V_{DS})tanh(\alpha V_{DS}) \tag{4.1}$$

The use of the $tanh()$ formulation ensures that the current expressions possess infinite derivatives, making the model particularly well-suited for harmonic-balance simulations. I_{pk} is the drain current at maximum transconductance. λ is the channel length modulation parameter and α is the saturation voltage parameter. φ is a power series, centered at V_{pk}, to take account the V_{gs} dependence, shown in Equation 4.2

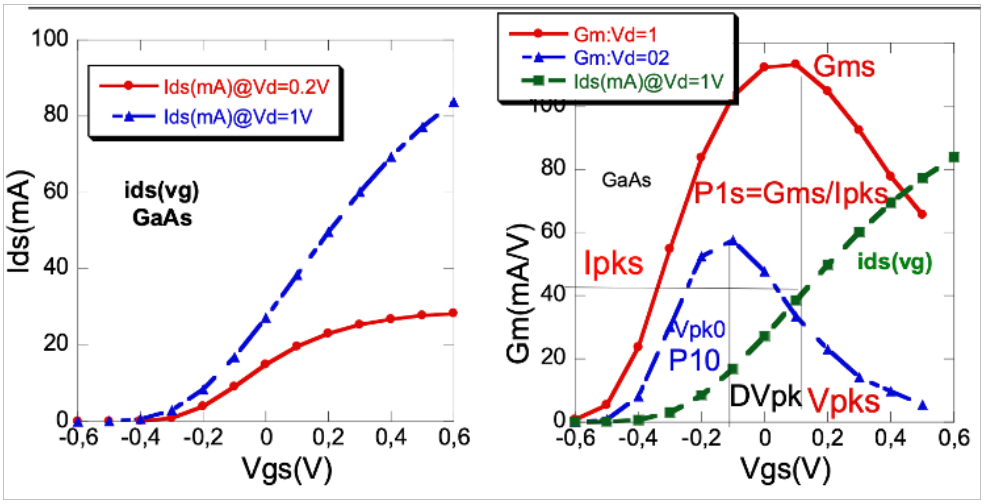


Figure 4.1: I-V and the 'bell-shaped' transconductance g_m characteristics used in Angelov model [32]

$$\varphi = P_1(V_{GS} - V_{pk}) + P_2(V_{GS} - V_{pk})^2 + P_3(V_{GS} - V_{pk})^3 \tag{4.2}$$

P_1, P_2, P_3 are empirical fitting parameters for current V_{GS} dependence. It is clear that the model is empirical in nature and parameters do not have physical meanings. There are around 90 parameters in this model [29], which can accurately capture the non-linear behavior and harmonics in power circuits. However, the model has to be re-fitted with any change to device dimension or process technology since the model is not scalable with respect to geometry, which will take large time and effort. Another drawback is not the model could not provide any physical insights to device engineers or circuit designers due to the lack of scalability.

In terms of compact model developed specifically for SiC MOSFET, some researches model the intrinsic region with inverted channel using the Angelov model and then add more modules to take into account other unique physical effect in SiC MOSFET such as voltage-dependent C_{GD}, body diode current to capture 3^{rd} quadrant IV behaviour and non-linear drift region resistance.

Hsu *et al.* proposed a behavioral SPICE model for SiC MOSFET [33][34]. with the equivalent circuit shown in Fig. 4.2. The intrinsic region uses the Angelov model, which can accurately capture the 1^{st} quadrant IV behaviour.

In order to model the 3^{rd} quadrant I-V curve, a PN-diode and an N-type JFET model

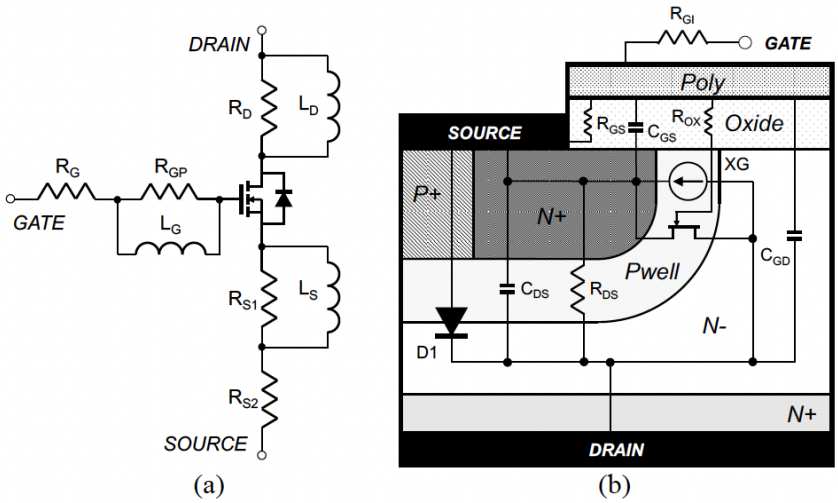


Figure 4.2: Subcircuit model of SiC MOSFET used in behavior model proposed by Hsu *et al.* [33]

[34]

is used. Referring to the device structure shown in Fig. 4.2, when $V_{GS} = 0V$, the area $Pwell - N^- - N^+$ forms a partial pinch-off JFET with some leakage current. When applying a negative V_{GS}, the field effect pinches-off the channel and is purely body diode effect.

To model the CV characteristics, C_{GS} is modelled as a constant parameter C_{GS0}. C_{DS} formulation is shown in Equation 4.3. V_{bi} is the built-in voltage across the P/N drift region.

$$C_{DS} = C_{DS0} \cdot (\frac{V_{bi}}{V_{bi} + V_{DS}})^M \tag{4.3}$$

C_{GD} (Equation 4.4) also uses hyperbolic function. It is calculated using a transition voltage parameter (V_{CGDT}), depletion width (t_{GDdep}) and oxide thickness (t_{ox}).

$$C_{GD} = \frac{\epsilon_{SiC} \cdot A_{GD}}{t_{ox} + t_{GDdep}} \tag{4.4}$$

$$t_{GDdep} = \frac{1}{2}1 - tanh(V_{GD} - V_{CGDT})\sqrt{\frac{2\epsilon_{SiC}|V_{CGDT-V_{GD}}|}{qn_{dope}}} \tag{4.5}$$

$$V_{bi} = \frac{kT}{q} ln(\frac{n_{dope} \cdot 10^{16}}{n_i^2}) \tag{4.6}$$

The model shows a good fit in terms of both current and capacitance curves and is easy to use. However, the model is not scalable since the intrinsic region uses the empirical Angelov model discussed before. It needs more effort when fitting for a device with different dimension/specifications. In terms of C_{DS} modeling, it only considers the depletion charge, but the reverse recovery charge is not captured, which is an important metric for diode switching from on to off-state.

Yang *et al.* proposed a nonsegmented empirical SPICE model for SiC MOSFET [35]. The cross-section along with the proposed subcircuit model is shown in Fig. 4.3. This work mainly improves the I_{DS} and C_{gd} formulations.

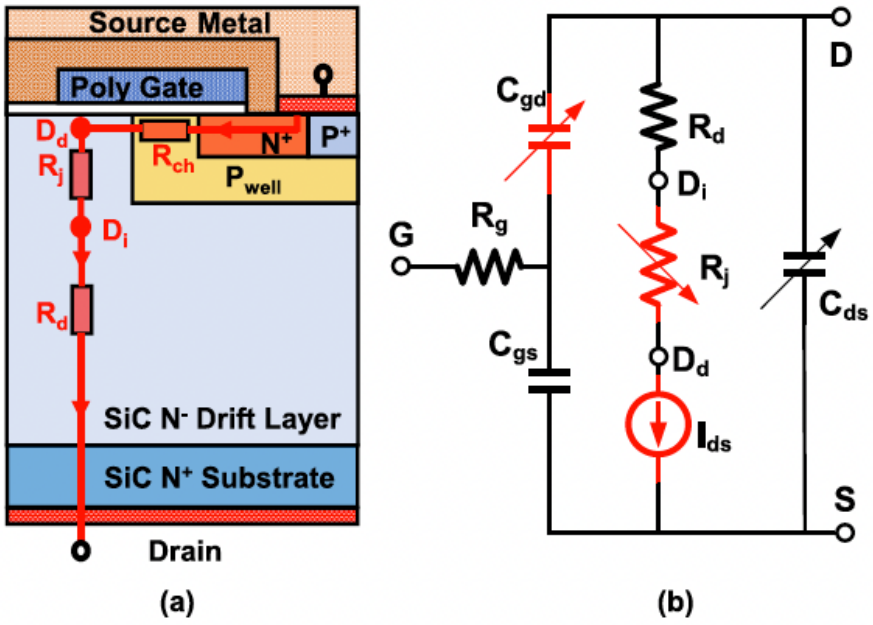


Figure 4.3: Cross section, with subcircuit model, used in [36]

To model the 1^{st} quadrant I-V behaviour, the current formulation (Equation 4.7) is very similar to Angelov model. tanh(x) function is used. Voltage difference between two sides of the surface inversion channel is represented as V_{Dds}.

$$I_{DS} = K_n \cdot (V_{GS} - V_{th})^{\alpha} \cdot tanh(\beta \cdot V_{DdS}) \tag{4.7}$$

When tanh(x) equals to x (x close to 0), V_{Dds} is small, the equation describes the MOSFET in linear region.

$$I_{DS} = K_n \cdot (V_{GS} - V_{th})^{\alpha} \cdot \beta \cdot V_{DdS} \tag{4.8}$$

On the other hand, when tanh(x) is close to 1 (x is large), the current equation becomes the following, which describes the saturation region. In this way, non-segmented equations can be used to describe the channel current, with smooth transition from linear to saturation region.

To model the JFET region, which is the region between p-wells, the voltage dependence of JFET resistance is shown as the following, where V_{DiS} is the voltage between the internal node D_i and source electrode. R_{j0} is the JFET resistance when $V_{DiS} = 0$, and m is a fitting parameter. However, this equation is not differenciable at $V_{DiS} = 0$, so it does not pass the Gummel symmetry test.

$$R_j = R_{j0} \cdot (1 + m \cdot \sqrt{V_{DiS}}) \tag{4.9}$$

For C-V modeling, C_{GS}, C_{DS} are similar to other models. C_{GD} is carefully modeled especially at low drain bias to capture the immediate drop. Accurately modeling the nonlinear capacitance C_{gd} is crucial for simulating the switching characteristics of SiC MOSFETs.

Traditional capacitance model for C_{gd} describe two capacitors in series (C_{ox}, C_{dep}).[37] [38] [39]. Therefore, C_{gd} is expressed as

$$C_{gd} = \frac{C_{ox} \cdot C_{gd_dep}}{C_{ox} + C_{gd_dep}} \tag{4.10}$$

C_{gd_dep} is the depletion capacitance under the gate. It depends on permittivity of SiC (ϵ), width of the depletion region (d) and capacitance area (A).

$$C_{gd_dep} = \frac{\epsilon \cdot A}{d} \tag{4.11}$$

It can be re-formatted as in Equation 4.12, with C_{gd_dep0} being the p-n junction depeltion capacitance at zero drain bias and γ is a fitting parameter.

$$C_{gd_dep} = \frac{C_{gd_dep0}}{\sqrt{1+\gamma \cdot V_{DG}}} \tag{4.12}$$

This equation could accurately predict C_{DG} at $V_{DS} = 0$ or high V_{DS}. However, at low V_{DS}, p-well provides a strong shielding effect on the gate oxide, as shown in Figure 4.5. C_{gd} drops faster due to the shielding effect. To capture this effect, a hyperbolic function (Equation 4.13) is used for C_{gd}, where $\gamma_1, \gamma_2, \gamma_3$ are fitting parameters. C_{gd0} represents the C_{ox} when $tanh(x) = 0$. C_{dg} becomes to Equation 4.12 for high V_{DS} and $tanh(x)$ approaches unity. C_{gdmin} is to ensure that C_{gd} will saturate to a constant value for high drain bias.

$$C_{gd} = \frac{C_{gd0} \cdot (1 - \gamma_1 \cdot tanh(\gamma_2 \cdot V_{DG}))}{\sqrt{1+\gamma_3 V_{DG}}} + C_{gdmin} \tag{4.13}$$

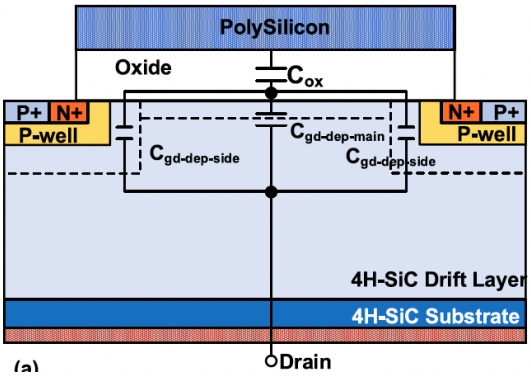


Figure 4.4: C_{gd} when $V_{ds} = 0$. The depletion width in accumulation and JFET region is small, C_{ox} dominates

This model achieves an accurate C_{gd} modeling, but the other modules are over simplified such as the JFET and drift region. The model is not comprehensive enough to cover all the critical physical effects such as temperature dependence, 3^{rd} quadrant behaviour and reverse recovery effect. It is also not scalable with structural and technology parameters.

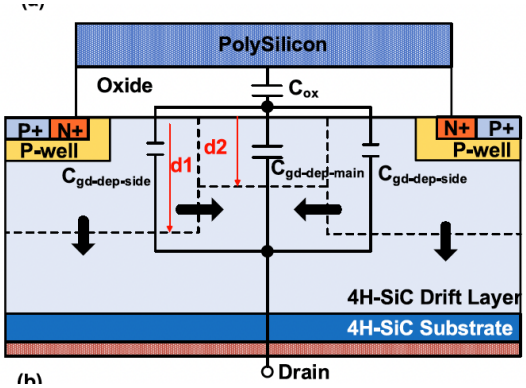


Figure 4.5: C_{gd} when V_{ds} is low. The depletion width in accummulation and JFET region increases, C_{gd} drops faster due to the shielding effect from the adjacent p-wells.

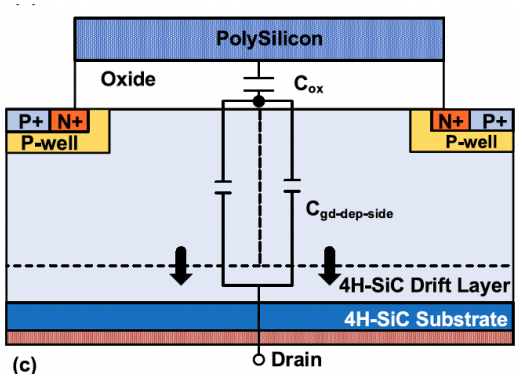
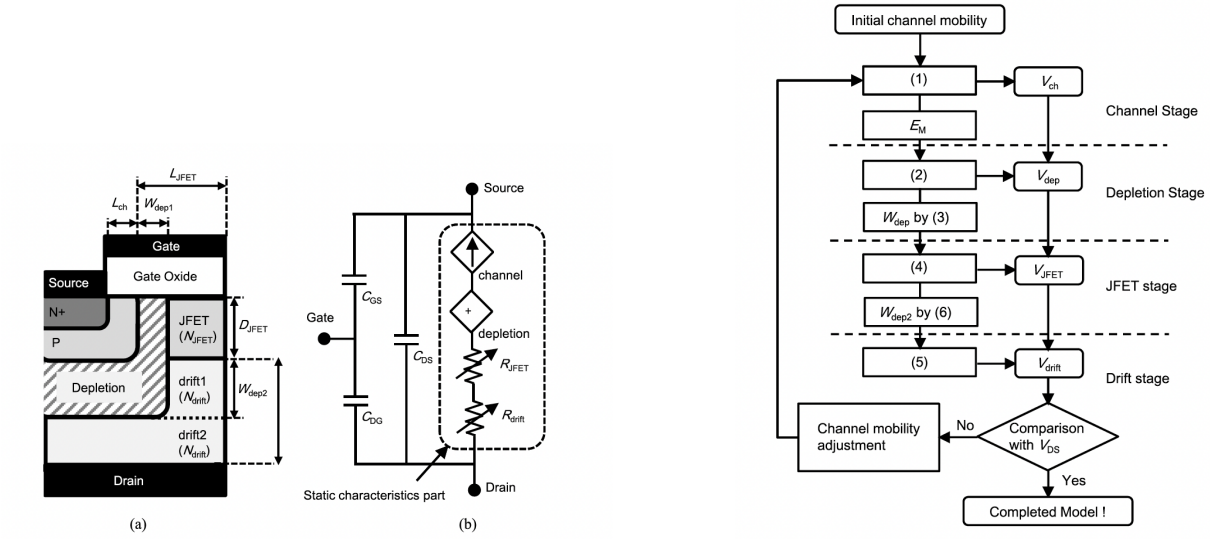


Figure 4.6: C_{gd} when V_{ds} is high. The depletion width in accummulation and JFET region is large, C_{gd_dep} dominates.

4.2 Physics-based Model

Mukunoki *et al.* introduced a model featuring adjustable channel mobility in [40] [41]. Schematic and extraction flow are shown in Fig 4.7. The physical structure consists of intrinsic channel, depletion region, JFET stage and drift stage connecting in series. Voltage drop at each stage is calculated and then compare with the measurement to get a correct mobility based on the fact that mobility decreases as I_D increasing.



(a) cross-section and subcircuit model

(b) Parameter extraction flow

Figure 4.7: Cross-section, subcircuit model and extraction flow proposed by Mukunoki *et al.*, from [40]

The voltage drop at each stage is calculated in Equation 4.14 - Equation 4.20. The notation of variables/parameters can be found in [40] [41]. The current depends on μ at different position in the inverted channel. W_{dep1}, W_{dep2} calculate depletion width at sidewall and bottom junction respectively, which models the non-linear behavior of JFET and drift regions.

$$I_D = C_{ox}(V_{GS} - V_{th} - V_{ch}(x))\mu_c h\frac{\Delta V}{\Delta x} \tag{4.14}$$

$$V_{dep} = \frac{E_M^2 \varepsilon_{SiC}}{2qN_{JFET}} \tag{4.15}$$

$$W_{dep1} = \sqrt{\frac{2\varepsilon_{SiC} V_{dep}}{qN_{JFET}}} \tag{4.16}$$

$$V_{JFET} = \frac{I_D D_{JFET}}{qN_{JFET} 2(L_{JFET} - W(dep1)) Z\mu_{bulk}} \tag{4.17}$$

$$W_{dep2} = \sqrt{\frac{2\varepsilon_{SiC}(V_{dep} + V_{bi} + V_{JFET}}{qN_{dfirt}}} \tag{4.18}$$

$$V_{drift1} = \frac{I_D W_{dep2}}{qN_{drift} 2(L_{JFET} - W_{dep1} Z\mu_{bulk})} \tag{4.19}$$

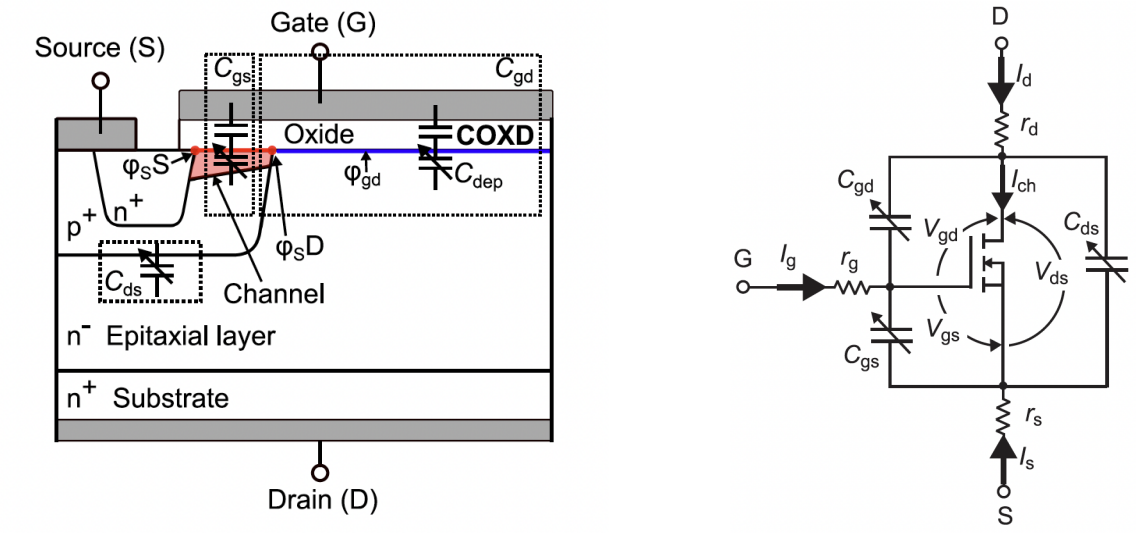
$$V_{drift2} = \frac{I_D(D_{drift} - W_{wdep2})}{qN_{drift} A\mu_{bulk}} \tag{4.20}$$

Additionally, the C_{GD} is calculated through gate-charge measurements under various bias conditions. Finally, an exponential function is used to describe C_{DG} in terms of both V_{GS} and V_{DS}.

Overall, parameter μ helps to reduce the computational complexity of the conduction branch without significantly compromising accuracy. However, the total number of parameters are still not enough to capture all the critical physical behaviors such as short channel effects, velocity/mobility saturation and temperature dependence. It also requires iterations of fitting to get the calibrated model. It accurately models the non-linearity in JFET and drift regions through calculating the depletion width, but the model still lacks a complete picture of the SiC MOSFET such as third-quadrant current behavior and body diode reverse-recovery charge.

Shintani *et al.* presented a model based on surface potential [37] [42]. The vertical double-diffused MOSFET structure, along with the equivalent circuit of the proposed model is shown in Fig. 4.8a, 4.8b respectively.

Considering the carrier trapping at the $SiC/SiO2$ interface, the model could accurately capture the electron mobility due to interface traps. It consists of the device current through the MOSFET channel (I_d), and three internal capacitances (C_{gs}, C_{ds}, C_{gd}). The surface potential of the MOS structure is used to derive I_{ch}. I_{ch} equation is shown in Equation 4.21 and I_{DD} is expressed in terms of surface potential. The detailed equations can be found in [37] [42].



(a) Cross-section

(b) subcircuit model

Figure 4.8: Cross-section and subcircuit model proposed by Shintani, from [37]

$$I_{ch} = L \cdot \mu_{eff} \cdot I_{DD} \tag{4.21}$$

C_{gd} is also derived using surface potential. The mobile charges resulting from capacitive coupling are calculated by surface potential at the channel. The MOS capacitance C_{gd} are then derived from the mobile charge.

The terminal current I_d is computed as Equation 4.22. The charge terms (Q_{ds}, Q_{gd}) are from taking integral of their corresponding capacitance equation (C_{dep}), which are also computed from surface potential.

$$I_d = I_{ch} + \frac{Q_{ds}}{dt} - \frac{Q_{gd}}{dt} \tag{4.22}$$

Since the model is physically accurate, the I-V and C-V fit shows excellent fit over a wide voltage and temperature range. It uses surface potential for all the current, capacitance and charge calculations, resulting self-consistency between sub-modules. However, this model does not include all the critical physical effects such as drift region, body diode current and reverse-recovery charge.

Yan *et al.* demonstrated a compact model that extends the BSIM3 model for SiC power MOSFET [43]. BSIM3 family models are proven to be highly accurate, scalable, continuous and computationally robust for standard CMOS logic devices. Therefore, it is chosen to be the core channel model. Adding on to the core channel model, body diode and drift region resistance models are developed to suit for power MOSFETs. The drift resistance consists two parts. (1) accumulation and JFET region R_{dch} (2) deep drift region and drain substrate region R_{d0}

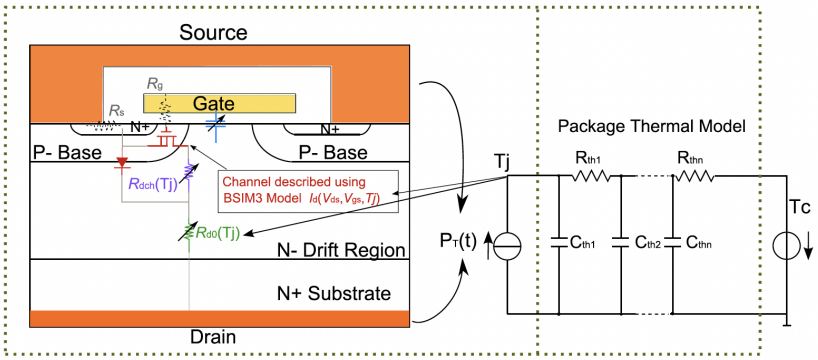


Figure 4.9: Cross section, including both subcircuit model and thermal subcircuit proposed by Yan *et al.* [43]

V_{drift} is the voltage across the drift region and R_{drift0} is the initial constant drift resistance. Velocity saturation is captured in $\alpha_{vsat}, V_{SAT,L}$. θ_{acc} takes into account the gate voltage bias.

$$R_{dch} = R_{drift0}[\frac{1 + (\frac{V_{drift}}{V_{SAT,L}})^{\alpha_{vsat}}}{1 + \theta_{acc} \cdot |V_{gs}|}] \tag{4.23}$$

The C_{dg} and body diode formulations are taken from existing models in BSIM3 with slight modifications. Lumped-charged based analytical model is used for model diode current and charge, which has complicated definition and lots of model parameters. It could potentially cause convergence problem.

This model shows good effort in modeling the intrinsic channel region, but the regions outside of the intrinsic channel (e.g. JFET, accumulation regions) are treated with empirical description. It lacks scalability and robustness in the JFET and accumulation region by using overly simplified physical model.

4.3 Summary on Current SiC MOSFET Compact Model

There have been lots of compact models proposed for SiC MOSFET, both empirical and physics-based models. The empirical models use a large number of fitting parameter to fit the device under specific geometry, bias and temperature to the measurement data. It lacks physical insight and scalability, but is computationally efficient and simple to implement in circuit simulators.

On the other hand, physics-based models use equations from semiconductor physics. Most parameters have clear physical meaning, facilitating the calibration process and providing a way to validate the extracted parameters. It also achieves self-consistency since current, charge and capacitance are based on same physics origins. The main limitation is those equations could be computational intensive, which needs extra care for approximating the equations to make the solution close-form. It might also need detailed process or structure information of the device, which is not available for most commercial devices.

Both empirical and physics-based models demonstrate accurate modeling for the intrinsic channel with inverted layer. Besides that, the capacitance (C_{gd}), body diode, JFET, and drift region are usually added as separate modules and most of the models use similar forms. The main limitation on the current the compact model is that they do not cover all the aspects in SiC MOSFET. Most of them lack one or several aspects such as accurate C_{gd} modeling, 3^{rd} quadrant behavior through body diode modeling, reverse recovery charge in body diode and scalability/temperature dependence/velocity saturation with non-linear drift region.

Chapter 5

SiC MOSFET Compact Model

This chapter introduces the second application using modular formulation approach - WAVSiC, a comprehensive and user-friendly physics-based compact model for SiC MOSFETs. Compared with the first application of a multi-channel SBD, it uses completely different semiconductor material with different device structures, but the same method could still be applied.

The model formulation, including details of the modular approach and construction of each basic module are explained. The model can automatically account for scalability with device channel-length and other dimensions, as well as critical effects from body diode, JFET depletion, and non-linear drift resistance. Good agreement has been achieved between simulation using fitted model and experimental measurements, for both a commercial 650V device and a commercial 1200V device, showing the accuracy, scalability and flexibility of the proposed model. The model has also been validated for computational efficiency and robustness, circuit simulator compatibility, and is ready for PDK adoption.

5.1 Motivation

The PE field has been rapidly growing, accelerated by a massive adoption of electric vehicle with a market size exceeding $2 Billion. SiC is actively employed as the next generation PE technology, due to its inherent strengths of high breakdown voltage, high electric field, high-operating temperature, high-switching frequency and low losses [2]. To facilitate circuit design with SiC transistors and development of PDKs, there is a growing demand for compact models that are accurate, scalable, robust and standardized.

5.2 Model Formulation

We propose Waterloo Virtual-source SiC MOSFET Model (WAVSiC), which is a physics-based compact model for SiC MOSFET inheriting the virtual source concept from the original MIT Virtual Source Compact Model, known for its simplicity to capture essential physics with a very small number of parameters ($\sim$ 20 parameters per transistor, most of which have clearly defined physical meanings).

WAVSiC is applicable for both planar-gate and trench-gate SiC MOSFETs, which are currently adopted by industry. The cross-section of typical planar-gate and trench-gate SiC MOSFET is shown in Figure 5.1.

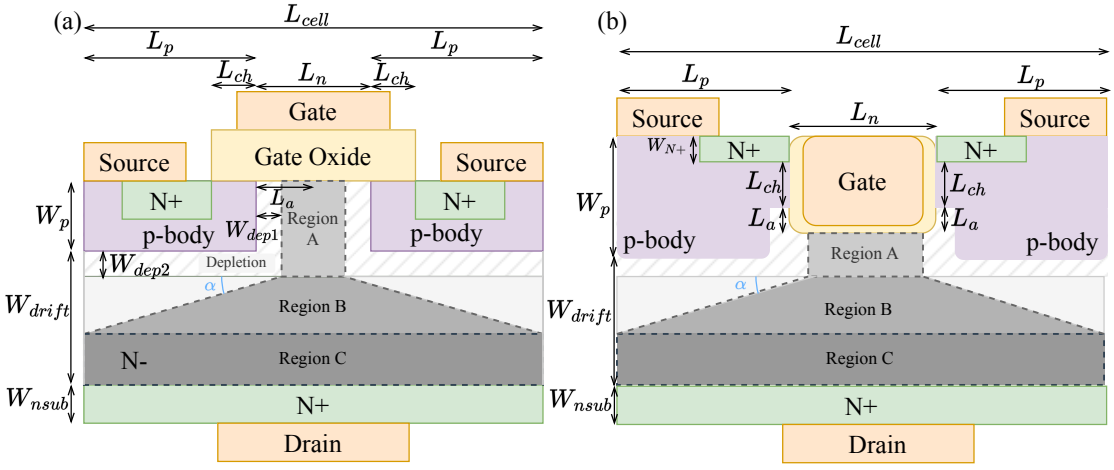


Figure 5.1: Cross section of typical SiC MOSFETs with dimensions labeled for (a) planar-gate and (b) trench-gate structures.

The model is constructed through a modular formation, by mapping each physical region in the device into one of the basic modules. The equivalent circuit accounting for current terms is shown in Fig. 5.2, with some charge terms. The shades are color-mapped to the specific physical regions in its cross-section. Using this subcircuit model, we can trace the channel current path at ON state. The carriers travel through source contact (R_{CS}), heavily-doped source region (R_S), intrinsic core region with inverted channel (M_1 closely modulated by V_G), accumulation region (M_A loosely modulated by V_G), vertical JFET region (M_{J1}, M_{J2}, modeled as implicitly-gated transistors and can be deactivated if negligible), non-linear drift resistance from the epi regions (R_{DR1}, R_{DR2}), heavily doped

substrate region (R_D), and drain contact (R_{CD}). The junction body diode (D_J) and sidewall body diode (D_{SW}) account for third-quadrant behavior. The breakdown current is implemented through D_{BD}.

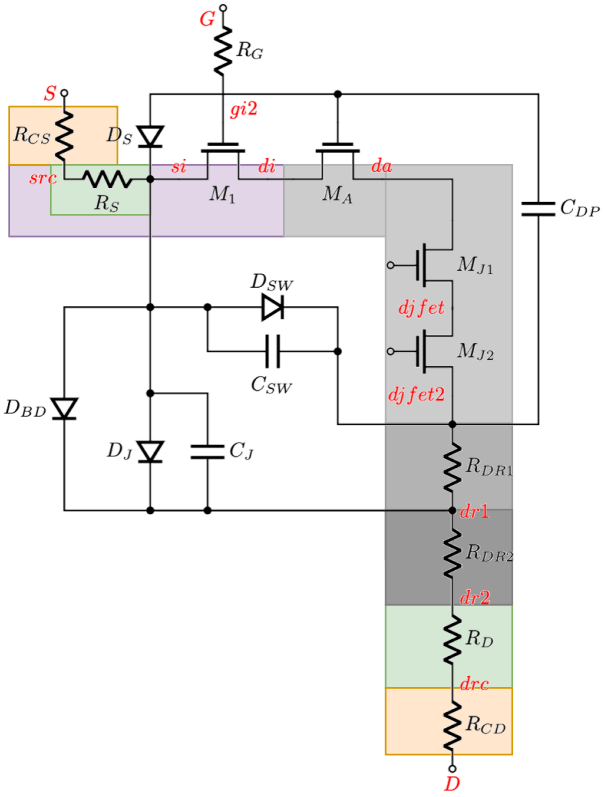


Figure 5.2: (a) The equivalent circuit of the proposed model, with the shades color-mapped to the specific physical regions in Fig. 5.1.

Fig. 5.3 lists the mapping of key dimensional parameters for each element in the netlist (e.g. channel length for each transistor, length and depth for two non-linear resistors). This model is able to model both planar-gate and trench-gate structures by correctly passing the dimensional data following the label in Fig. 5.1. The main difference between two structures is in the JFET region. Some trench structures might not have it. The model is able to deactivate the JFET region, by setting its channel length to 0, to account for that situation.

	Channel length
M_1	L_{ch}
M_A	L_a
M_{J1}	Planar: W_p
	Trench: $W_p - L_{ch} - L_a$

	Length	Depth
R_{DR1}	From L_n to L_{cell}	$L_p \cdot \tan(\alpha)$
R_{DR2}	L_{cell}	$W_{drift} - L_p \cdot \tan(\alpha)$

Figure 5.3: Key dimensional parameters for transistors (M_1, M_A, M_{J1}) and drift resistors (R_{DR1}, R_{DR2}) linked to device physical dimensions defined in Fig. 5.1 (a) and (b). M_{J2} is deactivated in this case.

All the transistors in the equivalent circuit (M_1, M_A, M_{J1}, M_{J2}) use the T-Module equations and all the diodes (D_{BD}, D_J, D_{SW}) use the D-Module equations. R_{DR1}, R_{DR2} are two non-linear drift resistors, which are newly added named as R-Module. C_J, C_{SW} are the corresponding capacitance components for two body diodes which are updated in this model. Lastly, voltage-dependent C_{DP} is computed separately. Such modular model formation approach where most of these basic modules have been proven efficient, scalable and computationally robust in the family of MVSG compact models developed for Gallium-nitride (GaN) devices (including GaN HEMTs for both radio-frequency and PE applications [21], kilo-volt multi-channel GaN diodes [1], GaN-based transmission-line non-linear resistors [23]). The MVSG GaN HEMT model has been approved and supported as an industry-standard model by Compact Model Coaltion (CMC) [15].

The complete list of charge components are presented in Fig. 5.4. The intrinsic channel capacitances (C_{GS} and C_{GD}) are computed self-consistently with the channel current through the core transistor. C_{DP} accounts for voltage-dependent charges in the accumulation and JFET regions. Body-diode related charges are accounted for by C_J (for junction diode) and C_{SW} (for side-wall diode), each of which captures both junction depletion charges (for reverse bias condition) and reverse-recovery charges (for forward bias condition). Bias-independent overlap capacitance ($C_{OVERLAP}$) and bias-dependent fringing capacitance (C_{OFS}) are also included.

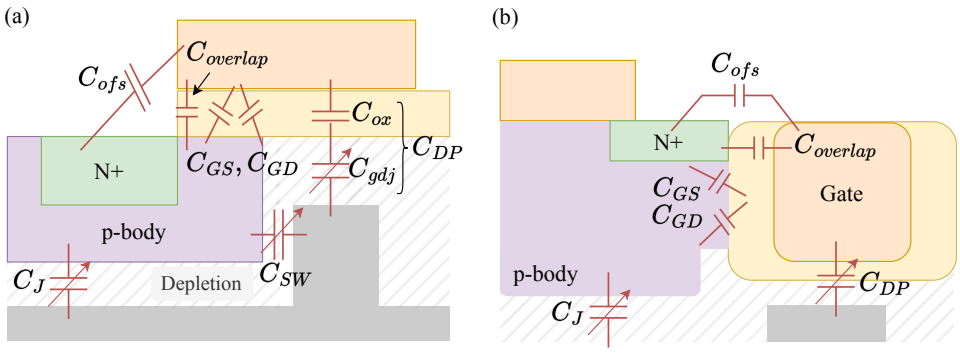


Figure 5.4: Illustration of capacitances included in the proposed WAVSiC model for (a) planar-gate and (b) trench-gate structures.

5.2.1 T-Module

The transistor module: (key equations presented in Chapter 2) It is used to model all regions with transistor-like behaviors. This includes the intrinsic core region and accumulation region, both modulated by the gate terminal. The current and charge/capacitance terms in T-Module follows drift-diffusion transport, with smooth transitioning between sub-threshold and above-threshold and between linear and saturation regions. The module is able to capture (1) scalability between long channel and short channel, (2) non-linear effect such as velocity saturation and self-heating, (3) channel charge computed self-consistently with channel current, (4) temperature dependence, and (5) other short channel effects such as Drain Induced Barrier Lowering (DIBL). T-Module is also used to describe JFET region (M_{J1}) by assigning an implicit gate, following [23]. A second JFET transistor (M_{J2}, deactivated by default) is included to provide flexibility to account for two different doping levels in the overall JFET region. Both M_{J1} and M_{J2} can be deactivated (shorted) for those trench structures where JFET region is negligible. Using T-Module for accumulation and JFET regions allow comprehensive physical effects (such as voltage and temperature dependence, velocity saturation, short channel effects, etc) to be properly accounted for.

5.2.2 D-Module

The diode module: (key current equations presented in Chapter 2 and capacitance equations are newly added) It is used to model all diode related behaviors. The current in the D-Module has components computing forward junction current (including high-injection effect), reverse-recombination current, and breakdown effect. Pairing charge equations in

D-Module (schematic shown in Figure 5.5) account for junction depletion charges (Q_{dep}) and reverse-recombination charges (Q_{rr}) [44] (Equation 5.1).

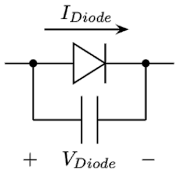


Figure 5.5: Junction diode with its paring capacitor

$$Q_{J/SW} = Q_{rr} + Q_{dep} \tag{5.1}$$

Reverse recovery charge When diode switches from on to off-state, the charges initially stored (exponential relationship with applied voltage) in the depletion region have to leave before the reverse-recombination current dominates. The formulations are inspired from [45]. Q_{rr} (Equation 5.2) is calculated with unit-area reverse recovery charge at zero bias ($qrr0$) and diffusion length (ld). High injection effect is realized through k_{hinj}. k_{wdep} is proportional to $exp(\frac{-wdep_{lim}}{l_d})$, with equation in Equation 5.3. Depletion width at zero bias is $wdep0$ and $wdep_{lim}$ ensures that the depletion width would be capped at the maximum depletion width w_i, shown in Equation 5.4. The depletion width $wdep$ is calculated in Equation 5.5, where the maximum voltage across the diode is also capped at v_f, shown in Equation 5.6.

$$Q_{rr} = qrr0 \cdot ld \cdot k_{hinj} \cdot k_{wdep} \tag{5.2}$$

$$k_{wdep} = \frac{exp(\frac{-wdep_{lim}}{ld}) - exp(\frac{-wi}{ld})}{exp(\frac{-wdep0}{ld}) - exp(\frac{-wi}{ld})} \tag{5.3}$$

$$wdep_{lim} = min(wdep, wi) \tag{5.4}$$

$$wdep = wdep0 \cdot \sqrt{\frac{vbi - v_{diode_lim}}{vbi}} \tag{5.5}$$

$$v_{diode_lim} = min(v_{diode}, v_f) \tag{5.6}$$

The effect of reverse recovery charges is demonstrated for a turning-off process of a single diode, shown in Fig. 5.6. When the diode is switching from on to off-state, the current has to first drop to negative and then return to 0.

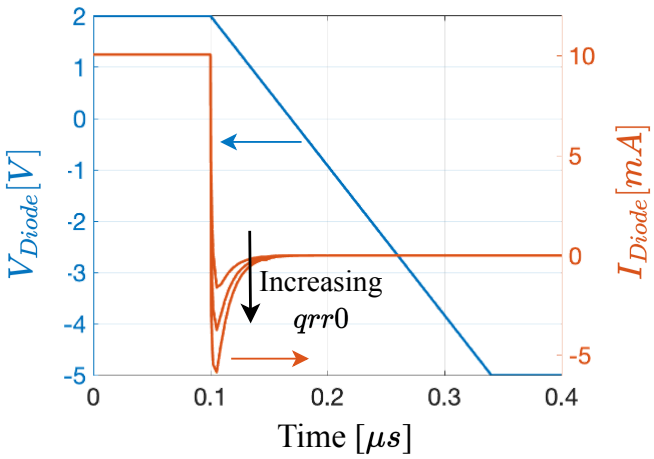


Figure 5.6: Reverse recovery current vs voltage during a turning-off process of a single diode. $qrr0$ is a fitting parameter to describe the amount of reverse recovery charge.

Depletion charge: It is the charge stored in the device under reverse bias. Q_{dep} (Equation 5.7) is relevant to zero-bias unit area junction capacitance c_{j0} and built-in potential vbi. v_{diode_lim} takes the minimum between diode turn-on voltage v_f and voltage across the diode v_{diode}, which ensures the depletion charge has a maximum value.

$$Q_{dep} = 2c_{j0} \cdot w \cdot ngf \cdot vbi \cdot \sqrt{1 - \sqrt{1 - \frac{v_{diode_lim}}{vbi}}} \tag{5.7}$$

5.2.3 R-Module

A third resistance module (**R-Module**) is newly added for the drift resistance in Region B and C of Fig. 5.1. The key equations are developed following approximation and approaches in [46] [47] [48]. A schematic is shown in Fig 5.7 to help explain the equations.

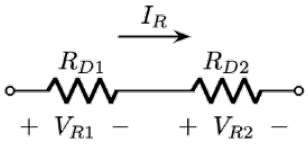


Figure 5.7: Schematic of two drift resistors in series

R_{DR1} (Equation 5.8) is calculated following a constant-angle (α) current spread model, computed by integration of the elemental resistance in Region B. $w \cdot ngf$ is the total device width, $\rho_{r1,2}$ is the resistivity reflecting doping level and carrier mobility including temperature dependence, α is a fitting parameter determining the spread angle. Velocity saturation effect is included in $E_{c1,2}$, where $E_{c1,2} = \frac{v_{sat}}{\mu}$ indicates the critical E-field for on-set of velocity saturation.

$$V_{R1} = \rho_{r1} \cdot \frac{I_R}{w \cdot ngf} \cdot tan(\alpha) \cdot ln(1 + \frac{l_p}{l_a - \frac{l_R}{w \cdot ngf} \cdot \frac{\rho_{r1}}{E_{c1}}}) \tag{5.8}$$

R_{DR2} (Equation 5.9) is calculated using a transmission line model, including velocity saturation (through E_{c2}), resistivity ρ_{r2}. Its width is l_{cell} and depth is $w_{drift} - l_p \cdot tan(\alpha)$.

$$V_{R2} = \rho_{r2} \cdot \frac{I_R}{w \cdot ngf} \cdot \frac{w_{drift} - l_p \cdot tan(\alpha)}{l_{cell} - I_R \cdot \frac{\rho_{r2}}{E_{c2}}} \tag{5.9}$$

5.2.4 Additional Modules

Temperature dependence are implemented in all three basic modules (e.g. through temperature coefficients for mobility, saturation velocity, threshold voltage, bandgap, etc.) In addition to the three basic modules and voltage-independent lumped resistors ($R_{CS}, R_{CD}, R_S, R_D, R_G$) and capacitance ($C_{OVERLAP}$), two bias-dependent capacitance are also introduced.

C_{DP} calculates the capacitance from gate oxide above the accumulation region (C_{OX}) in series with the capacitance of the depletion of JFET region (C_{gdj}) (Fig. 5.8. With high drain bias, depletion width increases, C_{gdj} dominates, while with more negative drain bias, C_{ox} dominates. C_{ox} is a fitting parameter representing the oxide capacitance above Region A.

C_{OFS} is the gate-to-source fringing capacitance with an option to include the slight depletion of the source region near the gate at very low V_G, following [16].

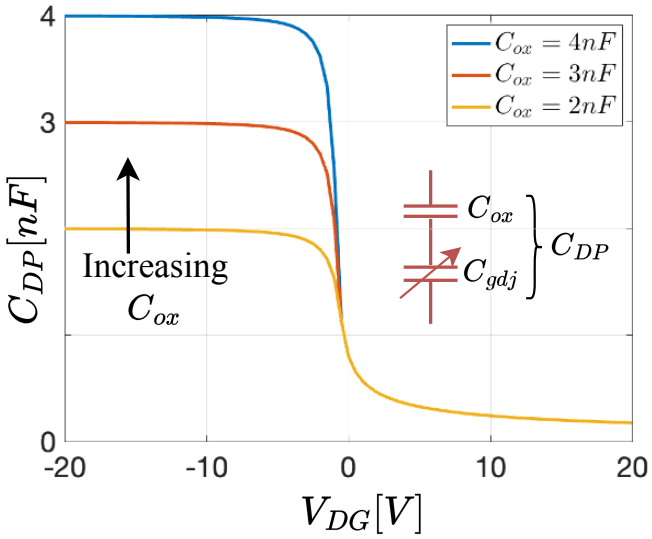


Figure 5.8: Voltage-dependent charge in the accumulation and JFET region versus V_{DG}.

Overall, different modules explained above are connected together to formulate the equivalent circuit shown in Fig. 5.2. The model is capable of describing both planar (Fig. 5.1 (a)) and trench (Fig. 5.1 (b)) structures by mapping the dimensions of the corresponding basic module according to Fig. 5.2 (c). A preliminary thermal subcircuit (Fig. 5.2 (b)) is used to account for the internal (self) device heating and also allowing thermal coupling from adjacent components to be defined at the netlist level. Further additions to the thermal network can be easily done to account for different system-level thermal and cooling capabilities by introducing separate thermal R-C network for different regions of the device. Computational robustness, such as convergence, continuity, and Gummel symmetry near zero drain bias, have been verified.

5.3 Extraction Flow

To get the calibrated physical compact model that can be used in circuit simulations, an extraction flow is shown in Fig. 5.9. Required data ($I_D - V_G, I_D - V_D, Q_G, C - V$) and key parameters in certain modules to be extracted are listed for each step. WAVSiC model inherits the advantage from MVS and MVSG that most parameters have clear physical meanings (such as threshold voltage, mobility, saturation velocity, DIBL, etc).

Modular formation of WAVSiC also allows the user to clearly link the specific regions in the measurement results with parameters of certain modules. For example, $I-V$ curves with lower V_{GS}/higher V_{DS} are dominated by the core transistor M_1, while those with higher V_{GS}/lower V_{DS} are more influenced from the rest of the device; contribution from different capacitance/charge terms in different regions of $C-V$ data can also be traced.

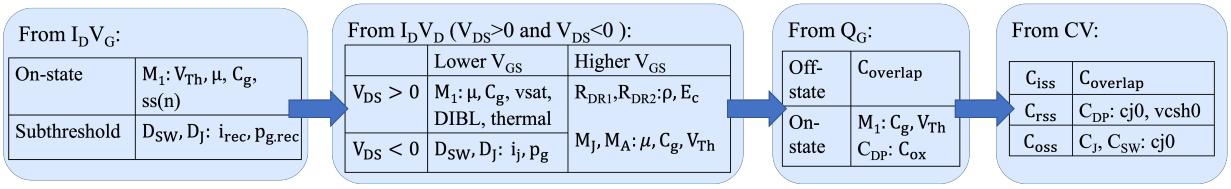


Figure 5.9: Summary of parameter extraction flow.

Step I: In terms of $I_D - V_{GS}$ curve, it is easy to extract the threshold voltage of the core transistor M_1, together with its mobility and unit-area gate capacitance. For the subthreshold current, which is not shown in Figure 5.10, it is relevant to subthreshold slope in M_1 and also reverse-recombination current parameters in two body diodes.

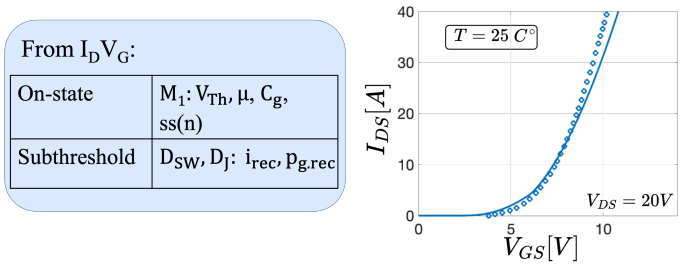


Figure 5.10: Step I in parameter extraction for WAVSiC.

Step II: For $I_D - V_D$ curve, if we first look at the 1^{st} quadrant behavior when V_{DS} is positive, it can be separated into two regions (low V_{GS} and high V_{GS}). At low V_{GS}, the core transistor M_1 dominates the overall on-state resistance, therefore mobility, unit-area gate capacitance, velocity saturation parameters could be extracted for M_1. At high V_{GS}, the two drift resistors will contribute more, so the slope is determined by resistivity and maximum electric field for R_{DR1}, R_{DR2}. At higher V_{DS}, short channel effects and thermal effects related parameters could be extracted. Afterwards looking at the 3^{rd} quadrant behavior when V_{DS} is negative. It can also be separated into low/high V_{GS} regions. When V_{GS} is low (e.g. 0V), the transistor is in off-state, current is due to the forward current

of the two body diodes. When V_{GS} is high (e.g. 10, 15V), the transistor is in on-state. The transistor branch will contribute to the overall current, which is related to parameters for M_1, R_{DR1}, R_{DR2}. When V_{DS} is larger up to several hundred volts (not shown in the Figure), JFET and Accumulation region will block larger voltage drop. The current will become more relevant to parameters of M_J, M_A .

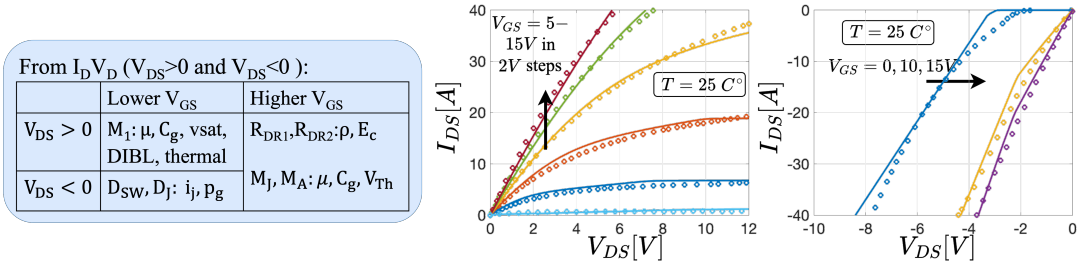


Figure 5.11: Step II in parameter extraction for WAVSiC.

Step III: The circuit schematic for simulating the $V_{GS} vs Q_G$ is shown in Figure 5.12. A constant current is applying to the gate and the transistor will switch on. During the off-state, all the current will be charging C_{gs}. When V_{GS} hits the miller plateau, the current starts charging the miller capacitor C_{GD}, then parameters related to C_{DP} could be projected. It can also be used to validate if the C_g, V_{Th} parameters extracted before are correct.

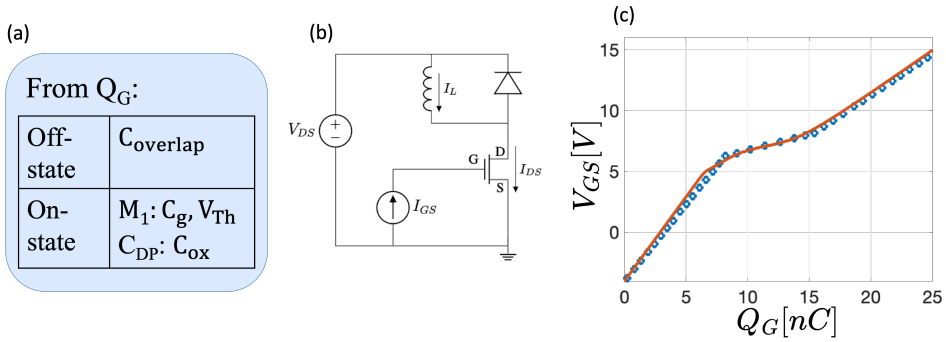


Figure 5.12: Step III in parameter extraction for WAVSiC.

Step IV: Lastly, The capacitance curve will help to determine the charge component parameters. C_{iss}, C_{rss} which has already been extracted before. $C_{oss} = C_{gd} + C_{ds}$, which helps to determine the charge components for two body diodes.

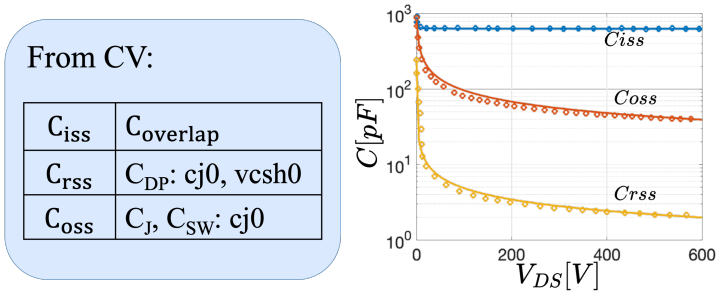


Figure 5.13: Step IV in parameter extraction for WAVSiC.

Several rounds of tuning might be needed to get a calibrated model covering all the measurement data since lots of parameters appear several times in the complete parameter extraction flow.

5.4 Results: Model vs Measurement

Following the parameter extraction flow summarized in Fig. 5.9, the model is fitted to the measurement of a commercial 650V planar-gate SiC MOSFET. The model shows excellent fit for 1^{st} quadrant I-V at three temperatures - 25°, −40° and 175°. It takes the advantage that most parameters in T-Module and D-Module have temperature coefficients. The model also shows excellent fit for third-quadrant I-V and $I_{DS}V_{GS}$ curve, shown in Figure 5.15.

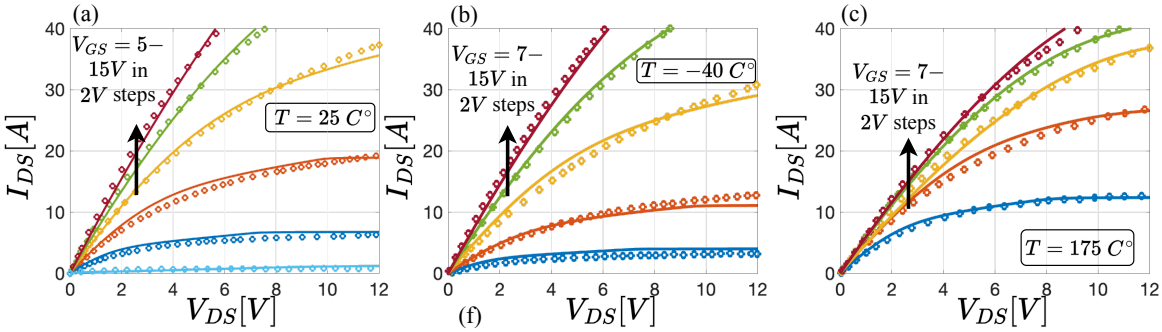


Figure 5.14: Comparison between proposed model simulation results (solid lines) and device measurement results of a commercial 650V SiC power MOSFET (circles).

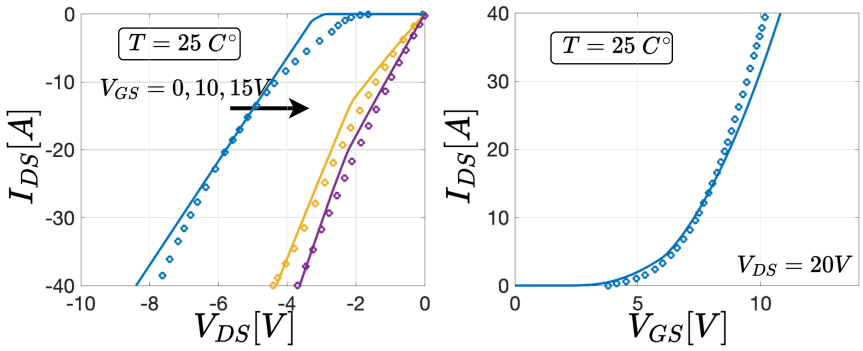


Figure 5.15: Third quadrant current and $I_{DS}V_{GS}$

Comparison between proposed model simulation results (solid lines) and device measurement results of a commercial 650V SiC power MOSFET (circles). The proposed model shows excellent match for $C_{iss}, C_{oss}, C_{rss}$, shown in Fig. 5.16.

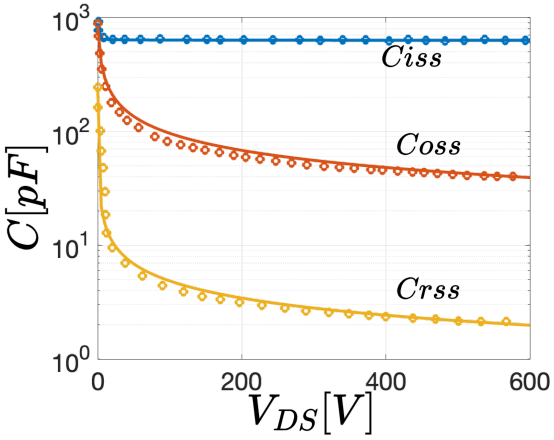


Figure 5.16: Capacitance fitting

Using the fitted model, gate charge simulation also matches well with the measurement performed using the set up shown in Fig. 5.17. The transition and Miller plateau is accurately captured.

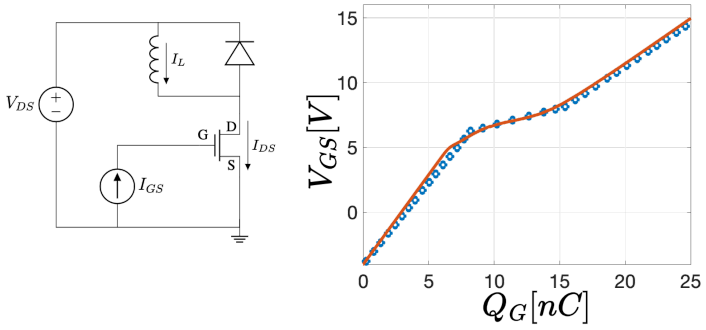


Figure 5.17: Gate charge measurement schematic and V_{GS} versus Q_G

The key parameters used to generate the fitting in Figure 5.14, 5.15, 5.16 and 5.17 is shown in Figure 5.18 and 5.19. The diode parameters are not shown here, due to the existing problem in modeling the third-quadrant I_DV_D curve when V_{GS} is near the threshold voltage. The body diode module still needs to be modified to accommodate the V_{GS} dependence.

	M_1	M_A	M_J
L [µm]	0.5	0.1	1
V_{Th} [V]	-4	-5	-640
C_g [F/m^2]	1.7e-2	5e-2	7e-4
SS [V/dec]	0.12	3.2	0.3
v_x [m/s]	1e5	1.2e5	1e5
µ [m^2/(Vs)]	4e-3	4e-3	5e-2

	R_{DR1}	R_{DR2}
W_{drift} [µm]	10	
α [°]	45	
ρ [$\Omega \cdot m$]	2e-4	2e-4
E_c [V/m]	3e6	3e6

Figure 5.18: Key parameters for transistors and drift region resistors used to generate fitting for 650V SiC MOSFET

The contribution of each region to total resistance R_{DS} is illustrated at different bias conditions, matching expected trends and composition. The composition of the R_{DS} of the 650V power MOSFET predicted by the proposed model with V_{GS} from 9 to 17V and V_{DS} at 2V (solid shade, in linear region for ON resistance) and 10V (striped shade, in/approaching saturation region). R_{DS} is contributed by channel region (purple), accumulation and JFET regions (green), and other resistive regions including epi, substrate, source/drain (grey). With relatively low V_{GS}, the gated transistor M_1 contributes to most of the resistance. When V_{GS} increases, the resistance of the non-linear resistors in the epi

	C_J	C_{SW}
C_{j0} [F/m^2]	3e-2	3e-2
V_{bi} [V]	0.8	0.8
m_j	0.5	0.5
l_{d0} [m]	1e-6	1e-6
V_f [V]	0.6	0.6
W_{depo} [m]	0.1e-6	0.1e-6
$qrr_0[C/m^2]$	5e-3	8e-3

	C_{DP}
V_{csh0} [V]	0.04
C_{csh0} [F/m^2]	9e-3
$C_0[F/m^2]$	7e-10
V_0 [V]	0

Figure 5.19: Key parameters for diode charges and voltage-dependent C_{DP} used to generate fitting for 650V SiC MOSFET

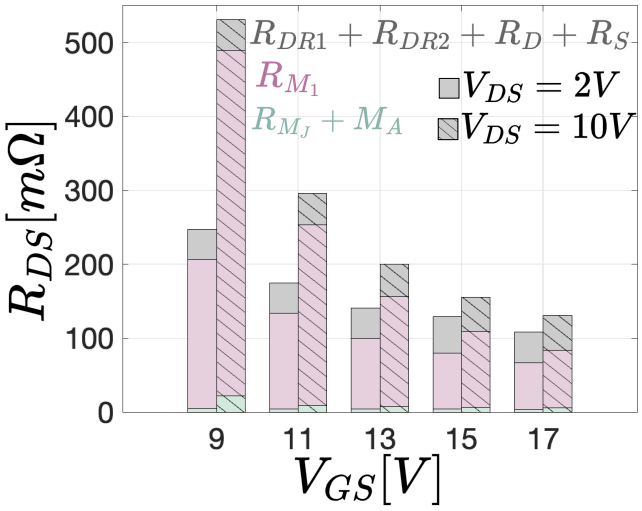


Figure 5.20: R_{DS} contribution due to intrinsic transistor, accummulation, JFET, drift resistor region for 650V SiC MOSFET

layers (R_{DR1}, R_{DR2}) increases due to velocity saturation. At higher V_{DS}, the resistance due to core is significantly higher due to current saturation, and the accumulation and JFET regions is higher due to the depletion in the JFET region.

Double Pulse Test (DPT) is also fitted with the proposed model. Photo of DPT test setup is shown in Fig. 5.21. The power loop consists of a DC power supply (V_{DC}), 10uF

DC input capacitance (C_{DC}), 5mH inductor (L), 1200V/10A free-wheeling diode (FWD), and the 650V SiC MOSFET as device under test (DUT). The gate driver circuit is used to generate +18V/-4V gate trigger signals. A 0.1 Ω current shunt and a 1.0kV passive voltage probe are used to capture the current and voltage waveforms.

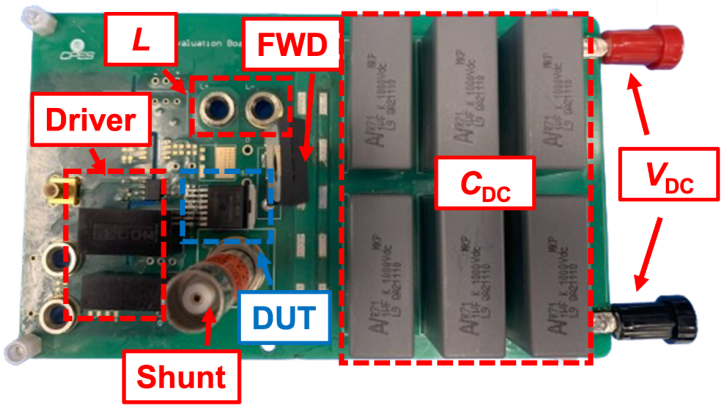


Figure 5.21: DPT test set-up for 650V SiC MOSFET

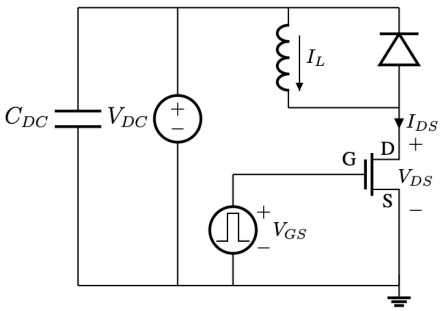


Figure 5.22: DPT circuit schematic

Circuit schematics shown in Fig. 5.22 is used to simulate the DPT test.

Comparison of model simulation results (line) with the measurement (circles) for voltage and current through DUT. Good agreement has also been achieved with a DPT for both voltage and current.

Zoom-in waveforms around 20μs and 30μs also show excellent fit for both hard turn-off and hard turn-on conditions.

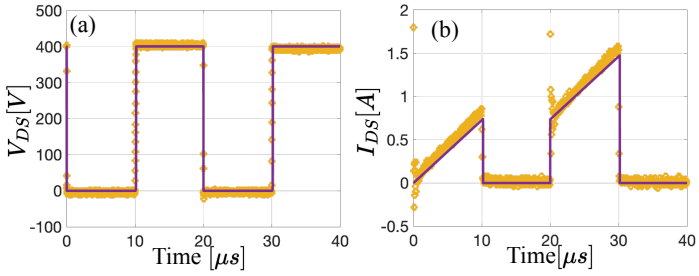


Figure 5.23: DPT current and voltage up to 40 μs

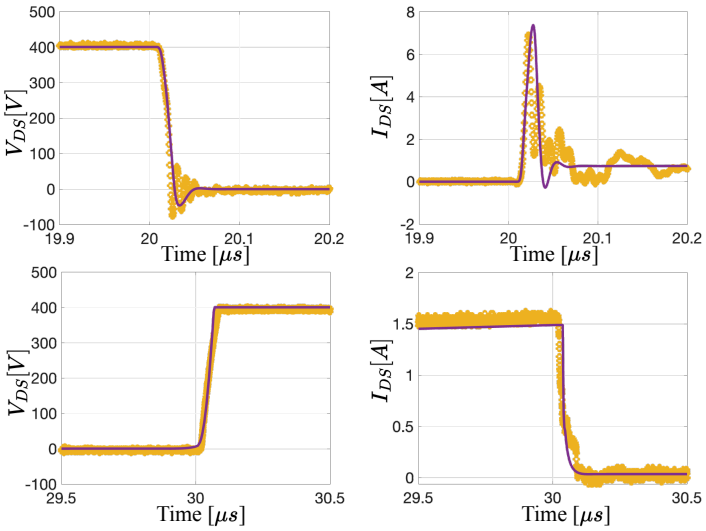


Figure 5.24: Zoom-in waveform at turn-on and turn-off point.

To demonstrate the scalability, the model has also been fitted to a commercial 1200V SiC MOSFET. Similar high quality has been achieved, with excellent agreement between simulation and measurement for I-V, C-V, and gate charge (Fig. 5.25), including (a) forward $I_D - V_D$ (b) 3^{rd} quadrant $I_D - V_D$ (c) $I_D - V_G$, (d) C-V, and (e) gate charge Q_G, all at 25°. The predicted contributions from different regions to the total resistance in linear and saturation are shown in (f), following the same legend as Fig. 5.20 (h). The drift region resistance contributes more to the overall on-state resistance since the drift region is longer for 1200V device, which matches our expectation. This proves the accuracy and scalability of the proposed model. With good scalability, the proposed physics-based model can also serve as a useful tool for technology projection, benchmarking, and device optimization.

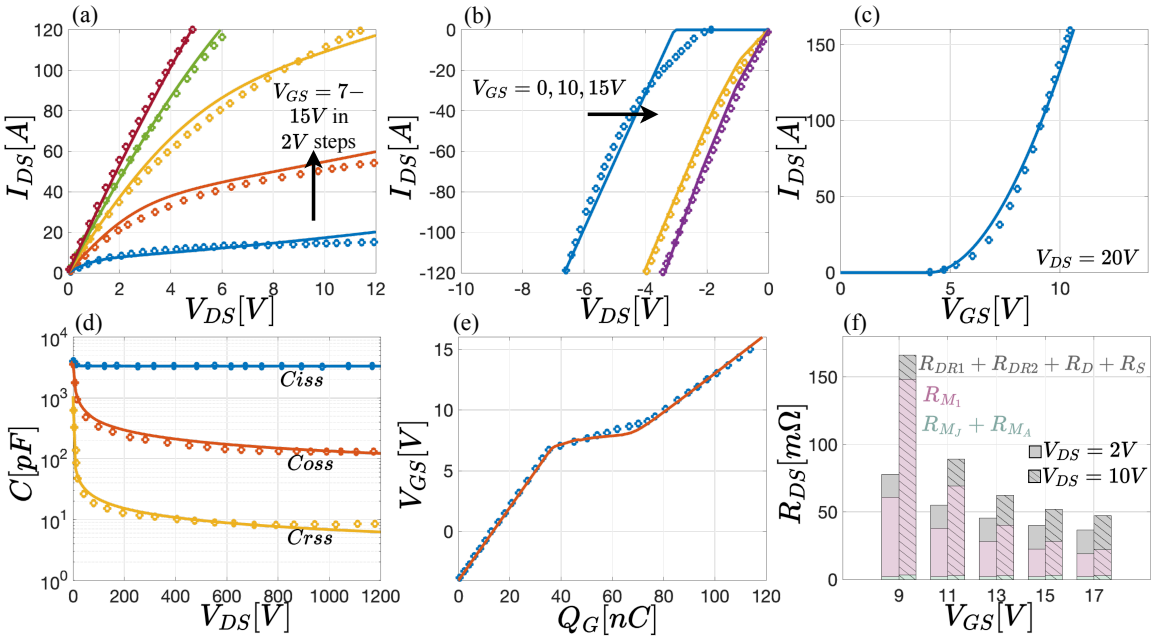


Figure 5.25: Comparison between proposed model simulation results (solid lines) and device measurement results (circles) of a commercial 1200V SiC power MOSFET

5.5 Summary on SiC MOSFET Compact Model

WAVSiC is constructed with a balance of rich physics and user friendliness. It accounts for comprehensive physical effects (e.g. voltage dependent capacitances, current/charge from body diodes, temperature dependence, non-linear effects and short channel effects in channel/JFET/epi regions, etc), and also shows excellent scalability, accuracy and computational efficiency and robustness. The model and parameter extraction is easy to understand and use by the designers, given each module has a clear mapping to one of the physical region and most of the model parameters also carry clear physical meanings.

With the modular approach, the model is flexible to adapt for different device structures and processes. For regions outside of the channel (e.g. JFET, accumulation and epi regions), proper physics are implemented to account for dependence on dimensions, bias, and temperatures. Verilog-A code package has been developed for WAVSiC, compatible with major circuit simulators (such as Spectre®, ADS®, and HSPICE®) and ready for PDK implementation. As a candidate being considered for SiC industry standard model,

the model has been implemented following CMC-recommended Verilog-A practice, with proving computational robustness and efficiency. The model has been validated across several mainstream circuit simulators and is ready for PDK integration.

Chapter 6

Summary and future work

6.1 Conclusions

To facilitate the circuit simulation using GaN/SiC transistors with innovative device architectures, a coherent modular formulation approach is used to model a multi-channel SBD and a SiC MOSFET. Since both T-Module and D-Module equations are from MVSG, which is an industry-standard model by CMC, it inherits the advantages of the model's accuracy, completeness, scalability and computational robustness. The benefit also includes that most parameters have clear physical meanings, such as threshold voltage, mobility, saturation velocity and DIBL. It allows users to clearly link the specific regions in the measurement results with parameters of certain modules. Parameter exaction flow are also defined for both compact models.

In terms of the Multi-channel AlGaN/GaN SBD, T-Module is applied for the region under the gate electrode and the RESURF region. D-Module is used for Schottky contact between drain contact and all five channels, reverse-recombination current and channel breakdown. Unique physical effects are captured through setting threshold voltage of transistors in each channel to be the depletion voltage, reflected on the CV graph. Effective gate voltage of transistor in each channel is set to be the minimum between applied voltage and the threshold of the transistor above it in order to capture the charge screening effect.

In terms of SiC MOSFET, T-Module is used to describe the intrinsic core region with inverted channel, accumulation region with loose gate control and vertical JFET region. D-Module is used to describe the junction body diode and side-wall body diode to capture the third-quadrant current behaviour and channel breakdown. Charge terms from body diode,

including junction depletion charges and reverse-recovery charges are newly developed. R-Module is also developed to take into account the bottom drift region.

With the understanding of the device strcuture and operation, parameter extraction flow are developed for both models. Both models show excellent fit with measurement results. The multi-channel SBD is validated via IV, CV, breakdown and show good scalability with RESURF length. It is also used as a tool for technology optimization and scaling projections through simulations on (1) the impact of barrier/channel thickness on device capacitance and (2) the effect of RESURF length on the Baliga Figure-of-Merit (FoM) and area-scaling FoM. The SiC MOSFET is fitted to both a commercial 650V planar and a 1200V power device, both showing excellent agreement between simulation and measurement for IV, CV and gate charge. Good agreement has also been achieved with a double-pulse test (DPT) for both voltage and current in hard turn-off and hard turn-on conditions.

6.2 Future work

6.2.1 Multi-channel SBD Compact Model

Figure 6.1 illustrates the cross-section of a multi-channel transistor, where the Multi-Channel section is the same as the SBD structure. The proposed multi-channel SBD model could serve as the starting point with minimal adjustment such as separating source and gate terminals, ohmic contacts on both source/drain ends and connecting a series single-channel transistor. The cascading connection of another single-channel transistor also enables E-mode operation.

FinFET structures is another popular candidate to further improve power devices performance, with Figure 6.2 shown the cross-section of an n-channel Fin-MOSFET and Fin-JFET. Modular formulation approach could also be used, where the region under each fin-shape gate could be modeled as a gated-transistor or an implicitely-gated transistor (JFET) with different parameters. This method is very similar when modeling the multi-channel SBD. Unique physical effects such as self-heating and strain effects for FinFET should be studied and accounted for in the new compact model.

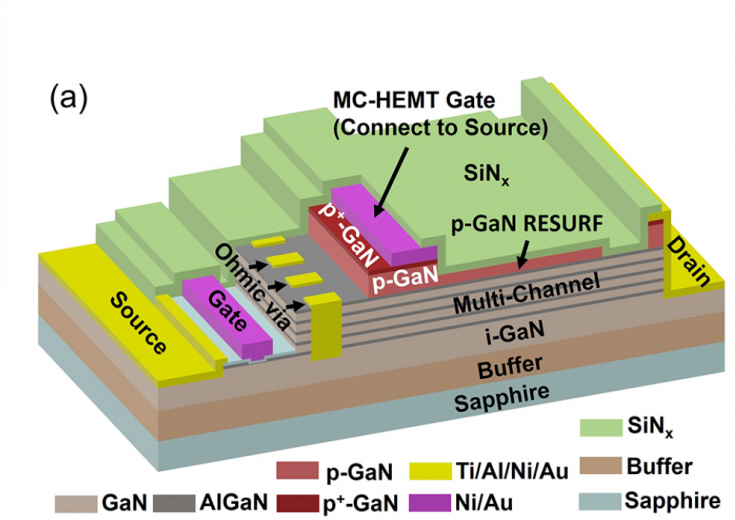


Figure 6.1: 3-D schematic of the AlGaN/GaN $MC^2 - HEMT$, fabricated in [25].

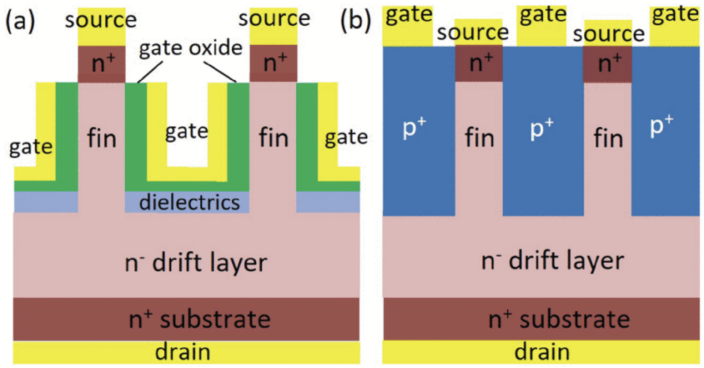


Figure 6.2: Cross-section of an n-channel (a) Fin-MOSFET and (b) Fin-JFET. [49]

6.2.2 SiC MOSFET Compact Model

There are still several problems in the current SiC MOSFET model, firstly, the model has a bad fitting for 3^{rd} quadrant behavior at low V_{GS} , when the transistor (M_1) is in off-state and the current is due to the forward current of two body diodes. V_{GS} dependence needs to be added to the body diode. Secondly, when plotting $C_{GD}vsV_{DS}$ in log scale, the capacitance does not show a sharp drop at very low V_{DS}, which is clearly shown in measurement. The charge formulations still need to be updated. Thirdly, in order for it to

also model a p-type transistor, another parameter $Type$ should be added, which will flip the voltage. The body diode should be flipped under the p-type condition.

Besides the problems, existing in the current model, there are also lots of future directions that could be explored. Firstly, the model is able to account for both planar-gate and trench-gate devices. However, only planar-gate devices fitting is demonstrated. The trench-gate structure still needs to be verified using the current compact model.

Secondly, the proposed SiC MOSFET compact model is able to predict the composition of the R_{DS} from gated transistor, non-linear resistors in the epi layers, accummulation and JFET regions. If the model predicts the correct physical behavior, this voltage drop should match the TCAD simulation results using the same dimensions. The TCAD simulation could further verify the physics in the model. If the model is able to predict the physics accurately and correctly, then it can serve as a useful tool for technology projection, benchmarking, and device optimization. Besides having accurate fitting with measurement data, it also helps the device-designers to further optimize/innovate on device-design using this model as a tool. The model has physical parameters which can be changed to preview how a modified device would look and how other device-metrics would change as a consequence.

Thirdly, lots of modules in the current model use empirical functions, which are separated to the core transistor module, such as breakdown effect and drain-to-gate capacitance. The breakdown voltage now is a fitting parameter and the current model could not predict it. Semiconductor physics could be explored to also change those modules into physics-based model. The trade-off is between accuracy, scalability and the computational efficient. Including more physics equations will make the model more difficult to converge but greatly enhance its physical meaning, which makes it useful as a projection/optimization tool for device/circuit engineers.

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