# Design of a Multi-Stage Power Amplifier for a 16 Element MIMO Transmitter Testbed

by

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## Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

## Abstract

The next-generation standard for fifth-generation (5G) wireless communication demands significant advancements in the transmitter front end compared to its predecessor. This need arises from the exponential increase in both data rate requirements and the number of connected devices. The primary approach to achieving these improvements relies on the adoption of massive multiple-input multiple-output (mMIMO) systems. These systems, combined with beamforming technology, which enhances the equivalent isotropic radiated power (EIRP) by focusing transmission power in specific directions, increase the data rate of the communication systems.

While 5G aims to leverage millimeter-wave frequencies for increased bandwidth and data rates, the sub-6 GHz spectrum remains valuable, offering a practical balance between range and performance. Given the new performance requirements, the power amplifier (PA) must exhibit high linearity to minimize memory effects and distortion. As the most power-intensive component in the transmitter chain, the PA also faces increasing efficiency challenges, particularly due to the rising peak-to-average power ratio (PAPR) in 5G systems. In mMIMO configurations, additional complexities arise from factors such as load mismatch and antenna crosstalk, which further impact PA performance. Just as important, electromagnetic interference (EMI) within the transmission chain itself can degrade overall system efficiency —an often overlooked concern, which is the issue that this thesis addresses.

To address these challenges, this thesis presents a multi-stage Class AB PA operating in the 3.2–3.8 GHz range, designed for linearization within a 4×4 mMIMO transmitter array. External aluminum shielding is also employed to counteract the EMI. The PA is evaluated through S-parameter, continuous-wave (CW), and modulated signal simulations. CW simulations indicate that the driver and PA together achieve a small-signal gain of approximately 23–25 dB. The PA, utilizing 6W MACOM CGHV1F006 transistors, reaches saturation at 37 dBm output power. The 1 dB compression point is observed around 36 dBm, providing a broad linearity range before saturation.

The PA-stage demonstrates power-added efficiency (PAE) between 54% and 61% at maximum power, with a maximum phase distortion of -4 degrees at high-power levels. Modulated signal simulations, conducted with a 100 MHz modulation bandwidth, confirm that the PA is linearizable under single-input single-output (SISO) digital predistortion (DPD). The application of DPD reduces the adjacent channel power ratio (ACPR) from -35 dBc to -55 dBc, demonstrating a significant improvement in linearity compared to the non-DPD case.

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# Chapter 1

# Introduction

## 1.1 Motivation

With the introduction of new technologies and tools, especially the Internet of Things (IoT), to the wireless world, the number of users and connected devices is facing a tremendous increase. This increase, in return, will generate unprecedented data traffic. In their current configuration, fourth-generation (4G) wireless systems are not capable of supplying the data demands of the exponentially growing number of links. That is why the industry is moving towards fifth-generation (5G) wireless systems, which will consider the mentioned hardships [14]. Multiple-input-multiple-output (MIMO) transmitters have been used in base-station (BS) in 4G transmitters, which is a technology that utilizes multiple antennas at both the transmitter and receiver to transmit and receive multiple data streams at the same time. 5G intends to elevate the system to an even higher level. 4G systems used have been using large and bulky antennas, and power amplifiers (PAs) that have high output power [15]. With 5G, the intention is to use hundreds or even thousands of antennas simultaneously to increase the data rates and throughput. These new MIMO structures will be referred to as massive MIMO (mMIMO), and they will also introduce higher modulation bandwidths compared to 4G systems, by switching to higher frequency bands.

The shift in the transmitter architecture will have consequences for both the antennas and the PAs. 4G PAs use bulky isolators or circulators between antennas and PAs to eliminate possible reflections to the PA which minimizes the interference. However, such a solution will not be available for 5G systems that are densely populated. This causes issues with PA linearity and efficiency, which degrades system performance. 5G is heavily

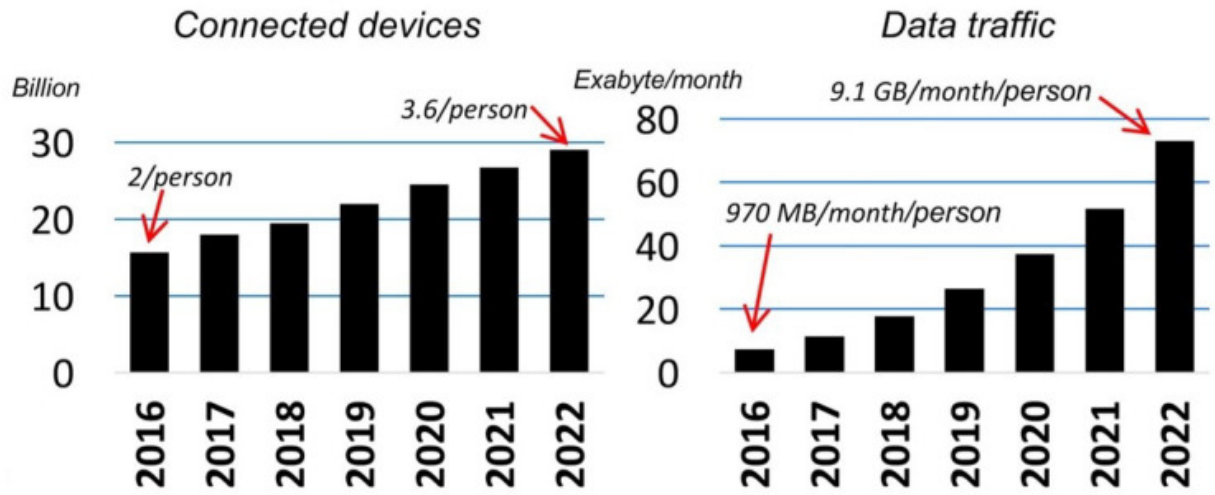



Figure 1.1: Plots showing the growth in the number of connected devices and data rate from 2016 to 2022 [1].

dependent on the modulation technique named orthogonal frequency division multiplexing (OFDM), which uses multiple orthogonal subcarriers for transmission. Although this technique grants high spectral efficiency and robustness against the multipath issue, it generates significantly high peak-to-average-power-ratio (PAPR), typically around 6-8 dB. This pushes the amplifier to non-linear regions of operation, which degrades signal quality and may cause leakage to adjacent channels.

## 1.2 Problem Statement

It is apparent that the 5G standards will require better performance in terms of linearity and efficiency from the transmitter front end, particularly from the PA. Different linearization techniques are being studied to combat performance degradation, one of the most widely used being digital pre-distortion [16]. Although this technique can cause significant improvement in linearity, it may also come at a cost of high power consumption for the hardware that executes the algorithm which can at times be significant, depending on the algorithm itself.

Furthermore, there are some significant problems that are coming up with the realization of 5G scenarios which are the crosstalk between individual antennas and the load mismatch between the PA and the antenna [17]. The antenna crosstalk is a phenomenon

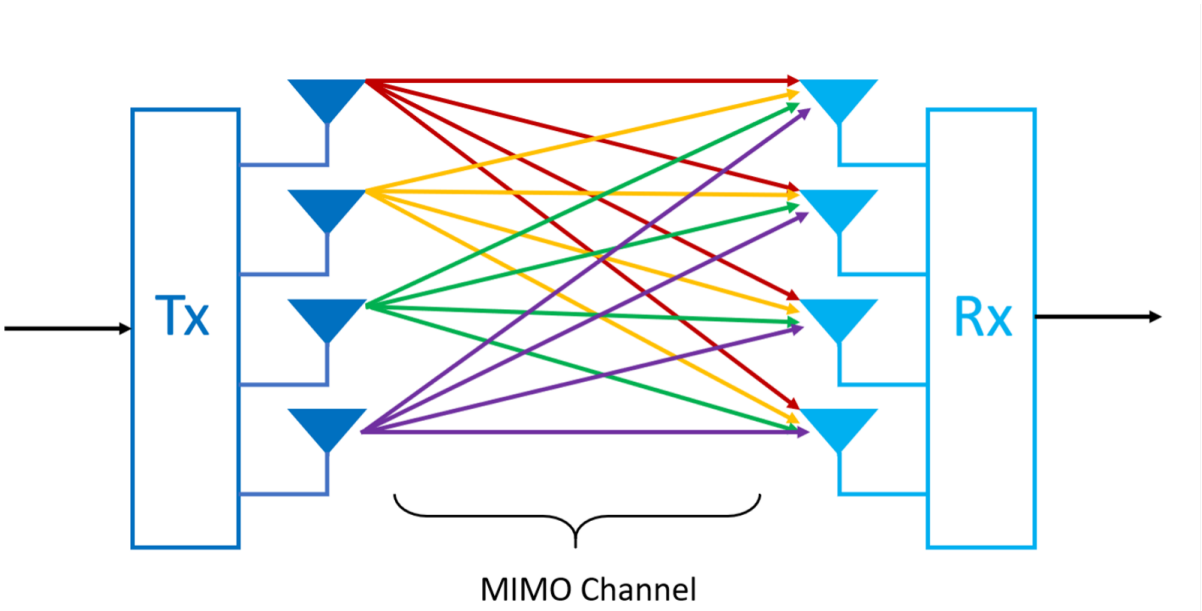



Figure 1.2: Transmitter and receiver shown in a MIMO architecture, different colors can correspond to different frequency bands or time-frames depending on the utilized duplexing scheme [2].

that further complicates the linearization effort that is carried out by the DPD. However, it is also observed that the radio frequency (RF) traces on the printed circuit board (PCB) can act as antennas and due to this rogue electrical fields can emerge, or the PAs themselves might also radiate RF waves at their outputs. Although antenna cross-talk and load mismatch are significant issues, the coupling between the PAs or the channels due to the mentioned electromagnetic interference (EMI) in these new very compact transmitters creates yet another nonlinearity issue for the PA to handle [12]. This would further burden the existing DPD algorithms.

This study intends to come up with a solution to the referred problem of designing a PA and its shielding against EMI, suited for the 5G systems in terms of efficiency and linearizability, to be scalable to a 16-channel, namely to a 4x4 transmitter testbed. The PA will be tested for continuous-wave (CW) simulations to assess the linearity and efficiency performance, and the transmitter array with be tested with 100 MHz OFDM signals for overall performance.

## 1.3 Thesis Organization

This thesis is organized as follows. In Chapter 2, the background information and literature review regarding the contents of the thesis are presented, intending to review the fundamental concepts related to the assertion of the thesis. To that end, an overview of the fundamentals of MIMO systems, PA design considerations, and essentials are discussed.

Chapter 3 goes through the design methodology of the transmitter module used in this thesis, which includes the design of the class-AB power amplifier, the driver amplifier, and the integration with the pre-driver stage.

Chapter 4 introduces the intricacies of shielding theory and design, and its incorporation into the designed PA. Then the shielded design is further extended to a mMIMO system with a mechanical design,

Lastly, Chapter 5 concludes the thesis with the important takeaways this work offers to the reader. In addition, what can be done to improve the performance and possibilities that might be of interest to other researchers are also elaborated upon.

# Chapter 2

# Background and Literature Review

## 2.1 mMIMO, Beamforming and the Role of Power Amplifiers

Massive MIMO is a technology that employs hundreds or thousands of antennas at base stations to enhance network capacity, data throughput, and spectral efficiency. These arrays provide significant antenna gain, and together with beamforming, allow radiated power to be directed toward specific locations. mMIMO and beamforming are essential components of 5G, with various beamforming architectures actively researched in academia. Beamforming is fundamentally a delay-and-sum process that can be implemented in either the analog or digital domain [18].

Analog beamforming, as the name suggests, performs the delay-and-sum operation in the analog domain. The main challenge is generating multiple simultaneous beams. To achieve this, the main path must be split, and each sub-path must be equipped with variable amplitude and phase (VAP) blocks and splitters. As the number of elements increases, these blocks consume significant space, making multiple beams impractical despite being theoretically feasible. Furthermore, analog beamforming has an inherent limit on the number of elements, as excessive splitting degrades signal power, potentially bringing it close to the noise floor, leading to signal loss. In digital beamforming (DBF), the delay-and-sum operation is performed digitally before the RF chains, which remain independent, unlike analog beamforming. DBF avoids the scalability issues of analog beamforming, making it suitable for large-scale arrays. However, its primary drawback is high power consumption and substantial hardware requirements, which impose practical limits on the number of

elements. Additionally, DBF enables dynamic reconfiguration of beams, a capability not feasible with analog methods. DBF also offers superior calibration and adaptive nulling, making it highly attractive for phased array applications in communications and radar systems [18].

Power amplifiers are typically the final component in the signal chain before the antenna. Their primary function is to amplify the modulated signal to a sufficiently high power level to ensure that transmission losses do not degrade the signal beyond recognition in the midst of white noise. However, achieving this objective requires addressing critical design metrics. For example, the input signal must be amplified with minimal distortion to maintain linearity and reduce bit error rate (BER) at the receiver. Linearity is also critically important when analyzing power spectrum density plots. If a device lacks sufficient linearity, the modulation products—discussed later—will become significantly pronounced. These products manifest at the edges of the frequency band in use and can interfere with neighboring bands, creating an undesirable situation [19].

Power amplifiers are the most energy-intensive components in the transmitter chain, with their power consumption often dominating the entire system. Thus, designing power amplifiers with high efficiency is essential, presenting a significant challenge for designers. Compounding this complexity, there is often a trade-off between linearity and efficiency, as improving one typically compromises the other. The following section will explore the principles and challenges of designing linear and efficient power amplifiers.

## 2.2 High-Power Amplifier Design

### 2.2.1 Linearity Characterization

The primary contributors to PA nonlinearity are transconductance and input capacitance nonlinearities [20]. Input capacitance mainly affects phase nonlinearity, while transconductance influences gain nonlinearity, varying with transistor biasing. At high power levels, transconductance nonlinearity becomes more prominent. Using a black-box PA model, we assume a sinusoidal input, $v_i(t)$ [4]:

$$v_i(t) = V_0 cos\omega_0 t, \tag{2.1}$$

where $V_0$ is the amplitude and $\omega_0$ is the angular frequency. The output of this black-box, $v_o(t)$ can be written as the following using the Taylor expansion:

$$v_o(t) = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \ldots, \tag{2.2}$$

where $a_0$, $a_1$, $a_2$, and $a_3$ are the Taylor coefficients which denotes the DC, linear, squared, and cubic multipliers respectively. Using equation 2.1, the output can be expanded as:

$$v_o(t) = a_0 + a_1 V_0 \cos\omega_0 t + a_2 V_0^2 \cos^2\omega_0 t + a_3 V_0^3 \cos^3\omega_0 t + \ldots \tag{2.3}$$

$$= \left(a_0 + \frac{1}{2}a_2 V_0^2\right) + \left(a_1 V_0 + \frac{3}{4}a_3 V_0^3\right)\cos\omega_0 t + \frac{1}{2}a_2 V_0^2 \cos 2\omega_0 t + \frac{1}{4}a_3 V_0^3 \cos 3\omega_0 t + \ldots. \tag{2.4}$$

Here one can observe that, the linear term of the output, is given as:

$$a_1 V_0 + \frac{3}{4}a_3 V_0^3. \tag{2.5}$$

This proves that harmonic distortion arises even with a linear input. The third harmonic contributes to gain expansion or compression, typically leading to compression as input power increases. The output 1 dB compression point ($OP_{1dB}$) quantifies this effect. While harmonics usually lie outside the band of interest, real signals are modulated rather than single-tone. Intermodulation distortions (IMD) occur when two-tone inputs create additional frequency components. Consider the following input, where $V_1$ and $V_2$ are the respective amplitudes, $\omega_1$ and $\omega_2$ are the respective angular frequencies:

$$v_i(t) = V_1 cos\omega_1 t + V_2 cos\omega_2 t. \tag{2.6}$$

When the two-tone input is inserted, the output then becomes:

$$\begin{aligned} v_o(t) = {} & \alpha_1\Big(V_1\cos(\omega_1 t) + V_2\cos(\omega_2 t)\Big) \\ & + \alpha_2\Big(V_1\cos(\omega_1 t) + V_2\cos(\omega_2 t)\Big)^2 \\ & + \alpha_3\Big(V_1\cos(\omega_1 t) + V_2\cos(\omega_2 t)\Big)^3 + \ldots. \end{aligned} \tag{2.7}$$

| **Frequency Components** | **Corresponding Terms** |
|---|---|
| $\omega_1, \omega_2$ | $\left(\alpha_1 + \frac{3\alpha_3 V_1^2}{4} + \frac{3\alpha_3 V_2^2}{2}\right) V_1 \cos(\omega_1 t)$ $+ \left(\alpha_1 + \frac{3\alpha_3 V_1^2}{4} + \frac{3\alpha_3 V_2^2}{2}\right) V_2 \cos(\omega_2 t)$ |
| $\omega_1 \pm \omega_2$ | $\alpha_2 V_1 V_2 \cos(\omega_1 + \omega_2)t$ $+\alpha_2 V_1 V_2 \cos(\omega_1 - \omega_2)t$ |
| $2\omega_1 \pm \omega_2$ | $\frac{3\alpha_3 V_1^2 V_2}{4} \cos(2\omega_1 + \omega_2)t$ $+\frac{3\alpha_3 V_1^2 V_2}{4} \cos(2\omega_1 - \omega_2)t$ |
| $2\omega_2 \pm \omega_1$ | $\frac{3\alpha_3 V_2^2 V_1}{4} \cos(2\omega_2 + \omega_1)t$ $+\frac{3\alpha_3 V_2^2 V_1}{4} \cos(2\omega_2 - \omega_1)t$ |

Table 2.1: Frequency components and the corresponding terms.

If the equation 2.7, is expanded and reorganized in a way that the frequency components that are akin are kept together, then the Table 2.1 can be constructed to evaluate the results.

As was the case with the single-tone input, for a two-tone input signal, we also see a gain compression effect on the linear terms. Third-order intermodulation products ($2\omega_1 \pm \omega_2$) can fall outside but close to the desired frequency band, leading to spectral regrowth. Adjacent channel power ratio (ACPR) quantifies this effect. Nonlinearities affecting PA performance are summarized by amplitude modulation to amplitude modulation (AM-AM) distortion, which describes gain compression, and amplitude modulation to phase modulation (AM-PM) distortion, which describes phase shifts depending on the change in amplitude. Both depend on transistor biasing and the PA class of operation.

### Linearization with Digital Pre-Distortion

Linearity is shown to be a major concern for the PA. Luckily, there are ways to improve the linearity in terms of AM-AM, AM-PM, and ACPR. Although all of them will not be

covered in this thesis, prominent examples of these methods are feedforward linearization, feedback linearization, linear amplification with nonlinear components (LINC), analog predistortion and DPD, which comes out as the method that is more frequently used in contemporary designs due to its significant linearization and adaptability in different PA variations, like load-modulated PAs. DPD uses memory polynomials to pre-correct the AM-AM and AM-PM distortions. This linearization technique can achieve significant ACPR improvement, which may be around 8 dB for 5G PA. However, DPD algorithms cause additional power consumption which may be significant depending on the deployed algorithm and polynomials [21].

### 2.2.2 Efficiency Characterization

Power amplifiers can be referred to as devices that convert DC power, $P_{DC}$, to RF power, $P_{out}$. A common metric for evaluating efficiency is called drain efficiency $\eta$.

$$\eta = 100\% \frac{P_{out}}{P_{DC}}. \tag{2.8}$$

However, there is a more realistic way of measuring the efficiency of a PA. Although, the drain efficiency underlines the efficiency of conversion from the DC power to RF power, it does not account for the gain of the PA, which is something crucial for an amplifier. This can be done with including the RF input power, $P_{in}$. Bearing this in mind, another metric, the power-added efficiency, PAE, can be calculated as the following,

$$PAE = 100\% \frac{P_{out} - P_{in}}{P_{DC}}. \tag{2.9}$$

Furthermore, the power amplifier efficiency will be crucial for energy saving and cooling for the entire system. Likewise linearity, the efficiency of the amplifier highly relies on the class of operation and the device that is being used. However, if the efficiency is evaluated not only at the saturated power levels, but at the average as well, one can see that there is room for improvement. There are many techniques that are being used to improve the efficiency at back-off levels, such as envelope tracking, outphasing technique, and load-modulated PAs. The Doherty power amplifier (DPA) is the most popular solution today, utilizing two PAs to enhance efficiency while dynamically modulating each other's seen loads [22].

### 2.2.3 Semiconductor Materials and Technologies

The selection of the transistor, particularly its semiconductor material, is as crucial as design techniques in power amplifier development, defining the maximum physical potential of the design. Different semiconductors offer trade-offs in power output, efficiency, linearity, and operating frequency. Common technologies include silicon-based semiconductors, gallium arsenide (GaAs), and gallium nitride (GaN).

Silicon-germanium (SiGe) is a strong contender among silicon-based devices for RF applications. It is widely used due to its broad operating frequency range, from DC up to 100 GHz. However, its limited power capabilities constrain its application. In general, silicon-based semiconductors generally struggle to achieve high power levels, with the exception of laterally diffused metal-oxide semiconductors (LDMOS). While LDMOS is effective for high-power applications, its efficiency declines beyond 2.5 GHz, and even Above 1.5 GHz, the output impedance of LDMOS becomes more challenging to match [23].

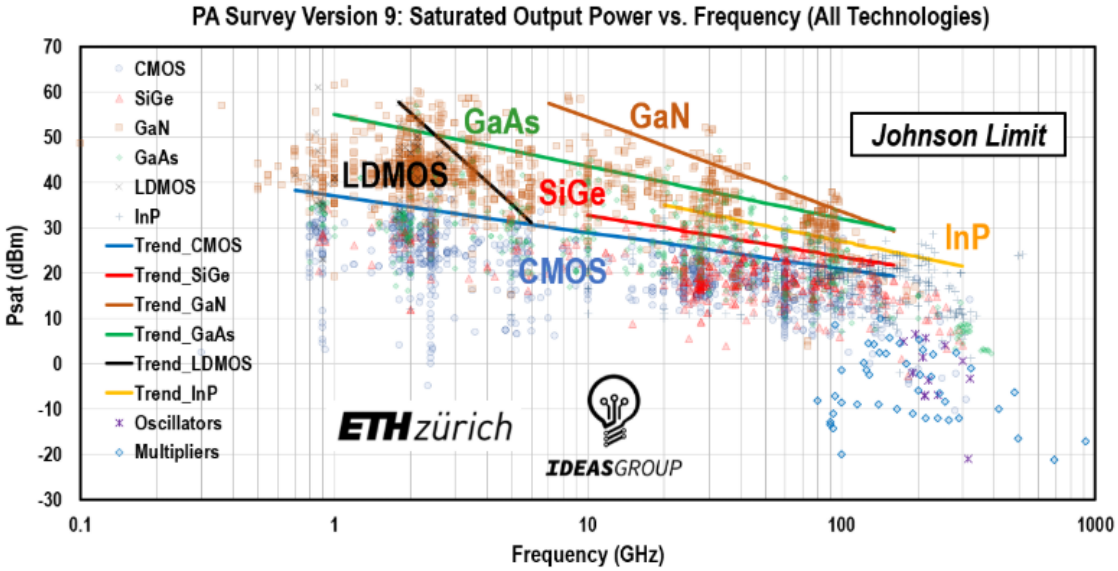



Figure 2.1: Comparison of various device technologies in delivered output power versus frequency [3].

GaN has gained widespread attention due to its advantageous properties. Its large bandgap enables high breakdown fields, allowing operation at voltages up to 100V, surpassing silicon-based devices. GaN devices also feature high saturation velocities, which

determine current density limits. Since output power depends on current and voltage, GaN devices achieve high power levels. Additionally, they offer excellent thermal properties, improving long-term reliability. However, while GaN excels in power, its linearity is inferior to silicon-based counterparts, particularly LDMOS. Gain compression occurs at lower power levels due to transconductance nonlinearity [24, 25].

### 2.2.4 PA Classes of Operation

The class of a power amplifier defines its mode of operation, which is primarily determined by the transistor's biasing. The amplifier's main characteristics, such as linearity, efficiency, and current profiles, are influenced by the chosen bias point. Each amplifier class offers distinct trade-offs in performance, balancing these characteristics differently. The class is determined by the device's DC operating point, which is set by its gate-to-source voltage, $V_{GS}$, drain-to-source voltage, $V_{DS}$, and drain current, $I_D$.

#### Class A

Class A operation is often considered the linear mode for most amplifiers. However, this does not imply that an amplifier must be biased in Class A to achieve linearity [26]. The principle of Class A amplifiers involves biasing the amplifier at the midpoint of the linear region and showing a load that will ensure that the entire voltage signal swing remains within this region, thereby maintaining linearity. In this mode of operation, the transistor is always turned ON.

The optimum load impedance, $R_{L,opt}$, can be calculated as the following:

$$R_{L,opt} = \frac{V_{DS,max} - V_{knee}}{I_{D,max}}, \tag{2.10}$$

where $V_{knee}$ is the knee voltage. The DC power consumption of the amplifier will be determined by

$$P_{DC} = I_{D,Q} V_{DS,Q} \tag{2.11}$$

where Q denotes the quiescent point, DC operating point, for that particular metric. Similarly, the RF power that can be delivered can be written as:

$$P_{RF} = \frac{1}{2} I_{D,RF} V_{DS,RF} = \frac{1}{2} \frac{I_{D,max}}{2} \frac{V_{DS,max} - V_{knee}}{2} \tag{2.12}$$

$$P_{RF} = \frac{1}{8} I_{D,max} (V_{DS,max} - V_{knee}) \tag{2.13}$$

If the knee region voltage is considerably low, one can see that equation 2.8 will lead to a drain efficiency of 50%. However, in most scenarios, this is not the case because devices in general do not have negligible knee region voltages.

### Class B

Class B amplifiers fall under the category of reduced conduction angle operation, meaning the transistor is not continuously active. In an ideal linear operation, a Class A amplifier takes a sinusoidal voltage input and produces a sinusoidal current output. In contrast, reduced conduction angle classes of operation use input waveforms that are perfect sinusoids but this input is presented in a clipped manner, resulting in output currents that are also not perfect sinusoids. This discrepancy introduces challenges, as the output voltage must remain sinusoidal. The simplest solution to address this issue is to include a resonator at the output to filter out unwanted harmonics. However, in most real-world applications, this method is seldom employed. Instead, the output-matching network itself is typically designed to filter the harmonics [27].

Revisiting 2.1 and adding the biasing voltage gives:

$$v_i(t) = V_b + V_0 cos\omega_0 t. \tag{2.14}$$

The voltage offset that the signal will have can be defined with $V_x = V_b - V_{th}$, where $V_{th}$ is the threshold and $V_b$ is the constant bias voltage for the transistor to start conducting current. In this case, the conduction angle can be defined as the following:

$$\phi = \cos^{-1}\left(\frac{V_x}{V_0}\right), \tag{2.15}$$

where conduction angle is $2\phi$. The conduction angle in this case is 180°, with the transistor being ON only half the time. This causes the DC power consumption is reduced by half, leading to improved efficiency compared to Class A operation, However, this

comes at the cost of reduced gain, 6 dB lower than Class A. Furthermore, equation 2.15, can be used together with Taylor expansion to calculate the frequency components that constitute the output waveform. For class B, the fundamental component will not vary with conduction angle; therefore, the linearity of the fundamental component will not be affected theoretically [27].

#### Class AB

Class AB operation serves as a middle ground between class A and class B in terms of biasing. In this mode, the conduction angle falls between 180° and 360°. Unlike a Class B amplifier, where the conduction angle remains fixed at 180°, a Class AB amplifier exhibits a variable conduction angle that depends on the input signal level. This variability introduces a nonlinear relationship between the input voltage and the fundamental output.

Similar to class B operation, harmonic components must be filtered to ensure a sinusoidal output. While linearity can be a concern, class AB amplifiers offer higher gain than class B and greater efficiency than class A. With proper biasing, an optimal balance between linearity, gain, and efficiency can be achieved.

| **Class of Operation** | **Efficiency** | **Linearity** | **Conduction Angle** |
|---|---|---|---|
| A | 50% | High | 360° |
| B | 78.5% | Medium | 180° |
| AB | 50%-78.5% | Varied | 180° to 360° |

Table 2.2: Comparison of the amplifier classes of operation.

### 2.2.5 Load and Source Pull Characterization

The optimal load impedance for a transistor depends on its characteristics and class of operation. This impedance must be carefully chosen to achieve the desired performance. For an ideal transistor, it can be derived from DC I-V curves.

Transistors are often modeled as voltage-controlled current sources (VCCS) [28]. They exist in various forms, including integrated circuits, die, and packaged devices. Packaged transistors typically have parasitics due to pads and interconnects, whereas die transistors

mainly have pad-related parasitics. These parasitics shift the optimal load impedance from theoretical values, making it complex rather than purely real.

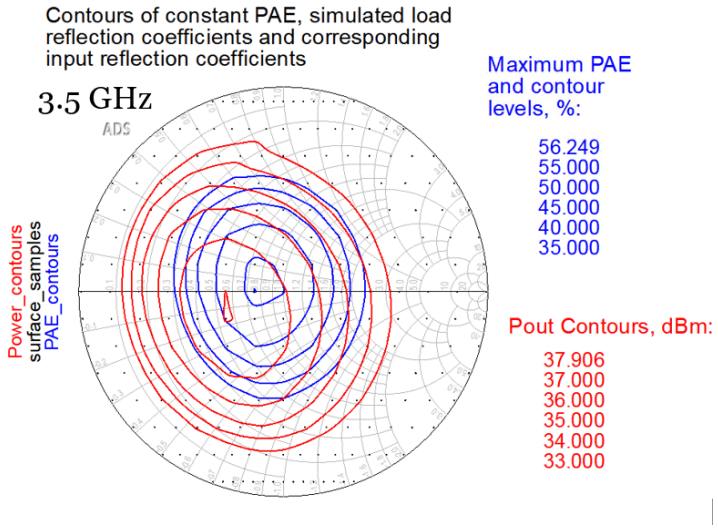



Figure 2.2: Load-pull results of a sample transistor at 3.5 GHz.

The optimal impedances for maximum power, efficiency, and gain would differ. Load pull is a widely used technique to determine these points by adjusting load tuners and measuring performance across different impedances. This data extraction procedure helps designers select the best impedance based on design requirements [4].

Load impedance plays a critical role in determining amplifier efficiency and power delivery. A similar technique, known as source-pull, is applied at the input side to optimize gain and input-side linearity. Despite efforts to design transistors as unilateral devices, real-world transistors exhibit bilateral behavior, meaning that changes on one side influence the other. Consequently, while load-pull primarily impacts efficiency and output power, source-pull also has an effect on these metrics, just as load-pull influences gain and linearity.

### 2.2.6 Matching Networks

To achieve optimal impedance, matching networks convert impedance from the standard 50-ohm system. Impedance matching is essential for amplifier performance, particularly in determining bandwidth. Large impedance transformations on the Smith chart typically result in narrower bandwidths. The impedance transformation ratio (ITR) plays a crucial role in this trade-off, influencing the selection of matching techniques.

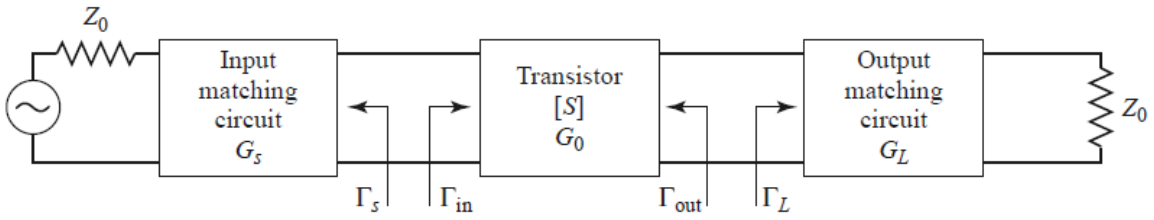



Figure 2.3: Overall block diagram of an RF power amplifier, including the input and output matching networks[4].

A fundamental approach to impedance matching involves LC-based networks, which use lumped elements such as L-section or $\pi$-section configurations. However, LC matching has limitations, particularly at microwave frequencies, due to parasitics introduced by traces and connectors. High-Q inductors are often required but may be impractical due to size constraints and physical limitations [4].

To address these issues, transmission lines can replace lumped components in stub tuning, where open- or short-circuited stubs adjust impedance. A common technique involves converting LC matching networks into their transmission line equivalents using Richards' transformation and Kuroda identities. Another widely used approach is the quarter-wave transformer, which employs a 90-degree transmission line to invert impedance. However, quarter-wave transformers are inherently narrowband, and high ITR values further restrict bandwidth.

To mitigate these limitations, multi-section quarter-wave transformers introduce a gradual impedance transition, improving bandwidth performance. However, they can only match real impedances, requiring additional transmission lines to convert complex impedances beforehand. An alternative technique, multi-section impedance matching with stepped impedance transformers, offers greater flexibility than quarter-wave transformers, as it does not rely on fixed-length sections, allowing for more adaptable impedance transformations.

### 2.2.7 Stability

Since the amplifiers are active devices there is the threat of the PAs being unstable devices due to the reflections and the feedback. Depending on the source and load reflection coefficients, $\Gamma_S$ and $\Gamma_L$, the device might be overblown with oscillation causing stability issues. Stability is a metric that is frequency dependent; therefore, the amplifier might be potentially unstable at some of the frequencies. The oscillations are particularly prevalent

at low frequencies, which is generally the cause of potential instability in most amplifiers. If an amplifier is stable at all frequencies it is referred to as unconditionally stable. A common test for stability is $K - \Delta$ test, the following conditions must be met to achieve unconditional stability [4]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1, \tag{2.16}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1. \tag{2.17}$$

### 2.2.8 Biasing

Transistors must be supplied with appropriate voltage levels according to their class of operation. To ensure stable biasing, these voltage supplies should be protected using RF chokes. Ideally, inductors can serve this purpose; however, similar to the challenges faced in LC-based impedance matching, inductors are often impractical in RF circuits due to parasitic effects and size constraints. Instead, transmission lines can be used to achieve the necessary choking behavior. When sufficiently narrow transmission lines are employed, they provide a stable connection to the voltage source while effectively blocking RF signals.

For proper biasing, the gate bias should be applied before the stability network, whereas the drain bias should be connected just after the transistor output. Additionally, DC-blocking capacitors should be placed in series with the matching networks to ensure that RF signals remain isolated from the DC biasing networks.

Furthermore, decoupling capacitors of varying values should be incorporated into both the gate and drain biasing networks. These capacitors help suppress voltage ripples, ensuring stable operation and reducing unwanted noise from the power supply.

### 2.2.9 Multi-Stage Power Amplifiers

Sometimes a single stage alone cannot deliver the required power for an application. In those cases, one of the solutions is to cascade more than one amplifier to get more gain. There are two options to use when designing a multi-stage power amplifier. First option is valid when good matching is achieved when designing the individual stages. If both the inputs and the outputs of each stage are perfectly matched to 50 $\Omega$, then the stages can be cascaded without much issue. In these applications, the gains of each stage can be added

for finding the total gain. The other option is to match one stage to the other, not to 50 Ω terminations. Both options have their own benefit and drawbacks.

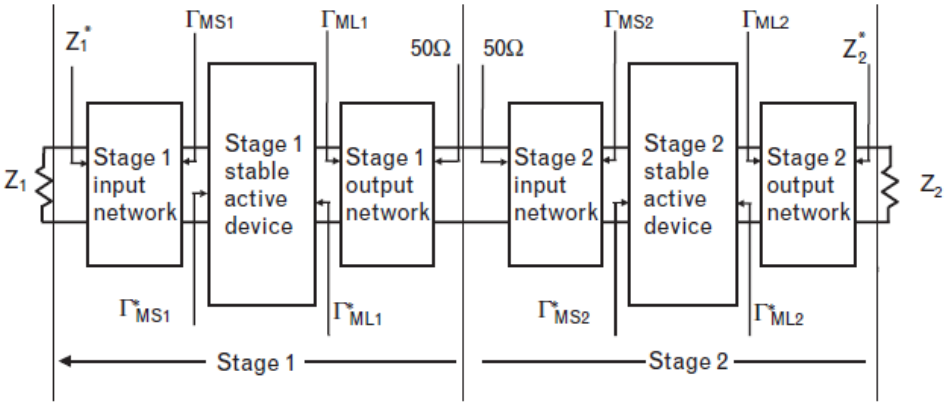



Figure 2.4: Cascading operation for two amplifiers shown with the reflection coefficients [5].

Cascading matched stages gives more predictable gain. More importantly, if the individual stages are designed to be unconditionally stable, the stability for the overall amplifier will also be ensured. Furthemore, further tuning and troubleshooting will be considerably easier compared to the direct matching method. Although this operation is easier to accomplish, the real-life amplifiers will not be perfectly matched to 50 Ω, which may result in some uncertainty [5].

If the reflection coefficients are somewhat large, then the calculated gain may not be so close to the measured gain. This uncertainty is particularly troublesome for wideband systems, as it is hard to maintain the same reflection coefficient on a wideband, which will in return affect the uncertainty. As for direct impedance matched amplifiers, albeit it will be more intricate to design the matching networks, the interstage network can be simplified compared to cascading matched amplifiers. However, in this case, tuning and troubleshooting will be harder. When this method is used, the reflection coefficient at each port must be the complex conjugate of its matched termination.

For multi-stage amplifiers, initial stages should be designed to boost the gains as high as possible. Linearity should also be sought after in these stages. However, the power amplifier itself should be implemented at the last stage which will ensure that the nonlinearities that come with it would not be amplified with additional stages.

## 2.3 Literature Review

Literature review is conducted in order to discuss the most recent issues and the solutions based around the problem statement. The review includes the recent works in the academia regarding the contemporary PA designs for mMIMO systems, the role of the PA in mMIMO architecture's and their linearizability.

### 2.3.1 PA Designs Intended for Sub-6 Transmitter Front Ends

Different topologies of PAs are reviewed and analyzed in this section which also operate in the sub-6 GHz range. [6] introduces a co-design of a PA with an antenna array which aims to minimize the effect of load-mismatch due to antenna crosstalk. The PA is a traditional single-stage class AB design that is realized with MACOM CGHV1F006, which can deliver about 6W output power, and is driven with a large driver amplifier, namely Mini-Circuits ZHL-42+. The PA is operating between 3.2-3.8 GHz and it showed a large-signal performance of about 13.5 dB small-signal gain, 55-60% PAE at peak power, 4° AM-PM at mid-power ranges. The main drawback of this design is relatively low efficiency at the back-off ranges, which is an inherent characteristic of the default PA design.

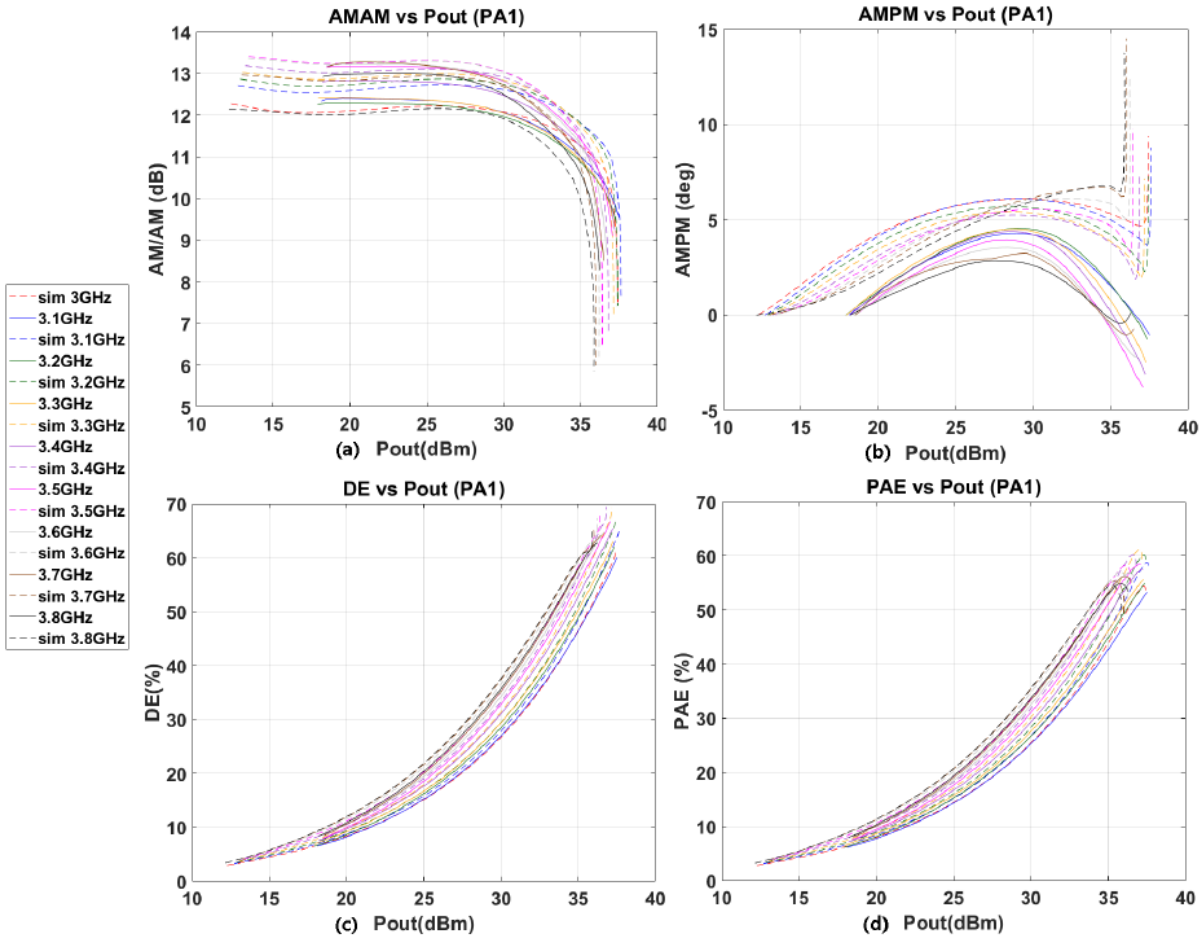



Figure 2.5: Large-signal simulation and measurement results given in [6] for one of the four manufactured PAs.

Another approach targeting the same band is presented in [29]. This study focuses on the design of a DPA, known for its characteristic improvement in back-off efficiency. In addition to the conventional Doherty architecture, the design incorporates an enhanced output combiner network that utilizes drain parasitic absorption, thereby achieving a broad bandwidth spanning 3.3–5.0 GHz. Improvements in the drain biasing network further contribute to enhanced linearity performance. For this design, MACOM CGHV1F006 transistors are employed for both the carrier and peaking PAs. Compared to the Class AB design discussed earlier, this DPA achieves lower gain, ranging between 7.8 dB and 9.7 dB. At saturation, around 38 dBm output power, the drain efficiency varies from 48% to

67% across the operating bandwidth. At 6 dB output back-off, efficiency remains relatively high, between 38.6% and 45.1%.

[7] is a work that emphasizes the challenges of using a DPA structure, namely possible bandwidth limitation and a fixed back-off range of 6 dB. Load-modulated balanced amplifiers (LMBA), which are also yet another type of load-modulated PAs are also given as an example of limited back-off range, albeit having bandwidth improvements compared to DPA. The authors introduce a three-stage load-modulated PA with three PAs having different biasing conditions (PA1 is class B, PA2, and PA3 are class C) which are connected to a four-port coupler. PA1 has high impedance at low-power regions, where PA2 and PA3 are turned OFF. As input power increases, PA2 starts to conduct, modulating the impedance seen by PA1, providing the first back-off peak. As power increases, PA3 also starts to conduct, modulating the impedances of PA1 and PA2, creating the second peak efficiency. The efficiency peaks: thus the back-off range can be adjusted by changing the biasing of PA2 and PA3; therefore, with this technique, the back-off range can be adjusted post-fabrication. The large-signal measurements show that the three-stage PA operates in the 3.3-3.6 GHz range. For 3.4 GHz, 45 dBm output power is achieved, showing a peak drain efficiency of 70%. The 6-dB, 8-dB, and 10-dB OBO efficiencies are measured as 62%, 53%, and 47%, respectively. This offers a few advantages over the DPA approach aside from adjusting the efficiency peak, having 2 efficiency peaks allows the efficiency to remain high as power levels increase, giving a flatter curve. A possible issue with this design might be the sequential behavior that the PAs are working in. This sustained operation under high stress for PA1 may pose reliability challenges.

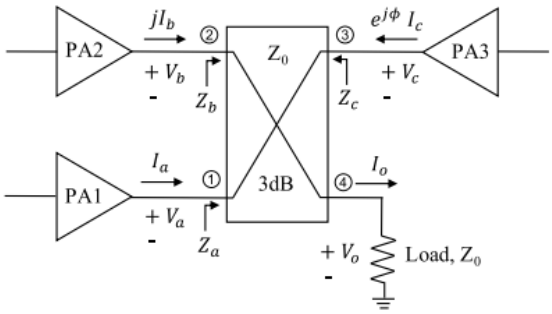



Figure 2.6: Output combiner of the three-stage load modulated PA, showing the three PAs'currents and voltages [7].

The linearity concerns in regards to AM-PM of the DPA is emphasized by [8]. They came up with a novel combiner with a quadrature coupler-based design, which resembles an

LMBA, but unlike an LMBA, and unlike [7], there is no PA connected to the isolated port of the output combiner, but the port is terminated reactively, which enables modulating the-load line behavior dynamically. The mathematical modeling they have done shows that the reactive load, can reshape the AM-PM profile, which can act against the parasitic output capacitance induced distortion. With this technique, the authors were able to limit AM-PM distortion to ±5° up to the 1-dB compression point. The bandwidth of the design is not given explicitly, but the design is centered around 3.5 GHz. It was observed that a gain around 13 dB was obtained with a PAE of 57.2%. Potential limitations may arise in large-signal bandwidth scalability due to the coupler, though not explicitly addressed.

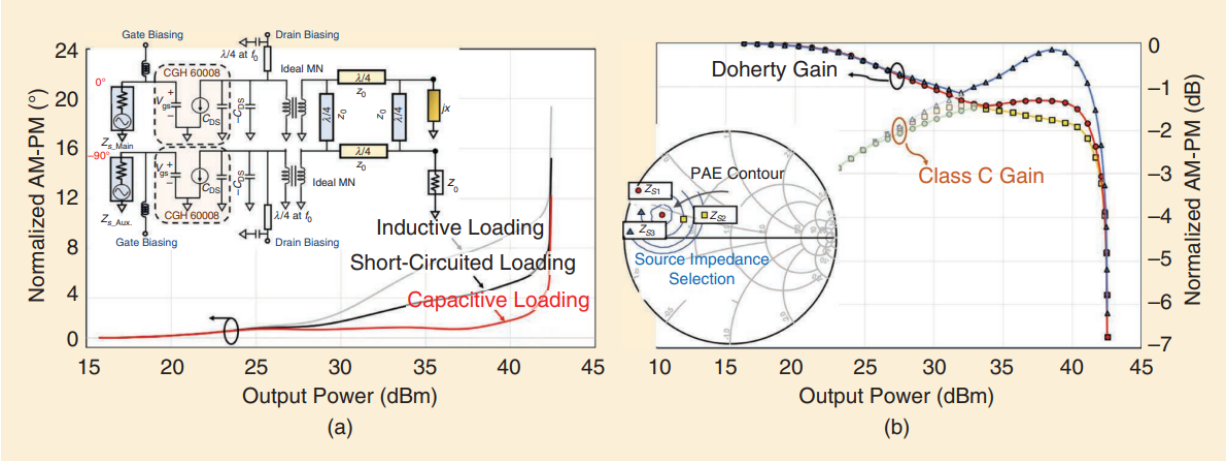



Figure 2.7: Output combiner of the three-stage load modulated PA, showing the three PAs'currents and voltages [8].

### 2.3.2 Different Transmitter Architectures and the Linearizability Efforts

[17] investigates the impact of antenna crosstalk and load mismatch on linearity in MIMO systems using a 4-channel transmitter architecture. To validate the proposed DPD architecture, the study employs Skyworks SKY66001-11 evaluation boards. The authors address these challenges through a DPD-based approach, introducing a shared Crosstalk and Mismatch Model (CTMM) along with a dual-input nonlinear DPD model for each antenna element. Their proposed structure is said to be linearly scalable with an increasing number of elements, a significant improvement over conventional approaches, which often suffer from increased complexity.

A key advancement in this work is that parameter identification is directly extracted from the PA output, unlike many prior studies. Measurements are conducted at 2.12 GHz, with the PA exhibiting an adjacent channel leakage ratio (ACLR) between -36 dBm and -40 dBm in the absence of predistortion. Applying single-input single-output (SISO) DPD results in only a 5 dB ACLR improvement, whereas multi-input DPD methods, used for comparison, achieve 10–12 dB improvements, yielding ACLR values of -50 dBm to -52 dBm. While these methods provide effective linearization, the authors highlight their computational intensity as a drawback. Instead, their dual-input CTMM DPD achieves similar ACLR performance (˜50 dBm) with lower computational resource requirements, making it a more efficient alternative.

[9] tackles the same issues discussed in the previous work using two different PA topologies, [6, 29]. The study is conducted at sub-6 GHz 5G MIMO scenario. The first topology is a class AB PA and the other is a Doherty PA that is designed with class AB biasing. The class AB practically acts more linear compared to the Doherty, whereas the Doherty PA is exceptional in increasing the back-off efficiency. Both PAs are installed on a 2x2 transmitter front end which can be observed in Figure 2.8.

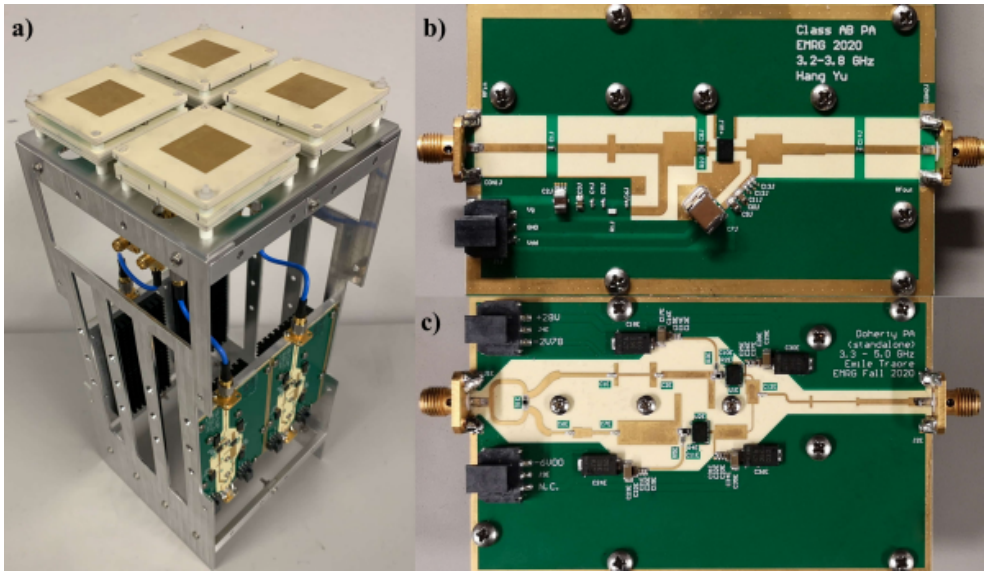



Figure 2.8: (a) Modular and scalable transmitter front-end showing antenna and PA arrays (b) Class AB PA (c) Doherty PA [9].

Two digital predistortion (DPD) techniques are employed to evaluate linearizability: single-input single-output (SISO) DPD and dual-input single-output (DISO) DPD. DISO

DPD proves to be more effective, as it accounts for antenna crosstalk during linearization. The testing is conducted using 100 MHz OFDM signals, which better reflect real-world scenarios compared to lower modulation bandwidths such as 20 MHz. Measurements are performed with antenna spacings of $0.6\lambda$, $0.7\lambda$, and $0.8\lambda$. The study finds that load mismatch has a greater impact on output power, efficiency, and linearity than crosstalk, which primarily affects linearity to a lesser extent.

Regarding the linearizability comparison between Class AB power amplifiers (PAs) and Doherty power amplifiers (DPAs), under ideal conditions without crosstalk, both PAs achieve approximately -55 dBc ACLR with SISO DPD. When antenna load effects are introduced, performance slightly degrades to -50 dBc for both amplifiers. In an mMIMO scenario, the DPA experiences greater degradation with SISO DPD: for Class AB PAs, ACLR degrades to -47 dBc, whereas for DPAs, it falls within -49 dBc to -43 dBc. However, when DISO DPD is applied, the DPA performance improves to -48 dBc, catching up to the Class AB PA. Despite these challenges, DPA's enhanced back-off efficiency surpasses that of Class AB PAs, making it a more attractive option. These findings suggest that DPA architectures, when combined with DPD, can achieve superior linearity and efficiency even in high-crosstalk environments, making them a preferable choice for mMIMO applications.

Although the 4-channel scenario gives an accurate estimate of the situation in the MIMO transmitters, having a larger array size for experimentation should give more insightful results. For that purpose, [10] can be analyzed. This study builds a 16-channel transmitter array to be used as a MIMO system in the sub 6-GHz range with an antenna spacing of $0.7\lambda$. The main priority of the study is to observe the linearization performance of different DPD techniques under an 8 dB PAPR scenario with different modulation bandwidths. As an initial take, this study highlight that the 16-channel array is relatively hard to linearize with using conventional methods such as SISO and MISO DPD because these DPD models assume fixed PA impedance, which is why they fail to full correct deterioration.

In this study, multi-stage class AB PAs are utilized which constitutes the 16 channel transistter front end. The multi-stage power amplifier has variable gain stages which allows a gain from 23 to 35.5 dB. The driver stage itself acts as a linearizer only compressing by 1.8 at a saturation of 38 dBm.

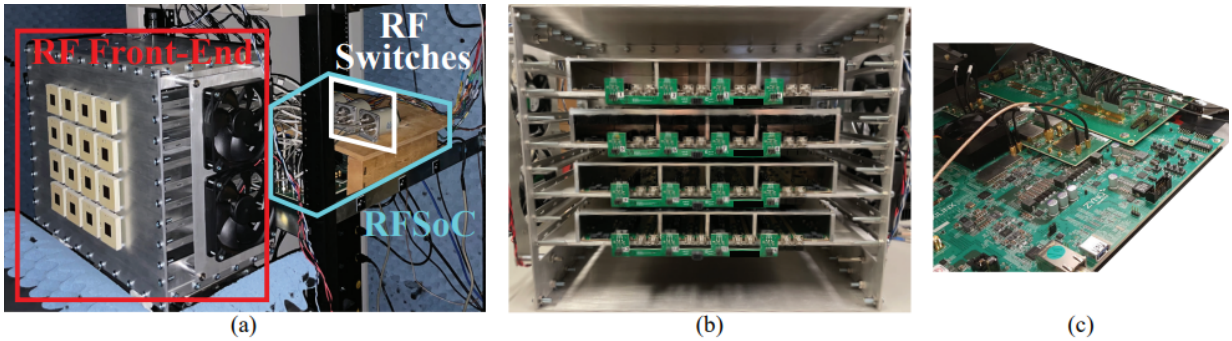



Figure 2.9: Measurement setup of the 16-chain fully-digital MIMO transmitter: (a) fully connected 16-chain transmitter front-end, (b) back view of 16-chain transmitter front-end, (c) Xilinx Ultrascale+ RFSoC ZCU216 used for 16-chain signal synthesis [10].

The study applies a digital linearization approach named Iterative Learning Control (ILC) on the 16-channel transmitter. Without linearization, the root normalized mean square error (RNMSE) reaches 28%, while the adjacent channel power ratio (ACPR) is −36 dBc, highlighting significant distortion. After ILC-based linearization, RNMSE is reduced to below 2% across all 16 chains, while ACPR improves to −54 dBc, −52 dBc, −51 dBc, and −48 dBc for 60 MHz, 80 MHz, 100 MHz, and 120 MHz bandwidths, respectively. In contrast, pruned-Volterra-based SISO and MISO DPD models perform significantly worse, with MISO DPD achieving only −46 dB ACPR and SISO DPD failing at −42 dB ACPR.

[11] gives an overview on the work that is done at HWU on active array antennas, which uses a similar architecture by deploying a 16-channel for a mMIMO transmitter, that is also intended for wireless communication at 3.5 GHz. MACOM CGHV1F006S transistors are used for both driver and the PA stage, with 20 V drain biasing and 100 mA drain current for the amplifiers. Unlike the previous work, this one has the drivers and the PA as different blocks which are linked by connectors. Although no linearity metrics are given, this work is relatable due to the fact that they emphasized the importance of coupling between adjacent channels and provide measured coupling for E-waves and H-waves. Not only those, but coupling that caused by cabling and other connectors are taken into account. This is an important factor that might also affect the linearity performance of the front-end as a whole.

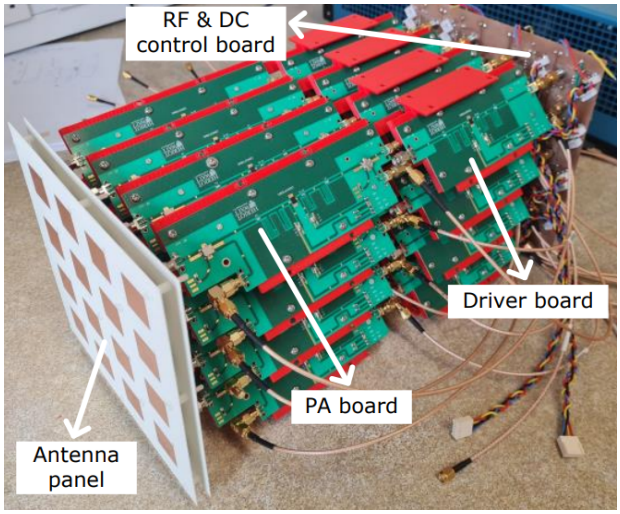



Figure 2.10: Active antenna array on display with the driver and the PA modules visible on inside the frame [11].

In contrast to these works, another approach would be to help the linearity effort by eliminating the cross-channel effect associated with the electromagnetic interference between the RF paths. Although the cited work in the literature review does not discuss this effect. Works like [12] mention the hardships caused due to this interference. They came up with a DPD algorithm that takes this into account, named Double Crosstalk Canceling (DCC) DPD. In addition to the DPD perspective, they mention that the crosstalk depends on the proximity of the PAs, how the antennas are arranged, and the overall routing of the PCB. The test set-up includes two PAs that are operating at 2.6 GHz, and two independent OFDM signals of 10 MHz modulation bandwidth and 8.3 dB PAPR are created with a vector signal generator (VNA). They generate artificial crosstalk effects by using couplers to test their algorithms. Their results indicate that their approach with DCC prevails against existing crosstalk-canceling DPD methods, particularly DCC with iterative training (DCC-IT), which has an ACPR improvement of 17.2 dB under a strong crosstalk effect.




Figure 2.11: A representation of the crosstalk between the PAs in a linear configuration [12].

### 2.3.3 Discussion and Analysis

In the context of PA design, it is observed that the reviewed works span a range from traditional approaches to increasingly complex architectures. The conventional design presented in [6] exhibits low OBO efficiency, presenting a significant challenge for accommodating the high PAPR signals characteristic of 5G systems. While the DPA approach addresses the efficiency limitations, it does so at the expense of gain and linearity—deficiencies that are subsequently corrected through DPD. However, in larger array configurations, achieving sufficient linearization through DPD alone may become increasingly difficult. More advanced architectures employing LMBA-like structures achieve substantial improvements in OBO efficiency while alleviating the inherent narrow bandwidth limitations associated with traditional designs. Nevertheless, these approaches introduce considerable design complexity and may increase susceptibility to EMI effects.

Existing works addressing transmitter architecture and PA linearizability in mMIMO systems, particularly in digital beamforming arrays, rely heavily on DPD to achieve acceptable performance. Although the importance of DPD cannot be underestimated, exclusive reliance on DPD significantly complicates the PA design, increases system nonlinearity, and results in greater power consumption by the associated hardware. Moreover, mitigating crosstalk effects should be an integral aspect of PA design, rather than an afterthought. Accordingly, the methodology proposed in the following sections aims to contribute a different perspective, emphasizing circuit-level design optimization and the management of cross-channel effects through the physical shielding of individual PAs from adjacent beamforming elements. The implementation will be carried out on a 4×4 transmitter array. Although a larger array, such as an 8×8 configuration, would yield results that are more representative of practical deployments, a 4×4 array is selected to simplify manufacturing while maintaining the focus on a traditional PA structure without load modulation enhancements.

# Chapter 3

# Multi-Stage PA Design

## 3.1 Design Requirements and Methodology

This chapter includes the intricacies of the PA design based on the background analysis. The design choices will be discussed and the reasoning for those decisions will be given backed with simulation data. This thesis will focus on solutions based on the sub-6 GHz band. This band is highly promising for 5G as it offers a balance between coverage and capacity. Additionally, since most countries have allocated this band for 5G deployment, the transition to the new generation will be both cost-efficient and seamless [30, 31].

As discussed in the previous literature review, the ultimate goal of the solution is to achieve both linearizability and efficient performance in 16-channel transmitters. Regarding linearity, the final design should target an ACPR of approximately -50 dBc with DPD in a 4×4 transmitter configuration, where crosstalk is present, and at least -52 dBc for a single-channel scenario, while also achieving a decent PAE for each PA. However, the achievable PAE is heavily dependent on the choice of transistor. For the purposes of this study, the CGHV1F006S, a MACOM transistor capable of delivering 6 W of output power, is selected for both the power and driver stages. The transistor operates within the designated 3.2–3.8 GHz frequency range and can achieve approximately 62% PAE when biased in a deep Class AB configuration. It typically operates with either a 40 V or 28 V drain bias. Regarding the substrate selection for the PCB, Rogers 4003C with a 20 mil thickness is chosen, which has a relative dielectric constant, $\epsilon_r$, of 3.55.

The data input to the chain will be supplied by the AMD Zynq™ UltraScale+™ RFSoC ZCU216 Evaluation Kit [32], which can deliver a peak output power of approximately -12 dBm. Considering that the peak output power of the PA should be 6 W, equivalent

to 37.78 dBm, an approximate total gain of 50 dB is required, not accounting for the gain compression that will occur near saturation. This gain requirement cannot be met with a single CGHV1F006S, which typically provides a gain of around 13–14 dB. While bulky driver modules capable of generating the necessary gain could be used to drive the transistor, such a solution would be impractical due to the assembly challenges that would arise within the 4×4 transmitter frame. Therefore, a custom-made driver stage is necessary.

Having concluded the requirements that the PA should achieve, the steps that are taken while designing the PA should also be discussed. Firstly, the preliminary stages and the design of the PA itself are done in Keysight Advanced Design Systems (ADS), since it is a tool that is well-proven as an industry standard and its streamlined use for PA design. However, both for cross-validation purposes and on top of that, enabling the 3D EM-simulation option for the simulation with the shielding, Ansys Electronics Design Desktop (AEDT/HFSS) is used to conclude the simulations.

The first step should be to evaluate the capabilities of CGHV1F006S to determine the ideal trade-off between drain efficiency and linearity without fault. To that end, step zero should be to extract the parasitics of the device so that the transistor can be viewed as a VCCS. This enables the designer to absorb the device parasitics into the matching networks, providing better control over circuit behavior. This step is critical before determining the class of operation, which should be the next step. Then, load-pull and source-pull simulations should be performed under the given bias conditions to identify the optimum impedances, considering linearity, gain, efficiency, and output power.

## 3.2 PA Stage

### 3.2.1 Parasitic Extraction

Knowing which reference plane is being accessed is crucial in load-pull measurements, as it directly affects impedance characterization, and; thus, the matching. Parasitics introduced by packaging create extrinsic parasitics, preventing direct access to the intrinsic drain of the transistor. Additionally, to accurately access the current source, the intrinsic capacitances of the transistor must also be removed. This step is essential for conducting load-pull analysis more effectively. Before characterizing the transistor and its properties, it is necessary to de-embed parasitics to obtain meaningful measurements. Since a packaged transistor is being used, both extrinsic and intrinsic parasitics must be accounted for and removed. Figure 3.1 illustrates the different reference planes affected by parasitics for the

drain side. The goal is gaining access to reflection coefficients seen by the current source, $\Gamma_{L0}$, when the starting point is the reflection coefficients seen by the packaged transistor, $\Gamma_{L2}$. This should also be done for the gate side.

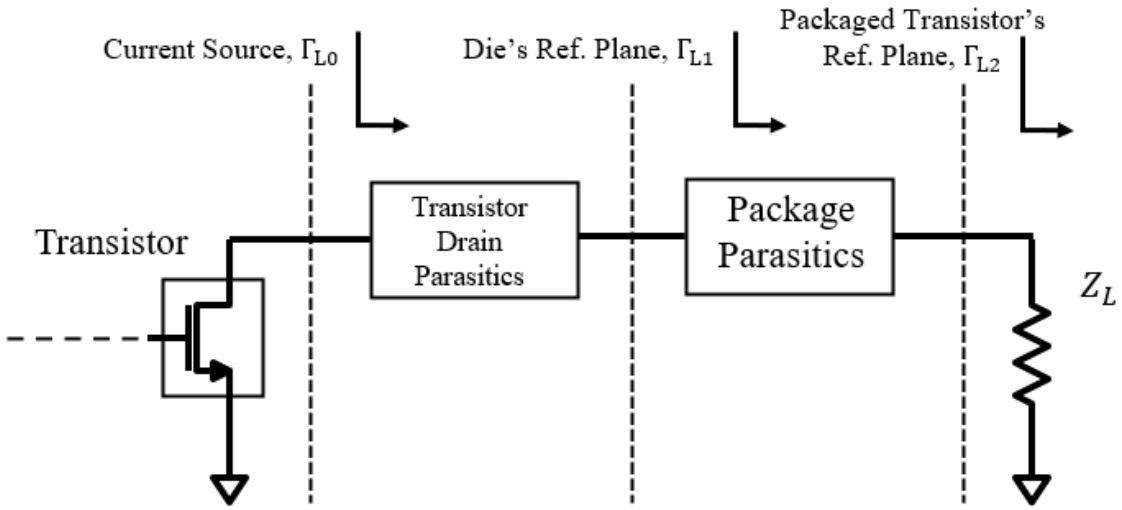



Figure 3.1: Reference planes with respect to the parasitics being involved at the drain side.

For de-embedding $C_{gs}$, $C_{ds}$, and $C_{gd}$, the method in [13] can be used. However, since the package parasitics are not removed yet, there is no access to the correct reference plane. Due to this limitation, either the package parasitics need to be extracted first or the die model of the same transistor, namely MACOM CGHV1J006D, should be used for intrinsic capacitance extraction. In either case, the die model is going to be needed in the extraction process; therefore, there is no harm in using it for intrinsic capacitance extraction. The plots in Figure 3.3 are obtained.

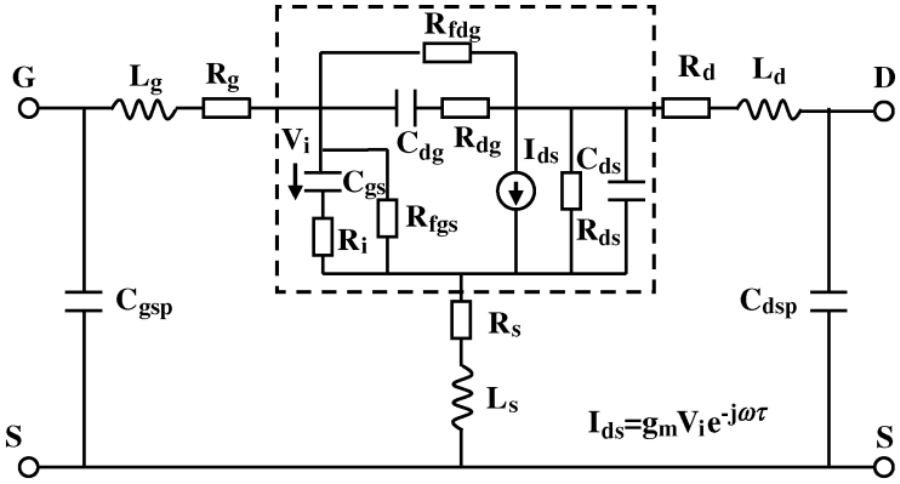



Figure 3.2: Device parasitics mapped for a transistor [13].

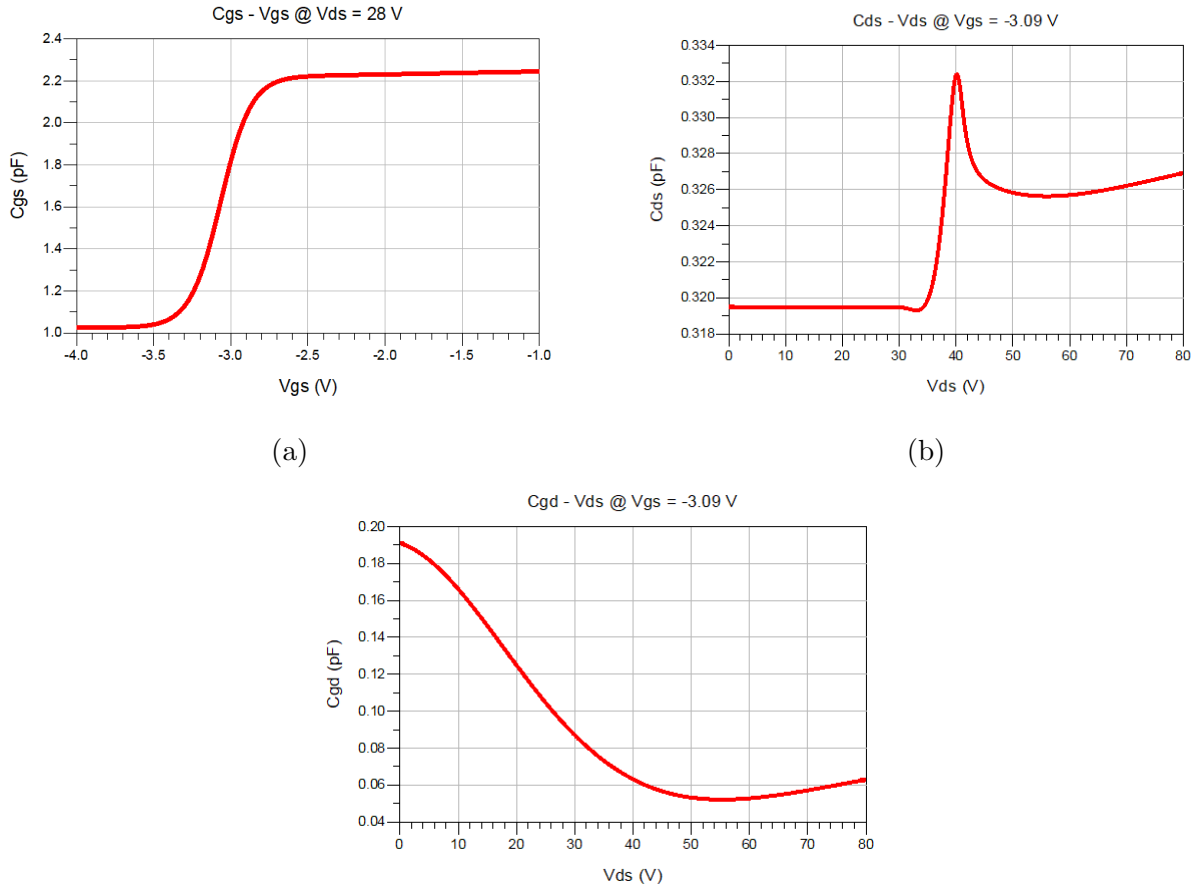



Figure 3.3: Intrinsic parasitics extracted for (a) $C_{gs}$, (b) $C_{ds}$, and, (c) $C_{gd}$.

As observed, $C_{gs}$ exhibits a steep nonlinear profile near the turn-on point of the amplifier. Additionally, since $C_{gd}$ serves as the feedback capacitance, its effective contribution to the input capacitance must be determined using Miller's theorem. Fortunately, $C_{gd}$ is relatively small and can be neglected in this context. Although $C_{gd}$ appears to undergo an abrupt jump in capacitance, the change occurs at an insignificant magnitude (on the order of digits). Further simulations indicate that this behavior is linked to the gate bias point, which is close to the transistor's turn-on voltage. At lower gate bias voltages, no abrupt jumps were observed.

The method that utilizes optimization models to extract extrinsic parasitics is signifi-

cantly more straightforward compared to the extraction of intrinsic capacitors. Similar to the previous extraction technique, this approach requires CGHV1J006D to be used in the simulation environment. The core idea is to model the extrinsic parasitics on top of the die model, effectively replicating the behavior of the packaged transistor. To achieve this, a comparative simulation of S-parameters is conducted to determine appropriate values for the modeled parasitics. Once the simulated S-parameters closely match the measured ones, the optimization process is considered complete. The optimization is performed over a frequency range from DC to 16 GHz, aligning with the transistor's operating region.

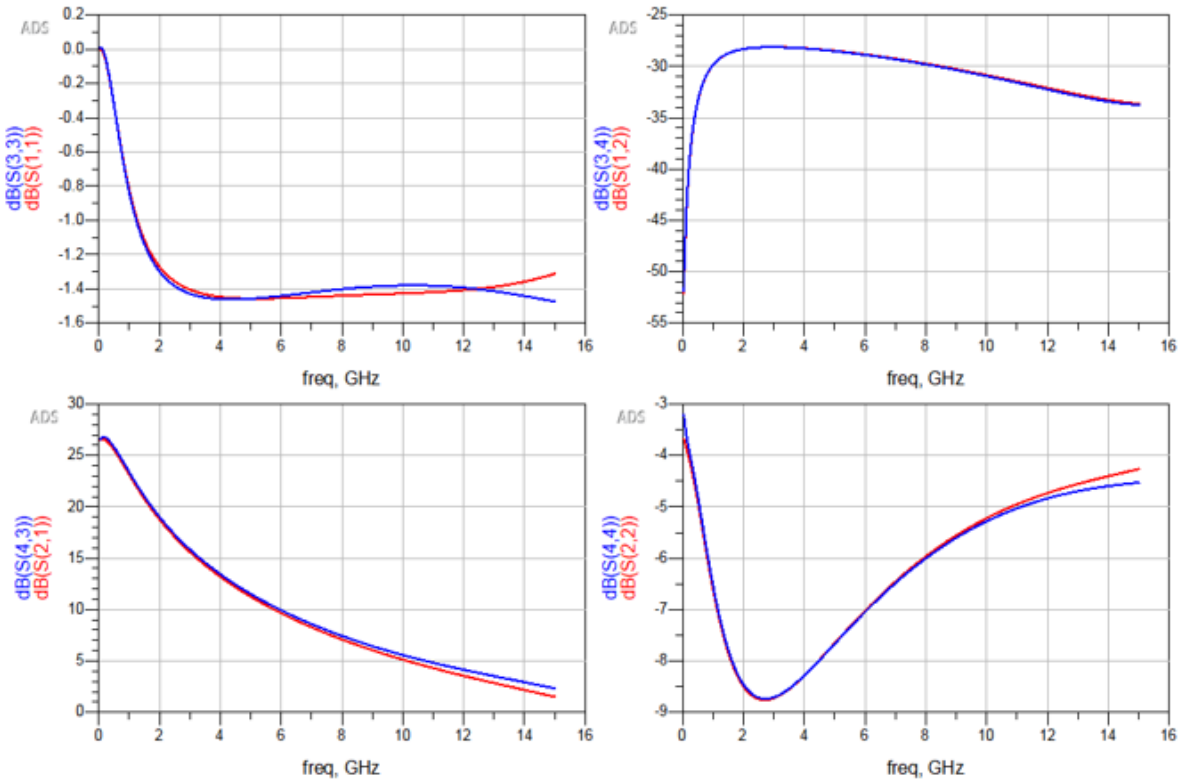



Figure 3.4: Final results for optimization ran based on the match between the S-parameters for the packaged transistor (blue) compared to the die model with added parasitics (red).

Figure 3.4 shows the results of the optimization process, and sufficient closeness was obtained for the two models, which together with the intrinsic parasitic extraction, should give access to the current source of the packaged model. A way to improve would be to do a narrower frequency sweep. Since the PA should be operating between 3.2 to 3.8 GHz range,

the optimization can be done from DC to 11.4 GHz, as an example. The explanation for this is the fact that the PA's linearity will be dominated by the third harmonic nonlinearity, and going above that range may be unnecessary in terms of computational power and time requirements. Although the matching between the frequencies above 11.4 GHz are sacrificed, this new range may give better results.

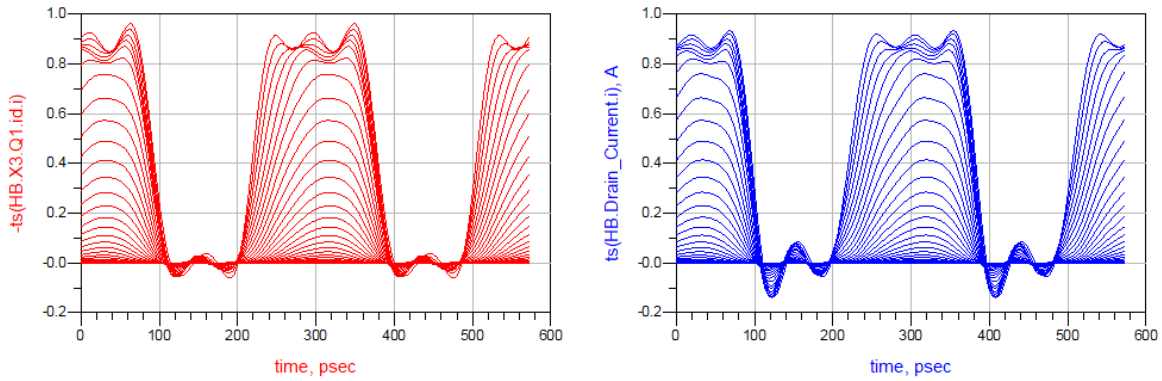



Figure 3.5: The comparison between the current flowing through the transistor with the parasitics the current source (left) and extracted (right).

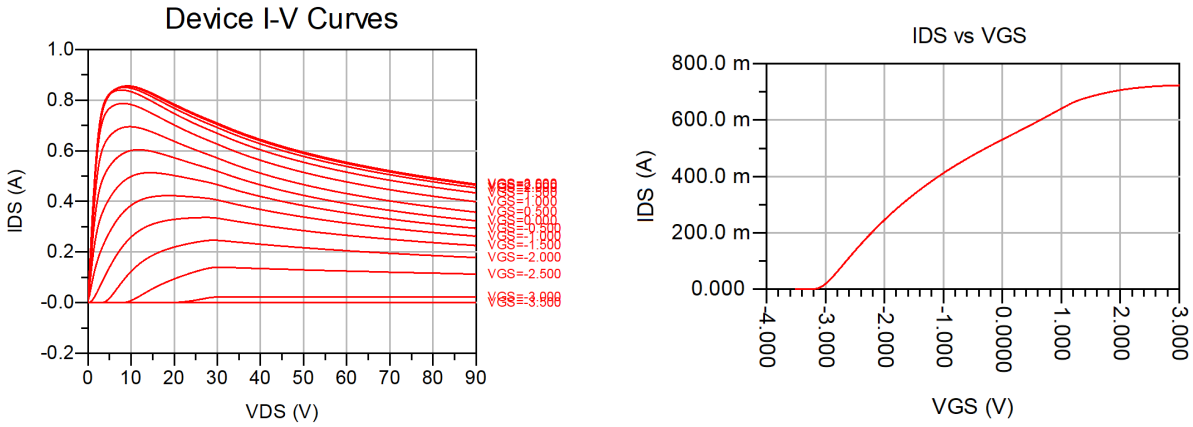
The results of the parasitic extraction can be verified by examining the drain currents shown in Figure 3.5. The device is configured in a deep Class AB mode with a 28 V drain bias and a 50 Ω load. The current source of the transistor is accessed through the ADS model of the device. For a perfect extraction, the drain current of the de-embedded transistor should match that of the current source from the model. While minor discrepancies exist, the agreement between the two currents in Figure 3.5 is sufficiently accurate for our purposes. One important observation is the clipping effect in the drain current at high input power levels. This behavior is attributed to the knee region, where the transistor exits saturation and enters the triode region. As a result, the gain decreases at these power levels, producing the characteristic shape observed in the plots.

### 3.2.2 Transistor characterization

With the transistor parasitics extracted, direct access to the current source is achieved, allowing the designer to proceed with characterization. However, it is important to note that this is a design choice—one may also choose to use the packaged model with its parasitics

for load-pull measurements. Extracting the parasitics provides additional flexibility during matching network design, as it enables more precise impedance tuning. Moreover, it allows the designer to analyze waveforms at the current source, which is crucial for understanding the implemented concepts and for debugging if needed. Fortunately, for the transistor used in this study, the manufacturer already provides access to the current source waveform. However, this is not always the case for other transistors, making parasitic extraction a valuable technique, even if the load-pull analysis is not explicitly based on the extracted model.

The first step for the characterization is to check the DC I-V curves of the transistor. These curves will be $V_{GS}$ vs $I_D$ and $V_{DS}$ vs $I_D$ when $V_{GS}$ is stepped.




(a) (b)

Figure 3.6: (a) DC-IV curves and (b) the $I_{DS}$ vs $V_{GS}$ curve when $V_{DS} = 28\,V$ for the used device.

Figure 3.6, shows the behavior for a typical GaN transistor, with the overshoot in the maximum drain current, then a decrease as the $V_{DS}$ is increased. This effect is due to the effect of thermal performance of GaN devices. As the voltage across the channel is increased, the temperature is increased as well, which in return decreases the electron mobility. Another key point for understanding this plot is the knee voltage, $V_k$, which is around 5V, a limitation in the transistor drain efficiency. This effect will not allow the theoretical maximum efficiency to be reached.

Practically, the load line method provides an important perspective into the optimal load impedance, aiding in the selection of a suitable DC drain voltage. Additionally, the

achievable impedance using microstrip lines on the chosen substrate plays a critical role in the design. If the required load impedance determined by the load line is relatively high, achieving it with microstrip lines may be challenging due to physical constraints. For example, evaluating the class A load line at a 40 V drain bias results in a required impedance around 100Ω. However, manufacturability concerns arise when these lines become excessively narrow. An alternative approach is to use a 28 V drain bias, which trades off output power for improved manufacturing reliability. To address this trade-off, the 28 V bias is adopted for both the PA and driver design.

Additionally, analyzing the transconductance curves is essential, as they provide valuable insights into nonlinearities relative to gate bias points. When selecting a class AB bias, these curves, combined with load-pull predicted efficiency results, illustrate the trade-off between efficiency and linearity, aiding in an informed design choice.

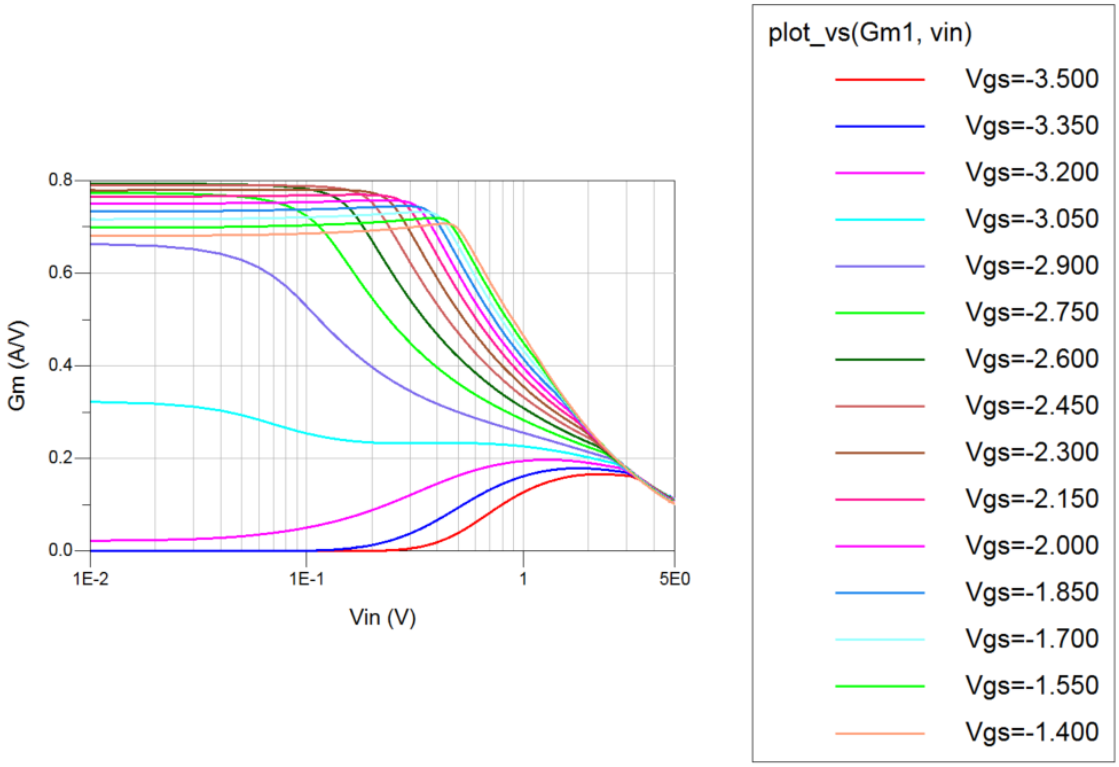



Figure 3.7: Transconductance of the transistor with different gate bias conditions swept with input voltage.

As shown in Figure 3.7, at higher gate bias voltages, current saturation occurs at lower input voltage levels. While the small-signal region exhibits linear behavior, the early drop in transconductance results in a reduced linear range due to a lower $OP_{1dB}$. Considering this, class A configuration and class AB biases with higher gate voltages appear unfavorable in terms of both linearity and efficiency, as corroborated by the efficiency calculations. In contrast, lower gate voltages around -3.05 V exhibit relatively good linearity, both in terms of small-signal gain and $OP_{1dB}$. Additionally, a deep class AB bias provides higher efficiency. However, this type of bias comes with two primary drawbacks: lower gain and variation in the small-signal gain. Given these trade-offs, adopting a deep class AB bias appears to be the most promising approach. After additional tuning the DC-operating point of the device is set as $V_{GS} = -3.09\,V$, $V_{DS} = -28\,V$, and $I_{DS} = 8\,mA$, this serves as the starting point for the design.

### 3.2.3 Stability Network

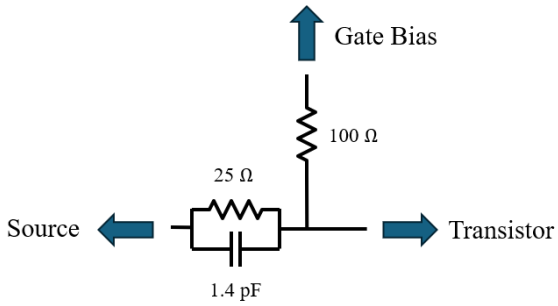



Figure 3.8: The applied stability network, without the microstrip components.

In most cases, to stabilize a power amplifier unconditionally, an additional network must be connected to the source side. This network should introduce some loss to dampen potential oscillations. Typically, it consists of a resistor and a capacitor in parallel, where the resistor provides the necessary damping and the capacitor ensures that the resistor predominantly affects low frequencies. This configuration allows the amplifier to retain a portion of its gain at higher frequencies, where the intended operation occurs. To determine appropriate values for the lumped components, it is ideal to use stability circles to observe the transistor's behavior across varying conditions. It is also possible to stabilize the transistor only to a certain degree, resulting in a potentially unstable condition. In

such cases, the amplifier would exhibit greater gain compared to an unconditionally stable configuration. However, given that the final product requires a multi-stage PA due to the total gain requirement, the risk of oscillations and instability at the individual stage level cannot be tolerated. Therefore, unconditional stability is prioritized in this design.

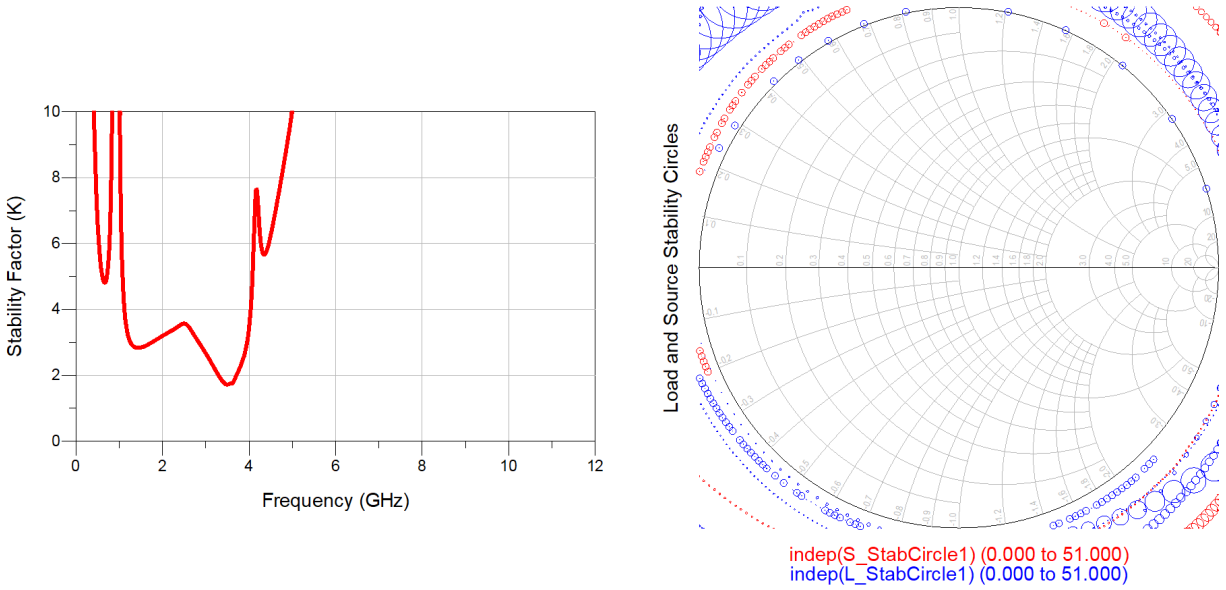



Figure 3.9: K-factor for the transistor with the used stability network (left) and the stability circles for both source (red) and load sides (blue).

### 3.2.4 Load and Source Pull

Having access to the transistor current source and with the bias point selected, load-pull can now be performed on the transistor. Since the characterization has been completed, it is expected that the contours will close around the real axis. Although the most common use of load-pull is to determine the optimum load impedance balancing output power and PAE, it also significantly affects another critical metric: the AM-AM profile and the $P_{1dB}$ point. Therefore, a more detailed load-pull test, involving input power sweeps, provides additional insight into the AM-AM behavior. Final decisions on the optimum impedance should be made in consideration of these profiles to achieve better linearity in the high-power region. The said characterization revealed that the matching should be done for the load impedance, $Z_L = 59 + j4.8\ \Omega$, as that is the point where the maximum output power is obtained and a decent PAE is also ensured.

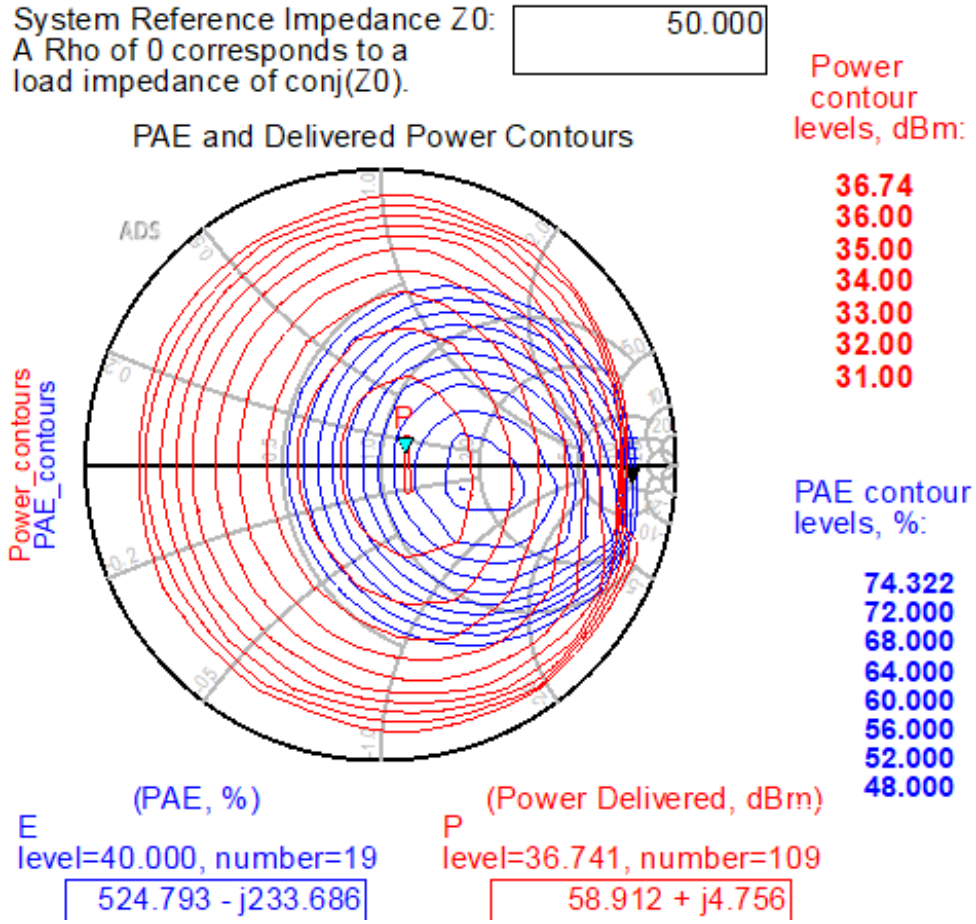



Figure 3.10: Load-pull results for the de-embedded packaged transistor with the deep class AB bias and 30 dBm peak input power.

Typically, for the source side, an option is to match the impedance to 50 Ω, which will allow maximum power transfer from the source and minimize the reflections, which will be significant considering that the front-end module needs cascade multiple stages and having inner reflections may cause oscillations or deteriorate the overall performance. However, 50 Ω matching does not necessarily mean that the maximum gain will be achieved for the source side. For that, source pull gives valuable insight, along with the contours that show the maximum AM-PM distortion value (not normalized) for a specific curve. That way, the compromise between the two can be evaluated more justly. Although, a strict 50 Ω match is not necessary, an $S_{11}$ of at least -10 dB is desired for minimizing the input

reflections. This means that the selected source impedance, $Z_s$, should be close to the center of the Smith Chart. Considering the gain requirements, and the AM-PM profiles that are observed with the power sweep that is done for the source side, a rough estimate of the impedance to be matched is selected as $Z_s = 30 + j16\ \Omega$.

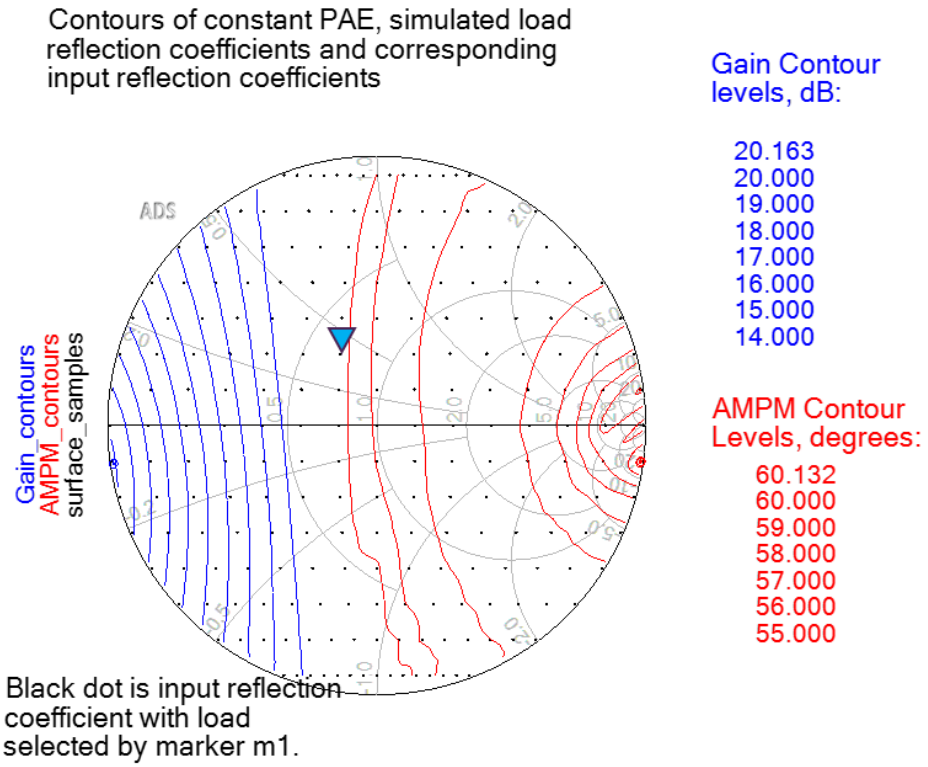



Figure 3.11: Source-pull results for the de-embedded packaged transistor with the deep class AB bias and 30 dBm peak input power.

### 3.2.5 Matching Network Design

According to the results of the load-pull, a matching network made of a stepped impedance transformer can be used. The reason for this choice is to achieve the 600 MHz bandwidth required for the design while also saving vertical space compared to the alternative approach of using stub-matching.

The matching networks do not solely consist of stepped impedance transformers; other components affect the matching as well. The DC-block capacitance, the bias lines, and even

the smallest bypass capacitors have a significant impact on the overall matching. However, these components can be designed so that their effects are minimized. For example, if a sufficiently large DC-block capacitor is used, the high-frequency matching will not be significantly affected. For the bias lines, the situation is more intricate. If a bias line with a length of $\lambda/2$ is selected, the bias lines will have negligible influence on the matching, along with the bypass capacitors. Although fully nullifying these effects could simplify the matching process, keeping them adjustable provides the designer with additional degrees of freedom for optimization, which is the approach adopted for this project.

The matching for the output matching network (OMN) is completed first, using the Smith Chart tool in ADS, starting with a two-section design. However, using only two sections did not provide sufficient matching across the entire band, so a three-section matching network was implemented, yielding better results. The bias lines were also tuned to achieve improved matching, with 47 pF capacitors acting as DC-blocks. The bias line widths were minimally adjusted to maintain their RF-choking functionality, resulting in a final width of approximately 0.5 mm. The input matching network (IMN) was designed in a similar manner, using a three-section stepped impedance technique.

After the initial simulations were conducted in ADS, the design was exported to HFSS for 3D EM simulation. A slight frequency shift of approximately 150 MHz toward higher frequencies was observed in the S-parameter results. Since all subsequent simulations were to be performed in HFSS, the results obtained from HFSS were prioritized. To compensate for the frequency shift and preserve the original behavior observed in ADS, the matching networks were slightly reduced in size.

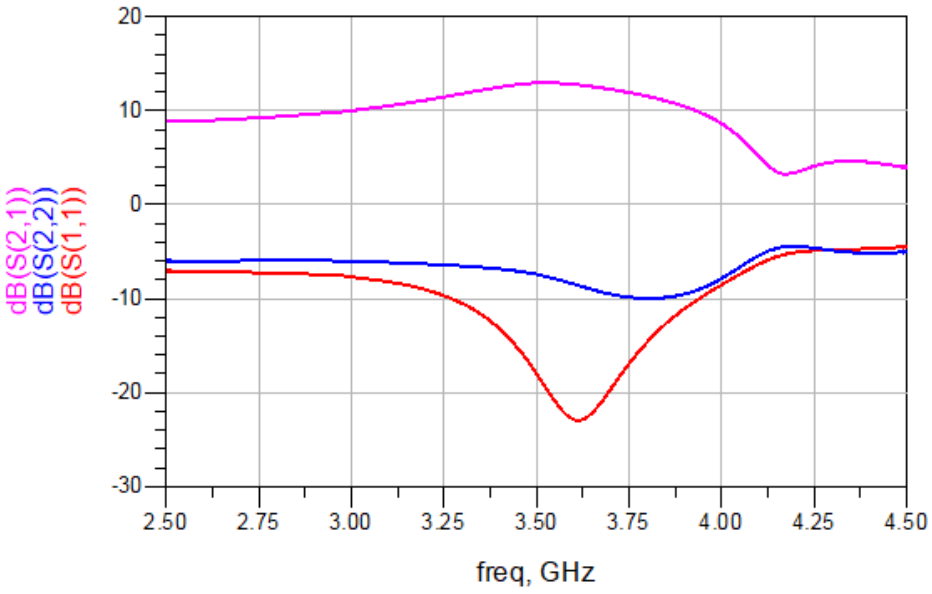



Figure 3.12: S-parameter simulation results for the PA, showing the $S_{11}$, $S_{22}$ and, $S_{21}$.

From Figure 3.12, it can be observed that within the band, the input return loss is aimed to be at least 10 dB; and for that of the output, it is at least 5 dB. For the output matching, although it is important to have a relatively high return loss, the primary objective is to match for output power and PAE; considering these metrics having a return loss of about 5 dB is fair.

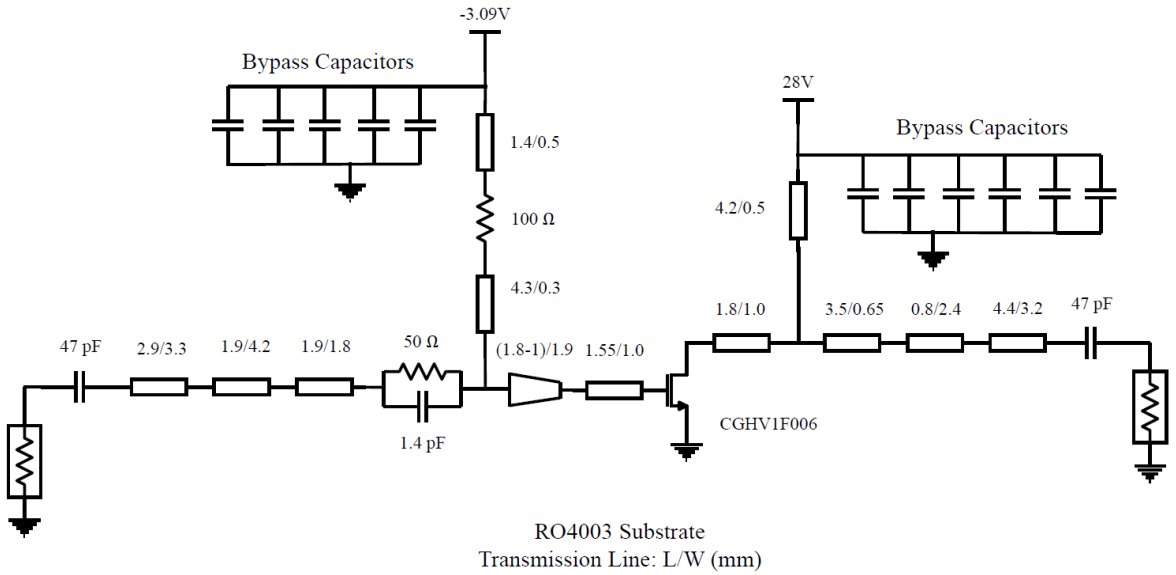



Figure 3.13: The schematic view for the PA, showing the dimensions or values of the component in the matching networks.

### 3.2.6 Biasing and Video Bandwidth Analysis

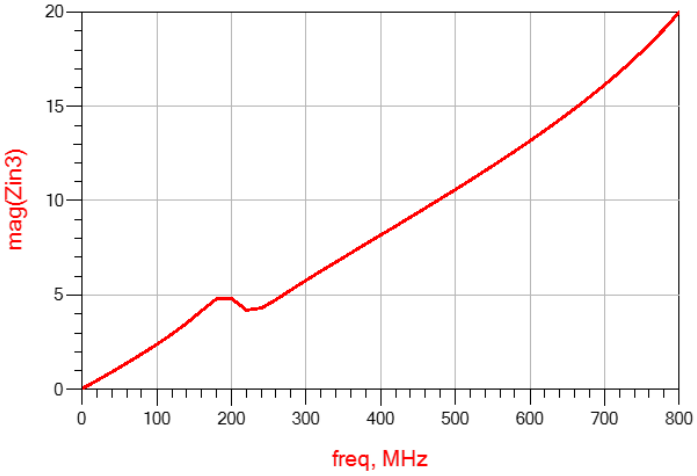
This design is also intended to be extendable to a balanced amplifier, which has proven to be a strong choice for load resiliency applications in PAs. Therefore, the bias lines are arranged in a curved manner so that two symmetric amplifiers can fit on the same board. The bent structure also provides space for the protection circuitry to be placed inside the nest that is formed. Aside from clearing possible ripples in the supply voltage, the decoupling capacitors also provide a short circuit to ground for RF signals. In most cases, the second-smallest capacitor is sufficiently small to completely short the RF signals, meaning that after this capacitor, the matching is no longer influenced by the bias traces.

The length of the bias lines before the capacitors has a significant impact not only on matching but also on the linearity of the amplifier under modulated signals. The resistance introduced by the bias line may become large if the line is excessively long or narrow. Considering a two-tone signal with frequencies $f_1$ and $f_2$ to approximate a modulated signal, the even-order product $|f_1 - f_2|$ corresponds to the large-signal bandwidth of the design. However, unlike the large-signal band, these modulation products are located in the megahertz range, which in this particular case is 600 MHz. This type of bandwidth

is referred to as the video bandwidth. The IMD component manifests at the drain as a current, and if the impedance seen at the drain at low frequencies is comparable to the RF impedance, a drain voltage modulation effect will occur at these low frequencies. This, in turn, will effectively alter the stable DC biasing of the design, resulting in memory effects. The drain modulation effect is outlined in equation 3.1:

$$V_{ds}(t) = I_{ds}(t)Z_L, \tag{3.1}$$

where $V_{ds}(t)$ is the voltage modulation at DC frequencies, $I_{ds}$ is the current induced by the interferer and $Z_L$ is the seen impedance at DC frequencies. Therefore, the bias line at the drain side cannot be arbitrarily long or narrow, as it must fulfill the requirements of an RF choke. Its dimensions must be carefully selected to effectively suppress RF frequencies while avoiding excessive low-frequency impedance at the drain. The impedance seen by the drain within the video bandwidth, along with the drain voltage modulation under varying input power levels, is presented in Figure 3.14. The impedance provides important clues about the video bandwidth; if the impedance values rise to a level comparable to the impedance at the fundamental frequency, it may pose an issue. Furthermore, since DPD will be employed at later stages, the video bandwidth criteria become even more stringent. DPD algorithms typically use a sampling rate five times the modulated bandwidth, and the video bandwidth should follow this trend. It can be observed that the drain voltage bias remains unaffected.




(a)

f = 100 MHz

| Pavs | Drain_Modulation |
|---|---|
| 15.000 | 0.008 / 39.615 |
| 18.333 | 0.011 / 41.284 |
| 21.667 | 0.015 / 52.979 |
| 25.000 | 0.017 / 52.267 |

f = 200 MHz

| Pavs | Drain_Modulation |
|---|---|
| 15.000 | 0.031 / -89.114 |
| 18.333 | 0.044 / -94.025 |
| 21.667 | 0.051 / -104.808 |
| 25.000 | 0.082 / -121.702 |

(b)

Figure 3.14: (a) The impedance seen by the drain side at the video bandwidth and the (b) drain voltage modulation calculated with equation 3.1.

### 3.2.7 Large-Signal Simulations

Harmonic balance simulations are done from 3.2 to 3.8 GHz from -20 dBm to 30 dBm input power, whose results can be observed in Figure 3.15. As it is also understood from the transconductance curves, the deep class-AB bias shows variation starting around 15 dBm. The $OP_{1dB}$ point is around, 36.5 dB, which gives a decent linear range for nearly full power utilization. The PAE is at maximum power ranges from 54 to 61%. This is the premise of the deep class-AB bias, achieving higher efficiency compared to higher gate biasing options. The results indicate a gain dispersion of around 2 dB. Although the AM-PM profile shows an undesirable nonlinear profile, due to the phase distortion at mid-power ranges, it does not pose a significant threat to linearizability as the distortion is low, only around 2°.

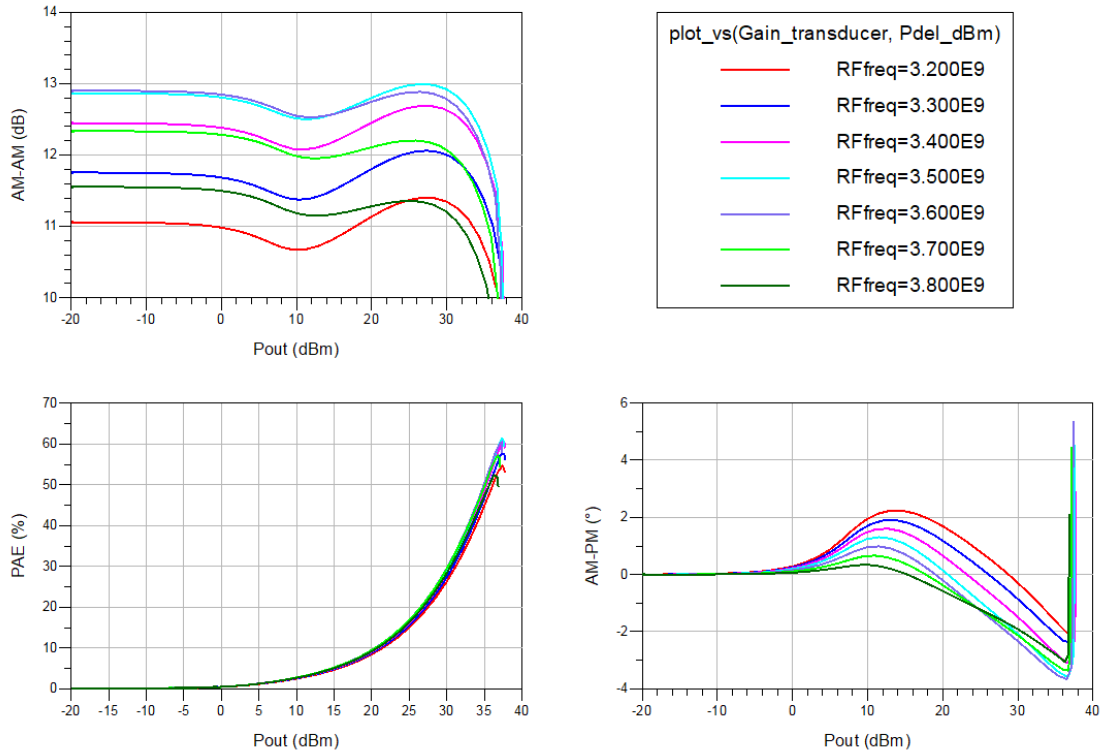



Figure 3.15: The large signal simulation results for the PA, including AM-AM, AM-PM, and PAE.

### 3.2.8 Modulated Signal Simulations

Modulated signal tests were conducted using MATLAB-based mathematical modeling. Using an OFDM signal with 100 MHz bandwidth at 3.5 GHz, 2001 subcarriers, and 8 dB PAPR, the design achieved an ACPR of approximately -35.80/-34.93 dBc without DPD. When SISO DPD was applied to the PA, the ACPR improved significantly to -54.46/-55.0 dBc. The effects of spectral regrowth were effectively eliminated, as shown in Figure 3.16. The AM-AM and AM-PM plots exhibit signs of memory effects, which are primarily attributed to thermal variations. As the device temperature changes, key parameters such as gain and threshold voltage shift, resulting in dispersed data points in the plots. Insufficient video bandwidth can further exacerbate this issue, as it affects the biasing conditions of the device.

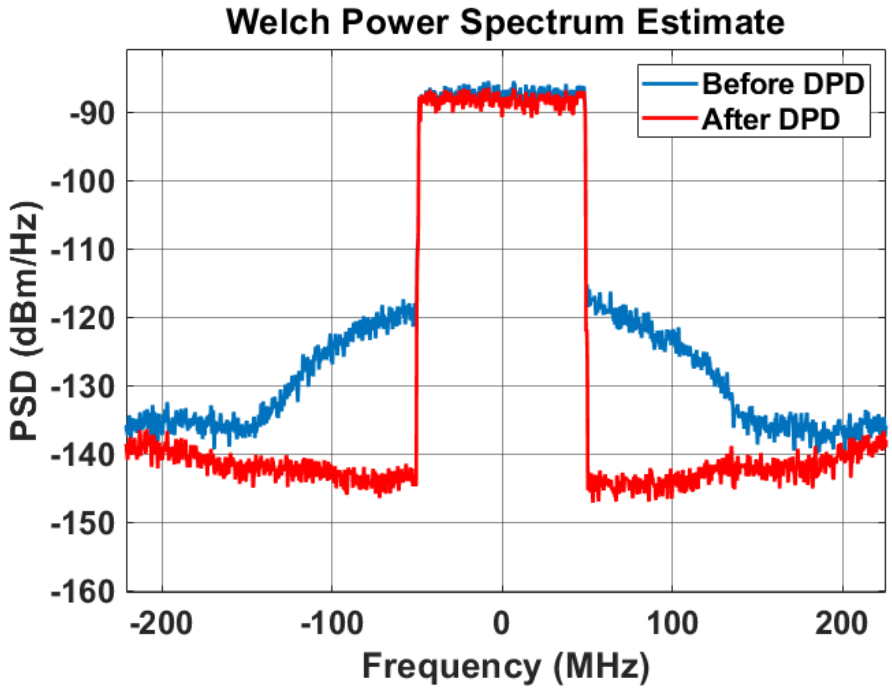



Figure 3.16: The power spectral density plots of the output of the PA without DPD, and with DPD.

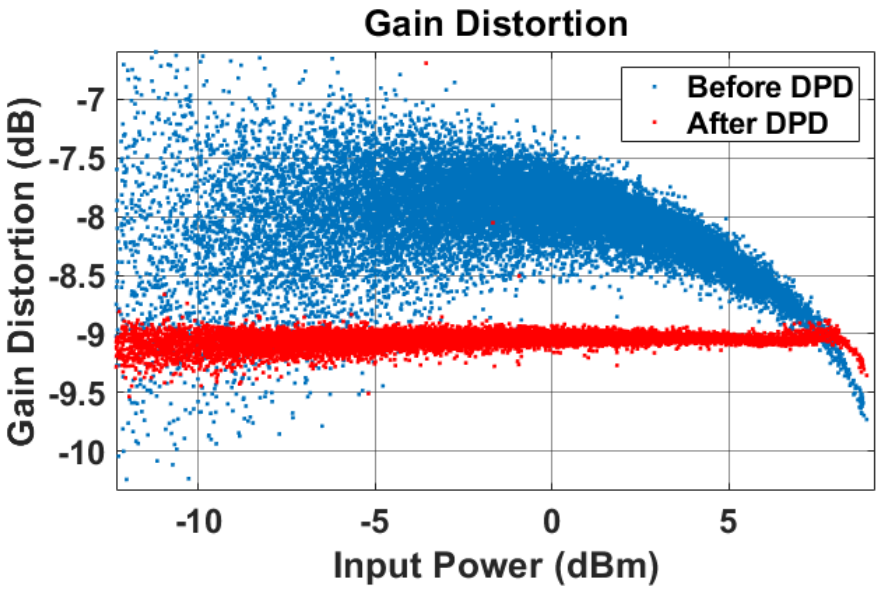



Figure 3.17: The AM-AM plots under 100 MHz modulated bandwidth for the output of the PA without DPD, and with DPD.

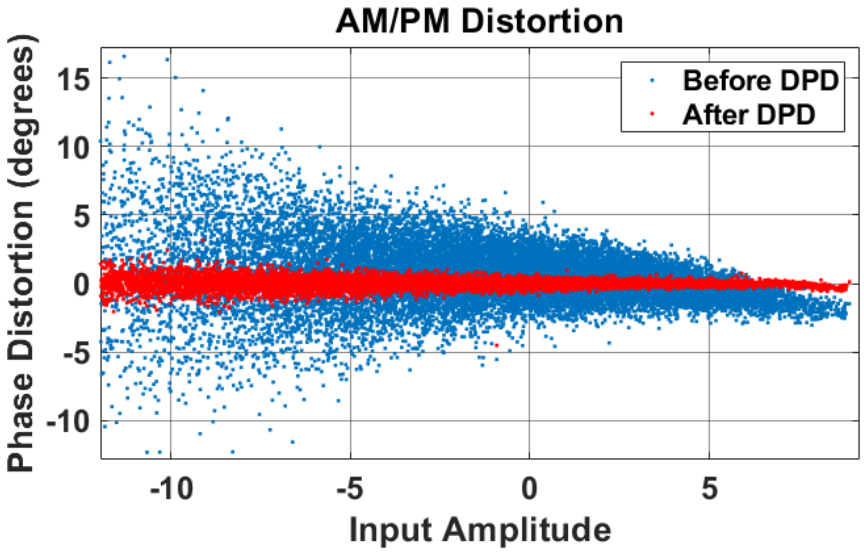



Figure 3.18: The AM-PM plots 100 MHz modulated bandwidth for the output of the PA without DPD, and with DPD.

## 3.3 Driver Stage

The PA is guaranteed to deliver around 36.5 dBm output power, when the input power is significantly high already, around 30 dBm range. However, having such a high input power from the source is not realistic, as the evaluation board [32] that will be used for providing the input signal will have a maximum output power of -12 dBm. Therefore, the input power should be increased so that the input to the PA itself should be high enough to achieve the output power goal. Thus, additional stage or stages should be added to deliver that power. Later, it will be shown that three stages will be needed for this purpose, consisting of the pre-driver, driver, and the PA stage. The PA stage is already covered, a similar analysis is also done for the driver stage.

### 3.3.1 Bias, Stability, and Matching

It was already established that the class of operation plays a determining role in the efficiency and the linearity trade-off. The PA stage is biased in deep class-AB so high efficiency would be achieved while retaining decent linearity. For the driver, the main concern should be linearity, not efficiency; therefore, a bias that is close to class A would give the best results. Not only that but also due to having three-stages will some extra gain, which means that the driver itself does not necessarily be used in full power utilization. Instead, the driver can be used in a way that it does not need to go to the saturation region; thus, not showing increased nonlinearity, which would affect the PA stage adversely. The linear behavior of the higher biasing can be seen in Figure 3.7, which should give little to no small-signal gain variation.

Since three stages are going to be used on the entire chain, the gain requirement on the driver stage is not that critical, which gives some flexibility from the designer's perspective. Specifically, this allows using a direct matching technique that is highlighted in the background section. Therefore the main aim of the matching is to have a high return loss for the input and output. The other essential concern is the gain dispersion, which is important because it will affect the dispersiveness of the PA stage as well. In the case that the gain is too dispersed, the modulated bandwidth may suffer from nonlinearities.

Since the same transistor is being used with the PA, the stability network does not need to be redesigned. The same network is used considering this. Likewise, as for the matching, the same three-section transformer topology is used for the driver stage. This is due to the three-section stepped transformer has proven capable of handling decent gain dispersion and large-signal bandwidth. The dimensions of the transformer are selected so

that the matching to 50Ω would be achieved initially. However, further tuning was done to reduce gain dispersion was done both at the input and output side.

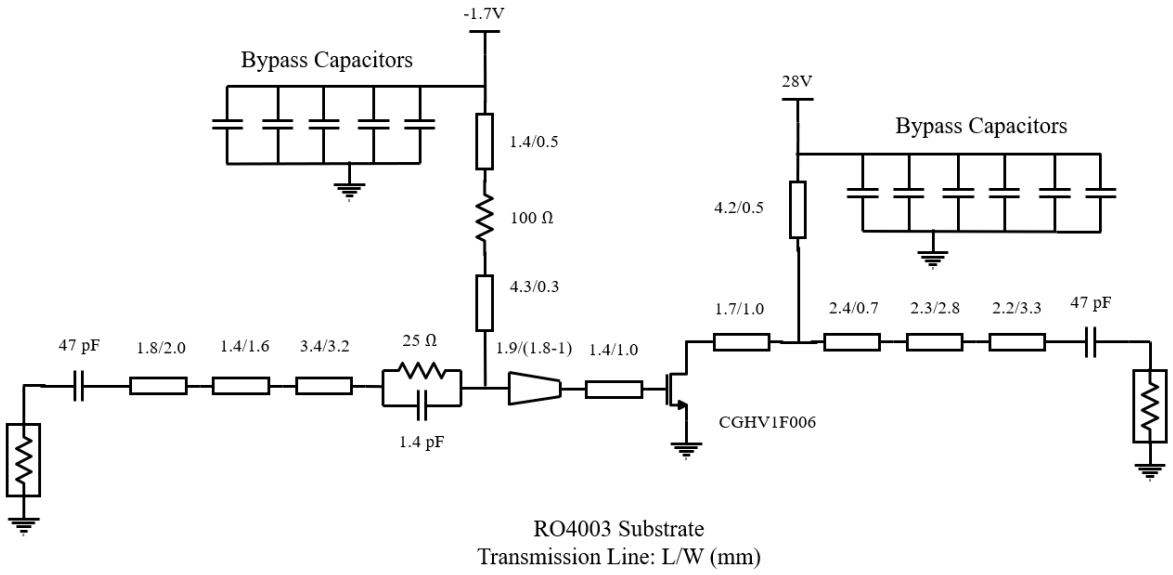



Figure 3.19: The schematic view for the driver amplifier, showing the dimensions or values of the component in the matching networks.

### 3.3.2 Large-Signal Simulations

Large-signal simulations for the driver stage were conducted using the harmonic balance simulator in ADS over the designated 3.2–3.8 GHz frequency band. The results, presented in Figure 3.20, illustrate the typical behavior of class A and high-class AB bias operation. The AM-AM profile exhibits no small-signal gain variation, with a low gain dispersion of approximately 1 dB. At higher power levels, a noticeable increase in AM-AM distortion occurs, followed by the onset of saturation. However, since the transistor is being used as a driver rather than operating at full power, this gain compression is not a significant concern. A similar trend is observed in the AM-PM profile. Up to 25 dBm output power, minimal phase variation is observed, which is a crucial characteristic. Given that the PA itself exhibits nonlinearity in this region, limiting additional phase distortion from the driver is essential to prevent further degradation of the output phase.

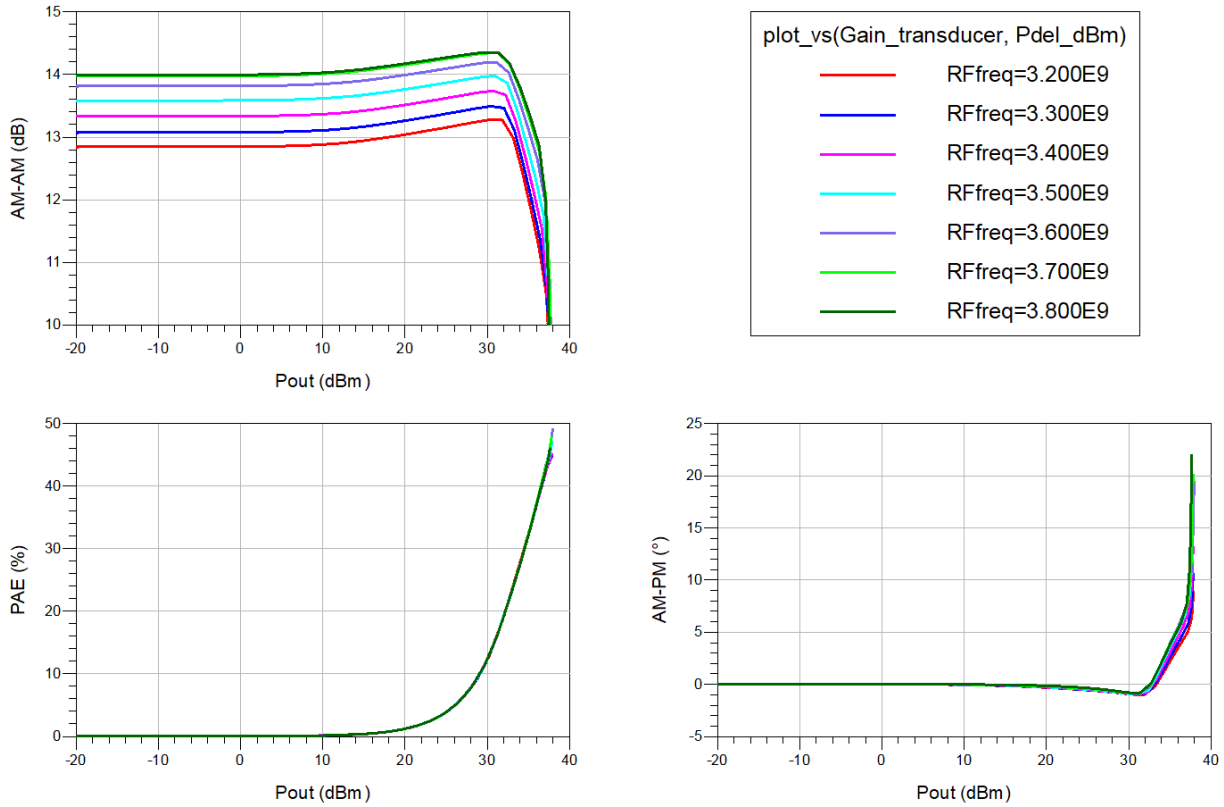



Figure 3.20: The large signal simulation results for the driver amplifier, including AM-AM, AM-PM, and PAE.

A layout comprised of the driver amplifier and the PA is drawn. The direct matching method, which is discussed in the background section, is used. Its effect can be seen in Figure 3.21. The small signal gain is the sum of the gains of the individual stages. It can be seen that the AM-PM performance deteriorates with cascading the two stages. A distortion around -6° is seen at the high power region. This can also be anticipated if Figures 3.15 and 3.20 are compared. The driver is not being used in full power utilization, which means that the distortion caused by the driver is about -2°. Then, the PA itself contributes to the distortion with -4°.

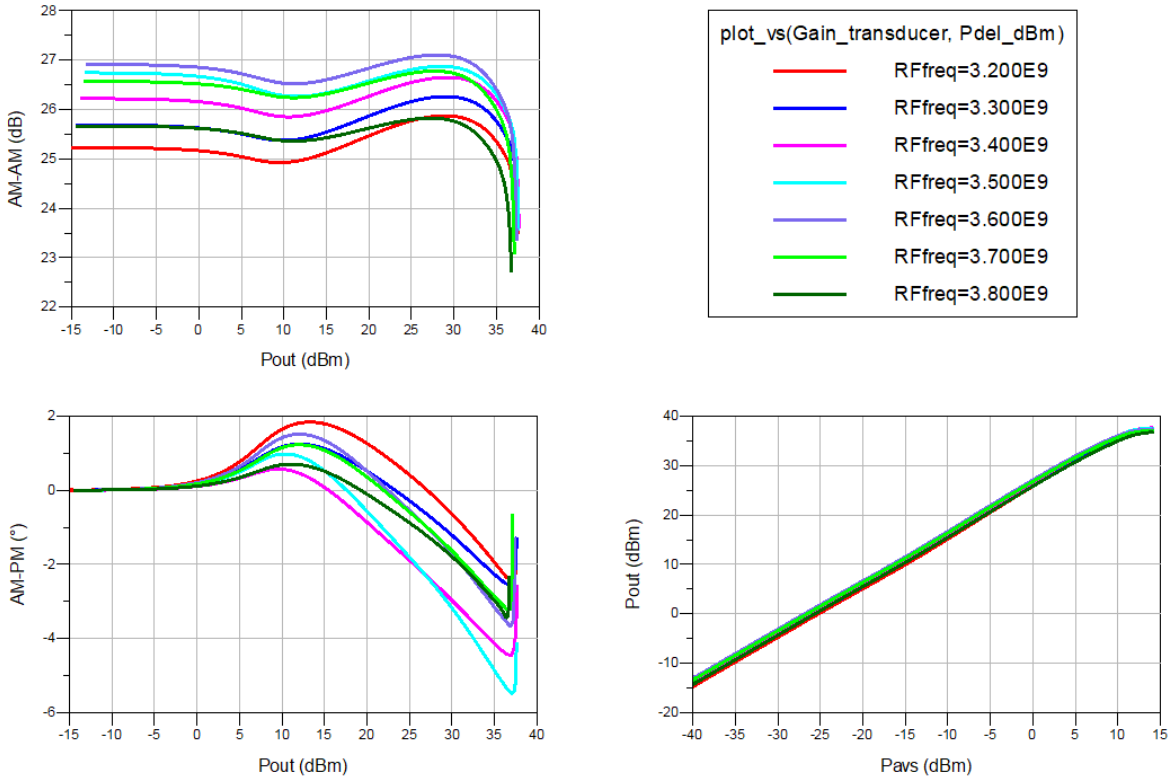



Figure 3.21: The large signal simulation results for the two stages combined, including AM-AM, AM-PM, and power sweep.

## 3.4 Extension to Multi-Stage Power Amplifier and to the One-Channel Module

### 3.4.1 Multi-Stage Amplifier

The input power to the front end is -12 dBm at peak, as this is the maximum output that the evaluation board can deliver. Therefore, although a driver stage is already implemented, an additional pre-driver stage is also required. The two-stage PA achieves a total gain of approximately 25 dB. Considering the output power requirements, the output of the pre-driver stage should be around 11 dBm, implying that the required gain from the pre-driver should be approximately 23 dB. For this purpose, the pre-driver lineup

proposed in [10] is adopted, which can deliver the necessary power to the driver. The pre-driver lineup consists of the QPA9127, HMC1122, and QPA9842 [33, 34, 35]. Each stage of the lineup must achieve a certain $OP_{1dB}$ to ensure that the power delivered to the PA remains as linear as possible. The first component in the lineup, the QPA9127—a gain block amplifier—provides a relatively constant gain of around 20 dB with a $OP_{1dB}$ of 19.5 dBm. The next component, the HMC1122, is a variable attenuator offering an attenuation range from -0.5 dB to -31.5 dB. Typically, to achieve a maximum output power of approximately 36.5 dBm, the attenuator should be set to around -15.5 dB. However, for the manufactured one-channel unit, this setting may require adjustment, as performance variations could arise. The final component, the QPA9842, has a gain of approximately 19.5 dB, which, combined with the set attenuation value, results in an output power of about 12 dBm—well below its $OP_{1dB}$ of 25 dBm. The full pre-driver lineup is shown in Figure 3.22.

The components in the pre-driver chain require different supply voltages to operate. To meet these requirements, low-dropout regulators (LDOs) are used in the pre-driver circuit. Additionally, a coupler is placed after the output of the PA, allowing a coupled signal to be extracted for DPD implementation. The chips selected for the pre-driver do not require matching. Between the pre-driver and driver stages, an intentional separation of approximately 5 mm is left to accommodate the inner wall of the shielding structure. This gap is sufficient, given the wall thickness of 2 mm. These layout considerations are illustrated in the 3D view of the design shown in Figure 3.23.

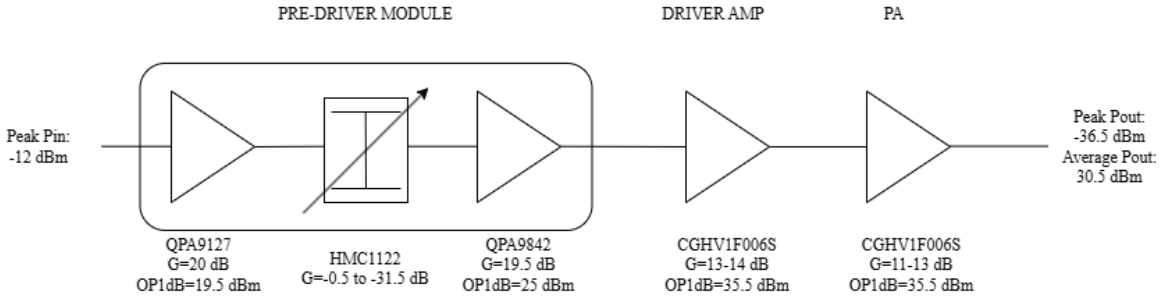



Figure 3.22: The line-up for the multi-stage amplifier showing the gain and the 1-dB compression points for each link.

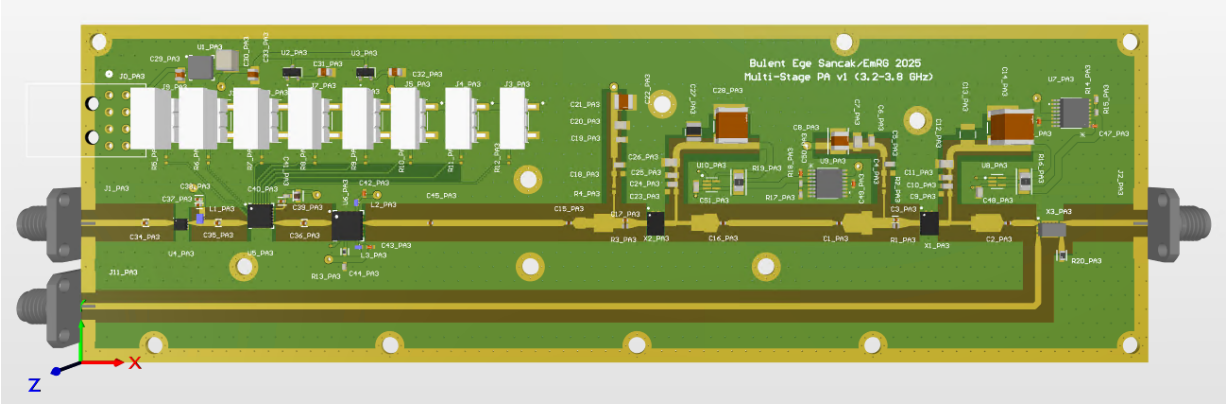



Figure 3.23: 3D-view of the multi-stage amplifier.

Current protection circuits are placed within the nests formed by the curved bias lines for both the driver and the PA stage. These circuits consist of the IC LT3012BEFE, an LDO with inherent current protection capabilities, and the INA280, a current sense amplifier. The LDO is configured such that currents exceeding 800 mA cause the drain voltage to drop, effectively turning OFF the multi-stage PA.

### 3.4.2 Simulation Results for the Multi-Channel Amplifier

The multi-stage topology is tested under large-signal simulations as well. Harmonic balance simulations are done with a power sweep from -60 dBm to -12 dBm. The results show that there is minimal change in gain dispersion and $OP_{1dB}$ performance in the AM-AM curves, while the necessary gain is supplied, which was discussed in the prelude of this chapter. AM-PM curves also show the same performance that was observed for the two-stage simulations, the pre-driver itself did not have a significant contribution to the phase distortion.

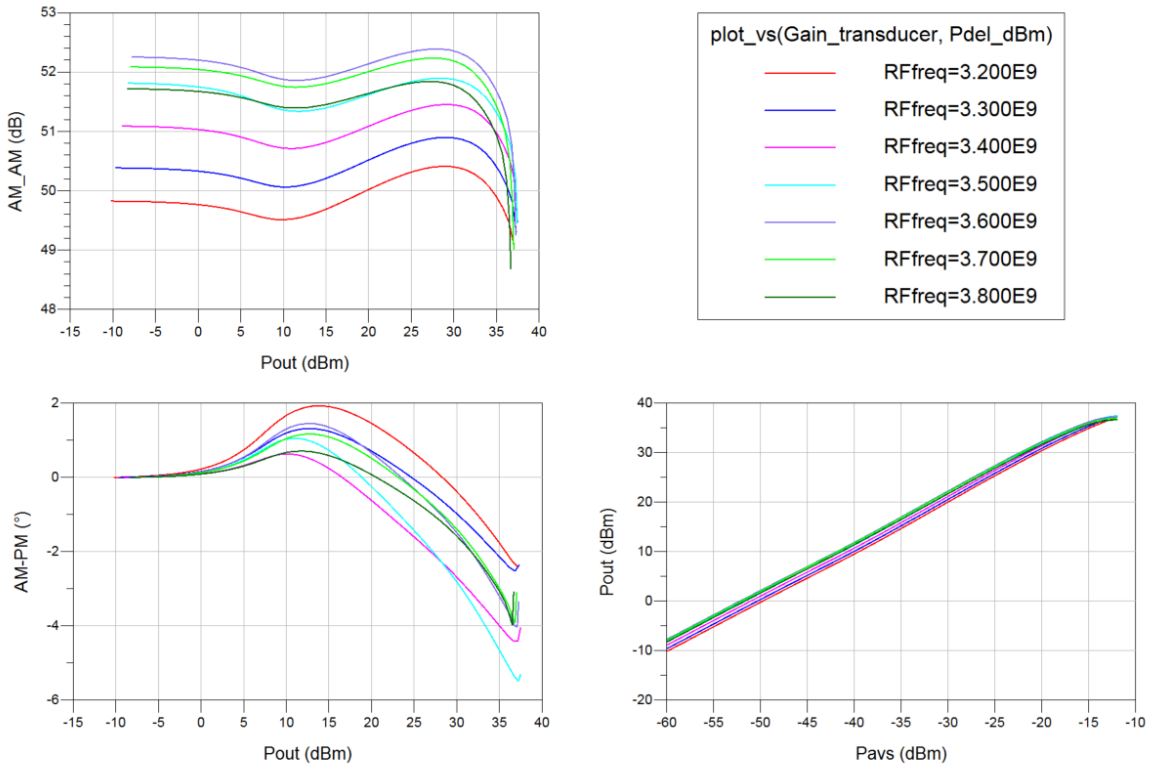



Figure 3.24: The large signal simulation results for the multi-stage power amplifier, including AM-AM, AM-PM, and Pout.

## 3.5 Comparison with the Class AB PAs in the Literature

Table 3.1 is given below to provide a comparison of Class AB PAs in the literature. The PA-stage from this work is used for the comparison. The list includes sub-6 GHz PAs designed using GaN transistors. Aside from the PA proposed in this thesis, which provides simulation data, the reported values are obtained from measurements.

| **Metric** | **This work**[a] | [6] | [36] | [37] | [38] |
|---|---|---|---|---|---|
| Frequency (GHz) | 3.2–3.8 | 3.2–3.8 | 2.3–2.7 | 3.3–3.6 | 3–3.5 |
| $P_{\text{sat}}$ (dBm) | 37–38 | 36–38 | 39.8–46.5 | 38.2–38.7 | 40[c] |
| OP1dB (dBm) | 36.5 | 33[c] | 35-38[c] | 35[c] | NA |
| PAE (%) | 54–61 | 51–61 | 52–59 | 40–45 | 40–73[c] |
| Gain (dB) | 11–13 | 11.7–14 | 12–15 | 17–17.2 | 13–15[c] |
| ACPR (dBc) | -35[b] | -33[b] | NA | NA | NA |
| Transistor | CGHV1F006 | CGHV1F006 | CGH40010F | QPDI009 | CGH40006P |

[a] Simulation data [b] 100 MHz modulated signal, 8 dB PAPR [c] Estimated from the plots

Table 3.1: Comparison of class AB power amplifiers in the literature.

# Chapter 4

# Enclosure Theory and Design

## 4.1 Effect of Electromagnetic Waves on Circuits

### 4.1.1 Electromagnetic Interference

Although the microstrip lines and the other passive components on the PCB are intended to carry the RF waves on the board itself, some of the waves will be emitted out of these components, as the microstrips will act as antennas. These waves may be received by other lines or passives on the circuit. This effect is called EMI, and in this particular case, it is caused by the components on the same board. Depending on the severity of the EMI, the system under its influence can show different types of hazards, including immune operation, performance degradation, operation suspension, and physical damage. For this application, since the main source of the EMI is the PA itself, the power levels are not high enough to physically harm or suspend the operation of the boards. However, they can cause significant performance degradation [39]. This performance degradation is highly dependent on the type of circuit being implemented, meaning RF circuits will have different responses to EMI compared to digital circuits. In particular, the individual PCBs on the tray may exhibit cross-channel coupling between each other, and the multi-stage PA may experience coupling between its stages, as mentioned in the previous section.

### 4.1.2 Shielding as a Measure Against EMI

Devices and systems require precautionary measures to minimize the EMI they cause while ensuring that the performance of the device is not significantly affected. This is

referred to as electromagnetic compatibility and is a critical consideration in the design of high-frequency circuits. One of the most direct approaches to addressing this issue is the implementation of metallic shielding. The shield can be designed either to prevent EM radiation from a source from interfering with other electronic devices or to protect a system from incoming EMI. The design of the shielding must be handled carefully; factors such as the size, material, thickness, and distance to the shielded device are crucial. Additionally, if the size of the shield is not properly selected, the shielding cavity may act as a resonator at the frequency of operation, thereby negating the intended protective effect due to self-resonance. Typically, the enclosure is electrically connected to ground.

### Shielding Effectiveness

A common method to evaluate the effectiveness of shielding was proposed by S.A. Schelkunoff, which treats the enclosure as part of a circuit modeled as a transmission line connected to a source and terminated by a load. In this model, voltage and current are replaced by $E$ and $H$ fields. Schelkunoff proposed three figures of merit to measure the effectiveness of the shield: reflection loss, absorption loss, and multiple reflections loss. Together, these components constitute the total effectiveness of the shield as a single metric, expressed as [40]:

$$S = A + R + B \quad dB. \tag{4.1}$$

where $A$ is the absorption loss, $R$ is the reflection loss and $B$ is the correction factor if multiple reflections are presumed to happen inside the shield wall.

The absorption loss indicates the shield's capability to attenuate the incoming waves as they pass through the medium of the shield which happens because the material itself absorbs the energy of the said waves. Through a series of equation in [40], the simplified version is given as:

$$A = 8.69 \left(\frac{t}{\delta}\right) \text{ dB}. \tag{4.2}$$

where $t$ is the material thickness and $\delta$ is the skin depth of the material, the property which indicates that the depth at which electromagnetic waves penetrate before their amplitude diminishes to approximately 37% of its initial surface value. For an aluminum shield, which will be preferred over copper due to its weight, the skin depth at 3.5 GHz is 1.41 $\mu m$. Due to manufacturability limitations, and considering the mechanical stability

of the shield, a 1 mm thickness is applied to the wall. This results in an absorption loss of 6163 dB, which is ample considering the frequency of operation. This absorption alone should give sufficient effectiveness to the shield at cutting out the cross-channel-related issues for RF frequencies.

The reflection loss, as the name suggests, is how much the incoming waves are reflected by the shield, instead of penetrating the shield and its being energy absorbed by the shield. If the wavelength is comparable to the skin depth, the waves might travel along the thickness of the shield and might be reflected from the inner walls of the shield, which constitutes the correction factor. However, if the shield thickness is greater than 1 skin depth, then this factor can be ignored, and the net reflection can taken as $R$, which is the case for the 1 mm shield. Reflection loss can be calculated for both far-field and near-field depending on the distance. If the distance between the source is less than $\lambda/(2\pi)$, then near-field equations apply. For this case, since the source of EMI is taken as the PAs themselves, THE distance is larger than that; thus far-field calculation should be used. Therefore, $R$ can be calculated for the far-field as the following, imitating the reflection on a transmission line:

$$R = 20 \log \frac{94.25}{|Z_s|} \text{ dB}, \tag{4.3}$$

where $Z_S$ is the impedance of aluminum. It can be calculated with using:

$$Z_2 = \frac{1+j}{\sigma\delta}, \tag{4.4}$$

where $\sigma$ is the electrical conductivity for aluminum and $\delta$ is the skin depth.

If the calculations are carried out, $R = 69 \quad dB$, which again gives decent far-field reflection performance for the shield on top of the incredibly high absorption loss. The key takeaway in these calculations is that since the used frequency is high, the PAs can be easily shielded from interfering with one another due to radiated RF waves. The main concern in this regard will be the mechanical manufacturability and the system integration.

### 4.1.3 Overall Shielding Design

The shield is designed to encapsulate the entirety of the one-channel PCB, a decision made in order to capture all possible stray fields into the ground. The shield must be grounded as well, otherwise, it will act as an antenna which will be another problem instead of a

solution. The shield will also dissipate heat together with the metal base that will be connected to the exposed bottom layer of the PCB. Since there are three stages, the shield is divided into three rooms: for the pre-driver, for the driver, and for the PA itself. The walls between the stages are 2 mm thick and have openings so that the traces that start from the input to the output in a straight line can pass. This structure should effectively minimize the inter-stage coupling.




Figure 4.1: A bird-eye view for the flipped shield, showing the rooms that are intended for each stage.

The pins of the SMA connectors soldered to the main trace can cause electromagnetic radiation. This radiation can be particularly problematic on the output side, where the power levels are significant and are likely to affect the linearity of the entire chain. Therefore, the shield is designed so that the referenced pin of the SMA connector is encapsulated inside the shield itself, with the connector secured to the shield using the top two holes on the flange. The lower two holes are used to screw the SMA connector to the metal base, which is primarily intended for heat dissipation.

A common practice in microwave filters involves inserting screws into the filter from multiple sides to introduce different modes depending on the screw positions. However, for this application, such flexibility could become a disadvantage, as the goal is to have the shield exert minimal influence on the RF properties of the PA. Thus, the screw ends must not be exposed inside the shielded rooms. The solution implemented involves adding a patch-like structure to the interior side of the shield wall where it interfaces with the SMA connectors. This patch, with a thickness of 3 mm, conceals the screw ends and prevents RF leakage. The realization of this structure can be observed in the section analysis of the input side of the PA shown in Figure 4.2.

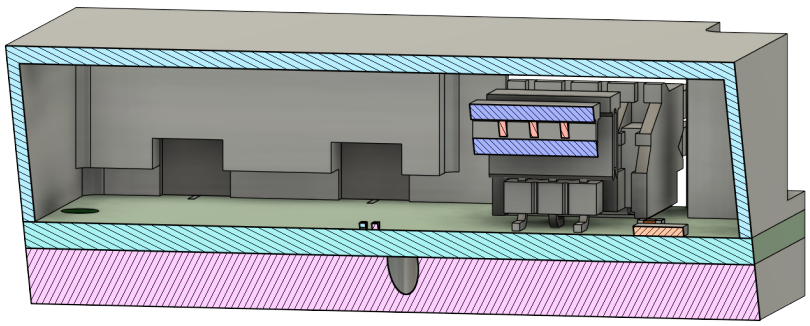


Figure 4.2: The vertical cross-section of the shielding for the multi-stage PA, showing the interior structure that encloses the screws that are used to connect the SMA connector to the shield itself.

The shield is also designed to safely cover the DC connector. However, unlike the SMA connectors, the DC connector does not have a flange-like structure that would enable secure concealment from the outside environment. This may pose an issue, as there is a possibility of EMI generated by the DC connector affecting the PA. Therefore, the DC connector will be fully covered with insulating tape to mitigate potential EMI effects. A full view of the shielded PA along with the metal base is shown in Figure 4.3, which provides further intuition regarding the described procedure.

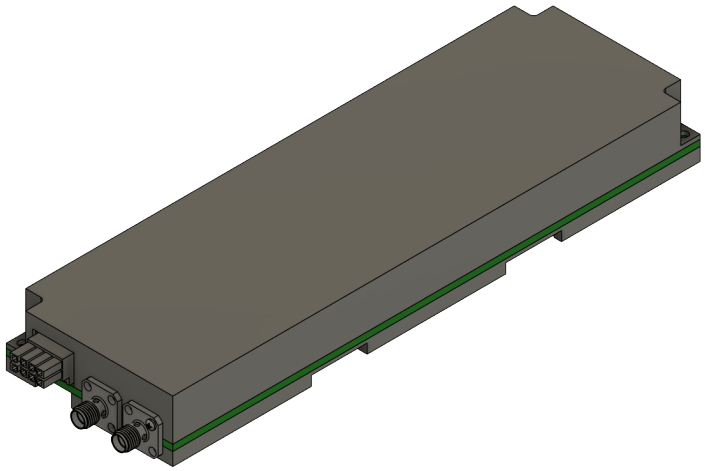


Figure 4.3: The trimetric view of the multi-stage power amplifier enclosed with the 3-room shield.

### 4.1.4 Shielded Simulations

The shielding that was designed for the multi-stage amplifier on Fusion 360 was exported to the EDS for 3D-EM simulations, and attached to the board itself. The simulation results were exported to ADS as an SnP file so that the large-signal tests could be carried out. These simulations, whose results can be viewed in Figure 4.4, showed that there were no significant changes from the original simulation results that were obtained with the bare board itself. The dispersion of the AM-AM is changed very little, which can be seen if the behavior of 3.3 GHz curves is compared. PAE and AM-PM were not affected by the design of the shield. The unchanged RF behavior of the multi-stage amplifier is essentially what is desired from the shield point of view, which is to provide sufficient absorption and reflection without causing any performance issues.

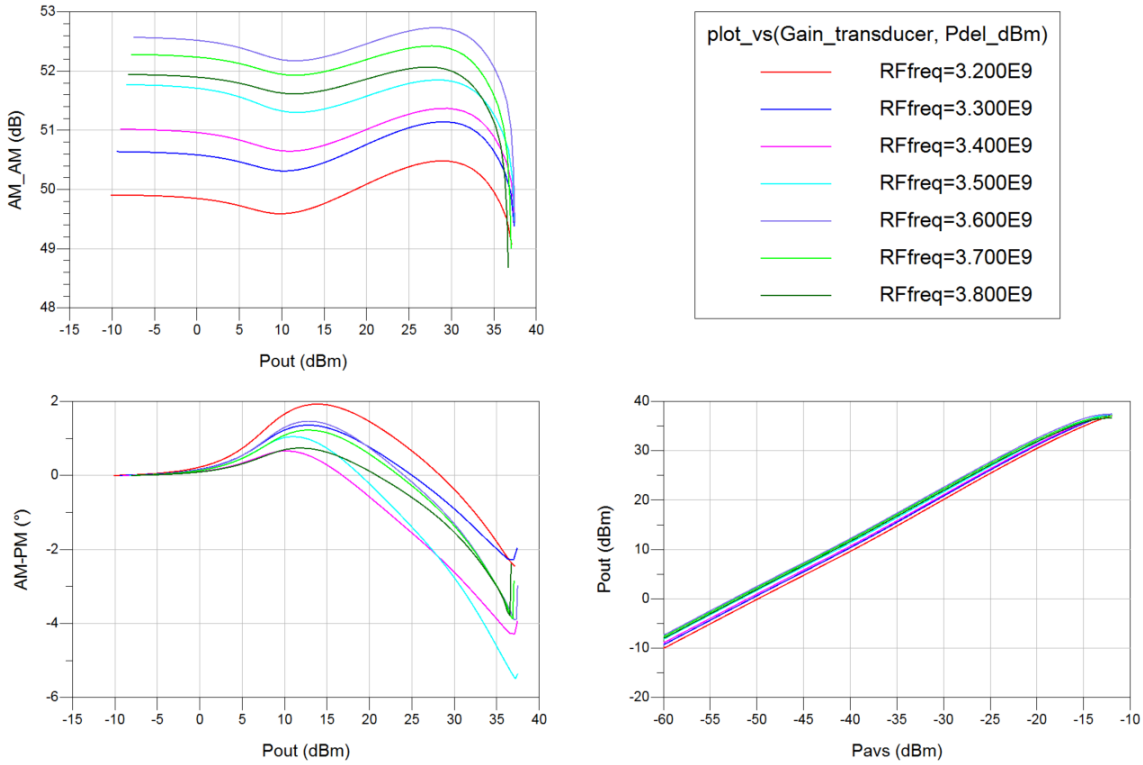



Figure 4.4: The large signal simulation results for the shielded multi-stage power amplifier, including AM-AM, AM-PM, and Pout.

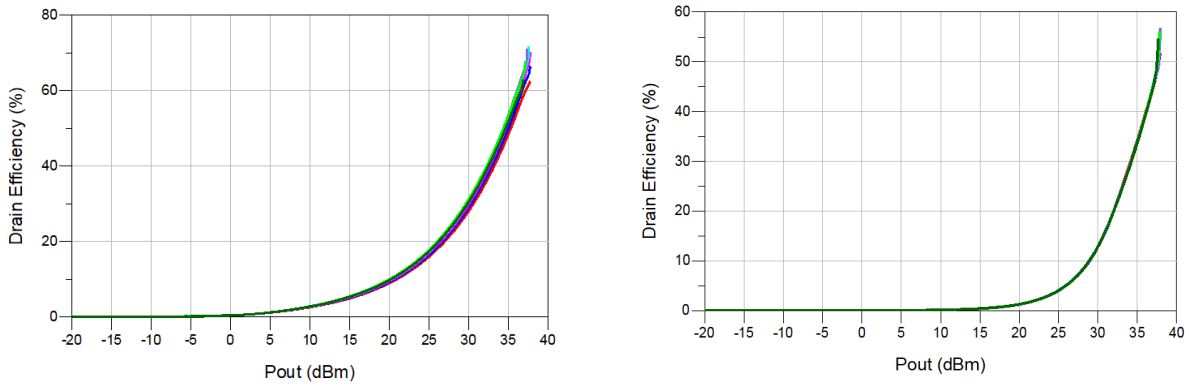
### 4.1.5 Thermal Analysis

One of the most significant challenges for the 4×4 front end is the heat generated during operation, which is predominantly dissipated by the PAs. Although the pre-drivers and other ICs that are not RF-related contribute to the overall thermal load, the majority originates from the PAs. Heat sinks can be employed to cool the system under forced convection, which may be provided by fans. The heat sinks should be mounted to the underside of the metal base interfaced beneath the PCB, to ensure both effective electrical grounding and thermal dissipation.

In selecting a heat sink, the thermal resistance, $\theta$, is the most critical parameter, alongside the physical size constraints. Thermal resistance characterizes the temperature rise resulting from heat flow, expressed as:

$$\theta = \frac{\Delta T}{P_{tot}}. \tag{4.5}$$

The power dissipated by the PAs can be inferred from the drain efficiency curves, as these effectively represent the DC power consumed relative to the delivered RF power. For the remaining ICs, the required dissipation values are provided in the respective data sheets. It is more reasonable to consider the PAs operating in their average power regions rather than at peak power. The drain efficiency curves indicate that an 8 dB back-off corresponds to an output power of 29.5 dBm for the PA stage and 22 dBm for the driver stage. These values correspond to DC power dissipations of 3.2 W and 7.5 W, respectively. The total dissipation due to the other ICs on the PCB adds approximately 3.5 W. Therefore, the total power dissipation, $P_{tot}$, is 14.2 W. Assuming a room temperature of 25°C, the maximum allowable PCB temperature to avoid significant performance degradation is approximately 70°C. This implies a required $\theta$ of 3.17 °C/W. A market search identified a suitable heat sink, APF30-30-13CB, with an area of 3×3 cm and a thermal resistance of 2.7 °C/W under forced convection at 200 LFPM.




(a) (b)

Figure 4.5: Drain efficiency curves for the (a) PA-stage and the (b) driver-stage.

### 4.1.6 Extension to 4x4 Front End

Having established that the multi-stage amplifier operates as intended for a one-channel design, the next step is to extend the design to a 4-channel module. Two approaches for achieving this extension are considered. The first method involves extending the PCB

itself to implement four one-channel designs on a single board. This extension would likely require additional digital control circuits to be integrated alongside the 4×1 PCB to control the drain and gate biases, adding complexity to the circuit. This approach would result in an electrically connected 4×1 PCB.

The second option is to mechanically combine four separate one-channel PCBs into a single frame, thereby achieving the 4×1 extension. This method offers advantages over the electrically connected design, primarily by providing easier debugging for the system. Specifically, if there is an issue with one of the one-channel modules, it can simply be replaced without impacting the others.

To mechanically connect the PCBs and form a 4×1 configuration, a tray is designed. The tray is structured to ensure that the heat sinks, which are attached beneath the metal bases, are not misaligned level-wise. This is achieved using a grill-like structure, as shown in Figure 4.6. The metal bases attached to the individual PCBs incorporate a dented structure, which acts as a docking mechanism onto the horizontal crossbars.

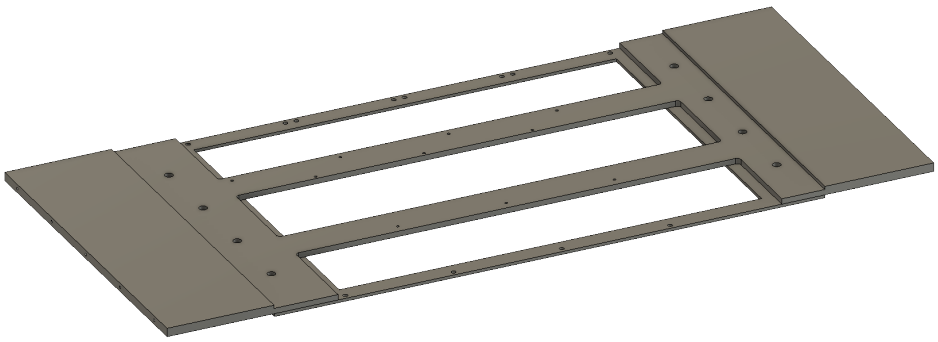


Figure 4.6: Trimetric view of an empty tray which will be the common base for the 4x1 FE module.

The tray uses screws to secure the one-channel modules to its structure. This provides an easily accessible method to reconfigure the tray if necessary. Moreover, the same screws

will also be used to mount the shield onto the PCB at the very corners. These screw holes are located along the front and back edges of the tray, as shown in Figure 4.6. In the same figure, it can also be seen that the left and right edges have additional screw holes, which are necessary to stabilize the tray within the 16-channel frame.

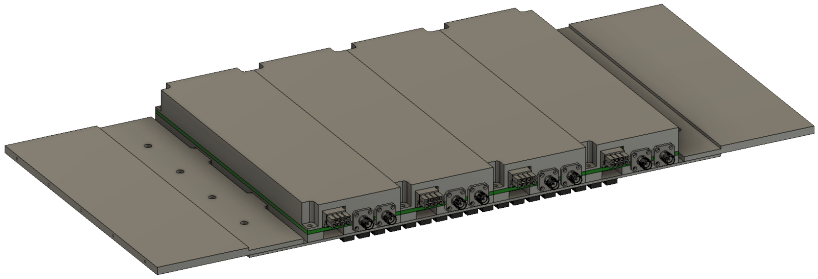


Figure 4.7: Trimetric view of a tray populated with shielded multi-stage PAs.

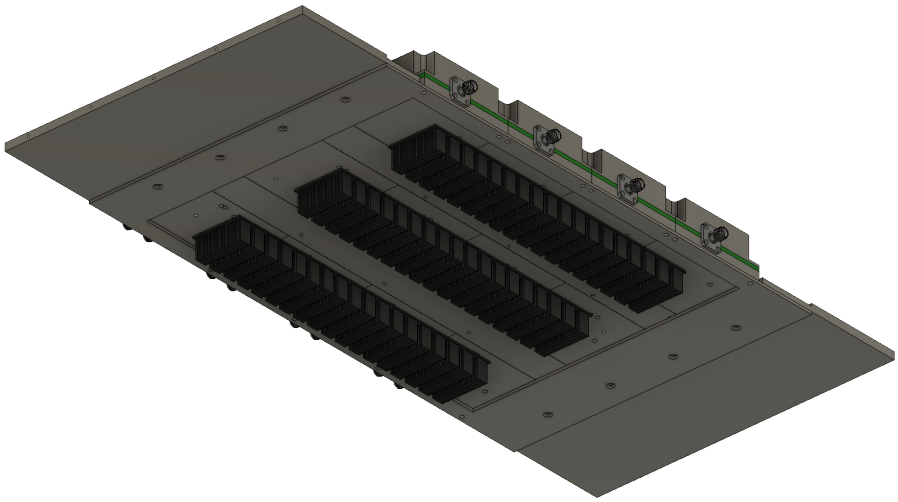


Figure 4.8: Underside of a tray populated with shielded multi-stage PAs, displaying the attahced heatsinks.

The frame that is to be used for housing all 16-channel is given in Figure 4.9. It is the same frame that was used in [10].

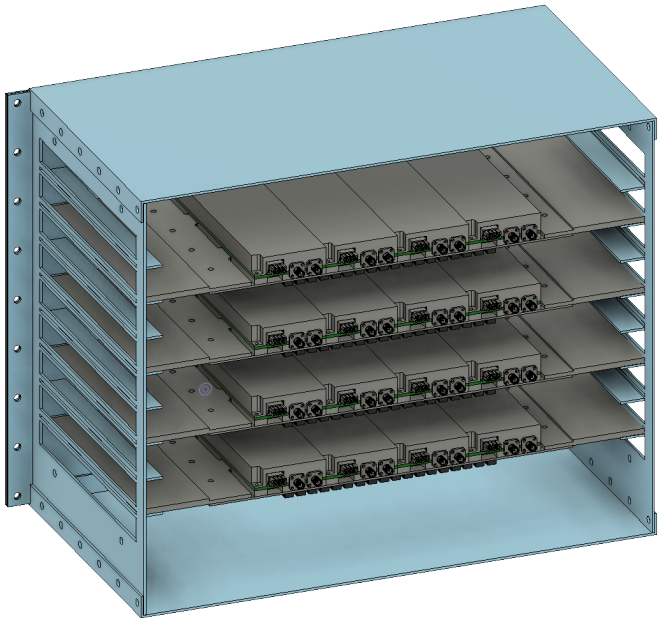


Figure 4.9: The populated trays shelved inside the frame for the 16-channel FE.

# Chapter 5

# Conclusions and Future Work

## 5.1 Conclusions

The upcoming standard for 5G wireless communication necessitates significant advancements in the transmitter front end compared to previous generations. Notable developments include the use of hundreds of elements, which implies that the PAs must be significantly more compact, and the absence of isolators between the PA and the antenna, leading to mismatch issues. These changes directly influence the performance requirements of the PA. To meet these demands, the PA must demonstrate high linearity to mitigate memory effects and signal distortion, while maintaining high efficiency. Due to the compact structure, PAs are also susceptible to crosstalk in the form of EMI, which can lead to substantial performance degradation.

To address these challenges, a literature review was conducted to assess recent advancements in PA design for sub-6 GHz transmitters and to evaluate their performance in MIMO systems. The review revealed that much of the current work emphasizes improving OBO efficiency through complex load modulation schemes, often at the expense of linearity. While enhancing efficiency is a valid objective, heavy reliance on DPD to compensate for nonlinearities introduces additional complications. Moreover, crosstalk between PAs has been identified as a critical issue in large array architectures. Given these considerations, this study proposes the design of a multi-stage Class AB PA to evaluate both its linearizability and the potential performance enhancements enabled by RF shielding.

The multi-stage PA is realized by cascading three stages: pre-driver, driver, and PA-stage. The PA-stage was designed with a focus on balancing linearity and efficiency. CW

simulations of the PA-stage alone achieved an output power of 37.5 dBm under 3 dB gain compression across the 3.2–3.8 GHz frequency range. Under the same conditions, the PAE ranged from 54% to 61%, and the $OP_{1dB}$ was 36.5 dBm. The AM-PM profile exhibited a nonlinear curve with a minimum at -4° at peak power, which remained within a linearizable range. This was confirmed through modulated signal testing using a 100 MHz OFDM waveform with 8 dB PAPR, yielding an original ACPR of -35 dBc, which improved to -55 dBc with SISO DPD. Together with the other stages, the Class AB PA was able to deliver the 50 dB gain specified in the design requirements, without compromising the $OP_{1dB}$. However, the AM-PM distortion exhibited a 2° deterioration, with the minimum shifting to -6° at peak power.

To maintain a compact form factor suitable for the 4×4 mMIMO transmitter frame, an existing pre-driver stage was integrated, eliminating the need for bulky driver amplifiers. A custom RF shield was also designed to enclose the entire one-channel PCB, segmented into three compartments—one for each stage—to suppress interstage EMI. The shielding effectiveness was evaluated using the Schelkunoff criteria, and CW simulations confirmed that the shield does not adversely affect the PA's performance. Finally, four one-channel shielded PCBs were mechanically integrated onto a single tray to form a four-channel assembly, comprising one-quarter of the complete 16-channel transmitter system.

## 5.2 Future Work

The current design offers several opportunities for improvement. One of the most notable enhancements would be to transition from the existing Class AB topology to a balanced Class AB configuration. This modification would be valuable, as balanced PAs are inherently more resilient to load mismatch effects. A more ambitious—and potentially controversial—improvement would be the implementation of an LMBA architecture. LMBAs combine the benefits of load modulation with the inherent robustness of balanced operation, offering both mismatch tolerance and enhanced back-off efficiency. However, this approach introduces challenges. LMBAs are inherently nonlinear devices, which would further burden the DPD to correct distortion. Although effective, this correction comes at the cost of increased computational complexity and power consumption on the DPD side, potentially offsetting the efficiency gains.

In terms of mitigating EMI, improvements could be made to the shielding structure. The current design covers only the top portion of the PCB, leaving the sides exposed, which may allow undesired EM radiation. Extending the shield to enclose the edges would improve EMI suppression. Additionally, incorporating EMI filters and replacing aluminum

with copper as the shielding material could yield further benefits. Although copper does not significantly alter the electrical shielding performance, it offers superior thermal conductivity, enabling more efficient heat dissipation. If the shield can be thermally connected to a grounded metal base, the additional copper mass would enhance thermal management, especially in scenarios involving higher-power transistors.

Another area for improvement lies in the transmitter front-end control. Integrating a digital control circuit, driven by a PA control IC, would introduce several quality-of-life enhancements. This setup would enable digital control of the pre-driver attenuator and allow bias voltages to be managed through the control IC. The IC could be interfaced with an FPGA, reducing the system's reliance on external DC power supplies and improving overall integration and automation of the transmitter front-end.

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